Loughborough University

Pilkington Library

Author/Filing Title ....LI, DEZHI..............

....

Vol. No. .... Class Mark ....T...............

Please note that fines are charged on ALL overdue items.

FOR REFERENCE ONLY

0403177375

PROPERTIES AND BEHAVIOUR OF PB-FREE SOLDERS IN FLIP-CHIP SCALE SOLDER INTERCONNECTIONS

By

Dezhi Li

A doctoral thesis
Submitted in partial fulfilment of the requirement for the award of
Doctor of Philosophy of Loughborough University

© by Dezhi Li, August 2005

Loughborough
University
Pilkington Library

Date JAN 2006

Class T

Acc
No. 0403177375

ABSTRACT

Due to pending legislations and market pressure, lead free solders will replace Sn-Pb solders in 2006. Among the lead free solders being studied, eutectic Sn-Ag, Sn-Cu and Sn-Ag-Cu are promising candidates and Sn-3.8Ag-0.7Cu could be the most appropriate replacement due to its overall balance of properties. In order to garner more understanding of lead free solders and their application in flip-chip scale packages, the properties of lead free solders, including the wettability, intermetallic compound (IMC) growth and distribution, mechanical properties, reliability and corrosion resistance, were studied and are presented in this thesis.

Electroless nickel (EN) without an immersion gold (Au) coating was used as the under bump metallization (UBM) in the chips studied, in order to avoid the formation of $AuSn_4$ IMCs. The wettability of EN coatings with lead free solders was studied by means of a wetting balance tester, and the results showed that with the assistance of a strong flux and nitrogen protection EN coatings maintained good wettability with lead free solders after long periods of storage. Microstructure analysis and shear tests showed that the Sn-Ag-Cu solder bumps on EN UBM had good adhesion strength.

Results from reflow and thermal ageing have shown that for the Sn-Ag-Cu/EN solder bumps the IMC behaviour was quite different from that of Sn-Pb solder. Large Ag_3Sn IMCs broke up into small parts and then coarsened during high temperature ageing. Kirkendall voids formed at the bottom of Ni_3P layer during ageing at 150 and 175°C. The shear strength degradation during ageing was caused by the coarsening of Ag_3Sn IMC.

The micro-mechanical properties of different phases in solder joints were studied using nanoindentation. These results were useful for understanding the toughness and reliability of solder joints and could also be used in finite element modelling (FEM).

Thermal cycling results showed that when immersion Au was used as the surface finish on a printed circuit board (PCB), the solder joints on the pads with a micro-via had the poorest reliability and the solder joints on bare pads exhibited good reliability. The

deformation of a PCB during reflow can also greatly reduce the reliability of solder joints. Potentiodynamic polarization tests showed that Sn-3.5Ag, Sn-0.7Cu and Sn-3.8Ag-0.7Cu lead free solders have better corrosion resistance than Sn-37Pb in 3.5%NaCl solution.

Keywords: Chip-scale package; Flip-Chip; Lead free solders; Intermetallic Compounds; Under Bump Metallization; Micro-mechanical properties; Reliability; Corrosion resistance; Nanoindentation; Kirkendall voids; Thermal cycling; Shear test

To my family, for their unconditional support

To my wife Lilly, for her deepest love and continuous encouragement

ACKNOWLEDGEMENT

The author would like to express his sincere gratitude to Professor Paul P. Conway and Dr. Changqing Liu for their invaluable instructions, advices and encouragement throughout the research as supervisors.

The author would also like to acknowledge Dr. David A. Hutt for his suggestions and assistance in experiments and paper preparation and Dr. Mike Hendriksen, Dr. Rob Horsley, Dr. Gavin Jackson, and Dr. Frank Frimpong in Celestica Limited for the help with solder assembly, shear tests and thermal cycling.

Dr. Rebecca L. Higginson, Dr. Geoff D. Wilcox, Mr. John S. Bates, Dr. Keming Chen and Mr. Soran Birosca from Institute of Polymer Technology and Materials Engineering have provided great support in the EBSD analyses and potentiodynamic polarization tests and all their work is appreciated.

Deep gratitude is expressed to Mr. Andy P. Sandaver for his continuous help in sample preparation and analyses and to Dr. Senlin Zheng for his assistance in nanoindentation tests.

The author wishes to thank all the members of InterConnection Group (ICG) in Wolfson School and friends in Loughborough for their help and knowledge.

The author wants to take this chance to thank the financial support of department scholarship for the PhD study and funding from Engineering and Physical Science Research Council Innovative Manufacturing and Construction Research Center at Loughborough University for the research project.

Finally, the author wants to express his deepest gratitude to his parents for their understanding and continuous assistance during all the years of his formal education and his sincere acknowledgement to his wife for her unrelenting support.

Table of content

ABSTRACT ... I
ACKNOWLEDGEMENT ... IV
Table of content ... V
List of figures ... X
List of tables ... XIX
Glossary of symbols ... XXI
Context of the Research ... 1
CHAPTER 1 Electronic Packages ... 4
CHAPTER 2 Under Bump Metallization and Solder Bumping ... 8
2.1 Electroless Ni UBM process ... 8
2.1.1 Electroless Ni plating mechanism ... 9
2.1.2 Working mechanism of stabilizer ... 10
2.1.3 Stress in electroless Ni coating ... 11
2.1.4 Challenges for electroless Ni in wafer bumping ... 12
2.2 Solder bumping process ... 14
2.2.1 Solder dipping ... 14
2.2.2 Stencil printing ... 15
2.2.3 Evaporation plating ... 18
2.2.4 Electroplating ... 19
CHAPTER 3 Lead Free Solder Alloys ... 21
3.1 The rationale for the development of lead free solders ... 21
3.2 The properties of lead free solders ... 23
3.2.1 Solder alloy cost ... 23
3.2.2 Microstructure and composition of bulk solder alloys ... 23
3.2.3 Melting temperature ... 28
3.2.4 Wetting ability ... 30
3.2.5 Thermal properties ... 33

3.3 Sn whisker....34
CHAPTER 4 Nanoindentation....36
4.1 Introduction....36
4.2 Initial idea of nanoindentation....36
4.3 Indenter area function....38
4.4 Stiffness measurement....39
4.5 Current analysis method....40
4.6 Implementation of the method....44
4.6.1 Choice of indenter geometries....44
4.6.2 Measurement of the initial unloading stiffness....45
4.6.3 Determination of load frame compliance and diamond area function....46
CHAPTER 5 Experimental Programme....50
5.1 Introduction....50
5.2 Under bump metallization - Electroless Ni plating....52
5.3 Wettability testing....54
5.3.1 Storage effects on wetting and wetting environment specification....54
5.3.2 Surface roughness effects on wetting....55
5.4 Stencil printing....56
5.5 Reflow....57
5.6 Assembly and underfill....58
5.7 Thermal ageing and thermal cycling....60
5.8 Interfacial reactions between different solders and substrates....63
5.9 Solidification with different cooling media....64
5.10 Shear tests....65
5.11 Nanoindentation tests....67
5.12 Corrosion tests....70
5.13 Analysis techniques....71
5.13.1 SEM, EDX and EBSD....71
5.13.2 X-ray photoelectron spectroscopy....71
5.13.3 X-ray diffraction....71
5.13.4 Atomic force microscopy....72
CHAPTER 6 Results....73
6.1 Wettability of electroless Ni with lead free solders....73
6.1.1 Wettability with different storages....74

6.1.2 Wettability with different substrate roughness 79
6.2 Microstructures of lead free solders 81
6.2.1 Microstructures of bulk solders 81
6.2.2 Microstructures with different cooling media 82
6.2.3 Morphologies and distributions of IMCs Sn-Ag-Cu solder joints 89
6.3 IMC growth during reflow processes and thermal ageing 93
6.3.1 Thermal ageing at 80°C 93
6.3.2 Thermal ageing at 150°C 96
6.3.3 Thermal ageing at 175°C 97
6.4 IMCs formed with different solders and substrates 99
6.4.1 Compositions and microstructures of IMCs 99
6.4.2 Morphology of IMCs 106
6.5 Micro-mechanical properties 110
6.5.1 Mechanical properties of ASH solder bumps 112
6.5.2 Mechanical properties of ASH solder joints after assembly 113
6.5.3 Mechanical properties of phases formed in long-time reflow 117
6.5.4 Mechanical properties of bulk solders with different cooling media 122
6.6 Creep properties 126
6.6.1 Creep property of solder joints 127
6.6.2 Creep property of bulk solders 130
6.7 Shear strength of ASH solder bumps after thermal ageing 133
6.8 Reliability 136
6.9 Corrosion properties 139
6.9.1 Potentiodynamic polarization curves 139
6.9.2 Microstructures of corrosion products 145
CHAPTER 7 Discussion of Results 146
7.1 Wettability of electroless Ni with lead free solders 146
7.1.1 Influence of flux and wetting environment 146
7.1.2 Influence of oxygen concentration 149
7.1.3 Influence of storage 151
7.1.4 Influence of substrate roughness 154
7.2 Microstructure of lead free solders 156
7.2.1 Influence of cooling media 156
7.2.2 Morphology and distribution of IMCs in Sn-Ag-Cu solder joints 158

7.3 Interface reactions 161
7.3.1 IMCs formed in the solder bumps 162
7.3.2 IMC growth 165
7.3.3 Formation of Kirkendall voids 169
7.4 IMCs formed with different solders and substrates 172
7.4.1 Growth and thickness of IMCs 172
7.4.2 Cracks in the IMCs 174
7.4.3 Formation of Kirkendall voids 175
7.5 Micro-mechanical properties 176
7.5.1 Influence of assembly and ageing 176
7.5.2 Influence of testing temperatures 177
7.5.3 Pile-up and sink-in during nanoindentation 177
7.5.4 Influence of cooling media 181
7.6 Creep properties 181
7.7 Shear strength of ASH solder bumps 184
7.7.1 Influence of shear parameters on the shear force 186
7.7.2 Influence of cooling rate 189
7.7.3 Influence of thermal ageing 190
7.8 Thermal cycling and reliability 193
7.9 Corrosion properties 199
CHAPTER 8 Conclusions and Future Work 207
8.1 Wettability of EN coatings with lead free solders 209
8.2 Microstructures of lead free solders 210
8.3 Interface reactions 210
8.4 IMCs formed with different solders and substrates 211
8.5 Micro-mechanical properties 212
8.6 Creep properties 212
8.7 Shear strength 213
8.8 Thermal cycling and reliability 213
8.9 Corrosion properties 214
8.10 Suggestions for future work 214
8.10.1 Influence of size, morphology and distribution of Ag_3Sn IMCs 214
8.10.2 Influence of surface finishes and pad size 215
References 218

Appendix 1 Gerber files of MT030 test board A1
Appendix 2 Publications A5

List of figures

Fig. 1-1 Application and development trend of IC packages ... 5
Fig. 1-2 Size and weight comparison of several IC packages ... 7
Fig. 2-1 Process route for electroless Ni bumping on Al pads ... 9
Fig. 2-2 Process of zincating for electroless Ni bumping on Al pads ... 9
Fig. 2-3 Different diffusion mechanism for different micropad arrays, a) and b) linear diffusion, c) non-linear diffusion ... 13
Fig. 2-4 Stencil printing process for wafer bumping ... 15
Fig. 2-5 Fishbone diagram for stencil printing ... 16
Fig. 2-6 IBM's well-known evaporation wafer-bumping process ... 18
Fig. 2-7 Electroplated solder wafer-bumping process ... 19
Fig. 3-1 Sn-Zn phase diagram ... 24
Fig. 3-2 Sn-Ag phase diagram ... 24
Fig. 3-3 Sn-Cu phase diagram ... 25
Fig. 3-4 Sn-Bi phase diagram ... 25
Fig. 3-5 Typical solidification microstructure of eutectic Sn-Pb solder, a) lamellar microstructure formed by slow cooling, b) fine equiaxied microstructure formed by rapid cooling ... 26
Fig. 3-6 Microstructure of eutectic Sn-Bi ... 27
Fig. 4-1 A schematic diagram of a section through an indentation showing various quantities used in the analysis ... 41
Fig. 4-2 A schematic diagram of load and displacement curves showing quantities used in the analysis as well as a graphical interpretation of the contact depth ... 42
Fig. 4-3 The peak load stiffness of a 120 mN indentation in tungsten computed using linear and power law fitting of different proportions of the unloading data ... 45
Fig. 5-1 Geometry of ASH wafer ... 50

Fig. 5-2 Schematic structure of solder bump after reflow 51
Fig. 5-3 Sn-Ag-Cu solder joint formed on the pad with micro-via 52
Fig. 5-4 RPS 6-SIGMA Wetting Balance Tester..54
Fig. 5-5 DEK 265 stencil printing machine..56
Fig. 5-6 T-Track reflow oven..57
Fig. 5-7 Lead free reflow profile...58
Fig. 5-8 Karl Suss FC6 assembly machine..59
Fig. 5-9 FineTech Electronic pick and place machine.......................................59
Fig. 5-10 MT030 board assembled with ASH chips..61
Fig. 5-11 CTS thermal cycling machine...61
Fig. 5-12 Temperature profile of thermal cycling..62
Fig. 5-13 Solder joints subjected to shear strain during thermal cycling due to CTE mismatch between the Die (α_1), the solder (α_2) and the substrate (α_3)........65
Fig. 5-14 Dage Series 400 Bondtester...66
Fig. 5-15 Micro Materials NanoTest 600 nanoindentation...................................67
Fig. 5-16 Schematic diagram of nanoindentation...68
Fig. 6-1 Microstructure of an Al substrate after zincate pre-treatment..................74
Fig. 6-2 Microstructure and morphology of an EN coating..................................74
Fig. 6-3 The oxygen concentrations with different nitrogen flow current................75
Fig. 6-4 The maximum wetting force and time to wet of EN coatings in Sn-Ag-Cu solder during the storage in lab ambient...75
Fig. 6-5 The maximum wetting force and time to wet of EN coatings in Sn-Ag-Cu solder during the storage in freezer...76
Fig. 6-6 The maximum wetting force of EN coating in Sn-Ag solder without nitrogen protection during the storage in ambient environment and freezer.............76
Fig. 6-7 The maximum wetting force and time to wet of EN coatings in Sn-Ag solder during the storage in lab ambient..77
Fig. 6-8 The maximum wetting force and time to wet of EN coatings in Sn-Cu solder during the storage in lab ambient..78
Fig. 6-9 The maximum wetting force and time to wet of EN coatings in Sn-Cu solder during the storage in freezer...78
Fig. 6-10 Roughness of Al coupons after different polishing before and after the electroless Ni plating in testing direction, A, perpendicular and B,

parallel to the polishing or rolling track direction....79
Fig. 6-11 Maximum wetting force of EN coatings in Sn-Ag solder with different substrate roughness and dipping direction, A, perpendicular and B, parallel to the polishing or rolling track direction....80
Fig. 6-12 Maximum wetting force of EN coatings in Sn-Ag-Cu solder with different substrate roughness and dipping direction, A, perpendicular and B, parallel to the polishing or rolling track direction....80
Fig. 6-13 Microstructure of Sn-Ag from solder bar....81
Fig. 6-14 Microstructure of Sn-Ag-Cu from solder bar....82
Fig. 6-15 Microstructure of Sn-Cu from solder bar....82
Fig. 6-16 Microstructure of ASH bump cooled in furnace....83
Fig. 6-17 Microstructure of ASH bump cooled in air....83
Fig. 6-18 Microstructure of ASH bump cooled in water....84
Fig. 6-19 Microstructure of Sn-Ag bulk solder cooled in water....84
Fig. 6-20 Microstructure of Sn-Ag bulk solder cooled in air....84
Fig. 6-21 Microstructure of Sn-Ag bulk solder cooled in a furnace....85
Fig. 6-22 Microstructure of Sn-Ag-Cu bulk solder cooled in water....86
Fig. 6-23 Microstructure of Sn-Ag-Cu bulk solder cooled in air....87
Fig. 6-24 Microstructure of Sn-Ag-Cu bulk solder cooled in furnace....87
Fig. 6-25 Microstructure of Sn-Cu bulk solder cooled in water....87
Fig. 6-26 Microstructure of Sn-Cu bulk solder cooled in air....88
Fig. 6-27 Microstructure of Sn-Cu bulk solder cooled in furnace....88
Fig. 6-28 Microstructures of Sn-Ag-Cu solder bumps after vertical cross-section and etching....89
Fig. 6-29 Morphologies of $(Cu,Ni)_6Sn_5$ and Ag_3Sn IMCs in Sn-Ag-Cu solder bumps....90
Fig. 6-30 Microstructures of Sn-Ag-Cu solder bumps after horizontal cross-section....91
Fig. 6-31 Microstructure of the same Sn-Ag-Cu solder bumps after horizontal cross-section at different level....92
Fig. 6-32 Microstructure of solder bump interface as-reflowed....93
Fig. 6-33 Microstructure of solder bump interfaces after ageing 50h at 80°C....94
Fig. 6-34 Microstructure of solder bump interfaces after ageing 440h at 80°C....94
Fig. 6-35 Microstructure of solder bump interface after ageing 750 h at 80°C....95

Fig. 6-36 Microstructure of solder bump interface after ageing 1080 h at 80°C.........95
Fig. 6-37 Microstructure of solder bump interface after ageing 2 d at 150°C............96
Fig. 6-38 Microstructure of solder bump interface after ageing 10 d at 150°C...........96
Fig. 6-39 Microstructure of solder bump interface after ageing 18 d at 150°C...........97
Fig. 6-40 Microstructure of solder bump interface after ageing 3 d at 175°C............97
Fig. 6-41 Microstructure of solder bump interface after ageing 15 d at 175°C...........98
Fig. 6-42 Microstructure of solder bump interface after ageing 30 d at 175°C...........98
Fig. 6-43 Microstructure of IMCs formed at the interface of Sn-Ag-Cu solder and different substrates..........100
Fig. 6-44 Microstructure of IMCs formed at the interface of Sn-Cu solder and different substrates..........101
Fig. 6-45 Microstructure of IMCs formed at the interface of Sn-Ag solder and different substrates..........102
Fig. 6-46 IMCs formed at the interface of a Sn-Ag-Cu/ENIG solder joint..............104
Fig. 6-47 IMCs formed in the solder of a Sn-Ag-Cu/ENIG solder joint.................104
Fig. 6-48 IMCs formed in a Sn-Ag-Cu/Cu solder joint..........105
Fig. 6-49 IMCs formed in a Sn-Ag-Cu/EN solder joint..........106
Fig. 6-50 IMCs formed in a Sn-Ag-Cu/ImAg solder joint..........107
Fig. 6-51 IMCs formed in a Sn-Ag/EN solder joint..........107
Fig. 6-52 IMCs formed in a Sn-Ag/ImAg solder joint..........108
Fig. 6-53 IMCs formed in a Sn-Cu/Cu solder joint..........108
Fig. 6-54 IMCs formed in a Sn-Cu/ENIG solder joint, a) thick IMC and b) thin IMC..........109
Fig. 6-55 Indentations of line 2 in a solder bump after ageing at 80°C for 50 h.........110
Fig. 6-56 Indentations of line 3 in a solder bump after ageing at 80°C for 50 h.........111
Fig. 6-57 Room temperature indentations and element mapping of solder joints......113
Fig. 6-58 Mechanical properties of line 2 in a solder joint at room temperature........114
Fig. 6-59 Creep indentations in Sn-Ag-Cu solder and normal indentations in Ag_3Sn IMC tested at room temperature..........114
Fig. 6-60 Nanoindentation loading and unloading curves of different phases in solder joints at room temperature..........115
Fig. 6-61 Nanoindentations across a solder joint and ageing at 150°C for 24 h........116
Fig. 6-62 Nanoindentations across a solder joint and ageing at 150°C for 80 h........116
Fig. 6-63 Indentations on Sn-Cu solder in a Sn-Cu/Cu solder joint.....................117

Fig. 6-64 Indentations on Sn-Ag solder in a Sn-Ag/EN solder joint....................118
Fig. 6-65 Indentations on Ni_3Sn_4 IMC in a Sn-Ag/EN solder joint......................118
Fig. 6-66 Indentations on Cu_6Sn_5 IMC in a Sn-Cu/Cu solder joint......................118
Fig. 6-67 Indentations on Ag_3Sn IMC in a Sn-Ag-Cu/Cu solder joint..................119
Fig. 6-68 Nanoindentation loading and unloading curves of different phases..........119
Fig. 6-69 Indentations and element mapping in Sn-Ag bulk solder
cooled in air...121
Fig. 6-70 Indentations and element mapping in Sn-Ag bulk solder
cooled in furnace...121
Fig. 6-71 Indentations and element mapping in Sn-Ag bulk solder
cooled in water..122
Fig. 6-72 Indentations and element mapping in Sn-Ag-Cu bulk solder
cooled in air...123
Fig. 6-73 Indentations and element mapping in Sn-Ag-Cu bulk solder
cooled in furnace...123
Fig. 6-74 Indentations and element mapping in Sn-Ag-Cu bulk solder
cooled in water..124
Fig. 6-75 Indentations and element mapping in Sn-Cu bulk solder
cooled in furnace...124
Fig. 6-76 Indentations and element mapping in Sn-Cu bulk solder
cooled in water..125
Fig. 6-77 Hardness of Sn-Ag, Sn-Cu and Sn-Ag-Cu lead free solders
cooled in different media...125
Fig. 6-78 Modulus of Sn-Ag, Sn-Cu and Sn-Ag-Cu lead free solders
cooled in different media...126
Fig. 6-79 Creep stress exponent of Sn-Ag-Cu solder at room temperature..............127
Fig. 6-80 Creep exponent of Sn-Cu at room temperature.................................128
Fig. 6-81 Creep curves of Sn-Ag-Cu at different temperatures..........................128
Fig. 6-82 Creep exponent of Sn-Ag-Cu at different temperatures.......................129
Fig. 6-83 Creep curves of Sn-Ag at different temperatures...............................129
Fig. 6-84 Creep exponent of Sn-Ag at different temperatures............................130
Fig. 6-85 Creep exponent of Sn-Ag solder cooled in ambient air........................131
Fig. 6-86 Creep exponent of Sn-Ag solder cooled in water...............................131
Fig. 6-87 Creep exponent of Sn-Ag solder cooled in furnace.............................132

Fig. 6-88 Creep exponent of Sn-Ag-Cu solder cooled in water 132
Fig. 6-89 Creep exponent of Sn-Cu solder cooled in water 133
Fig. 6-90 Shear force of ASH bumps after ageing at 80°C for different periods of time 134
Fig. 6-91 Shear force of ASH bumps after ageing at 150°C for different periods of time 134
Fig. 6-92 Shear force of ASH bumps after ageing at 175°C for different periods of time 135
Fig. 6-93 Microstructure of solder joints (pads with solder mask in the PCB side) after thermal cycling, a) 100 cycles, b) 500 cycles, c) 1000 cycles, and d) 1500 cycles 136
Fig. 6-94 Microstructure of solder joints (bare pads in the PCB side) after thermal cycling, a) 100 cycles, b) 500 cycles, c) 1000 cycles, and d) 1500 cycles 137
Fig. 6-95 Microstructure of solder joints (pads with micro-via in the PCB side) after thermal cycling, a) 100 cycles, b) 500 cycles, c) 1000 cycles, and d) 1500 cycles 138
Fig. 6-96 Potentiodynamic polarization curves of Sn-Ag solder in salt solution 140
Fig. 6-97 Potentiodynamic polarization curves of Sn-Ag-Cu solder in salt solution 141
Fig. 6-98 Potentiodynamic polarization curves of Sn-Cu solder in salt solution 141
Fig. 6-99 Potentiodynamic polarization curves of Sn-Pb solder in salt solution 142
Fig. 6-100 Microstructure of the corrosion products on Sn-Ag solder after the test with scanning rate 30 mV/min 143
Fig. 6-101 Microstructure of the corrosion products on Sn-Ag solder after the test with scanning rate 300 mV/min 143
Fig. 6-102 Microstructure of the corrosion products on Sn-Ag-Cu solder after the test with scanning rate 30 mV/min 143
Fig. 6-103 Microstructure of the corrosion products on Sn-Ag-Cu solder after the test with scanning rate 300 mV/min 144
Fig. 6-104 Microstructure of the corrosion products on Sn-Cu solder after the test with scanning rate 30 mV/min 144
Fig. 6-105 Microstructure of the corrosion products on Sn-Cu solder after the test with scanning rate 300 mV/min 144

Fig. 6-106 Microstructure of the corrosion products on Sn-Pb solder after the test with scanning rate 60 mV/min....145
Fig. 6-107 Microstructure of the corrosion products on Sn-Pb solder after the test with scanning rate 300 mV/min....145
Fig. 7-1 Wetting curves of EN coating in Sn-Ag-Cu solder with different fluxes and wetting environment....147
Fig. 7-2 Wetting curves of EN coating in Sn-Cu solder with different fluxes and wetting environment....148
Fig. 7-3 EN plated samples after the wettability tests in Sn-Ag-Cu and Sn-Cu solders....148
Fig. 7-4 The maximum wetting force and time to wet of EN coating in Sn-Ag-Cu solder with different nitrogen flows....150
Fig. 7-5 The maximum wetting force and time to wet of EN coating in Sn-Ag solder with different nitrogen flows....150
Fig. 7-6 The maximum wetting force and time to wet of EN coating in Sn-Cu solder with different nitrogen flows....151
Fig. 7-7 XPS spectra (normalized) of electroless Ni coating after the storage in lab for different time....152
Fig. 7-8 XPS peak of nickel after storage in air for 24 h....152
Fig. 7- 9 The relationship between apparent contact angle and true contact angle on a rough surface....155
Fig. 7-10 Cooling rate of samples cooled down in furnace....157
Fig. 7-11 Microstructure of Sn-Ag-Cu solder bumps after cross-sectioned at different level, a) top and b) bottom....159
Fig. 7-12 Morphology of $(Cu,Ni)_6Sn_5$ IMCs in solder bumps, a) top layer of IMCs and b) bottom layer of IMCs....159
Fig. 7-13 Voids formed in solder bumps near solder/EN interface....160
Fig. 7-14 SEM image and EDX mapping of solder bump interfaces after ageing 50 hours in 80°C....163
Fig. 7-15 EBSD diffraction patterns of different phases after ageing, a) Ag_3Sn, b) $(Cu,Ni)_6Sn_5$....164
Fig. 7-16 EBSD mapping of solder joint as-reflowed, a) inverse pole figure and b) phase map and image quality....164
Fig. 7-17 IMC growth during ageing at different temperatures....167

Fig. 7-18 Arrhenius plot of $(Cu,Ni)_6Sn_5$ IMC growth....................................167
Fig. 7-19 Microstructure of ASH solder bumps as reflowed and after ageing at different temperature. a) as reflowed, b) after ageing at 80°C for 750 h, c) after ageing at 150°C for 2 d, d) after ageing at 150°C for 10 d, e) after ageing at 175°C for 3 d, and f) after ageing at 175°C for 30 d................168
Fig. 7-20 Ag_3Sn IMC at the corner of the Sn-Ag-Cu solder bump.........................169
Fig. 7-21 Ag_3Sn IMC and hole in the Sn-Ag-Cu solder bump............................169
Fig. 7-22 Microstructure of IMC/EN interface in solder bump after different ageing, a) aged 2 d at 150°C, b) aged 18 d at 150°C, c) aged 3 d at 175°C and d) aged 30 d at 175°C..170
Fig. 7-23 Possible formation process of Kirkendall voids in Sn-Ag-Cu/EN solder bumps during high temperature ageing..171
Fig. 7-24 Solder joints with cracks in the IMCs after the initial polishing..............175
Fig. 7-25 Microstructure of IMCs formed at the interface of Sn-Ag-Cu solder and Cu substrates after etching...175
Fig. 7-26 AFM images of nanoindentations in different phases..........................179
Fig. 7-27 AFM section analysis of nanoindentation in Sn-0.7Cu solder................180
Fig. 7-28 AFM section analysis of nanoindentation in Sn-3.5Ag-0.7Cu solder........180
Fig. 7-29 Typical force-displacement curve of shear test.................................185
Fig. 7-30 The shear force of as reflowed ASH bumps with different shear heights...186
Fig. 7-31 Fracture surface of solder bumps as reflowed with different shear heights, a) 10 μm, b) 15 μm, c) 20 μm and d) 25 μm..........................187
Fig. 7-32 solder bump as reflowed failed at the interfaces and bulk solder (shear height 10 μm)...188
Fig. 7-33 The shear force of as reflowed ASH bumps with different shear speed.....188
Fig. 7-34 The shear force of ASH bumps with different shear heights and cooling media...189
Fig. 7-35 Fracture surfaces of solder bumps after different ageing, a) as reflowed, b) aged 45 d at 80°C, c) aged 10 d at 150°C, d) aged 18 d at 150°C, e) aged 15 d at 175°C and f) aged 30 d at 175°C (shear height 15 μm)......191
Fig. 7-36 Fracture surfaces of solder bumps after ageing at 175°C for different time, a) 3 d, b) 15 d and c) and d) 30 d. (Shear height 10 μm)................192
Fig. 7-37 Possible crack initiation positions during thermal cycling, a) sharp

points, b) joint corner and $AuSn_4$/solder interface, c) voids and joint corner, d) Ag_3Sn/solder interface, e) poor wetted area and voids and f) $AuSn_4$/solder interface......194

Fig. 7-38 Irregular solder joint shapes after reflow soldering when pads with solder mask were used, a) b) narrow neck, c) UBM lift and d) solder disconnection......195

Fig. 7-39 Failure modes of solder joints when pads with micro-via were used, a) b) failure at $AuSn_4$/solder interface, c) failure in bulk solder and d) failure at $AuSn_4$/solder interface and in bulk solder......197

Fig. 7-40 Failure mode of solder joints during thermal cycling when bare pads were used, a) failure in bulk solder and b) failure at poor wetted interface......197

Fig. 7-41 Failure mode of solder joints during thermal cycling when pads with solder mask were used: failure in bulk solder......198

Fig. 7-42 Ag_3Sn IMCs in the way of crack propagation......198

Fig. 7-43 Comparison of potentiodynamic polarization curves of different solder materials with the scanning rate 30 mV/min......201

Fig. 7-44 Comparison of potentiodynamic polarization curves of different solder materials with the scanning rate 60 mV/min......201

Fig. 7-45 EDX spectrum of different solder materials after the corrosion tests with the scanning rate 300 mV/min......203

Fig. 7-46 XRD spectra of different solder materials after the corrosion tests with the scanning rate 300 mV/min......204

Fig. 7-47 XRD spectra of Sn-Ag-Cu solder after the corrosion tests with the scanning rate 30 mV/min......205

List of tables

Table 3-1 Thermal properties of lead free solders and other electronic materials........33

Talbe 4-1 power law exponents predicted by Sneddon's analyses and the relevant geometry constants...44

Table 5-1 Formulation of electroless Ni plating solution..................................53

Table 6-1 Compositions of phases formed in the solder joint of Sn-Ag-Cu on Cu...102

Table 6-2 Compositions of phases formed in the solder joint of Sn-Ag-Cu on EN...102

Table 6-3 Compositions of phases formed in the solder joint of Sn-Ag on ENIG...102

Table 6-4 Summary of phases formed in the solder joints of different solders on different substrates...103

Table 6-5 Mechanical properties of solder bumps after ageing at 80°C for 50 h.......112

Table 6-6 Room temperature mechanical properties of phases in solder joints after assembly...114

Table 6-7 Mechanical properties of phases in solder joints after ageing at 150°C for 24 h...116

Table 6-8 Mechanical properties of phases in solder joints ageing at 150°C for 80 h...117

Table 6-9 Mechanical properties of different phases at room temperature.............120

Table 6-10 Mechanical properties of different phases at elevated temperatures........120

Table 6-11 Creep rate of lead free solders with different cooling media...............133

Table 6-12 Number of couples failed after different cycles to different type of pads...139

Table 6-13 Cycles when 1% and 50% couples failed to different type of pads........139

Table 7-1 Composition analyses of electroless Ni coating after different

storage by XPS..153

Table 7-2 Statistic data of the existing morphologies of Ag_3Sn IMC
in ASH bumps..158

Table 7-3 The IMC thickness increase of solder bumps during ageing at 80°C........165

Table 7-4 The IMC thickness increase of solder bumps during ageing at 150°C......166

Table 7-5 The IMC thickness increase of solder bumps during ageing at 175°C......166

Table 7-6 Standard electromotive force (emf) of metals used
in microelectronics..200

Table 7-7 Passivation properties of Sn-Pb and lead free solders.........................202

Glossary of symbols

A	Area
AFM	Atomic Force Microscopy
ASH	Type of wafer used
BGA	Ball Grid Array
C	Total measured compliance, Concentration
C_f	Compliance of the load frame
C_s	Compliance of the specimen
CSP	Chip Scale Packaging
CTE	Coefficient of Thermal Expansion
CuImAg	Immersion Ag on Cu
d	Thickness
D	Diffusion coefficient
d_0	Original thickness
D_0	Diffusion constant
DCA	Direct Chip Attach
DI	Deionised
E	Modulus
EBSD	Electron Back-Scattered Diffraction
EDX	Energy Dispersive analysis of X-ray
emf	Standard electromotive force
EN	Electroless Ni
ENIG	Electroless Ni Immersion Gold
E_r	Reduced modulus
FR4	Fire Retardant epoxy-fibre glass grade 4
g	Gravity acceleration
G	Shear modulus
h	Depth

h_c	Contact depth
h_f	Final depth of the residual hardness impression
h_r	Residual depth
h_s	Displacement of the surface at the perimeter of the contact
H	Hardness
IMCs	Intermetallic Compounds
J	Diffusion flux
k	Boltzmann constant
KGD	Known Good Die
k_R	Relaxation factor
n	Creep exponent, hardening coefficient
P	Load
PCB	Print Circuit Board
ppm	Piece per million
PTH	Pin-Through-Hole
Q	Activation energy
r, a	Radius
R_a	Mean roughness
RSS	Ramp-Soak-Spike
RTS	Ramp-to-Spike
S	Stiffness
SCE	Saturated Calomel Electrode
SEM	Scanning Electron Microscopy
SMT	Surface Mount Technology
t	Time
T	Absolute temperature
TCP	Tape Carrier Package
T_H	Homologous temperature
T_m	Melting temperature in Kelvin
UBM	Under Bump Metallization
XPS	X-ray Photoelectron Spectroscopy
XRD	X-Ray Diffraction
α_m	Groove steepness

β	Shape parameter in Weibull analysis
θ_0	True contact angle
θ_r	Apparent contact angle
γ	Surface tension
δ	Thickness
η	Scale parameter in Weibull analysis
σ	Stress
σ_{OB}	Orowan bowing stress
σ_{th}	Threshed stress
σ_y	Yield strength
ρ	Density
ν	Poisson's ratio
μ	Shear modulus

Context of the Research

The major trend in electronic products today is to make them smarter, lighter, smaller and faster, and in the meantime more user friendly, functional, powerful, reliable, robust, creative and inexpensive [1]. To meet the trend for miniaturization and high speed, increasing package pin counts and higher clock frequencies, i.e. more integrated electronic devices with smaller interconnection joints, are needed to satisfy market requirements. The solder joints are created by the reaction between the solder alloy and the surfaces to be joined together, through the formation of intermetallics (IMCs). Such solder joints provide the mechanical land and electrical interconnect of the product. These IMCs are often multilayered or even distributed within the solder joint. When these solder joints become smaller, intermetallics (IMCs) represent a larger volume fraction of a joint, and the interfacial reactions, mechanical properties and reliability of solder joints could be different to those found in larger joints.

Sn-Pb solders have been used in electronic packaging for a long time and Pb is a very important element in the solders, however, due to the toxicity of Pb, Sn-Pb solders are going to be banned in electronics industry. In the US, legislation to limit the use of Pb has been introduced in both Senate and the House of Representatives. Although the legislation has not been passed, it is likely that some legislation will be passed in the future. In Europe, the WEEE/RoHS Directives has been passed into legislation that will ban the use of lead in all electronic assemblies from July 2006 [3]. Legislation proposed in Japan will prohibit lead from being sent to land fills and other waste disposal sites, which means that the manufacturers either recycle the lead 100 percent or use the lead free replacements.

Manufacturers and end-users are therefore increasing concerned with the dual challenges of the progression in decreasing joint sizes and the step change arising from

the removal of Pb from the solder joint. Both these challenges affect the IMCs and microstructure of a solder joint, which in turn dictate the reliability and mechanical integrity of the solder joints and, as such, these are worthy of research to further the body of knowledge in this field.

Some lead free solder alloys have already been extensively investigated. In order to maintain or enlarge their markets, avoid trade barriers, many companies, including IBM, Compaq, Motorola, Hewlett Packard, and Sony etc., have been involved in this area and are assessing alternative alloys.

Although a lot of work has been done, there are still many problems existing for lead free solders. These include the following:

- The eutectic temperature of Sn-Pb is 183°C and most of the assembly equipment in use today is designed to operate using 183°C as a base reference. In addition, thermoset polymers are currently widely used in electronic packaging, and the highest temperature that these polymeric materials are exposed to is approximately 230-250°C for 90-120 s. So the melting temperature of lead free solders cannot be too high and needs to be close to 183°C, otherwise new production infrastructure for lead free solders, such as high glass transition temperature (Tg) polymeric materials, would need to be established.
- Possible lead free solder replacements for Sn-Pb solders are Sn-rich alloys, and their costs are higher than that of Sn-Pb.
- The interfacial reactions of lead free solders are different from those of Sn-Pb solders and different lead free solders may require different under metallurgies of the surfaces to be joined, i.e. the solder under bump metallizations (UBMs) to maintain or assure appropriate interfacial strength.
- High reflow temperatures will cause more serious Coefficient of Thermal Expansion (CTE) mismatch problems, and solder joints will be subject to more shear and tensile stresses.
- The wettability of lead free solder materials on the commercial plating finishes used on PCBs and components is not as good or as well understood as that of Sn-Pb solders.

- Many properties of lead free solder materials, such as mechanical properties, electrical properties, reliability and corrosion resistance etc., are not as well understood as they are for Sn-Pb systems.

Based on the requirements for miniaturization and application of lead free solders in flip chip scale packaging, IMC growth, shear strength, mechanical properties and reliability of small Sn-3.8Ag-0.7Cu/electroless Ni (EN) flip chip solder joints with small pitch size have been studied. In order to determine the optimum substrates or UBMs for different lead free solders, interfacial reactions between different lead free solders and different substrates were investigated. In order to derive criteria for the production and storage of EN UBM, the wettability of EN coatings with different lead free solders was tested after different storage regimes. In the mean time, the morphologies of IMCs, the influence of cooling rates on the microstructure of solders and the corrosion resistance of Sn-Pb and lead free solders were studied to improve lead free packaging processes and provide more understanding about the robustness of lead free solder joints.

In this thesis, Chapter 1 describes the background of electronic packages; Chapter 2 briefly introduces technologies about under bump metallization and solder bumping; Chapter 3 gives some properties of lead free solders; Chapter 4 reviews the development and current analysis method for nanoindentation; Chapter 5, Chapter 6 and Chapter 7 present the experiment details, research results and associated discussion, respectively; finally, Chapter 8 presents the conclusions and possible work for future research.

CHAPTER 1

Electronic Packages

In order to satisfy the requirements for the packaging of different electronic devices, many packaging technologies have been developed and they include ball grid array (BGA), thin small outline package (TSOP), small outline J-leaded (SOJ), small outline C-leaded (SOC), tape carrier package (TCP), plastic quad flat pack (PQFP), chip scale packaging (CSP), flip chip, and direct chip attach (DCA). Different technologies are required for different electronic devices and applications, and technologies can overlap, such as flip chip and CSP.

Fig. 1-1 shows the application regions of different package technologies, with different package pin counts and clock frequencies. It can be seen that area array flip chip can deliver to applications that need high performance.

The main feature of BGA is the solder ball connection with the grid array, and the substrate is not a silicon chip. The connection method within a BGA could be solder bonding or wire bonding. There are many kinds of BGA packages, and depending on their substrate technologies they include: ceramic BGA (CBGA); plastic BGA (PBGA); metal BGA (MBGA) and Tape BGA (TBGA). CBGA, MBGA, and TBGA can meet the high pin counts (>500), power, and clock frequency requirements of high-I/O and high performance application specific integrated circuits (ASICs) and microprocessors,

but at higher costs. PBGA is cost effective at package pin counts between 250 and 600 due to its low cost relative to CBGA, MBGA, and TBGA [1].

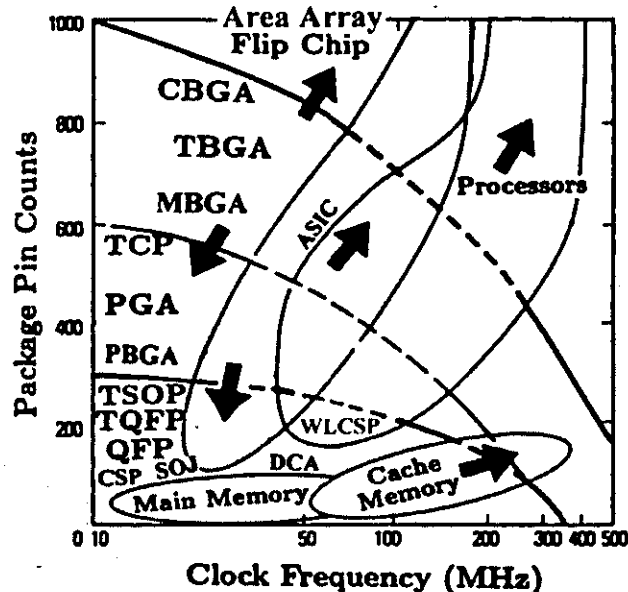


Fig. 1-1 Application and development trend of IC packages. [1]

PQFP is the most cost effective surface mount technology (SMT). It has been widely used for ASICs and low performance, low-pin-count microprocessors and sometimes cache memories. The main drawbacks for PQFP are that they are only a peripheral interconnection solution, possess relatively long lead lengths, are difficult to handle on account of their fragility and have a relatively low board-level manufacturing yield. The TSOP is a very low-profile package specially designed for static random access memory (SRAM), dynamic random access memory (DRAM) and flash memory for space-limited applications. The definition of CSP given by IPC is that the package area is less than 1.5 times that of the chip area [4]. There are many CSP technologies developed by different companies, such as: solder-bumped or wire-bonded flip chip; Fujitsu's small outline no-lead/C-lead package (SON/SOC) and bump chip carrier (BCC); NEC's fine pitch ball grid array (FPBGA); Tessera's micro-ball grid array (μBGA) and IBM's ceramic mini-ball grid array (Mini-BGA) [4]. CSP is usually used to package memory

and low power (<1W), low-pin-count (<200) ASICs. The wafer level chip scale package (WLCSP) is a new technology that adresses the problems facing DCA, i.e., the Known Good Die (KGD) issues and requirements for high density Printed Circuit Boards (PCBs). The unique feature of WLCSP is the use of a metal layer to redistribute the very fine-pitch peripheral-arrayed pads on the chip to much larger-pitch area-array pads that provide larger solder joints on the PCB. With WLCSP, the requirement for a high-density PCB is relaxed and no underfill is needed, which makes the KGD issues much simpler [1].

In comparison with the above packaging technologies, flip chip is a solution to meet the trend of electronic product development, where the chip faces down, towards the underlying substrate. There are many bonding methods applicable to a flip chip package, such as solder bonding, wire bonding, anisotropic conductive film (ACF), anisotropic conductive adhesive (ACA), anisotropic conductive paste (ACP), conductive adhesive polymer and Au stud bumps with conductive adhesive. Among them, solder bonding is the one that has been used widely due to its low price, high I/O density and good reliability.

For high-price and high-speed microprocessors and ASICs, the integrated circuit (IC) design requires very high I/O and performance packages. The development of area-array solder bumped flip chip technology satisfied this requirement. As mentioned above, CBGA, MBGA, and TBGA can meet the requirements of high-I/O and high performancc applications, so the area-array solder bumped flip chip is often packaged in a CBGA, a MBGA, or a TBGA [1].

DCA is one of the most cost-effective packaging technologies. DCA packages the chips directly to the board and has many advantages, such as high I/O density, low profile, short lead length and low weight. However, because of the infrastructure and the cost of

supplying the KGD and the corresponding fine line and space PCB, DCA is still waiting for the commensurate development of KGD and high density PCB.

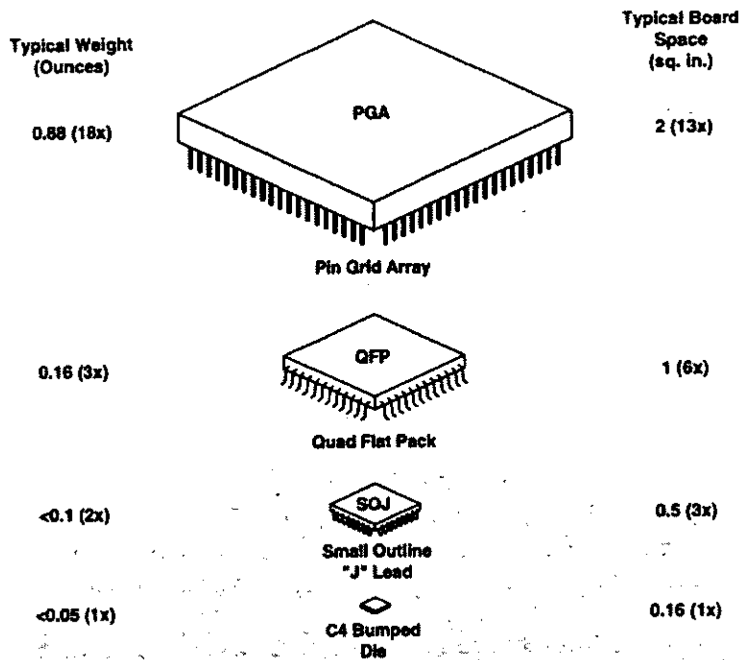


Fig. 1-2 Size and weight comparison of several IC packages. (*Source: Motorola/IBM*)

A development trend of electronic products is to make them smaller and lighter. From this point of view, flip chip is one of the best choices. Fig. 1-2 shows the size, weight and typical board space of several IC packages [5]. It illustrates that, if packaged by DCA technology, the chip (die) has the lightest weight and needs the smallest space. However, because of the mismatch of the coefficient of thermal expansion (CTE) between the silicon chip and the epoxy substrate, an underfill encapsulant is needed to increase the reliability, which is going to increase the manufacturing cost and reduce the throughput. In addition, the underfill will make rework very difficult, and as such further compound the KGD issues.

CHAPTER 2

Under Bump Metallization and Solder Bumping

Due to its advantages, including miniaturization and high input/output characteristics, flip chip technology was introduced to electronic packaging. However, by using this technology, most low cost wafer bumping methods, such as solder dipping, stencil printing, micro-punching, micro-ball mounting, and jet printing require a pre-treatment of the Al or Cu bond pads, this being known as the Under Bump Metallization (UBM). There are many UBM deposition methods that have been used, including electrolytic plating, sputter deposition and electroless plating.

2.1 Electroless Ni UBM process

During the development of semiconductor technologies, the cost of the electronics has been a critical factor. Because of its low cost and simple process route, electroless Ni (EN) is increasingly used as an UBM method.

Due to its minor doping elements, Al is the dominant material for wafer bond pad metallization. Because Al is not catalytic for EN plating, pre-treatment of the Al pad before EN plating is necessary. The Zincate treatment is a process that is used to activate the Al pads for subsequent EN plating. Zincating relies on the electrochemical reactions between zinc complexes in the solution and the Al substrate to deposit Zn particles on the Al surface at the expense of Al dissolution [6]. The typical wafer EN plating process route is shown in Fig. 2-1, and it includes pad cleaning and etching, zincating, EN plating, and immersion gold plating. Liu et al [7-9] investigated and compared the morphologies and mechanical properties of the UBMs deposited by single

and double zincating routes. The results showed that a double zincate pretreatment produced a thinner, denser and more uniform zincate layer, resulting in more uniform nucleation and growth of EN coating. For double zincating, another etching process (50% HNO_3 solution) and a further zincating step are required after the first zincating process. The zincating process is shown in Fig. 2-2.

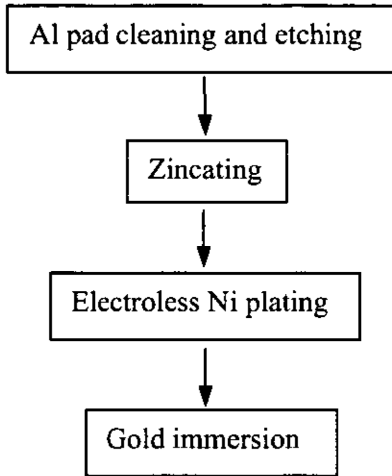


Fig. 2-1 Process route for electroless Ni bumping on Al pads.

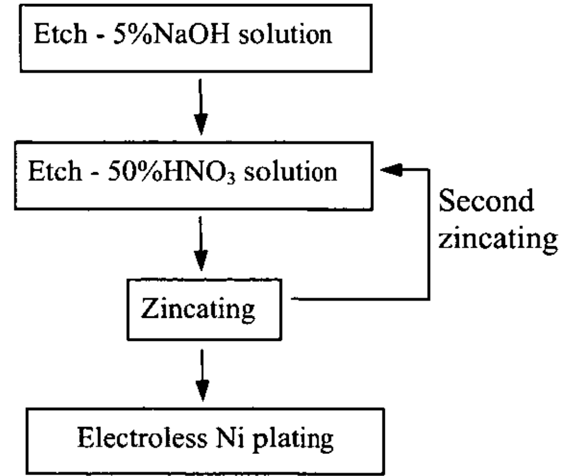
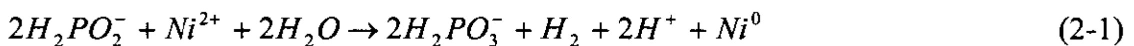


Fig. 2-2 Process of zincating for electroless Ni bumping on Al pads.

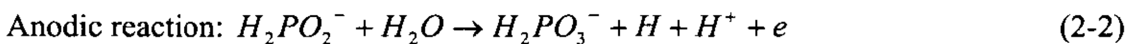
2.1.1 Electroless Ni plating mechanism

For the hypophosphite-based EN baths, the overall reaction can be written as:



$$2H_2PO_2^- + Ni^{2+} + 2H_2O \rightarrow 2H_2PO_3^- + H_2 + 2H^+ + Ni^0 \qquad (2\text{-}1)$$

From an electrochemical point of view, the reaction above can be further divided into an anodic reaction and a cathodic reaction, as below [10]:



Anodic reaction: $H_2PO_2^- + H_2O \rightarrow H_2PO_3^- + H + H^+ + e$ (2-2)

Cathodic reaction: $Ni^{2+} + 2e \rightarrow Ni$ (2-3)

As the anodic partial reaction is the electron source for the cathodic one, it is the driving force for the whole deposition process. The Ni deposition includes the diffusion towards and absorption on the catalytic surface of the reactants, the de-absorption and diffusion of products away from the surface, and the electrochemical reactions on the

surface. The Ni deposition rate is controlled by the electrode potential and catalytic activity.

The Ni deposition reactions could happen on the surface of colloid particles present in the solution when there are little or no stabilizers. As the formation of these colloid particles is uncontrollable and the Ni deposition process is autocatalytic, working EN baths may decompose spontaneously by triggering a self-accelerating chain reaction on those colloid particles. So, in practice, all working EN baths contain some kind of stabilizer to prevent such spontaneous decomposition. Pb salts were initially used as the stabilizer; however, due to the toxicity of Pb, thiourea and other lead-free chemicals were chosen.

The absorption of stabilizer ions on a catalytic surface blocks the catalytic sites from being used for the absorption of the reactants, and thus impedes the deposition process. When the surface density of absorbed stabilizer ions reaches a certain level, the deposition process could be completely inhibited. As the concentration of the stabilizer in bulk solution is usually in the order of *ppm*, unlike the absorption of reactants, the absorption of the stabilizer is diffusion-controlled. [10]

2.1.2 Working mechanism of stabilizer

If the active surface is a large surface, and the concentration gradient of the stabilizer in the vicinity of the surface is laminar, the diffusion of the stabilizer is a linear diffusion with the diffusion flux perpendicular to the surface. Following Fick's first diffusion law:

$$J = -D(\frac{dc}{dx}) \tag{2-4}$$

the diffusion flux can be expressed by equation:

$$J = D(C_0 - C_S)/\delta \tag{2-5}$$

Here D, C_0, C_s and δ stand for the diffusion constant, the concentration in the bulk solution, the concentration on the absorbed surface and the thickness of the diffusion layer, respectively. In the absence of forced convection, the value of δ is usually in the order of 100 μm. Linear diffusion exists only when the dimension of the active surface is large enough compared to the diffusion layer, so the boundary effect can be neglected.

But when the dimension of an active surface approaches the value of δ, the boundary effect is no longer negligible. In this condition, the diffusion is controlled by a non-linear diffusion mechanism as below [10]:

$$J' = 4D(C_0 - C_S)/(\pi r) \qquad (2\text{-}6)$$

Where r is the radius of a circular surface. It can be seen from above equation that for non-linear diffusion, the smaller the active surface, the larger the diffusion flux. Fine particles of colloid are subject to non-linear diffusion, and thus can absorb much more stabilizer. As a result, their catalytic activity is poisoned and hence the spontaneous decomposition of the bath is inhibited. On the other hand, large surfaces ($r >> \delta$), as they are subject to linear diffusion, maintain a much lower surface density of absorbed stabilizer and thus remain catalytic for Ni deposition. During deposition, the Ni deposits can also bury the stabilizer, so the dynamic density of absorbed stabilizer is the net result of two opposite actions: the absorption from the bulk solution by diffusion and the burying by Ni deposition [10]. Research [11, 12] also shows that the addition of thiourea stabilizer can decrease the phosphorus content of EN coating.

2.1.3 Stress in electroless Ni coating

The stress in EN coating can come from two sources: the mismatch of the coefficient of thermal expansion (CTE) between the substrate and the EN coating and the coating growth. The stress caused by the coating growth is called intrinsic stress.

When EN coating is used as the UBM in electronic packaging, the plating substrates are Al or Cu. Because their CTEs are higher than that of EN coating, during the cooling of the samples from deposition temperature, e.g. 85°C, to room temperature, compressive stress will form inside the coating and tensile stress in the substrates.

The intrinsic stress is connected to many factors during deposition, such as phosphorous (P) content in the coating, bath pH value, working life of the solution and heat treatment. When the P content is reduced or the pH value increases, the intrinsic stress in the coating will change from compressive stress to tensile stress [13-15]. With the ageing of the plating solution, the intrinsic stress will increase, which is related to the concentration increase of HPO_3^{2-} during the working life of the plating solution [13, 14].

When an EN coating is annealed around 400°C, the amorphous coating will transfer into a crystalline Ni_3P, and the coating will shrink, due to the smaller volume of Ni_3P [13]. This means that, if there is a compressive stress in the coating before annealing, the stress will decrease, and likewise if there is a tensile stress before annealing, the stress will increase. So whether annealing is needed or not, and what kind of parameters are going to be used is worth careful consideration before application.

Stress will increase with the growth of an EN coating. Compressive stress can benefit the adhesion of the EN coating to the substrate; however, a high level of tensile stress will induce cracks and lead to adhesion failure [13, 16].

2.1.4 Challenges for electroless Ni in wafer bumping

In the process of EN bumping, the zincate pretreatment and EN plating steps are the most critical steps to ensure high quality products. Although EN plating had been used for many decades in metal plating industry, when it was introduced as a bumping method it presented many challenges, and its application in wafer bumping is still relatively in its infancy and detailed studies and information are lacking. Because the Al pads are thin and small, approaching or even less than the thickness of the diffusion layer (about 100 μm), when commercial EN plating solution are used in pad bumping, it can cause many faults, such as missed plating, due to non-linear diffusion.

If a group of pads were distributed to form an array, depending on the pitch and size of the array, both linear and non-linear diffusion is possible [17], as illustrated in Fig. 2-3. If the dimension of the active surface is much larger than the thickness of the diffusion layer, the boundary effect can be negligible, and the individual diffusion zones of two adjacent pads can overlap, so that the discrete pads mimic a continuous area and thus behave like linear diffusion. If the dimension of the active surface is not large enough and so the boundary effect can't be negligible, then non-linear diffusion will take place. The results from Zhang et al [10] showed that when the active surface coverage was larger than 20%, the deposition was linear diffusion and, when the active surface coverage was less than 10%, it was non-linear diffusion and, when the coverage was

between 10% and 20%, it depended on marginal conditions, such as the local agitation caused by the bubbling of evolved hydrogen.

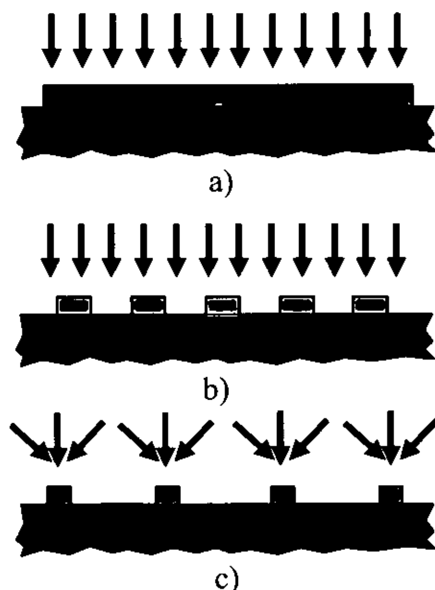


Fig. 2-3 Different diffusion mechanism for different micropad arrays, a) and b) linear diffusion, c) non-linear diffusion.

The non-linear diffusion of the stabilizer ions in the bulk solution could significantly increase the mass transfer towards the pads. Because the surface density of the stabilizer ions on a continually growing surface is the net result of two opposite actions, as mentioned above, the non-linear diffusion leads to a higher surface density of the stabilizer ions. The absorbed stabilizer ions occupy the surface sites required for the deposition of the reactants and thus impede the deposition rate of Ni, which in turn reduces the stabilizer ions burying rate by Ni deposition. This is a positive feedback, and it could easily lead to a quick cessation of local Ni deposition. As a result, in the wafer UBM process, Ni will not be able to plate on some small pads, which will result in poor solderability in the subsequent solder bumping and will lead to the 'missing bump' problem.

During the EN plating on wafer pads, when one big pad is connected with one small pad, both of the two pads can be plated well, which is caused by potential pinning. The term '*potential pinning*' means that when two or more surfaces are electrically interconnected, they will share the same plating potential. Van der Putten and de Bakker [17]studied the effect of potential pinning in their work. They attributed the result of potential pinning purely as a galvanic effect. They argued that when a micropad was

spatially isolated but electrically interconnected with a large surface, non-linear diffusion of stabilizer toward the micropad would stop the local electroless process completely; the nickel deposition on the micropad was purely caused by galvanic effects, i.e., the micropad relied on the large surface for its electron supply. However, the study of Zhang et al [10] argued that the benefit of potential pinning was not a constant electron flow from the large surface to the small surface. They thought that at the beginning of plating there were some electrons flowing from the large surface to the small surface, at this time the large surface acted as a trigger, so the small surface could begin plating, and once the plating took place on the small surface, the plating on the small surface became self-supporting.

2.2 Solder bumping process

Wafer bumping is the heart of solder-bumped flip-chip technology. Today, there are many different techniques to put tiny solder bumps (usually no larger than 100 μm in diameter) on a wafer, including evaporation plating, electroplating, solder dipping, stencil printing, and solder jet printing. The most important task in solder bumping is to put a controlled volume of solder materials on the pads or UBMs, so they can act as connection materials during assembly with other chips or the PCB.

2.2.1 Solder dipping

Solder dipping is a cheap solder bumping method when coupled with a UBM. The process for solder dipping contains 3 steps and is very simple. The first step is to deposit a layer of UBM on the Al or Cu pads; the second step is to dip with flux and solder; and the last step is to reflow the solder to create uniform bumps. The wafer is dipped into a solder bath, with or without flux depending on the characteristics of the UBM, so that the solder can wet the pads or UBM on the wafer. After a short dwell time in the solder bath the wafer is pulled out, with the solder material forming thin solder bumps on the wafer. After the wafer is subsequently reflowed, well-formed truncated spherical solder bumps can be obtained.

One of the drawbacks of solder dipping is that it is difficult to obtain a large volume of solder material on each of the pads or UBM metallized pads. Another problem is when the wetting ability of the solder on the pads or UBMs is not sufficient it can cause some 'missing solder' defects. Also, when the pitch size of the pads on the wafer is very small, the pads are easily bridged by the solder, thereby short-circuiting the pads.

2.2.2 Stencil printing

Wafer bumping by the stencil printing method is very popular in electronic packaging because of its potential low-cost and high production rate. The only limitation is that it cannot be used for very fine pitch size pad geometries.

Fig. 2-4 shows the key process for stencil printing on the wafer. The first step is to deposit the electroless Ni on the Al or Cu pads and then immerse a thin layer of electroless Au; the second step is to stencil print the solder paste on the UBM; the third step is to reflow and clean the bumps.

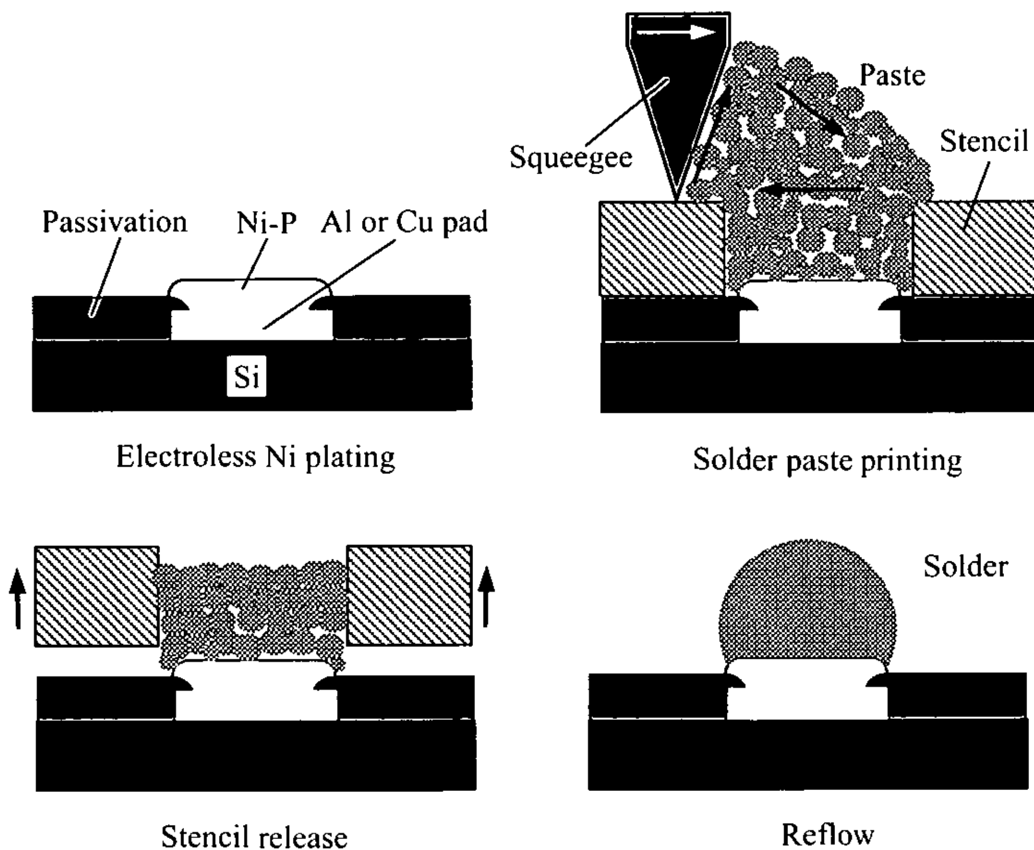


Fig. 2-4 Stencil printing process for wafer bumping.

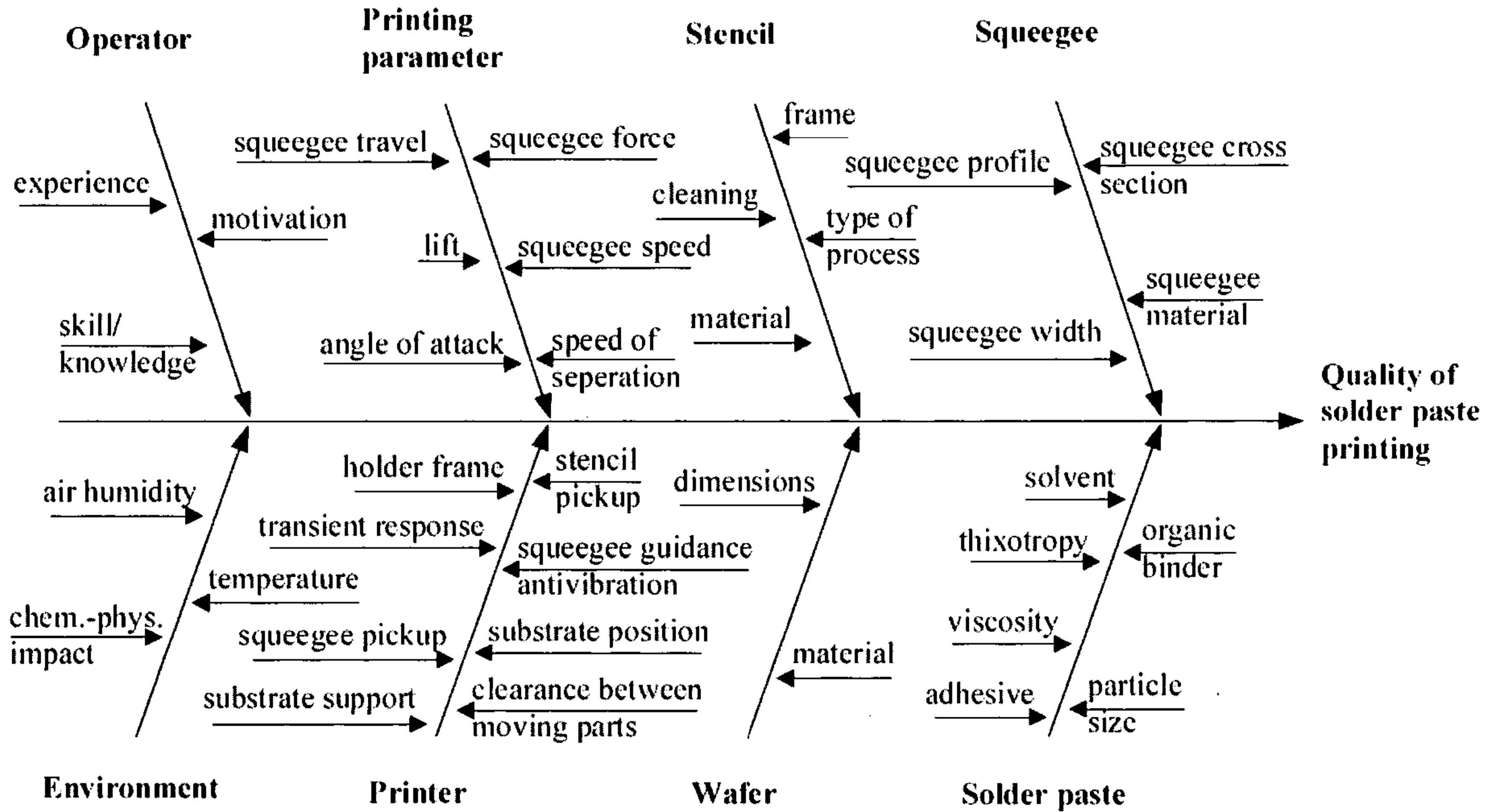


Fig. 2-5 Fishbone diagram for stencil printing [1].

Fig. 2-5 is the fishbone diagram for solder paste printing. It can be seen that there are eight major categories (operator, environment, printing parameter, printer, stencil, wafer, squeegee, and solder paste) that influence the quality of solder paste printing on a wafer [1]. For fine pitch stencil printing, the machine, tools and printing processes have been improved in recent years. Research has focused on the development of solder pastes, stencils and squeegees [18].

The rheology of solder paste is critical to achieve sufficient paste deposit without bridges. An active rosin flux containing halides should be avoided because the halide residues are detrimental to the long-term properties of the solder joints. Paste containing chemical components that create difficult-to-remove residues should also be avoided. Solder pastes with homogeneously distributed small sizes of solder particles are desirable. An electroformed stencil is better than the chemical-etched and laser-cut stencils. Although the chemical-etched stencils are cheaper, because of accuracy and dimension limitations they cannot meet the fine-pitch wafer-bumping requirement and, although laser-cut stencils are accurate, sequential processing (cutting apertures one-by-one) could make stencil costs prohibitive for wafer bumping. One advantage of laser-cut stencils is the tapered wall of the apertures, which can help the release of the solder paste and this is especially helpful in the case of thick stencils [19]. In order to realize fine pitch stencil printing, the stencils need to have fine pitch and small sized apertures, good aperture filling properties, a good paste release and a long stencil life [20].

The volume of the printed solder paste is determined by the aperture size, the stencil thickness and the material of the squeegee [18, 21]; however, a thick stencil does not mean a tall solder bump. The ratio of the area of the sidewall of the stencil aperture to the area of the stencil aperture has a critical value. When the ratio is equal to or greater than this critical value, the height of the solder bump is smaller than the thickness of the stencil and when the ratio is less than this critical value, the height of solder bump will equal to the thickness of the stencil. At the same time, the orientation of the aperture in the stencil and the printing rate will also influence the quality of printed solder bumps.

For the stencil, the limits of the aperture dimension are from the pitch size as well as the pad arrangement [18, 19, 21]. The apertures in peripheral arrays only have the limit from one direction, so they could be rectangular; however, the apertures in an area array

have the limit both from the horizontal direction and the vertical direction due to the adjacent pads, such that the apertures in an area array have to be symmetric.

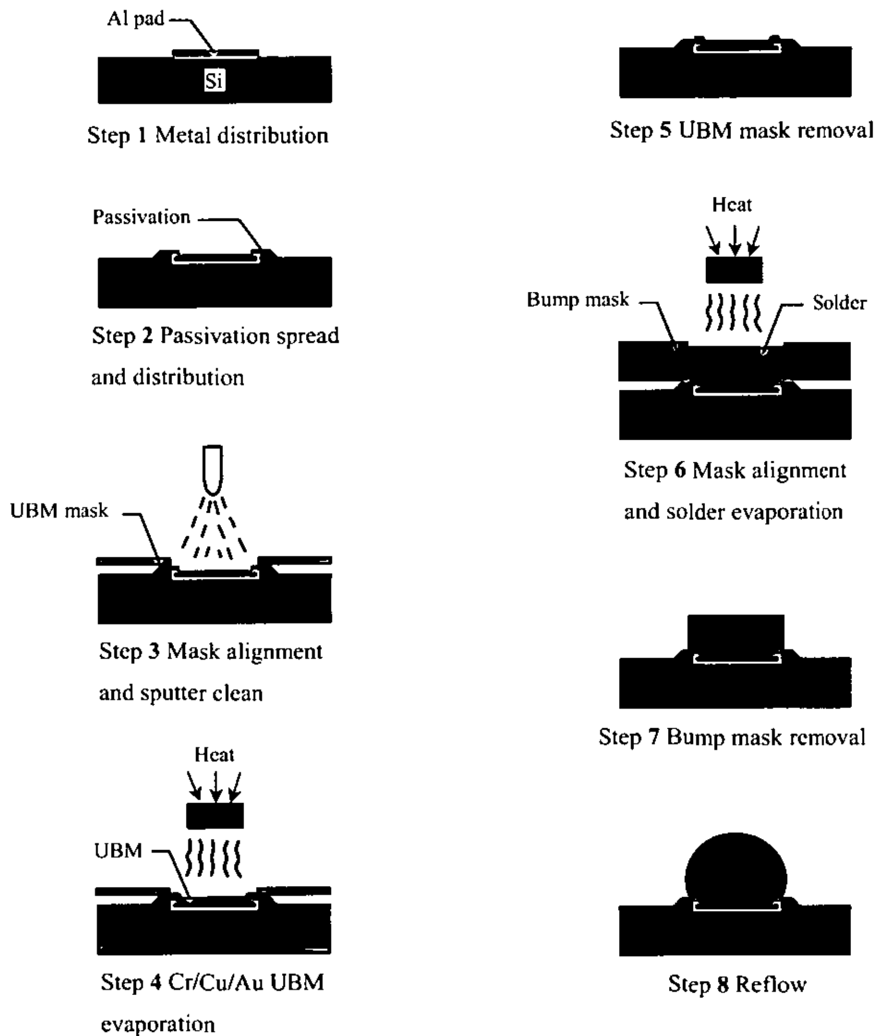


Fig. 2-6 IBM's well-known evaporation wafer-bumping process.

2.2.3 Evaporation plating

The most mature wafer-bumping method is by evaporation, which was perfected by IBM more than 30 years ago [1]. Fig. 2-6 shows the evaporation process. It requires two metal masks made of molybdenum, whose coefficient of thermal expansion is very close to that of silicon. In addition, molybdenum has excellent long-term dimensional stability at high temperatures. The first mask with smaller openings is for the deposition of the UBM through evaporation, and the second mask with larger opening is for the

deposition of solder materials. IBM calls these controlled collapse chip connection (C4) bumps. Since two metal masks and an evaporation process are needed, this method can be expensive.

Recently, Motorola developed an E-3 (evaporated extended eutectic) wafer-bumping process that also uses the evaporation method. It creates a bump with a mostly "pure" Pb column and a small amount of pure Sn at the tip. It is not reflowed prior to die attachment. Since unreflowed Pb is very soft, shipping of these bumps poses a challenge.

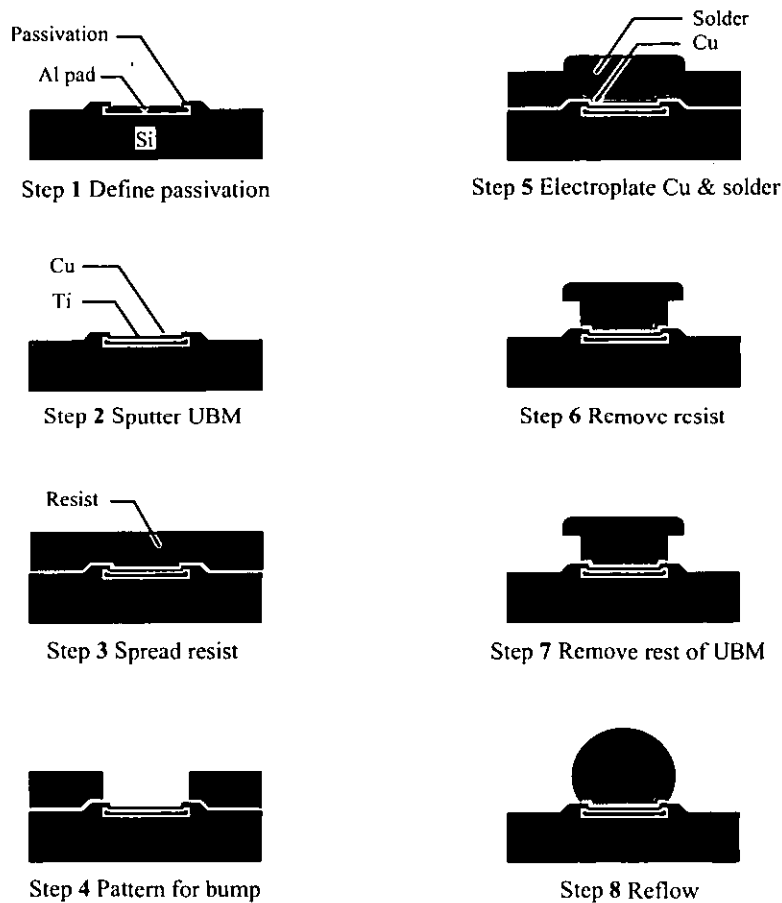


Fig. 2-7 Electroplated solder wafer-bumping process [1].

2.2.4 Electroplating

The second most mature method in wafer bumping is electroplating, which is considered a wet solder build-up process. Fig. 2-7 shows the bumping process [1]. The UBM, e.g., Ti-Cu and TiW-Cu, are sputtered over the entire surface of the wafer. A

layer of resist is then overlaid on the UBM. A mask is used to define the bump pattern, with the openings in the resist a little wider than the pad openings in the passivation layer. A layer of Cu is then plated over the UBM, followed by electroplating solder materials. This is done by applying a static or pulsed current through the plating bath with the wafer as the cathode. In order to plate enough solder to achieve the final solder height, the solder is plated over the resist coating to form a mushroom shape. The resist is then removed and the UBM layer outside of the bump is stripped off with a special etchant. The wafer is then reflowed, which creates smooth truncated spherical solder bumps.

This method is very popular today because it can plate solders in any combination. One of the drawbacks is bump height non-uniformity. Usually, due to the boundary effect, i.e., current density near the edge of the wafer is larger during the electroplating process, the solder bumps near the edge of the wafer are taller than those near the centre of the wafer. The other drawback is that the plating rate of 1-2 μm/min is slow. However, this method is cheaper than the evaporation method, since only one bump mask is needed and the process is simpler.

CHAPTER 3

Lead Free Solder Alloys

3.1 The rationale for the development of lead free solders

Sn-Pb solder alloys have been used in electronic packaging on account of their low melting temperature, good reliability, low cost and compatibility with printed circuit board assemblies. As one of the primary components of eutectic Sn-Pb solder, Pb, provides many technical advantages, such as the following: [2, 22]

- Pb lowers the surface tension and the interfacial energy. The surface tension of pure tin is 550 mN/m at 232°C, but the surface tension of 63Sn-37Pb (the composition of solders in this thesis is based on weight percentage if not specified) is 470 mN/m at 280°C.
- As an impurity in tin, even at levels as low as 0.1 wt.%, Pb prevents the transformation of white (β) tin to gray (α) tin upon cooling past 13°C. The transformation, if it occurs, results in a 26% increase in volume and causes loss of structural integrity.
- Pb serves as a solvent metal, enabling the other elements in the joints, such as Sn and Cu, to form intermetallic (IMC) bonds rapidly, by diffusion in the liquid state.
- The eutectic Sn-Pb solder has a low eutectic and melting temperature at 183°C, so the reflow temperature is low, typically around 200-225°C, which has little thermal influence on the printed circuit board (PCB) and electronic components.
- The high-Pb solders such as Sn-95Pb, with a reflow temperature of around 350°C, have a very narrow temperature gap of melting, about 10°C, between its

liquidus and solidus points, so it can be used as a high temperature solder. Therefore, a high-low combination of the high-Pb and eutectic Sn-Pb can be applied in a two-level reflow soldering operation. This solder is used extensively to form the joints in the first level pacakaging, such as processors and memory modules, which subsequently experience another soldering operation when soldered to the PCB.

Despite the above beneficial properties, the toxicity of Pb has resulted in legislation to eliminate Pb from the electronic industry [3].

The concern about the use of Pb in the electronics industry stems from occupational exposure, Pb waste derived from the manufacturing process and the disposal of electronics at the end of useful life. The adverse influence of Pb on the environment comes primarily from the disposal of electronics. At the end of the useful life Pb containing electronics are typically disposed of in solid waste landfills. But the mechanism, by which Pb migrates from disposed electronic products to ground water, or the animal and human food chain, is not yet clear. When Pb accumulates in the body over time, it can have adverse health effects. Research shows that when the level of Pb in the blood exceeds 50mg/dL, Pb poisoning will occur.

In Europe, the WEEE/RoHS Directives have passed legislation that will ban the use of lead in all electronic assemblies from July 2006 [3]. So lead free solders have to be used to replace Sn-Pb solders.

Some lead free solder alloys have already been extensively investigated. In order to maintain or enlarge their markets, avoid trade barriers, many companies, including IBM, Compaq, Motorola, Hewlett Packard, and Sony etc., have been involved in this area and are assessing alternative alloys. These efforts have focused on the search for drop-in replacements, seeking to find low temperature alloys compatible with materials and production equipment.

3.2 The properties of lead free solders

3.2.1 Solder alloy cost

The microelectronics industry is extremely cost-conscious due to intense competition. The history of the industry has been to continuously produce higher performance at lower cost. Since cost of the product is the result of the cumulative cost of the components, the cost of lead-free solder alloys can impact the cost of the finished products.

The lead free solders are Sn-based. Most materials are the eutectic alloys of Sn and metals, such as Au, Ag, and Cu. Other eutectic elements with Sn are Bi, Zn, In, Sb etc. Among them Zn is the cheapest metal, and then Cu and Sb, and at the other end of the scale indium is the most expensive, which is even more expensive than Au because it is so rare. Another problem with In is supply; only approximately 200 tons of indium are produced globally each year, which can lead to supply problems and drastic price fluctuations. In general, all the lead-free solder alloys are more expensive than eutectic Sn-Pb alloy.

3.2.2 Microstructure and composition of bulk solder alloys

The lead-free solder alloys currently being studied are mostly eutectic or near-eutectic alloys. Because a eutectic alloy has a single and low melting point, the entire solder joint will melt or solidify at a fixed temperature, i.e. partial melting or partial solidification will not happen. Partial solidification can cause the formation of defects and stress in the solder joints, which can damage the mechanical properties and reliability of solder joints.

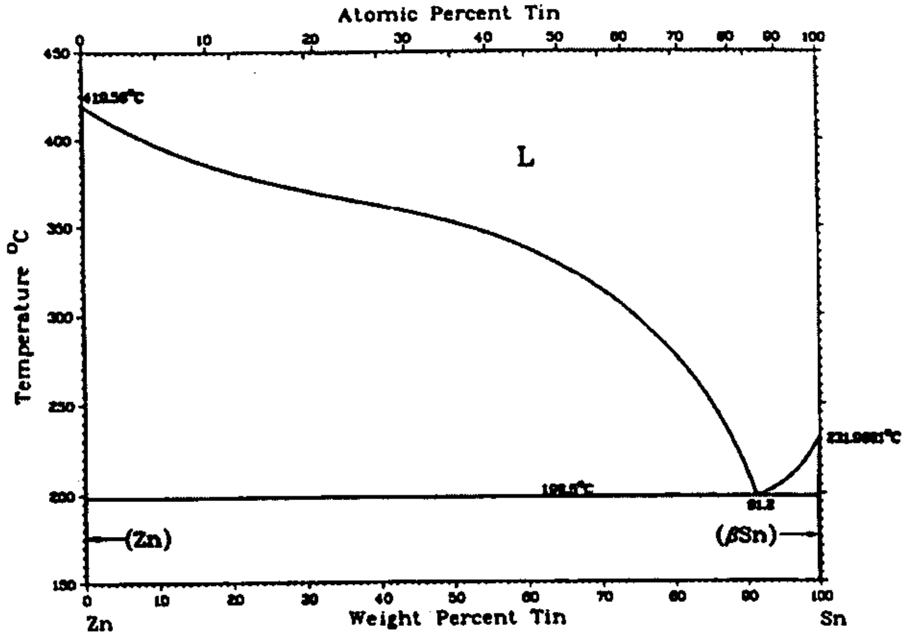


Fig. 3-1 Sn-Zn phase diagram.

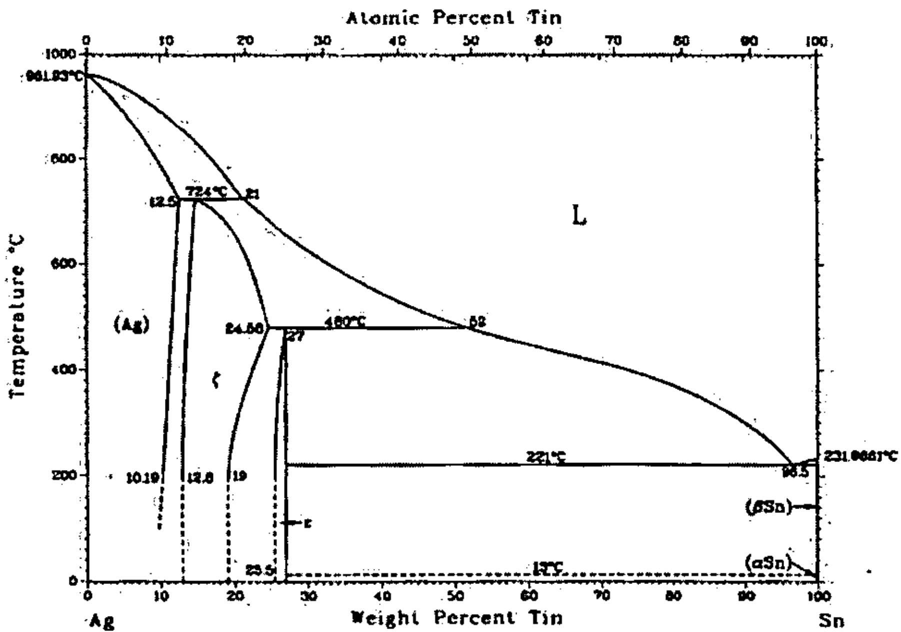


Fig. 3-2 Sn-Ag phase diagram.

A large number of lead-free solder alloys have been proposed, and they are binary, ternary and even quaternary. The most common used lead-free solder alloys are Sn-Ag, Sn-Cu, Sn-Bi, Sn-Zn, Sn-Ag-Cu. Among them Sn-Ag-Cu seems to be the most promising alternative for eutectic Sn-Pb. Figs. 3-1 to 3-4 are the phase diagrams of these solder alloys [23, 24].

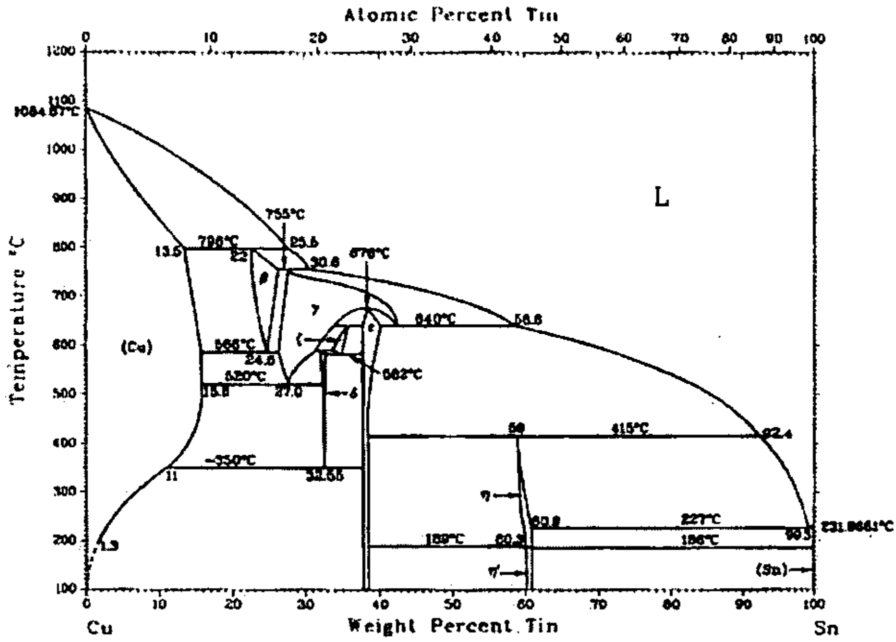


Fig. 3-3 Sn-Cu phase diagram.

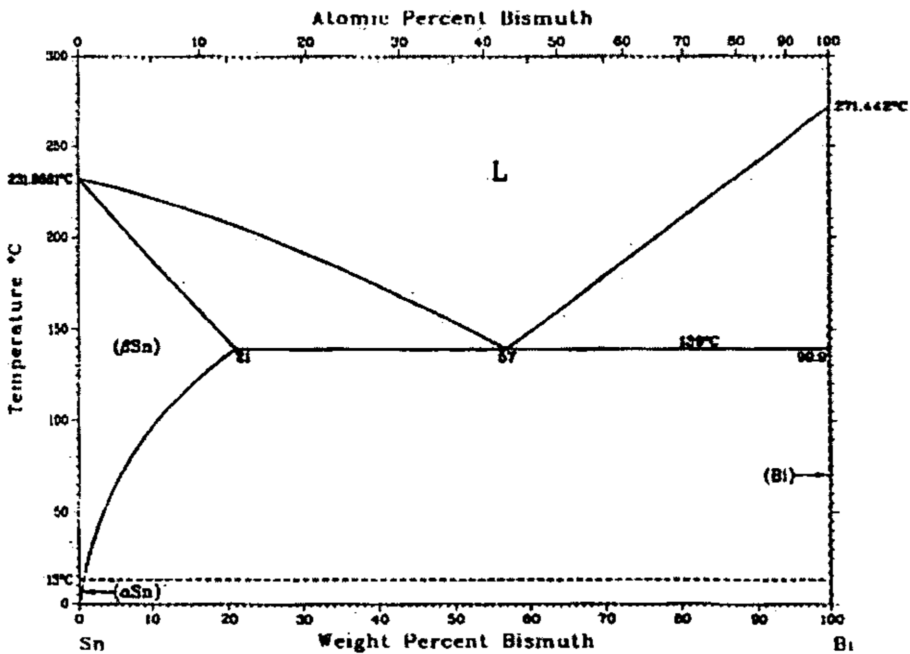


Fig. 3-4 Sn-Bi phase diagram.

Microstructure can be defined as the combination of the phases that are present in a material, their defects, morphology, and distribution [25]. The composition and microstructure of a material determines its properties. The microstructure is in turn a function of the composition of the material and its thermal, mechanical and chemical history.

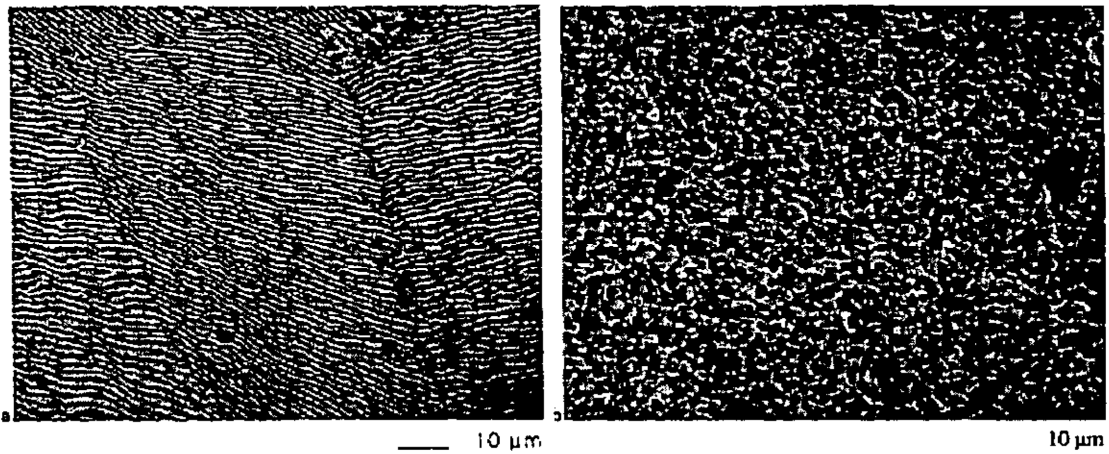


Fig. 3-5 Typical solidification microstructure of eutectic Sn-Pb solder, a) lamellar microstructure formed by slow cooling, b) fine equiaxied microstructure formed by rapid cooling.

In electronic assembly, the primary processing variable that affects the initial solder microstructure is the cooling rate. Then the microstructure of bulk solder or solder joints can evolve during later processes or service life stages. Normally the microstructure of Sn-Pb is lamellar, but if it is cooled quickly the microstructure could be equiaxed, as shown in Fig. 3-5 [25]. Faster cooling means a finer microstructure because more nucleation sites exist due to super-cooling and there is less time for diffusion to occur.

Sn: Sn can exist in two forms, white (β) Sn, which is the stable form at room temperature, and grey (α) Sn, the stable form below 13°C. White Sn has a tetragonal crystal structure that is much denser than the diamond cubic crystal structure of grey Sn. The transformation of β to α Sn, also called Sn pest, will take place if the temperature is reduced below 13°C [2]. A large volume increase will go with this transformation, which can cause extensive cracking in the Sn structure. Consequently, Sn pest can be a problem in systems that are exposed to low temperatures in service and can be particularly problematic for devices that cycle across the 13°C barrier. Because Sn has a body centred tetragonal crystal structure that is anisotropic and tends to deform by twinning (Sn cry) [26], the thermal expansion and mechanical properties are also anisotropic. Sn whisker, single crystal growth in response to stress, is another problem that Sn solder may encounter.

Sn-Ag and Sn-Cu: The microstructures of eutectic alloys Sn-0.7Cu and Sn-3.5Ag are a mixture of Sn and a small concentration of intermetallics (IMCs), which are different from that of eutectic Sn-Pb alloy. In the eutectic Sn-Cu alloy, Cu is generally found as scallop-like IMCs Cu_6Sn_5, while in the eutectic Sn-Ag alloy, the second phase is either the plate-like or scattered Ag_3Sn particles.

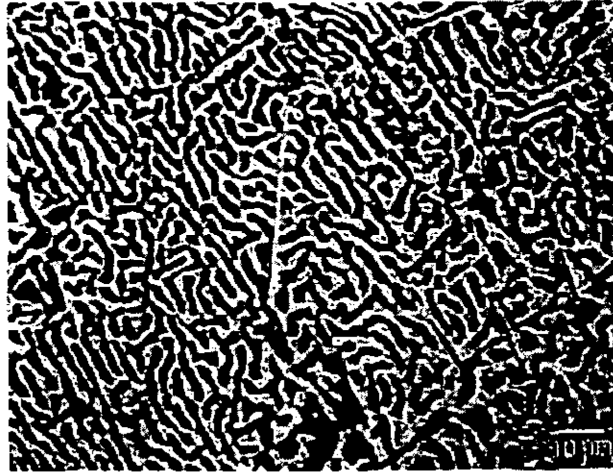


Fig. 3-6 Microstructure of eutectic Sn-Bi.

Sn-Bi: The microstructure of eutectic Sn-Bi is lamellar, as shown in Fig. 3-6 [25], with degenerate material at the boundaries of the grain for all moderate-cooling rates. Increasing the cooling rate refines the microstructure, however there still remains a lamellar structure, which is different from the eutectic Sn-Pb system. The eutectic composition in the Sn-Bi system is at 42Sn-58Bi. Bismuth has significant solubility in Sn at the eutectic temperature; consequently, as the alloy cools Bi precipitates in the Sn phase. The Bi phase is essentially pure Bi. The volume ratio of the Sn phase to Bi phase is 49:51.

Bi does not deform easily because dislocation motion is difficult. Bi has five valency electrons per atom and the atoms are bound predominately by covalent bonds. It has a rhombohedral crystal structure, which can also be viewed as puckered sheets, loosely bound to each other [27]. The directional nature of the bonding in this structure means that it is not easy to deform.

Sn-Bi alloys are an exception to the general rule that solder alloy, like most other metals, contract during solidification. Although Sn contracts, Bi expands 3.87% in volume during solidification, which is much more than the contraction of Sn, so the eutectic Sn-Bi alloy will expand on solidification [25, 28]. When the alloys are cooled rapidly, they have been observed to grow after solidification.

Sn-Zn: The 91Sn-9Zn is the eutectic composition for the Sn-Zn system, and its eutectic structure consists of two phases: a body-centred tetragonal Sn matrix phase and a Zn phase containing less than 1wt.% Sn in solid solution. The microstructure of eutectic Sn-Zn alloy is a lamellar structure with alternating Sn-rich and Zn-rich phases.

3.2.3 Melting temperature

The melting temperature reported for ternary and quaternary systems is in fact the liquidus temperature, i.e. the temperature at which the solder alloys are completely molten, since it is liquidus temperature that is important to soldering operations in the microelectronics industry. From a manufacturing perspective the melting temperature, i.e. the liquidus temperature, is perhaps the first and most important factor. The eutectic temperature of Sn-Pb is 183°C, and most of the assembly equipment in use today is designed to operate using 183°C as a base reference. While some temperature variation, for example 50°C, can be accommodated by the equipment currently in place, if the melting point of the replacement lead-free solder is significantly higher, then new equipment will have to be purchased by manufacturers, leading to product cost increase.

Another reason for maintaining the melting point at a temperature close to 183°C is the broad use of thermoset polymers in microelectronics packaging, such as underfill and PCB. It is important that these and other materials do not degrade during soldering operations. Currently, the highest temperature that these polymeric materials can survive at is 230-250°C for 90-120 s.

For binary and higher systems, only the alloys with eutectic compositions have a consistent melting temperature. Other compositions can be expected to melt in a temperature range, with melting beginning at the solidus temperature and finishing at the liquidus temperature. The eutectic alloys are preferred because they have a single

melting point and the entire solder joints will melt and solidify at a temperature, otherwise partial melting or solidification may happen and defects and stress can form in the solder joints.

The melting temperatures of solder alloys cannot be too high. In order to make sure the solder can melt completely, there must be some margin as to the processing temperature relative to melting temperature. When using a eutectic Sn-Pb solder with a eutectic temperature of 183°C, the typical solder reflow temperature is 220°C, with a margin of about 40°C. So a high melting temperature means even higher processing temperature.

The solidus temperatures of solder alloys cannot be too low as well. The solidus temperature determines the homologous temperature (T_H), which is obtained by dividing the alloy's desired service Kelvin temperature by its solidus temperature in Kelvin. When $T_H > 0.5$, then the atoms within the alloy have sufficient energy to participate in thermally activated processes, such as creep and grain growth. The solder alloy with low solidus temperature will have a high homologous temperature, which can result in the alloy being subjected to more severe creep conditions. For eutectic Sn-Pb and most lead free solder alloys, the homologous temperature is larger than 0.5 at room temperature.

The melting temperature of Sn-3.5Ag and Sn-0.7Cu is 221°C and 227°C, respectively. Indium is effective in reducing the melting temperature of Sn-3.5Ag, but the eutectic temperature of Sn-Ag-In is too low (about 113°C). Besides In is too scarce and too expensive to be considered for widespread application and it oxidises very easily. Eutectic Sn-Ag-Cu solder has a melting temperature, 217°C, which is a little lower than that of Sn-3.5Ag and Sn-0.7Cu, and it is the most promising lead free solder alternative to Sn-Pb solder.

McCormack and Jin [29] have studied the influence of the addition of Zn to a eutectic Sn-Ag alloy. The addition of Zn can slightly lower the melting temperature of Sn-Ag alloy. In the ternary Sn-Ag-Zn alloy, Zn is incorporated into the Ag_3Sn precipitates and makes the Ag_3Sn precipitates finer and more spherical, and it tends to suppress the formation of Sn dendrites. In order to find the effects of rare-earth elements on the bonding nature of lead free solders, Ramirez et al. [30] and Wang et al. [31] studied the

influence of small additions of rare-earth elements on the properties of Sn-3.5Ag solder. The results showed that the additions of rare-earth elements did not significantly modify the solidification microstructure or melting point, but these oxide-bondable solders are useful for applications in optical fibers for various optical communication devices. The results of Wang et al. also show that the wettability and tensile properties of Sn-3.5Ag were improved by a 0.25-0.5wt.% addition of (La, Ce) mixture.

The eutectic Sn-Bi solder alloy has a low melting temperature of 139°C, and Bi has very good wetting and physical properties [22]. But the alloy has a high Bi content, 58%, and although the price of Bi is not too high, almost the same as Sn, the availability of Bi could be limited by the restriction on Pb, because the primary source of Bi is as a by-product in Pb refining. A more serious problem with Bi is that if a bismuth alloy picks up any Pb, a secondary eutectic Sn-Pb-Bi phase of 95°C will be formed, resulting in poor fatigue resistance [25].

Sn-9Zn seems to be an attractive alternative, with a melting temperature of 198°C that is close to eutectic Sn-Pb, but it quickly forms a stable oxide, resulting in excessive drossing during wave soldering and possesses a very poor wetting ability.

3.2.4 Wetting ability

To form a strong metallurgical bond between the solder and the substrate, the solder must wet the substrate. During wetting, the solder will react with the substrate and form some intermetallic compounds (IMCs) at the interface. So the formation of a certain amount of IMCs at the interface is desirable for a strong interconnection. The ability of the molten solder to flow or spread during the soldering process is of prime importance for the formation of a metallic bond. The phenomenon of spreading is also frequently referred to as 'wetting'. By definition, wetting is the ability of a material, generally a liquid, to spread over another material, usually a solid. The extent of wetting is measured by the contact angle that is formed at the juncture of a solid and liquid in a particular environment. In general, if the wetting angle is between 0 and 90° the system is said to wet, and if the wetting angle is between 90 and 180° the system is said not to

wet. The contact angle (θ) is determined from the balance of surface tension at the juncture, according to the Young-Dupre equation:

$\gamma_{gs} = \gamma_{ls} + \gamma_{gl} \cos\theta$

where γ_{gs} is the surface tension of the solid in the particular environment, γ_{ls} is the surface tension between the solid and the liquid, and γ_{gl} is the surface tension of the liquid in the same environment. In term of free energy, good wetting can take place only when the free energy of the system is decreasing, i.e., the surface energy of the wetting system is lowered by forming an interface.

The surface tension of solder on the substrate is one of the critical physical properties that determine its wetting ability. In addition to wetting, the surface tension also has influence on the capillary flow for pin-through-hole (PTH) soldering, self-alignment of surface mounted devices, the capability to keep devices from falling off during second reflow, and the natural radius of curvature.

The surface tension of a liquid is a thermodynamic quantity and is defined as the amount of work needed to isothermally increase a unit of surface area. Thermal equilibrium is seldom reached in the actual soldering process, because normally the soldering operation is completed before equilibrium is reached. Furthermore, dissolution of the substrate in the molten solders, the oxidation of the solder, the flux and the soldering environment etc., also affect the surface tension of solders. Studies have shown that the surface tension value of solder varies with temperature, flux composition, and the extent of solder-substrate interaction [2]. For these reasons the surface tension of solders and most other liquid metals under processing conditions are not precisely known. The natural radius of curvature can be calculated using the following equation:

$$R = \sqrt{\frac{\beta\gamma}{\rho g}} \tag{3-1}$$

where γ is the surface tension, ρ is the liquid density, β is a shape factor, and g is the acceleration due to gravity.

Although surface tension and wetting angle are related, the latter is more specifically related to the particular materials combination under investigation. The wetting angle is affected by a variety of factors, including surface roughness, wetting time, the flux used and its effectiveness and the temperature of measurement. However, in one particular system, probably only one or two of the factors are determinant factors.

In addition to the sessile drop method for determining the contact angle, and thus the wettability, a wetting balance that measures the wetting force and the wetting time when a solid substrate is dipped into a liquid, is also used to determine the wettability. The wetting force can be correlated to the wetting angle, and higher wetting forces indicate smaller wetting angles and therefore better wetting ability. While both techniques permit measurement of the wettability, the wetting force balance also permits the measurement of wetting time. This is an important parameter for actual manufacturing operations. Typical processing times for completing soldering operations are 60-90 s. Solders that might have very good wetting characteristics, i.e. low wetting angles or high wetting forces, but require long incubation periods, such as 2-5 min for maximum wetting to be attained, might be suitable from a scientific perspective, but cannot be used commercially due to the low productivity. The wetting time can therefore dictate the industrial acceptability of solders.

The maximum wetting force and wetting time of three Pb-free solders and eutectic Sn-Pb solder, with Cu substrates, were measured at 240°C using an 'aqueous clean' flux (Kester #2224-25) and a no-clean flux (Alpha Metals Lonco SL5-65) [32]. The Pb-free solders used in this study were Sn-3.5Ag, Sn-58Bi, and Sn-9Zn. The results show that all three Pb-free solders had wetting forces significantly lower than eutectic Sn-Pb. The Sn-9Zn solder has poor wetting ability with the Cu substrate, and its wetting force is much lower than those of other solders, with dewetting occurring when a no-clean flux is used. The wetting time of lead free solders was also longer than that of eutectic Sn-Pb, and Sn-3.5Ag needed a longer time to wet than other solders [32].

The wetting abilities of solders depend on the type of flux used. The use of a more aggressive flux results in better interaction, as reflected by higher wetting forces. This is due to the fact that when the flux is more aggressive the reaction to remove surface oxidation is more effective.

Collazo has studied the influence of stored surface energies on the wetting force using both eutectic Sn-Pb solder and 77.2Sn-20Zn-2.8Ag Pb-free solder on Cu coupons [33]. During the experiments, Cu coupons were cold rolled with 10, 20, 30, 40, and 50% of cold work stored in the surface respectively, then the wetting forces were measured. The results showed that wetting forces increased with the stored surface energies, over the range tested. This trend was the same for both solders, although the 77.2Sn-20Zn-2.8Ag solder had wetting forces that were typically 0.6-0.7mN lower than the Sn-Pb solder. Concomitant with the increase in wetting force, the wetting time was also found to decrease. However, all values of wetting time were 0.4 s or less, and therefore have no influence on industrial soldering operations. Collazzo's work shows that in cases where the wetting force is inadequate, cold working of the lead frame might be an avenue of increasing this characteristic.

3.2.5 Thermal properties

A typical microelectronics assembly usually contains a lot of materials, such as metals, silicon, polymers, polymer based composites and ceramics, with different coefficients of thermal expansion (CTE). During the service life of electronic products, every time the system is powered-on, heat will be generated in the components and their temperature will increase, which causes different expansion in different materials and thereby stress accumulates.

Table 3-1 Thermal properties of lead free solders and other electronic materials.

Solders	**CTE** (10^{-6}/K)	**Thermal conductivity** (W/m·K)	**Reference**
Sn-58Bi	15.0	21	[25]
Sn-52In	20.0	34	[25]
Sn-3.5Ag	22; 30	33	[25]
Si	2.8	150	[34]
Cu	17	391	[25]
Al	22.3	237	[34]
FR-4 (x,y; T<Tg)	15-18	0.35	[25]

The heat generated by the components needs to be dissipated by the substrates, encapsulation materials and solders in order to keep the components in suitable service

environment. The ability of materials to diffuse the heat away depends on their thermal conductivity, so the thermal conductivity of these materials is very important.

Table 3-1 lists the thermal properties of some lead free solders and other electronic materials summarized by Glazer [25] and Winterbottom [34].

3.3 Sn whisker

Most lead-free solder alloys are Sn-rich alloys, so the problems that occur with pure Sn, such as Sn pest, Sn cry, and Sn whisker, can also easily happen with these alloys.

The whisker growth is thought to be a result of compressive stress relaxation; however, compressive stress is not enough on its own. Tu et al. [22, 35-37] showed that Sn whiskers can grow over 0.3 mm at room temperature and there are three necessary and sufficient conditions for the growth of Sn whisker: a fast atomic diffusion source, a compressive stress and a protective film on the surface. The growth process is believed to be diffusion controlled. Sn has a low melting temperature of 231°C, so it can diffuse fast at room temperature with the grain boundary diffusivity about 10^{-8} cm^2/s. The compressive stress for Sn whisker growth comes from the formation of a Cu_6Sn_5 IMC. Research from Tu [35] shows that Sn can react with Cu to form Cu_6Sn_5 IMC at room temperature, resulting in whisker growth at room temperature. A protective film is needed for the stress gradient and the localized Sn whisker growth site. A free surface of Sn in ultra-high vacuum will not have Sn whiskers, because the free surface is a good source and sink of vacancies and the compressive stress can be relieved uniformly in each of the Sn grains. Hence, only those metals that can have a protective oxide, such as Sn and Al, are known to have whisker or hillock growth.

Sn whiskers can grow to over 10 mm in length and they can be many different shapes, e.g., filament, nodule and hillock [38]. Some research [39, 40] has shown that a high humidity environment can increase the whisker growth. The research of Winterstein [41] shows that room temperature ageing can increase the whisker density and high temperature annealing can cause a retardation to whisker growth. After annealing, the stress inside the system is relieved, so the whisker growth loses the driving force and

will stop. But the Sn will react with Cu continually and form new compressive stress, and then the whisker will resume growth. It is evident that stress is the driving force of whisker growth.

Whiskers do not influence solderability nor do they cause deterioration of the Sn coatings. However, longer whiskers may cause electrical shorts in PCBs.

CHAPTER 4

Nanoindentation

4.1 Introduction

Nanoindentation has been used in the mechanical, creep and fatigue property testing of materials. Due to its precise control and measurement of load, depth and displacement of a small testing head, it is useful for testing the mechanical properties of thin films, multi-layered components and other materials with small volumes.

Development has been made over the past few years to the techniques of probing the mechanical properties of materials at the sub-micron scale. The advances have been made possible by the development of instruments that continuously measure load and displacement as an indentation is made. The techniques rely on the fact that the displacements recovered during unloading are largely elastic, in which case elastic indenter theory can be used to determine the modulus, *E*, from the unloading curve, which can be used to determine mechanical properties even when the indentations are too small to be imaged conveniently. Since the indentation positioning capability is also in the sub-micron regime, nanoindentation can be used to map the mechanical properties of a surface with sub-micron resolution.

4.2 Initial idea of nanoindentation

The elastic contact problem, which plays a key role in the analysis procedure, was originally considered in the late 19th century by Boussinesq and Hertz [42]. Boussinesq developed a method and a potential theory for computing the stresses and displacements

in an elastic body loaded by a rigid, axisymmetric indenter. His method has subsequently been used to derive solutions for a number of important geometries such as cylindrical and conical indenters. Hertz analyzed the problem of the elastic contact between two spherical surfaces with different radii and elastic constants. His now-classic solutions are based on much experimental and theoretical work in the field of contact mechanics and provide a framework by which the effects of non-rigid indenters can be included in the analysis. Another major contribution was made by Sneddon [43], who derived general relationships among the load, displacement and contact area for any indenter that can be described as a body of revolution of a smooth function. His results, which form one of the foundations of nanoindentation, show that the load-displacement relationships for many simple indenter geometries can conveniently be written as

$$P = \alpha h^m \tag{4-1}$$

where P is the indenter load, h is the elastic displacement of the indenter, and α and m are constants. The exponent m is geometry dependent, and for some common indenter geometries values of it are $m = 1$ for flat cylinders, $m = 2$ for cones, $m = 1.5$ for spheres in the limit of small displacements, and $m = 1.5$ for paraboloids of revolution.

Sneddon's analysis also leads to a simple relation between P and h over the initial portion of unloading curve

$$P = \frac{4\mu a}{1-\nu} h \tag{4-2}$$

where a is the radius of the cylinder, μ is the shear modulus, and ν is Poisson's ratio [44]. Because the projected contact area, A, is πa^2, based on a flat cylinder indenter and the shear modulus can be related to the elastic modulus through $E = 2\mu(1+\nu)$, Eq. (4-2) can be written as

$$P = \frac{2}{\sqrt{\pi}} \sqrt{A} \frac{E}{1-\nu^2} h \tag{4-3}$$

Differentiating P with respect to h leads to

$$S = \frac{dP}{dh} = \frac{2}{\sqrt{\pi}} \sqrt{A} \frac{E}{1-\nu^2} \tag{4-4}$$

here, $S = \mathrm{d}P/\mathrm{d}h$ is the experimentally measured stiffness of the initial portion of the unloading data. It is thus seen that the modulus can be computed directly from the initial unloading slope, provided a reasonable estimate of Poisson's ratio and an independent

measure of the contact area are available. In the case that the indenter itself has finite elastic constants, E_i and ν_i, such that the influence of the indenter deformation on the measured displacement cannot be ignored, a reduced modulus, E_r, needs to be defined

$$\frac{1}{E_r}=\frac{1-\nu^2}{E}+\frac{1-\nu_i^2}{E_i} \tag{4-5}$$

where E and ν are Young's modulus and Poisson's ratio for the specimen. Thus Eq. (4-4) becomes

$$S=\frac{dP}{dh}=\frac{2}{\sqrt{\pi}}\sqrt{A}E_r \tag{4-6}$$

By measuring the initial unloading stiffness and assuming that the contact area is equal to the optically measured area of the hardness impression, the modulus can thus be derived.

Although Sneddon derived the Eq. (4-4) through a conical indenter in 1965, later Pharr, Oliver and Brotzen [44] found that the equation is suitable to any indenter that can be described as a body of revolution of a smooth function. By finite element calculation, King [45] studied the load-displacement characteristics of elastic half spaces by flat punches with circular, triangular and square cross-sections, and the results present that the unloading stiffness can be given by:

$$S=\beta\frac{2}{\sqrt{\pi}}\sqrt{A}E_r \tag{4-7}$$

The values for the constant β are 1.000 for circular, 1.034 for triangular and 1.012 for square. The latter two geometries, which cannot be described as bodies of revolution, are equivalents of the Berkovich and Vickers indenters. It means that Eq. (4-4) does not have any significant limitation on application to Berkovich and Vickers indenters.

4.3 Indenter area function

In the initial stage of a nanoindentation, the projected contact area is measured through optical methods. Since imaging very small indentations is both time-consuming and difficult, Pethica, Hutchings, and Oliver [46] suggested a simple method based on measured indentation load-displacement curves to determine the indenter area function, that is, the cross-sectional area of the indenter as a function of the distance from its tip.

The method is based on the notion that, at peak load, the material conforms to the shape of the indenter to some depth; if this depth can be established from the load-displacement data, the projected contact area can be estimated directly from the shape function. Two observation choices for the depth are the depth at peak load, h_{max} (i.e. the maximum displacement in the loading cycle), and the final depth, h_f (i.e. the residual depth of the hardness impression after final unloading), both of which are easily determined from indentation load-displacement data. Using TEM replication methods to establish the shape function, Oliver et al. found that the final depth gives a better estimate of the contact area than the depth at peak load.

Doerner and Nix [47] subsequently put together many of these ideas to produce the most comprehensive method to date for determining hardness and modulus from indentation load-displacement data. Their approach is based on the observation that during the initial stages of unloading, the area of contact remains constant, as the indenter is unloaded. To independently evaluate the contact area, Doerner and Nix proposed a simple empirical method based on extrapolating the initial linear portion of the unloading curve to zero load and using the extrapolated depth with the indenter shape function to determine the contact area. With the contact area so determined, the modulus can be computed from Eq. (4-7) and the hardness from its normal definition:

$$H = \frac{P_{max}}{A} \qquad (4\text{-}8)$$

where P_{max} is the peak indentation load and A is the projected contact area of the hardness impression.

4.4 Stiffness measurement

Doerner and Nix [47] have reported that linear unloading is observed in metals over most of the unloading range and in silicon for at least the first one-third of the unloading curve. They used linear unloading to calculate the stiffness. However, there are many materials, particularly ceramics and glasses, for which unloading curves are not linear, and even in metals, the results of Oliver et al. [42] show that their unloading behavior are best described by nonlinear relation. After four sets of loading and unloading (three partial unloading to 10% maximum load and one full), they tested the unloading behavior of fused silica, soda-lime glass, (001) sapphire, (001) quartz, tungsten, and

aluminium by using a Berkovich indenter, and plotted the data on logarithmic axes. The results show that the load-displacement relationship can be described reasonably well by power law relations with exponents greater than 1. For the six materials studied, the power law exponents range from 1.25 to 1.51. The representative material for Doerner and Nix's theory is aluminium. When the data is plotted on a single set of axes, the unloading curve is very steep and gives an appearance of being linear. This is the reason that causes the difference between the two observations.

4.5 Current analysis method

The current analysis method for nanoindentation was proposed by Oliver et al. Because a flat punch approximation is not an entirely adequate description of the behavior of materials when indented by a Berkovich indenter, Oliver et al. [42] proposed a new analysis method based on analytical solutions for other indenter geometries. In addition to accounting for curvature in the unloading data, the method also provides a physically justifiable procedure for determining the depth that should be used in conjunction with the indenter shape function to establish the contact area at peak load.

The new method is based on the conical and paraboloid indenter geometries. The conical indenter is a natural choice since, like the Berkovich indenter, its cross-sectional area varies as the square of the depth of contact and its geometry is singular at the tip. The paraboloid indenter, whose behavior is the same as that of a spherical indenter in the limit of small displacements, is also a potentially useful geometry in that no real indenter is ever perfectly sharp; i.e., at some scale the tip exhibits some rounding. In addition, because of plasticity, an elastic singularity cannot really exist at the tip of the indenter, and the paraboloid geometry potentially accounts for this. For both geometries, the load-displacement relationships are nonlinear and the contact area changes continuously during unloading.

An important fundamental assumption in the development is that Sneddon's solutions, which describe the elastic unloading, apply equally well to a flat surface and a surface with a hardness impression.

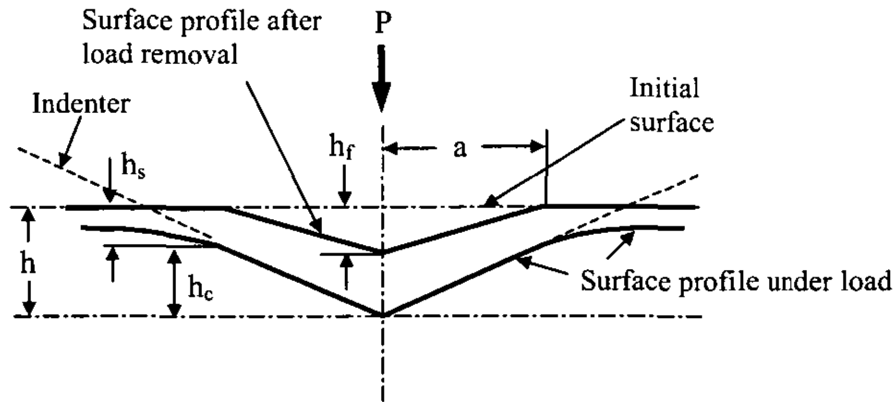


Fig. 4-1 A schematic diagram of a section through an indentation showing various quantities used in the analysis [42].

Fig. 4-1 shows a cross section of an indentation and identifies the parameters used in the analysis [42]. At any time during loading, the total displacement h is written as

$$h = h_c + h_s \quad (4\text{-}9)$$

where h_c is the contact depth, and h_s is the displacement of the surface at the perimeter of the contact. At peak load, the load and displacement are P_{max} and h_{max}, respectively, and the radius of the contact circle is a. On unloading, the elastic displacements are recovered, and when the indenter is fully withdrawn, the final depth of the residual hardness impression is h_f.

The experimental parameters needed to determine hardness and modulus are shown in the schematic load-displacement curve, Fig. 4-2 [42]. The three key parameters are the peak load (P_{max}), the depth at peak load (h_{max}), and the initial unloading contact stiffness (S_{max}). It should be noted that the contact stiffness is measured only at the peak load, and no restrictions are placed on the unloading data being linear during any portion of the unloading.

As mentioned above, Eq. (4-6) is suitable to any indenter that can be described as a body of revolution of a smooth function and not limited to a specific geometry. Thus, by measuring the initial unloading stiffness the reduced modulus can be calculated if the contact area at peak load can be measured independently.

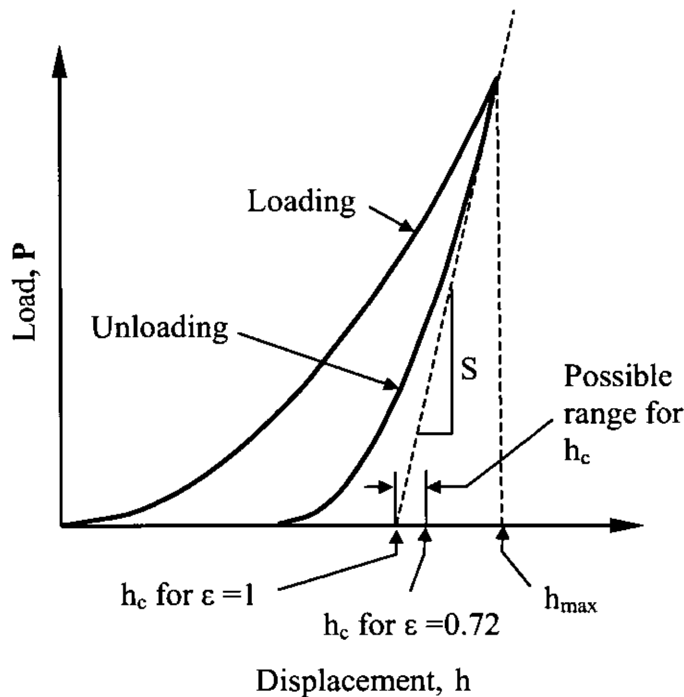


Fig. 4-2 A schematic diagram of load and displacement curves showing quantities used in the analysis as well as a graphical interpretation of the contact depth [42].

The area of contact at peak load is determined by the geometry of the indenter and the depth of contact, h_c. Oliver et al. [42] assumed that the indenter geometry can be described by an area function $F(h)$, which relates the cross-sectional area of the indenter to the distance from its tip, h. Given that the indenter does not itself deform significantly, the projected contact area at peak load can then be computed from the relation

$$A = F(h_c) \tag{4-10}$$

The functional F must be established experimentally prior to analysis.

The contact depth can be got through

$$h_c = h_{max} - h_s \tag{4-11}$$

which follows directly from Eq. (4-9). Since h_{max} can be experimentally measured, the key to the analysis then becomes how the displacement of the surface at the contact perimeter, h_s, can be ascertained from the load-displacement data.

The deformation of the surface at the contact perimeter depends on the indenter geometry. Sneddon's analysis [43] shows that the shape of the surface outside the area of contact can be expressed as

$$h_s = \varepsilon \frac{P_{max}}{S} \tag{4-12}$$

and the geometry constant ε for conical indenter, flat punch and paraboloid indenter is 0.72, 1 and 0.75, respectively.

The graphical interpretation of Eq. (4-12) is shown in Fig. 4-2. For $\varepsilon = 1$, the value for the flat punch, $h_s = P_{max}/S$, and the contact depth h_c is given by the intercept of the initial unloading slope with the displacement axis. Interestingly, this is precisely the depth used by Doerner and Nix in their analysis based on the flat punch approximation. Thus, the current method is consistent with the Doerner and Nix's approach when the flat punch geometry is assumed. For the conical and paraboloid indenters, however, the contact depths are greater than those for the flat punch, and this must be accounted for in analyses using these indenter geometries if accurate measurements are to be obtained.

In addition to the modulus, through Eq. (4-8) the data obtained using the current method can be used to determine the hardness, H, which is defined as the mean pressure that the material will support under load. It should be noted that hardness measured using this definition may be different from that obtained from the more conventional definition in which the area is determined by direct measurement of the residual hardness impression. The reason for the difference is that, in some materials, a portion of the contact area under load may not be plastically deformed, and as a result, the contact area measured by observation of the residual hardness impression may be less than that at peak load. However, for most of the materials that have been studied, the contact areas computed using the procedure outlined here compare favorably with residual contact areas measured in the SEM, and the two definitions of hardness give similar results.

The important limitations of the current analysis method include potentially large errors associated with the application to the data obtained from inhomogeneous samples or from materials that generate significant pile-up at the perimeter of the indenters [48, 49]. Another problem is the accuracy of determining the point of contact. The indenter needs to contact the surface of a sample and then draw back before the penetrating of the

indentation to determine surface position; however, the contact point has some depth and this point may not be the real indentation point. Because the indentation depth is tested based on the surface position, any error in the point of contact will strongly affect the results.

4.6 Implementation of the method

4.6.1 Choice of indenter geometries

The analyses mentioned above are from flat punch, conical and paraboloid revolutions, in order to implement the analysis method with Vikers and Berkovich indenters, one needs to find out which of the indenter geometries can best describe the experimental data. Although it is easy to think that the best description varies from one material to another, the data from Oliver et al. [42] suggest otherwise. They re-plotted the unloading curves with the loads and displacements normalized with respect to their maximum values. When plotted this way, it is apparent that the unloading data are all remarkably similar in form. In fact, with the exception of fused silica data, which are slightly higher than the rest, the curves for the materials are so similar that they can hardly be distinguished. This suggests that unloading behavior of a wide variety of materials can be described by one single indenter geometry.

Table 4-1 power law exponents predicted by Sneddon's analyses and the relevant geometry constants

Indenter geometry	ε	m
Flat	1	1
Paraboloid	0.75	1.5
Conical	0.72	2

The power law exponent m, which describes the unloading behavior, has been used to find out which indenter geometry works best. Table 4-1 summarizes the power law exponents predicted by Sneddon's analyses and the associated geometry constants [43]. The experimental results from Oliver et al. show that the value of m for all the materials they studied range from 1.25 to 1.51 with a mean value of 1.40. Comparison of these two results shows that the unloading behavior is best described by the paraboloid

geometry, and the geometry constant ε to be used is 0.75. Why the parabolloid is a better description of the unloading behavior is probably due to the fact that the elastic singularity characteristic of the conical geometry is not physically realizable when plasticity occurs, and the pressure distribution, which actually forms around the tip of the indenter, is more like that predicted by the paraboloid indenter. It is notable, however, that even had the conical geometry been chosen, the only difference in the analysis would have been to use a slightly smaller value of ε, i.e., $\varepsilon = 0.72$.

4.6.2 Measurement of the initial unloading stiffness

One important practical question that arises in the analysis procedure is how the initial unloading stiffness, S, should be measured from the unloading data. One simple way to accomplish the measurement is to fit a straight line to a fraction of the upper portion of the unloading curve and use its slope as a measure of the stiffness. The problem with this is that for nonlinear unloading data, the measured stiffness depends on how much of the data is used in the fit.

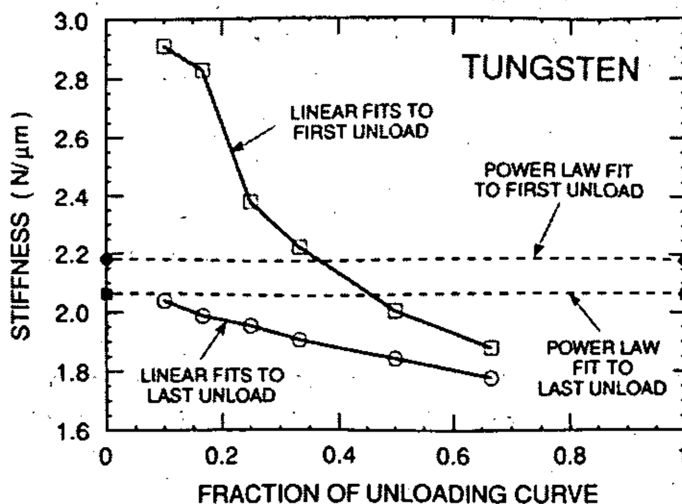


Fig. 4-3 The peak load stiffness of a 120 mN indentation in tungsten computed using linear and power law fitting of different proportions of the unloading data [42].

Oliver et al. [42] studied the influence of the proportion of data used in the fit on the value of measured stiffness. They plotted the stiffness measured for tungsten as a function of the fraction of the unloading data used in the fit in Fig. 4-3. Two features are worthy of note. First, the stiffnesses obtained from the first and last loadings are very

different based on linear fit. The reason for this is that there is a significant amount of creep during the first unloading, causing the slope of the upper portion of the unloading curve to be abnormally high. Because of this, there is no way that the proper unloading stiffness can be identified from the first unloading data from this technique if the creep influence cannot be removed. These effects can be minimized by the inclusion of peak load hold periods in the loading sequence to diminish time-dependent plastic effects. Second, it can be seen that even in the final unloading data, there is a significant variation in the measured stiffness, depending on how much of the unloading curve is used in the fit. So another better procedure is needed to get a reasonable stiffness.

This procedure is based on the observation that unloading data are well described by a simple power law relation, as directly evidenced by the excellent correlation coefficients. The relationship used to describe the unloading data for stiffness measurement is

$$P = A(h - h_f)^m \tag{4-13}$$

where the constants A, m, and h_f are all determined by a least squares fitting procedure. The initial unloading slope is then obtained by analytically differentiating this expression and evaluating the derivative at the unloading point.

Results for tungsten are shown in Fig. 4-3 as horizontal dashed lines. It is seen that the stiffness computed from the final unloading curve is very close to that of the linear fits obtained using small fractions of the last unloading data. Interestingly, when applied to the first unloading data, the power law method produces a stiffness that is only slightly greater than that derived from the last unloading curve, thereby implying that the power law method is less sensitive to creep. For these reasons, the power law method is preferred.

4.6.3 Determination of load frame compliance and diamond area function

Another important practical consideration is how well the load frame compliance and area function of the diamond indenter are known. The load frame compliance is important because the measured displacements are the sum of the displacements in the specimen and the load frame, and, thus, to accurately determine specimen displacements, the load frame compliance must be known with some precision. This is especially important for large indentations made in materials with high modulus for which the load

frame displacement can be a significant fraction of the total displacement. The area function is equally important since computation of both the modulus and the hardness depend on the contact areas through Eqs. (4-6) and (4-8).

The standard procedure used in the past for determining area functions was to make a series of indentations at various depths in materials in which the indenter displacement is predominantly plastic and measure the size of the indentations by direct imaging. Using the contact depths computed from the indentation load-displacement data, an area function is then derived by empirically fitting a function to a plot of imaged areas vs. the contact depths. Clearly, the imaging technique must have sufficient contrast, resolution and precision to accurately determine the area. Optical imaging works well for larger indentations, but cannot be used exclusively since it is usually necessary to characterize the area function well into the sub-micron range. Scanning electron microscopy is also of limited value for small indentations because the shallowness of the hardness impressions results in very poor contrast. TEM replication methods have proved useful, but they are tedious, time-consuming, and require equipment and expertise that may not be available in all laboratories.

Oliver et al. [42] propose a method for determining area functions that requires no imaging at all. The method is based on the assumption that the elastic modulus is independent of indentation depth. It is important to note that specific values for the modulus are not assumed.

The method relies on modeling the load frame and the specimen as two springs in series, in which case

$$C = C_s + C_f \qquad (4\text{-}14)$$

where C is the total measured compliance, C_s is the compliance of the specimen, and C_f is the compliance of the load frame. Since the specimen compliance during elastic contact is given by the inverse of the contact stiffness, S, Eqs. (4-6) and (4-14) combine to yield

$$C = C_f + \frac{\sqrt{\pi}}{2\beta E_r}\frac{1}{\sqrt{A}} \qquad (4\text{-}15)$$

It is thus seen that if the modulus is constant, a plot of C vs. $A^{-1/2}$ is linear for a given material, and the intercept of the plot is a direct measure of the load frame compliance. The best values of C_f are obtained when the second term on the right-hand side of Eq. (4-15) is small, i.e., for large indentations.

Aluminium was chosen to find the area function and frame compliance, because it has a low hardness, and relatively large indentations can be made. For the largest aluminium indentations, the area function for a perfect Berkovich indenter,

$$A(h_c) = 24.5h_c^2 \tag{4-16}$$

can be used to provide a first estimate of the contact area. Initial estimates of C_f and E_r were thus obtained by plotting C vs. $A^{-1/2}$ for the two largest indentations in aluminium. Using these values, contact areas were then computed for all six indentation sizes by rewriting Eq. (4-15) as

$$A = \frac{\pi}{4\beta^2}\frac{1}{E_r^2}\frac{1}{(C-C_f)^2} \tag{4-17}$$

from which an initial guess at the area function was made by fitting the A vs. h_c data to the relationship

$$A(h_c) = 24.5h_c^2 + C_1h_c^1 + C_2h_c^{1/2} + C_3h_c^{1/4} + \ldots\ldots + C_8h_c^{1/128} \tag{4-18}$$

where C_1 through C_8 are constants. The lead term describes a perfect Berkovich indenter; the others describe deviations from the Berkovich geometry due to blunting at the tip.

Because the area function influenced the values of C_f and E_r, in order to get the accurate load frame compliance and area function, the procedure needs to be applied again using the new area function and iterated until convergence was achieved.

To extend the area function to smaller depths and to check the validity of the constant modulus assumption, the procedure was subsequently applied to all the other materials. In these analyses, the load frame compliance was held constant at the value determined from the aluminium. The area of the largest indentation in each of the other materials was computed using the aluminium area function, and the modulus for each material was estimated using Eq. (4-6). The areas needed to produce a constant modulus as a function of depth for each material were then computed using Eq. (4-17). The resulting areas and the corresponding contact depths for all materials were fitted as a group using

Eq. (4-18) to define a new area function. The process of determining E_r at the largest depth for each material (using the latest area function), recalculating areas and contact modulus, and re-determining the area function, was then repeated iteratively until the area function accurately described the data for all of the materials at all depths. Note that nowhere in the procedure was a specific value for a modulus assumed, and the only assumption is that the modulus is independent of depth.

Oliver et al. [42] drew the computed contact area vs. contact depth for all the materials and the fitted result showed that all the data were lying in the same line, which means that one single area function adequately describes the data.

Oliver et al. [42] then assessed the predictive capability of the new method using the load-displacement data from the six materials: fused silica, soda-lime glass, (001) sapphire, (001) quartz, tungsten, and aluminium. The results show that the contact areas calculated from the load-displacement data and measured by direct imaging in the SEM matched well, except for the aluminium at the high loads, for which the calculated areas are slightly greater than imaged areas. This may be related to the fact that aluminium is the only material studied that has a significant pile-up around the indentation. The good agreement in contact areas also suggests that the peak load contact areas computed using the new method and the imaged residual contact areas are much the same in most materials, and thus the definition of hardness given in Eq. (4-8) is consistent with the conventional definition. It should be noted that for materials with significant elastic recovery upon unloading, such as ceramics and glasses, because during unloading the sides of the indentation elastically recovered but the corners did not, the imaged areas need to be computed according to the triangle defined by the impression corners. The data also show that the hardness and modulus computed using this method remain more or less constant over the entire range of load, i.e., the indentation size effect is very little. For materials with isotropic elastic properties, the moduli computed from this method are all within 4% of the literature values. But for anisotropic materials, the measured moduli are higher than the Voigt/Reuss average values by about 9% for the sapphire and about 30% for the quartz. The reason that causes this difference is still not clear, and the influence of elastic anisotropy on the measurement of modulus in nanoindentation is an area that requires further study.

CHAPTER 5

Experimental Programme

5.1 Introduction

The lead free solders studied in this research included Sn-3.8Ag-0.7Cu, Sn-3.5Ag and Sn-0.7Cu, and in some cases eutectic Sn-Pb was used as a reference. For the corrosion tests and some of the nanoindentation tests and in studying the influence of cooling rate, bulk solders from Multicore were used.

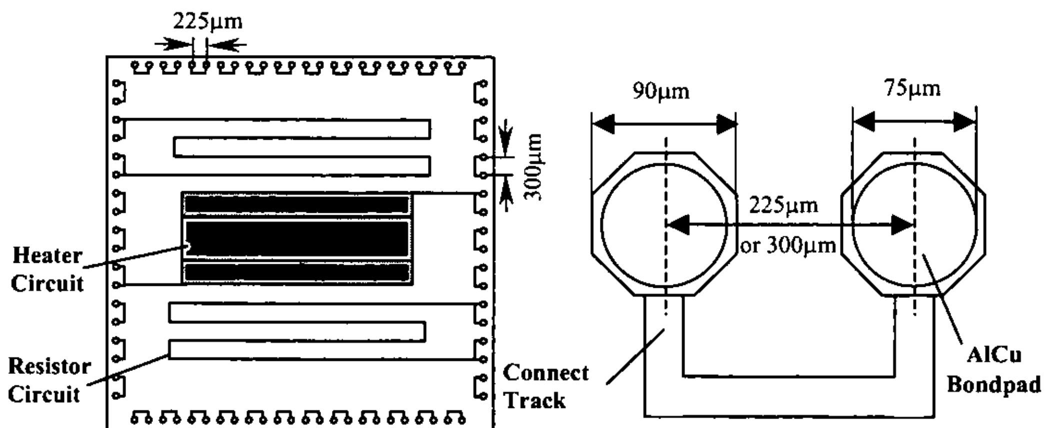


Fig. 5-1 Geometry of ASH wafer.

The silicon wafers (ASH wafer) for the experimental programme were fabricated by a commercial organization, with die on the wafer designed with a peripheral array of daisy chain interconnected bondpads with the pitch sizes of 225 μm and 300 μm as shown in Fig. 5-1. The bondpads were octagonal in shape measured 90 μm across the opposite two sides, but had circular openings in the silicon nitride passivation layer of 75 μm in diameter. Al-1wt.%Cu bond pads were deposited by sputtering with a

thickness of 1 μm. The lead free solder used in the flip chip solder joints was Sn-3.8Ag-0.7Cu, and the schematic structure of these solder bumps is shown in Fig. 5-2.

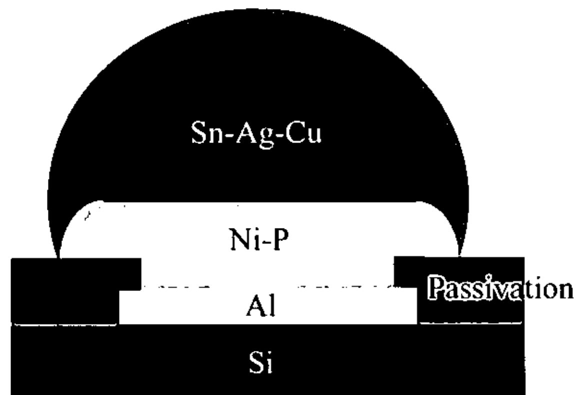


Fig. 5-2 Schematic structure of solder bump after reflow.

The under bump metallization (UBM) used was electroless Ni without immersion gold. Studies of the IMCs formed as a result of the interfacial reactions of Sn-Ag-Cu solders and different UBM, such as Al/Ni(V)/Cu [22, 36, 50-52] and Al/Ni(P)/Au [22, 53-55], have been reported, but there has been little study about the IMCs formed between Sn-Ag-Cu solders and Ni(P) UBM without Au. Although Au has been widely used to protect the Ni and improve wettability, Au can react with solder material rapidly to form a brittle $AuSn_4$ phase [56, 57] resulting in inferior mechanical properties. In the Sn-Pb system, the $AuSn_4$ phase firstly forms in the bulk solder, but after ageing it aggregates at the interface of solder and Ni_3Sn_4 layer, which can seriously degrade the mechanical properties of solder joints. In Pb-free solder systems, normally $AuSn_4$ stays in the bulk solder, which doesn't influence the mechanical properties of solder joints greatly [58]. However, this study showed that when the solder volume was restricted in the joints and the immersion gold content is relatively high, especially in the case of a micro-via, the $AuSn_4$ IMC had a greater fraction compared to the other IMCs and tended to grow into large phases with some of them aggregating at interfaces. Because the $AuSn_4$ IMC is brittle and when it grows into a large phase, it can cause stress concentration and crack initiation, which can greatly damage the mechanical integrity of the solder joints. Fig.5-3 shows a Sn-3.8Ag-0.7Cu solder joint formed on a board. The UBM on the chip was electroless Ni, and the pads on the PCB were micro-via with electroless Ni immersion Au surface finish. The white phase in the joint was $AuSn_4$, and it can be seen that a crack formed along the solder/$AuSn_4$ interface and across the $AuSn_4$ phase. So one

intention of this work was to study the properties of Sn-Ag-Cu solder joints with electroless nickel (EN) without immersion gold on the UBM, such that the negative influence of immersion gold on the mechanical properties of solder joints can be eliminated. In addition, to have more understanding about lead free solders, the wettability of EN coating with several kinds of lead free solder alloys, the corrosion and mechanical properties of bulk solders and the interface reactions of different lead free solders with different substrates were also studied.

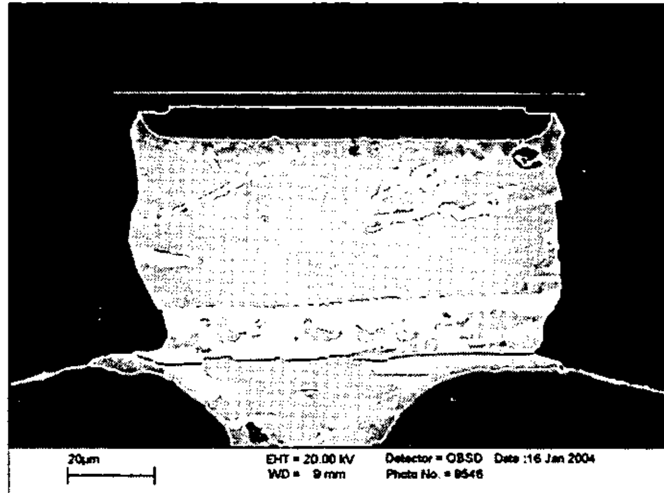


Fig. 5-3 Sn-Ag-Cu solder joint formed on the pad with micro-via.

5.2 Under bump metallization - Electroless Ni plating

Under Bump Metallization (UBM) of flip chips provides an electrically conductive, but chemically inactive interlayer to enable the minimum interaction of the bondpad metals (e.g. Al or Cu) during soldering processes and interdifussion in subsequent service life of the components. Electroless Ni (EN) plating, is a low-cost maskless process for under bump metallization (UBM) of fine pitch flip chips, and is suitable for mass production. With chemically inert characteristics and excellent conductivity, Ni metal has a low diffusion rate in solder materials; it can thereby act as a diffusion barrier to resist the formation of extra intermetallics (IMCs). Electroless Ni coating has been reported to be much more effective than electroplated Ni in preventing Cu diffusion [59].

The electroless Ni plating process used in this work is a procedure developed for the UBM of flip chip wafer bumping [7-9]. The samples used for electroless Ni plating

were half-hard Al foil with the original surface finish and a purity of 99.0%. The size of the coupon used in this test was 250 μm thick, 20 mm long and 7 mm wide.

Table 5-1 Formulation of electroless Ni plating solution.

$NiSO_4 \cdot 7H_2O$	28.8g/L
$NaH_2PO_2 \cdot H_2O$	27g/L
CH_3COONH_4	20.3g/L
$C_4H_4Na_2O_4 \cdot 6H_2O$	6.8g/L
$C_6H_5Na_3O_7 \cdot 2H_2O$	3.5g/L
CH_3COOH	15.3mL/L
NH_2CSNH_2	< 1mg/L
pH	4.5-4.8
Temperature	85°C

During deposition the samples were held using clips with plastic protection. Zincate pre-treatment was used to activate the surface before the Ni deposition. Firstly, the samples were etched in 5% NaOH solution for 20 s at room temperature to remove the oxide film on the surface. They were then cleaned with de-ionised (DI) water and dipped into 50% HNO_3 solution, again for 20 s. The concentrated HNO_3 solution was used to remove the metal "smut" and organic residues on the surface left behind by the NaOH etching. Following the HNO_3 cleaning, the samples were moved to the zincate solution for 20 s to activate the surface by depositing clusters of zinc particles on the surface. After this, they were etched in 50% HNO_3 solution for 10 s to completely remove the zinc layer and then reacted again with zincate solution for 20 s to form the final zinc layer. After every process step, the samples were rinsed with DI water. The results show that a second zincate pre-treatment could produce a more repeatable zinc layer with finer particles than achieved with a single zincate process. Finally, The samples were immersed into an electroless Ni plating solution for 20 min. Following Ni deposition the samples were thoroughly rinsed with DI water and then dried with a cool air blower. The Al coupons with the electroless Ni finish were stored in different environments for later tests. The formulation of electroless Ni plating is shown in Table 1. The stabilizer used was thiourea (NH_2CSNH_2), and its concentration was less than 1 mg/L. The thickness of the Ni-P layer after the electroless plating was approximately 6 μm and based on this procedure the P content of Ni-P coating was about 7.3wt.%.

5.3 Wettability testing

5.3.1 Storage effects on wetting and wetting environment specification

Lea and Dench [60-63] from National Physical Laboratory (NPL) studied the solderability measurement of electronic components intensively, and it seems that wetting balance is a good method that can be used to study the wettability of components. In this research, the solderability of electroless Ni was tested with the RPS 6-SIGMA Wetting Balance Tester equipped with lead-free solder baths as shown in Fig. 5-4. The fluxes used in these tests were Multicore ACTIEC 5 (rosin strongly activated), ACTIEC 2 (rosin mildly activated) and SM/NA (non-activated), and the lead free solders were Sn-3.8Ag-0.7Cu, Sn-3.5Ag and Sn-0.7Cu. The bath temperature for wetting tests was controlled to 240°C. Nitrogen was available to provide an inert environment. The oxygen concentration in the wetting environment was controlled through the nitrogen flow and tested using Z210 Oxygen Analyzer. During the wettability tests, after the coupons were dipped with flux they were preheated for 20s over the solder bath at a distance 1mm from the bottom of the coupon to the top of the solder. Then the coupons were dipped 8 mm into the solder bath for 25 s. The wettability was evaluated from the wetting curves obtained with the specific solder material.

Fig. 5-4 RPS 6-SIGMA Wetting Balance Tester.

Different fluxes, with and without nitrogen protection, were used to explore which kind of flux and wetting environment were needed for different lead free solders to wet the EN coating. When strong flux was used, different nitrogen flows were applied to learn the requirement to oxygen concentration in the wetting environment. During these tests, the nitrogen pressure was controlled at 1.5 bars and nitrogen flow was controlled by turning the valve.

The EN plated samples were also stored prior to testing in an ambient environment and a freezer for different periods of time before the wetting tests, to examine the influence of storage on the wettability. Multicore ACTIEC 5 flux was used in these tests and some samples were tested under nitrogen protection with the concentration of oxygen about 210 ppm.

5.3.2 Surface roughness effects on wetting

In order to study the influence of surface roughness on the wettability of the EN coating, the electroless Ni was plated on Al substrates with different surface roughnesses. Before plating the Al coupons were ground with different silicon carbide papers, comprising of grit 240, 400, 600, and 1200. The samples were turned about 90° after grinding in one direction and then ground until the primary grinding tracks were removed completely. Several grindings were conducted on each sample. Before and after the EN plating, the roughness of the samples were tested with a TAYLOR-HOBSON Talysurf 4 Machine in both the directions parallel and perpendicular to the rolling direction of the Al foil or the final grinding tracks.

The wettability of EN coatings on Al substrates with different surface roughness were tested and compared immediately after the EN plating. Multicore ACTIEC 5 flux and nitrogen protection were used during these tests, and the solder materials used were Sn-3.8Ag-0.7Cu and Sn-3.5Ag.

SEM and AFM were used to study the microstructure and morphology of Al coupon before and after the electroless Ni plating. After storage in the ambient environment for different periods the coupons were analysed by XPS to study the oxidisation behaviour of the electroless Ni coating.

5.4 Stencil printing

In order to form the solder bumps after the electroless Ni UBM, solder dipping was attempted, but it proved difficult to achieve a sufficient solder volume to form adequate solder joints during assembly with the PCB or other components. Because stencil printing is potentially low in cost, it was used in the study to form the solder bumps.

Fig. 5-5 DEK 265 stencil printing machine.

The equipment needed in stencil solder bumping includes: a wafer holder to locate the wafer in the machine during printing, a suitable stencil with the requisite apertures and, a printing machine with adequate accuracy and repeatability. The printing machine used in this research was DEK 265 Horizon, as shown in Fig. 5-5, and the stencil had the required pattern of apertures to match the wafers or other components (e.g. PCBs). This pattern of apertures was formed of many small holes, which can be produced through electroplating (Ni stencils), chemical etching and laser cutting (stainless steel stencils). The solder material used was Sn-3.8Ag-0.7Cu solder paste, type 6 and type 7, with very small particle sizes.

Before printing the wafer was held in a wafer holder with vacuum, and the stencil was fitted to the printing machine. By using the fiducials on both the wafer and the stencil and a two-way digital camera, the wafer and stencil were aligned to each other. The solder paste was dispensed onto the stencil, and by means of the squeegee the printing

machine rolled the solder paste and pressed it through the small holes in the stencil, such that the solder paste was deposited on the wafer pads. Some parameters could be chosen before the printing, such as squeegee pressure, printing speed and gap between stencil and wafer, which could influence the solder volume and the quality of solder bumps formed on the wafer.

Fig. 5-6 T-Track reflow oven.

5.5 Reflow

After stencil printing, the wafers with the solder paste were reflowed in a convection oven with a nitrogen inert environment. The oven used was a Planer T-track reflow oven, as shown in Fig. 5-6. The reflow profile (temperature vs. time history) was controlled by a pre-set program. Because the melting temperatures of lead free solders are higher than that of eutectic Sn-Pb solder and a certain margin is needed to melt the solder completely during reflow, the reflow profile for lead free solder materials is critical to successful bump formation. To maintain compatibility with current assembly facilities, the top reflow temperature cannot be too high. Currently, it is thought that 240°C is necessary for lead free reflow soldering. Another issue that can influence the reflow profile is the thermal properties of PCB materials, such as FR-4. The polymeric materials can withstand a maximum temperature of 230-250°C for 90-120 s without onset of degradation. It is thought by industry that the time above the melting temperatures of lead free solders, such as 217°C for eutectic Sn-Ag-Cu solder, needs to be controlled between 30-90 s. Following these criteria, the reflow profile used is shown

in Fig. 5-7 with two ramp stages and one soak stage during the temperature-time regime. The top temperature was 246°C and the durations for temperature above 217°C and 240°C were about 86 s and 15 s respectively. After reflow, truncated-sphere solder bumps formed on the substrates.

During reflow the solder was heated past its melting temperature and then reacted with the connection pad and UBM whilst in its liquid state. IMCs formed at the interfaces to give good adhesion strength. The time for the solder to be kept liquid is very important for the liquid reactions, and different reaction times would produce different volumes and thicknesses of the IMCs.

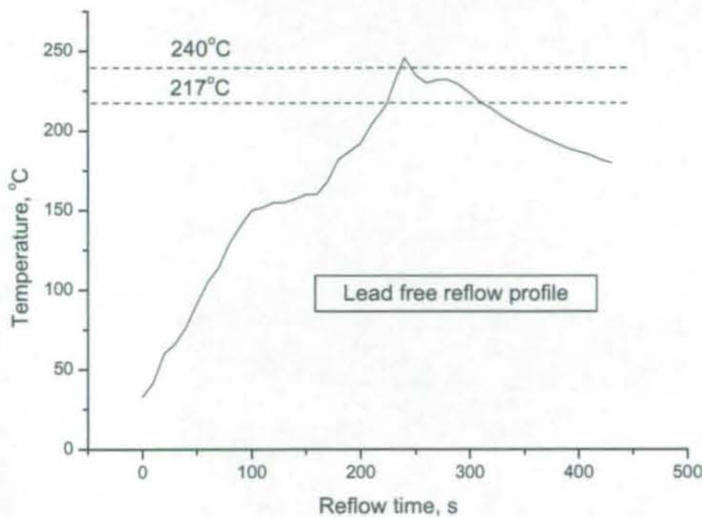


Fig. 5-7 Lead free reflow profile.

5.6 Assembly and underfill

Two kinds of assembly machines, a Karl Suss FC6 and FineTech Electronic pick and place machine, as shown in Fig. 5-8 and 5-9 respectively, were used to assemble the chips and PCBs together. Both of these machines have a two-way camera, and the FC6 has a semi-automated alignment function, but the pick and place machine required manual alignment. Indalloy Tacflux, specific to lead free assembly, was used. This semi-solid flux was spread on a tray to form a thin layer about 10-20 μm thick and the chip touched to this flux layer to pick up some flux before the assembly stage. The chip and the PCB were then aligned using the two-way camera and assembled. After the

assembly was finished, the components were reflowed again in the reflow oven to form the joints.

Due to the substantial difference in the coefficient of thermal expansion (CTE) between the chip and the substrate, strain and stress can accumulate when the components are subjected to thermal shock or cycling, which may result in failure of the solder joint. An effective solution is to encapsulate the chip and the substrate with an underfill material, which can reduce the deformation of the chip and substrate and improve the long-term reliability of flip chip. Underfill materials used in flip chip assemblies consist of a composite of polymer and filler particles (e.g. silica). The underfill must have low viscosity, good thermal and chemical stability, good adhesion to the interfaces after curing, a CTE close to solder, and high modulus and strength. It has been reported that the fatigue life of solder joints improves when the underfill has a lower CTE, a high Young's modulus and a high glass transition temperature [64, 65].

Fig. 5-8 Karl Suss FC6 assembly machine.

Fig. 5-9 FineTech Electronic pick and place machine.

The underfill used in this study was Loctite Hysol FP4527 with a low viscosity and small filler particles, which can fill a gap as small as 25 μm. The components were heated to 70-80°C using a hot plate, and then the underfill was injected from two perpendicular sides of the connection gap between the chip and the substrate until the

underfill could be seen from the opposite sides. The assembly was then cured in an oven at 150 ± 3°C for 40 min.

5.7 Thermal ageing and thermal cycling

When an electronic device is switched "on" and "off", and when the operational temperature is changed from high to low and vice versa, it may suffer thermal shock and cycling. These operational conditions can change the microstructure of solder joints and cause the stress concentration, resulting in deformation and crack propagation. When an electronic device is exposed to a high temperature for a long time, the properties of the solder joints are affected due to IMC growth and microstructure evolution. As such, it is necessary to assess the properties of electronics materials through thermal ageing and thermal cycling.

Thermal ageing was used to study the influence of temperature and time on the microstructure evolution and IMC growth. In order to study the influence of temperature on thermal ageing, three different temperatures were used, these being 80°C, 150°C and 175°C. The ASH chips were put inside a convection oven that could control the temperature within ±1°C at these temperatures for up to 45 d, 18 d and 30 d, respectively. In order to study the influence of ageing time, some of the chips were taken out after ageing for certain periods. The kinetic mechanism of the IMC growth was analysed according to the ageing data from the three different ageing temperatures.

Thermal cycling is an accelerated test for the reliability of assembled components that may be applied in both high temperature and low temperature regimes. Due to the substantial difference in CTE between the chip and substrate, stress and strain can accumulate in the solder joints during thermal cycling and cause the initiation and propagation of cracks, resulting in joint failure. There are many different temperature ranges that are currently used in thermal cycling, such as -25~125°C, -40~125°C, -55~125°C, and -20~110°C. The upper temperature for thermal cycling cannot be too high, because the glass transition temperature of the PCB is about 120°C and the PCB cannot survive for long in high temperatures. The conditions for thermal cycling are decided by the temperature profile. Even the same temperature range can have different

influences on the solder joints, as they can be applied with different dwell times and different temperature increment and decrement rates.

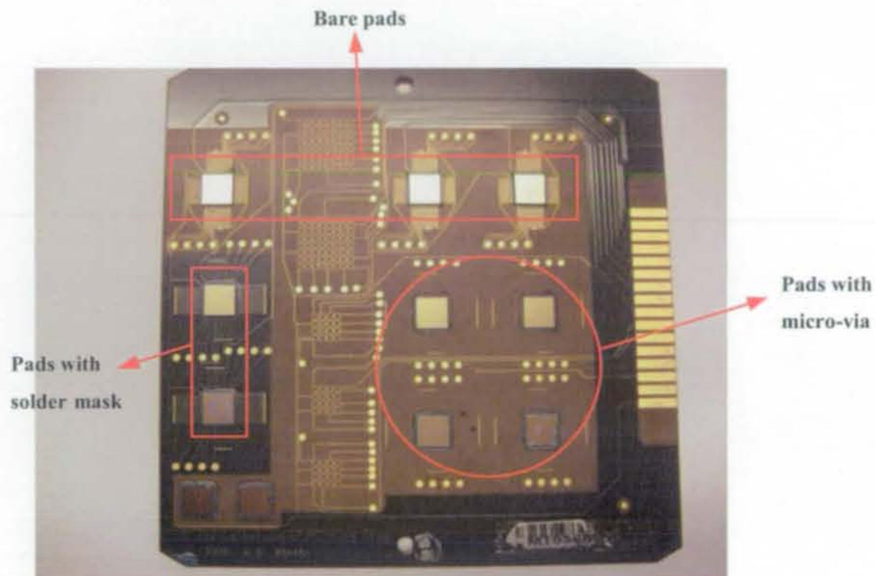


Fig. 5-10 MT030 board assembled with ASH chips.

Fig. 5-11 CTS thermal cycling machine.

The samples used for the thermal cycling tests were ASH chips assembled with MT030 boards as shown in Fig. 5-10. The surface finish on the boards was electroless Ni with immersion gold (ENIG); however, the pads on the boards were produced by different methods as indicated in Fig. 5-10, i.e., by means of microvia, solder mask, and bare pads. The pads were formed as a peripheral daisy chain with test pads that can be used to assess the electrical resistance of the whole chain and individual connects. Isolated

pads were also provided on the boards for solely studying the microstructure of the solder joints. Some of the boards were cut with a low speed diamond saw into small pieces with single flip chip pad array and then assembled with one ASH chip. Both the whole boards and boards with single device pad arrays were studied.

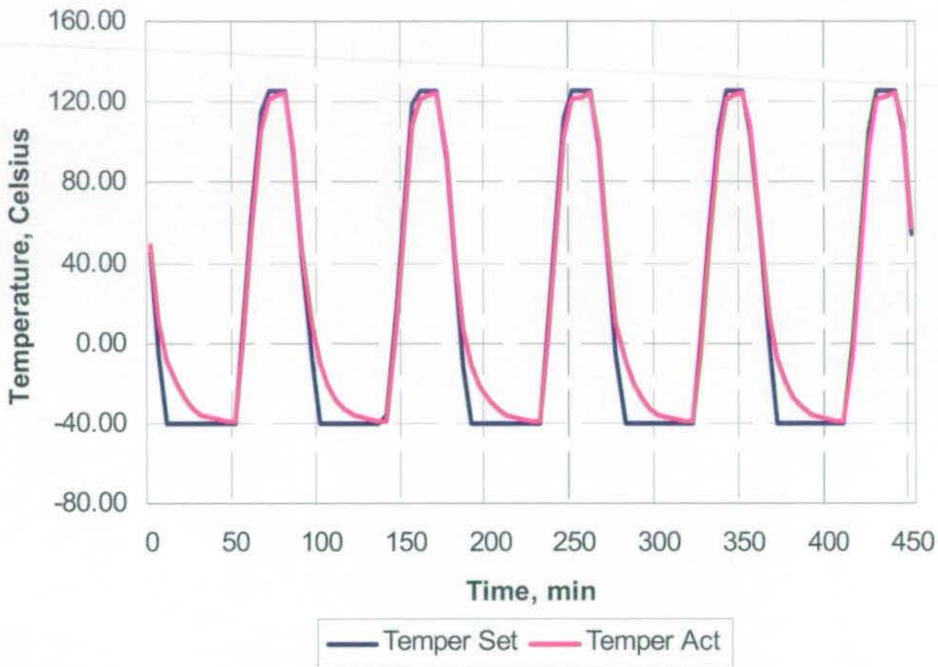


Fig. 5-12 Temperature profile of thermal cycling.

The thermal cycling machine used in this study was a CTS cycling machine, as shown in Fig. 5-11. After assembly and underfill, the components were put into the thermal cycling chamber. The temperature range used was from -40 to 125°C, and the temperature profile is shown in Fig. 5-12. The ramp rate was about 11°C/min, and the temperature increasing and decreasing between -40 and 125°C took about 15 min. Due to the slow cooling rate in the low temperature range the dwell time at -40 and 125°C was set as 40 min and 15 min respectively in the designed profile to keep the actual dwell time at high and low temperatures about 15 min. The time for one cycle was about 90 min. Before the thermal cycling and after 50, 100, 200, 300, 400, 500, 750, 1000 and 1500 cycles, the electrical resistance of the samples were tested and after 100, 500 and 1000 cycles some of the samples with the three kinds of different pads on the PCB, i.e., microvia, solder mask and bare pad, were taken out for analysis. Several samples remained in the chamber for up to 1500 cycles.

After thermal ageing and thermal cycling, the samples were mounted, cross-sectioned and polished. SEM with EDX and/or EBSD was used to analyse the microstructure and IMC evolution.

5.8 Interfacial reactions between different solders and substrates

In order to study the interfacial reactions between different lead free solders and different substrates and to grow large IMCs for nanoindentation to test their mechanical properties, different lead free solders were exposed to several long-duration reflow cycles and ageing regimes on different substrates, with the intermetallic compounds (IMCs) and microstructure then analysed using SEM with EDX.

The lead free solders, Sn-3.8Ag-0.7Cu, Sn-3.5Ag and Sn-0.7Cu, used in this study are solder pellets, and the substrates include Cu, electroless Ni (EN), immersion Ag on Cu (CuImAg) and electroless Ni immersion gold (ENIG). The electroless Ni was coated on Al foil with a thickness of 250 μm following a procedure developed for the UBM of flip chip wafer bumping [7-9], and the thickness of the EN coating was about 7 μm. The ImAg and ENIG substrates were taken from a series of test boards. Before reflow, the substrates were cleaned in acetone with ultrasonic assistance for 2 min and rinsed with isopropanol (IPA).

The reflow was conducted in T-Track reflow oven with a nitrogen inert environment. After being dipped with flux, the solder pellets were put on the substrates and heated to 270°C for a duration of 8 min (T-Track oven does not support long dwell times at high temperature). The temperature in the chamber was then dropped to 40°C, and then increased again to 270°C again for another 8 min dwell. 10 such reflow cycles were applied on each sample with the total time at 270°C amounting to 80 min. The flux used was specific to the different substrates because they have different solderabilities with lead free solders. For Cu, CuImAg and ENIG substrates, Multicore rosin mildly-activated flux ACTIEC 2 was used, and for the EN substrate, the Multicore rosin strongly-activated flux ACTIEC 5 was used. After the reflow cycles the samples were aged at 80°C for 10 days and then 150°C for 18 days.

To avoid thermal shock caused by the T-Track oven during the multiple-reflows, which may cause the formation of cracks in the IMCs, the samples for nanoindentation tests were reflowed in a furnace with ventilation and without nitrogen protection. These samples included Sn-3.8Ag-0.7Cu and Sn-0.7Cu on a Cu substrate and Sn-3.5Ag on an EN substrate. For Cu and EN substrates, the fluxes ACTIEC 2 and ACTIEC 5 were used, respectively. The furnace was preheated to 250°C prior to loading the samples. After the solder pellets were dipped with flux and put on the substrates, the samples were put into the furnace, and the temperature of the furnace was increased to 270°C. The samples were kept at this temperature for 90 min and then cooled inside the furnace.

5.9 Solidification with different cooling media

In order to study the influence of cooling rate on the microstructure and mechanical properties of lead free solders, both ASH wafer bumps and bulk solders were melted and cooled in different media.

The ASH wafer bumps were produced by a commercial organization. In this study, the second reflow stage was conducted and then cooled in different media. The reflow was carried out in the T-Track oven with a nitrogen inert environment. After the temperature was stable at 272°C, the chips were kept in the chamber for about 2.5 min, and the top temperature of the reflow was about 280°C. For furnace cooling, the chips were cooled inside the chamber; for air cooling, the chip was taken out immediately and cooled in the ambient environment and for water cooling, the chip was taken out and immediately quenched in cool water.

For the bulk solder experiments, solder bars were cut into small parts and put into crucibles of 20 mm in diameter and 25 mm in height. The crucibles were put into a ventilated furnace. The temperature of the furnace was increased to 330°C and kept there for half an hour, and then the crucibles were cooled with the same regimes as applied to the ASH chips.

5.10 Shear tests

When an electronic device is in operation, the solder connections are subjected to mechanical stresses and strains due to the different coefficients of thermal expansion within the board and the component. An example of how these stresses are generated, in the case of flip chip packages, between the silicon die and the substrate, is shown in Fig. 5-13 [2]. Normally, the melting temperature of solder material represents the unstrained condition. When the operational temperature is beyond or below this temperature, because the board and the component will expand or contract to different degrees, the solder ball connection is subjected to a shear strain. As the system is switched "on" and "off", it is subjected to thermal cycling, resulting in the solder connection being subjected to cyclic shear stresses. The residual shear-strain will be determined by the shear modulus of the particular solder materials. The solder connections may fail because of fatigue after some cycling. Plastic deformation is also possible, if the shear stress exceeds the yield shear strength.

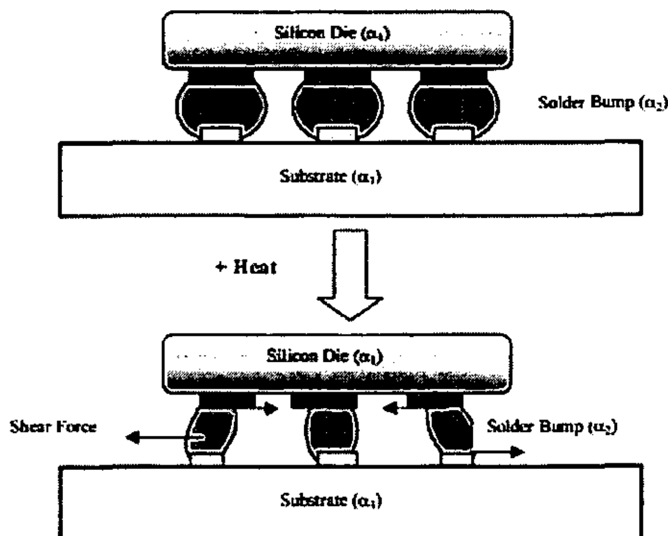


Fig. 5-13 Solder joints subjected to shear strain during thermal cycling due to CTE mismatch between the Die (α_1), the solder (α_2) and the substrate (α_3) [2].

There are two kinds of tests that can be done to measure the shear strength of solder joints: one is to shear the solder bumps directly, and the other is to shear the samples after assembling the chips on board. Different shear heads and shear rates can be used in

shear tests. Because some mechanical properties are rate sensitive, i.e., they may change greatly with different shear rates, the shear rates need to be specified for the shear tests for later comparison with the results of other authors.

In this study, bump shear was used to test the shear strength of the Sn-Ag-Cu solder bumps, and the shear test facility used was the Dage Series 4000 Bondtester, as shown in Fig. 5-14. The shear head used was BS250. The shear height and shear speed can influence the measured shear strength of the solder bumps and joints, so in these tests, for the as-reflowed ASH chips, different shear heights were examined, i.e., 10 μm, 15 μm, 20 μm and 25 μm, and different shear speeds were used, i.e., 50 μm/s, 100 μm/s, 150 μm/s and 300 μm/s. For the aged samples, the shear speed was kept as 150 μm/s. The other parameters for the shear tests were kept consistent for all the tests, and they are: test load, 100 g; load speed, 100 μm/s and overtravel, 100 μm. For statistical purposes, at least 15 bumps were sheared for each testing protocol.

Fig. 5-14 Dage Series 400 Bondtester.

The fracture surface and cross-sections of the sheared solder bumps were studied using an SEM to locate the position of the fracture surface and to analyse the fracture mechanism.

5.11 Nanoindentation tests

With the miniaturization of electronic packaging, solder joints are becoming smaller. The solder connections form a multi-layered structure and the IMCs formed inside the solder joints are normally in the scale of several microns or even less than one micron. As such, conventional testing methods cannot be used to study the interfacial properties of solder joints. Nanoindentation can provide some information about the mechanical properties of different layers by measuring the force and the depth of indentations made in the actual solder joints because nanoindenters have small testing heads and high position resolution. Nanoindentation can put the first indentation within a few microns of a given location and the remaining indentations of the array can be placed with respect to the first with a resolution of 0.5 μm.

In this research, nanoindentation was used to study the solder joint properties, including the mechanical and creep properties of bulk solders, small solder joints from flip chips, and large phases formed with different lead free solders and substrates.

Fig. 5-15 Micro Materials NanoTest 600 nanoindentation.

Fig. 5-15 shows the Micro Materials NanoTest 600 Nanoindentater used and Fig. 5-16 is a schematic diagram of the functional parts. A diamond indenter is fixed to the end of a load shaft that is connected to a pendulum. The pendulum is the heart of nanoindentation, which can rotate around a frictionless pivot. A coil next to a permanent

magnet is mounted at the top of the pendulum. When the coil is supplied with a current it will be attracted towards the permanent magnet, producing motion of the diamond indenter towards the sample and into the sample surface. The displacement of the indenter is measured by means of a parallel plate capacitor. Motion of the indenter toward the sample is measured by a capacitance displacement gage with a displacement resolution of 0.2 nm. The indentation made by the indenter is not observed but rather is determined from the measured depth of the indentation and the known shape of the indenter.

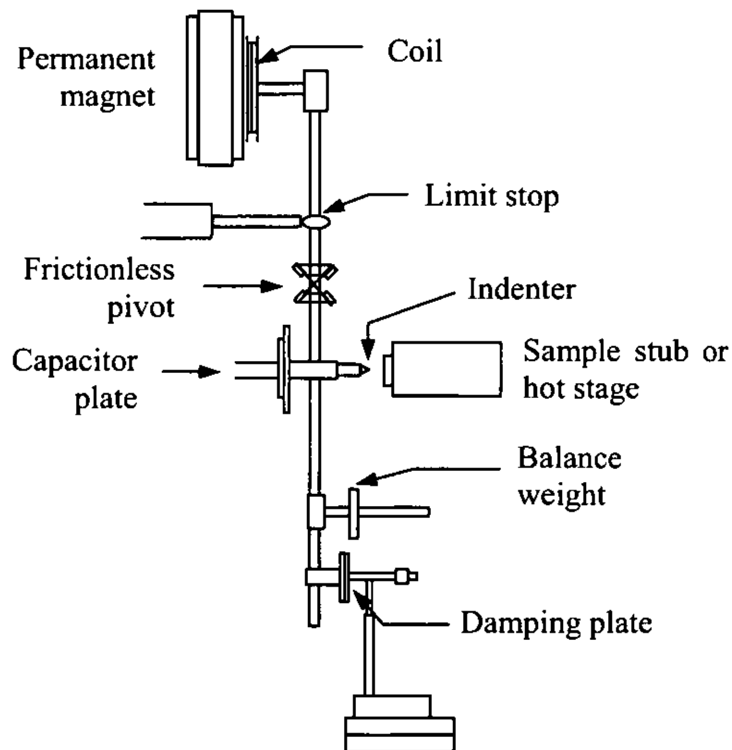


Fig. 5-16 Schematic diagram of nanoindentation.

The test was conducted in a chamber that can control the temperature and humidity, and during the test the temperature is controlled at 22 ± 0.1°C. Before the test, samples were ground and polished and finished with 0.02 μm silica suspension. For the tests at ambient temperature, samples were directly mounted onto a metal stub by cyanoacrylate adhesive. The tests at elevated temperature were conducted at 80°C, 115°C, 125°C, 150°C and 175°C and for this the samples were mounted onto a hot-stage using a special type of cement. Before the temperature was increased to the test temperature, the cement was heated to 100-110°C for at least 12 hours for the cement to cure. The hot-

stage can control the temperature of samples within 0.1°C, and the maximum temperature that it can reach is around 500°C. In all the tests, a three-faced Berkovich diamond indenter was used, which has the same area-to-depth relationship as a four-faced Vickers indenter. For the tests at the elevated temperature, after the temperature of samples reached the test temperature and became stable, the indenter was pre-contacted with the sample for 5-10 min to warm up the indenter. With this enabled, during the subsequent tests the indenter remained at almost the same temperature as the sample. A load-control method was used during the nanoindentation tests. The maximum loads used in this test were 3 mN, 5 mN and 10 mN and the loading rate was set as 0.15 mN/s, 0.25 mN/s and 0.5 mN/s respectively for the different maximum loads. When the load reached the maximum value, it was held for a certain period (dwell time) to reduce the influence of creep on the hardness and modulus measurement. Different dwell times from 10 s to 120 s were used for different phases, due to their different creep properties.

The creep property of Sn-3.8Ag-0.7Cu, Sn-3.5Ag and Sn-0.7Cu lead free solder materials was also tested. Again, the indenter pre-contacted with the sample for 5-10 min. The creep loading used was 3mN, 5mN or 10mN. In these loads the indenter was held for 30 min to fully develop the creep behaviour.

Prior to nanoindentation, the samples were analysed by SEM with EDX to examine microstructure and phase distribution, so that during nanoindentation interesting phases can be targeted to explore the mechanical properties. Because some of the samples were tested at elevated temperatures and the testing could last several days, during the tests the microstructure of the samples could evolve. Therefore, after nanoindentation, the samples were again analysed to compare differences in microstructure before and after testing. The positions of indentations in the solder joint were confirmed by SEM and for some of the samples EDX mapping was used to reveal the composition in different indentations.

5.12 Corrosion tests

Solder alloys could be exposed to air, moisture, air pollutants from industry and oceanic environments, depending on their application, so they must be resistant to such corrosion media. The potentiodynamic polarization test has been widely used to study the corrosion properties of materials [66-70]. In order to test the corrosion resistance of solder materials, the potentiodynamic polarization test was conducted to test the polarization curves using an ACM AutoTafel HP testing machine. A 3.5wt.% NaCl solution was used to simulate the use environment of electronic components in oceanic environments.

The solders used for corrosion tests were Sn-3.8Ag-0.7Cu, Sn-3.5Ag and Sn-0.7Cu lead free bulk materials, and eutectic Sn-Pb solder was used as reference. The solder materials were cut into blocks and soldered with copper wire with a plastic insulating layer and then mounted with SAMPL-KWICK mounting material, presenting an exposed area of about 100 mm^2. The cell consisted of solder material as a working electrode, a platinum foil as counter electrode and a saturated calomel electrode (SCE) as a reference electrode with a Luggin capillary bridge connected with the testing solution. The distance between working electrode and counter electrode was about 35-40 mm. The first sample was tested from -2000 to 4000 mV to check the activation area and passivation area, and then the potentiodynamic polarization experiments were conducted from -800 to 2500 mV at room temperature. Prior to the polarization scanning, the samples were cathodically treated at -1000 mV for 5 min in 3.5wt.% NaCl solution. At least three samples were tested for each testing condition.

The microstructure and composition of the corrosion products were analysed by SEM with EDX, and XRD was also used to identify the corrosion products of different solder materials after the potentiodynamic polarization testing.

5.13 Analysis techniques

5.13.1 SEM, EDX and EBSD

Several Scanning Electron Microscopes (SEM) were used to examine microstructure and morphology, analyse the surface compositions and identify the phases of solder joints and other samples. A Zeiss LEO 440 SEM without the Energy Dispersive analysis of X-ray (EDX) function can only take static images; A Zeiss LEO S360 SEM and Zeiss LEO 1530VP Field Emission Gun SEM (FEGSEM) can both do the EDX analysis, and the LEO 1530VP FEGSEM also has the Electron Back-Scatter Diffraction (EBSD) function. The secondary electron (SE1) image or backscatter electron (QBSD) image was taken for different samples. Before the SEM analyses, some of the sample were etched, with the etching solution consisting of 1 part of acetic acid, 1 part of nitric acid and 4 parts of glycerol. The etching took 20 s and then the samples were cleaned in DI water with ultrasonic assistance to remove the residues of the corrosion products, or the samples were etched 20 s with ultrasonic assistance and then cleaned with DI water.

5.13.2 X-ray photoelectron spectroscopy

The degree of oxidation of EN coating was analysed through X-ray Photoelectron Spectroscopy (XPS). In XPS analysis, Al K_α radiation was used as the x-ray source and a 90° take-off angle is applied to maximize the depth of analysis. The pass energy and dwell time used were 85 eV and 3ms for the XPS survey scan, and 25 eV and 20ms for individual scans. The charging during the analysis caused the shifting of the binding energy, and the energy scale was calibrated using C 1s peak coming from the contamination.

5.13.3 X-ray diffraction

X-Ray Diffraction (XRD) was measured using a Bruker D8 x-ray diffractometer. The samples were scanned in 2-theta angle from 5° to 100° with a step of 0.02°/s. The x-ray source used was Cu K_α radiation (λ=0.15406 nm), with an anode current of 40 mA and a tube voltage of 40 kV.

5.13.4 Atomic force microscopy

A Dimension 3100 Atomic Force Microscope (AFM) was used to analyse the surface morphology of samples to understand the mechanism of wetting and the factors that influence wettability. The surface morphology and roughness of the electroless Ni coating were analysed by AFM with the Tapping Mode. AFM was also used to analyse the pile-up and sink-in phenomena for nanoindentations in different phases.

CHAPTER 6

Results

In order to have more understanding of lead free solders and their application in flip-chip scale packages, the properties of lead free solders and solder joints were examined and are presented in this chapter, including the following studies:

- Wettability of electroless Ni with lead free solders;
- Microstructure evolution of Sn-Ag-Cu solder joints;
- Intermetallic Compound (IMC) growth and distribution in solder joints, and,
- The mechanical properties of lead free solders.

These results of these studies are discussed in detail in Chapter 7.

6.1 Wettability of electroless Ni with lead free solders

In order to use the EN coating without immersion Au as the UBM in lead free solder packages, the wettability of EN coating on Al substrate with lead free solders was studied. Figs. 6-1 and 6-2 show the microstructures of an Al substrate after a second zincate process and subsequent EN plating, respectively. It can be seen that after the zincate process some Zn particles were deposited on the Al surface, which act as active points for EN plating and that, after EN plating the Ni-P coating is present on the surface of Al as a cluster of nodules.

The concentration of oxygen in the wetting test environment was controlled by adjusting a nitrogen flow. In order to study the influence of oxygen concentration on the wettability of EN coating, the oxygen concentration with different nitrogen flows was

tested. Fig. 6-3 shows the relationship of oxygen concentration with the nitrogen flows. It can be seen that the oxygen concentration dropped parabolically with the increase of nitrogen flow.

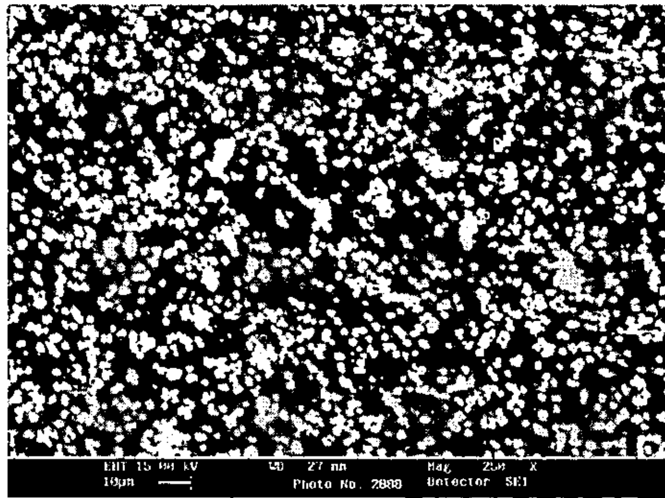


Fig. 6-1 Microstructure of an Al substrate after zincate pre-treatment.

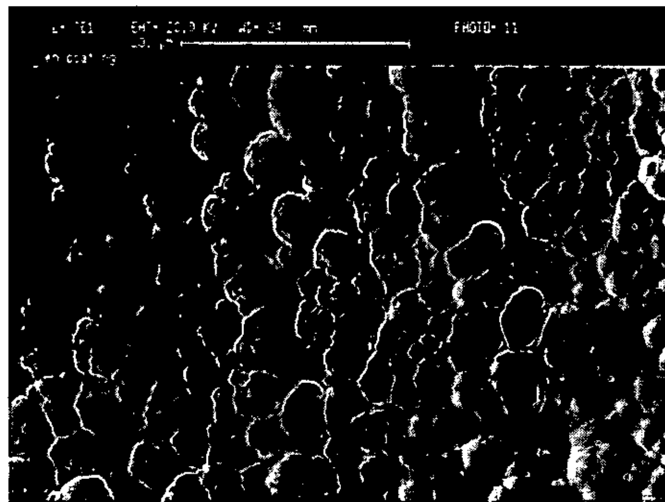


Fig. 6-2 Microstructure and morphology of EN coating.

6.1.1 Wettability with different storages

Fig. 6-4 shows the maximum wetting force and time to wet (the time for the wetting force to reach zero again) for an EN coating in Sn-Ag-Cu solder after storage in an ambient lab environment for different periods of time. There was some variation in the wettability of EN coating due to the minor difference of surface condition. However, it can be seen that the storage in an ambient lab environment did not influence the

maximum wetting force for the EN coating, although the time to wet did increase with storage duration.

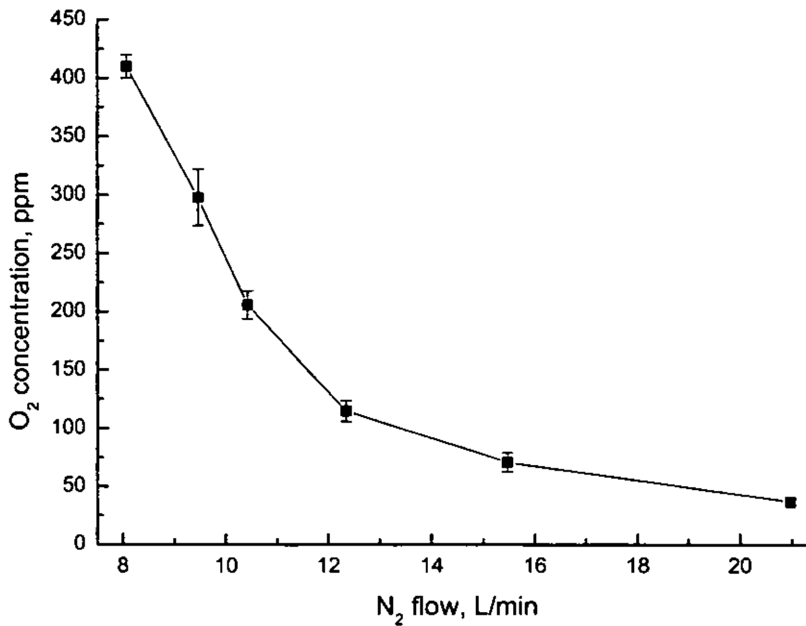


Fig. 6-3 The oxygen concentrations with different nitrogen flows.

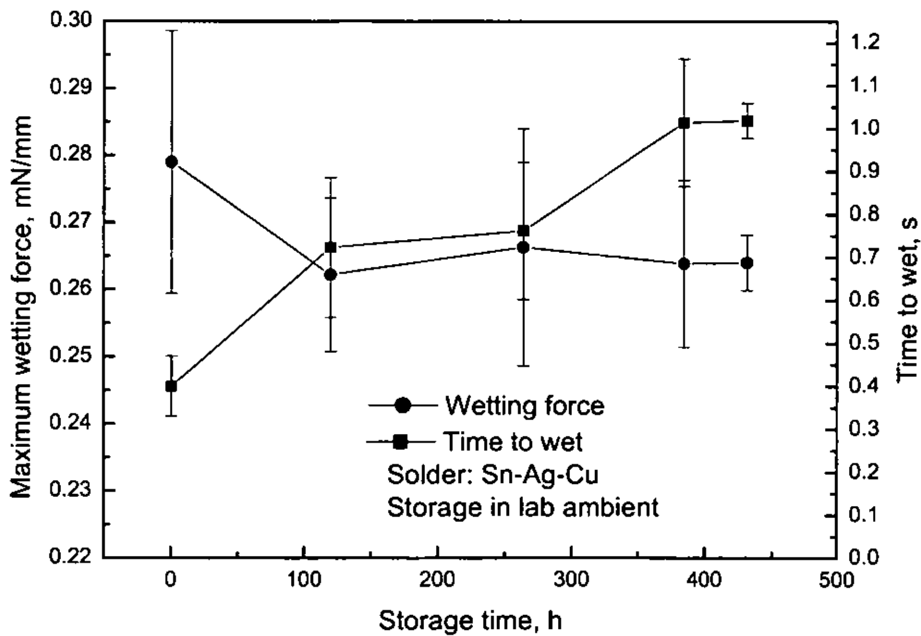


Fig. 6-4 The maximum wetting force and time to wet of EN coatings in Sn-Ag-Cu solder during the storage in lab ambient.

Fig. 6-5 shows the wetting force and time to wet of EN coatings in Sn-Ag-Cu solder after storage in a freezer for different periods of time. It can be seen that whether from

the point of view of maximum wetting force or time to wet, the storage in the freezer did not significantly influence the wettability of EN coatings with Sn-Ag-Cu solder.

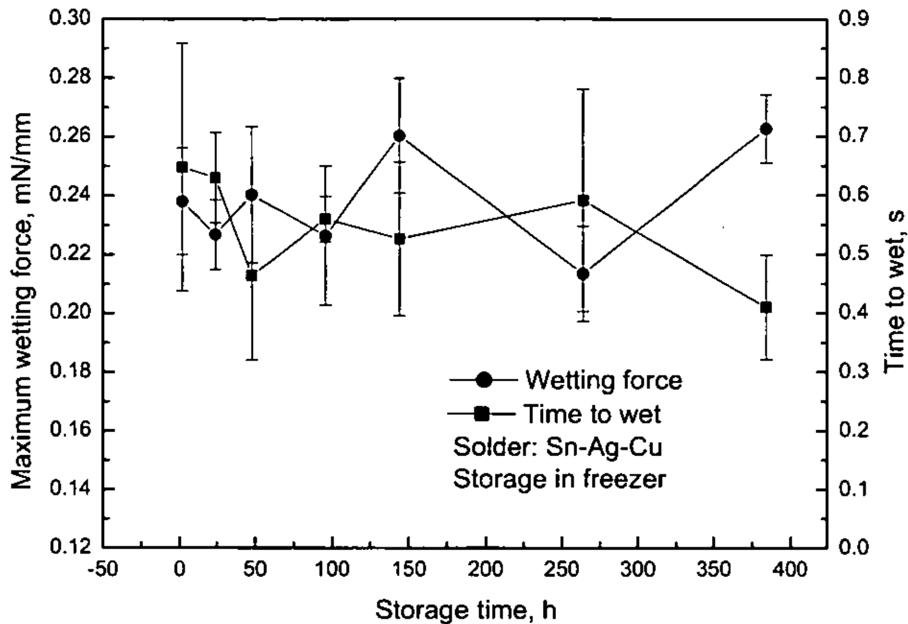


Fig. 6-5 The maximum wetting force and time to wet of EN coatings in Sn-Ag-Cu solder during the storage in freezer.

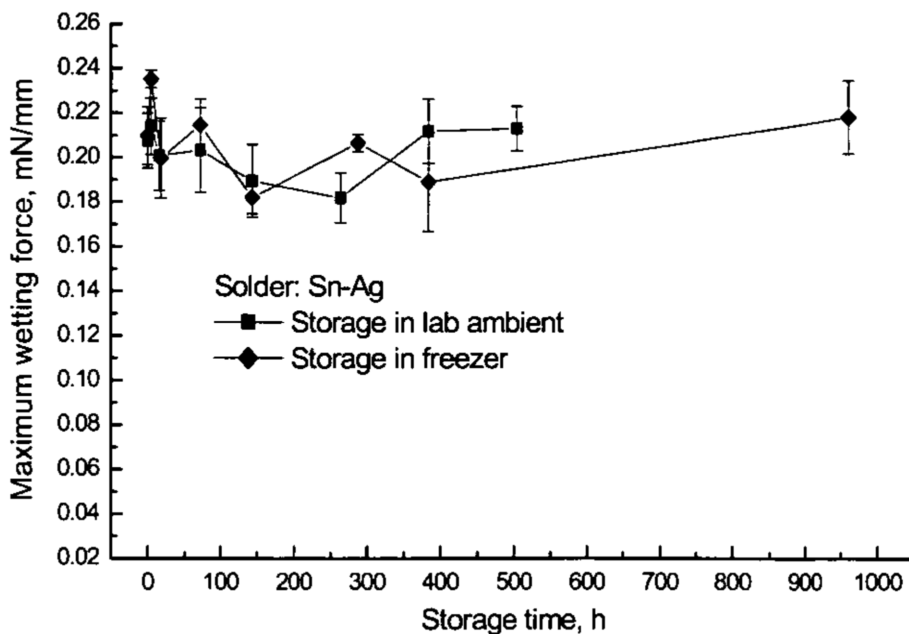


Fig. 6-6 The maximum wetting force of EN coatings in Sn-Ag solder without nitrogen protection during the storage in ambient environment and freezer.

Fig. 6-6 shows the maximum wetting force for an EN coatings in Sn-Ag solder without nitrogen protection after storage in the ambient lab environment and freezer for different

periods of time. It can be seen that the storage in both the ambient lab and freezer did not influence the wettability of EN coatings. The maximum wetting force showed similar results after the storage in ambient lab and freezer, which meant that the storage environment also did not influence the wettability of EN coatings with Sn-Ag solder when a strong flux was used.

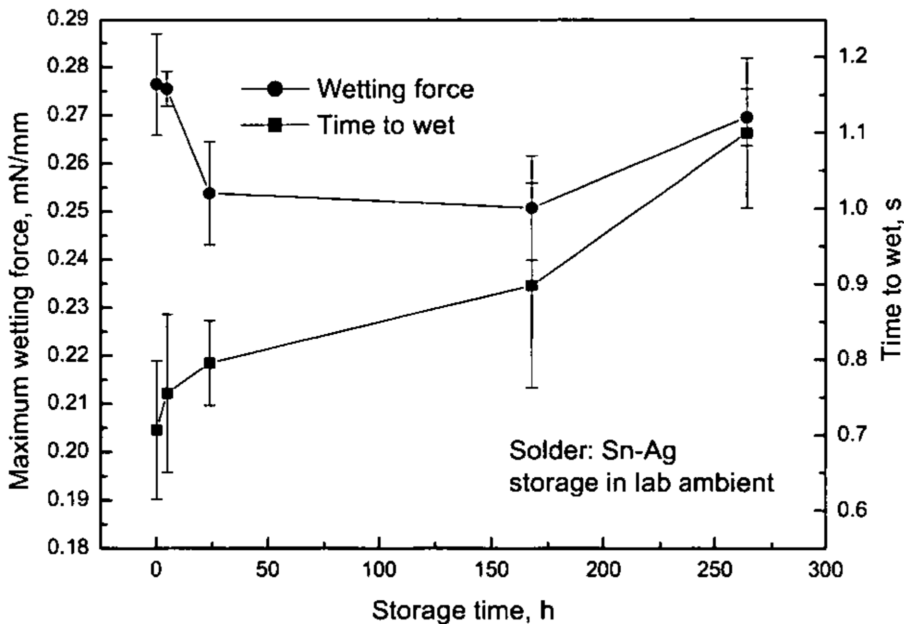


Fig. 6-7 The maximum wetting force and time to wet of EN coatings in Sn-Ag solder during the storage in lab ambient.

Fig. 6-7 shows the wetting force and time to wet of EN coatings in Sn-Ag solder after storage in ambient lab environment for different periods of time. It shows a similar result as that for Sn-Ag-Cu solder. The maximum wetting force was of the same level, but the time to wet increased gradually during storage. Compared with the results without the nitrogen protection, it can be seen that the nitrogen did improve the wettability.

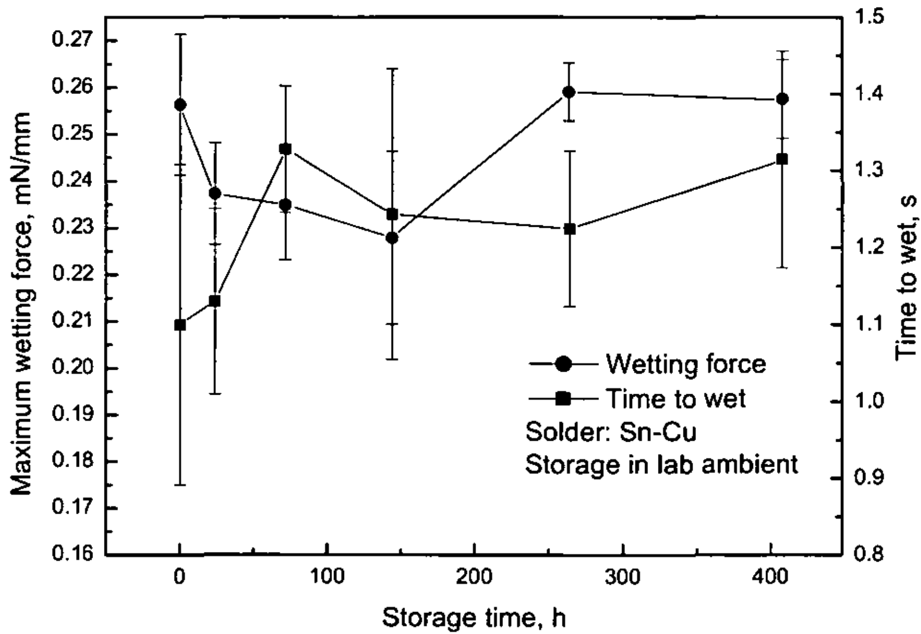


Fig. 6-8 The maximum wetting force and time to wet of EN coatings in Sn-Cu solder during the storage in lab ambient.

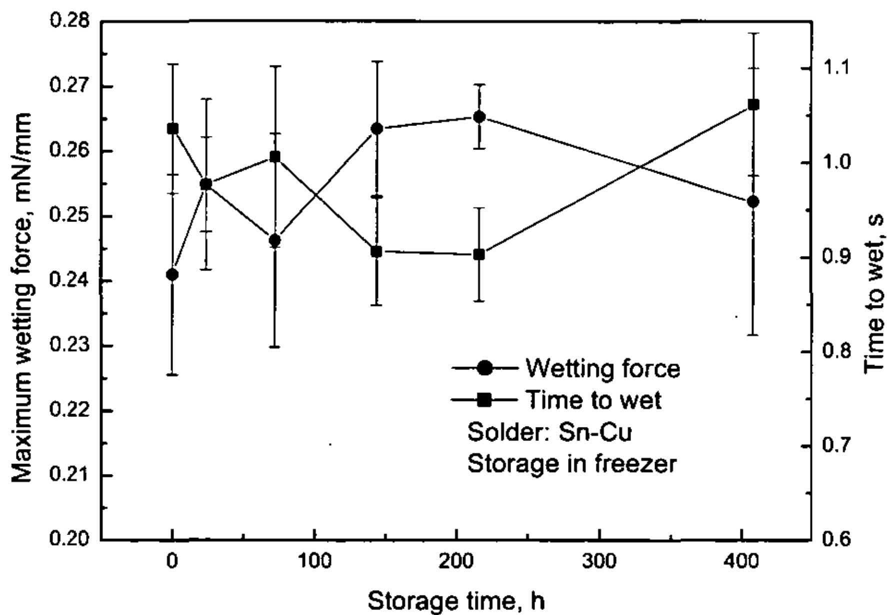


Fig. 6-9 The maximum wetting force and time to wet of EN coatings in Sn-Cu solder during the storage in freezer.

The wettability of an EN coating in Sn-Cu solder after storage in an ambient lab and freezer can be seen from Figs. 6-8 and 6-9, respectively. It can also seen that when the samples were stored in the ambient lab environment the maximum wetting force did not change, but the time to wet increased gradually, and when the samples were stored in a freezer, the storage did not influence the wettability.

6.1.2 Wettability with different substrate roughness

Fig. 6-10 shows the roughness of Al coupons after different polishing regimes before and after the electroless Ni plating in the directions both perpendicular (A) and parallel (B) to the polishing or rolling track directions. It shows that after different polishing regimes the Al coupons, before and after EN plating, had different surface roughnesses and the roughness of the samples after EN plating was higher than that before EN plating.

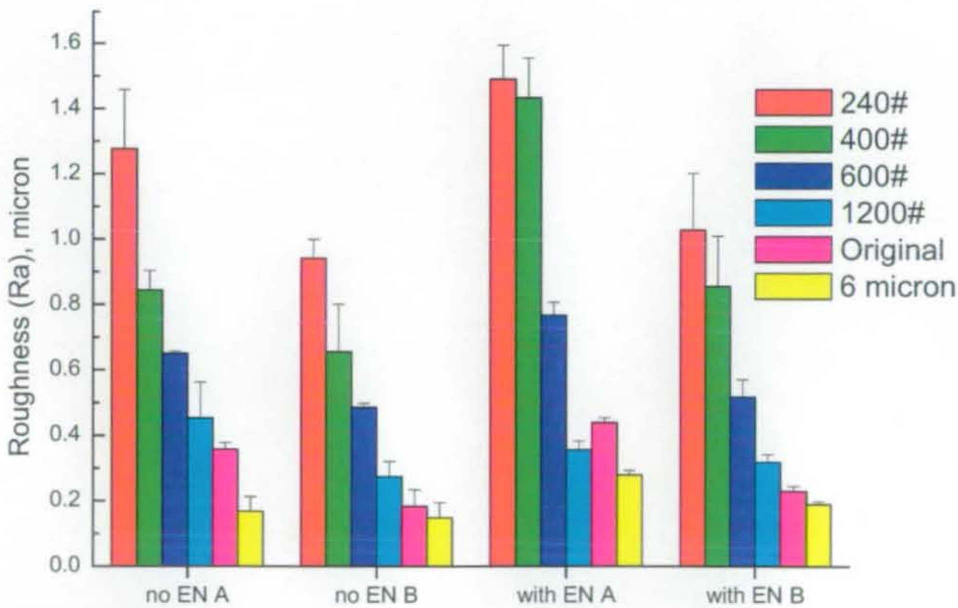


Fig. 6-10 Roughness of Al coupons after different polishing before and after the electroless Ni plating in testing direction, A, perpendicular and B, parallel to the polishing or rolling track direction.

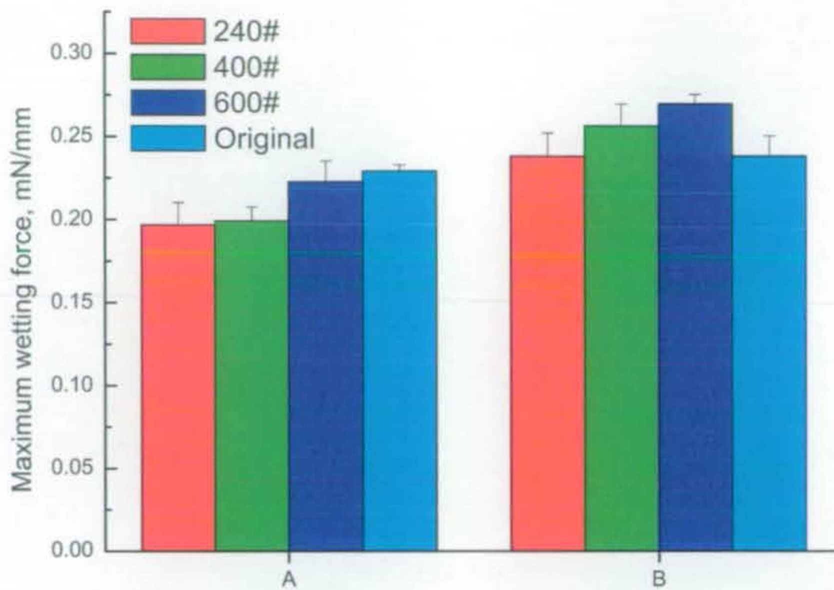


Fig. 6-11 Maximum wetting force of EN coating in Sn-Ag solder with different substrate roughness and dipping direction, A, perpendicular and B, parallel to the polishing or rolling track direction.

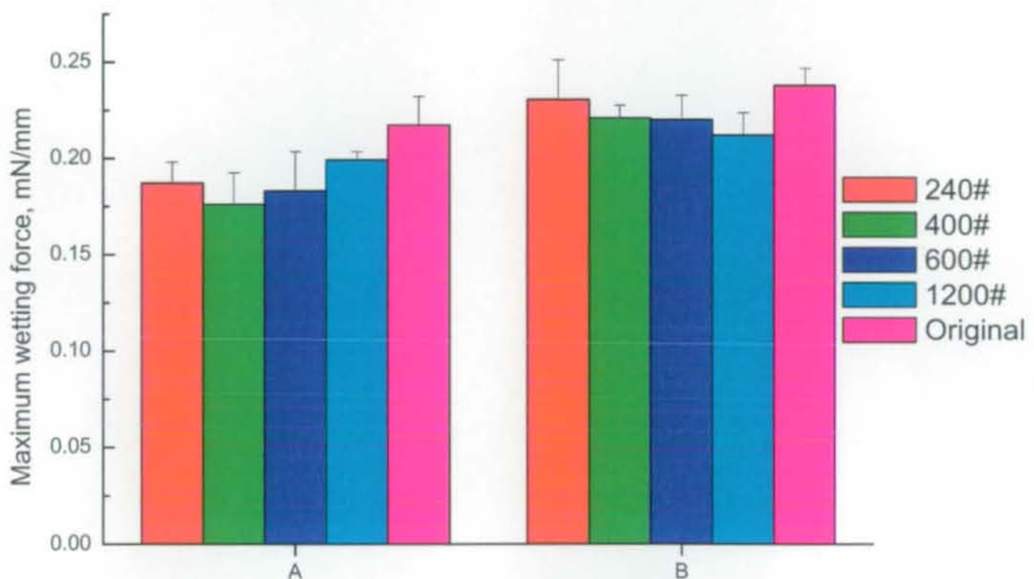


Fig. 6-12 Maximum wetting force of EN coating in Sn-Ag-Cu solder with different substrate roughness and dipping direction, A, perpendicular and B, parallel to the polishing or rolling track direction.

Fig. 6-11 shows the maximum wetting force of an EN coating in Sn-Ag solder with different substrate roughnesses and test directions. It can be seen that the wetting force for the EN coating increased a little with the decreasing of surface roughness except for the EN coating on the original Al surface when the dipping direction was parallel with the polishing or rolling track direction, but this influence was not significant. It can also

be seen that all samples had a higher maximum wetting force when the dipping direction was parallel with the polishing track direction. For the EN coating on the original Al substrate, the maximum wetting force in the A and B directions was similar. Fig. 6-12 shows the maximum wetting force of an EN coating in Sn-Ag-Cu solder with different substrate roughnesses and test directions. It shows the same results as that with Sn-Ag solder.

6.2 Microstructures of lead free solders

6.2.1 Microstructures of bulk solders

In order to examine the microstructures of bulk solders and to provide a comparison with those of small solder bumps/joints, the microstructures of lead free bulk solders were studied. Fig. 6-13 shows the microstructure of Sn-3.5Ag bulk solder. Some clusters of Ag_3Sn small particles were distributed randomly in the β-Sn. Fig. 6-14 shows the microstructure of Sn-3.8Ag-0.7Cu bulk solder. Many Ag_3Sn and Cu_6Sn_5 small particles were distributed evenly in β-Sn, which were larger than those found in Sn-Ag solder. Fig. 6-15 shows the microstructure of Sn-0.7Cu bulk solder. The Cu_6Sn_5 IMC particles were too small to be seen at this magnification. In all three alloys of solder, there were different areas showing different optical contrasts. EDX analyses showed that these phases were all β-Sn and the different contrast might be caused by different crystallographic orientations.

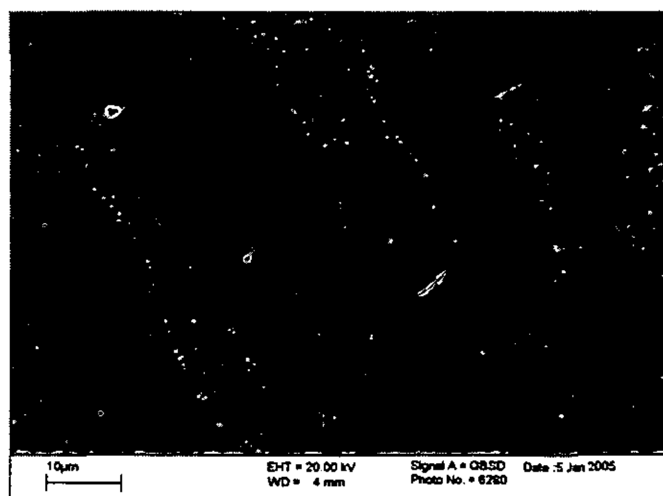


Fig. 6-13 Microstructure of Sn-Ag from solder bar.

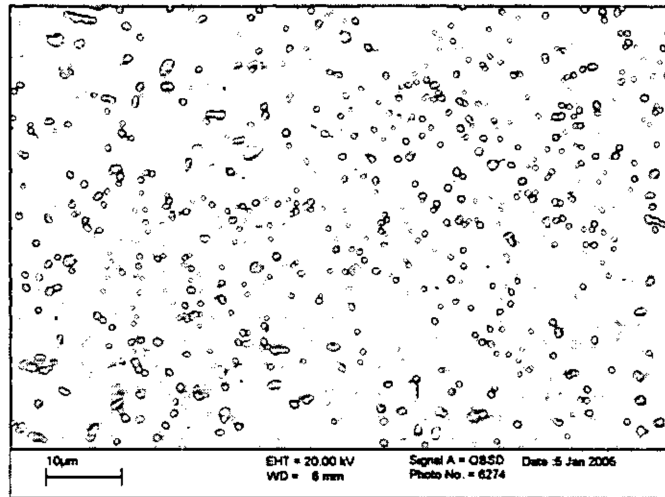


Fig. 6-14 Microstructure of Sn-Ag-Cu from solder bar.

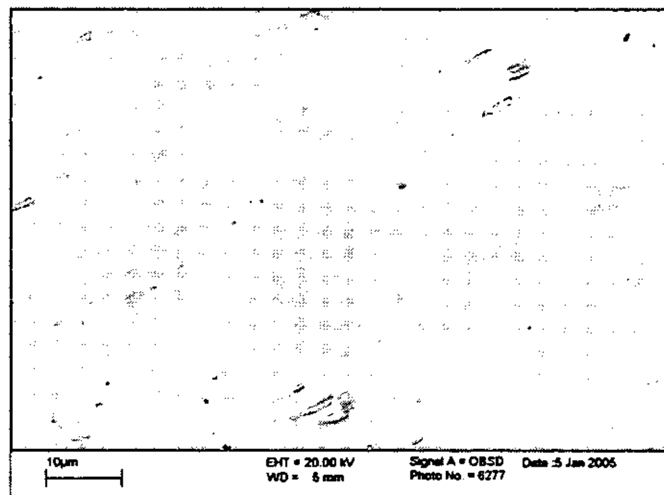


Fig. 6-15 Microstructure of Sn-Cu from solder bar.

6.2.2 Microstructures with different cooling media

Different cooling media can provide different cooling rates. A faster cooling rate can cause more nucleation sites and as a result a finer feature. During the solidification of solder materials, different phases will form inside the solder or at the interfaces, including brittle IMCs. When these IMCs are too large and when the component suffers thermal shock or external forces, stress will accumulate at the solder/IMC interface, resulting in the initiation and propagation of cracks, which may greatly degrade the mechanical properties of solder joints. In order to avoid of the formation of large IMCs, the influence of cooling media on the microstructure and mechanical properties was studied for the ASH wafer bumps and bulk lead free solders.

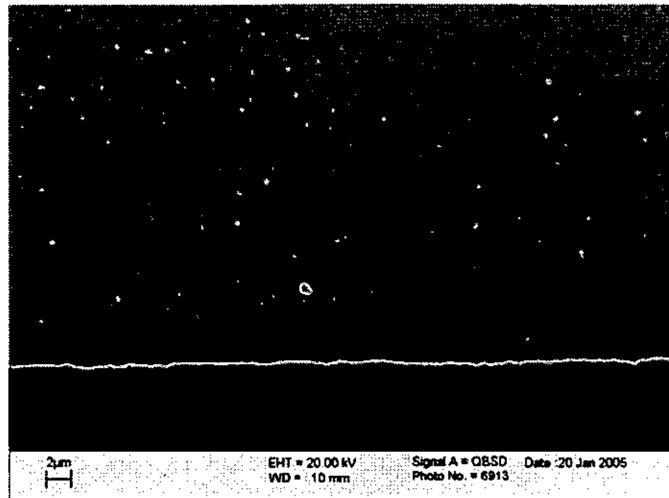


Fig. 6-16 Microstructure of ASH bump cooled in furnace.

6.2.2.1 ASH bumps

Figs. 6-16 to 6-18 show the microstructures of Sn-Ag-Cu solder bumps after cooling in furnace, air and water media, respectively. Because the second reflow temperature (top temperature 280°C) was much higher than the first reflow temperature, the microstructure of these solder bumps was different from that of solder bumps with only an initial reflow. The $(Cu,Ni)_6Sn_5$ IMC layers were thicker and rougher than those with the single initial reflow process and the Ag_3Sn IMCs increased in number and became much smaller.

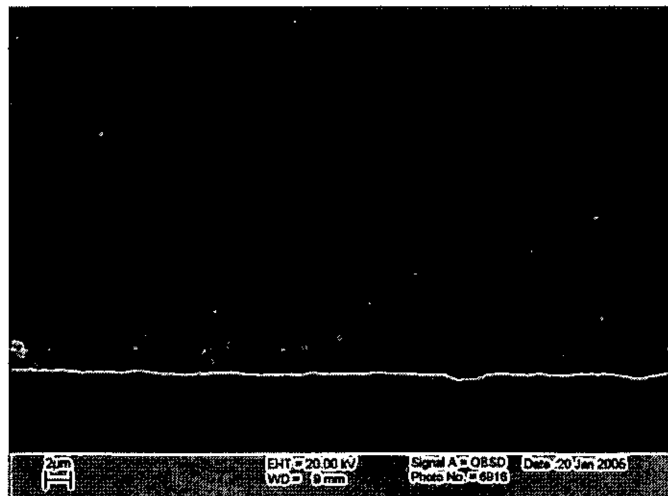


Fig. 6-17 Microstructure of ASH bump cooled in air.

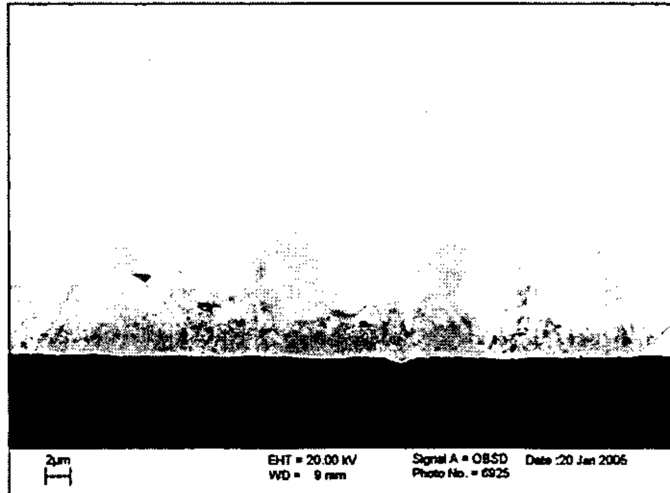


Fig. 6-18 Microstructure of ASH bump cooled in water.

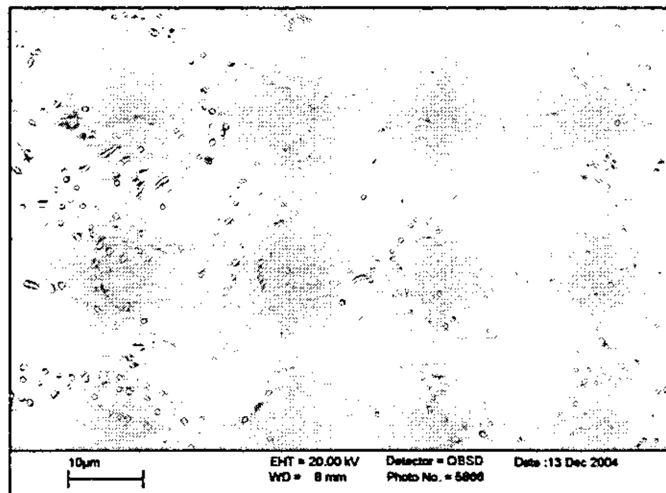


Fig. 6-19 Microstructure of Sn-Ag bulk solder cooled in water.

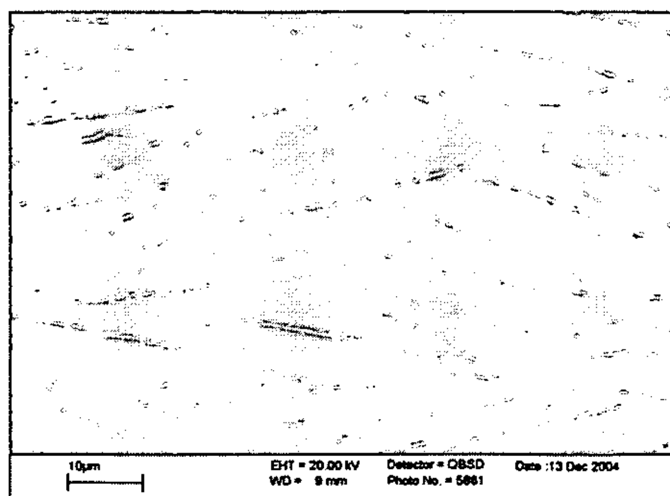


Fig. 6-20 Microstructure of Sn-Ag bulk solder cooled in air.

6.2.2.2 Bulk solders

The bulk lead free solders studied include Sn-3.5Ag, Sn-0.7Cu and Sn-3.8Ag-0.7Cu. Fig. 6-19 shows the microstructure of Sn-Ag bulk solder cooled in the water medium. EDX analyses showed that two kinds of microstructures existed in the solder: one was the β-Sn with distributed small Ag_3Sn particles or plates and the other was β-Sn. Because of non-equilibrium solidification, the phase distribution in the solder was not even. Fig. 6-20 shows the microstructure of Sn-Ag bulk solder cooled in air medium. Small plate-like Ag_3Sn IMCs were evenly distributed in the β-Sn matrix. Fig. 6-21 shows the microstructure of Sn-Ag bulk solder cooled in a furnace. The Ag_3Sn IMCs existed in the solder as plate-like phases. It can be seen that these phases are much larger than the Ag_3Sn formed in the solders after they were cooled in air and water. In fact, some of these phases were as large as 50 μm thick and 1 mm long. However, the distribution density of Ag_3Sn was much lower than that for the solders cooled in air and water.

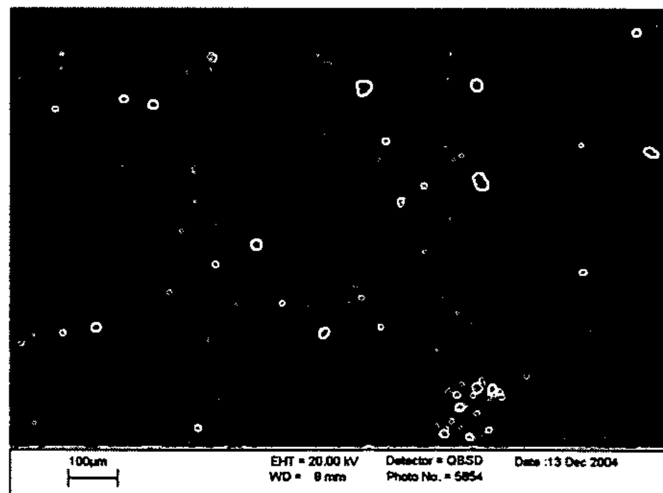


Fig. 6-21 Microstructure of Sn-Ag bulk solder cooled in a furnace.

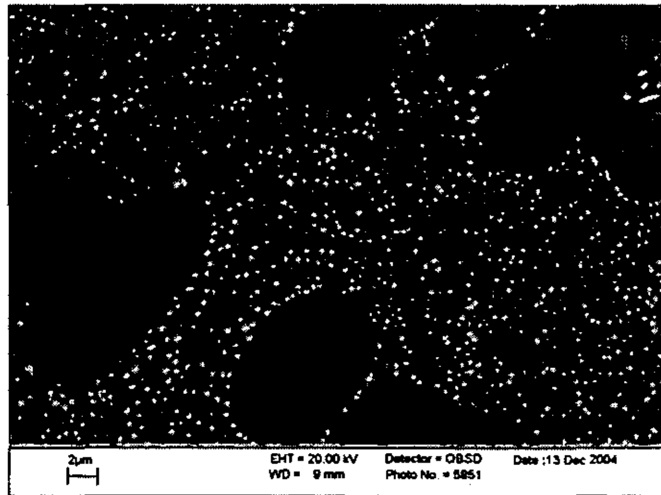


Fig. 6-22 Microstructure of Sn-Ag-Cu bulk solder cooled in water.

Fig. 6-22 shows the microstructure of Sn-Ag-Cu bulk solder cooled in a water medium. Two kinds of microstructures existed in the solder: β-Sn and β-Sn with distributed small Ag_3Sn white particles, similar to but much smaller than those formed in Sn-Ag solder. EDX analysis also showed that there were a small number of Cu_6Sn_5 IMCs distributed around the grain boundaries of β-Sn. However, due to their small size and poor contrast with β-Sn, they cannot be seen clearly in the images. Fig. 6-23 shows the microstructure of Sn-Ag-Cu bulk solder cooled in the air medium. Two kinds of phases were distributed in the β-Sn, Ag_3Sn and Cu_6Sn_5. The grey phases were Ag_3Sn with a plate-like shape. Some of the Ag_3Sn phases were as large as 20 µm thick and 1 mm long. The dark phases were Cu_6Sn_5, and they existed as small plate-like phases or small particles. Fig. 6-24 shows the microstructure of Sn-Ag-Cu bulk solder cooled in a furnace. Two kinds of phases were distributed in the β-Sn, these being a grey Ag_3Sn and darker Cu_6Sn_5. The Ag_3Sn phases had the plate-like shape. Some of the Cu_6Sn_5 phases were plate-like, but others presented as a hollow hexagonal shape. The plate-like Cu_6Sn_5 phases were not as straight as the Ag_3Sn phase.

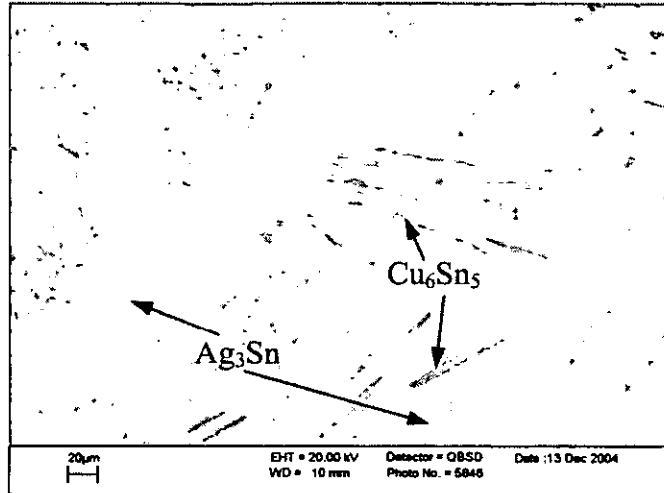


Fig. 6-23 Microstructure of Sn-Ag-Cu bulk solder cooled in air.

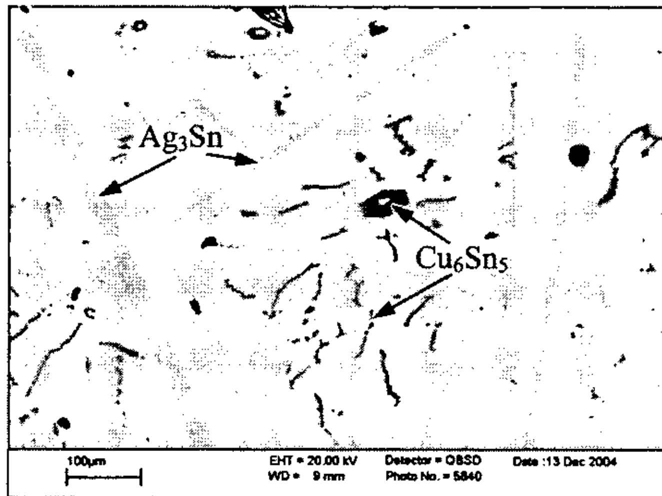


Fig. 6-24 Microstructure of Sn-Ag-Cu bulk solder cooled in furnace.

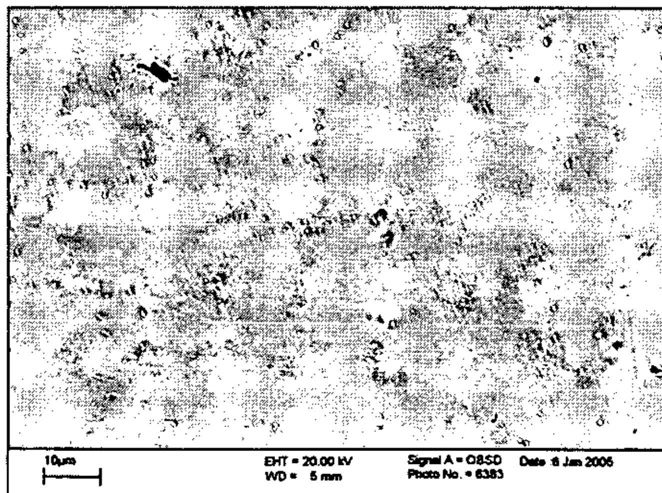


Fig. 6-25 Microstructure of Sn-Cu bulk solder cooled in water.

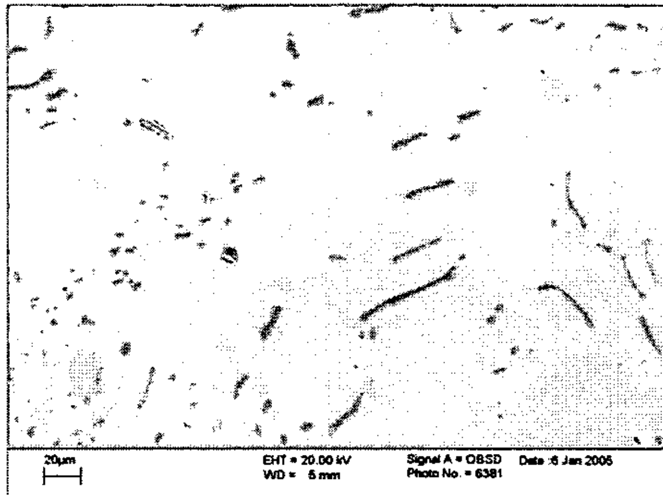


Fig. 6-26 Microstructure of Sn-Cu bulk solder cooled in air.

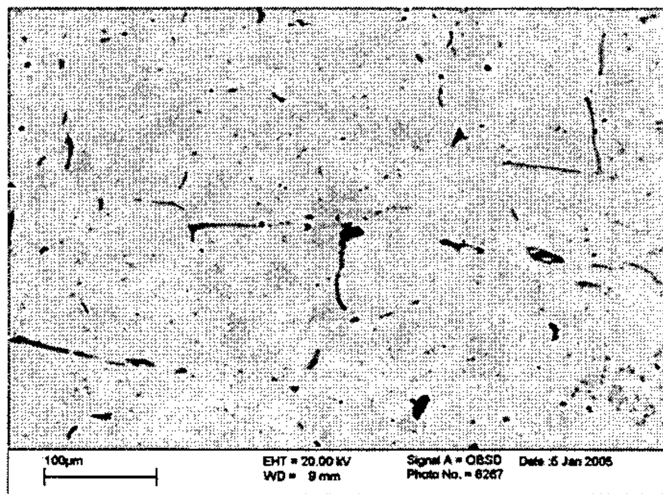


Fig. 6-27 Microstructure of Sn-Cu bulk solder cooled in furnace.

Fig. 6-25 shows the microstructure of Sn-Cu bulk solder cooled in the water medium. Small Cu_6Sn_5 particles were distributed around β-Sn grain boundaries. Figs. 6-26 and 6-27 shows the microstructure of Sn-Cu bulk solder cooled in the air medium and furnace respectively. In these solders, plate-like and pebble-like Cu_6Sn_5 IMCs were distributed in the β-Sn matrix.

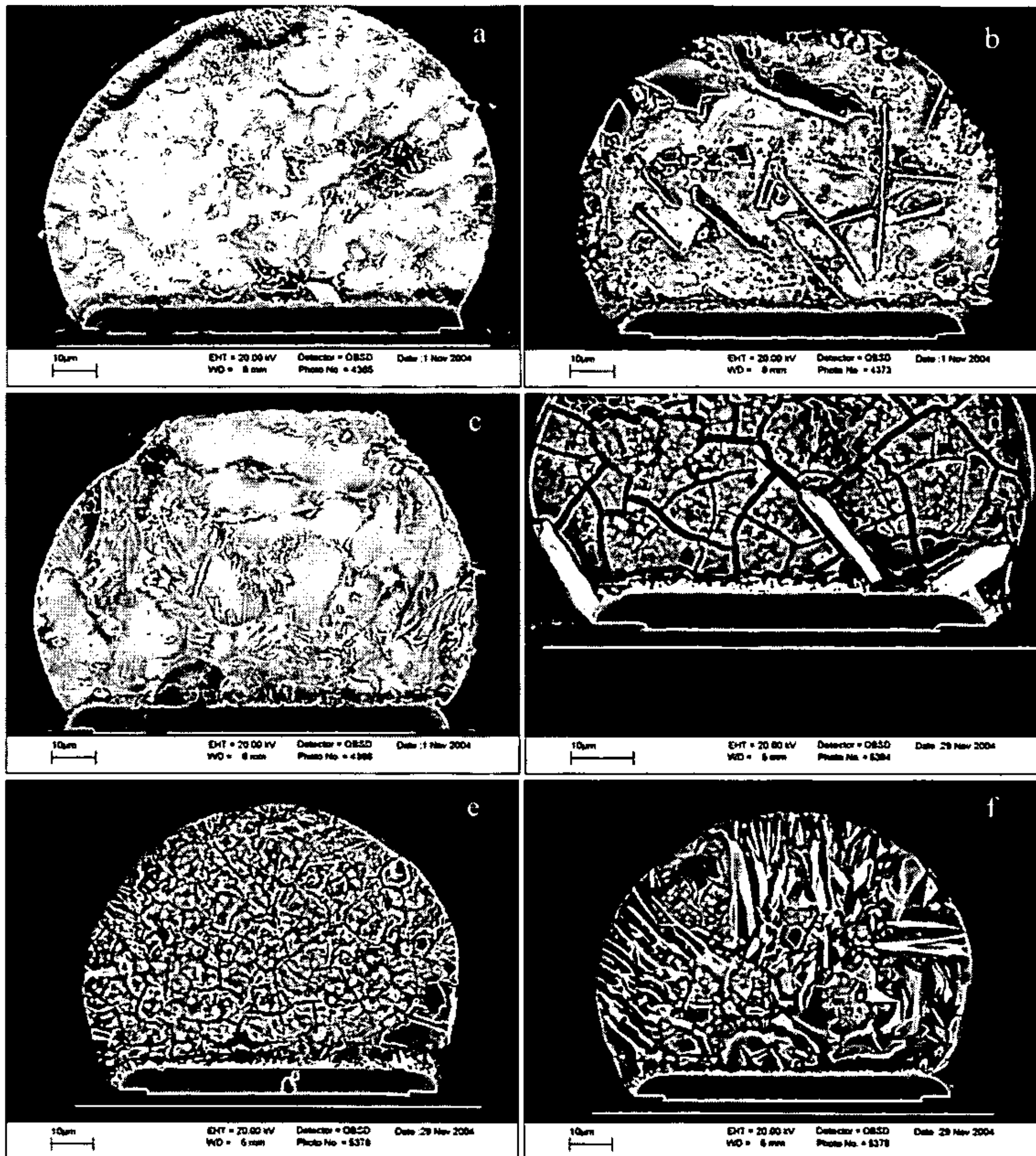


Fig. 6-28 Microstructures of Sn-Ag-Cu solder bumps after vertical cross-section and etching.

6.2.3 Morphologies and distributions of IMCs Sn-Ag-Cu solder joints

Due to the brittle nature of IMCs, the existence of large IMCs can be detrimental to the mechanical properties of solder joints, especially when these large phases form at the interfaces or at the corner of the solder joints. As such, understanding of the morphologies and distributions of these IMCs derived from both modelling and experimental activities is important with regard to the reliability of solder joints.

Fig. 6-29 Morphologies of $(Cu,Ni)_6Sn_5$ and Ag_3Sn IMCs in Sn-Ag-Cu solder bumps.

From the vertical cross-section of the ASH bumps (Fig. 6-28), it can be seen that for the Ag_3Sn IMC, there are four kinds of morphologies and distributions, shown in Fig. 6-28a-d respectively. In Fig. 6-28a, the Ag_3Sn IMC existed as small particles or small plate-like phases around the β-Sn dendrites; in Fig. 6-28b, the Ag_3Sn IMC existed as middle size plate-like phases throughout the solder bump; in Fig. 6-28c, the morphology of the Ag_3Sn was the mixture of the first two types, small particles and plate-like phases around the β-Sn dendrites and middle size plate-like phases in the solder; in Fig. 6-28d, the Ag_3Sn IMC existed as a large plate-like phase. The solder bumps in Figs. 6-28a-c were etched for 20 s with 1 part of acetic acid, 1 part of nitric acid and 4 parts of glycerol without ultrasonic assistance during etching and some of the corrosion residues can be seen beside the IMCs. The solder bumps in Figs. 6-28d, e and f were etched 20 s with ultrasonic assistance and the boundaries of the IMCs are very clear, but many cracks were created in the remaining solder. When the plate-like phases were large enough there would be only a small number of Ag_3Sn particles existing in the rest of the solder bumps, which could be seen through Figs. 6-28b, d and f. From Fig. 6-28d and f, it can be seen that the middle and large size Ag_3Sn IMCs are plate-like, and not stick-like or needle-like. Fig. 6-29 shows the morphologies of $(Cu,Ni)_6Sn_5$ IMC at the solder/EN UBM interface. Fig.6-29b is the zoomed image of Fig.6-29a at interface. It can be seen that this IMC is facet-like or needle-like and the IMC layer is not compact and there could be more $(Cu,Ni)_6Sn_5$ IMC at the corner of the solder bumps than in the middle.

In order to derive more understanding of the morphologies and distributions of IMCs in the ASH solder bumps, the bumps were cross-sectioned and studied in the horizontal direction.

Figs. 6-30a-d show optical images of ASH solder bumps after the horizontal cross-section. They confirmed that the morphologies and distributions were the same as that in the vertical direction.

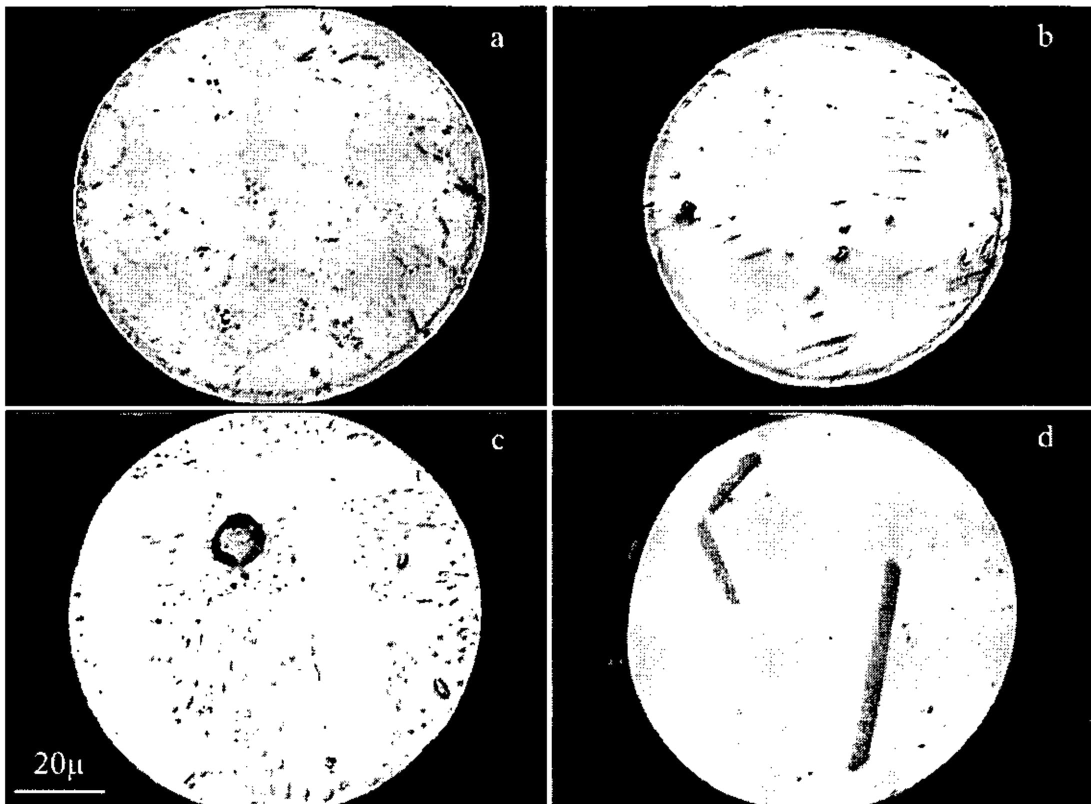
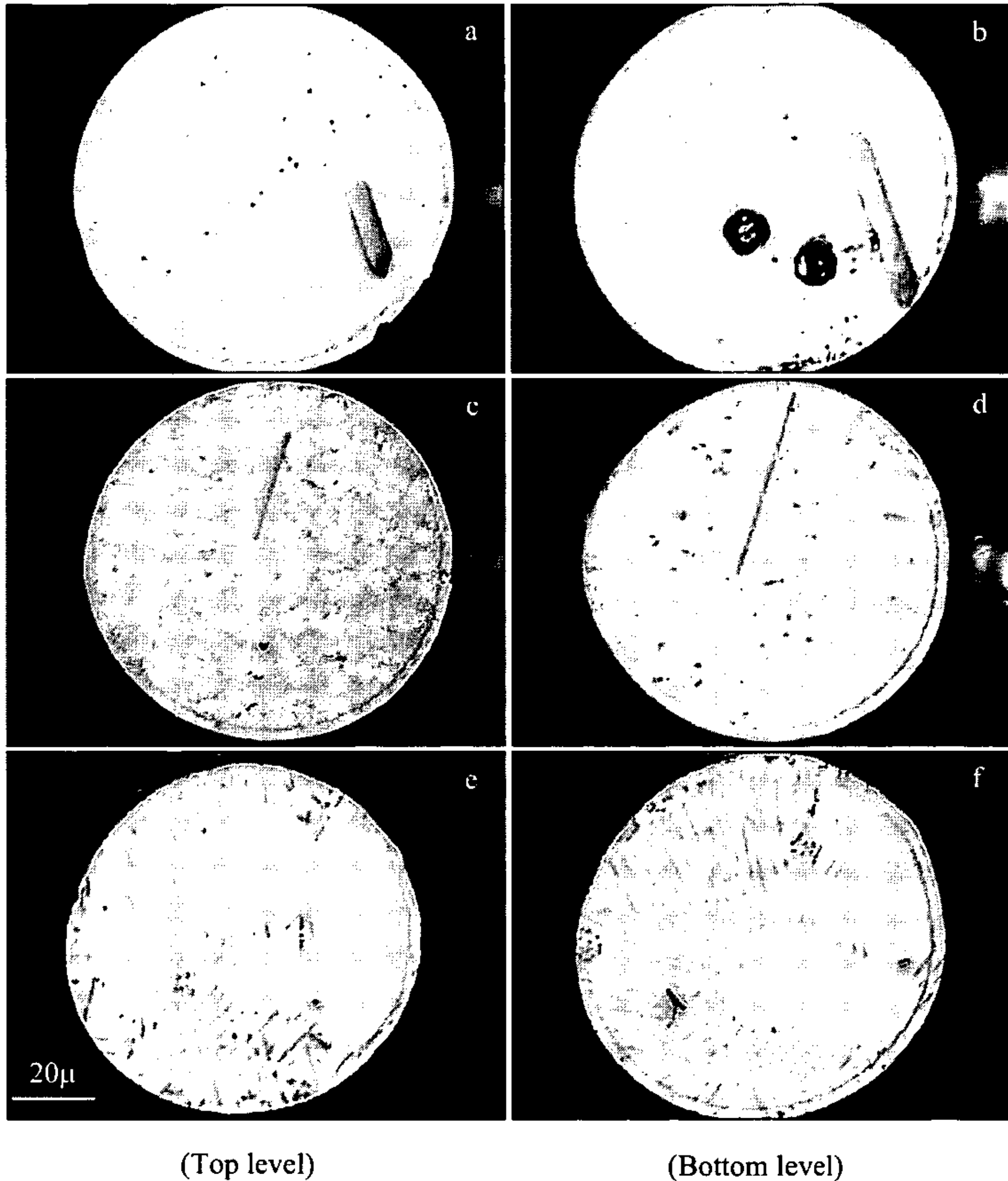


Fig. 6-30 Microstructures of Sn-Ag-Cu solder bumps after horizontal cross-section.

The solder bumps were cross-sectioned at two different levels, with the distance between them of about 10-15 μm, to get some stereoscopic idea of the morphologies and distributions of the Ag_3Sn IMCs. Fig. 6-31 shows the images of the same solder bumps viewed from the different level. Figs. 6-31a, c and e are from the top layer, and b, d and f, the respective lower layer. Comparing these two layers, it can be seen that the morphologies and distributions of the Ag_3Sn IMC are the same in different layers. When there is a large plate-like Ag_3Sn phase in one layer, there is normally a large plate-like Ag_3Sn phase in the next layer. This means that the Ag_3Sn phases were not

branch-like but plate-like. Additionally, these cross-sections indicate that the large Ag_3Sn plate is trapezoidal or polygonal in shape. However, for the small particles and middle size plate-like Ag_3Sn phases, they could be discontinuous.



(Top level) (Bottom level)

Fig. 6-31 Microstructure of the same Sn-Ag-Cu solder bumps after horizontal cross-section at different level.

6.3 IMC growth during reflow processes and thermal ageing

6.3.1 Thermal ageing at 80°C

During reflow soldering and subsequent ageing, solder reacts with the UBM and forms the IMCs at the Sn-3.8Ag-0.7Cu solder/UBM interface and in the solder. Fig. 6-32 shows the microstructure of solder/EN UBM interface in the solder bump as-reflowed. Some small Ag_3Sn particles formed in the solder and $(Cu,Ni)_6Sn_5$ IMC formed at the solder/EN interface. Fig. 6-33 shows the microstructure of the solder/EN interface after ageing at 80°C for 50 h. Many small Ag_3Sn particles formed in the solder bump. However, from the images of other bumps, it can be seen that the Ag_3Sn IMC could exist as distributed particles and large plate-like phase features in both the as-reflowed and aged states, and their morphologies could vary between different bumps.

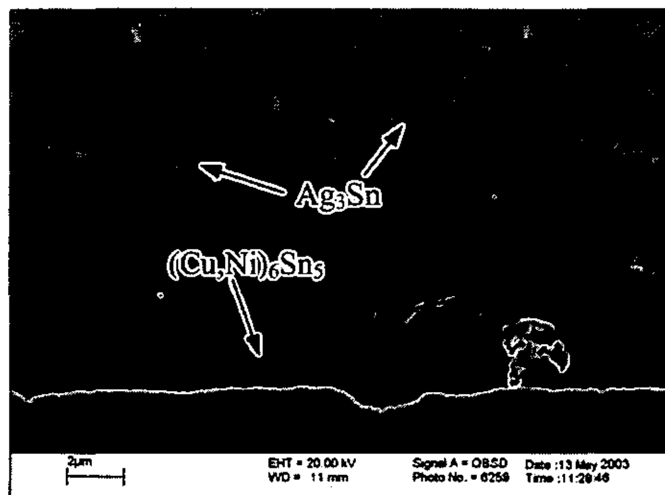


Fig. 6-32 Microstructure of solder bump interface as-reflowed.

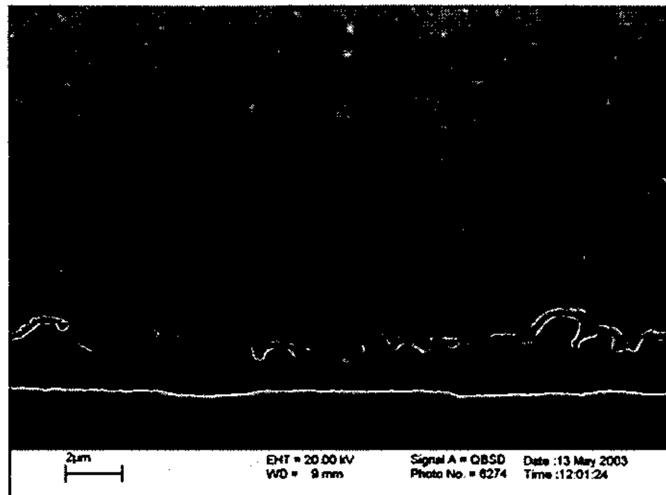


Fig. 6-33 Microstructure of solder bump interfaces after ageing 50h at 80°C.

Fig. 6-34 presents the microstructure of the IMCs along the solder/EN interface after ageing 440 h at 80°C. Some of the facet-like IMCs, identified as $(Cu,Ni)_6Sn_5$, were observed to separate from the main IMC layer into the bulk solder, but no de-wetting occurred at the interface between the $(Cu,Ni)_6Sn_5$ IMC and EN UBM at this stage of ageing.

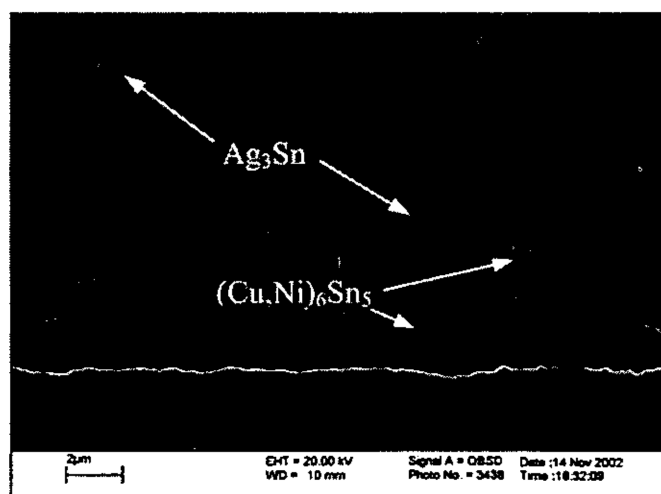


Fig. 6-34 Microstructure of solder bump interfaces after ageing 440h at 80°C.

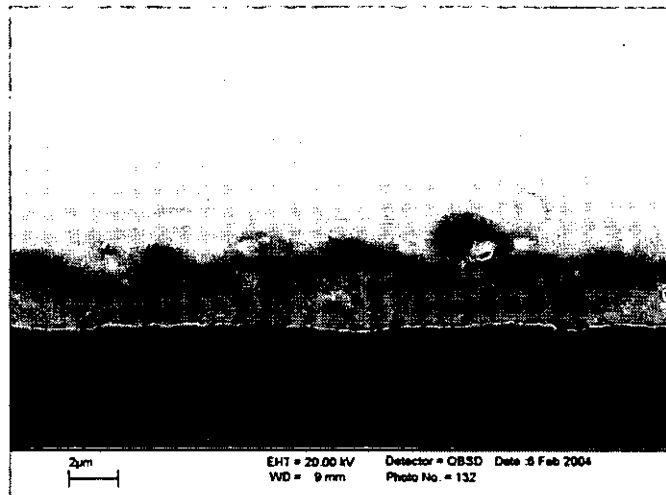


Fig. 6-35 Microstructure of solder bump interface after ageing 750 h at 80°C.

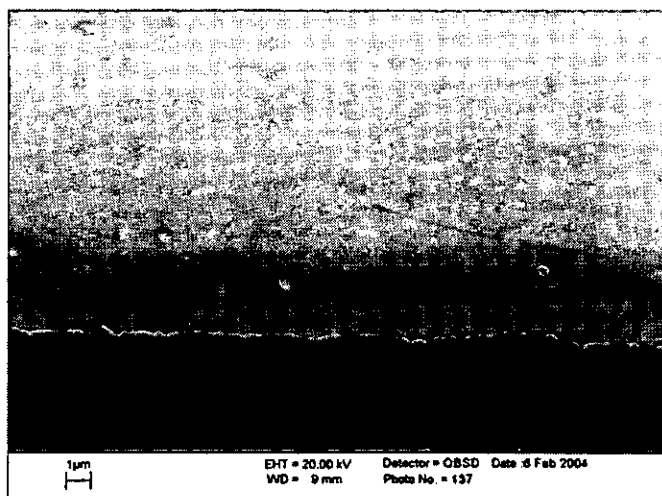


Fig. 6-36 Microstructure of solder bump interface after ageing 1080 h at 80°C.

Fig. 6-35 and Fig. 6-36 show the IMCs formed at the interface of solder bumps after ageing 750 h and 1080 h (45 d) respectively. It can be seen that even after ageing at 80°C for 1080 h, the microstructure of the solder bumps did not change significantly. The results show that when the chips were aged at 80°C, the IMCs formed in the solder bumps were the same as those in the as-reflowed samples. Although the IMCs were growing during ageing, compared with the solder bumps as-reflowed, the thickness of the $(Cu,Ni)_6Sn_5$ IMC at the interface did not increase significantly during ageing at 80°C.

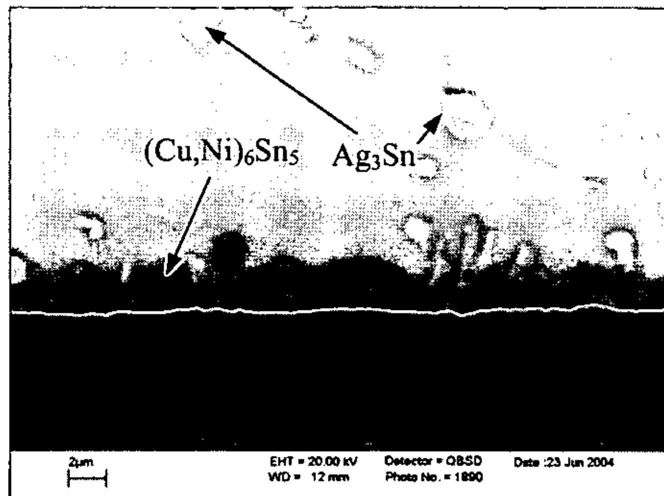


Fig. 6-37 Microstructure of solder bump interface after ageing 2 d at 150°C.

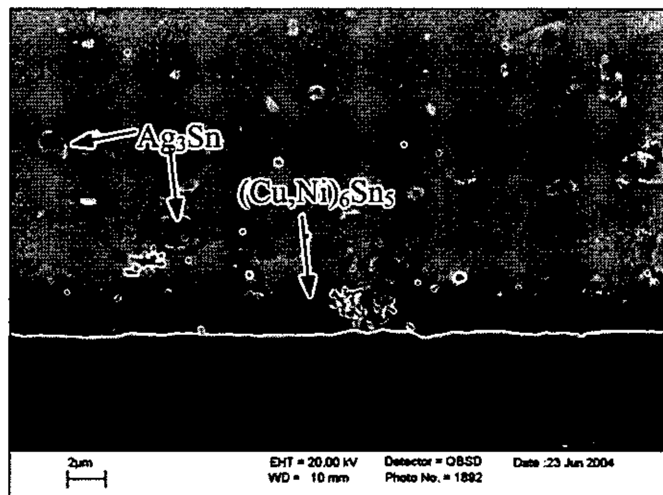


Fig. 6-38 Microstructure of solder bump interface after ageing 10 d at 150°C.

6.3.2 Thermal ageing at 150°C

Figs. 6-37 to 6-39 show the microstructures of solder bumps after ageing at 150°C for 2, 10, and 18 d, respectively, with $(Cu,Ni)_6Sn_5$ at the interface and Ag_3Sn in the bulk solder. Compared with the solder bumps aged at 80°C, however, the thickness of the main IMC layer at the interface was more uniform and the growth of the IMCs became more obvious. It could also be seen that the Ag_3Sn IMC particles in the solder bumps

were much larger than those in the solder bumps as-reflowed and aged at 80°C, but these particles did not grow further after the initial stage ageing at 150°C.

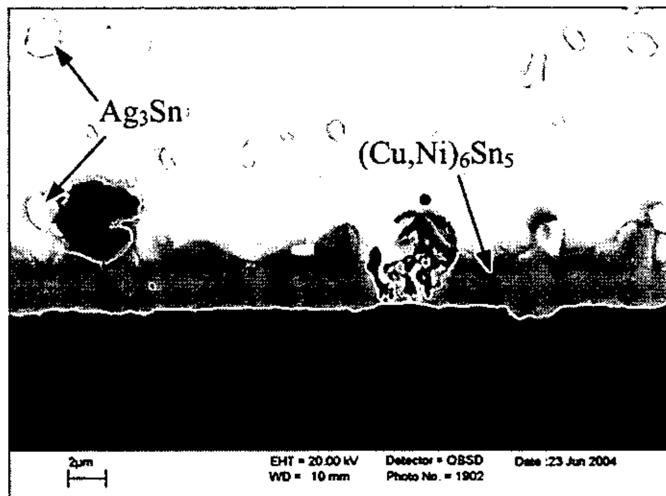


Fig. 6-39 Microstructure of solder bump interface after ageing 18 d at 150°C.

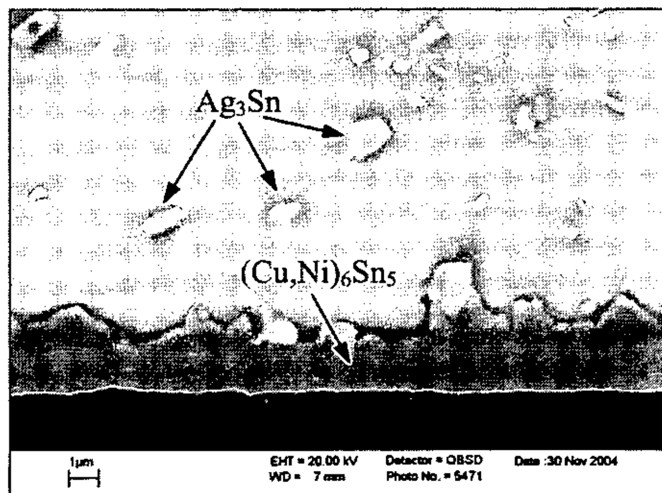


Fig. 6-40 Microstructure of solder bump interface after ageing 3 d at 175°C.

6.3.3 Thermal ageing at 175°C

Figs. 6-40 to 6-42 show the microstructures of solder bumps after being aged at 175°C for 3, 15, and 30 d, respectively. Compared with the solder bumps as-reflowed, the main IMC at the interface grew significantly, becoming much thicker. The growth of Ag_3Sn IMC particles was obvious in the initial stage of ageing and almost kept the same size

during further ageing. Another important feature in the solder bumps aged at 175°C is the formation of Kirkendall voids at the top of the EN layer. EDX analysis showed that the top layer of EN UBM was crystallized into Ni_3P, and a large number of Kirkendall voids formed at the bottom of this layer. It can be seen that these voids were growing during ageing at 175°C and after 15 d a lot of quite large Kirkendall voids formed.

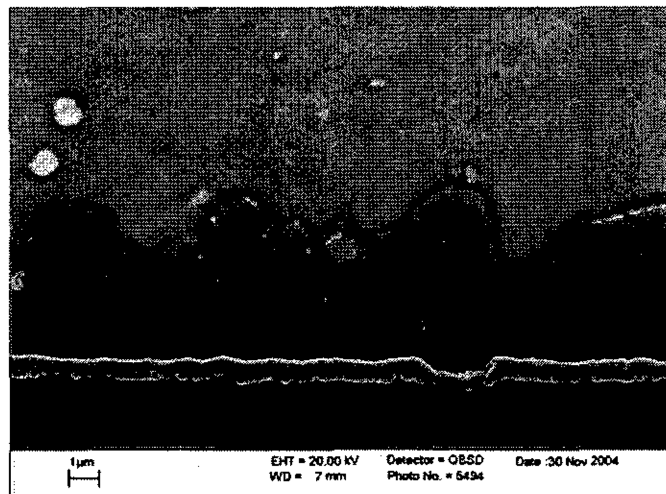


Fig. 6-41 Microstructure of solder bump interface after ageing 15 d at 175°C.

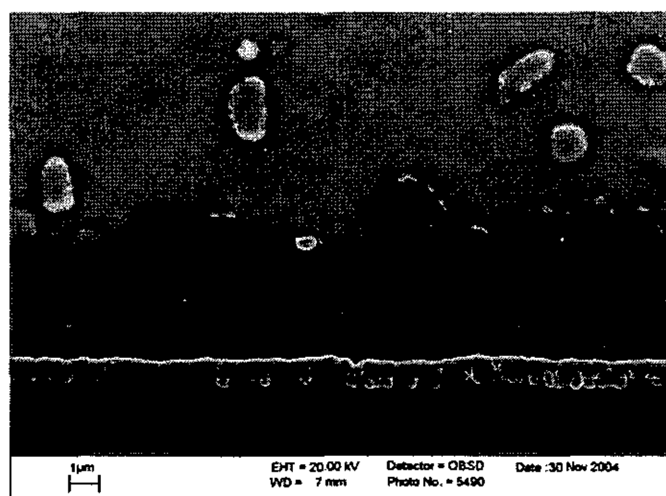


Fig. 6-42 Microstructure of solder bump interface after ageing 30 d at 175°C.

6.4 IMCs formed with different solders and substrates

In order to study the interface reactions between lead free solders and different substrates, different lead free solders were soldered on different substrates through long-time reflow and ageing, and the microstructures of solder joints, IMC growth and IMC morphologies were studied.

6.4.1 Compositions and microstructures of IMCs

Fig. 6-43 shows the microstructures of solder joints formed at the interface of Sn-3.8Ag-0.7Cu solder and different substrates. Fig. 6-43a shows the microstructure of the solder joint formed on Cu. It can be seen that there were two continual IMCs formed at the interface, Cu_6Sn_5 and Cu_3Sn, which were identified by EDX analyses. The thickness of Cu_6Sn_5 IMCs was not uniform with the average thickness about 6 μm. The Cu_3Sn layer exactly followed the morphology of the Cu substrate and the thickness was uniform and about 1.5 μm. The white phases were large plate-like Ag_3Sn IMCs formed near the Cu_6Sn_5 IMC. Fig. 6-43b shows the microstructures of a solder joint formed on the electroless Ni substrate, which indicates the IMC formed at the interface was $(Cu,Ni)_6Sn_5$. This IMC layer was not continual and the thickness was about 7 μm. Fig. 6-43c shows the microstructure of a solder joint formed on the CuImAg substrate. The IMCs formed in the solder joints were similar to those formed on Cu. However, there were many Kirkendall voids formed in the Cu_3Sn layer. Fig. 6-43d shows the microstructures of a solder joint formed on ENIG substrate. The IMCs formed at the interface were $(Cu,Ni)_6Sn_5$, but the IMC layer was much thinner than those formed on Cu and CuImAg, being only 2 μm thick. The top layer of the EN coating crystallized into Ni_3P with some Kirkendall voids. When Sn-3.8Ag-0.7Cu solder reacted with different substrates, small particles and large plate-like Ag_3Sn IMC could also form in the solder joints. Table 6-1 and Table 6-2 show the compositions of phases formed in the solder joint of Sn-Ag-Cu on Cu and EN substrates, respectively. It can be seen that most phases are consistent with their stoichiometry, but sometimes the compositions of the phases were different from the stoichiometry due to the influence of surrounding elements.

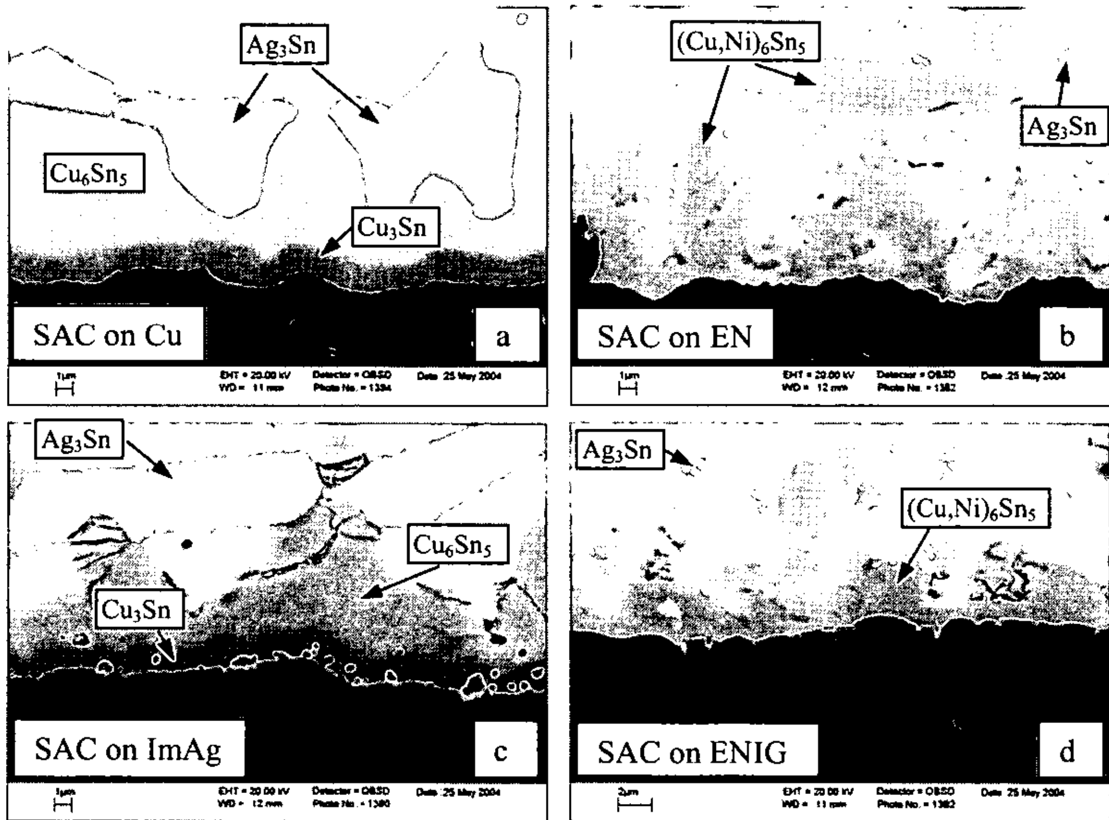


Fig. 6-43 Microstructure of IMCs formed at the interface of Sn-Ag-Cu solder and different substrates.

Fig. 6-44 shows the microstructures of solder joints formed at the interface of Sn-0.7Cu and different substrates. Fig. 6-44a shows the microstructure of solder joint formed on Cu. The phases formed in the solder joints were similar to those formed in Sn-3.8Ag-0.7Cu solder on Cu system, with Cu_6Sn_5 and Cu_3Sn at the interface and Ag_3Sn in the solder. The Cu_6Sn_5 IMC had a facet-like shape. Fig. 6-44b shows the microstructure of a solder joint formed on the EN substrate. The IMC formed at the interface was facet-like $(Cu,Ni)_6Sn_5$, and the thickness was about 2 μm. There was some $(Cu,Ni)_6Sn_5$ IMC formed in the bulk solder as well. Fig. 6-44c shows the microstructure of a solder joint formed on the CuImAg substrate. The IMCs formed at the interface were Cu_6Sn_5 and Cu_3Sn, and these two IMC layers were quite uniform with the thickness about 4 μm and 1.5 μm, respectively. There were many Kirkendall voids in the Cu_3Sn layer. Also, there were some Cu_6Sn_5 and Ag_3Sn IMCs formed in the bulk solder. Fig. 6-44d shows the microstructure of a solder joint formed on an ENIG substrate. The IMC formed at the interface was $(Cu,Ni)_6Sn_5$, which had a facet-like shape. The top layer of the EN coating

crystallized into Ni_3P with some Kirkendall voids. There were some $(Cu,Ni)_6Sn_5$ IMC formed in the bulk solder and a few $AuSn_4$ small particles formed in the solder near the IMC layer with a white colour.

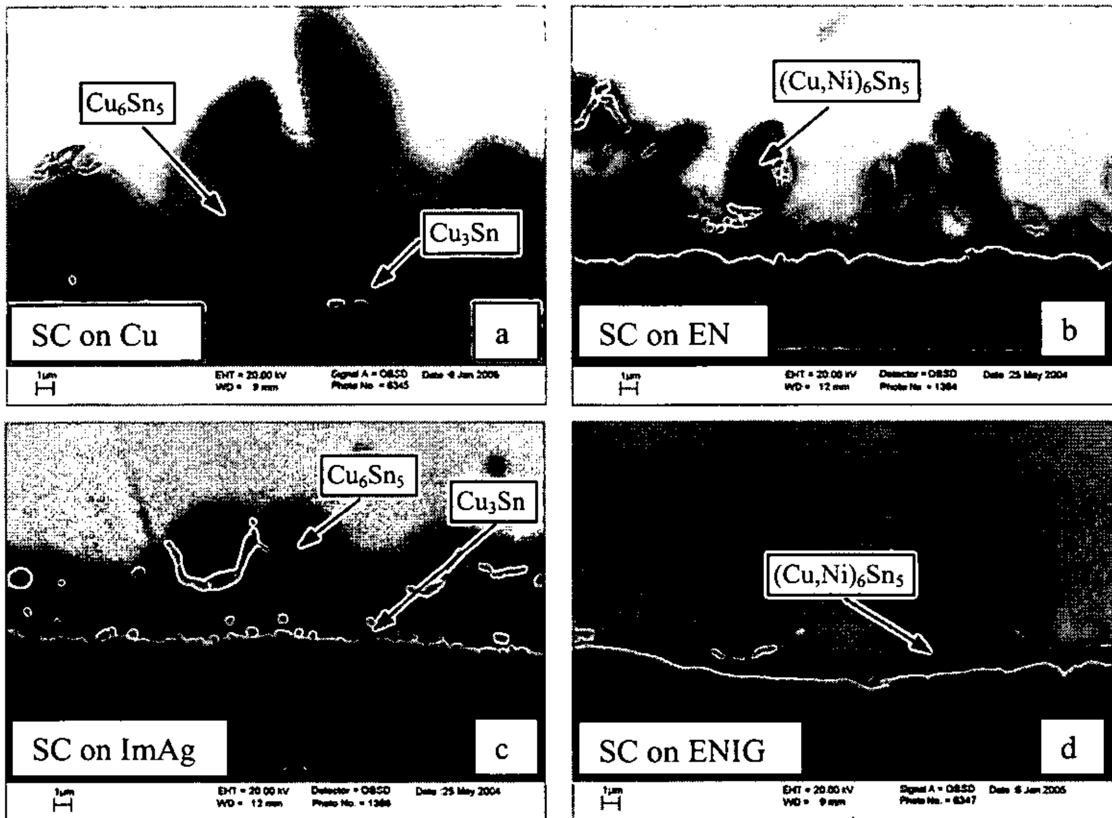


Fig. 6-44 Microstructure of IMCs formed at the interface of Sn-Cu solder and different substrates.

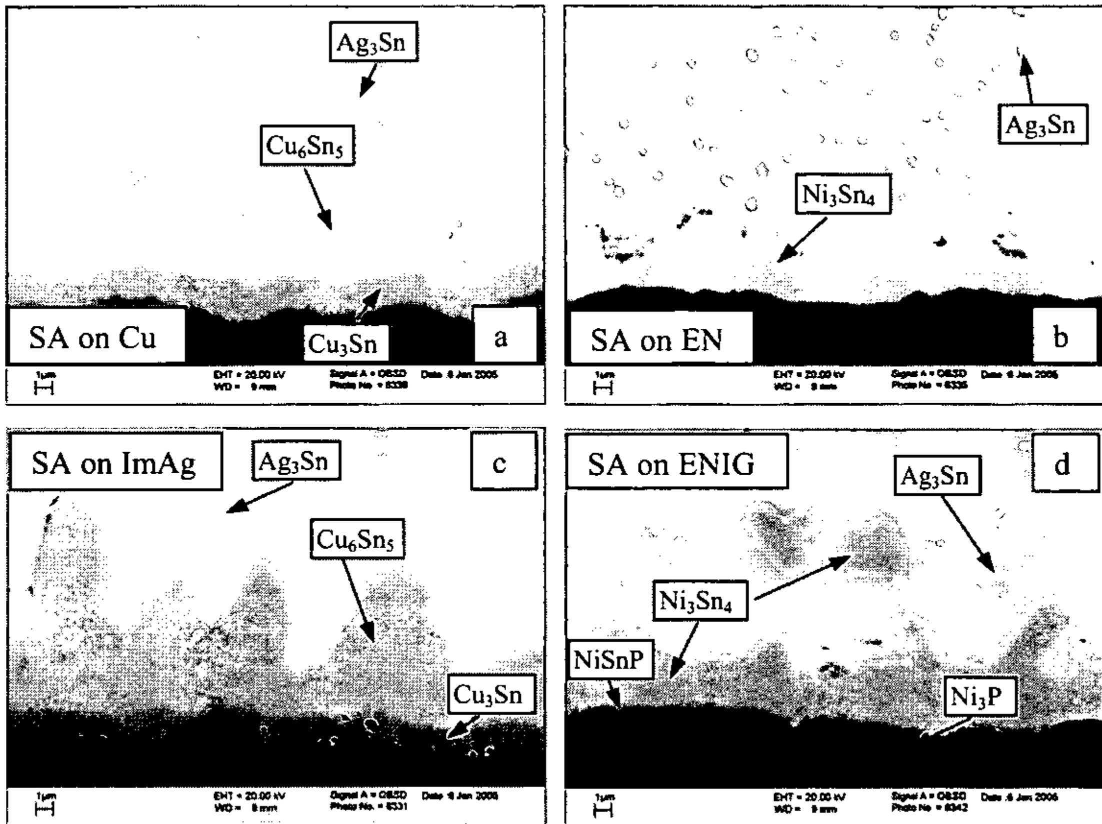


Fig. 6-45 Microstructure of IMCs formed at the interface of Sn-Ag solder and different substrates.

Table 6-1 Compositions of phases formed in the solder joint of Sn-Ag-Cu on Cu.

Phases	Cu, at.%	Ag, at.%	Sn, at.%
Cu_6Sn_5	55.6	-	44.38
Cu_3Sn	76.0	-	24.0
Ag_3Sn	-	73.6	26.4

Table 6-2 Compositions of phases formed in the solder joint of Sn-Ag-Cu on EN.

Phases	Cu, at.%	Ag, at.%	Sn, at.%	Ni, at.%
$(Cu,Ni)_6Sn_5$	38.1	-	43.8	18.1
Ag_3Sn	-	57.18	42.82	-

Table 6-3 Compositions of phases formed in the solder joint of Sn-Ag on ENIG.

Phases	Ni, at.%	P, at.%	Ag, at.%	Sn, at.%	Au, at.%
Ni_3Sn_4	43.7	-	-	56.3	-
NiPSn	65.9	16.8		17.3	-
$AuSn_4$	-	-	6.0	75.2	18.8
Ni_3P	75.0	25.0	-	-	-
Ag_3Sn	-	-	57.5	42.5	-

Table 6-4 Summary of phases formed in the solder joints of different solders on different substrates.

Systems	IMCs at interface		IMCs in solder	Kirkendall Voids	Ni_3P layer
	Phase	Thickness			
SA on EN	Ni_3Sn_4	4 μ	Ni_3Sn_4, Ag_3Sn	Many	Thick
SA on CuImAg	Cu_6Sn_5	6 μ	Cu_6Sn_5, Ag_3Sn	A few	-
	Cu_3Sn	2 μ			
SA on Cu	Cu_6Sn_5	8 μ	Cu_6Sn_5, Ag_3Sn	No	-
	Cu_3Sn	2.5 μ			
SA on ENIG	Ni_3Sn_4	4 μ	$AuSn_4$, Ni_3Sn_4, Ag_3Sn	Line voids	Very thick
SAC on EN	$(Cu,Ni)_6Sn_5$	7 μ	$(Cu,Ni)_6Sn_5$, Ag_3Sn	No	No
SAC on CuImAg	Cu_6Sn_5	4 μ	Cu_6Sn_5, Ag_3Sn	Many	-
	Cu_3Sn	1.5 μ			
SAC on Cu	Cu_6Sn_5	6 μ	Cu_6Sn_5, Ag_3Sn	No	-
	Cu_3Sn	1.5 μ			
SAC on ENIG	$(Cu,Ni)_6Sn_5$	2 μ	$(Cu,Ni)_6Sn_5$, Ag_3Sn	A few	Very thin
SC on EN	$(Cu,Ni)_6Sn_5$	2μ	$(Cu,Ni)_6Sn_5$, CuNiSn	Many	Very thin
SC on CuImAg	Cu_6Sn_5	4 μ	Cu_6Sn_5, Ag_3Sn	Many	-
	Cu_3Sn	1.5 μ			
SC on Cu	Cu_6Sn_5	7μ	Cu_6Sn_5	No	-
	Cu_3Sn	2 μ			
SC on ENIG	$(Cu,Ni)_6Sn_5$	2 μ	$AuSn_4$, $(Cu,Ni)_6Sn_5$	A few	Very thin

Fig. 6-45 shows the microstructures of solder joints formed at the interface of Sn-3.5Ag and different substrates. Fig. 6-45a shows the microstructure of a solder joint formed on Cu. The IMCs formed at the interface were Cu_6Sn_5 and Cu_3Sn. Fig. 6-45b shows the microstructure of solder joints formed on the EN substrate. The IMCs formed at the interface were Ni_3Sn_4. Fig. 6-45c shows the microstructure of solder joints formed on the CuImAg substrate. The IMCs formed at the interface were Cu_6Sn_5 and Cu_3Sn. There were some Kirkendall voids in the Cu_3Sn layer. Fig. 6-45d shows the microstructure of solder joints formed on ENIG substrate. The IMC formed at the interface was Ni_3Sn_4, and some of the white phase near the interface was $AuSn_4$. Almost the entire EN layer crystallized into the Ni_3P layer with a column structure and between the Ni_3Sn_4 and

Ni_3P there was a NiPSn layer. When Sn-Ag solder reacted with different substrates, small particles and large plate-like Ag_3Sn IMCs could also be seen in the solder joints. Table 6-3 shows the compositions of phases formed in the solder joint of Sn-Ag on ENIG substrate. It can be seen that the $AuSn_4$ IMC contained some Ag.

The results also show that when CuImAg and ENIG substrates were used, the Ag and Au layer was completely dissolved by the solder and could no longer be seen. Table 6-4 summarises the phases and their features formed in the solder joints of different solders on different substrates.

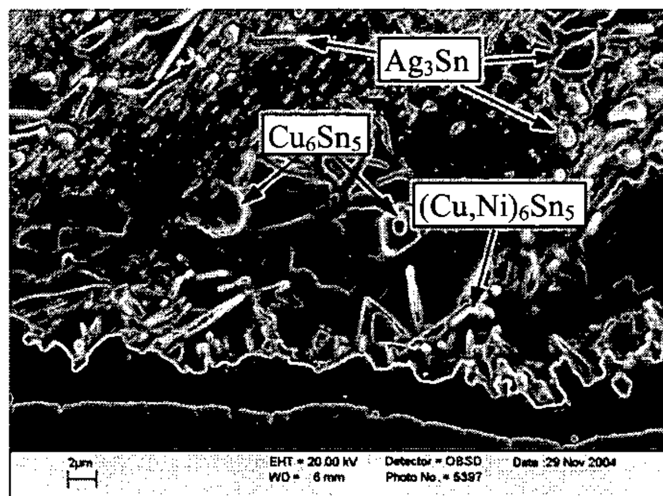


Fig. 6-46 IMCs formed at the interface of a Sn-Ag-Cu/ENIG solder joint.

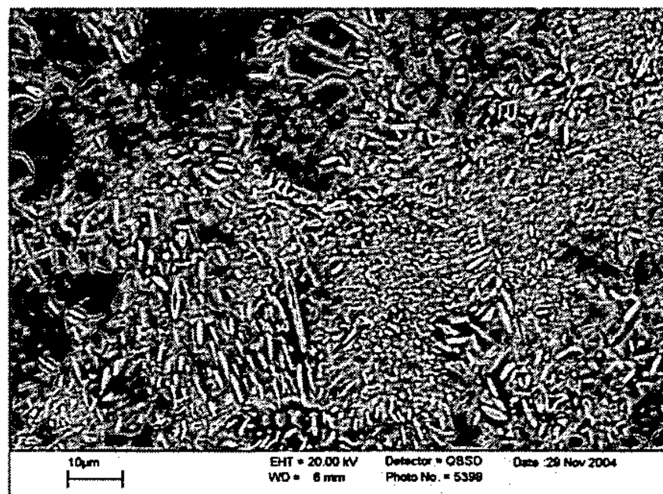


Fig. 6-47 IMCs formed in the solder of a Sn-Ag-Cu/ENIG solder joint.

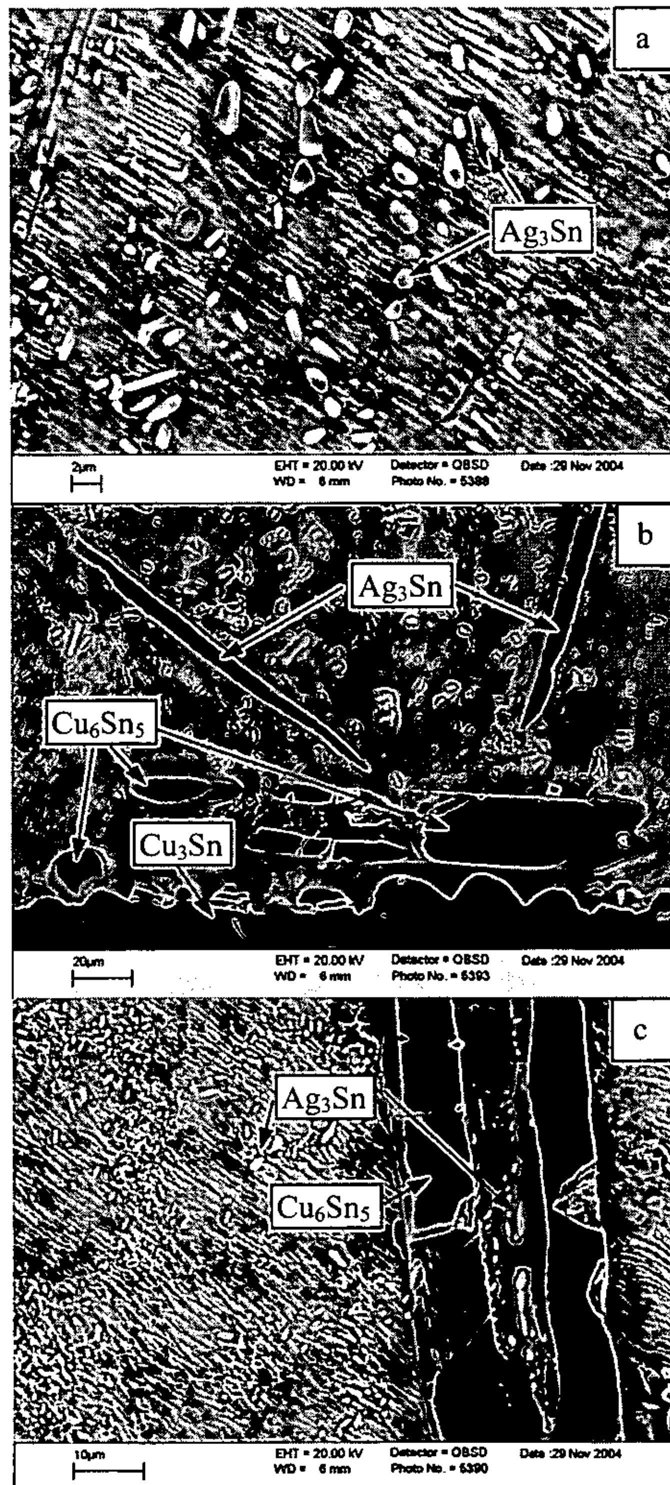


Fig. 6-48 IMCs formed in a Sn-Ag-Cu/Cu solder joint.

6.4.2 Morphology of IMCs

Figs. 6-46 and 6-47 show the IMCs formed at the interface and in the solder of a Sn-Ag-Cu/ENIG solder joint after etching the solder away. From Fig. 6-46, it can be seen that the $(Cu,Ni)_6Sn_5$ IMC formed at the interface is needle-like, but the bottom of the IMC layer is very compact and the individual needle cannot be seen. In the solder, the Cu_6Sn_5 IMC formed as a hexagonal prism shape with some of these appearing hollow; the Ag_3Sn IMC formed as the platelet-like or needle-like shapes, which can also be seen from Fig. 6-47.

Fig. 6-48 shows the morphologies of IMCs formed in the Sn-Ag-Cu/Cu solder joint after etching the solder around the IMCs away. The IMCs formed at the interface were Cu_6Sn_5 and Cu_3Sn, and Cu_6Sn_5 had a facet-like shape and the Cu_3Sn was a uniform layer following the topography of Cu substrate. It can be seen that the Ag_3Sn IMCs formed in the bulk solder were pebble- or needle- or plate-like. The Cu_6Sn_5 formed in the bulk solder was prismatic in shape, and some of the Cu_6Sn_5 IMCs was hollow with solder and Ag_3Sn IMC existing inside the chamber.

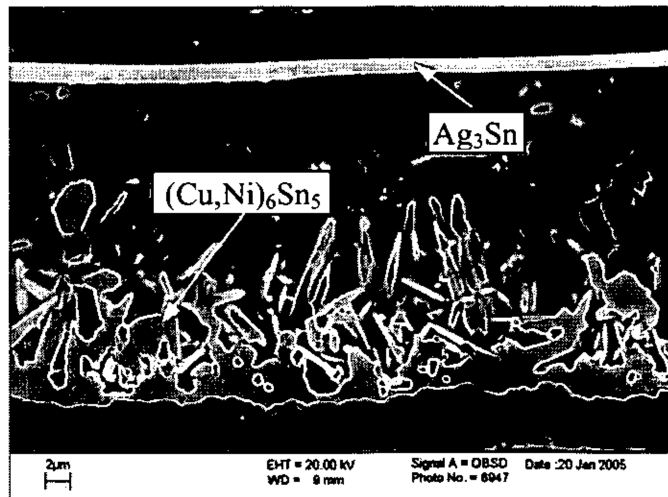


Fig. 6-49 IMCs formed in a Sn-Ag-Cu/EN solder joint.

Fig. 6-49 shows the morphologies of IMCs formed in the Sn-Ag-Cu/EN solder joint after etching the solder around the IMCs away. The IMC formed at the interface was the needle-like $(Cu,Ni)_6Sn_5$, and some plate-like Ag_3Sn IMCs formed in the solder, which could be as long as 500 μm. Other Ag_3Sn IMCs in the solder were pebble- or needle-like phases.

Figs. 6-50 to 6-52 show the morphologies of IMCs formed in the Sn-Ag-Cu/CuImAg, Sn-Ag/EN and Sn-Ag/CuImAg solder joints, respectively. The Cu_6Sn_5 and Ni_3Sn_4 IMCs formed at the interface were facet-like and Ag_3Sn IMCs in the solder were pebble- or needle- or plate-like.

Fig. 6-53 shows the morphologies of IMCs formed in a Sn-Cu/Cu solder joint after etching away the solder around the IMCs. The Cu_6Sn_5 formed at the interface was a facet-like phase, which had a larger length/diameter ratio than the Cu_6Sn_5 formed in Sn-Cu/CuImAg solder joints, and the Cu_6Sn_5 formed in the solder had hollow prismatic shape.

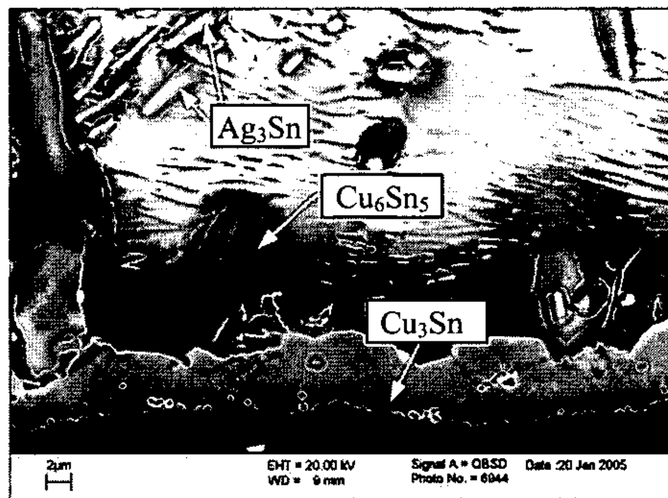


Fig. 6-50 IMCs formed in a Sn-Ag-Cu/CuImAg solder joint.

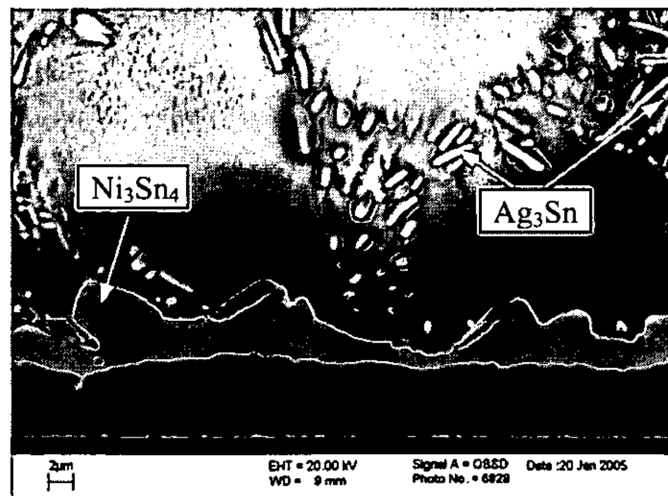


Fig. 6-51 IMCs formed in a Sn-Ag/EN solder joint.

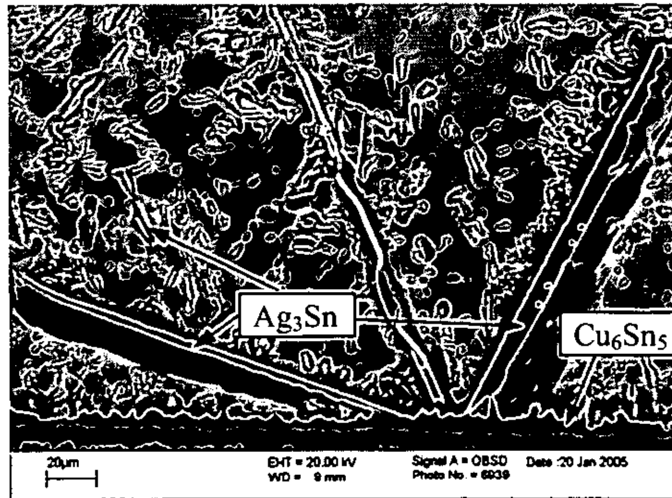


Fig. 6-52 IMCs formed in a Sn-Ag/CuImAg solder joint.

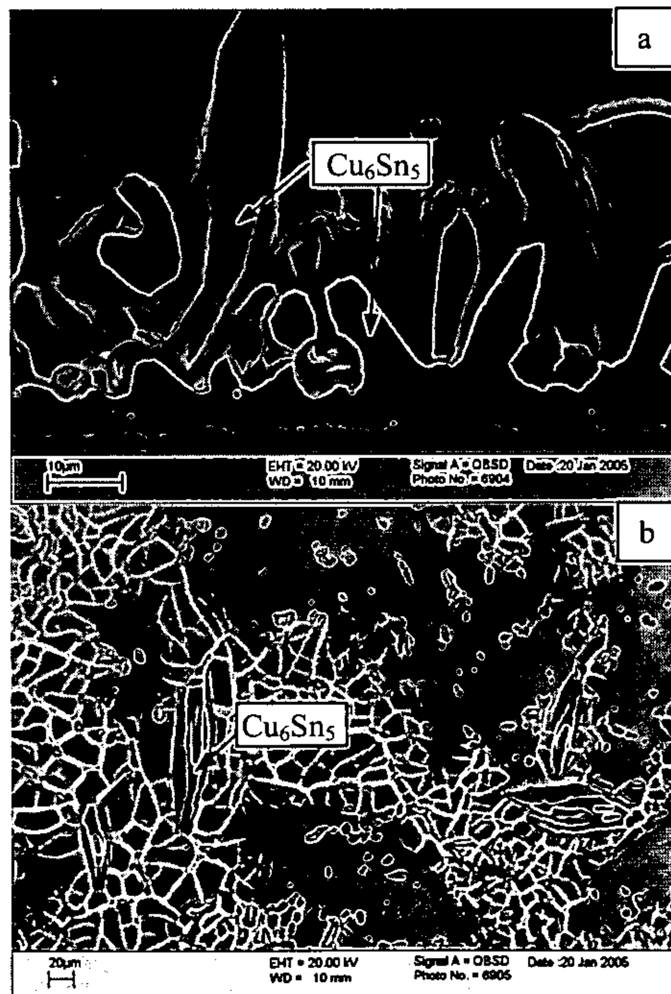


Fig. 6-53 IMCs formed in a Sn-Cu/Cu solder joint.

Fig. 6-54 shows the morphologies of IMCs formed in a Sn-Cu/ENIG solder joint after etching away the solder around the IMCs. It can be seen that the $(Cu,Ni)_6Sn_5$ IMCs formed at the interface could be needle-like or facet-like phases. When the IMCs were needle-like, the thickness was greater than that of IMCs with facet-like phases and the top of this IMC layer was not compact. EDX analysis shows that the compositions of these IMCs with different morphologies did not have great difference.

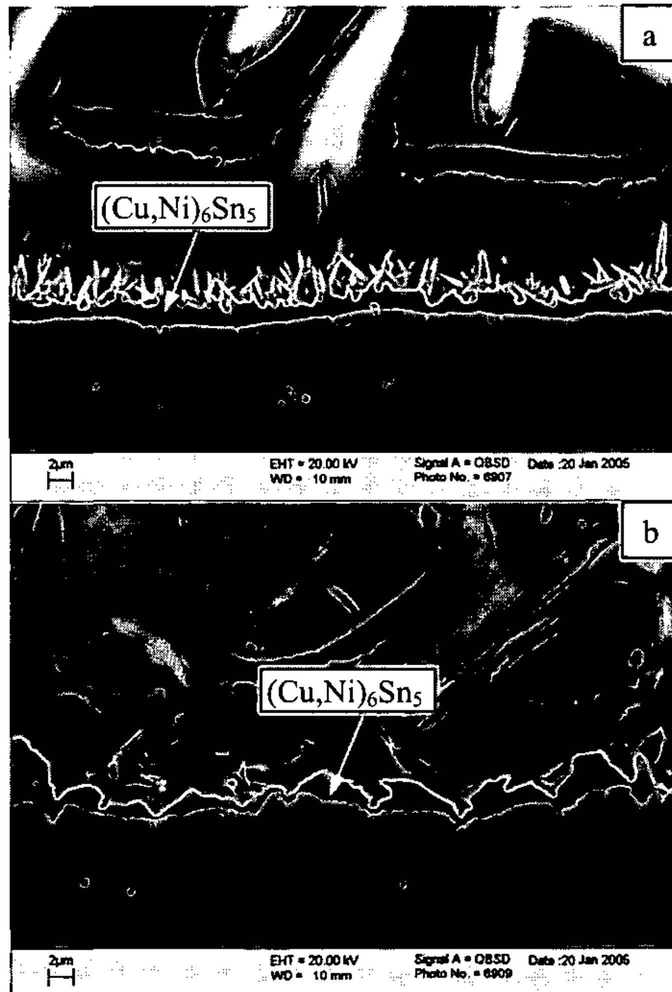
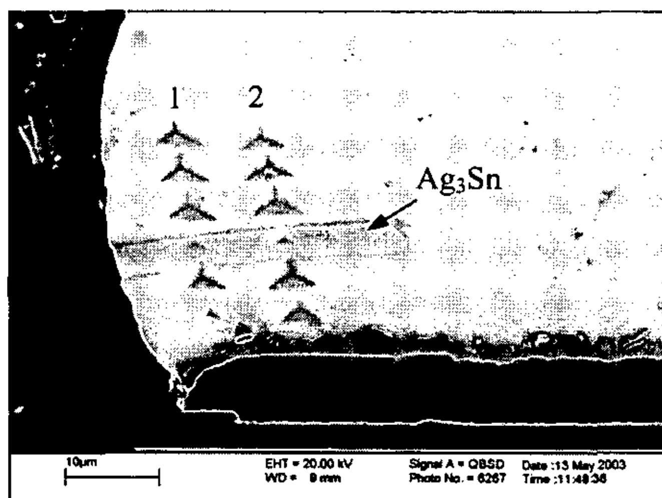


Fig. 6-54 IMCs formed in a Sn-Cu/ENIG solder joint, a) thick IMC and b) thin IMC.

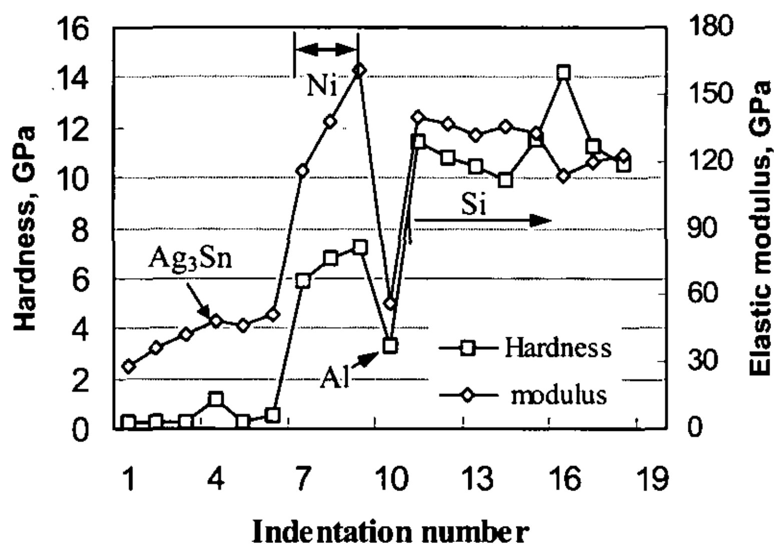
Only the typical results are shown above, and in general at the interface, the $(Cu,Ni)_6Sn_5$ IMCs formed were needle- or facet-like phases and the Cu_6Sn_5 and Ni_3Sn_4 IMCs were facet-like phases; in the solder, the Cu_6Sn_5 IMCs had a prism-like shape with some of them appearing hollow and the Ag_3Sn IMCs existed as plate- or pebble- or needle-like phases.

6.5 Micro-mechanical properties

The mechanical properties of individual phases in a solder joint may dictate the mechanical properties of the whole solder joint and the reliability of the electronic assembly. Due to the small size of the phases, these properties are quite hard to study using conventional methods and are instead studied in this research using nanoindentation techniques.

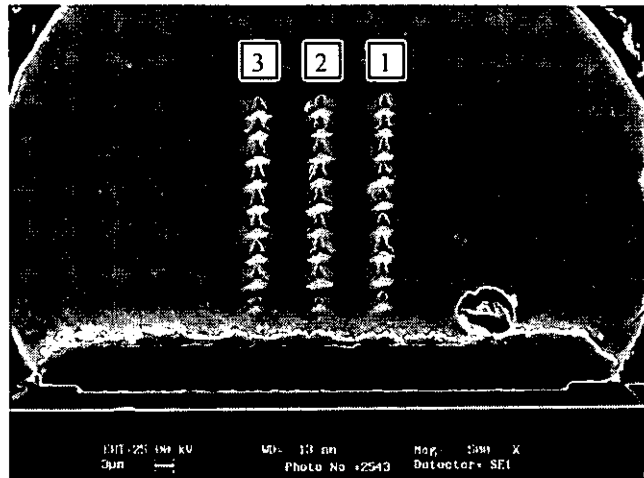


a)

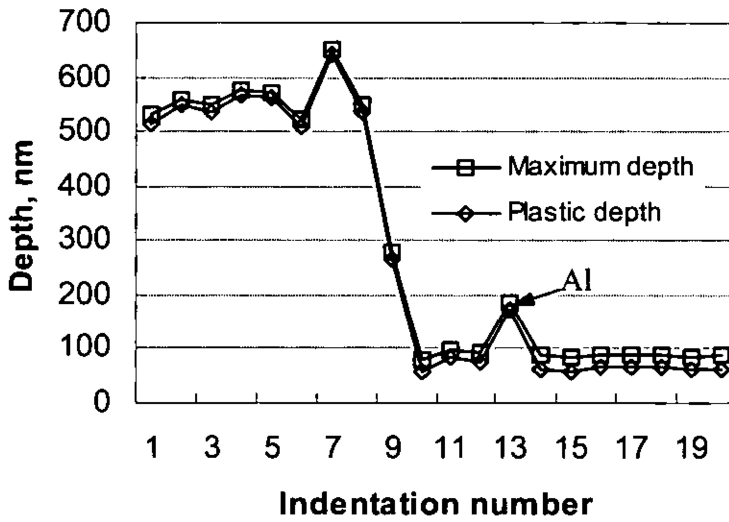


b)

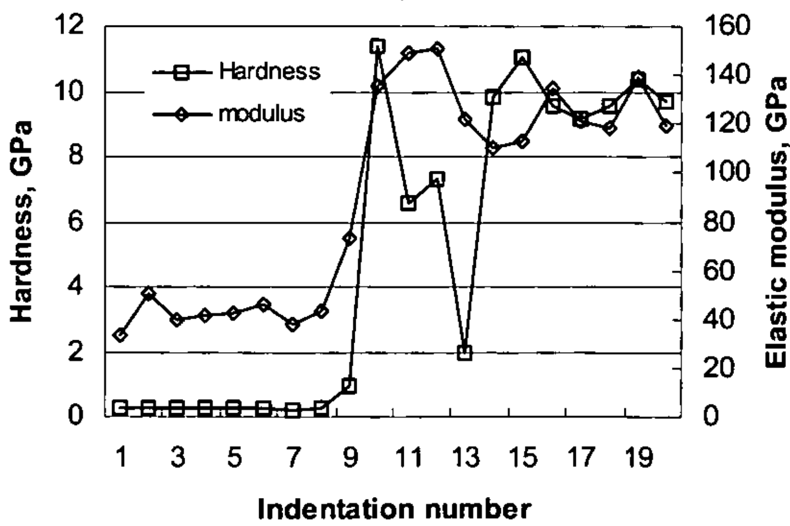
Fig. 6-55 Indentations of line 2 in a solder bump after ageing at 80°C for 50 h.



a)



b)



c)

Fig. 6-56 Indentations of line 2 in a solder bump after ageing at 80°C for 50 h.

6.5.1 Mechanical properties of ASH solder bumps

Fig. 6-55a shows the indentations in a solder bump after ageing 50 h in 80°C and Fig. 6-55b is the hardness and elastic modulus profiles of phases along line 2 in Fig. 6-55a. The indentations are numbered from the top to the bottom in the image. It can be seen that in different layers the indentations had different sizes. Indentation No.10 probably was in the Al layer because it presented much lower hardness and elastic modulus than the EN UBM and Si. It was very clear that indentation No. 4 was just in the middle of a Ag_3Sn IMC. The hardness and elastic modulus of Ag_3Sn were higher than those of the Sn-Ag-Cu solder material but smaller than those of $(Cu,Ni)_6Sn_5$ IMCs (indentation No.7).

Fig. 6-56 shows indentations and mechanical properties of phases across the interface of the solder bump after ageing 50 h in 80°C. The indentations in the solder show high depth and the indentations in $(Cu,Ni)_6Sn_5$ IMCs, EN UBM and Si are too small to be seen at this magnification. Indentation No.13 (line 2, counted from top) is in the Al pad and shows a low hardness and modulus.

Table 6-5 Mechanical properties of solder bumps after ageing at 80°C for 50 h.

Phases	**Hardness/GPa**	**Elastic Modulus/GPa**
Sn-3.8Ag-0.7Cu	0.27 ± 0.03	39.55 ± 8.49
Ag_3Sn*	1.04 ± 0.13	48.47 ± 0.85
$(Cu,Ni)_6Sn_5$*	5.40 ± 0.69	116.77 ± 1.64
Ni-P	7.18 ± 0.41	139.93 ± 13.67
Al**	1.45	91.56
Si	10.75 ± 1.36	126.79 ± 12.51

* Only two indentations located on this phase

** Only one indentation located on this phase

Table 6-5 shows the mechanical properties of different phases in the ASH solder bumps after ageing at 80°C for 50 h. The results illustrate that the Si and EN UBM have the highest hardness and modulus and $(Cu,Ni)_6Sn_5$ and Ag_3Sn IMCs are harder than Sn-Ag-Cu solder.

6.5.2 Mechanical properties of ASH solder joints after assembly

After ASH chips were assembled with test boards, the mechanical properties of solder joints were tested to have a comparison with those of ASH bumps before assembly. Fig. 6-57 shows the room temperature indentations and element mapping of solder joints after assembly. There were some $AuSn_4$ IMCs distributed in the solder joint. Fig. 6-58 shows the hardness and modulus of different phases along indentation line 2 in Fig. 6-57. Indentations No. 5 and 11 were in the EN UBM presenting high hardness and modulus. Indentations No. 6 and 10 were in the solder near $(Cu,Ni)_6Sn_5$ IMC and they presented higher hardness than those in the solder but away from the IMCs. Indentation No.12 was at the Al/Si interface.

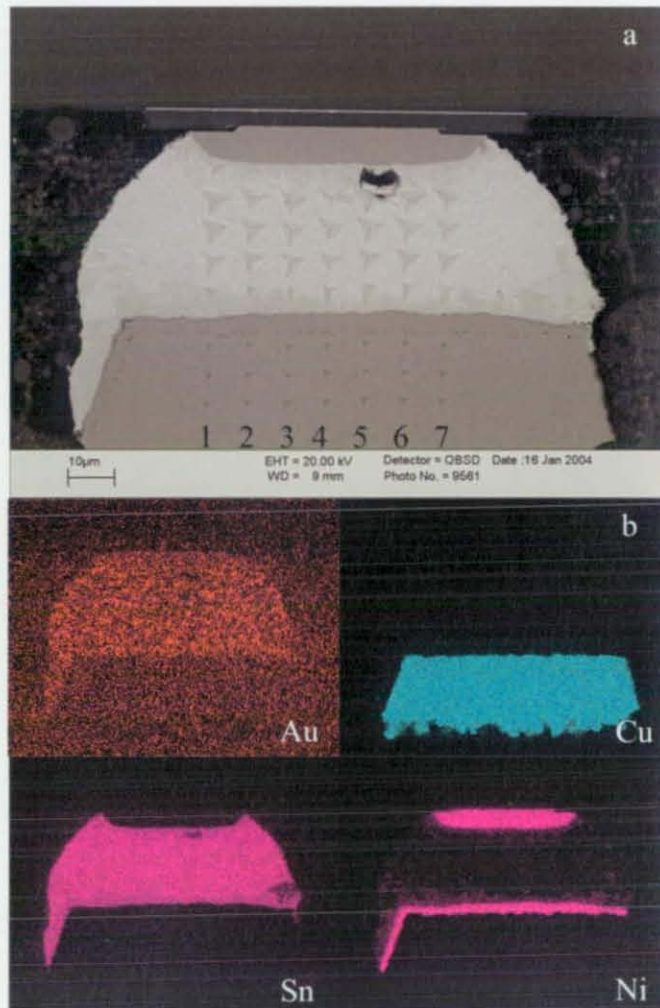


Fig. 6-57 Room temperature indentations and element mapping of solder joints.

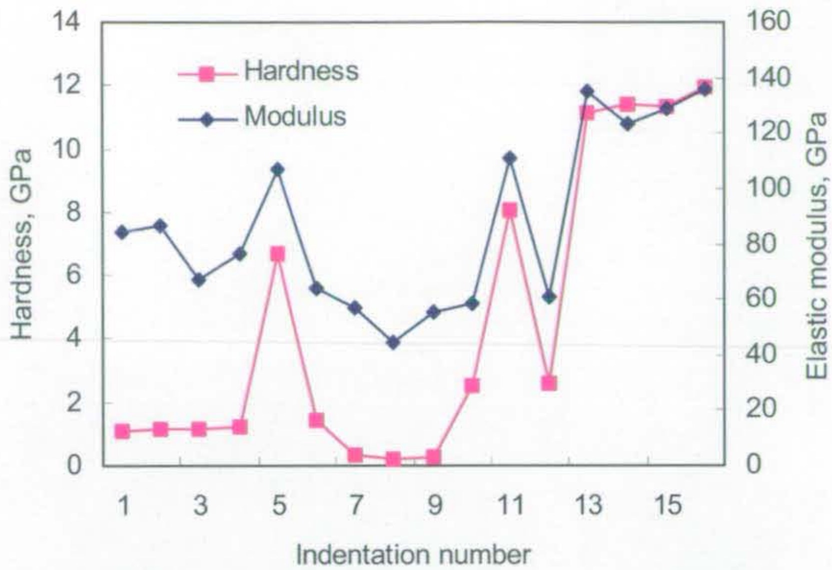


Fig. 6-58 Mechanical properties of line 2 in a solder joint at room temperature.

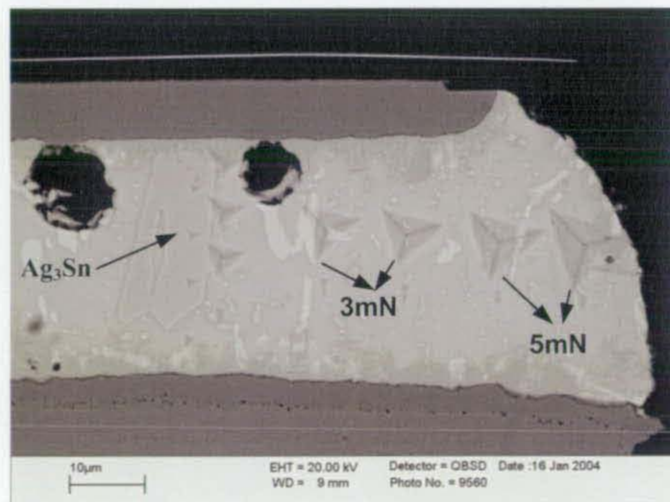


Fig. 6-59 Creep indentations in Sn-Ag-Cu solder and normal indentations in Ag_3Sn IMC tested at room temperature.

Table 6-6 Room temperature mechanical properties of phases in solder joints after assembly.

Phases	Hardness/GPa	Elastic Modulus/GPa
Sn-3.8Ag-0.7Cu	0.23 ± 0.04	45.51 ± 97.93
Ag_3Sn	1.8 7± 0.08	71.06 ± 6.53
$(Cu,Ni)_6Sn_5$	5.37 ± 0.67	108.27 ± 6.60
Ni-P	7.65 ± 0.27	136.10 ± 5.56
Al	1.32 ± 0.10	93.48 ± 8.70
Si	10.57 ± 0.28	139.66 ±4.43
Cu	1.18 ± 0.07	106.44 ± 9.73

Some indentation lines were put in $(Cu,Ni)_6Sn_5$ and Ag_3Sn IMCs over several trials, and Fig. 6-59 shows the SEM micrographs of the indentations on a Ag_3Sn phase tested at room temperature. The size of indentations on Ag_3Sn was much smaller than those at the Ag_3Sn/solder interface. Table 6-6 shows the room temperature mechanical properties of different phases in the solder joint after assembly. Fig. 6-60 shows the nanoindentation loading and unloading curves of different phases in solder joints at room temperature. Due to the scatter in hardness for different phases, different maximum loads were used. From the curves, it can be seen that when the same maximum load was used the indentations in different phases showed different depths and the slope of the unloading curves was different.

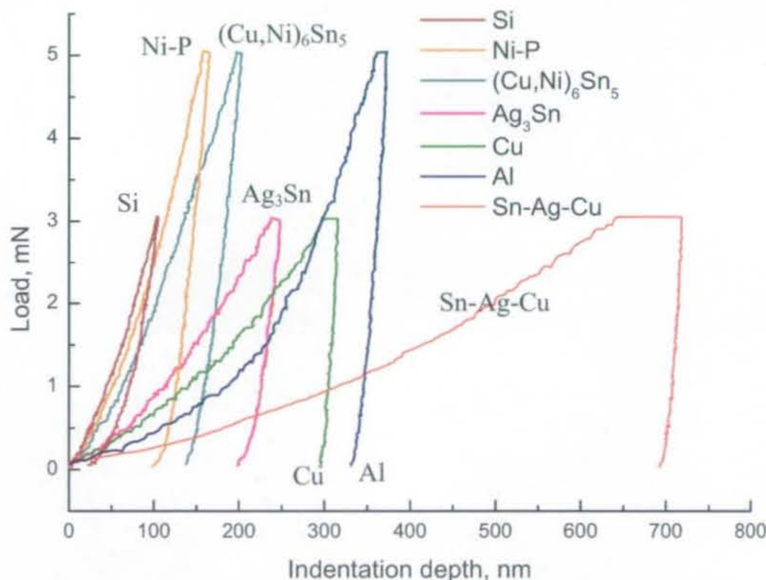


Fig. 6-60 Nanoindentation loading and unloading curves of different phases in solder joints at room temperature.

Fig. 6-61 shows the nanoindentations across the solder joint after ageing at 150°C for 24 h, and Table 6-7 shows mechanical properties of different phases in solder joints after ageing at 150°C for 24 h. Compared with the solder joints as-assembled, the mechanical properties of the phases did not change during ageing. Fig. 6-62 shows the nanoindentations across the solder joint after ageing at 150°C for 80 h, and Table 6-8 shows mechanical properties of different phases in solder joints after ageing at 150°C for 80 h. Although the hardness of most phases was a little higher than that in the solder joint after ageing 24 h, the value was still of a similar level.

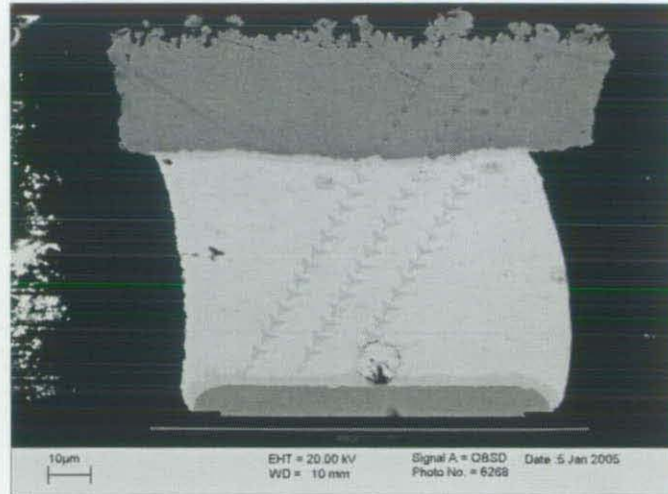


Fig. 6-61 Nanoindentations across a solder joint and ageing at 150°C for 24 h.

Table 6-7 Mechanical properties of phases in solder joints after ageing at 150°C for 24 h.

Phases	Hardness/GPa	Elastic Modulus/GPa
Sn-3.8Ag-0.7Cu	0.23 ± 0.02	48.97 ± 7.44
$(Cu,Ni)_6Sn_5$	6.05 ± 0.25	94.99 ± 3.54
Ni-P	9.16 ± 0.72	137.86 ± 10.26
Al	1.29 ± 0.02	110.54 ± 0.75
Si	12.89 ± 1.32	146.66 ± 8.56
Cu	1.58 ± 0.17	101.77 ±8.91

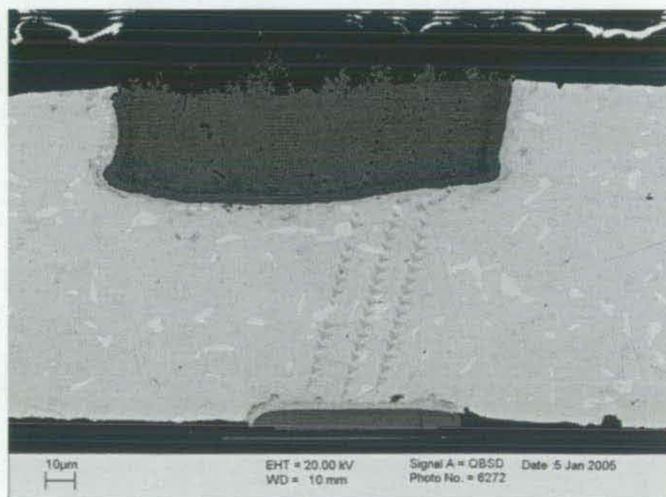


Fig. 6-62 Nanoindentations across a solder joint after ageing at 150°C for 80 h.

Table 6-8 Mechanical properties of phases in solder joints after ageing at 150°C for 80 h.

Phases	Hardness/GPa	Elastic Modulus/GPa
Sn-3.8Ag-0.7Cu	0.26 ± 0.04	50.09 ± 8.66
Ag_3Sn	2.84 ± 0.43	90.36 ± 6.68
$(Cu,Ni)_6Sn_5$	6.98 ± 1.98	98.72 ± 10.53
Ni-P	10.64 ± 1.47	149.33 ± 26.23
Al	1.64 ± 0.29	106.62 ± 14.42
Si	12.94 ± 1.52	143.21 ± 9.24
Cu	1.80 ± 0.27	111.47± 17.00

6.5.3 Mechanical properties of phases formed in long-time reflow

6.5.3.1 Properties at room temperature

The IMC phases formed after a long period of reflow were much larger than those in as-reflowed solder bumps, and in this case the influence of materials around the phases on the mechanical properties will be alleviated and the test will be more accurate. Figs. 6-63 to 6-67 show the indentations on Sn-0.7Cu, Sn-3.5Ag solders, Ni_3Sn_4, Cu_6Sn_5 and Ag_3Sn IMCs, respectively. It can be seen that the indentations in solders were of a much smaller size than those in the IMCs, and there were large margins around the indentations in IMCs.

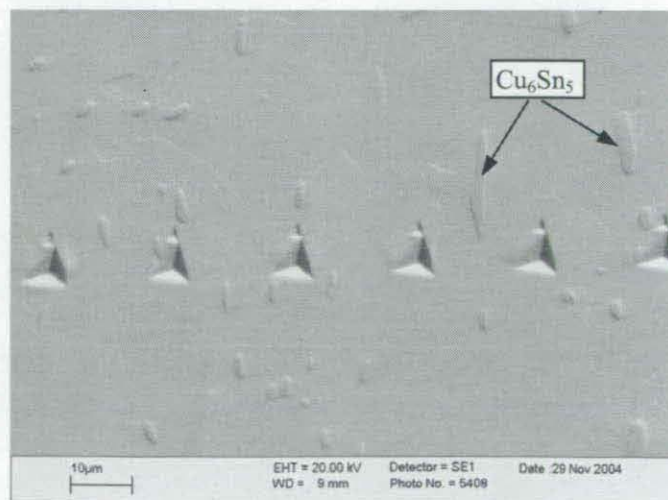


Fig. 6-63 Indentations on Sn-Cu solder in a Sn-Cu/Cu solder joint.

Fig. 6-64 Indentations on Sn-Ag solder in a Sn-Ag/EN solder joint.

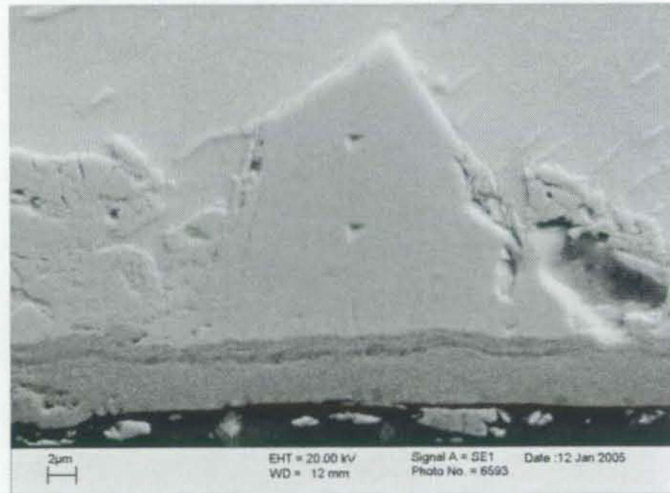


Fig. 6-65 Indentations on Ni_3Sn_4 IMC in a Sn-Ag/EN solder joint.

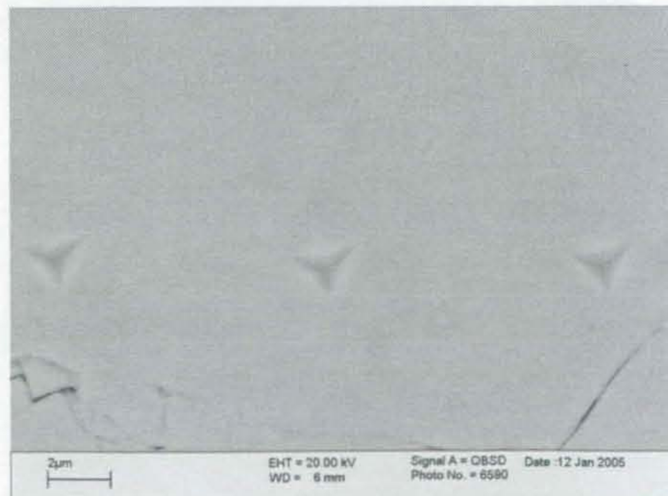


Fig. 6-66 Indentations on Cu_6Sn_5 IMC in a Sn-Cu/Cu solder joint.

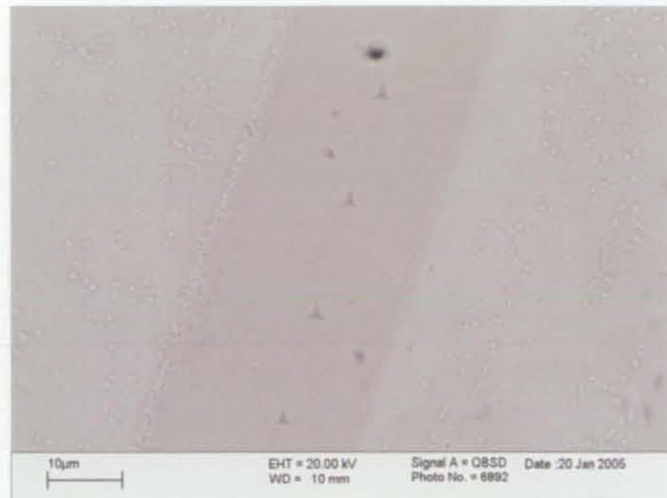


Fig. 6-67 Indentations on Ag_3Sn IMC in a Sn-Ag-Cu/Cu solder joint.

Fig. 6-68 shows the nanoindentation loading and unloading curves for different phases in solder joints at room temperature. It can be seen that due to the different hardness, when the same load was applied, different phases had different penetration depths. Table 6-9 shows the hardness and modulus of different phases from different kinds of solder joints at room temperature. It can be seen that the Ni_3Sn_4 and Cu_6Sn_5 IMCs had the highest hardness followed by the Cu_3Sn IMCs. The mechanical properties of different solders were of the same level, although Sn-Ag-Cu and Sn-Pb were a little harder than Sn-Cu and Sn-Ag. Compared with the mechanical properties of phases in small solder joints, it can be seen that the properties presented some variation.

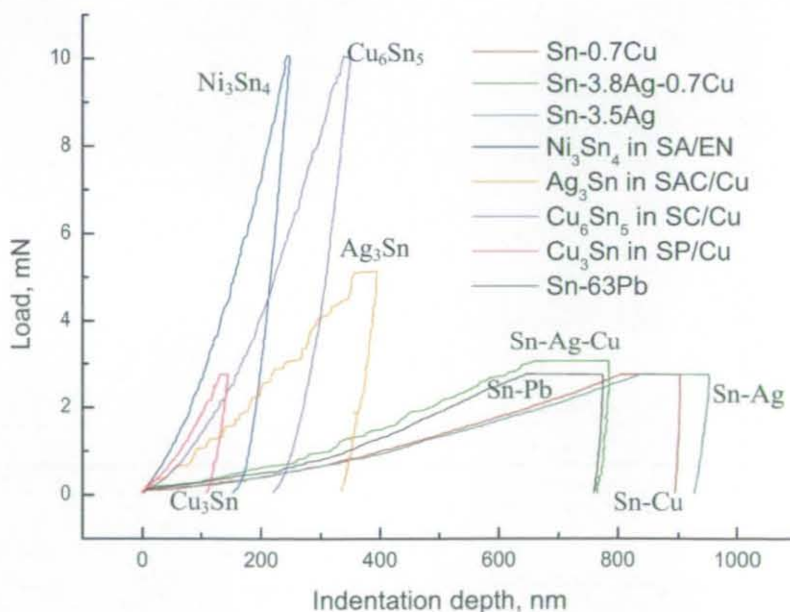


Fig. 6-68 Nanoindentation loading and unloading curves of different phases.

Table 6-9 Mechanical properties of different phases at room temperature.

Phases	Hardness/GPa	Elastic Modulus/GPa
Sn-3.8Ag-0.7Cu	0.23 ± 0.03	56.44 ± 6.90
Sn-3.5Ag	0.18 ± 0.02	54.87 ± 15.38
Sn-0.7Cu	0.14 ± 0.01	66.06 ± 12.96
Sn-63Pb	0.20 ± 0.02	54.82 ± 7.81
Ag_3Sn in SAC/Cu joint	1.58 ± 0.25	61.97 ± 5.90
Cu_6Sn_5 in SC/Cu joint	6.17 ± 0.41	114.79 ± 5.97
Ni_3Sn_4 in SA/EN joint	7.08 ± 0.29	128.53 ± 10.77
Cu_3Sn in SP/Cu joint	5.59 ± 0.83	138.35± 8.47

Table 6-10 Mechanical properties of different phases at elevated temperatures.

		Hardness/GPa			Elastic Modulus/GPa		
		125°C	150°C	175°C	125°C	150°C	175°C
Sn-Ag-Cu on Cu	Ag_3Sn	1.47±0.17	0.42	0.02±0.00	47.15±3.32	8.44	0.55±0.08
	Cu_6Sn_5	3.19±0.05	-	0.14±0.01	66.09±1.00	-	0.89±0.07
	SAC	0.05±0.01	-	0.01±0.00	23.74±3.63	-	0.38±0.26
Sn-Ag on EN	Ag_3Sn	5.29±0.75	-	-	78.44±2.35	-	-
	Ni_3Sn_4	4.43±0.11	-	0.89±0.07	74.88±7.17	-	8.18±0.66
	SA	0.05±0.01	0.03±0.00	0.01±0.00	16.95±1.73	4.75±0.37	2.06±0.36
Sn-Cu on Cu	Cu_6Sn_5	2.38±0.27	1.04±0.18	0.58±0.05	52.59±6.01	35.93±1.63	11.51±0.79
	SC	0.05±0.01	-	0.03±0.00	15.47±2.09	-	5.39±0.57

6.5.3.2 Properties at elevated temperatures

Table 6-10 shows the hardness and modulus of different phases from different kinds of solder joints at elevated temperatures. It can be seen that the hardness and modulus of IMCs were lower at 125°C than at room temperature. However, the hardness and modulus of IMCs at even higher temperatures (150°C and 175°C) became too low to accurately represent their mechanical properties. It is possible that the mechanical properties of IMCs from nanoindentation were not reliable due to the strong influence of the surrounding solder materials. For the lead free solder materials, their hardness and modulus at elevated temperatures were much lower than those at room temperature, and the decrease of hardness was more evident than that of modulus. It can be seen that

the higher the melting temperature of the solder, the smaller the influence of test temperature on the mechanical properties, such that the moduli of Sn-Cu and Sn-Ag were higher than that of Sn-Ag-Cu at 175°C. Another result noticed is that the same kind of IMC formed from different solder/substrate solder joints had different mechanical properties, which may be caused by the different element contents in these phases. From table 6-1 to 6-3, it can be seen that when the substrate was Cu the element contents of Ag and Sn in Ag_3Sn was about 75at.% and 25at.%, respectively, and when the substrate was EN the element contents changed to about 57at.% and 43at.%, respectively. It seems that the existence of Ni may change the element content of Ag_3Sn although Ag_3Sn phases normally do not contain any Ni.

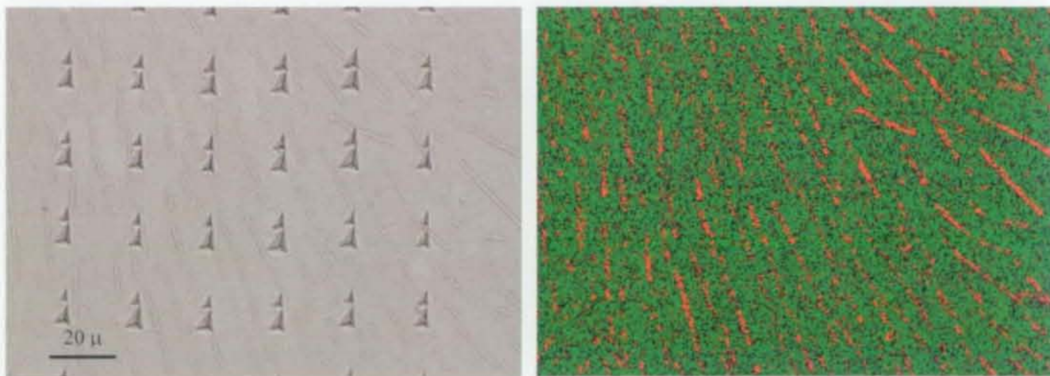


Fig. 6-69 Indentations and element mapping in Sn-Ag bulk solder cooled in air. Element mapping, red: Ag, green: Sn.

Fig. 6-70 Indentations and element mapping in Sn-Ag bulk solder cooled in furnace. Element mapping, red: Ag, green: Sn.

6.5.4 Mechanical properties of bulk solders with different cooling media

Fig. 6-69 shows the indentations and element mapping of Sn-Ag bulk solder cooled in a free air environment. The middle size plate-like Ag_3Sn IMCs were distributed evenly in the solder, and the size of the indentations was uniform. For each indentation, there is also a smaller adjacent indentation, which was caused by the pre-contact of the indenter with the sample. For Nano Test 6000 nanoindentation, before the indentation penetration the indenter needs to pre-contact the sample surface to get a depth reference. Due to the pendulum mechanism, the pre-contact point is different from the test point, and for soft materials a smaller indentation will appear beside the testing indentation. Fig 6-70 shows the indentations and element mapping of Sn-Ag bulk solder cooled in a furnace environment. The middle size plate-like Ag_3Sn IMC was distributed throughout the solder, but compared to the solder cooled in free air, the size was larger and the number was smaller. Some indentations were on the Ag_3Sn IMC, and their size was smaller. Fig. 6-71 shows the indentations and element mapping of Sn-Ag bulk solder cooled in water. It shows that many small Ag_3Sn particles were distributed around the grain boundaries of β-Sn and the size of the indentations was very uniform.

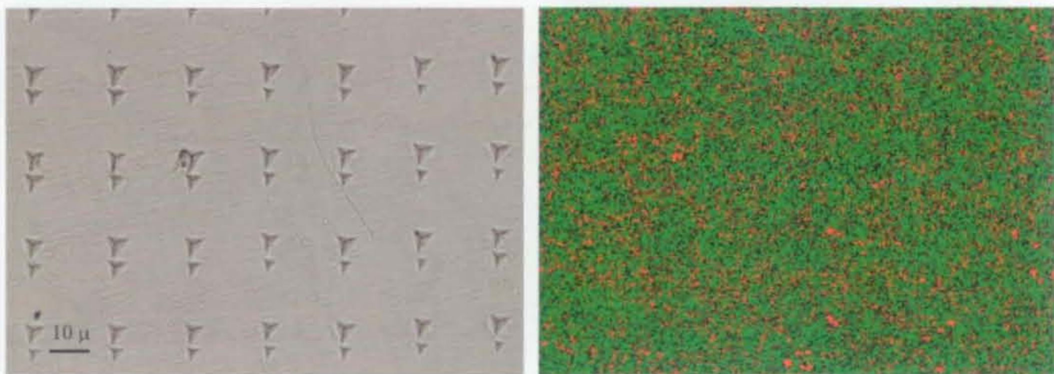


Fig. 6-71 Indentations and element mapping in Sn-Ag bulk solder cooled in water. Element mapping, red: Ag, green: Sn.

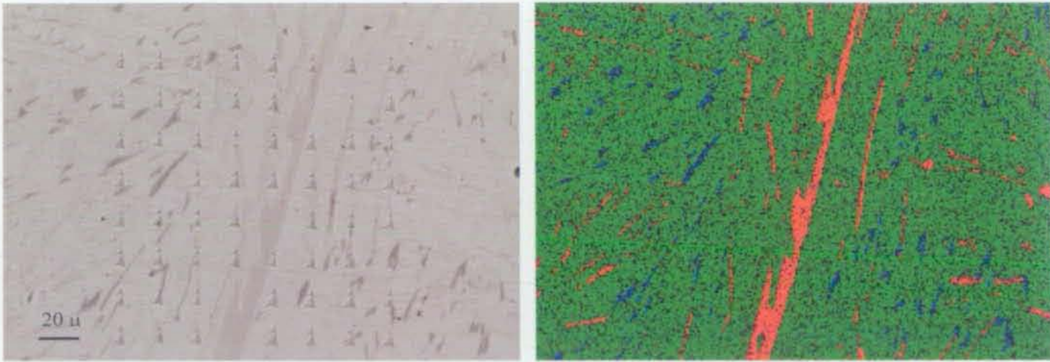


Fig. 6-72 Indentations and element mapping in Sn-Ag-Cu bulk solder cooled in air. Element mapping, red: Ag, green: Sn, blue: Cu.

Fig. 6-72 shows the indentations and element mapping of Sn-Ag-Cu bulk solder cooled in a free air environment. The middle size plate-like Ag_3Sn and Cu_6Sn_5 IMCs and some large Ag_3Sn IMC were distributed in the solder. Some indentations on the large Ag_3Sn IMC were much smaller and could almost not be seen at this magnification. Fig. 6-73 shows the indentations and element mapping of Sn-Ag-Cu bulk solder cooled in a furnace environment. Both large and middle size Ag_3Sn and Cu_6Sn_5 IMCs were distributed in the solder and the indentations on the large IMCs were much smaller. Fig. 6-74 shows the indentations and element mapping of Sn-Ag-Cu bulk solder cooled in water. The Ag_3Sn and Cu_6Sn_5 IMCs were too small to be seen, but they caused the optical contrast in the image to be different from that of β-Sn without IMC distribution. It can also be seen that the indentations were quite uniform for this cooling regime.

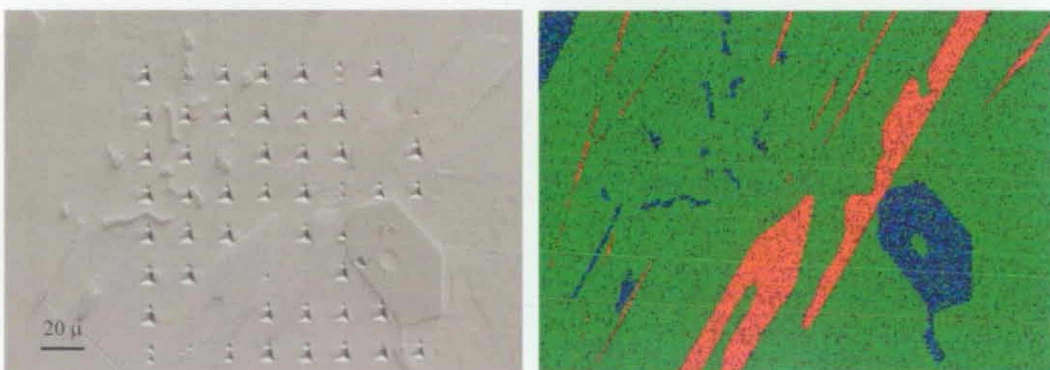


Fig. 6-73 Indentations and element mapping in Sn-Ag-Cu bulk solder cooled in furnace. Element mapping, red: Ag, green: Sn, blue: Cu.

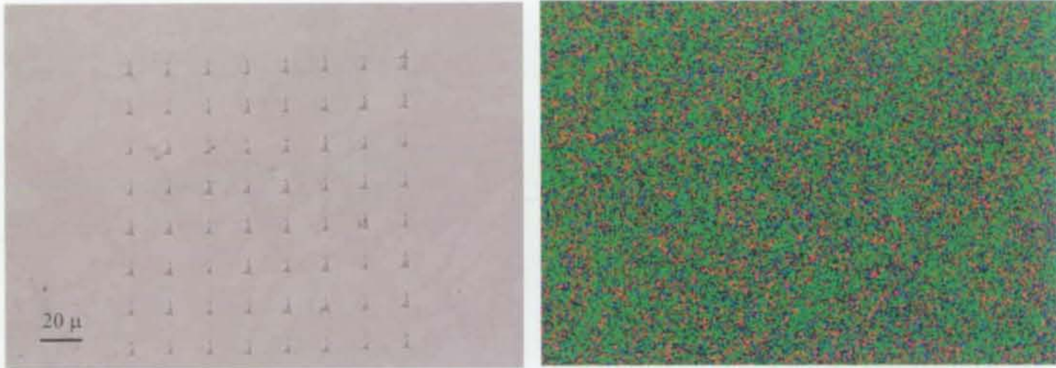


Fig. 6-74 Indentations and element mapping in Sn-Ag-Cu bulk solder cooled in water. Element mapping, red: Ag, green: Sn, blue: Cu.

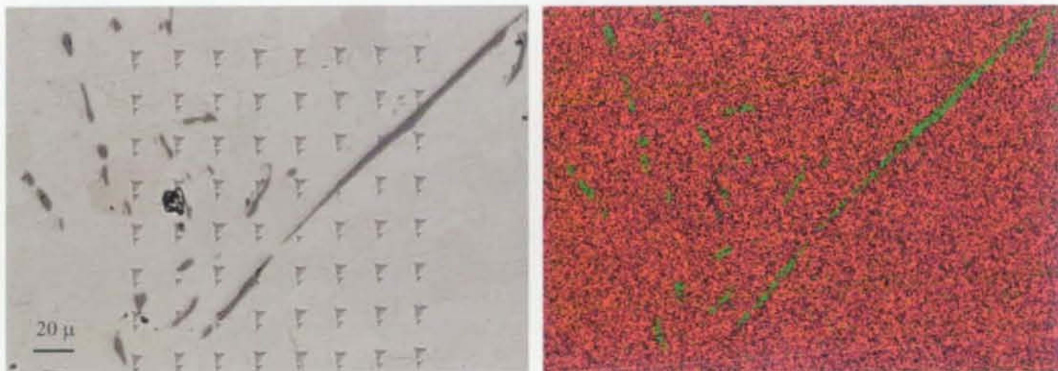


Fig. 6-75 Indentations and element mapping in Sn-Cu bulk solder cooled in furnace. Element mapping, red: Sn, green: Cu.

Fig. 6-75 shows the indentations and element mapping of Sn-Cu bulk solder cooled in a furnace environment. Some plate- and facet-like Cu_6Sn_5 IMCs were distributed in the solder. When the indentations were in the IMCs, their size was much smaller than that of indentations in solder. Fig. 6-76 shows the indentations and element mapping of Sn-Cu bulk solder cooled in water. It can be seen that the very small Cu_6Sn_5 IMCs were distributed around the β-Sn grain boundaries and the indentations were very uniform.

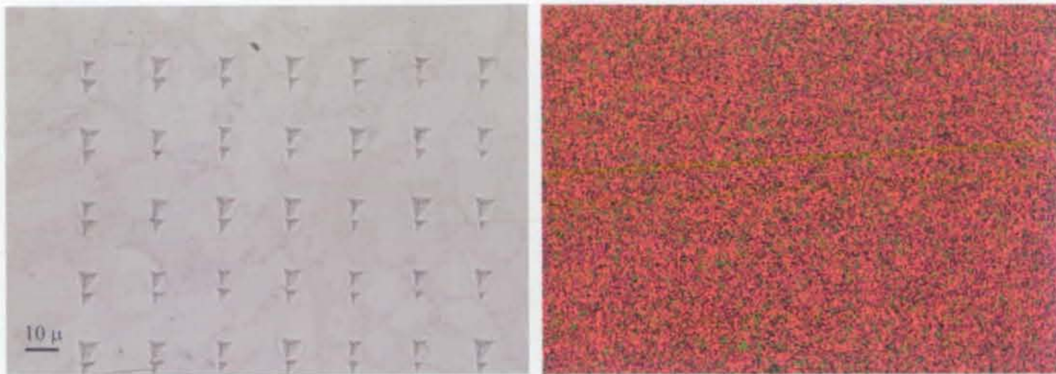


Fig. 6-76 Indentations and element mapping in Sn-Cu bulk solder cooled in water. Element mapping, red: Sn, green: Cu.

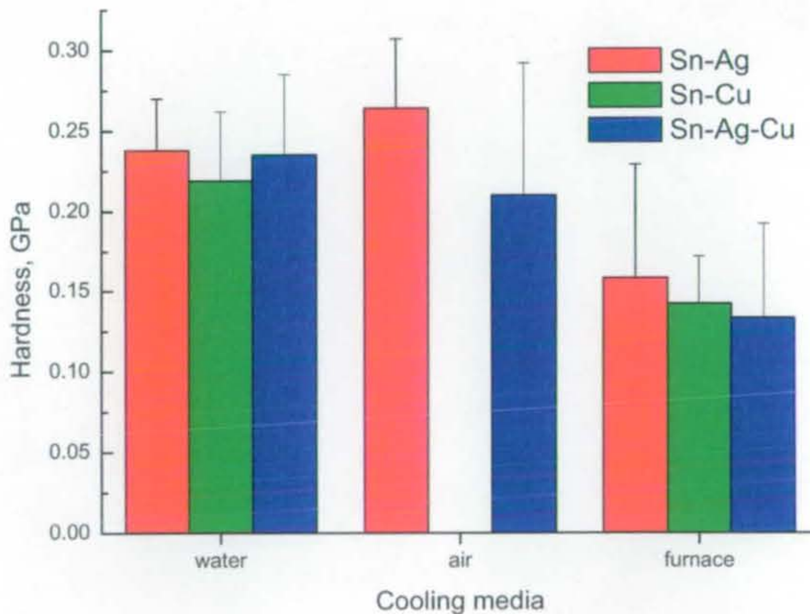


Fig. 6-77 Hardness of Sn-Ag, Sn-Cu and Sn-Ag-Cu lead free solders cooled in different media.

The hardness and modulus from all the indentations were calculated and the indentations on the IMCs were removed from the statistics. Fig. 6-77 and 6-78 show the average hardness and modulus of Sn-Ag, Sn-Cu and Sn-Ag-Cu lead free solders cooled in water, air and furnace regimes respectively. They illustrate that the hardness and modulus of these lead free solders were similar, and the solders cooled in water and air had higher hardness and modulus than those cooled slowly in a furnace environment.

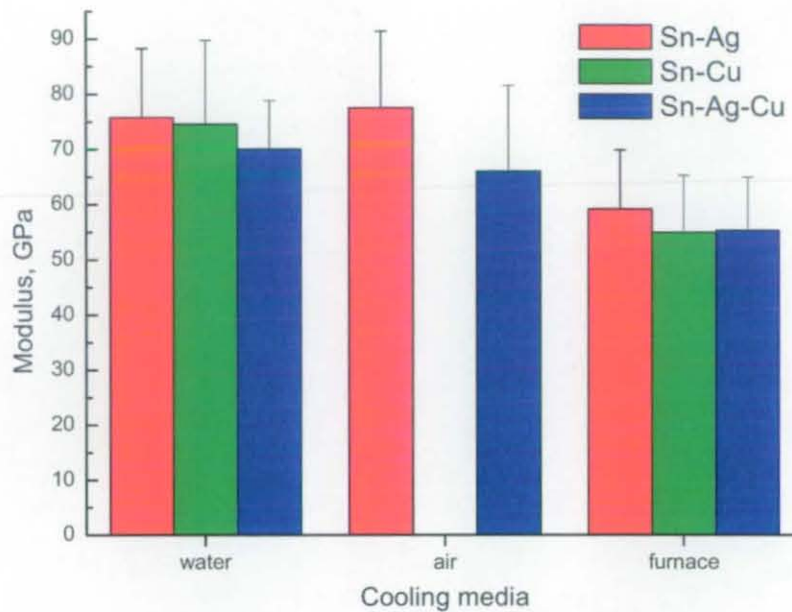


Fig. 6-78 Modulus of Sn-Ag, Sn-Cu and Sn-Ag-Cu lead free solders cooled in different media.

6.6 Creep properties

Due to the low melting temperature of solder materials, creep deformation of solder joints is critical, even at room temperature. The creep property of Sn-Pb has been studied widely [71-76]; however, Sn-Pb solder will be replaced by lead free solders due to impending legislation. As such it is worthwhile understanding the creep properties of lead free solders.

During nanoindentation tests, if the load is held constant, the indenter will continue to travel into the material in a time dependent manner, since creep flow under the indenter load occurs. This allows a study of the creep properties of very small quantities of material [77]. Creep rates of a given alloy are dependent on stress and normally the steady-state creep rate of metals is affected by a power function of the stress. This can be represented as:

$$\dot{\varepsilon} = k\sigma^{n} \tag{6-1}$$

where $\dot{\varepsilon}$ is the creep rate, σ the stress, n the stress exponent and k is a constant, from this, the stress exponent can be expressed as:

$$n = \frac{d(\ln \dot{\varepsilon})}{d(\ln \sigma)} \tag{6-2}$$

For nanoindentation, the creep rate and stress can be expressed as the following equations respectively [77, 78]:

$$\dot{\varepsilon} = \frac{1}{h}\frac{dh}{dt} \tag{6-3}$$

$$\sigma = \frac{P}{A} \tag{6-4}$$

where h is the indentation depth, t the creep time, A contact area and P is the load. The indentation depth is used to approximate the effective indentation depth during the calculation.

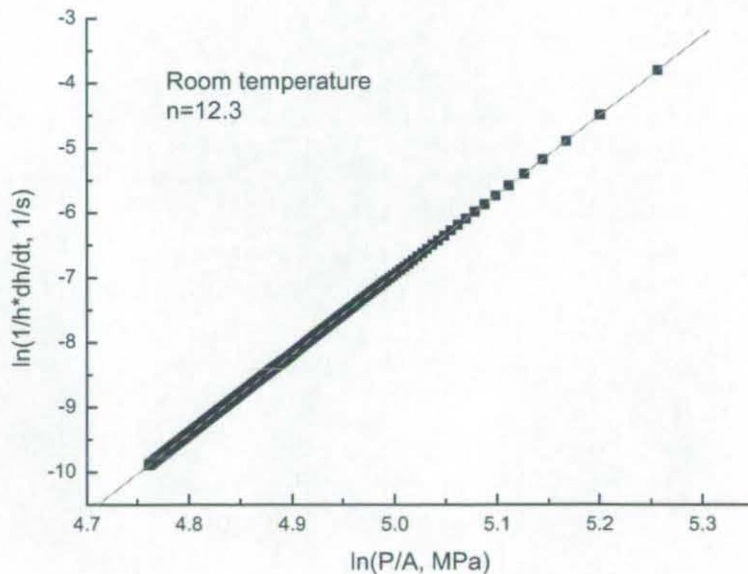


Fig. 6-79 Creep stress exponent of Sn-Ag-Cu solder at room temperature.

6.6.1 Creep property of solder joints

The creep property of Sn-Ag-Cu solder in flip chip solder joints was tested at room temperature. Curves were fitted to the data and the creep exponent was calculated using the method described above. Fig. 6-59 shows the indentations on solder after creep testing at room temperature. When there were some IMCs in the solder, the creep marks of the indentations became smaller due to the influence of the hard IMCs. Fig. 6-79 shows that the creep exponent of Sn-Ag-Cu solder at room temperature is 12.3.

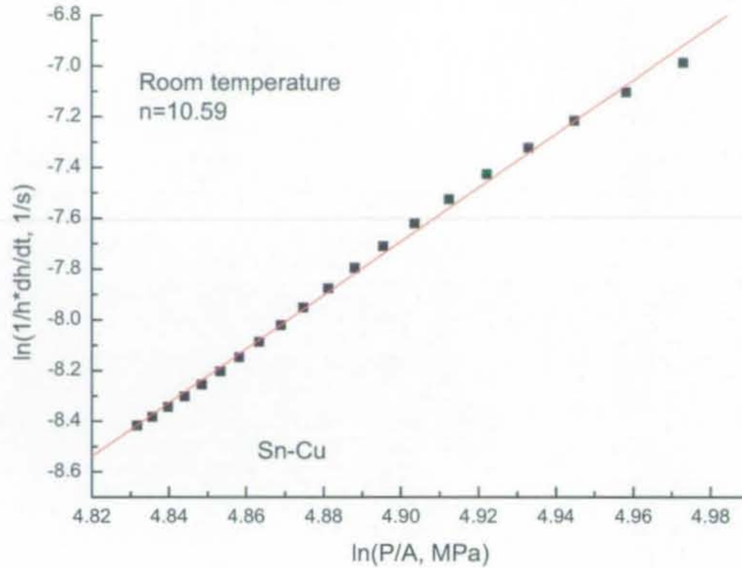


Fig. 6-80 Creep exponent of Sn-Cu at room temperature.

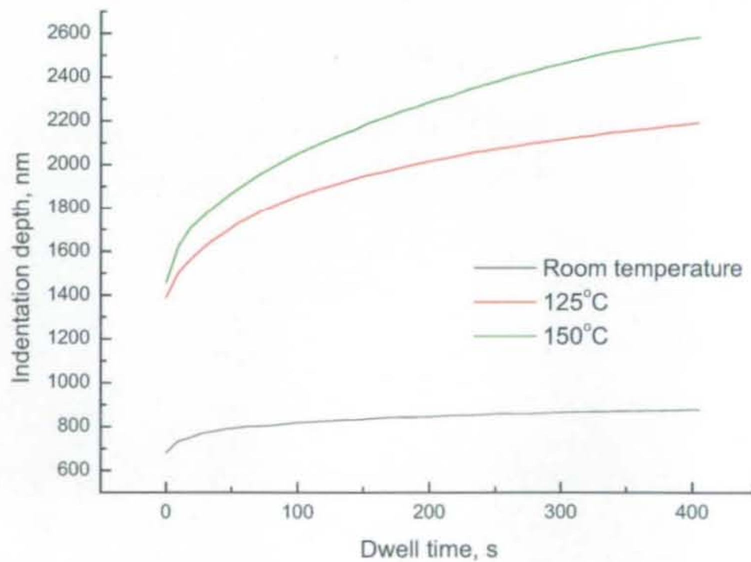


Fig. 6-81 Creep curves of Sn-Ag-Cu at different temperatures.

The creep properties of lead free solders in much larger solder joints, formed with different lead free solders and substrates after long periods of reflow, were also conducted and compared. Fig. 6-80 shows the creep exponent of Sn-Cu at room temperature. Due to the curve quality, fitting accuracy and problems inherent in nanoindentation test (steady state creep cannot be reached when sharp indenters are used [79]), the curve was not a perfect line, and the creep exponent was derived through a linear fitting of this curve.

Fig. 6-81 shows the creep curves of Sn-Ag-Cu solder in Sn-Ag-Cu/Cu solder joints at different temperatures under a load of 3 mN. It can be seen that the higher the test temperature the deeper the indentations and the larger the strain rate (slope on the curves). Fig. 6-82 shows the creep exponent of Sn-Ag-Cu at different temperatures. It can be seen that at higher temperatures the creep exponent of the solder would become smaller.

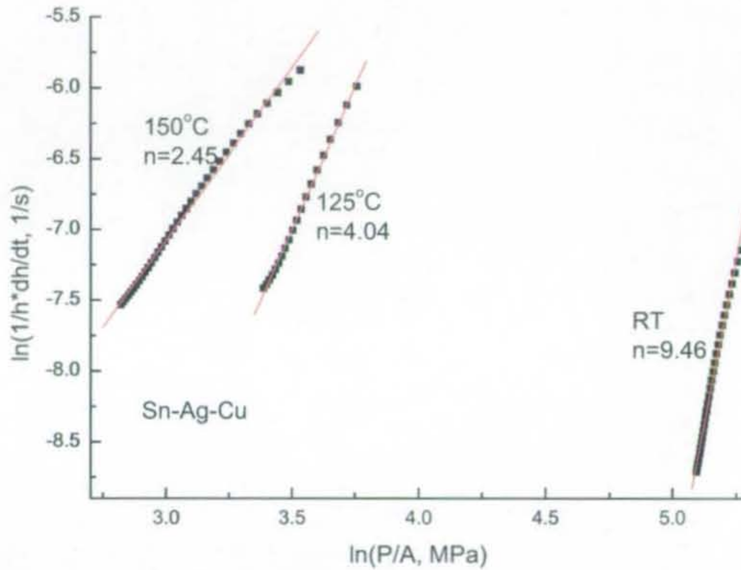


Fig. 6-82 Creep exponent of Sn-Ag-Cu at different temperatures.

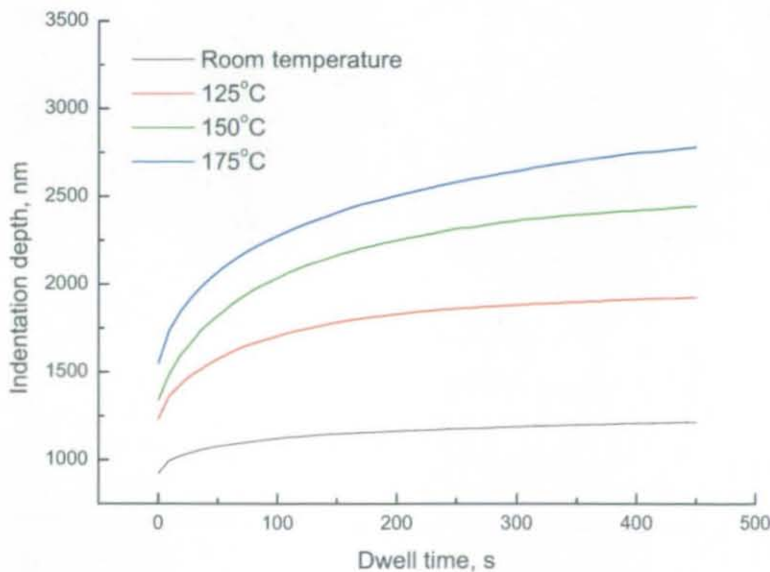


Fig. 6-83 Creep curves of Sn-Ag at different temperatures.

Fig. 6-83 and 6-84 show the creep curves and creep exponents of Sn-Ag solder in Sn-Ag/EN solder joints, respectively. It can be seen that the creep curves and exponents

changed with the temperature in a similar manner to those of Sn-Ag-Cu solder. Comparison of the creep properties of these two lead free solders shows that the creep exponents of Sn-Ag solder was a little higher than those of Sn-Ag-Cu solder.

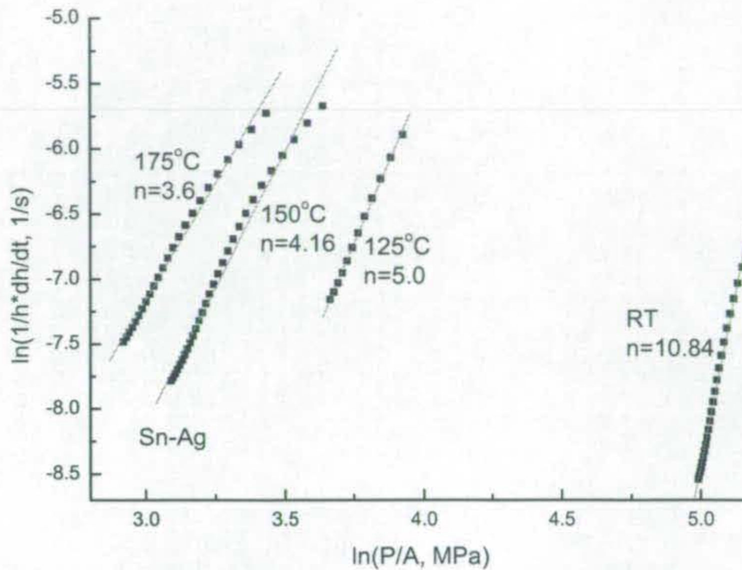


Fig. 6-84 Creep exponent of Sn-Ag at different temperatures.

6.6.2 Creep property of bulk solders

Creep testing was also conducted on lead free bulk solders solidified in different cooling media, in order to find the influence of solder volume and cooling rate on the creep properties of lead free solders.

Figs. 6-85 to 6-89 show the curves of ln($\dot{\varepsilon}$) vs. ln(σ) of different lead free solders solidified in different cooling media and Table 6-11 shows their creep exponents. It can be seen that the creep exponent of lead free solders ranged from 7.5 to 11.5, and the creep exponent of Sn-Ag solder with small distributed IMCs was higher than that of a solder without IMCs. It seems that the distribution of small IMCs can improve the creep properties of a solder. It can also be seen that the creep properties of the studied lead free solders were similar, and the variation might be caused by the IMC distribution, since the selected point for creep testing could be in an area with small IMCs or an area without IMCs. Generally, the cooling media did not change the creep properties of solders.

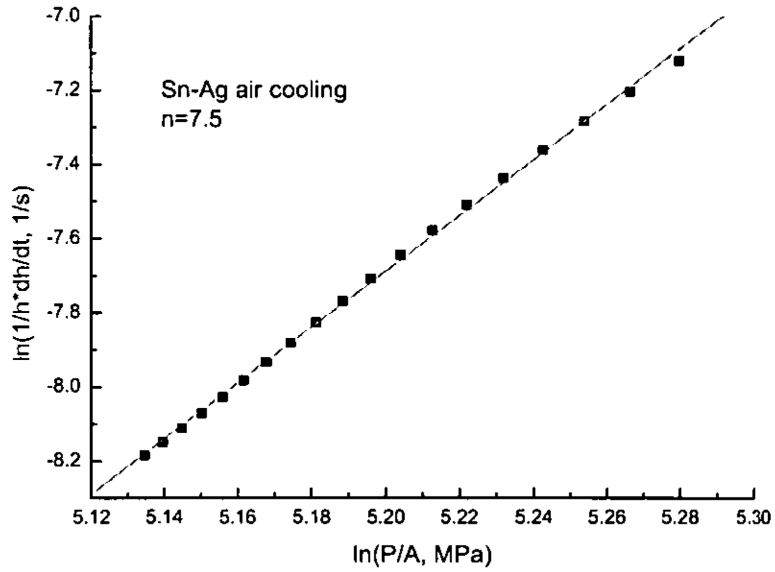


Fig. 6-85 Creep exponent of Sn-Ag solder cooled in ambient air.

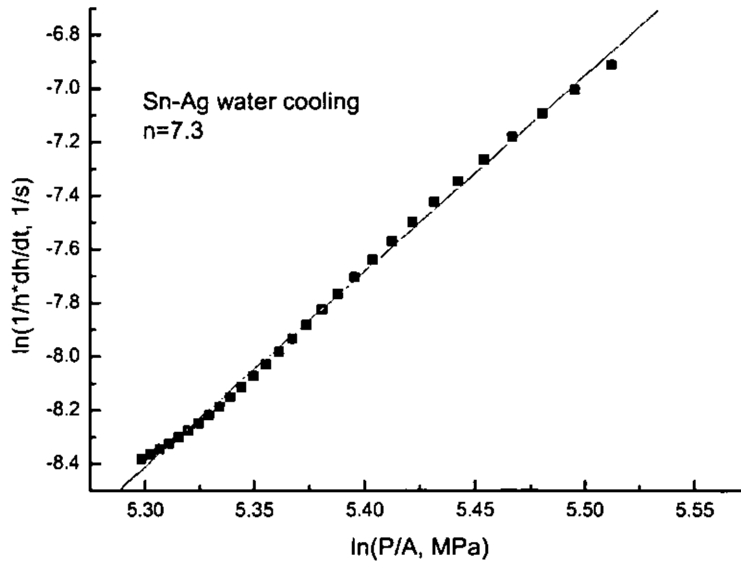


Fig. 6-86 Creep exponent of Sn-Ag solder cooled in water.

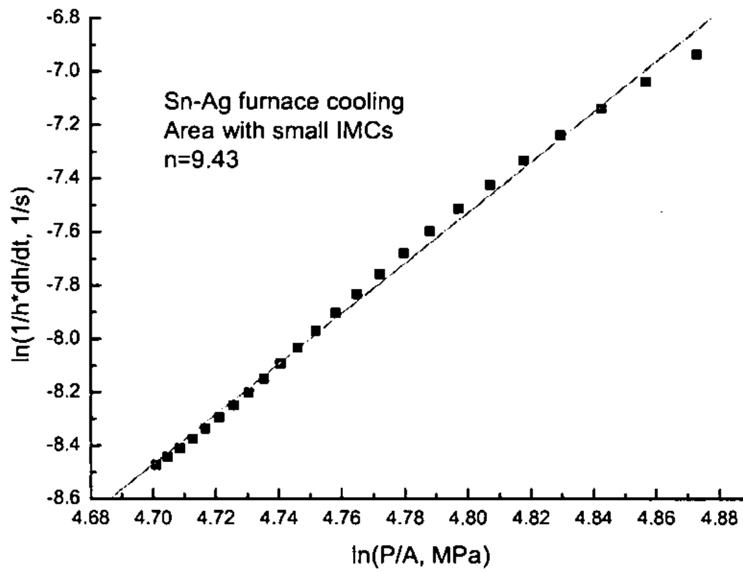


Fig. 6-87 Creep exponent of Sn-Ag solder cooled in furnace.

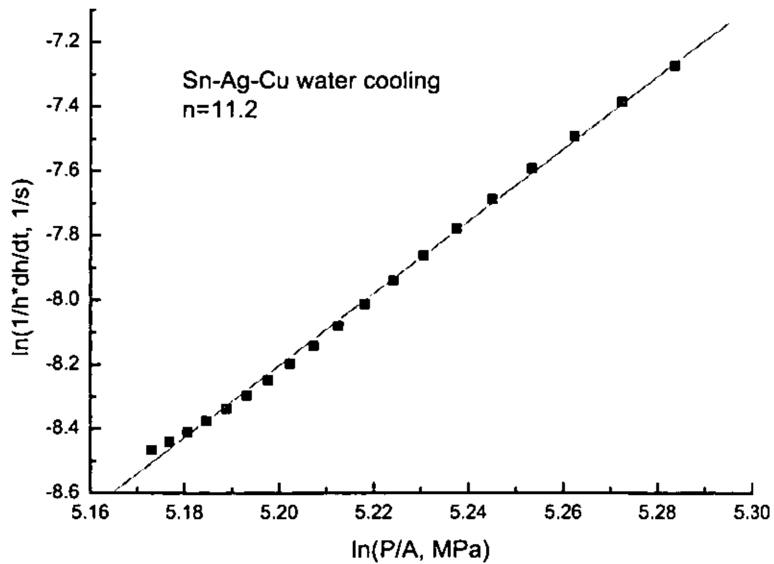


Fig. 6-88 Creep exponent of Sn-Ag-Cu solder cooled in water.

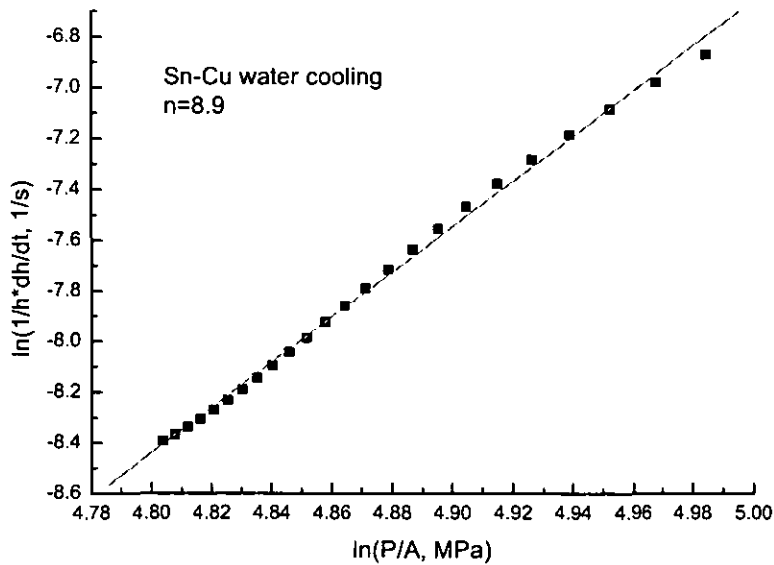


Fig. 6-89 Creep exponent of Sn-Cu solder cooled in water.

Table 6-11 Creep rate of lead free solders with different cooling media.

Sample		Creep exponent (n)
Sn-Ag solder furnace cooling	Small IMC area	9.43
	No IMC area	7.5
Sn-Ag solder air cooling		7.5
Sn-Ag solder water cooling		7.3
Sn-Ag-Cu solder furnace cooling		9.5
Sn-Ag-Cu solder water cooling		11.3
Sn-Cu solder furnace cooling		10.4
Sn-Cu solder water cooling		8.9

6.7 Shear strength of ASH solder bumps after thermal ageing

Electronic components may suffer shear stress due to large CTE differences and/or external forces. As such, the shear strength of solder joints is important for the lifetime of components. Fig. 6-90 shows the shear force of ASH solder bumps after ageing at 80°C for different periods of time. It can be seen that when the shear height was 15 μm,

during the early stages the shear force almost remained the same and only after the solder bumps were aged for 18 d did the shear force decrease gently.

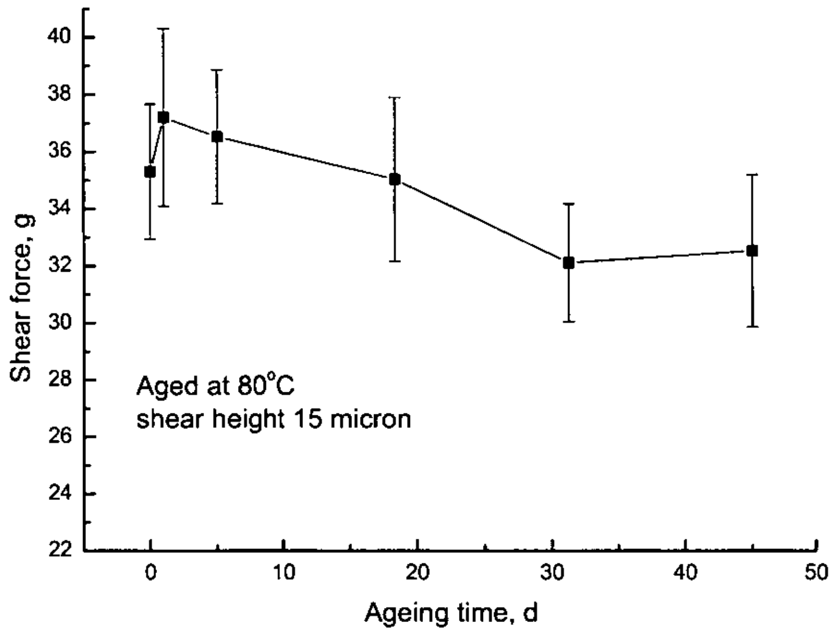


Fig. 6-90 Shear force of ASH bumps after ageing at 80°C for different periods of time.

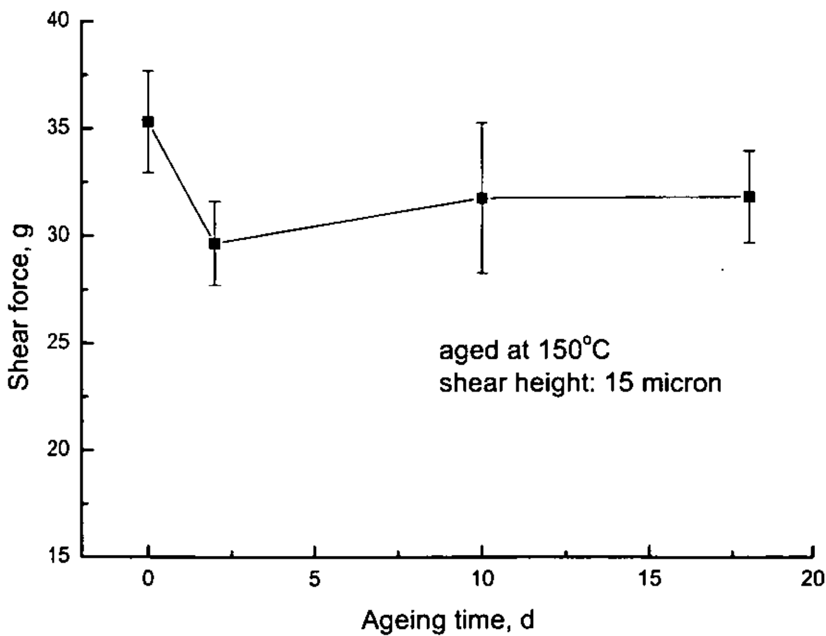
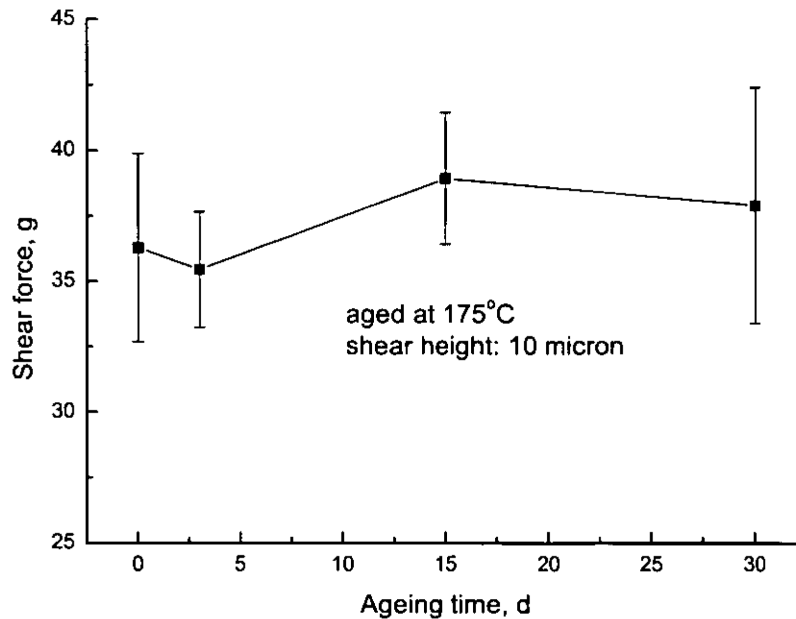
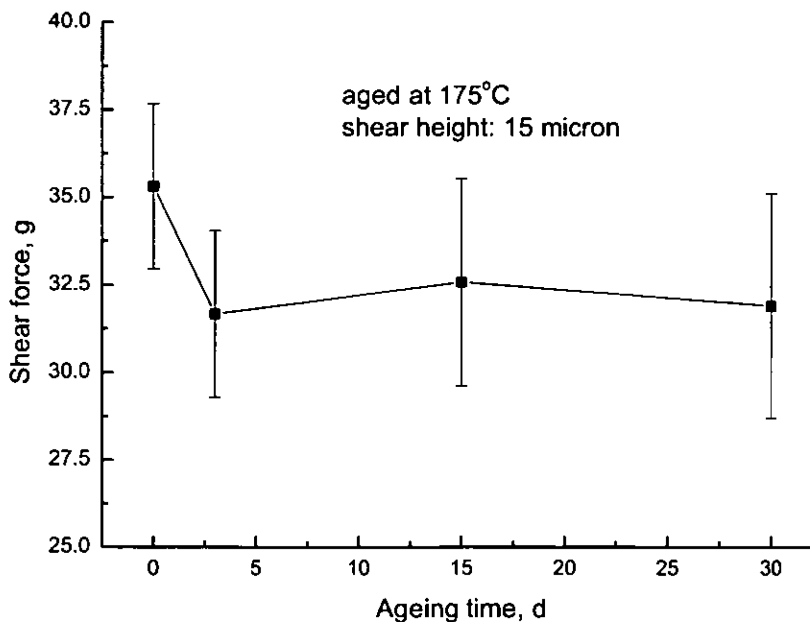


Fig. 6-91 Shear force of ASH bumps after ageing at 150°C for different periods of time.

Fig. 6-91 shows the shear force of ASH solder bumps after ageing at 150°C for different periods of time. It can be seen that the shear force of the solder bumps dropped during the first stage of ageing, about 2 d, and then the shear force almost kept the same during further ageing.



a)



b)

Fig. 6-92 Shear force of ASH bumps after ageing at 175°C for different periods of time.

Fig. 6-92a and b show the shear force of ASH solder bumps after ageing at 175°C for different periods of time, when the shear height was 10 and 15 μm, respectively. It can be seen that when the shear height was 10μm, the shear force did not change during ageing up to 30 d. However, when the shear height was 15 μm, the shear force dropped in the first 3 d's ageing and kept stable during further ageing.

6.8 Reliability

Reliability is a major concern with electronic components. In order to study the reliability of Sn-Ag-Cu solder joints, thermal cycling was conducted on devices comprising flip chips assembled on PCBs. The Cu pads on the PCB had an immersion Au finish but with different physical constructions, i.e., bare pads, pads with solder masks and pads with a micro-via, and the UBM used in the chips was EN without immersion Au.

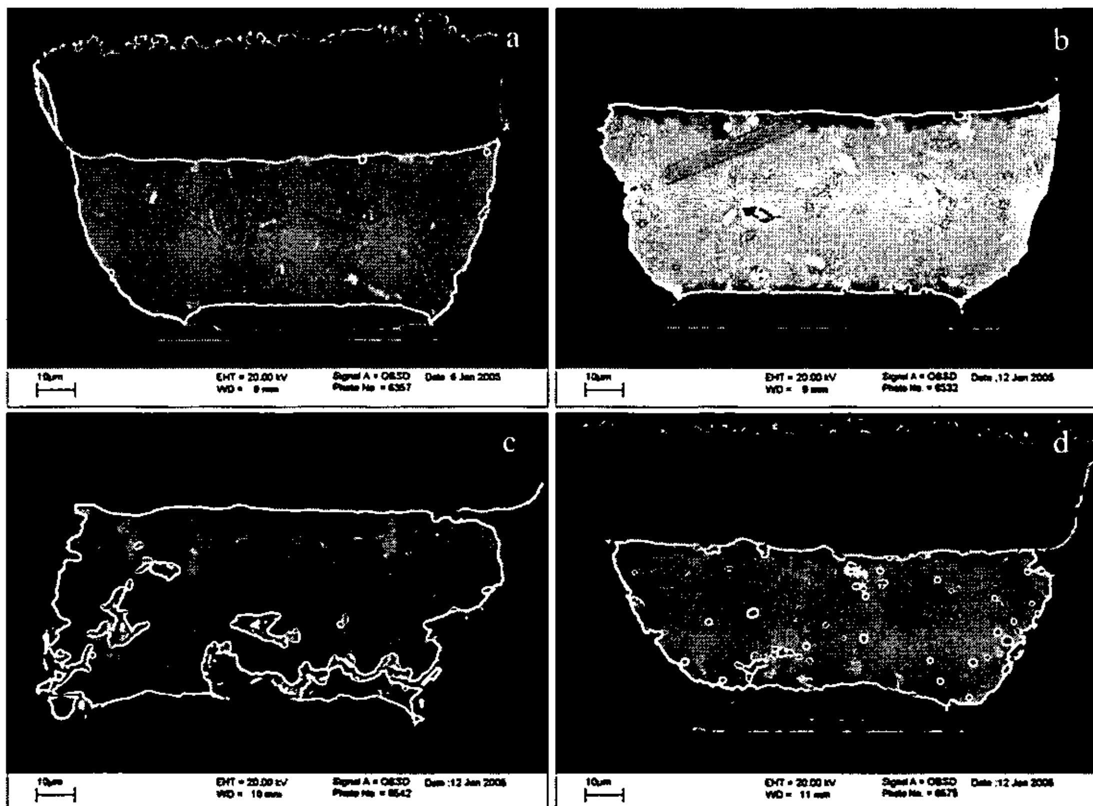


Fig. 6-93 Microstructure of solder joints (pads with solder mask in the PCB side) after thermal cycling, a) 100 cycles, b) 500 cycles, c) 1000 cycles, and d) 1500 cycles.

Fig. 6-93 shows the microstructures of solder joints on the pads with solder masks after thermal cycling for different cycles. In such a case, the alignment of chips with the PCB was good. Cu_6Sn_5 IMCs formed at the solder/pad interface and $(Cu,Ni)_6Sn_5$ IMCs formed at the solder/UBM interface. $AuSn_4$ IMCs were found in the bulk solder and near the interfaces. Small Ag_3Sn IMCs were distributed in the solder joints and some large plate-like Ag_3Sn formed in the solder. It can also be seen that after long period of cycling some cracks existed in the solder joints (Fig. 6-93c and d).

Fig. 6-94 shows the microstructures of solder joints on the bare pads after thermal cycling for different cycles. It can be seen that when the bare pads were used, alignment of chips with the PCB could be a problem. The IMCs formed in the solder joints were similar to those formed in the solder joints formed on the pads with solder masks. It was interesting that in these solder joints even after 1500 cycles no evident cracks were found.

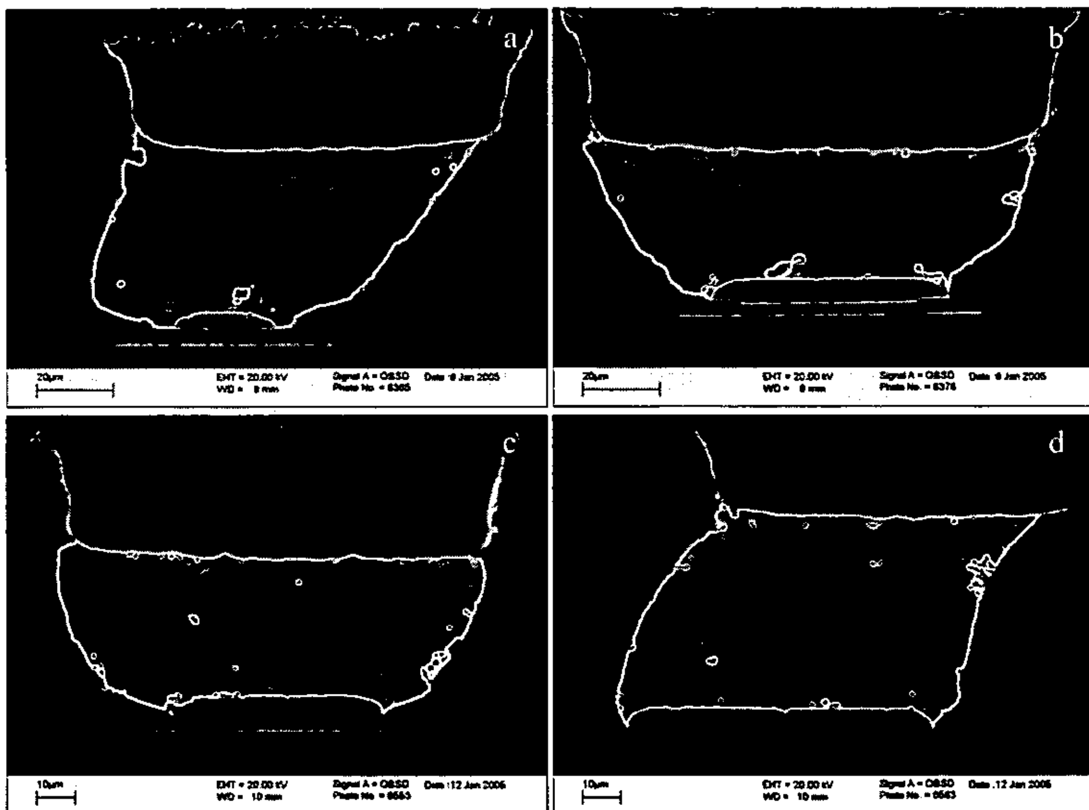


Fig. 6-94 Microstructure of solder joints (bare pads in the PCB side) after thermal cycling, a) 100 cycles, b) 500 cycles, c) 1000 cycles, and d) 1500 cycles.

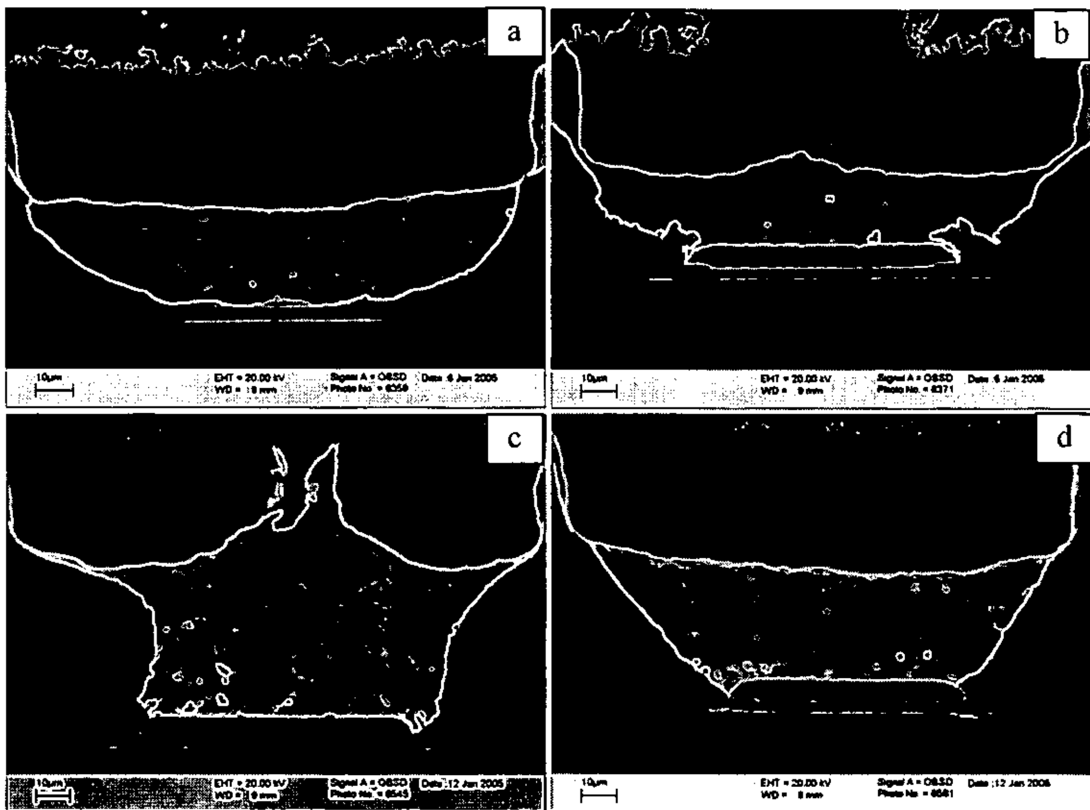


Fig. 6-95 Microstructure of solder joints (pads with micro-via in the PCB side) after thermal cycling, a) 100 cycles, b) 500 cycles, c) 1000 cycles, and d) 1500 cycles.

Fig. 6-95 shows the microstructures of solder joints on the pads with a micro-via after thermal cycling for different cycles. When the pads had a micro-via in them, the solder volume would not be sufficient, resulting in a low joint height or irregular shape. Because the pad with the micro-vias had a larger surface area, more immersion Au existed in this region. In the mean time, the micro-via in the pads would consume more solder. Therefore, the immersion Au to solder ratio in these joints with micro-vias became much higher compared to the joints without micro-vias, leading to the formation of large amounts of $AuSn_4$ IMC, which can be seen from Fig. 6-95. Because $AuSn_4$ IMCs are brittle, the formation of large amount of $AuSn_4$ can be detrimental to the mechanical properties of solder joints.

Table 6-12 Number of couples failed after different cycles for different type of pads.

	Couples failed after different cycles								
	50	100	200	300	400	500	750	1000	1500
Bare pads	0/40	0/40	0/36	0/36	0/36	0/36	0/32	0/32	0/28
Pads with micro-via	0/50	0/50	1/46	2/46	7/46	11/46	10/38	22/38	22/30
Pads with solder mask	0/25	1/25	2/23	2/23	4/23	4/23	5/19	5/19	3/15

Failure condition: electrical resistance increases 30%.

One testing couple includes two solder joints.

Table 6-13 Cycles when 1% and 50% couples failed for different type of pads.

	Cycles to 1% failure	Cycles to 50% failure
Bare pads	> 1500	> 1500
Pads with micro-via	200	1000
Pads with solder mask	400	> 1500

Table 6-12 shows the number of couples failed after different number of cycles among those tested. Once the electrical resistance of a couple increased 30%, this couple was considered to have failed. It can be seen that after 1500 cycles no couples with bare pads failed. However, after only 100 cycles and 200 cycles, some couples with solder masks and micro-vias began to fail, respectively. The solder joints with micro-vias showed the poorest reliability with more than half of the couples failed after 1000 cycles. It was interesting that the reliability of solder joints with a solder mask was poorer than that of solder joints with bare pads. Table 6-13 summaries the cycles to failure of these solder joints.

6.9 Corrosion properties

6.9.1 Potentiodynamic polarization curves

Potentiodynamic polarization testing is a method that can be used to study the corrosion properties of materials. Fig. 6-96 shows the potentiodynamic polarization curves of Sn-Ag solder in 3.5% NaCl solution with different scanning rates. When the scanning rates

were 60 and 300 mV/min, the corrosion potential of Sn-Ag in the salt solution was about -750 mV, and when the scanning rate was 30 mV/min, the corrosion potential was about -700 mV. During the potentiodynamic polarization, the samples started from cathodic polarization, then reached the corrosion potential and began the anodic polarization. When the samples reached the passivation potential, they began to form a passivation film on the surface, and the current density at this point is called the critical current density. After this point the corrosion current density began to drop. When a compact passivation film was formed on the surface, the corrosion current density became stable and this current density is called passivation current density. At this point the corrosion would remain at the same level and potential of the samples increased continually until the potential reached the breakdown potential. Then the passivation film began to break and lost its protection to the materials underneath, resulting in an increase of corrosion current density. The results show that when the scanning rates were 30 and 60 mV/min, the samples could reach the stable passivation state and the passivation current density was about 0.49 and 1.58 mA/cm^2, respectively and that, when the scanning rate was 300 mV/min the passivation film on the samples was broken before it could reach the stable state, such that no stable passivation stage can be found on the curve.

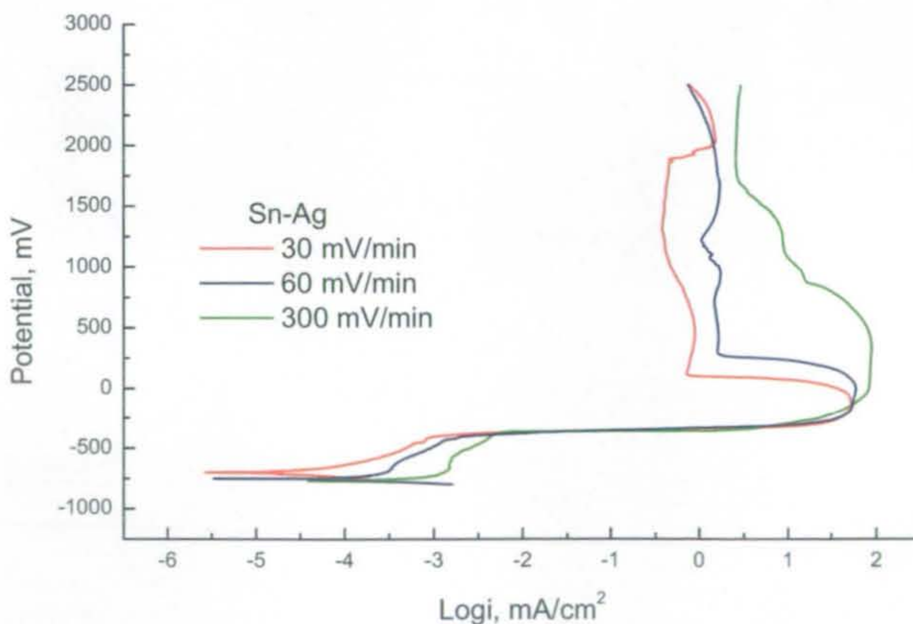


Fig. 6-96 Potentiodynamic polarization curves of Sn-Ag solder in salt solution.

Fig. 6-97 shows the potentiodynamic polarization curves of Sn-Ag-Cu solder in salt solution with different scanning rates. When the scanning rate was 30 mV/min, the corrosion potential and passivation current density were -720 mV and 1.07 mA/cm^2, respectively, and when the scanning rate was 60 mV/min, the corrosion potential and passivation current density were -760 mV and 2.24 mA/cm^2, respectively, and when the scanning rate was 300 mV/min the samples could not reach the stable passivation stage.

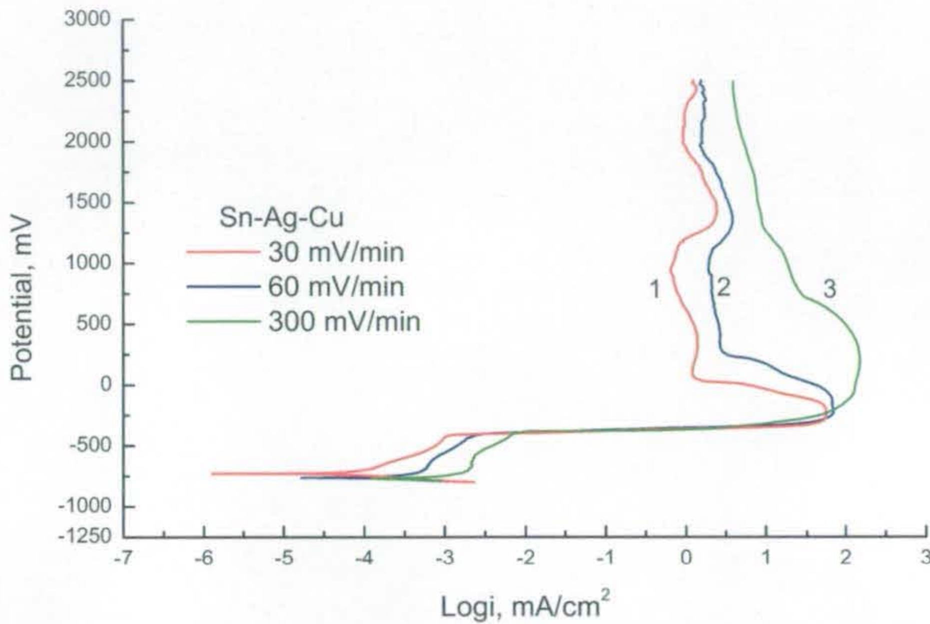


Fig. 6-97 Potentiodynamic polarization curves of Sn-Ag-Cu solder in salt solution.

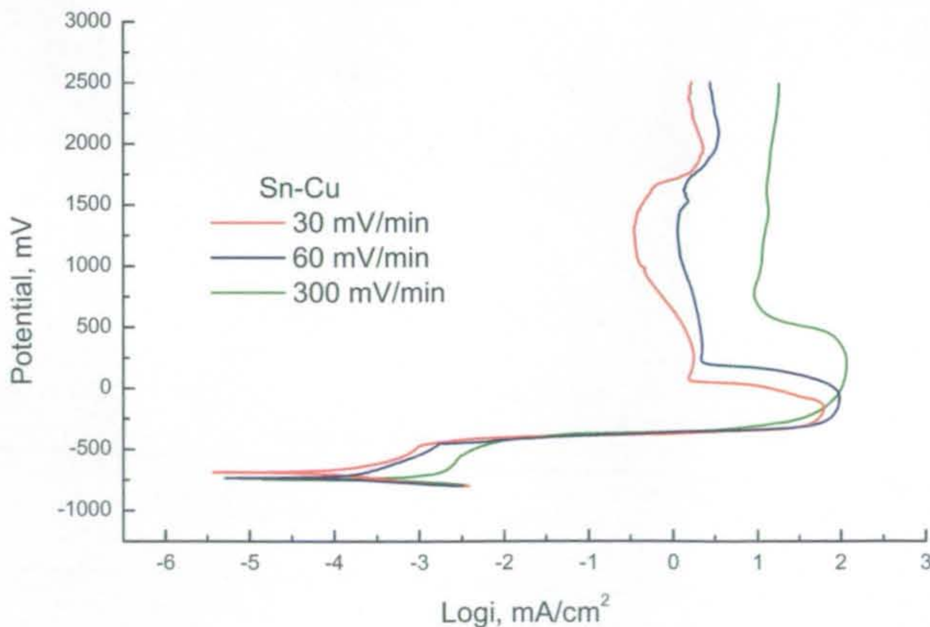


Fig. 6-98 Potentiodynamic polarization curves of Sn-Cu solder in salt solution.

Fig. 6-98 shows the potentiodynamic polarization curves of Sn-Cu solder in salt solution with different scanning rates. When the scanning rate was 30 mV/min, the corrosion potential and passivation current density were -690 mV and 0.74 mA/cm^2, respectively, and when the scanning rate was 60 mV/min, the corrosion potential and passivation current density were -730 mV and 1.62 mA/cm^2, respectively, and when the scanning rate was 300 mV/min the samples could not reach the stable passivation stage.

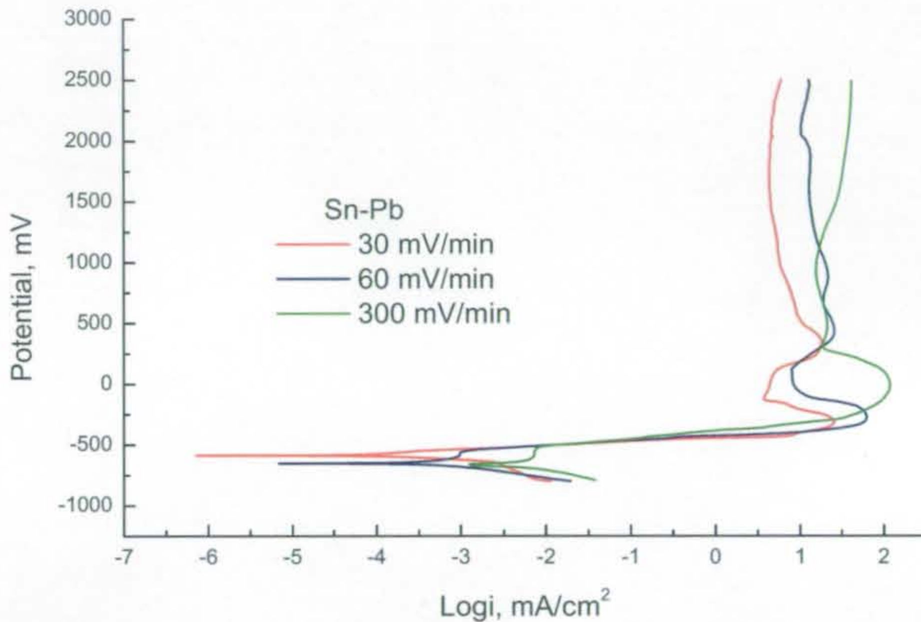


Fig. 6-99 Potentiodynamic polarization curves of Sn-Pb solder in salt solution.

Fig. 6-99 shows the potentiodynamic polarization curves of Sn-Pb solder in salt solution with different scanning rates. When the scanning rate was 30 mV/min, the corrosion potential and passivation current density were -590 mV and 4.17 mA/cm^2, respectively, and when the scanning rate was 60 mV/min, the corrosion potential and passivation current density were -650 mV and 8.10 mA/cm^2, respectively, and when the scanning rate was 300 mV/min the samples could not reach the stable passivation stage.

The corrosion of a material consists of many processes, such as mass transition and electromigration. Corrosion can only reach the equilibrium state after all the processes reach equilibrium. Since corrosion of a material normally happens in an equilibrium state, and only the reactions in this state represent the corrosion resistance, then during potentiodynamic polarization tests the scanning rate needs to be slow enough to ensure the reactions can reach the equilibrium state. Figs. 6-96 to 6-99 show that when the scanning rate was 30 mV/min and 60mV/min the polarization curves were quite close.

It seems that for these testing regimes, when the scanning rate was 30 mV/min, the polarizations were in a near-equilibrium state.

Fig. 6-100 Microstructure of the corrosion products on Sn-Ag solder after the test with scanning rate 30 mV/min.

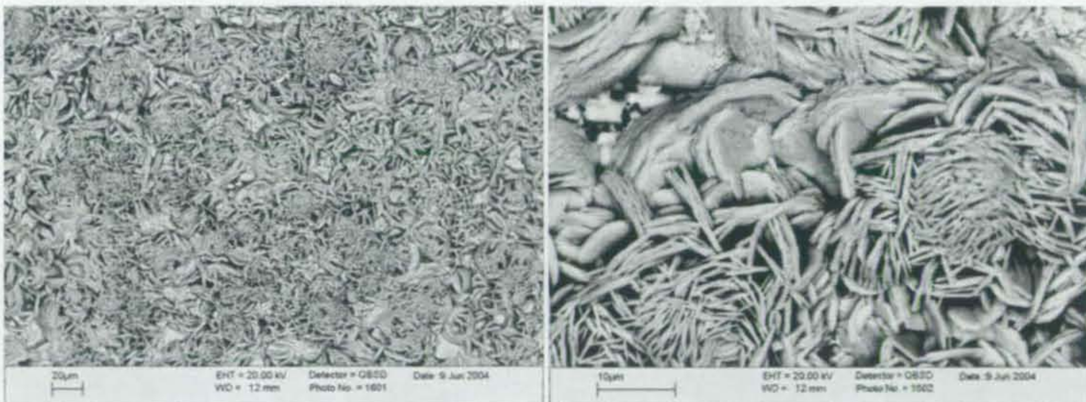


Fig. 6-101 Microstructure of the corrosion products on Sn-Ag solder after the test with scanning rate 300 mV/min.

Fig. 6-102 Microstructure of the corrosion products on Sn-Ag-Cu solder after the test with scanning rate 30 mV/min.

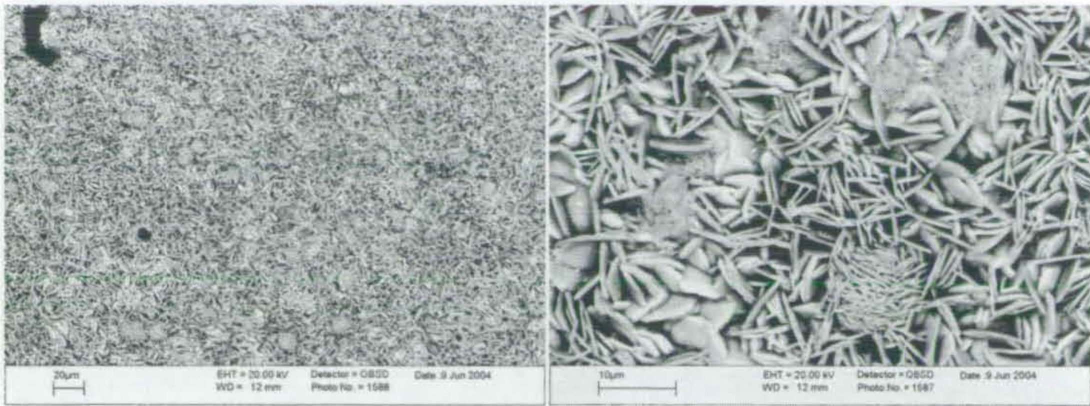


Fig. 6-103 Microstructure of the corrosion products on Sn-Ag-Cu solder after the test with scanning rate 300 mV/min.

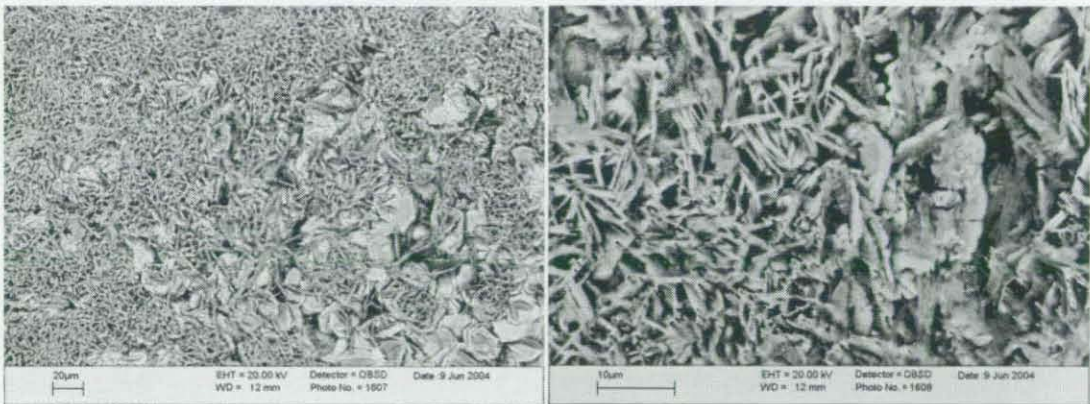


Fig. 6-104 Microstructure of the corrosion products on Sn-Cu solder after the test with scanning rate 30 mV/min.

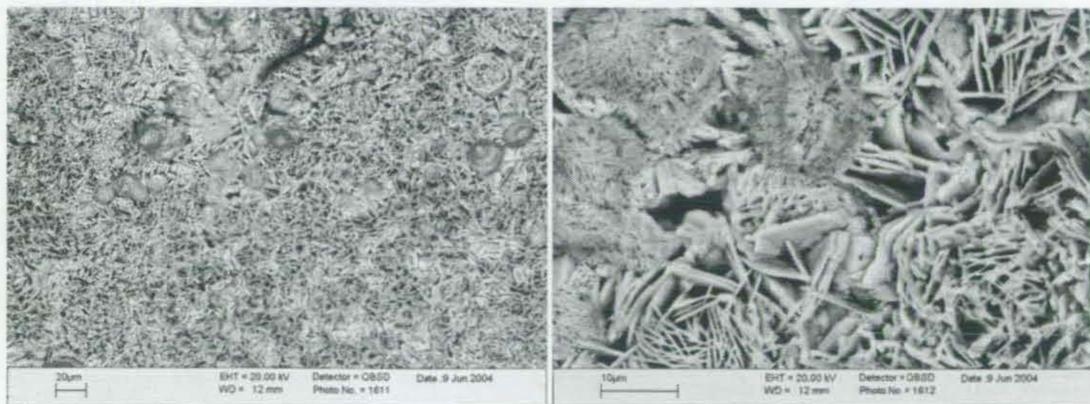


Fig. 6-105 Microstructure of the corrosion products on Sn-Cu solder after the test with scanning rate 300 mV/min.

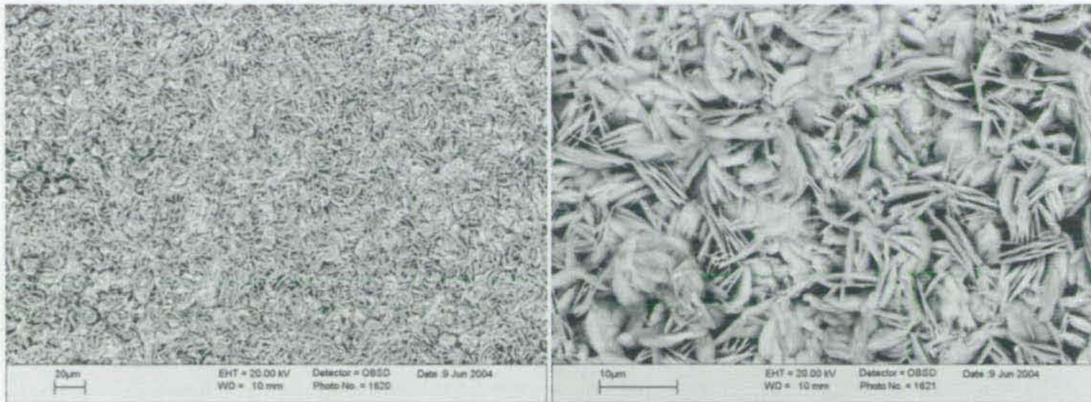


Fig. 6-106 Microstructure of the corrosion products on Sn-Pb solder after the test with scanning rate 60 mV/min.

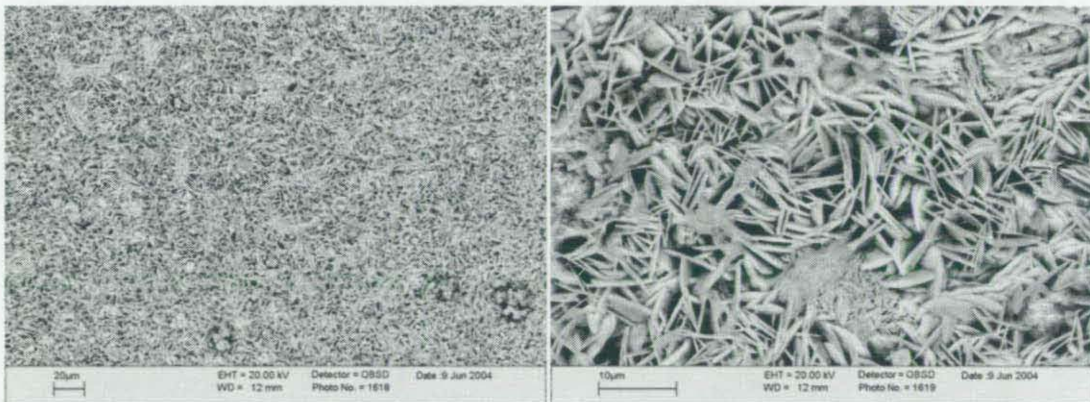


Fig. 6-107 Microstructure of the corrosion products on Sn-Pb solder after the test with scanning rate 300 mV/min.

6.9.2 Microstructures of corrosion products

Figs. 6-100 to 6-107 show the microstructures of corrosion products on different solder materials after the potentiodynamic polarization testing with different scanning rates. The results show that the corrosion products of Sn-3.8Ag-0.7Cu, Sn-3.5Ag, Sn-0.7Cu and Sn-37Pb had similar microstructures. The corrosion products had a platelet-like shape and were loosely distributed on the surface with different orientations. It can also be seen that when the test was conducted with lower scanning rate, the size of the corrosion products was a little larger and that the corrosion products arising with lead free solders were larger than those of Sn-Pb solder.

CHAPTER 7

Discussion of Results

The purpose of this research is to contribute to the knowledge for the successful application of lead free solders in flip-chip scale packages. A series of experiments have been presented up to Chapter 6, with their results consolidated into this discussion chapter.

7.1 Wettability of electroless Ni with lead free solders

The wettability of EN coatings depends on many factors. In this section, the influences of flux, wetting environment, storage and roughness are considered.

7.1.1 Influence of flux and wetting environment

One function of flux is to remove the oxidation, or other films, that may be present on the surface of a material and hence expose a fresh surface to the reacting liquid. The flux can also change the wetting environment and thereby the interacting surface energies at the wetting front and the solid-liquid contact angle. The role of flux is very important for the wettability of electroless Ni (EN) coating, because the EN coating can readily form a surface oxidation layer, which has a poor wetting ability with solder materials. Sattiraju et al. [80] studied the influence of surface finishes and fluxes on the wettability of lead free solders and the results showed that water soluble flux yielded better wettability than the non-clean flux and that, the wettability of Sn-3.5Ag was a little better than that of Sn-3.8Ag-0.7Cu and Sn-0.7Cu. Elbert et al. [81] showed that

nitrogen protection could reduce the formation of dross and decrease the soldering temperature.

Figs. 7-1 and 7-2 show the wetting curves of an as-plated EN coating with Sn-Ag-Cu and Sn-Cu solders when different fluxes and wetting environments were used, respectively. Different fluxes were used during the tests, these being Multicore ACTIEC 5 (rosin strongly activated, strong), ACTIEC 2 (rosin mildly activated, mild) and SM/NA (non-activated, weak). When nitrogen was used to provide inert soldering environment, the concentration of oxygen was about 210 ppm. If the time when the wetting force reaches zero again is defined as 'time to wet', which indicates wetting speed, the results show that when the strong flux was used the wetting had large maximum wetting forces and needed a short time to wet, but when the weak flux was used the solders either needed long time to wet the EN coating and had a small maximum wetting force or could not wet the surface on the whole. When the mild flux was used the maximum wetting force was smaller and time to wet was longer than those when strong flux was used. In the mean time, it can be seen that the nitrogen can increase the wettability, i.e., increasing the maximum wetting force and shortening the time to wet.

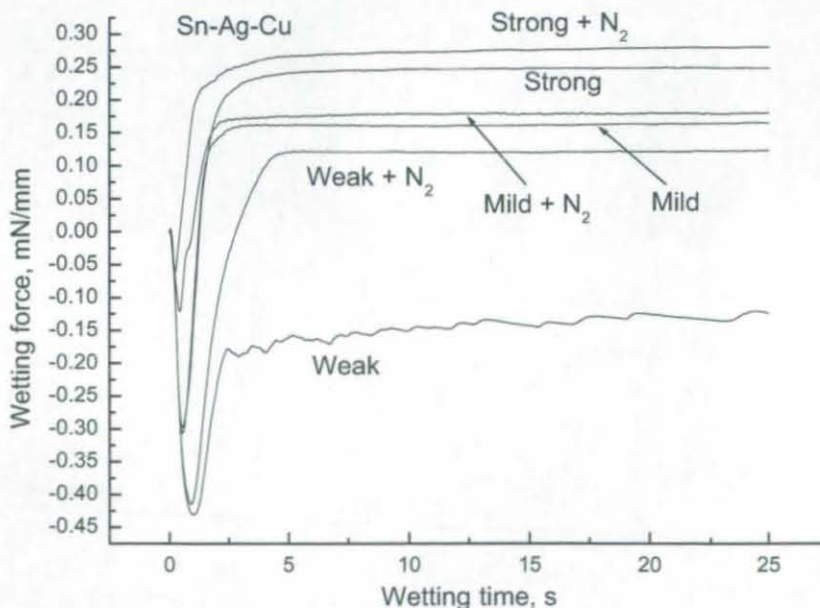


Fig. 7-1 Wetting curves of EN coating in Sn-Ag-Cu solder with different fluxes and wetting environment.

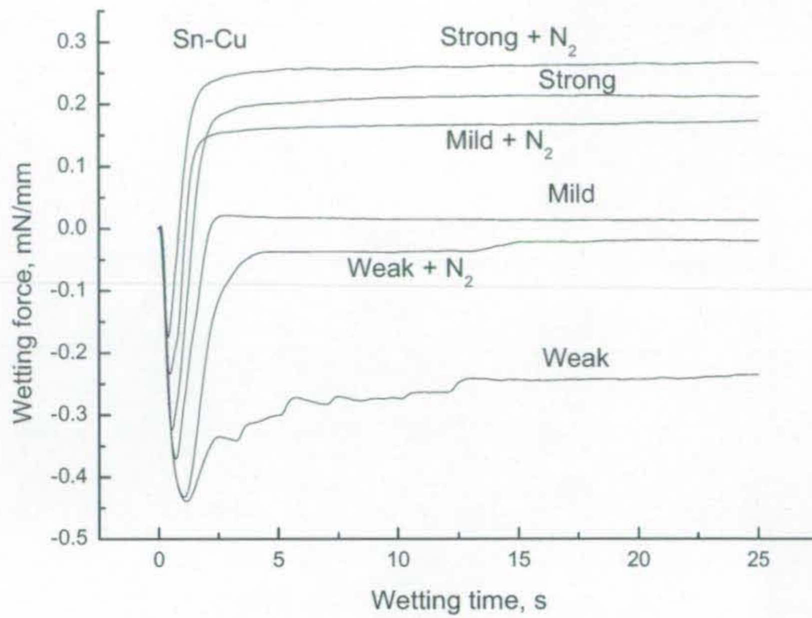


Fig. 7-2 Wetting curves of EN coating in Sn-Cu solder with different fluxes and wetting environment.

Fig. 7-3 EN plated samples after the wettability tests in Sn-Ag-Cu and Sn-Cu solders.

Fig. 7-3 shows EN plated samples after wettability tests with Sn-Ag-Cu and Sn-Cu solders when different fluxes and wetting environments were used. It can be seen that when the flux was not strong enough or, when no nitrogen was used, there were some non-wetted or poorly-wetted points remaining on the surface. Based on the wetting curves and the wetting results, it can be seen that a strong flux and nitrogen protection are needed for Sn-Ag-Cu and Sn-Cu solders to ensure the EN coating to perform good wettability.

7.1.2 Influence of oxygen concentration

As mentioned in Section 7.1.1, nitrogen protection can increase the wettability of EN coating. When nitrogen flows into a chamber, the oxygen concentration is reduced. In order to know which oxygen concentration level is acceptable to improve wettability, the influence of nitrogen flow on the wettability was studied. Fig. 7-4 shows the maximum wetting force and time to wet of an EN coating in Sn-Ag-Cu solder with different nitrogen flows. It shows that when the nitrogen flow increases, i.e., the oxygen concentration decreases, the maximum wetting force will increase and the time to wet will decrease. It seems that the wettability of EN coatings changes greatly with the N_2 flows when the O_2 concentration in the wetting environment getting lower (e.g. less than 400 ppm according to Fig. 6-3). Fig. 7-5 shows the maximum wetting force and time to wet of EN coatings in Sn-Ag solder with different nitrogen flows. It can be seen that the influence of nitrogen flow on the wettability of EN coating with Sn-Ag solder was similar to that with Sn-Ag-Cu solder. Fig. 7-6 shows the maximum wetting force and time to wet of EN coatings in Sn-Cu solder with different nitrogen flows. It seems that small amounts of nitrogen can greatly increase the wettability of Sn-Cu solder, and when the nitrogen flow was greater than 8 L/min the maximum wetting force and time to wet no longer changed to any significant degree. Considering the change of O_2 concentrations with different N_2 flows (Fig. 6-3), these results show that when Sn-Ag and Sn-Ag-Cu solders are used in soldering packages the O_2 concentration in the wetting environment needs to be lower than 210 ppm and, when Sn-Cu is used the O_2 concentration in the wetting environment can be kept around 400 ppm.

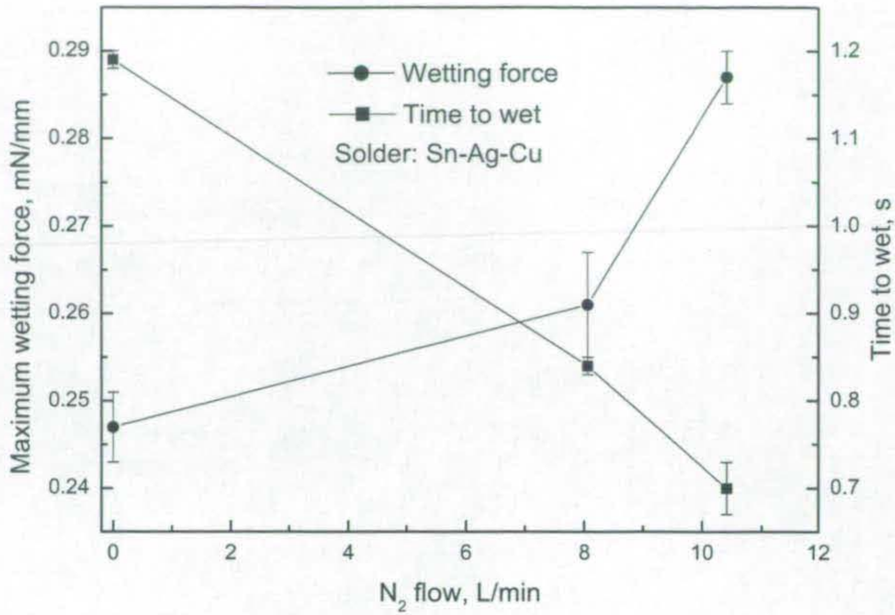


Fig. 7-4 The maximum wetting force and time to wet of EN coating in Sn-Ag-Cu solder with different nitrogen flows.

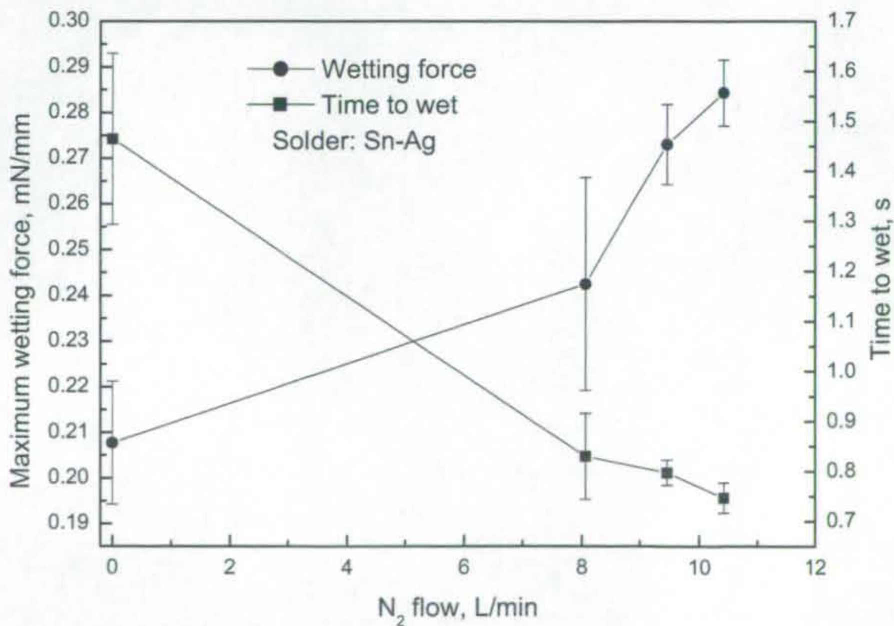


Fig. 7-5 The maximum wetting force and time to wet of EN coating in Sn-Ag solder with different nitrogen flows.

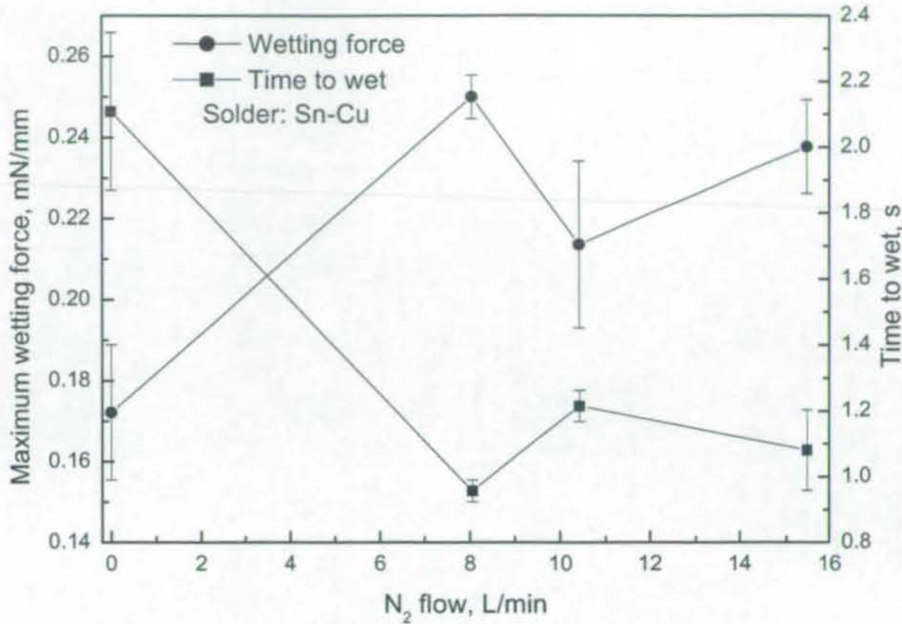


Fig. 7-6 The maximum wetting force and time to wet of EN coating in Sn-Cu solder with different nitrogen flows.

7.1.3 Influence of storage

The influence of storage on the wettability of EN coating with lead free solders was studied to derive some criteria for industrial applications. From Fig. 6-4 to 6-9, it can be seen that although the wettability of EN coating had some deviation due to the minor difference of the surface condition, both the storage time and environment did not influence the maximum wetting force with Sn-3.5Ag, Sn-0.7Cu and Sn-3.8Ag-0.7Cu solders. It was also seen that when the samples were stored in a freezer, the storage time did not influence the time to wet. However, when the EN plated samples were stored in an ambient environment, the time to wet was increased during storage. It seems that the oxidation film was thicker when the samples were stored in an ambient lab environment and as such needed more time to be removed by strong flux.

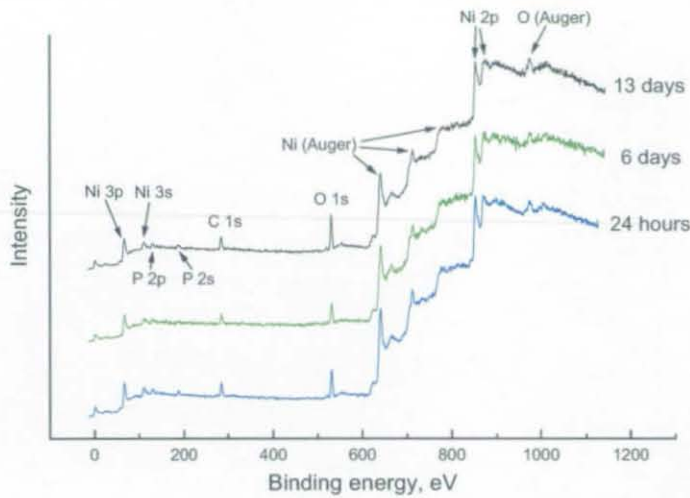


Fig. 7-7 XPS spectra (normalized) of electroless Ni coating after the storage in lab for different periods of time.

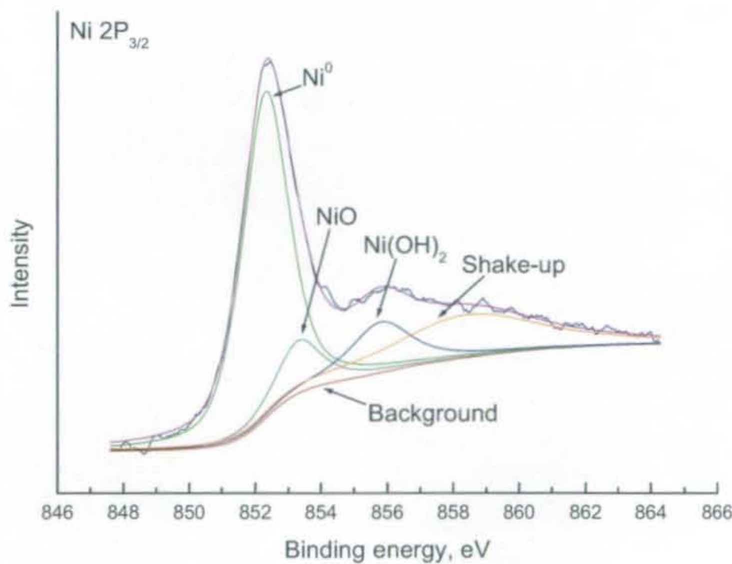


Fig. 7-8 XPS peak of nickel after storage in air for 24 h.

In order to study the influence of storage on the solderability of electroless Ni UBM, the coupons after different storage times in the laboratory were analyzed by XPS. Fig. 7-7 shows the energy spectra of electroless Ni coating with good solderability after different storage times in the laboratory. The peak positions are consistent with each other after different storage regimes, indicating the same compounds formed on the surface. The carbon peaks appear to be contamination on the samples. The Ni $2p_{3/2}$ peak of the electroless Ni coating after the storage in the laboratory for 24 h is shown in Fig. 7-8. This peak was analyzed by an XPS Peak software using a de-convolution procedure.

The result indicates that the nickel in the surface region of the Ni-P coating can exist in the forms of Ni (852.3 eV), NiO (853.3 eV) and $Ni(OH)_2$ (855.8 eV) [82]. However, there may be other nickel species present such as nickel phosphate and phosphite that could contribute to the XPS spectrum [83].

Table 7-1 Composition analyses of electroless Ni coating after different storage by XPS.

	P content (at.%)	O content (at.%)	Atomic ratio	
			O/Ni	P/Ni
Lab 24 h	12.6	28.6	1.57	0.69
Lab 6 d	11.4	30.0	1.61	0.61
Lab 13 d	9.0	34.6	2.18	0.57

Table 7-1 lists the contents of oxygen and phosphorus and content ratios of oxygen:nickel and phosphorus:nickel, as analyzed by XPS. The results show that during storage, the content of oxygen on the surface was gradually increasing and the content of phosphorus decreased with the storage time. This suggests that the surface of the electroless Ni coating oxidised continually as the time of exposure increased. XPS composition analysis seems to show that the content of oxygen on the Ni-P coating surface was much higher than that in pure NiO oxide, which may be attributed to organic contamination, phosphate and phosphite formed on the Ni-P surface [84].

The flux was used to remove the oxide film on the surface of Ni-P coatings. If the original sample has good wettability and the flux can remove the oxide film completely, the oxidised sample after storage will still have good wettability with the assistance of flux. In this study, the surface of electroless Ni coating was oxidised continually during storage, however after storage of several weeks in both environments, it still had acceptable solderability with lead free solders. This indicated that the oxide film on the Ni-P coating surface was not too thick to be removed by strong flux, even after a long period of storage. The results above show that with the assistance of a strong flux, both the storage time and the storage temperature did not influence the solderability significantly.

EDX and XPS are two kinds of methods that can be used to analyze surface composition of materials. The analysis depth of EDX is much higher than that of XPS,

so the result from XPS analysis better reflects the surface composition. Analysis from EDX showed that the average phosphorus to nickel ratios (at.%) was 0.149, which is much lower than that from XPS analyses as shown in Table 7-1. This means that the phosphorus content on the surface is much higher than that in the bulk Ni-P coating after it is oxidised. Zhang et al [83] studied the characteristics of Ni-P coatings by ToF-SIMS and XPS, and the results showed that the Ni-P coating was oxidised and the oxidised surface had two layers, with the nickel oxide and hydroxide on the top and nickel phosphate and phosphite (NiH_xPO_y) underneath. Because nickel phosphate and phosphite have high phosphorus content, the phosphorus content on the surface is higher than that in the bulk coating. The high oxygen content in nickel hydroxide, phosphate and phosphite at the same time makes the surface oxygen concentration higher than that expected for NiO.

7.1.4 Influence of substrate roughness

Wenzel [85] studied the effect of surface roughness on wetting and showed that a rougher surface has higher surface energy, resulting in smaller apparent contact angles to the rougher surface if the contact angle is less than 90°. However, the study of Shuttleworth and Bailey [86] predicted that the apparent contact angle would increase with the surface roughness because the local contact line is distorted by the rough surface. Later, Chen et al. [85] solved this discrepancy by regarding the asperities as a series of energy barriers that must be overcome as the liquid front spreads over the surface. Chen et al. considered that the wetting angle was decided not only by the spreading of liquid but also by the interface reactions. The rougher surface could increase the surface energy, but in the mean time posed an energy barrier for spreading. So if the increase of energy from the interface reactions was smaller than the spreading barrier, the apparent contact angle would become larger with increasing of surface roughness.

By treating the rough surface as a region distributed with many grooves, Shuttleworth and Bailey [86] pointed out that the apparent contact angle could be expressed as

$$\theta_r = \theta_0 \pm \alpha_m$$

where θ_r is the apparent contact angle, θ_0 the true contact angle and α_m the groove steepness. They thought that the value of apparent contact angle depended on whether the liquid was advancing or receding on the solid before the static contact angle was reached. From Fig. 7-9, it can be seen that if the liquid was receding the apparent contact angle would be smaller than the true contract angle, otherwise it would be larger than the true contact angle. For a natural wetting process, the liquid is advancing along the surface; the receding can only happen when the liquid is spread on the solid by some mechanical means and the true contact angle is smaller than the equilibrium contact angle.

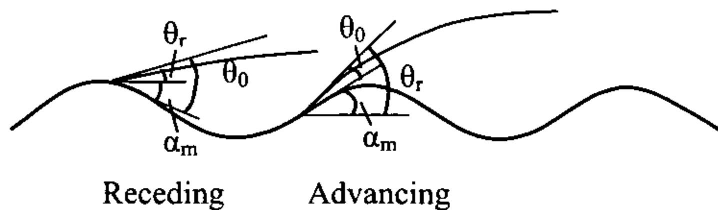


Fig. 7- 9 The relationship between apparent contact angle and true contact angle on a rough surface.

Fig. 6-11 and 6-12 show that when the dipping direction was in the A direction (dipping direction perpendicular to the polishing or rolling tracks) the wetting force of an EN coating increased a little with the decrease in surface roughness and that, the maximum wetting force of an EN coating in the B direction (dipping direction parallel to the polishing or rolling tracks) was higher than that in the A direction. For the wetting in the B direction, the liquid spreads along the grooves and does not need to pass the energy barrier, so the surface energy will determine the wetting behaviour and the maximum wetting force in the B direction is higher than that in the A direction. Since the maximum wetting force of a surface with different roughness in the B direction does not have great difference, it seems that the influence of surface energy on the wetting due to the rough surface is not significant. On the other hand, because the spread-energy barrier to the rougher surface is higher, it is more difficult for the liquid to spread on the rougher surface and consequently the contact angle will increase. When considering this issue from the viewpoint of the apparent contact angle, the same conclusion can also be drawn. Because the liquid is advancing on the solid during wetting, the apparent contact angle on a rough surface in the A direction is larger than the true contact angle (the

apparent contact angle on a smooth surface). Since the wetting force is caused by the surface tension γ and related to $\gamma \cdot cos\theta_r$, the maximum wetting force will decrease with the increase of surface roughness in the A direction. Fig. 6-11 and 6-12 show that for the EN coating on the original Al substrate, the maximum wetting forces in the A and B directions were similar. This is because the steepness of grooves on a surface with low roughness is very small and the difference between the apparent contact angle and the true contact angle is not significant.

7.2 Microstructure of lead free solders

7.2.1 Influence of cooling media

Cooling rate during solidification can influence the microstructure of solder materials, which in turn will influence the properties of solder joints. The microstructures of both the ASH solder bumps and bulk solders solidified by water quenching, air cooling and furnace cooling were studied. The results from Ochoa et al. [87] showed that the cooling rates of bulk solder from water quenching, air cooling and furnace cooling were about 24°C/s, 0.5°C/s and 0.08°C/s, respectively. In this study, the cooling rate when the bulk samples were cooled down in a furnace was tested and shown in Fig. 7-10. The rate 0.01°C/s seems much slower than that Ochoa et al. tested. For the small solder joints, the cooling rate should be much faster than that for bulk solder due to their small size.

From Figs. 6-16 to 6-18, it can be seen that the Ag_3Sn IMCs in solder joints with different cooling media had different sizes, with the order being: furnace cooling > air cooling > water cooling. However, this influence of cooling media on the IMC size was not significant for the small Ag_3Sn IMC particles. It is not clear what influence the cooling media had on the size of large plate-like Ag_3Sn phases, because they were not encountered in the cross-sections of the solder bumps. For the bulk solders, Figs. 6-19 to 6-27 show that the IMCs formed in the samples cooled in a furnace were much larger than those formed in the samples cooled in water. It seems that the influence of cooling media on the IMC size in the bulk samples is larger than that in small solder joints, and this is caused by the size difference between these two kinds of samples. Since the size

of solder joints is very small, the cooling rate may be already very fast in the furnace cooling case and their cooling rate in different cooling media has no great difference.

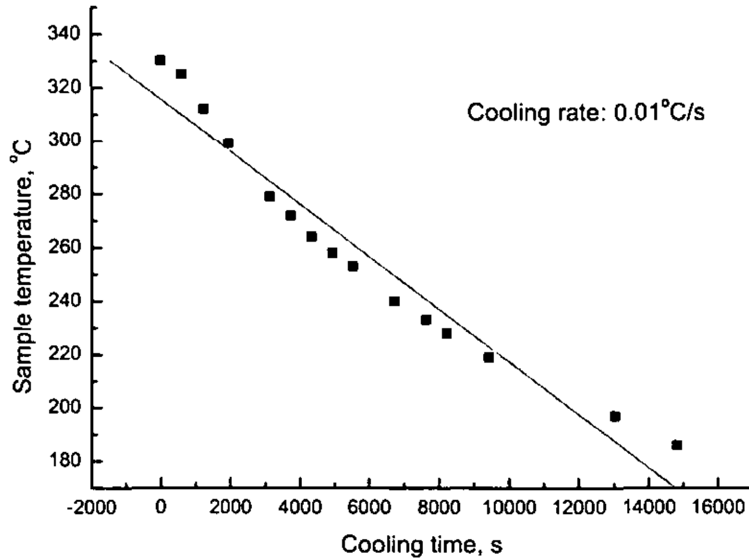


Fig. 7-10 Cooling rate of samples cooled down in furnace.

Kim et al. [88] and Ochoa et al. [87] studied the effects of cooling speed on the microstructure of Sn-3.5Ag-0.7Cu and Sn-3.5Ag solders, respectively. The sizes of IMCs in this study were larger than those in their studies, and this can be explained by the different cooling rates and different maximum temperatures of melted solders. The Sn-Ag solder in the study of Ochoa et al. was cooled in furnace, air and water as well, but their cooling rates were faster than those used in this research, and the cooling speeds of Sn-Ag-Cu samples in the study of Kim et al. were 0.012°C/s, 0.43°C/s and 8.3°C/s, respectively. Another difference is the maximum temperatures of molten solders. In this study, the solders were melted to 330°C for half an hour and then cooled in different media; however, in the study of Kim et al. the samples were melted at 300°C for 1 h, and in the study of Ochoa the samples were melted at 240°C for only 20 s. Since the samples were cooled unevenly, i.e., the outer part of the samples will cool more quickly than the inner part, a temperature gradient within the bulk samples was inevitable, and the higher the maximum temperature of molten solders the greater the temperature gradient. Because the outer part of samples cools very quickly, it reaches the solidification point, and the IMCs solidify and grow from this region first. A larger temperature gradient will cause longer solidification time, i.e., the IMCs have longer

time to grow when the maximum temperature of molten solders is higher, resulting in a larger size of IMCs. The influence of maximum temperatures of molten solders was relatively insignificant for the small solder joints because a large temperature gradient could not be set during solidification due to the small size.

7.2.2 Morphology and distribution of IMCs in Sn-Ag-Cu solder joints

Because the IMCs are harder and more brittle than the bulk solder material, different morphology and distributions of IMCs in the solder joints will have different influences on the mechanical properties. Table 7-2 presents the data for the existing morphologies of Ag_3Sn IMC in ASH bumps. As mentioned in Chapter 6, when the plate-like Ag_3Sn phases are large enough, there will be only a small number of Ag_3Sn particles in other areas. This means that if a cross-section only has a small number of particles, large plate-like Ag_3Sn phases probably exist in the solder bump at other areas. Another observation is that the large plate-like Ag_3Sn in the bottom layer are more abundant than those in the top layer, and it seems that the large plate-like Ag_3Sn tends to form near the solder/$(Cu,Ni)_6Sn_5$ IMC interface. Fig. 7-11 shows the microstructure of a solder bump at different levels. It can be seen that when a cross section showed the microstructure as a small number of Ag_3Sn particles distributed in β-Sn, there could be some plate-like Ag_3Sn IMCs existing towards the lower levels. If we presume there are some large Ag_3Sn IMCs existing in these solder bumps, it can be seen that the large plate-like phase is the most popular morphology of Ag_3Sn IMC and, the other popular microstructure of ASH solder bumps is the small particles and plates existing around the β-Sn dendrites. Although no statistics are presented, from the SEM images the same result can also be seen for the vertical cross-section microstructure.

Table 7-2 Statistic data of the existing morphologies of Ag_3Sn IMC in ASH bumps.

	Small particles and plates	Middle size plates	Mixture of small particles, plates and middle size plates	Large size plates	Small number of particles
Top layer	20/72*	3/72	2/72	21/72*	28/72
Bottom layer	15/67*	2/67	3/67	33/67*	14/67

* 2 and 3 images have both of the morphologies in the top and bottom layers, respectively.

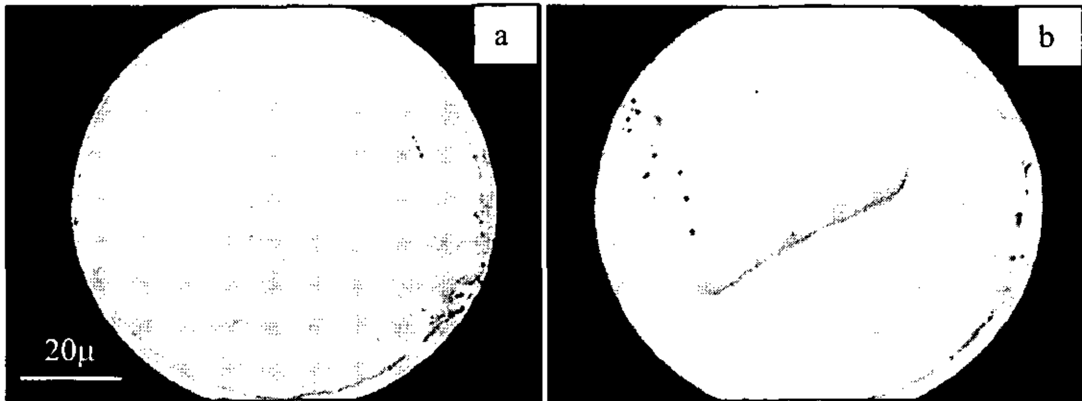


Fig. 7-11 Microstructure of Sn-Ag-Cu a solder bump after cross-sectioned at different level, a) top and b) bottom.

The formation of Ag_3Sn in the solder bumps is complicated because several kinds of morphologies can exist in the same sample. The cooling rate is one of many reasons that could cause this difference in morphology; however, cooling rate cannot alone explain this issue, since for the peripheral array chips, the cooling rate of different solder bumps is very close. During reflow the solder reacts with the UBM and IMCs form at the interface. It is possible that in some solder joints, due to the interfacial reactions the primary Ag_3Sn IMCs prefer to nucleate near the solder/EN interface and grow into large plate-like phases during the subsequent solidification.

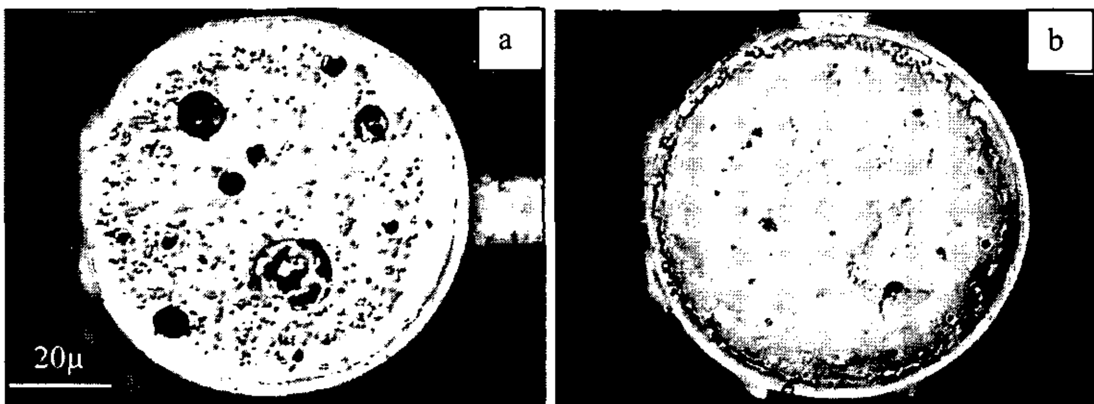


Fig. 7-12 Morphology of $(Cu,Ni)_6Sn_5$ IMCs in a solder bump, a) top layer of IMCs and b) bottom layer of IMCs.

The $(Cu,Ni)_6Sn_5$ IMCs formed in solder bumps had a facet-like shape, which has been presented in Fig. 6-29. Fig. 7-12 shows the morphology of $(Cu,Ni)_6Sn_5$ IMCs in a solder bump from a plan view. It confirms that the $(Cu,Ni)_6Sn_5$ IMC layer had a loose structure at the top and a compact structure in the bottom.

Voids are very easy to form in small solder joints because the small quantity and sluggish property of solder make the escape of bubbles very difficult. Fig. 7-13 shows the voids formed in such solder bumps. It can be seen that the voids tended to form at the solder/EN interface. When there was a large void at the interface, little or no $(Cu,Ni)_6Sn_5$ IMCs would form at these places, because little or no solder was available to react with the EN UBM.

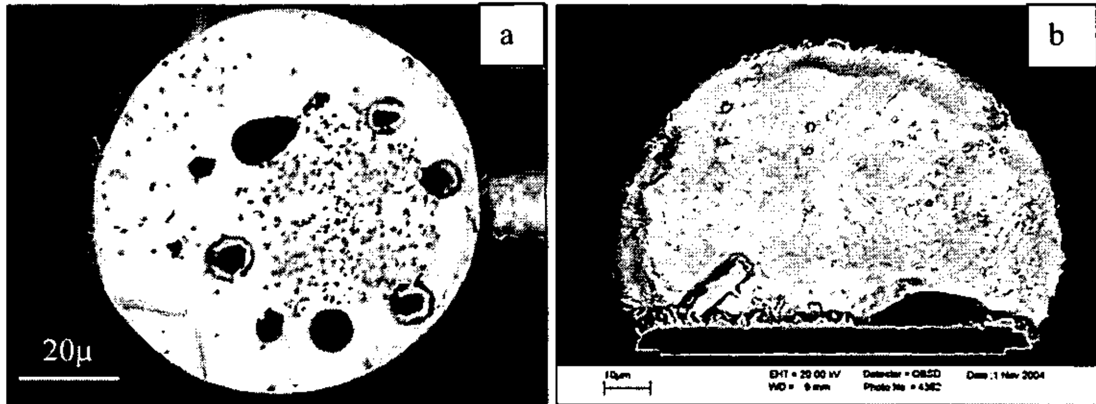


Fig. 7-13 Voids formed in solder bumps near solder/EN interface.

The studies and summaries of Wickham [89] and Biocca [90] showed that there could be many reasons that can cause the void formation during reflow soldering, such as high surface tension, solder shrinkage, surface contaminants, out-gassing and poor reflow profile etc. The technical-sheet of AIM [91] mentioned water-soluble solder pastes were more likely to result in voiding. In this sheet, a new reflow profile called LSP (Long-Soak-Profile) was suggested, which proved to be able to reduce the occurrence of voiding. This LSP profile can dry out the solvent in the solder paste before the reflow zone and is different from the RSS (Ramp-Soak-Spike) and RTS (Ramp-to-Spike) profiles. It is found that increasing the pre-heat time and the top reflow temperature may decrease the voiding. The surface tension of lead free solders is higher than that of eutectic Sn-Pb solder, which can increase the possibility of void formation. During solidification the solder is shrinking, and if the solidification is not even, voids can form in the parts that solidify late. This can happen when the solder is not a eutectic alloy or when the cooling is not even. Out-gassing is the main source of voiding, which can come from the volatilisation of flux and absorbed moisture, surface contaminants, micro-vias in the pads and incomplete cure of solder mask etc.

Yunus et al. [92] studied the effects of voids on the reliability of BGA/CSP solder joints and their results showed that for voids that were larger than 50% of the solder joint area they can cause potential reliability problems, resulting in a 25-50% reduction in service life and for small voids the influence was dependent on the void frequency and location and, if the voids lined up on the component side, they could also significantly reduce the reliability of solder joints. Voids can accelerate the failure of solder joints by reducing the distance that cracks have to propagate, although it is also possible that voids arrest the cracks during their propagation and postpone the growth of cracks. Except for the detrimental effect on reliability, voids can also cause junction temperature distortion of solder joints. The study of Ciampolini [93] showed that the junction temperature distortion peak was proportional to the void area. In order to improve the reliability of solder joints, the formation of voids need to be avoided. From the causes mentioned above, it seems that choosing the right flux and reflow profile and avoiding the out-gassing sources may reduce the formation of voids.

7.3 Interface reactions

During soldering, molten solder comes into contact and reacts with the pad or UBM on the substrate. The nature of this interaction is dependent on the compositions of the solder and how each of the constituents interacts with the pad or UBM. Whether or not the pad is coated can affect the nature of the interaction with the constituents of the solder.

After assembly, electronic devices may work at a relatively high temperature or need rework after failure, so solid-state reactions as well as liquid state reactions can happen in these conditions. Even at room temperature, solid-state reactions can occur. When the solder is in liquid state, e.g. reflow and rework, interfacial reactions can take place easily, and IMCs can nucleate and grow quickly. In solid-state reactions, through diffusion, the solder can react with the pad or UBM materials, so the IMCs will continue growing. Both liquid and solid state reactions can determine the phase constituents and the morphology of solder joints and therefore the mechanical properties and reliability.

There can be a number of IMCs formed at the solder and substrate interface during soldering. However, only the IMC that forms first, during the soldering process, has a significant effect on wetting and solderability. When intermetallic compounds are formed at the solder-substrate interface, the interfacial energy should consequently be lowered, indicating that wetting has taken place, resulting in the reduction of the net free energy at the interface. Both wetting and IMC formation are driven by interfacial energy and during soldering the formation of IMCs, which is required for good wetting, is very important to the adhesion between the solder and the substrate. However, not all wetting of a solid surface by a liquid will result in the formation of IMCs, and excessive amounts of IMCs, especially brittle phases, may degrade the mechanical properties and reliability of the solder joints. Because the pads with a UBM are a multi-layered structure, when one of the layers is depleted, the condition of the interface can be changed, and sometimes the free energy could be higher than the stable state. To lower the free energy of the system, in some conditions the IMCs will de-wet from the substrate.

7.3.1 IMCs formed in the solder bumps

Research has shown that the IMC formed at the interface between Sn-3.8Ag-0.7Cu [54, 55] or Sn-3.5Ag-0.75Cu [94] solder and Au/Ni(P) UBM is $(Ni_xCu_y)_3Sn_4$. Tai et al. [95] also showed that the IMC formed at the interface between Sn-Ag-Cu solder and Au/Ni(P) UBM is Ni_3Sn_4, but they did not mention the composition of the solder material. However, most other research has shown that the IMCs formed at the interface between Sn-Ag-Cu solder (of varying compositions) and Au/Ni [52, 95-105] or Ni(P) [106] UBM were typically Cu_6Sn_5 with a small amount of dissolved Ni and some small Ag_3Sn particles distributed in the solder. The results of Luo et al. [107] showed that the IMCs formed at the interface of Sn-Ag-Cu solder and pure Ni depended on the Cu concentration in the solder material. When the Cu concentration in the solder was not more than 0.2 wt.%, a continuous layer consisting of $(Ni,Cu)_3Sn_4$ formed at the interface. However, when the Cu concentration was more than 0.6 wt.%, the formation of $(Cu,Ni)_6Sn_5$ intermetallic dominated at the interface. If the Cu concentration was between 0.2wt.% and 0.6wt.%, the intermetallics would be a discontinuous $(Cu,Ni)_6Sn_5$ layer formed over a continuous $(Ni,Cu)_3Sn_4$ layer.

The results of this research showed that during reflow soldering, Sn-3.8Ag-0.7Cu solder materials reacted with an EN UBM coating, resulting in a continuous IMC layer i.e. $(Cu,Ni)_6Sn_5$ at the solder/EN interface, and Ag_3Sn in the body of solder bumps. These IMCs were confirmed by EDX analyses and EBSD diffraction patterns as shown in Fig. 7-14 and 7-15, respectively. It can be seen that Ag did not participate in the interfacial reactions with the Ni or Sn at the interface.

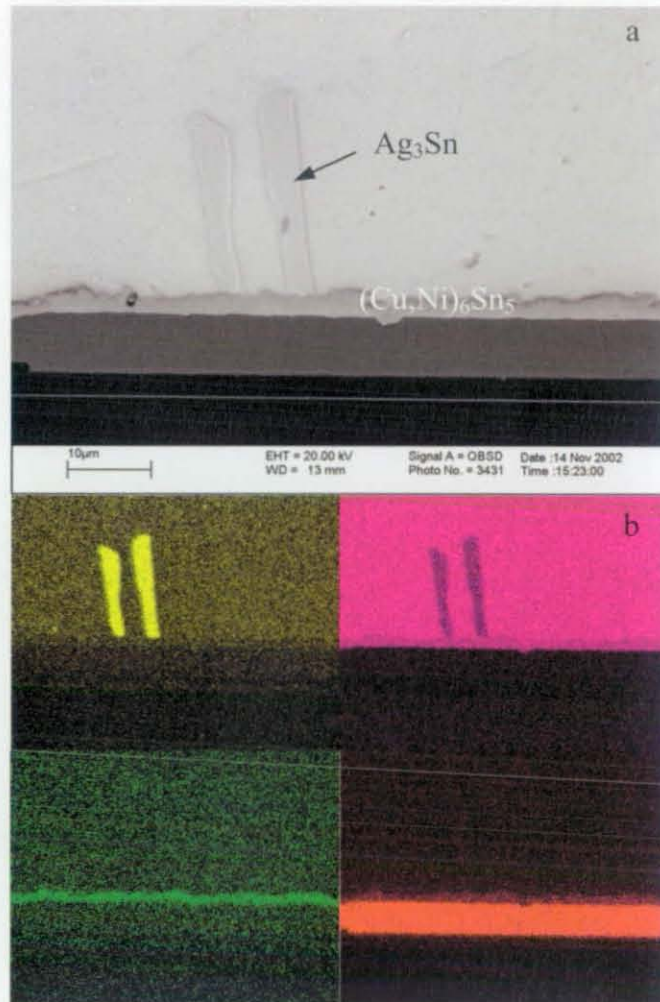


Fig. 7-14 SEM image and EDX mapping of solder bump interfaces after ageing 50 hours in 80℃.

Figs. 7-16 shows the EBSD mappings of the interface in a solder bump in the 'as reflowed' state. It shows that a large Ag_3Sn single crystal IMC had formed in the bulk solder next to the main IMC layer at the solder/EN interface. It seems that the large Ag_3Sn IMC grew from one nucleation point. Because the $(Cu,Ni)_6Sn_5$ IMC layer was not uniform and, after polishing, the surface was not smooth, the signal from this layer was very weak, such that the $(Cu,Ni)_6Sn_5$ IMC cannot be easily identified. The

existence and diffusion of the amorphous EN layer next to this IMC layer had also affected its identification. But EDX analysis and EBSD diffraction patterns from some points in the main IMC layer did confirm there was Cu_6Sn_5 containing a small amount of Ni. It is worth considering the possibility for the existence of the other Ni-Sn based IMCs, for instance a $NiSn_2$ phase was also identified at the interface in the 'as reflowed' samples.

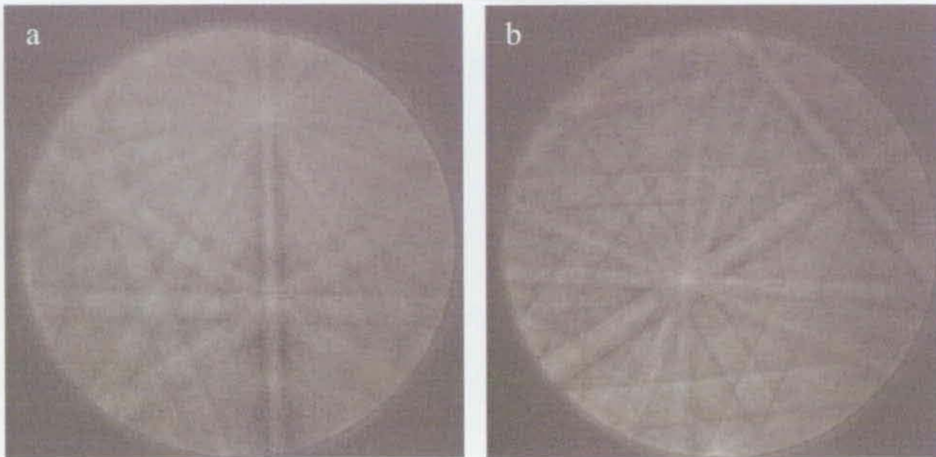


Fig. 7-15 EBSD diffraction patterns of different phases after ageing, a) Ag_3Sn, b) $(Cu,Ni)_6Sn_5$.

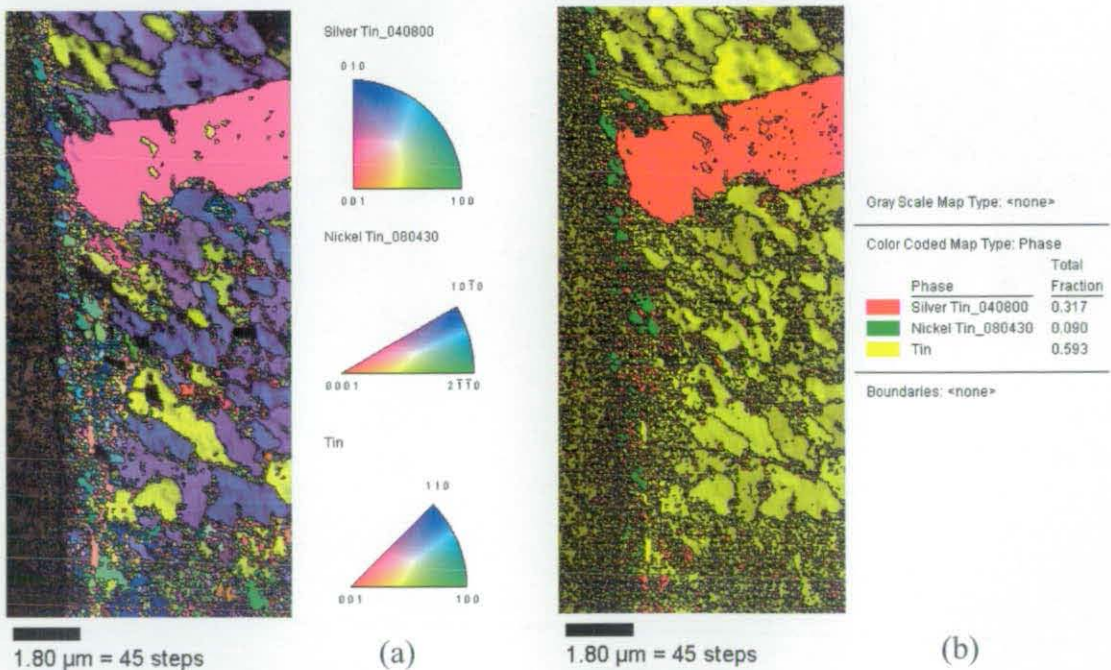


Fig. 7-16 EBSD mapping of solder joint as-reflowed, a) inverse pole figure and b) phase map and image quality.

According to research of Li et al. [53], the interface reactions between eutectic Sn-Ag-Cu and Al/Ni(V)/Cu UBM after one reflow at 260°C consumed the Cu layer completely. The Ni(V) UBM layer disappeared after 20 reflow cycles, when the $(Cu,Ni)_6Sn_5$ IMC began to de-wet and separate from the Al bond pad layer. Once the Ni(V) UBM layer was consumed completely the $(Cu,Ni)_6Sn_5$ IMC began to contact and react with Al, which had a high interface energy and therefore caused the de-wetting of the $(Cu,Ni)_6Sn_5$ IMC from the Al layer. In this study, no de-wetting was observed, because the consumption of the Ni-P UBM layer was very slow and 6 μm of Ni-P UBM was sufficient to avoid further interactions between solder and Al-Cu bond pad.

7.3.2 IMC growth

Appropriate IMCs formed at the interfaces can enhance the wettability and adhesion strength of solder joints [108]. However, due to their brittle property, overgrowth of these IMCs can degrade the mechanical properties of solder interconnections [109, 110]. In the mean time, growth of IMCs may decrease the electrical property of solder joints due to their low conductivity. Research has shown that the IMC layer increases linearly with the square root of ageing time [111-115]. It is believed that the growth of the IMC during ageing is controlled by the volume diffusion or stationary grain-boundary diffusion, such that:

$$d = d_0 + \sqrt{Dt} \tag{7-1}$$

where d is the IMC thickness, d_0 the original thickness, D diffusion coefficient and t the ageing time. It is also believed that Cu diffusion in the EN UBM layer is a kinetically slow process and, as such, the EN coating acts as a barrier to suppress further reactions between solder and Al-Cu bondpad. The continual $(Cu,Ni)_6Sn_5$ IMC layer formed at the interface is also expected to prevent inter-diffusion between the solder and EN layer.

Table 7-3 The IMC thickness increase of solder bumps during ageing at 80°C

Samples	IMC thickness (μm)	Thickness increase (μm)
As-reflowed	2.01±0.11	-
Aged 50 hours	2.06±0.09	0.05±0.14
Aged 750 hours	2.35±0.10	0.34±0.14
Aged 1080 hours	2.40±0.11	0.39±0.15

Table 7-4 The IMC thickness increase of solder bumps during ageing at 150°C

Samples	IMC thickness (μm)	Thickness increase (μm)
As-reflowed	2.01±0.11	-
Aged 2 days	2.19±0.10	0.18±0.15
Aged 10 days	2.61±0.10	0.60±0.14
Aged 18 days	2.99±0.09	0.98±0.14

Tables 7-3 to 7-5 show the $(Cu,Ni)_6Sn_5$ thickness increase (with standard error) for solder bumps during ageing at 80°C, 150°C and 175°C, respectively. The growth of $(Cu,Ni)_6Sn_5$ during thermal ageing at 80°C was observed as very slow and relatively benign. This is probably because the ageing temperature is lower and the diffusion of Cu in EN UBM and the diffusion of Sn and Ni in $(Cu,Ni)_6Sn_5$ is very slow, resulting in a very small diffusion coefficient D. However, when the chips were aged at 150°C and 175°C, the IMC growth became very obvious, although the thickness increase of the IMC was still very small even after ageing at 150°C for 18 d. Fig. 7-17 shows that the thickness increase of a $(Cu,Ni)_6Sn_5$ IMC during ageing at different temperatures. It can be seen that the IMC growth was diffusion controlled and the thickness increase was proportional to the square root of ageing time. Following the Arrhenius equation:

$$D = D_0 \cdot Exp(\frac{-Q}{kT}) \quad (7\text{-}2)$$

where D is the diffusion coefficient, D_0 the diffusion constant, Q the IMC growth activation energy, k the Boltzmann constant and T the absolute temperature, the activation energy Q can be calculated as shown in Fig. 7-18. The result shows that the activation energy of $(Cu,Ni)_6Sn_5$ IMC growth is about 0.59eV and the diffusion constant is about $8.12\times10^{-8}cm^2/s$.

Table 7-5 The IMC thickness increase of solder bumps during ageing at 175°C

Samples	IMC thickness (μm)	Thickness increase (μm)
As-reflowed	2.01±0.11	-
Aged 3 days	2.53±0.10	0.52±0.15
Aged 15 days	3.99±0.16	1.98±0.19
Aged 30 days	4.90±0.15	2.89±0.22

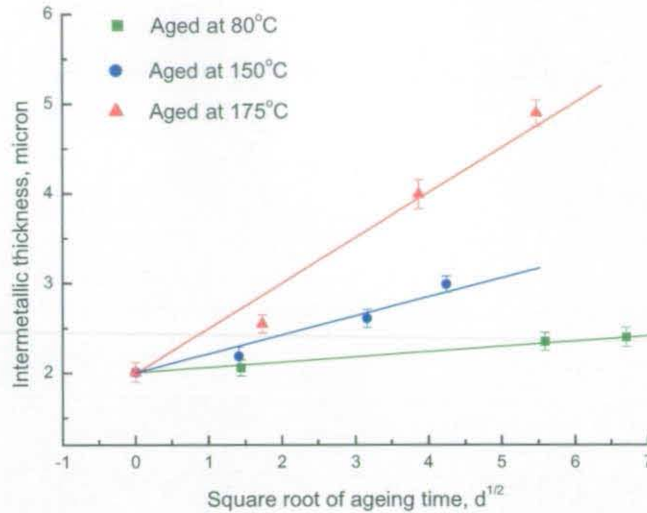


Fig. 7-17 IMC growth during ageing at different temperatures.

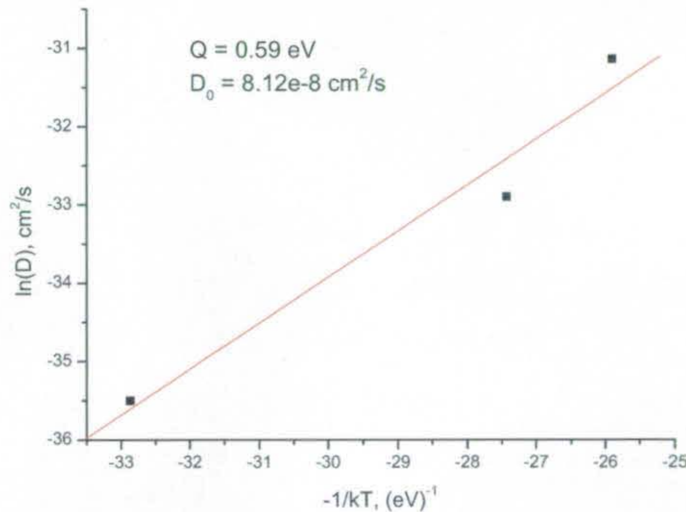


Fig. 7-18 Arrhenius plot of $(Cu,Ni)_6Sn_5$ IMC growth.

Many people have suggested that the Ag_3Sn IMC was predominately formed from the initial reflow processes and, as such, it did not evolve in the subsequent ageing processes due to its high chemical stability [105, 116, 117]. However, the results of Allen et al. [118] showed that during ageing Ag_3Sn IMCs could break up and then coarsen.

Fig. 7-19 shows that during the initial stage of high temperature ageing (150°C and 175°C) the Ag_3Sn IMCs became pebble-like phases and during later ageing they did not change significantly. There are two possibilities for the Ag_3Sn IMC growth: one is that only the small IMC particles grew into the pebble-like phases and the plate- and

lamella-like phases did not change significantly; the other is that the small IMC particles were coarsening and the plate- and lamella-like phases broke up first and then coarsened. No plate- or lamella-like Ag_3Sn phases were found after high temperature ageing. A chip after ageing at 80°C for 10 d and 150°C for 18 d was cross-sectioned from the top to different levels, with no plate- or lamella-like Ag_3Sn phases found. It seems that the second possibility is the growth mechanism of Ag_3Sn IMC during high temperature ageing.

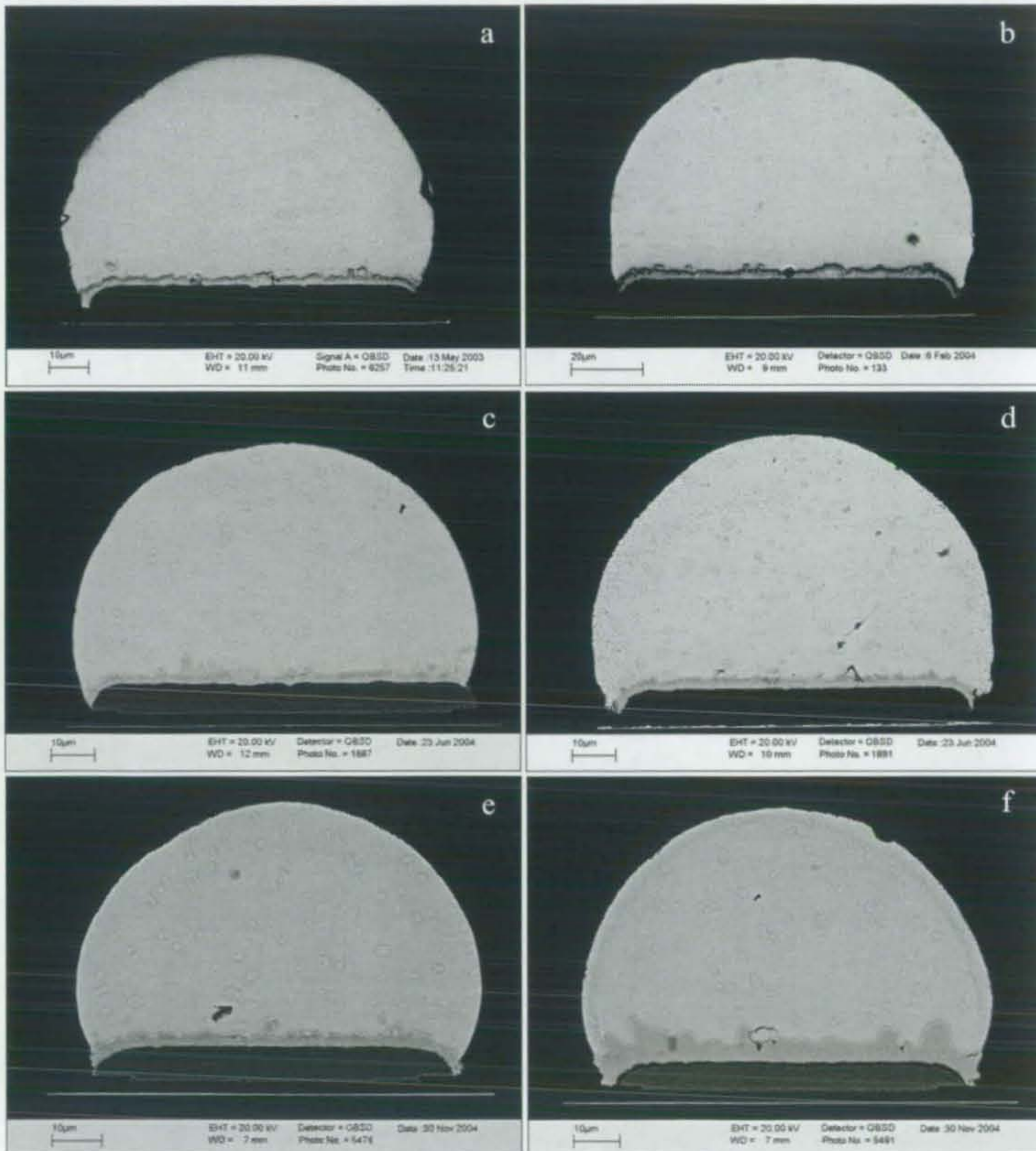


Fig. 7-19 Microstructure of ASH solder bumps as reflowed and after ageing at different temperature. a) as reflowed, b) after ageing at 80°C for 750 h, c) after ageing at 150°C for 2 d, d) after ageing at 150°C for 10 d, e) after ageing at 175°C for 3 d, and f) after ageing at 175°C for 30 d.

The small Ag_3Sn particles inside the solder interconnect can be beneficial due to precipitate strengthening. The Ag_3Sn is more brittle and less ductile compared to the matrix of the solder alloy and therefore the small, evenly distributed Ag_3Sn IMC particles in the solder may improve the mechanical properties and interconnect integrity and the solder becomes more compatible with the harder EN UBM. However, the plate-like Ag_3Sn phase across the bump can significantly deteriorate the homogeneity of mechanical properties in the solder bump interconnect. Figs. 7-20 and 7-21 show the Ag_3Sn IMCs formed at the corner and near the large void of solder bumps respectively, where stress will accumulate and cracks may initiate and propagate, resulting in failure of solder joints. Kim et al. [88] studied the influence of cooling speed on the tensile properties of Sn-Ag-Cu alloys and found that the existence of plate-like Ag_3Sn can reduce the elongation of bulk solder and cracks prefer to propagate along the Ag_3Sn/solder interface. Later the study of Henderson et al. [119] showed that not only crack, but also grain boundary sliding, could form at the Ag_3Sn/solder interface during thermal cycling. In this case it is perhaps prudent to avoid the formation of these large Ag_3Sn phases in the solder interconnect. The results of Kang et al showed that the formation of such large Ag_3Sn phases could be kinetically controlled by employing a fast cooling rate, such as 1.5 K/s or higher during the reflow soldering process [117].

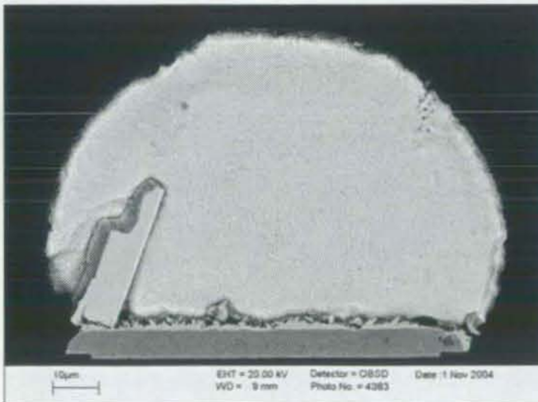


Fig. 7-20 Ag_3Sn IMC at the corner of the Sn-Ag-Cu solder bump.

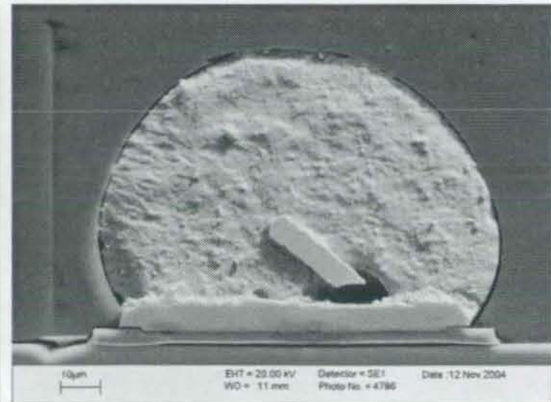


Fig. 7-21 Ag_3Sn IMC and hole in the Sn-Ag-Cu solder bump.

7.3.3 Formation of Kirkendall voids

During the solid-state reactions, Kirkendall voids may form at the interface of IMCs and UBM (Cu [111, 115] and EN [22, 114]) due to the different diffusion rates of elements

in different substrates. This research shows that the Kirkendall voids, if they exist at the IMC/EN interface after low temperature ageing (80°C for up to 1080 h), cannot be readily identified by SEM. However, Kirkendall voids were apparent in the solder bumps after high temperature ageing. Fig. 7-22 shows that Kirkendall voids can be seen in the solder bumps even when the chips were aged at 150°C and 175°C for only 2 d and 3 d, respectively, and during the further ageing the size and number of Kirkendall voids were increasing. This is consistent with the research reported by He et al [114].

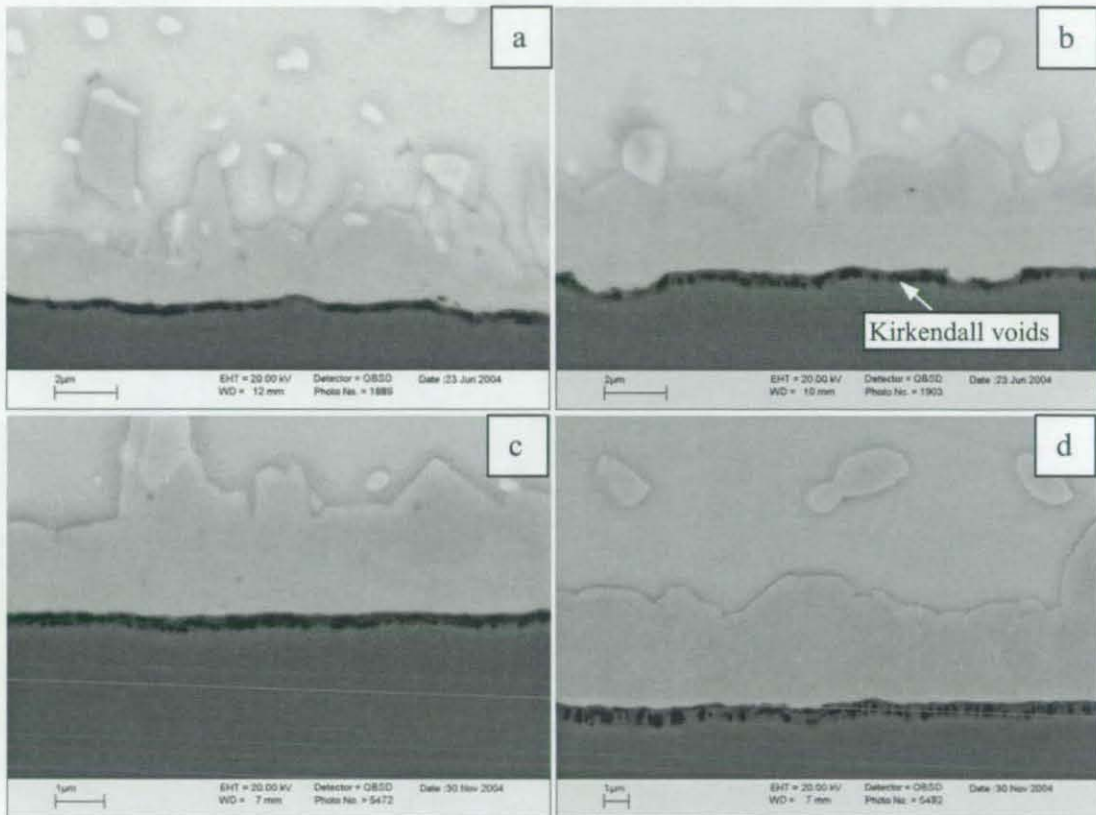


Fig. 7-22 Microstructure of IMC/EN interface in solder bump after different ageing, a) aged 2 d at 150°C, b) aged 18 d at 150°C, c) aged 3 d at 175°C and d) aged 30 d at 175°C.

When studied the interfacial reactions between eutectic Sn-Ag-Cu solder and Au/EN/Al UBM after different reflows and ageing, Zeng et al. [22] found that Kirkendall voids formed in the NiSnP layer near the $(Cu,Ni)_6Sn_5$ IMCs. It is thought the voids were generated by the outward diffusion of Sn from the NiSnP layer, because the diffusion of Sn to Ni_3P layer is faster than that of Sn from the $(Cu,Ni)_6Sn_5$ IMC. He et al. [114] studied the interfacial reactions of Sn-3.5Ag with Au/EN UBM. Their results showed that the main IMC formed at the solder/EN interface was Ni_3Sn_4 and there were two

layers of IMCs between Ni_3Sn_4 and EN UBM, i.e. NiSnP close to Ni_3Sn_4 and Ni_3P close to EN, and Kirkendall voids formed in the Ni_3P layer. The formation of NiSnP indicates that the Sn can diffuse through the Ni_3Sn_4 and react with Ni_3P. He et al. [18] analysed the formation mechanism of Kirkendall voids carefully and suggested the diffusion inside Ni_3P was along the grain-boundaries and the formation of the voids was caused by the net Ni diffusion out from Ni_3P layer to NiSnP and Ni_3Sn_4 layers while there was not enough compensation from other elements to fill the vacant sites left by Ni.

In this study, the Kirkendall voids formed in the Ni_3P layer close to the EN layer, which is consistent with the results of He et al., but no NiSnP layer was found. This is probably a result of the different IMC formed at the solder/EN interface. The solder studied in this study is Sn-3.8Ag-0.7Cu and the IMC formed at the solder/EN interface is $(Cu,Ni)_6Sn_5$. It seems that Sn and Ni diffuse much more slowly in $(Cu,Ni)_6Sn_5$ than in Ni_3Sn_4.

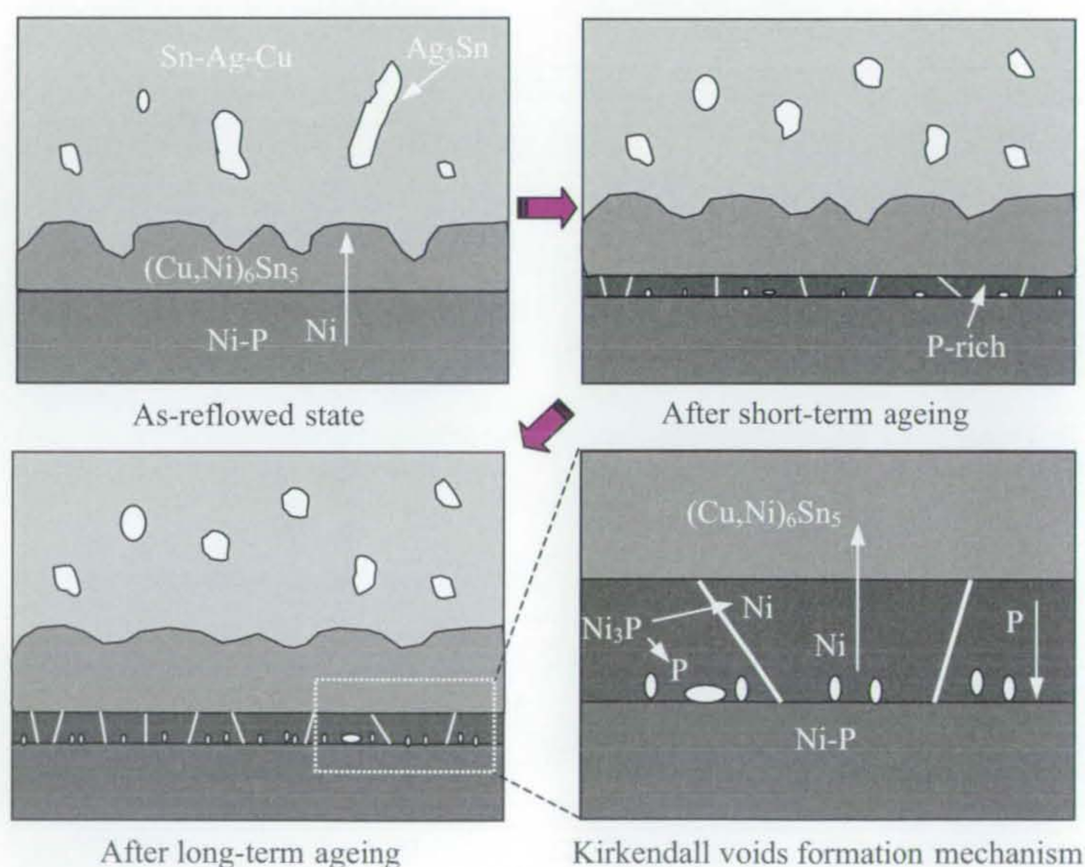


Fig. 7-23 Proposed formation process of Kirkendall voids in Sn-Ag-Cu/EN solder bumps during high temperature ageing.

Fig. 7-23 shows one possible formation process for Kirkendall voids in Sn-Ag-Cu/EN solder bumps during high temperature ageing. During the reflow and initial stage of ageing, Ni diffuses into and reacts with the solder to form $(Cu,Ni)_6Sn_5$ IMCs; however, P does not take part in the interface reactions and will stay in the EN layer, resulting in a P-rich layer, which subsequently crystallized into Ni_3P. During ageing the Ni_3P decomposes into Ni and P, which diffuse along the grain-boundaries because of the low activation energy. Ni will diffuse into the $(Cu,Ni)_6Sn_5$ IMC and solder resulting in the growth of $(Cu,Ni)_6Sn_5$ and P will diffuse back to the Ni_3P/EN interface to form more Ni_3P, since no P is found in the $(Cu,Ni)_6Sn_5$ and Sn-Ag-Cu solder. The Ni_3P layer has a columnar structure and there are many vacant sites, such that Ni diffuses faster in the Ni_3P layer, which can cause a net Ni diffusion out of the Ni_3P layer at the bottom side, resulting in the formation of Kirkendall voids in this region.

7.4 IMCs formed with different solders and substrates

Cu, immersion Ag on Cu (CuImAg), electroless Ni (EN) and electroless Ni immersion gold (ENIG) are several surface finishes normally used on PCBs or chips. The reactions of Sn-Pb solder with these substrates have been studied widely [99, 120-127], but the reactions between different lead free solders and different substrates have not been systemically studied and compared.

7.4.1 Growth and thickness of IMCs

As we know, when the substrates are Cu and CuImAg, during reflow the solders react with Cu to form the Cu_6Sn_5 IMC. Because in the solid state Sn and Cu diffuse very slowly inside Cu_6Sn_5 IMC, Cu will accumulate at the interface of Cu and Cu_6Sn_5 resulting in the formation of Cu_3Sn, which will consume some of the Cu_6Sn_5 IMC at the beginning of the solid reactions. During subsequent ageing, the Cu will diffuse towards the solder and Sn will diffuse towards the Cu substrate, resulting in the growth of both Cu_3Sn and Cu_6Sn_5 IMC layers. Lee et al. [128] studied the kinetics and thermodynamics of solid-state ageing of eutectic Sn-Pb and lead free solders on Cu, and their results showed that both Cu_6Sn_5 and Cu_3Sn IMCs formed at the interface of the solder joints for all the Sn-Pb and lead free solders. The results also showed that the thickness of

Cu_6Sn_5 decreased at the beginning of ageing at 125°C for eutectic Sn-Pb and Sn-3.5Ag solders and this thickness reduction was due to growth competition with Cu_3Sn. It seems that at the beginning of the ageing, if the consumption rate of Cu_6Sn_5 is greater than the growth rate, the thickness will decrease.

When the substrates are EN and ENIG, during reactions of the solders with the EN layer, the Ni will diffuse into the solder and form the Ni_3Sn_4 or $(Cu,Ni)_6Sn_5$ IMCs, but the P does not take part in the interface reactions and will stay in the EN layer, so the top of the EN layer will become P-rich and crystallize into Ni_3P.

This studies showed that the growth of Cu_6Sn_5 IMC was faster than that of $(Cu,Ni)_6Sn_5$ IMC, which was also mentioned in the study of Yoon et al. [129]. From Figs. 6-43 to 6-45 and Table 6-4, it can be seen that the thickness of IMCs on Cu and CuImAg substrates was much thicker than that of IMCs on EN and ENIG substrates. It seems that the growth of Cu_6Sn_5 is faster than that of Ni_3Sn_4 and $(Cu,Ni)_6Sn_5$.

For the reaction between lead free solders and EN or ENIG substrates, when there is no Cu in the solder, the IMC formed at the interface is Ni_3Sn_4 and, when the solder contains Cu as little as 0.6wt.%, the IMC will be $(Cu,Ni)_6Sn_5$ and not Ni_3Sn_4 [22, 107]. This is caused by the different activation energy of these two IMCs. In the Cu-Ni-Sn ternary system, $(Cu,Ni)_6Sn_5$ is more stable than Ni_3Sn_4, so when there is a certain amount of Cu in the solder, $(Cu,Ni)_6Sn_5$ will form at the interface [22]. Ni_3Sn_4 can consume much more Ni than $(Cu,Ni)_6Sn_5$, which can be confirmed by the interfacial microstructure of Sn-3.5Ag on ENIG substrate, in which almost all the EN layer has been consumed, but for the Sn-0.7Cu and Sn-3.5Ag-0.7Cu systems the remaining EN layers are still very thick (Figs. 6-43 to 6-45). Cu and Sn diffuse very slowly in an EN layer, which acts as a diffusion barrier. If most or the entire EN layer is consumed, the solder will react directly with Cu or Al. If the metal beneath EN coating is Cu, the reaction will become stronger and more IMCs will form at the interface; if the metal beneath EN coating is Al, as mentioned in Section 7.3 de-wetting may happen.

Since the Ni_3Sn_4 IMC has more diffusion channels than the $(Cu,Ni)_6Sn_5$ IMC, the elements can diffuse more quickly in the Ni_3Sn_4 IMC, resulting in a thicker IMC (Ni_3Sn_4) layer, as shown in Table 6-4. This means that when the substrate used is EN or

ENIG, a certain amount of Cu can be added into the lead free solders, such that the $(Cu,Ni)_6Sn_5$ IMC will form at the interface and act as a diffusion barrier, resulting in a slow IMC growth and a thin IMC layer. It is known that too much IMCs formed at the interface will degrade the mechanical properties of solder joints, so Cu is a very important element in lead free solders when an EN or ENIG substrate is used. The large diffusion rate of elements in a Ni_3Sn_4 layer could also be confirmed by the formation of the NiSnP layer between Ni_3Sn_4 and Ni_3P when Sn-3.5Ag reacted with ENIG substrate, which meant a large amount of Sn diffused through the Ni_3Sn_4 layer and reacted with Ni_3P. This NiSnP layer has also been reported by He et al. [114] when they studied the interfacial reactions of eutectic Sn-Pb and Sn-3.5Ag solders with EN UBM.

7.4.2 Cracks in the IMCs

The IMCs formed in the solder joints are brittle, and when their size becomes large they can be easily broken by an external force. During the initial stages, after polishing of the samples, there were many cracks found in the IMCs, as shown in Fig. 7-24. In order to find the reason for formation of these cracks, the solders around the IMCs were etched in some of the samples. Fig. 7-25 shows the microstructure of IMCs formed at the interface of Sn-3.8Ag-0.7Cu solder and Cu substrate after etching. From this image, it can be seen that the cracks are shallow and exist only in the top part of the IMC, which indicates these cracks might be created by the grinding and polishing processes. Samples were re-polished: starting with silicon carbide paper grit 400 and finished with 0.02 μm silica, and in total about 1 mm was removed from the surface. The microstructures of solder joints after re-polishing are shown in Fig. 6-43 to 6-45 without or with less cracks, which confirmed that the cracks were caused by grinding. So grinding and polishing of this kind of sample needs to be careful, and large forces and small grit silicon carbide papers need to be avoided.

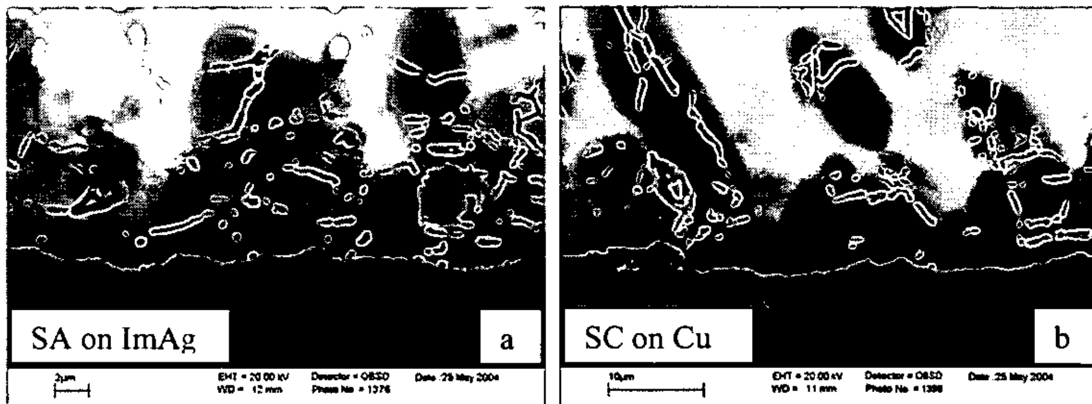


Fig. 7-24 Solder joints with cracks in the IMCs after the initial polishing.

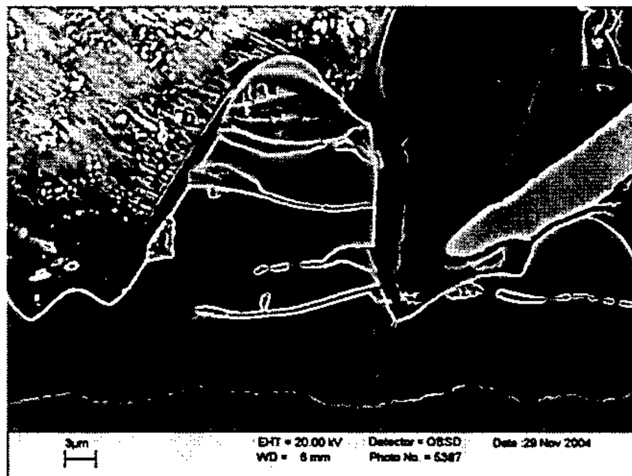


Fig. 7-25 Microstructure of IMCs formed at the interface of Sn-Ag-Cu solder and Cu substrates after etching.

7.4.3 Formation of Kirkendall voids

Figs. 6-43 to 6-45 showed that when an EN or ENIG substrate was used, Kirkendall voids formed inside the Ni_3P layer, except when Sn-3.8Ag-0.7Cu reacted with EN substrate and, when a CuImAg substrate was used Kirkendall voids formed inside the Cu_3Sn IMC layer.

For EN and ENIG substrates, the formation mechanism of Kirkendall voids is the same, because during the first reflow the thin immersion Au layer can be dissolved into the solder quickly and the solder will react directly with EN layer. The top of the electroless

Ni can crystallize into Ni_3P during reflow. The formation mechanism of Kirkendall voids has been discussed in Section 7.3.3. During high temperature ageing, more and more voids will form and the small voids will grow into the large voids, and even lines of voids can be formed as shown in Fig. 6-45d.

The study of Xiao et al. [111] shows that during long-time ageing of Sn-Pb solder on a electroplated Cu stud, Kirkendall voids formed in Cu_3Sn layer. The formation mechanism of Kirkendall voids in Cu_3Sn layer appeared to be different from that of Kirkendall voids in Ni_3P. The main diffusion element in Cu_6Sn_5 is Sn, but that in Cu_3Sn is Cu [130, 131]. The formation of Cu_3Sn results from the interdiffusion of Cu and Sn. Because Sn diffuses very slowly inside Cu_6Sn_5, no sufficient Sn is available to react with Cu in Cu_3Sn layer. The lack of Sn in the lattice spaces of Cu_3Sn can therefore result in the formation of Kirkendall voids. However in this study, when pure Cu was used as the substrate, no Kirkendall voids were found in the Cu_3Sn layer, and only when the CuImAg substrate was used could Kirkendall voids be found. It seems that the formation of Kirkendall voids is related to the immersion Ag, but the reason is still not clear at this time.

7.5 Micro-mechanical properties

Although the mechanical properties of individual phases do not represent the mechanical properties of the whole solder joint, they do influence the mechanical properties. In addition, such data can be used in finite element modelling.

7.5.1 Influence of assembly and ageing

Comparing the data from Tables 6-5 and 6-6, it can be seen that the mechanical properties of phases in the solder joints before and after the assembly were similar. Although a new phase, $AuSn_4$, formed in the solder joints after assembly due to the immersion Au on the PCB side, the composition of other phases in the solder joints did not change greatly. Since all the tests were conducted at room temperature and the same atoms before and after the assembly had the same activity, the mechanical properties of the same phase would be similar.

During ageing the thickness of IMCs increases and the composition of the IMC may change. Some researchers have shown that during reflow the content of Ni in $(Cu,Ni)_6Sn_5$ IMCs increases [129]. In this research the compositions of IMCs did not change greatly during ageing. Table 6-6 to 6-8 show that the mechanical properties of phases in the solder joints as assembled and after ageing at 150°C for different times were similar. It seems that ageing did not affect the mechanical properties of individual phases in the solder joints significantly.

7.5.2 Influence of testing temperatures

Table 6-9 and 6-10 show that the hardness and modulus of phases in solder joints decreased at elevated temperatures, and that this decrease was very significant when the testing temperature was higher than 150°C. Since the melting temperatures of solders are low and the homologous temperatures are greater than 0.5 even at room temperature, the atoms of solder materials will become very active at high temperatures. In this condition, the solder materials become very soft, which will greatly degrade the mechanical properties of solder materials. The mechanical property decrease of IMCs was not as expected due to their high melting temperature. Since the material underneath the IMCs was the solder material that was supporting the IMCs when they were pushed by the indenter and became soft at high temperature, the substantial mechanical property degradation of IMCs seems to have been caused by the softening of solder material. As a result, the mechanical properties of IMCs from nanoindentation at high temperatures are not reliable.

7.5.3 Pile-up and sink-in during nanoindentation

Pile-up or sink-in is often seen when indentations are made in materials. Fig. 7-26 shows the AFM images of nanoindentations on different phases of solder joints on different substrates after long reflow periods. It can be seen that the indentations in Sn-Cu and Sn-Ag-Cu solders had some pile-up, which were confirmed by AFM section analysis as shown in Figs. 7-27 and 7-28. However, for the Cu_6Sn_5 and Ag_3Sn phases no clear pile-up or sink-in can be seen. Deng et al. [132] calculated the degree of pile-up/sink-in of different phases in solder joints using a 2D model developed from that of

Dao et al. [133] and the results showed that pure Sn and eutectic Sn-Ag exhibited significant pile-up and Ag_3Sn, Cu_6Sn_5 and Cu_3Sn IMCs exhibited sink-in, but the degree of sink-in was very low, which is consistent with the results in this study. Because the sink-in of IMCs was very benign it could not be seen clearly in this study. When pile-up and sink-in existed around the indentations the true contact area will be larger or smaller than the ideal contact area, respectively. Since hardness is:

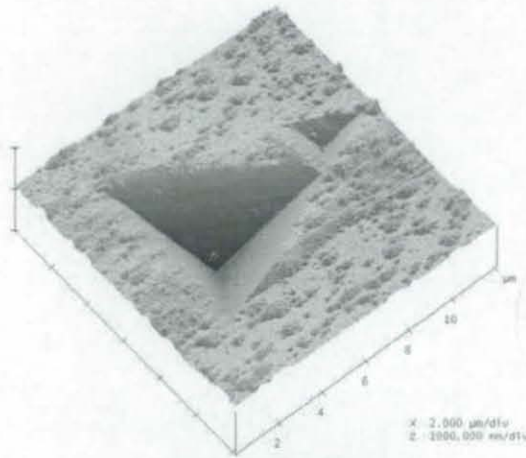
$$H = \frac{P_{Max}}{A} \tag{7-3}$$

and reduced modulus is:

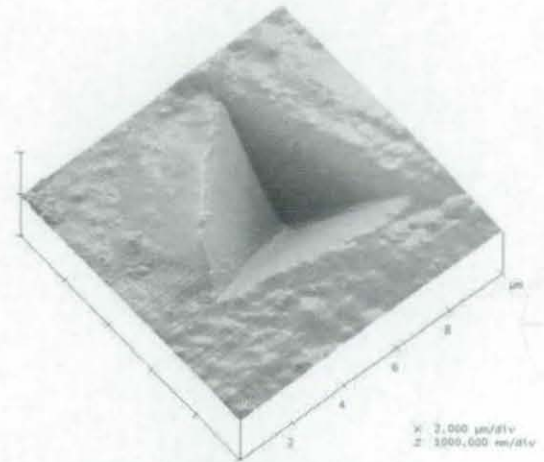
$$E_r = \frac{S}{2\beta}\sqrt{\frac{\pi}{A}} \tag{7-4}$$

pile-up will overestimate and sink-in will underestimate both the hardness and modulus.

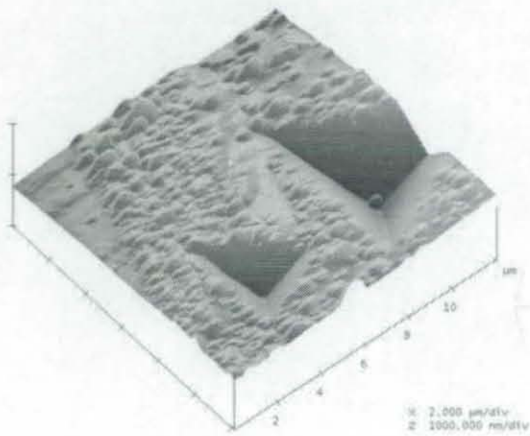
Many researchers [132-141] studied the pile-up and sink-in phenomena during nanoindentation tests. Giannakopoulos et al. [139] pointed out that pile-up occurs when $0.875 < (h_r/h_{max}) \leq 1$ and sink-in occurs when $0 \leq (h_r/h_{max}) < 0.875$ and no pile-up or sink-in occurs when $(h_r/h_{max}) = 0.875$ (h_r is the residual penetration depth). The results of Cheng et al. [142] and Deng et al. [132] showed that the effect of sink-in was less pronounced than that of pile-up. Through the dimensional analysis and finite element calculation, Dao et al. [133] and Cheng et al. [142] proposed one method to calculate the yield strength, σ_y, and the work hardening coefficient, n. Based on the value of σ_y and n, Malzbender et al. [134] gave one method to calculate the hardness and reduced modulus, which can take into account the influence of pile-up and sink-in. This method has not yet been applied in normal nanoindentation tests and calculation and therefore was not applied to the results presented in this thesis; however, it would be better to correct for the effect of pile-up and sink-in, especially the former, during the analysis.



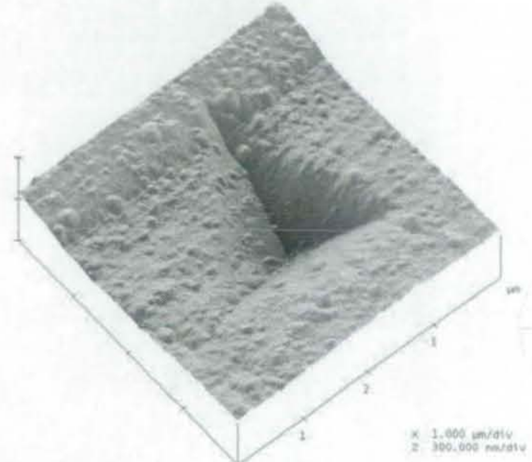
Sn-Cu in Sn-Cu/Cu solder joint



Sn-Ag-Cu in Sn-Ag-Cu/Cu solder joint



Cu_6Sn_5 in Sn-Cu/Cu solder joint



Ag_3Sn in Sn-Ag-Cu/Cu solder joint

Fig. 7-26 AFM images of nanoindentations in different phases.

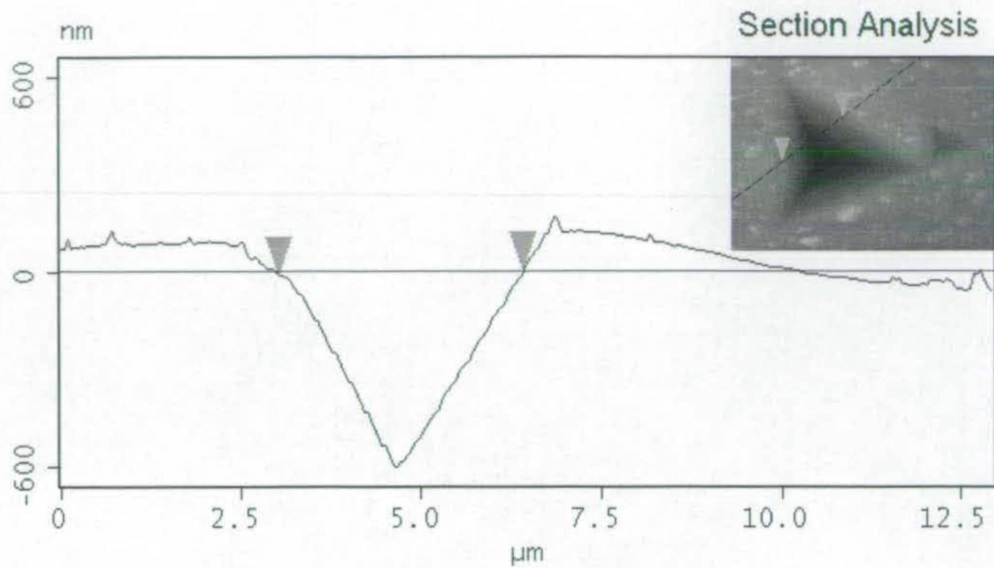


Fig. 7-27 AFM section analysis of nanoindentation in Sn-0.7Cu solder.

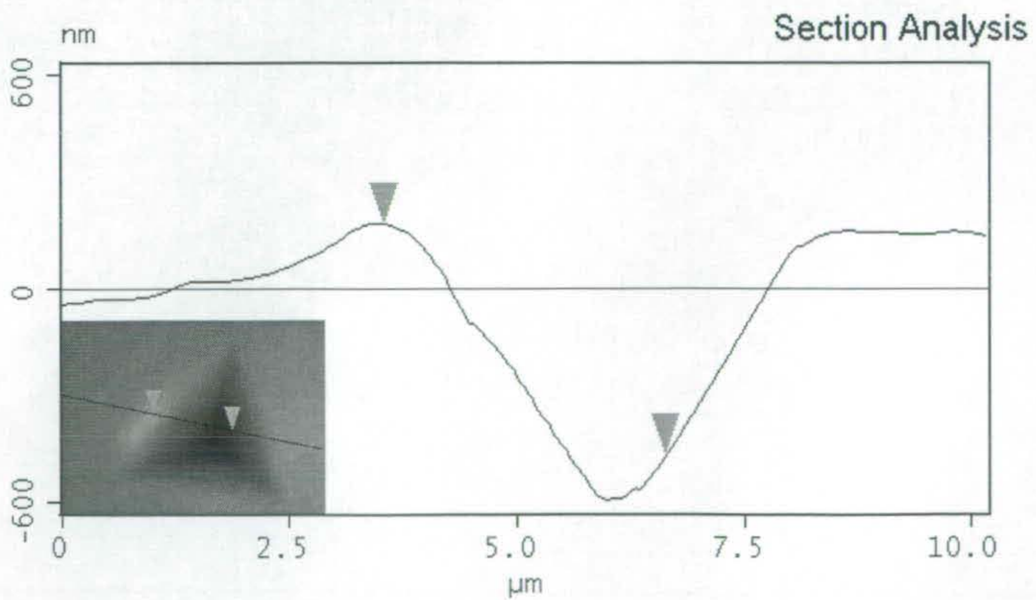


Fig. 7-28 AFM section analysis of nanoindentation in Sn-3.5Ag-0.7Cu solder.

7.5.4 Influence of cooling media

Fig. 6-77 and 6-78 show that the hardness and modulus of lead free solder materials cooled in water were higher than those of solder materials cooled in furnace. The Sn-Ag solder cooled in air presented the highest hardness and modulus, and the hardness and modulus of Sn-Ag-Cu solder cooled in air had the largest deviation. The high hardness and modulus of solders cooled in water were caused by the distribution of small IMCs in the solder. It seems that a high cooling rate can enhance the mechanical properties of solders and get them closer to those of large IMCs in the solder joints.

From Fig. 6-69, it can be seen that almost every indentation on Sn-Ag solder cooled in air was interrupted by the Ag_3Sn lamella, resulting in the high hardness and modulus. Fig. 6-72 shows that there were two kinds of IMCs, Cu_6Sn_5 and Ag_3Sn, with a different size for Sn-Ag-Cu solder cooled in air. Although the indentations on the IMCs were removed, most of the other indentations were still affected by the surrounding IMCs. Because of the various sizes and types of IMCs, the effect on indentations was different, resulting in a large deviation for the hardness and modulus values.

7.6 Creep properties

When solder alloys undergo a constant load at an elevated temperature, a combination of mechanical and thermal effects can lead to creep failure. Creep deformation becomes critical when the temperature exceeds 0.5 T_m (melting temperature in Kelvin) of the material. As for the most commonly used solders, including the Sn-Pb eutectic solder and many lead-free solders, even room temperature corresponds to ~0.6 T_m. Often the service temperature of components can be over 100°C, and the solder joints are normally under thermal and/or external stress, so it is important to gain an insight into the creep behaviour of solders at room and elevated temperatures, which will ultimately influence the reliability of solder interconnections.

Many researchers have studied the creep properties of Sn-Pb and lead free solder materials [71, 72, 143-148], and some results show that both Sn-Pb and lead free solders show different creep exponents in low stress and high stress regimes. The results of

Yang and Li [72] showed that the creep exponent, n, of eutectic Sn-Pb in a low stress regime ranged from 1.01 to 2.71 and in a high stress regime from 3.31 to 6.01 and, that the stress exponent decreased with increasing temperature. The study of Goldstein and Morris [143] showed that the creep exponent of eutectic Sn-Bi was around 3.2 in a low stress regime and 7.3 in a high stress regime. The creep properties of Sn-Ag solder have been studied widely, and the creep exponents range from 3 to 5 in a low stress regime and 7 to 12 in a high stress regime [145-153]. The variation in results from different researchers may be caused by different microstructures and stress regimes.

As we know, the microstructure of Sn-Pb and some lead free solders (i.e., Sn-Ag, Sn-Cu and Sn-Ag-Cu) are different: Sn-Pb presents Sn-rich and Pb-rich phases with lamellar (slow cooling) or equiaxed (fast cooling) structure and the lead free solders exist as β-Sn matrix distributed with IMCs. Due to the different microstructures, the creep mechanisms for Sn-Pb and the lead free solders are quite different. The Sn-rich and Pb-rich phases in Sn-Pb solder have a similar deformation resistance; however, the deformation resistance of IMCs in the lead free solders, such as Cu_6Sn_5 and Ag_3Sn, is much higher than that of the β-Sn matrix. The IMC particles act as obstacles and create a back stress that resists the motion of dislocations and creep deformation cannot occur unless dislocations are able to escape from the pinning particles by one of the following mechanisms [146]:

- Particle cutting
- Bowing between particles (Orowan bowing)
- Climb around particles.

Because the IMCs are much stronger than β-Sn matrix, the particle cutting mechanism is impossible, and the mechanism of dislocation climb over the IMC particle seems reasonable [149]. In order to explain the high creep exponent observed at high stress, a threshold stress was incorporated into the analysis [144, 145, 149]. The threshold stress can be expressed as:

$$\sigma_{th} = \sigma_{OB}\sqrt{1-k_R^{\,2}} \qquad (7\text{-}5)$$

where σ_{th} is the threshold stress at certain temperature, representing the stress required to cause thermally activated detachment of the dislocation segment from the IMC particle, σ_{OB} the Orowan bowing stress, and k_R the relaxation factor. No high stress creep occurs when the applied stress is lower than the threshold stress.

Fujiwara and Otsuka [71] studied the creep properties of β-Sn and eutectic Sn-Pb, and their result showed that there was a transition temperature where the creep activation energy would change. This difference of creep properties at a low temperature and a high temperature was caused by the different creep mechanisms. Research has shown that the creep at a low temperature was controlled by dislocation-pipe diffusion and that at a high temperature was controlled by lattice diffusion [71, 144, 149, 154].

From Figs. 6-79, 6-80, 6-82, and 6-84, it can be seen that the creep exponent of lead free solders in solder joints is around 9.5-12.5 at room temperature, which agrees with the results from other researchers in the high stress regime as mentioned above. The results also show that the creep exponent of lead free solder at high temperatures (125, 150 and 175°C) ranges from 2.5 to 5.0, which agrees with the results from other researchers in the low stress regime. For nanoindentation creep testing the load was held constant during the dwell time and the stress is the maximum load divided by the projected area of the indentations. Because the maximum load was similar for the tests at different temperatures, and the projected area of indentations at high temperatures was much larger than that at room temperature, the applied stress was much lower at high temperatures compared with that at room temperature. It seems that when the test was conducted at high temperatures, the stress was in a low stress regime, resulting in much smaller creep exponents.

Figs. 6-85 to 6-89 and Table 6-11 show that the room temperature creep exponent of bulk lead free solders after cooling in different media ranged from 7.5 to 11.5 and the creep exponent of Sn-Ag solder distributed with small IMCs was higher than that of solder almost without IMCs. It seems that for nanoindentation creep, the cooling rate did not influence the creep exponent. Because the creep was tested in a very small local area, the microstructure, i.e. the IMC distribution, around the indentation was the main factor that affected the creep deformation. According to the particle strengthening mechanism, if there are no particles close to the indentation, particle strengthening will not influence the creep property significantly. Huang et al. [149] studied the creep properties of Sn-Ag at different temperatures, and their results showed that the creep exponents were 12.3, 11.0 and 10.1 at 30°C, 75°C and 120°C, respectively. By introducing threshold stress and temperature dependent shear modulus, G, they removed

the influence of temperature and particle strengthening and got the true creep exponent as 7. In this study, the low creep exponent was just a little higher than 7, and it seemed that in these tests the influence of particle strengthening was quite benign because almost no IMC particles existed around these indentations.

Comparison of the creep properties of lead free solders in solder joints and in bulk solder shows that the solder volume did not affect the creep properties of solders.

Compared with traditional creep testing, the advantages of nanoindentation are that it can be used to test the material with a small volume and a large number of samples are not required. However, because nanoindentation can only control the load and not the stress as constant, when sharp indenters are used, the stress driving the creep process is decreasing and no steady state can be achieved [79]. As a result, the creep curves obtained through nanoindentation do not follow a power-law very well. Actually, in this study, only the first 300 s to 800 s of the curves can be used to calculate the creep exponents. In order to solve this problem, a flat cylindrical punch was suggested to replace the sharp indenters during the creep testing [84, 145]. Because the tip of this punch is flat, the contact area is constant during the test and thus the applied stress is constant at a constant load and steady state creep can be easily achieved.

7.7 Shear strength of ASH solder bumps

In order to replace Sn-Pb solder with lead free solders, the shear strength of these solders have been studied widely [9, 111, 129, 155-159]. Some results showed that the shear strength of lead free solders is better than that of Sn-Pb solder [160].

Due to the different mechanical properties in solder joints, there are several different failure modes in shear tests. A failure mode analysis, along with a fundamental understanding of shear test process and results, is needed to accurately assess solder joint toughness. Some researchers [111, 161, 162] have shown that there are four typical failure modes in shear tests. The first one is pad peel. This occurs when the pad peel strength is lower than the bulk flow stress of the solder. The second one is a ductile fracture through the bulk solder. This occurs when the flow stress of the bulk solder is

less than the pad-peel strength and the interfacial strength of the solder joints. The shear head ploughs through the bulk solder, leaving the pad covered with the solder after the ball has been sheared off. This is the expected failure mode and is typical for a robust solder joint. The third failure method is a brittle fracture at the interface between the solder ball and the IMCs or in the IMC layer. This occurs when the interfacial strength is less than the flow stress of the bulk solder. In this case, there is minimal distortion of the solder ball and the solder ball fractures within the IMC region in a brittle manner. The fourth failure mechanism is a combination of the second and the third. The failure surface exhibits properties of both ductile and brittle fracture.

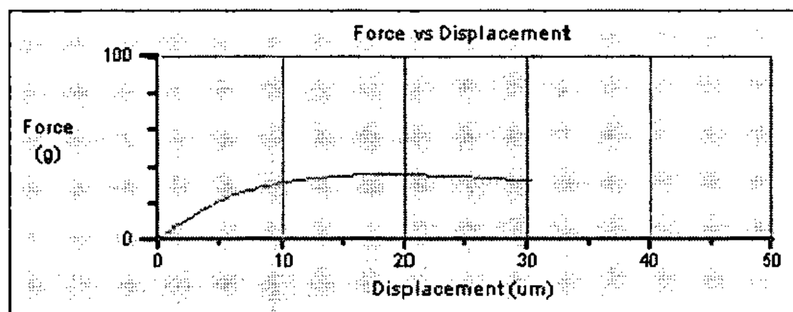


Fig. 7-29 Typical force-displacement curve of shear test.

Fig. 7-29 shows the typical force-displacement curve of shear tests. Once the shear head contacts the solder bump the shear head cuts into the solder bump and the load increases immediately, and when the shear displacement reaches about 20 μm, the shear load begins to drop and then the remaining part of the solder bump is torn away, leaving a dimple fracture surface. Many researchers have reported the dimple fracture surface in lead free solder joints during shear tests [129, 156, 163]. These dimples were caused by crack propagation following a certain angle at some weak points. The fracture surface of lap shear samples is different from that of ball shear samples. With a ball shear sample the first part of the fracture surface is caused by the cutting of the shear head and only the final part can show the dimple structure.

7.7.1 Influence of shear parameters on the shear force

The shear parameters, such as shear height and shear speed, can influence the shear force. The results of Pang et al. [164] and Kim et al. [159, 165] showed that the shear force of Sn-Ag and Sn-Ag-Cu solder joints increased linearly with the shear speed, and the result of Liu et al. [9] showed that the solder bumps showed different shear forces when different shear heights were used and in most studied ranges the shear force decreased with the shear height.

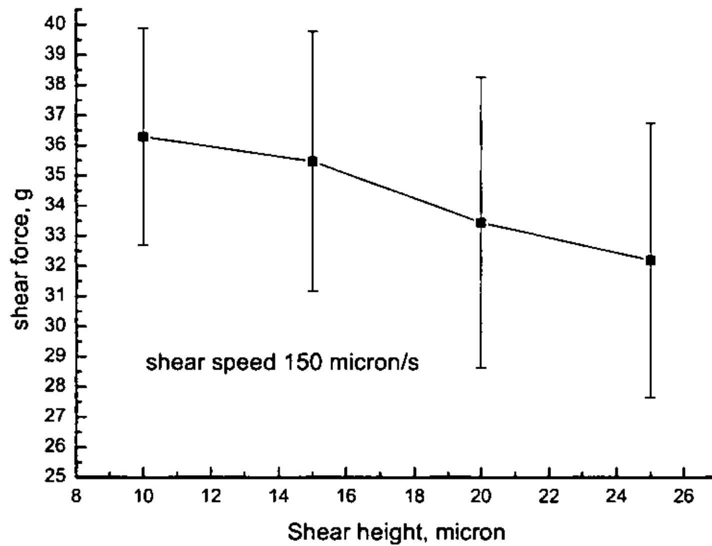


Fig. 7-30 The shear force of as reflowed ASH bumps with different shear heights.

Fig. 7-30 shows the shear force of as-reflowed ASH bumps with different shear heights. The bump height including the EN UBM is about 70 μm, and the thickness of the UBM is about 6 μm. The value of shear height was based on the Cu track connected to the pad, which was almost at the same level as the bottom of EN UBM. The result shows that the shear force decreases with the increase of the shear height in the studied range. The solder bumps have the maximum cross-section area at the height of ~23 μm, so the decrease of shear strength with shear height is slightly larger than shear force.

Fig. 7-31 shows the fracture surfaces of solder bumps as-reflowed with different shear heights. It can be seen that when the shear height was lower than 25 μm the first part of the fracture surface is smooth and the later part is rough. When the shear height was 10 μm the solder bumps fractured both in the solder and at the interfaces. The interfaces

could be solder/$(Cu,Ni)_6Sn_5$ or $(Cu,Ni)_6Sn_5$/Al-Cu or solder/Ag_3Sn, which can be seen more clearly in Fig. 7-32, in which the sample was tilted in the opposite direction. It can also be seen that when the shear height was higher than 15 μm all the solder bumps fractured in the bulk solder. The different shear force with different shear height may be caused by the different microstructures and shear area of solder bumps at different heights. Because the interfaces were stronger than the solder material, when the shear height was 10 μm, the solder bumps showed the highest shear force, although the shear area was smaller than that when the shear height was 15 μm.

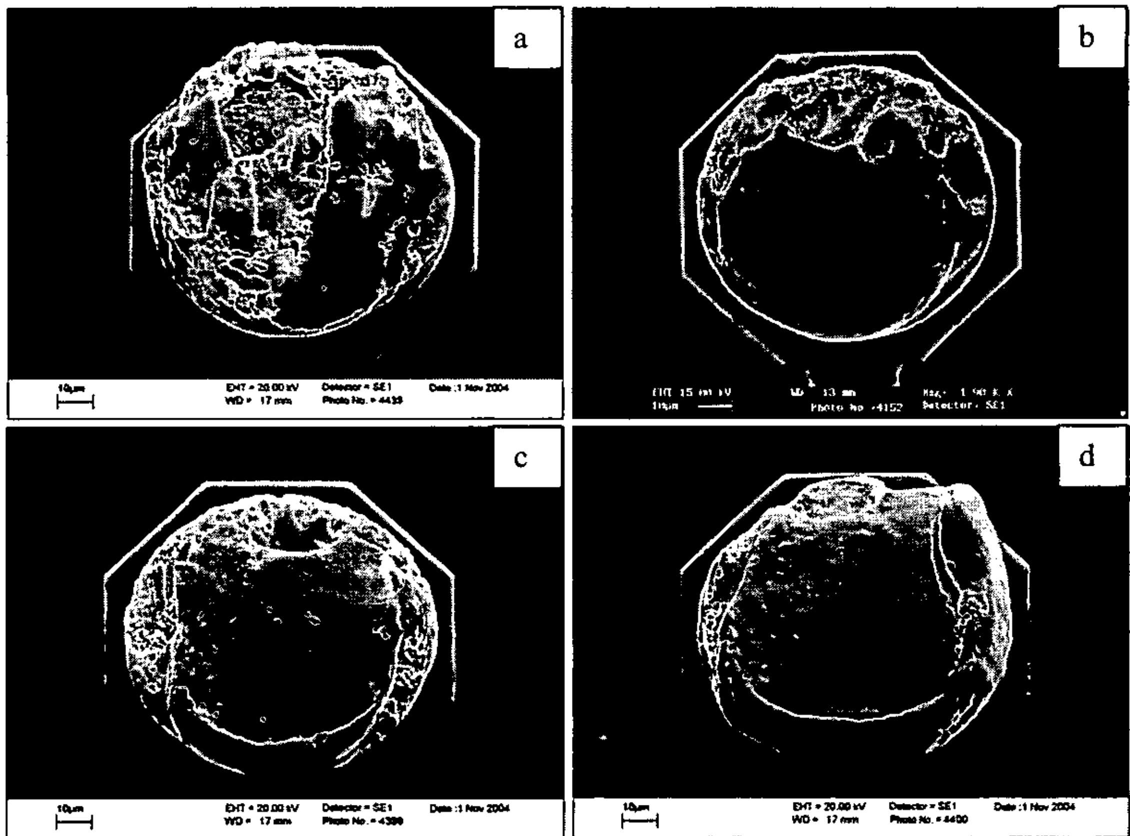


Fig. 7-31 Fracture surface of solder bumps as reflowed with different shear heights, a) 10 μm, b) 15 μm, c) 20 μm and d) 25 μm.

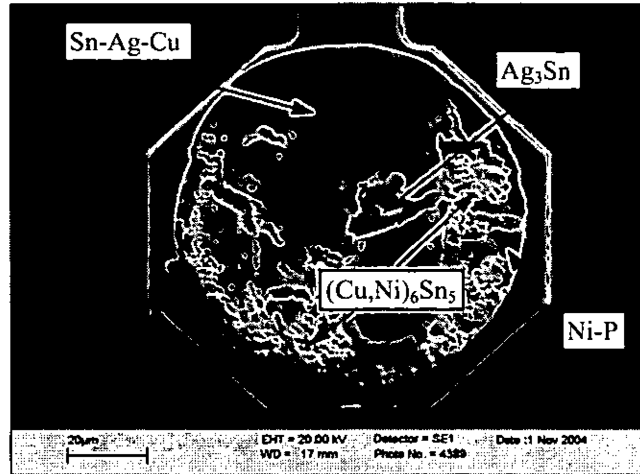


Fig. 7-32 solder bump as reflowed failed at the interfaces and bulk solder (shear height 10 μm).

Fig. 7-33 shows the shear force of as-reflowed ASH bumps with different shear speeds. It shows that the shear force increases with shear speed in the studied range. When the solder bumps were sheared with higher shear speeds, because there was not sufficient time for creep and stress relaxation to occur, the solder bumps showed higher shear force.

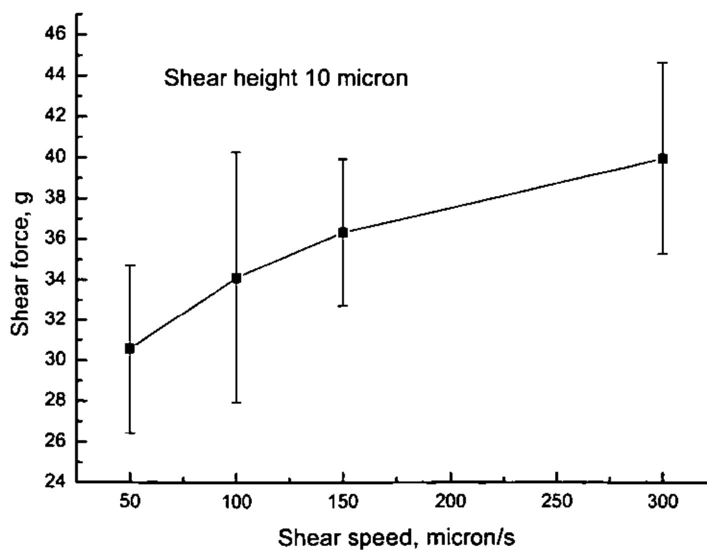


Fig. 7-33 The shear force of as reflowed ASH bumps with different shear speed.

7.7.2 Influence of cooling rate

Kim et al. [88] and Ochoa et al. [87] studied the influence of cooling rate on the tensile strength of Sn-Ag-Cu and Sn-Ag bulk solders, respectively, and their results showed that the rapid cooled solder had the highest tensile strength and the slow cooled solder had the lowest tensile strength, partially due to the formation of a large Ag_3Sn IMC. However, few people studied the influence of cooling rate on the shear strength of lead free solders.

Fig. 7-34 shows the shear force of ASH solder bumps with different shear heights and cooling media. It shows that a lower shear height can produce a higher shear force. However, the cooling media did not influence the shear force greatly. As mentioned in Section 7.2.1, although the particle size of Ag_3Sn IMC in the solder bumps cooled in water was smaller than that in the solder bumps cooled in the furnace, this difference was not significant. It is difficult to say why the shear force of solder bumps cooled in air is slightly higher than those of the solder bumps cooled in other media.

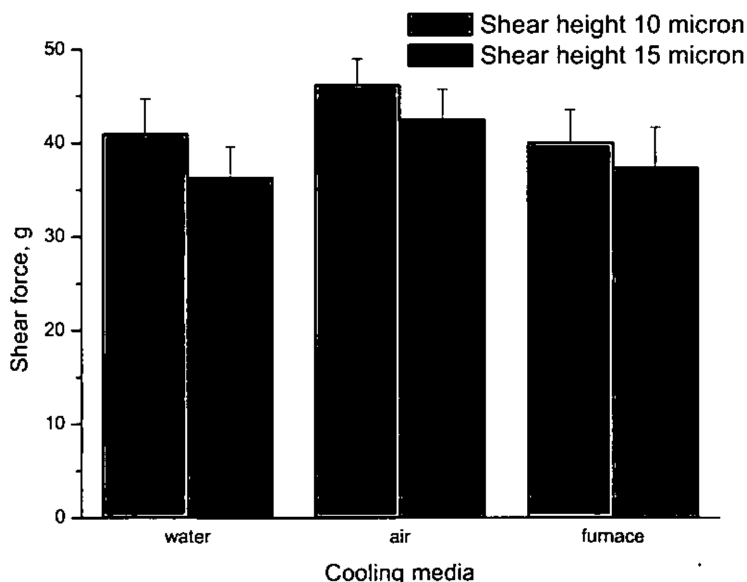


Fig. 7-34 The shear force of ASH bumps with different shear heights and cooling media.

7.7.2 Influence of cooling rate

Kim et al. [88] and Ochoa et al. [87] studied the influence of cooling rate on the tensile strength of Sn-Ag-Cu and Sn-Ag bulk solders, respectively, and their results showed that the rapid cooled solder had the highest tensile strength and the slow cooled solder had the lowest tensile strength, partially due to the formation of a large Ag_3Sn IMC. However, few people studied the influence of cooling rate on the shear strength of lead free solders.

Fig. 7-34 shows the shear force of ASH solder bumps with different shear heights and cooling media. It shows that a lower shear height can produce a higher shear force. However, the cooling media did not influence the shear force greatly. As mentioned in Section 7.2.1, although the particle size of Ag_3Sn IMC in the solder bumps cooled in water was smaller than that in the solder bumps cooled in the furnace, this difference was not significant. It is difficult to say why the shear force of solder bumps cooled in air is slightly higher than those of the solder bumps cooled in other media.

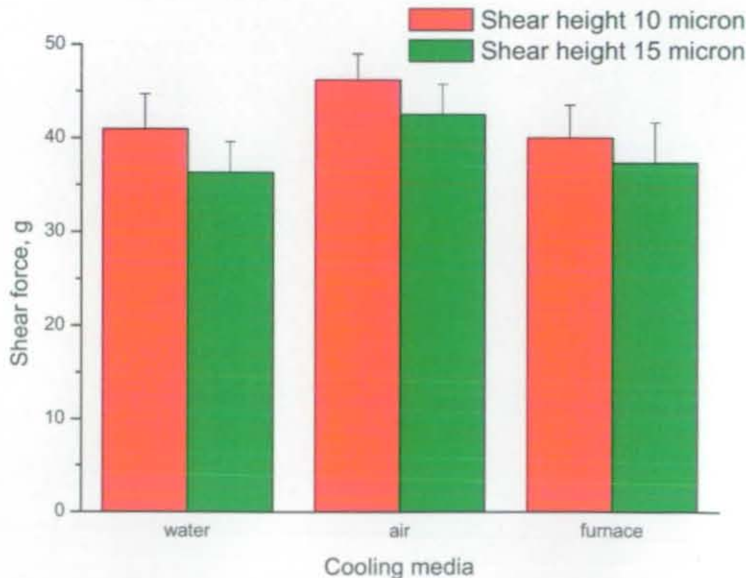


Fig. 7-34 The shear force of ASH bumps with different shear heights and cooling media.

7.7.3 Influence of thermal ageing

Many researchers have studied the influence of reflow time [129, 156, 158, 166] and thermal ageing [96, 156-158, 163] on the shear strength of lead free and Sn-Pb solder joints and their results have shown that the solder joints normally fractured in the bulk solder. Some research showed that multi-reflow or reflow time did not influence the shear strength significantly [129, 156, 158]. However, Lin and Liu [166] showed that multi-reflow degraded the shear strength of Sn-Pb/EN solder joints. The results of Lin and Liu showed that the shape of solder bumps were changed after several reflows and there were some cracks at the corner of solder bumps after 10 reflows, which might be the reason that caused the degradation of shear strength. In the mean time, research also showed that the shear strength of both Sn-Pb and lead free solder joints decreased during thermal ageing [156-158, 163].

There are several sources that can cause the degradation of shear strength of solder joints, such as IMC growth, void formation (e.g. Kirkendall voids), coarsening of IMC particles, and grain growth. During reflow the IMC growth is very quick; however, the shear strength did not degrade with the reflow time and the solder joints fractured in the bulk solder as mentioned above. It seems that the IMC and the interfaces are stronger than the solder materials and the IMC thickness does not influence the shear strength significantly. Thermal ageing can degrade the shear strength of solder joints and the research of Deng et al. [156] showed that the shear strength of Sn-3.5Ag solder joints after reflow was higher than that after thermal ageing at 140°C and 175°C, even though the IMC thickness after reflow was much thicker. During high temperature (such as 125 and 175°C) ageing, the IMC particles were coarsening, and for lead free solders the IMC coarsening is the critical cause of strength degradation. Although the shear strength of Sn-Pb solder joints also decreases during thermal ageing, its mechanism seems different to that of lead free solders. Because Sn-Pb does not have the IMC distribution in the solder the shear strength degraded even at room temperature storage [157, 158]. One possible explanation for the strength degradation of Sn-Pb solder bumps is the grain growth during thermal ageing.

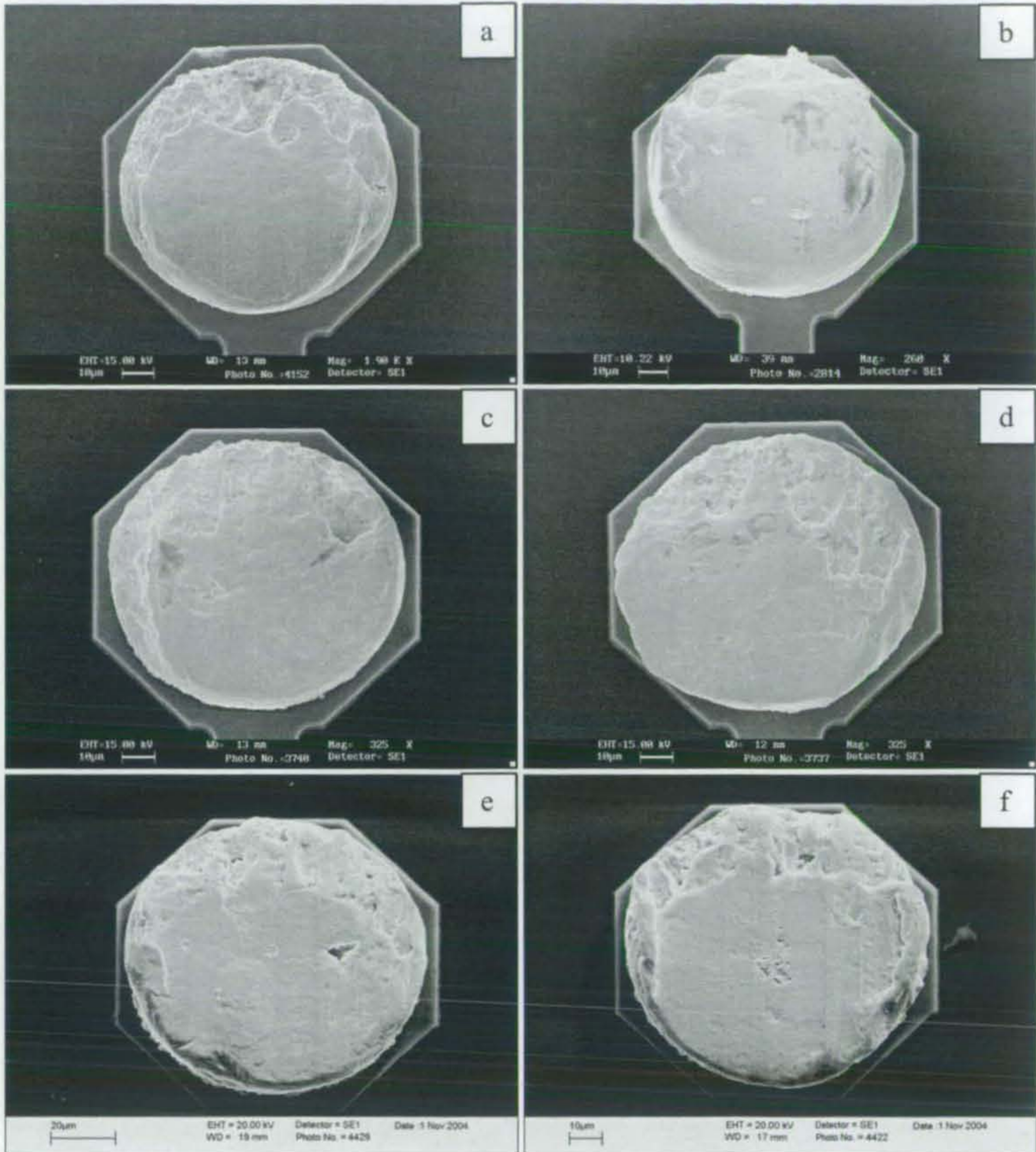


Fig. 7-35 Fracture surfaces of solder bumps after different ageing, a) as reflowed, b) aged 45 d at 80°C, c) aged 10 d at 150°C, d) aged 18 d at 150°C, e) aged 15 d at 175°C and f) aged 30 d at 175°C (shear height 15 μm).

Fig. 6-90 shows that the shear forces of Sn-Ag-Cu solder bumps only dropped after ageing at 80°C for 18 d and Figs. 6-91 and 6-92 b show that the shear force dropped in the initial stage of ageing at 150°C and 175°C. Fig. 7-35 shows the fracture surfaces of solder bumps after ageing at different temperatures. All the solder bumps failed in the bulk solder and showed ductile fractures with the first part of the fracture surface smooth and the later part rough.

Since all the solder bumps fractured in the bulk solder, the $(Cu,Ni)_6Sn_5$ IMC growth and the Kirkendall voids formation did not influence the shear force. As we know, when small hard particles distribute in a soft material, they can strengthen the material. Small Ag_3Sn particles coarsened into large pebble-like phases during ageing (Fig. 7-19), which reduced the strengthening function. It seems that it was the coarsening of Ag_3Sn particles that had caused the shear strength degradation. Because the IMC coarsening at low temperatures was much slower than that at high temperatures, the shear strength decreased much slower during the ageing at 80°C.

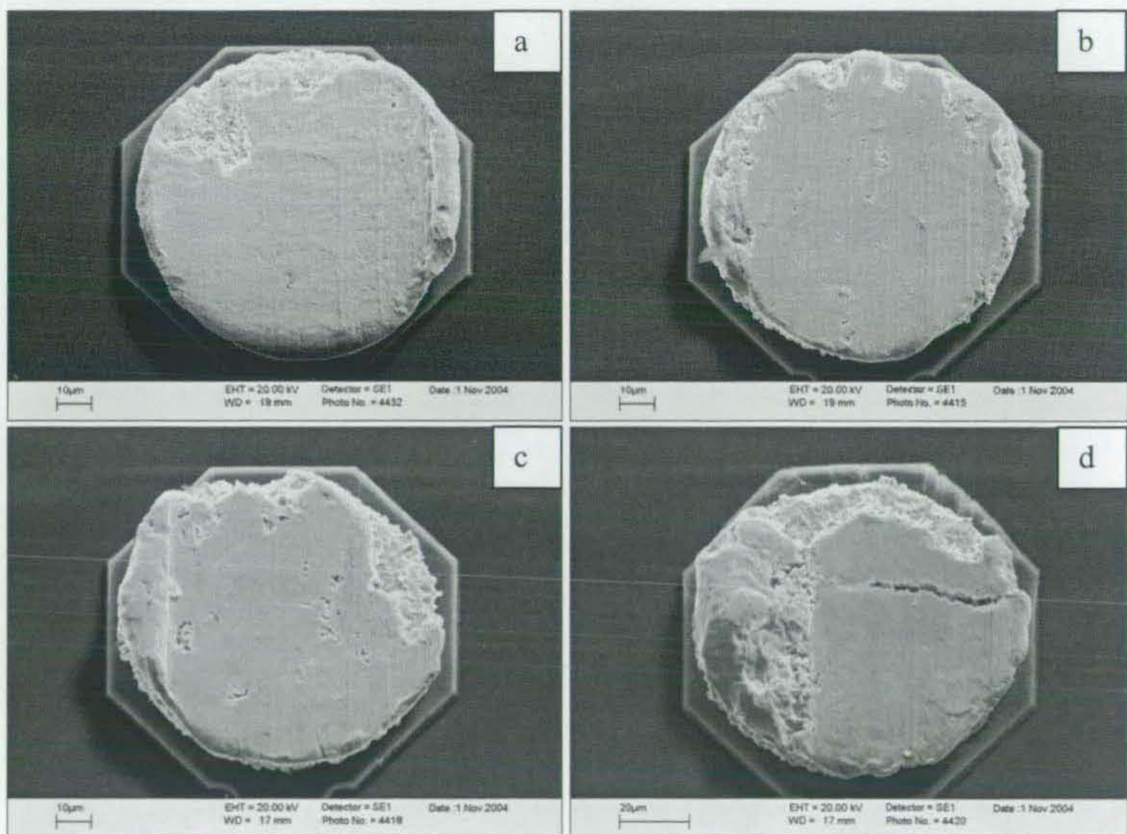


Fig. 7-36 Fracture surfaces of solder bumps after ageing at 175°C for different time, a) 3 d, b) 15 d and c) and d) 30 d. (Shear height 10 μm)

Fig. 6-92a shows that when the shear height was 10 μm the shear strength of solder joints did not change during ageing at 175°C. Fig. 7-36 shows the fracture surface of solder bumps after ageing at 175°C for different periods of time. It can be seen that the fracture surface was in the $(Cu,Ni)_6Sn_5$/solder interface and some of the final failure is brittle failure. Fig. 7-36 d shows that the IMC layer may crack during shear tests due to

its brittleness. Since the strength of this interface did not degrade during ageing and the Kirkendall voids did not form in this region, the shear strength did not decrease during ageing.

7.8 Thermal cycling and reliability

Due to the high CTE mismatch between the PCB (CTE ~ 15.8) and silicon chip (CTE ~ 2.8), the solder joints will be under cyclic stress when they suffer temperature excursions in service, which can affect reliability. Much research has been conducted on the reliability of Sn-Pb and lead free solder joints through thermal cycling or thermal shock [58, 116, 167-178]. Some results showed that the reliability of lead free solder joints was equivalent to or better than that of Sn-Pb solder joints [116, 169], but others showed that the reliability of lead free solder joints was a little poorer [170]. The results of Taguchi et al. [58] showed that the reliability of Sn-Pb and lead free solders depended on the surface finish on the board. When bare Cu and Alpha level Ag were used the reliability of Sn-Pb was better, and when ENIG was used lead free solders had better reliability.

From Figs. 6-93 to 6-95, it can be seen that during thermal cycling the microstructure of solder joints did not change and the growth of IMCs at interfaces was not significant. The dwell time at 125°C was about 15 min in one cycle, such that after 1500 cycles the total time of solder joints at 125°C was about 15 d. At this temperature the diffusion rate of atoms is not high, so the increase of IMC layer thickness was not significant. It can also be seen that due to the immersion Au on the PCB pads, $AuSn_4$ IMCs formed both in the bulk solder and at solder/$(Cu,Ni)_6Sn_5$ and solder/Cu_6Sn_5 interfaces. When the pads with micro-vias were used, more $AuSn_4$ IMCs formed in the solder joints and accumulated at the interfaces.

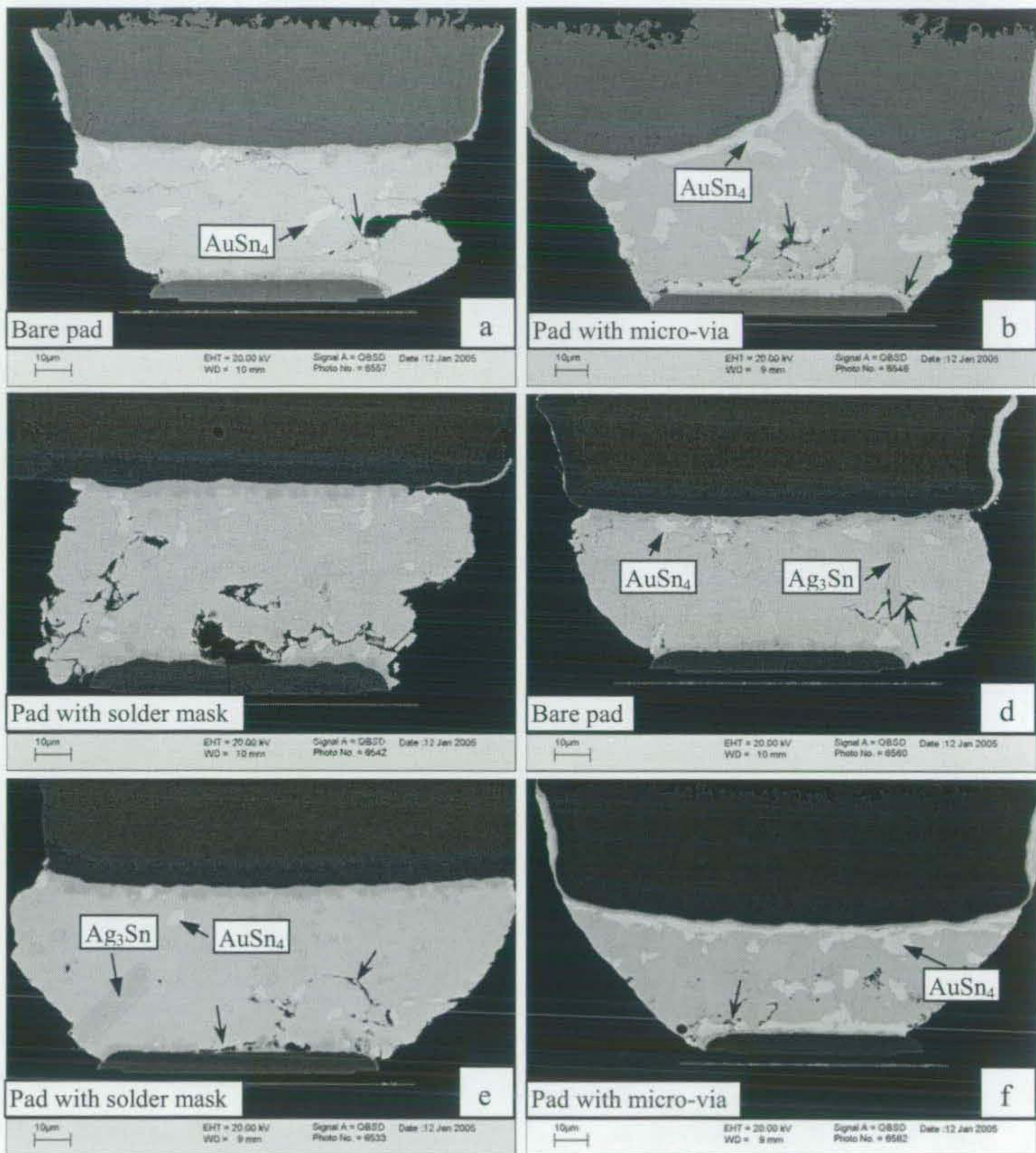


Fig. 7-37 Possible crack initiation positions during thermal cycling, a) sharp points, b) joint corner and $AuSn_4$/solder interface, c) voids and joint corner, d) Ag_3Sn/solder interface, e) poor wetted area and voids and f) $AuSn_4$/solder interface.

Fig. 7-37 shows the possible crack initiation positions in the solder joints during thermal cycling. The main crack initiation positions were the corner of solder joint at the chip side, where the maximum strain normally existed [170, 173]. The cracks may also initiate at $AuSn_4$/solder and Ag_3Sn/solder interfaces (Figs. 7-37b, d and f) due to the high modulus difference, and sharp points, voids and poor wetted areas are the other possible crack propagation positions as shown in Figs. 7-37a, c and e.

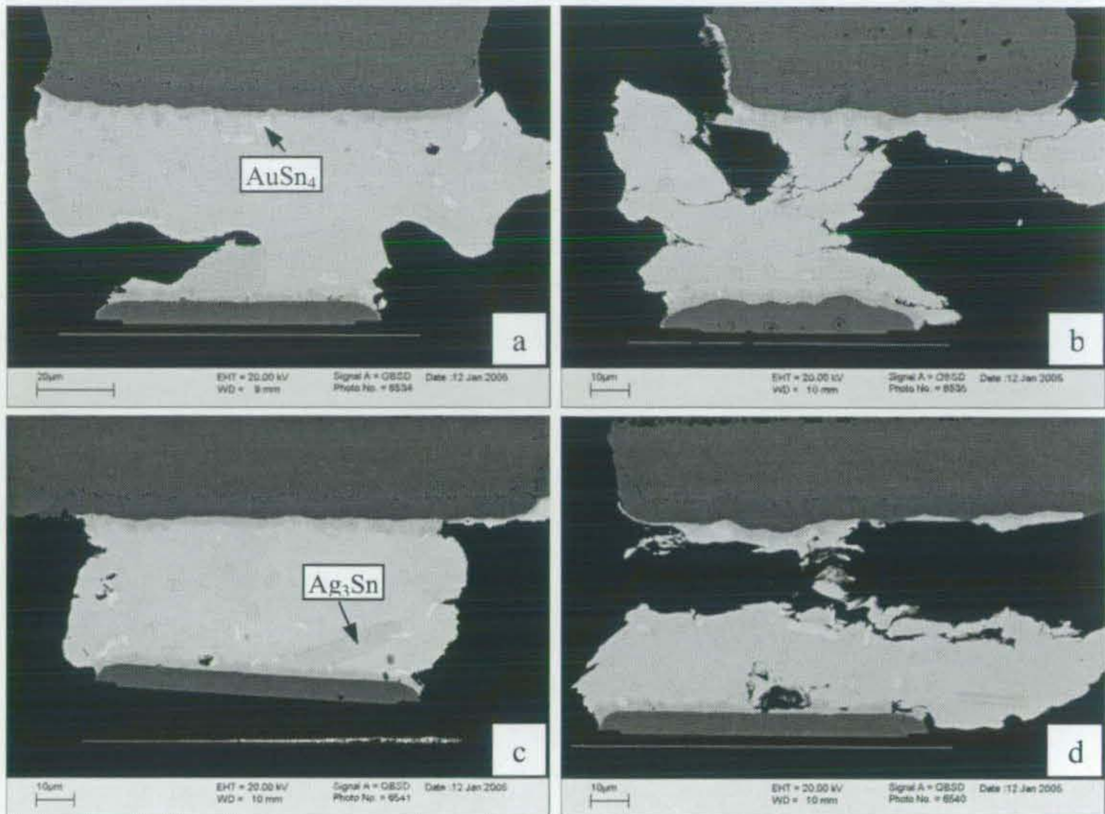


Fig. 7-38 Irregular solder joint shapes after reflow soldering when pads with solder mask were used, a) b) narrow neck, c) UBM lift and d) solder disconnection.

From Tables 6-12 and 6-13, it can be seen that the solder joints with bare pads had the best reliability and the joints formed on pads with micro-vias had the poorest reliability. As we know, solder mask can improve the alignment during assembly. However, it was noticed that the reliability of solder joints with solder mask was poorer than that of solder joints with bare pads. Analysis of the solder joint cross-section after thermal cycling showed that for the pads with solder mask there were some solder joints with irregular shapes, as shown in Fig. 7-38. The solder joints with the narrow necks had greatly degraded strength. It seems that this is the reason for some test couples to fail during thermal cycling. Because underfill particles can be seen at the gaps, these irregular shapes must have formed during assembly. The shape of these solder joints showed that there was a force dragging the board away from the chip during or after the solidification of the solder joint, resulting in the narrow neck or UBM lift. The highest temperature that the PCB material, FR-4, used in this work can resist, is about 240°C for 90 s and in the meantime the maximum reflow temperature for Sn-Ag-Cu solder was

around 240°C. So the board can be overheated during reflow, which will degrade its properties or even cause distortion of the circuit board. If the board is distorted, it will lose its planarity and the distance between some pads and chip will become larger during solidification, which will lift the solder and UBM to form the irregular shapes.

Weibull analysis has been used to predict the reliability of components for decades [167-172]. It often reveals the strengths and weaknesses of all kinds of test structures reliably. The life distribution of solder joints during thermal cycling can be analysed through the two-parameter Weibull cumulative distribution equation:

$$F(t) = 1 - Exp[-(\frac{t}{\eta})^{\beta}] \tag{7-6}$$

where t is cycling time (i.e., number of cycles to failure), η is a scale parameter, which is a characteristic life or cycles to 63.2% fail and β is a shape parameter (the Weibull slope). The scale parameter η and shape parameter β for the pads with micro-via were calculated as 1166 and 1.55 respectively. This analysis was not applied to the solder joints with bare pads and pads with solder mask since insufficient data were collected and some solder joints failed due to the irregular joint shape.

Fig. 7-39 shows the failure modes of solder joints when pads with micro-via were used. It can be seen that the main failure mode was crack propagation along the $AuSn_4$/solder interface and some solder joints may fail in the bulk solder. As mentioned in Chapter 6, the high Au to solder ratio in the solder joints with micro-via caused the formation of a large amount of $AuSn_4$ IMCs. The modulus of $AuSn_4$ and solder material is quite different, so during thermal cycling stress tends to concentrate at their interface, especially when this interface exists at the corner of solder joint, and a crack may initiate and propagate along this interface, resulting in the failure of solder joint.

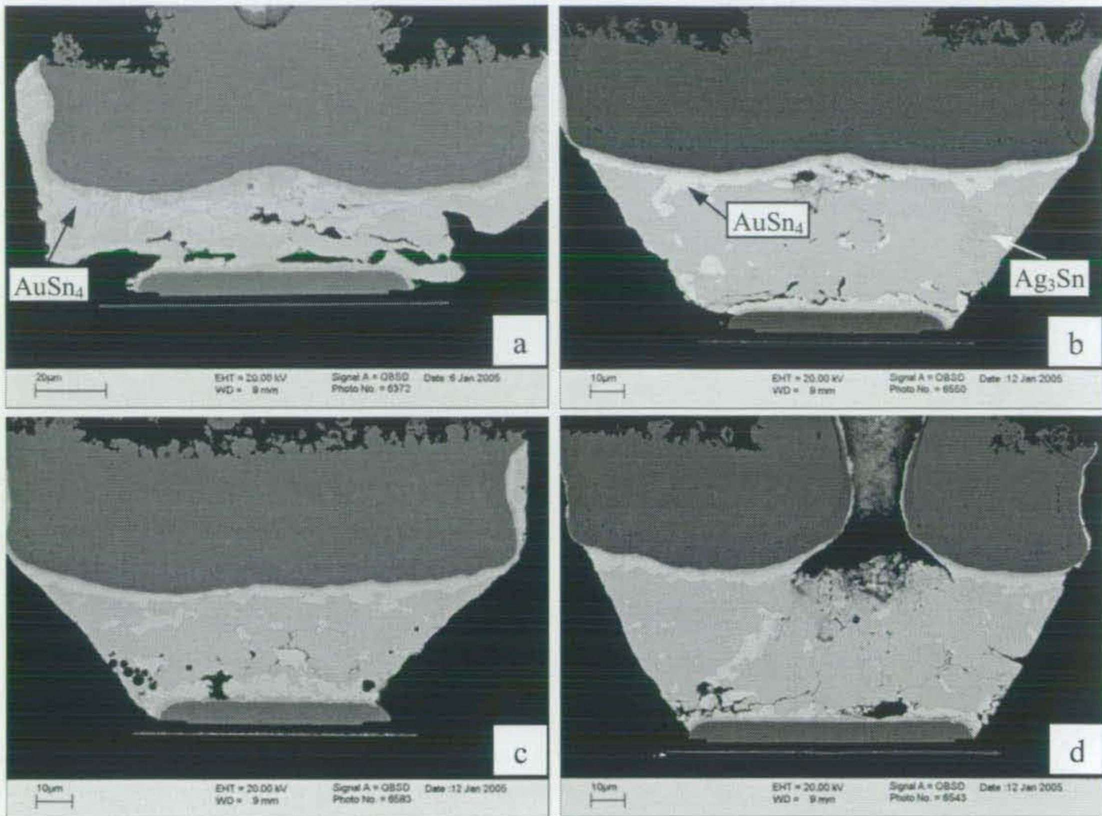


Fig. 7-39 Failure modes of solder joints when pads with micro-via were used, a) b) failure at $AuSn_4$/solder interface, c) failure in bulk solder and d) failure at $AuSn_4$/solder interface and in bulk solder.

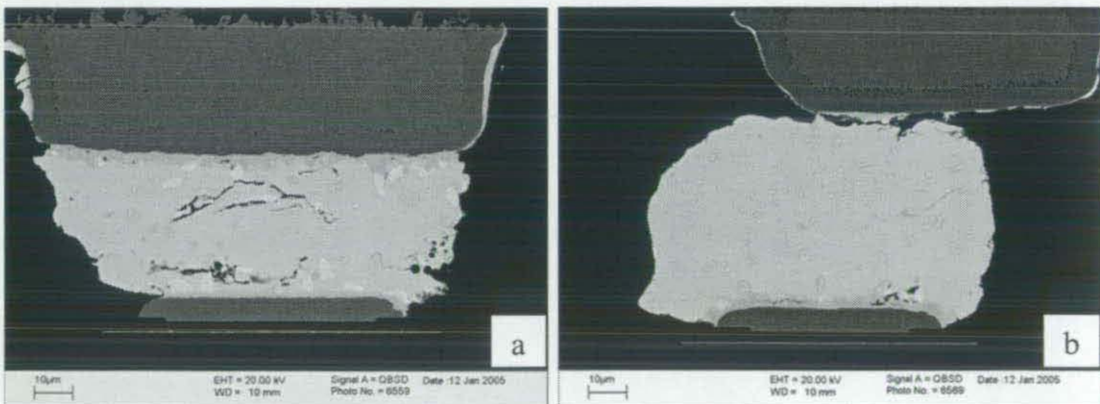


Fig. 7-40 Failure mode of solder joints during thermal cycling when bare pads were used, a) failure in bulk solder and b) failure at poor wetted interface.

Fig. 7-40 shows the failure modes of solder joints when bare pads were used. It can be seen that the main failure mode was crack propagation in the bulk solder and when the

pad did not have good wettability with the solder the fracture might be at the solder/pad interface.

To the solder joints formed on the pads with solder mask, the main failure is in the bulk solder as shown in Fig. 7-42. It is similar to that in the solder joints with bare pads.

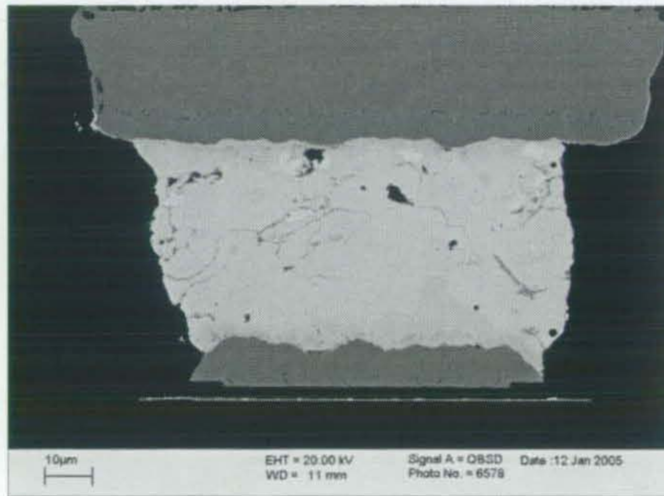


Fig. 7-41 Failure mode of solder joints during thermal cycling when pads with solder mask were used: failure in bulk solder.

When the cracks propagated in the bulk solder, the fracture could be transcrystalline and intercrystalline. Fig. 7-39c and Fig. 7-41 show that sometimes the cracks propagated along the grain boundaries of β-Sn, and grain boundary sliding may be its deformation mechanism.

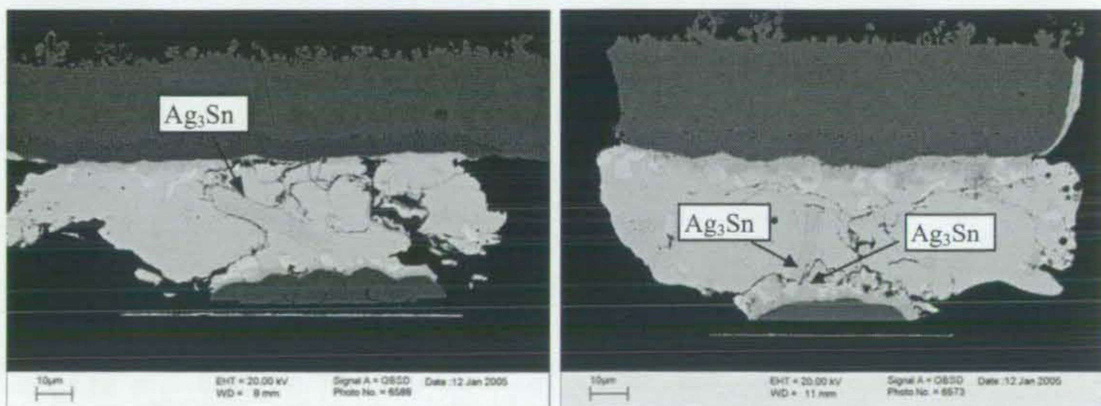


Fig. 7-42 Ag_3Sn IMCs in the way of crack propagation.

The Ag_3Sn/solder interface can be a weak position for a crack to initiate and propagate, as mentioned above and in the literature [176]; however, the Ag_3Sn IMC can change the

direction of crack propagation and increase the path length that cracks have to pass during thermal cycling, as shown in Fig. 7-42, which may improve the reliability of solder joints in some cases.

Some research showed that the delamination at the underfill/chip and underfill/solder interfaces might happen during thermal shock testing [167, 170, 173, 177]. The reason is that the CTE of underfill is higher than that of solder materials and on the cold side of thermal cycling the underfill tries to contract more than the solder material, placing the underfill in tensile stress. However, in this research no underfill delamination was found after 1500 cycles, which is due to the lower ramp rate applied in thermal cycling.

Of fundamental significance here is the long-term reliability of the solder joint, which is directly dependent on the quality of the bond formed between the solder and the pad. With properly designed pads, surface finishes, underfills and UBMs, the lifetime of solder joints under thermo-mechanical stress can be maintained.

7.9 Corrosion properties

Abtew et al. [2] provided a brief review on the corrosion properties of lead free solder in microelectronics. Depending on the application and the environment in service, electronic components may be exposed to corrosion media. In addition, solder alloys are electrically connected with other metals (pads or UBMs) and their potential is different. Table 7-6 shows the standard electromotive force (emf) of metals used in microelectronics. It can be seen that the standard emf of Sn, which is the main element in lead free solder alloys, is lower than that of most metals used for solder pads and UBMs, such as Au, Ag, Cu and Pd. This will cause the galvanic corrosion of solder alloys. In the mean time, the halide-containing contaminations during assembly, such as conventional fluxes, can also degrade the corrosion resistance of solder joints [25]. Lin and Liu [179] studied the corrosion behaviour of Al-Zn-Sn solders in NaCl solution, and the results showed that the solders had significant galvanic current densities with respect to electroless Ni-P, electroless Ni-Cu-P and Cu. It shows that if Al-Zn-Sn solders are connected with these materials corrosion will happen to the solders. When the electrochemical behaviour of Sn-In-Ag alloys in 3% NaCl solution was studied,

Oulfajrite et al. [180] found that the content of In did not influence the corrosion of solder alloys significantly, but the increase of Ag addition can increase the corrosion resistance. Lin et al. [70] also studied the corrosion resistance of XIn-9(5Al-Zn)-Sn solders in 3.5% NaCl solution, and their results showed that more In addition can slightly increase the corrosion resistance.

Table 7-6 Standard electromotive force (emf) of metals used in microelectronics.

Metal	**Standard emf (V)**	**Metal**	**Standard emf (V)**
Au	+1.50	Sn	-0.136
Ag	+0.799	Pb	-0.126
Cu	+0.337	In	-0.342
Ni	-0.250	Zn	-0.763
Pd	+0.987	Al	-1.66

In this research, the corrosion resistance of lead free and Sn-Pb solders was studied in 3.5% NaCl solution, whose content is similar to that of seawater. Figs. 7-43 and 7-44 show that the corrosion current density of these solders was similar and stable passivation films formed on all the Sn-Pb and lead free solders, which can protect the solders and increase their corrosion resistance. The passivation properties of these solders are summarized in Table 7-7. Lead free solders had a lower passivation current density and larger passivation domain than Sn-Pb solder. This means that when passivation films form on the surface of solder materials the films on the lead free solders were more stable than that on Sn-Pb solder and the corrosion current densities of lead free solders were smaller than that of Sn-Pb solder. In the mean time, after the passivation film broke down, the corrosion current density of three lead free solders was also smaller than that of Sn-Pb solder. All these indicated that the lead free solders had a better corrosion resistance than Sn-Pb in 3.5% NaCl solution. The results also show that the corrosion resistance of Sn-Ag and Sn-Cu solders was a little better than that of Sn-Ag-Cu solder because of the lower passivation current density and larger passivation domain.

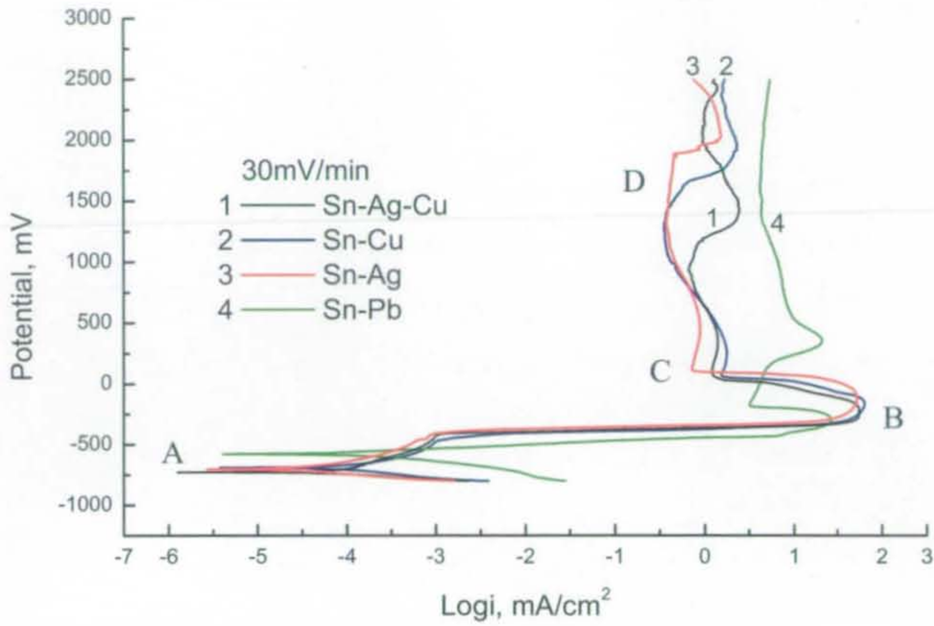


Fig. 7-43 Comparison of potentiodynamic polarization curves of different solder materials with the scanning rate 30 mV/min.

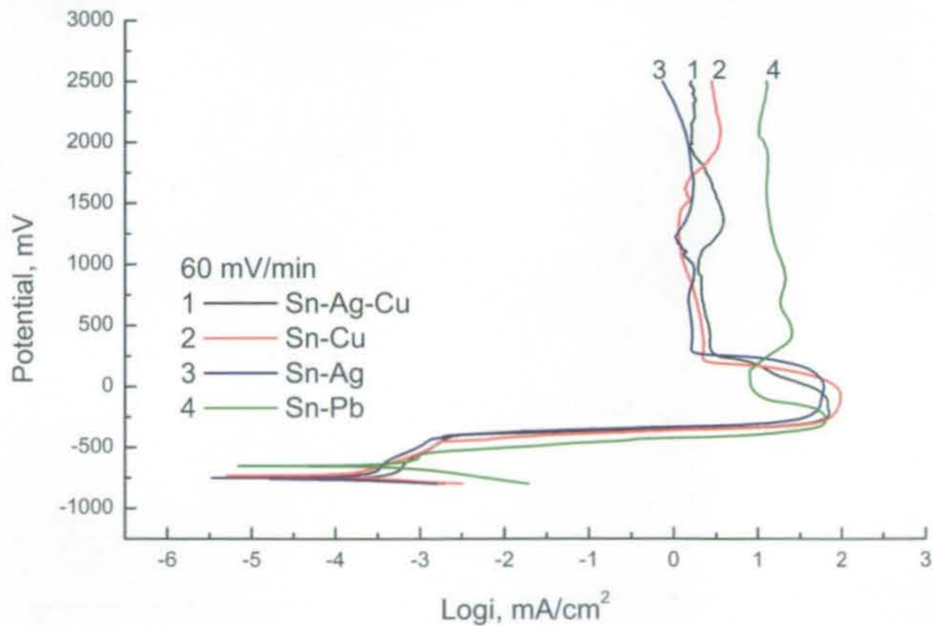


Fig. 7-44 Comparison of potentiodynamic polarization curves of different solder materials with the scanning rate 60 mV/min.

Table 7-7 Passivation properties of Sn-Pb and lead free solders.

Solders	Passivation current density (mA/cm^2)		Passivation domain (mV)	
	30mV/min	60mV/min	30mV/min	60mV/min
Sn-Pb	4.17	8.10	368	265
Sn-Ag	0.49	1.58	1766	927
Sn-Cu	0.74	1.62	1560	1442
Sn-Ag-Cu	1.07	2.24	1089	797

In order to understand the reactions during the corrosion, EDX and XRD were used to analyse the corrosion products on the surface after the potentiodynamic polarization tests. Figs. 7-45 and 7-46 show the EDX and XRD analyses of the corrosion products on the surface of lead free and Sn-Pb solder materials after the potentiodynamic polarization testing with the scanning rate 300 mV/min, respectively. They show that all the lead free and Sn-Pb solder materials had the same corrosion product, $Sn_{3+2}O(OH)_2Cl_2$, which is the oxide, hydroxide and chloride of Sn. Fig. 7-47 shows the XRD analyses of the corrosion products on the surface of Sn-Ag-Cu solder material after the potentiodynamic polarization testing with the scanning rate 30 mV/min. It shows the same corrosion product as that after the potentiodynamic polarization testing with the scanning rate 300 mV/min.

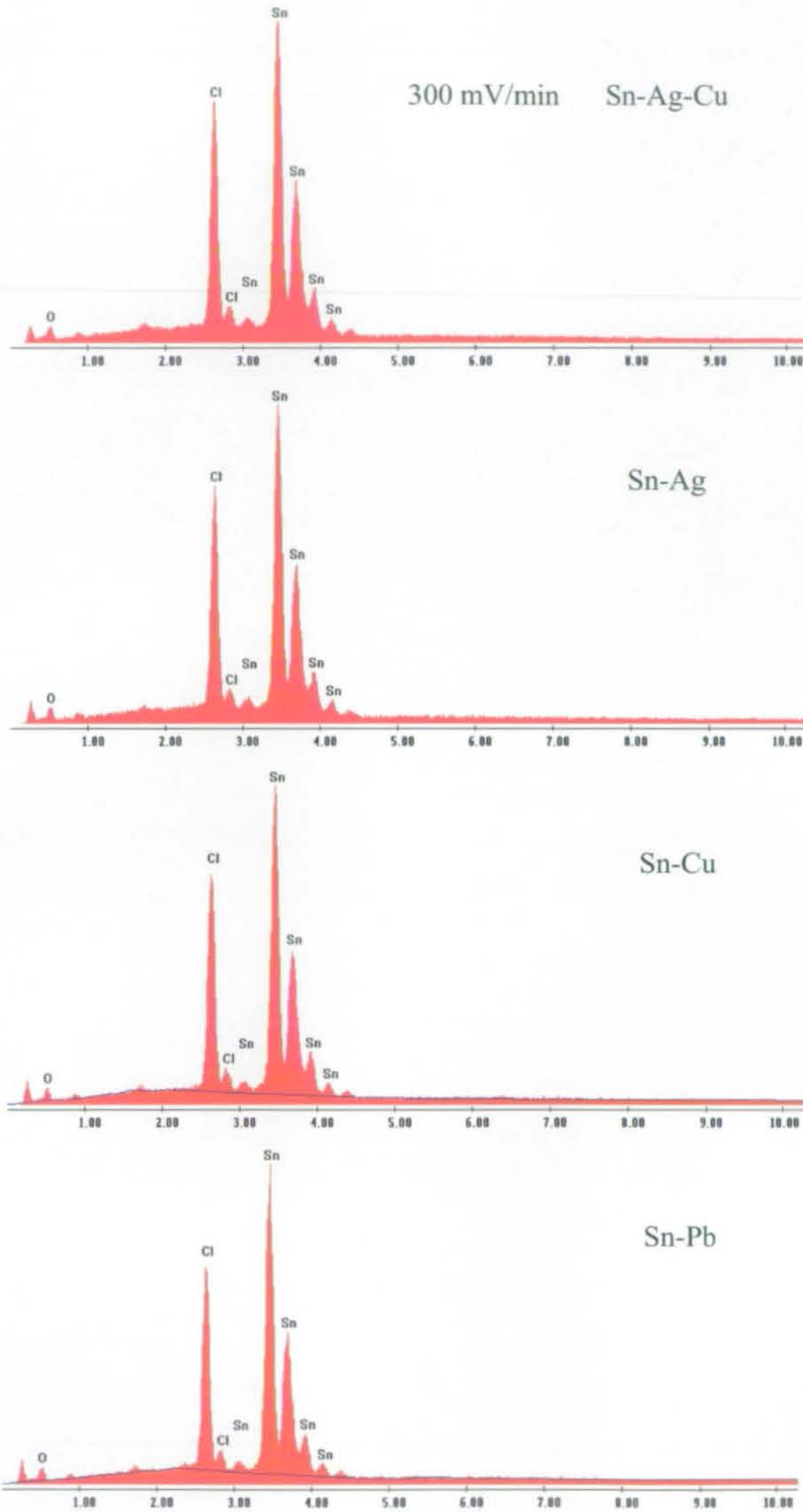


Fig. 7-45 EDX spectrum of different solder materials after the corrosion tests with the scanning rate 300 mV/min.

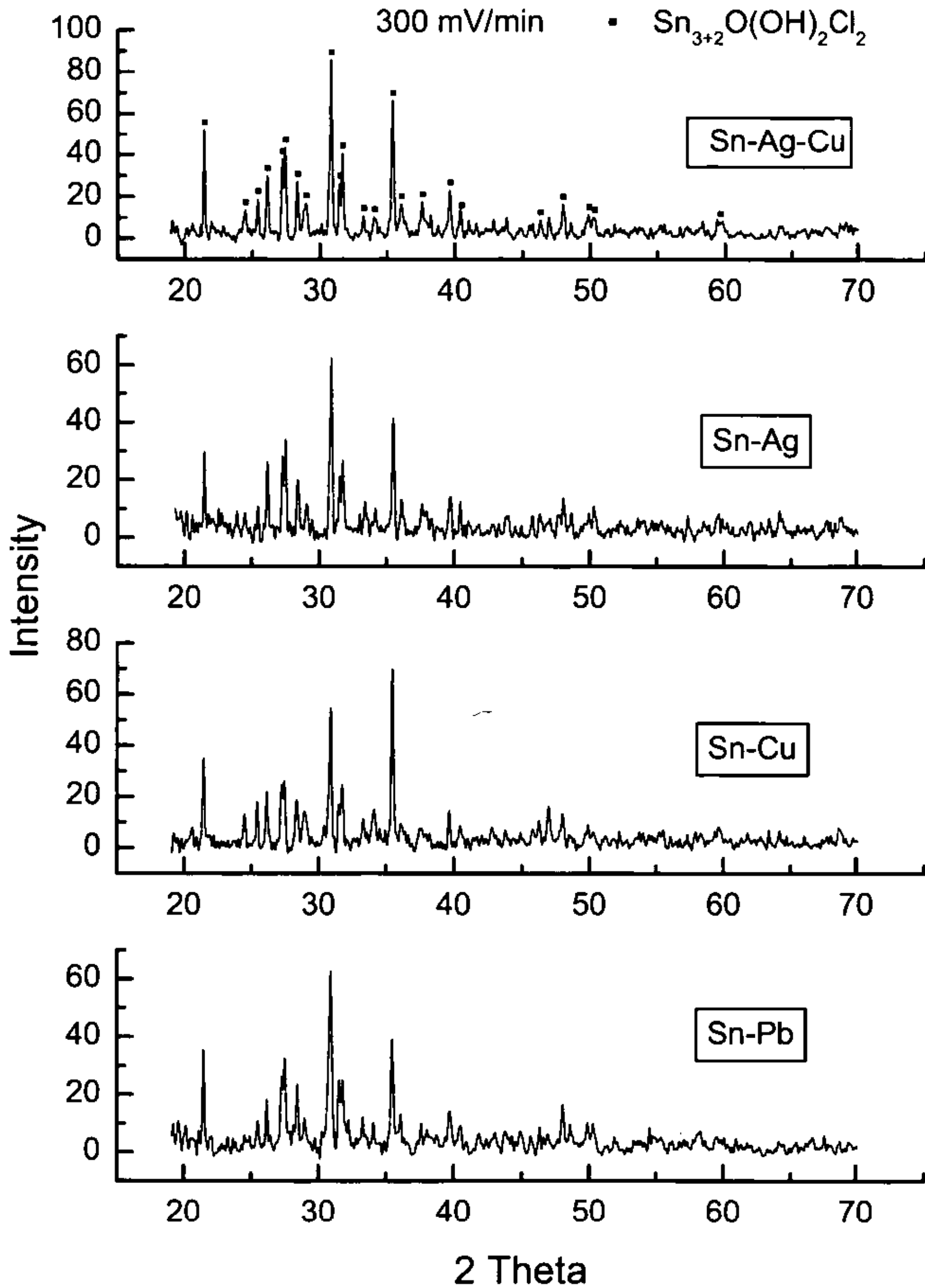


Fig. 7-46 XRD spectra of different solder materials after the corrosion tests with the scanning rate 300 mV/min.

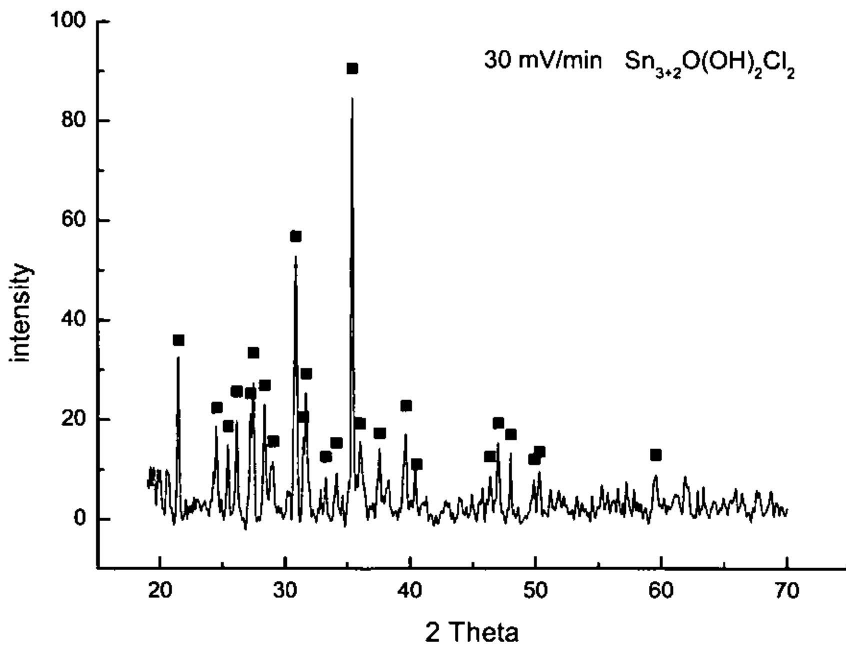


Fig. 7-47 XRD spectra of Sn-Ag-Cu solder after the corrosion tests with the scanning rate 30 mV/min.

During the potentiodynamic polarization testing, the initial reaction that happened on cathodic electrode was the oxygen absorption:

$$O_2 + 4e^- + 2H_2O \rightarrow 4OH^- \qquad (7\text{-}7)$$

When the current density reached about 10 mA/cm^2, many hydrogen bubbles came out from the cathodic electrode, which is because the hydrogen ions were absorbed on the cathodic electrode and reduced into hydrogen gas:

$$2H^+ + 2e^- \rightarrow H_2 \qquad (7\text{-}8)$$

The reactions on the anodic electrode during the polarization from point A to B, as shown in Fig. 7-44, are an active process, in which Sn in the solder materials dissolved into solution and formed $Sn(OH)_2$:

$$Sn + 2OH^- - 2e^- = Sn(OH)_2 \qquad (7\text{-}9)$$

When the polarization reached point B, a passivation film began to form on the surface:

$$Sn(OH)_2 + 2OH^- - 2e^- = Sn(OH)_4 \qquad (7\text{-}10)$$

Because $Sn(OH)_4$ is highly insoluble, when it precipitates on the solder surface it can inhibit the corrosion of solders. In the mean time, $Sn(OH)_2$ on the solder surface may dehydrate into SnO:

$$Sn(OH)_2 = SnO + H_2O \quad (7\text{-}11)$$

In NaCl solution, the chloride ion (Cl^-) has a large atomic radius and is weakly solvated, such that it can be absorbed on the surface of solders, resulting in the breakdown of the passivation film [180]. When the chloride ion was absorbed on the solder surface a chloride of Sn might form as a corrosion product. All these reactions made the corrosion products a mixture of the oxide, hydroxide and chloride of Sn.

Although the main element of Sn-Pb and lead free solders was Sn and all corrosion happened on Sn, the addition of other elements can still influence the corrosion resistance of solders. Results showed that the main effects were on the formation and stability of passivation films on the solders during corrosion. It seems that Pb is detrimental to the passivation of solder materials.

CHAPTER 8

Conclusions and Future Work

In this chapter, conclusions are drawn from the results and discussion presented in Chapters 6 and 7, and further research is required to further extend the understanding of lead free flip chip application.

Lead free solders have to replace Sn-Pb solders in electronic industry by July 2006 in Europe, and a lot of work still needs to be done to further enrich the knowledge base and satisfy the needs and requirements from industry.

The contributions of this work to the application of lead free solders in flip-chip scale packages are briefly stated here with contextual relevance and further elaborated upon in the following subsections:

- The wettability of EN coatings with lead free solders without the protection of immersion Au was studied with different storage durations and environment, and results show that storage durations and environment do not influence the wettability of EN coating with lead free solders significantly; however, strong flux and nitrogen protection are required to ensure the good wettability of EN coating. For an end-user, this is important in that it provides a guideline for the use and storage of EN UBM in production applications.
- Microstructures, morphologies, distributions and micro-mechanical properties of different phases in solder joints were studied. This information enhances the understanding of solder joint robustness and may also support finite element

modelling (FEM), which helps industry in addressing the potential reliability issues for Pb-free solder joints.

- The influence of cooling rates on the size of IMCs was studied and fast cooling during reflow was recommended because this produces a finer grained solder joint microstructure and more beneficial IMC morphology, thereby optimising the process set-up for longer term reliability performance.
- Interfacial reactions and shear tests were conducted for Sn-3.8Ag-0.7Cu/EN flip chip solder bumps after thermal ageing, and results show that solder/IMCs and IMCs/EN interfaces are stronger than bulk solder and thermal ageing does not degrade the shear strength of solder bumps significantly. Such information assures the manufacturer and end-user that these new materials systems have not resulted in particularly weak areas at joint interfaces and the weakest point is the solder itself.
- Interfacial reactions between different lead free solders and substrates were studied, which have provided criteria to allow end-users and manufacturers to better select solder and substrate for optimised reliability.
- Kirkendall voids were observed in Ni_3P and Cu_3Sn layers during high temperature ageing, and their possible formation mechanisms were proposed. This indicates a possible route to a failure mechanism and such understanding allows the avoidance of such failures by the adjustment of the metallurgy such that these voids cannot occur.
- Nanoindentation was used to study the mechanical properties of different phases in solder joints with a Berkovich indenter; however, a flat punch is suggested to replace the Berkovich indenter for creep testing. As such, as a research instrument, the nanoindentation technique, specifically the indenter geometry, should be optimised to obtain the desired properties the user wishes to get.
- Shear tests show that coarsening of Ag_3Sn IMCs can degrade the shear strength of solder joints during thermal ageing. These IMCs and their evolution overtime may serve as indicators of the joint reliability in a system.
- Results from thermal cycling tests of Sn-Ag-Cu solder joints show that the application of micro-vias should be considered very carefully, due to relatively large Au/solder ratio and the requirement for a larger volume of solder and, that high T_g PCBs need to be used with lead free solders to ensure a good reliability.

This allows the optimisation of micro-via design, specifications for solder alloy and its quantity, and the selection of suitable PCBs for these high temperature soldering alloys.

- Lead free solder have been shown to have better corrosion resistance than Sn-Pb solders in NaCl solution. As such, if the components after assembly have good hermeticity, corrosion issues with lead free solder will be less significant than they have been for Sn-Pb solders, which assures better reliability in corrosive environments and specific maritime applications (e.g. military, defence, aviation, naval and telecommunications sectors).

The following sections address the detailed academic findings supporting the above conclusions and their relevance.

8.1 Wettability of EN coatings with lead free solders

1. The P content of EN coating in the procedure used was about 7.3wt.%. The lead free solders, Sn-3.5Ag, Sn-0.7Cu and Sn-3.8Ag-0.7Cu, did not wet the EN coating when a weak flux was used, but had good wettability when a strong flux was used. Nitrogen protection can improve the wettability of EN coating and the oxygen concentration needs to be lower than 210 ppm.
2. Storage time and environment did not significantly influence the maximum wetting force of EN coating, but strong flux and nitrogen protection had to be used. When the samples were stored in a freezer, the maximum wetting force and time to wet did not change with the storage time; however, when the samples were stored in a lab ambient environment, time to wet increased with the storage time. It seems that the oxidation film was thicker when the samples were stored in a lab ambient environment and needed more time to be removed by strong flux. Results show that when strong flux and nitrogen protection are used an EN UBM can be stored for long periods and still possesses good solderability without the requirement for an immersion gold protection.
3. The oxygen content on the surface of EN coating increased during storage, which meant the EN coating was continuously oxidized. The surface of the EN

coating had a higher P content than the bulk, which might be caused by the formation of nickel phosphate and phosphite (NiH_xPO_y) on the surface.

4. An EN coating on Al with low surface roughness had better wettability when the dipping (spreading) direction was perpendicular to the polishing or rolled tracks, and the EN coatings had better wettability when the spreading direction was parallel to the polishing or rolled tracks than when the spreading direction was perpendicular to the polishing or rolled tracks.

8.2 Microstructures of lead free solders

1. The microstructures of bulk lead free solders, Sn-3.5Ag, Sn-0.7Cu and Sn-3.8Ag-0.7Cu, were β-Sn matrix with distributions of small IMC particle. The IMC particles in Sn-0.7Cu were much smaller than those in Sn-3.5Ag and Sn-3.8Ag-0.7Cu. β-Sn grains had different orientations with different optical contrasts.
2. Rapid cooling could reduce the IMC size in bulk solders and solder joints. The influence of cooling media on the IMC size in solder joints was much less promounced than that for bulk solders due to the small volume of solder joints.
3. $(Cu,Ni)_6Sn_5$ IMCs were facet-like phases and Ag_3Sn IMCs existed in the solder joints as small particles around the β-Sn dendrites or lamella- or plate-like phases. The plate-like phase was the most common morphology of Ag_3Sn IMCs followed by the small particles and plates.
4. Plate-like Ag_3Sn IMCs tended to grow from the bottom of solder bumps and many voids formed in the $(Cu,Ni)_6Sn_5$ IMC layer and at the $(Cu,Ni)_6Sn_5$/solder interface.

8.3 Interface reactions

1. The main IMC layer at Sn-Ag-Cu/EN interface was confirmed as $(Cu,Ni)_6Sn_5$ and the IMC in the bulk solder was Ag_3Sn.
2. The $(Cu,Ni)_6Sn_5$ IMC growth is diffusion-controlled and the IMC thickness increase is proportional to the square root of ageing time with the growth activation energy about 0.59eV. The IMC growth at high temperatures was

much faster than that at low temperatures. No de-wetting was observed during the ageing due to the low consuming rate of EN UBM.

3. During high temperature ageing, the $(Cu,Ni)_6Sn_5$ IMC facets become larger and the IMC layer becomes thicker and more compact. It is proposed that the small Ag_3Sn particles coarsen, and the plate- and lamella-like phases break up and then coarsen into pebble-like phases during high temperature ageing. The Ag_3Sn coarsening took place at the initial stage of high temperature ageing and the particles size did not change significantly during further ageing.
4. It has been also proposed that Kirkendall voids, formed in the Ni_3P layer above the EN UBM during high temperature ageing, is attributed to the faster diffusion of Ni in the Ni_3P layer via its columnar structure boundaries, causing a net Ni diffusion out of the Ni_3P layer.

8.4 IMCs formed with different solders and substrates

1. When the substrates were Cu or CuImAg, the IMCs formed at the interface had two layers with Cu_3Sn next to substrate and Cu_6Sn_5 next to solder. The formation of Cu_3Sn is due to the slow diffusion rate of Sn and Cu in the Cu_6Sn_5 IMC, and the growth of Cu_3Sn will consume some of Cu_6Sn_5 IMC in the initial stage. The growth of Cu_6Sn_5 was a result of growth competition with Cu_3Sn. When the substrates were EN or ENIG, for Sn-3.5Ag solders the IMCs formed at the interface was Ni_3Sn_4 and for Sn-3.8Ag-0.7Cu and Sn-0.7Cu solders the IMCs formed at the interface was $(Cu,Ni)_6Sn_5$.
2. The growth of Cu_6Sn_5 was faster than that of $(Cu,Ni)_6Sn_5$ and Ni_3Sn_4. During interfacial reactions, the formation of Ni_3Sn_4 would consume much more Ni than that of $(Cu,Ni)_6Sn_5$. A small addition of Cu into Sn-Ag solder can solve this problem when EN UBM is used.
3. At the interface, the $(Cu,Ni)_6Sn_5$ IMCs formed were needle- or facet-like phases and the Cu_6Sn_5 and Ni_3Sn_4 IMCs were facet-like phases. In the solder, the Cu_6Sn_5 IMCs had prism-like shapes with some of them appearing hollow and the Ag_3Sn IMCs existed as plate- or pebble- or needle-like phases.
4. When an EN or ENIG substrate was used, Kirkendall voids formed inside the Ni_3P layer, except when Sn-3.8Ag-0.7Cu reacted with EN substrate. When a

CuImAg substrate was used, Kirkendall voids formed inside the Cu_3Sn layer. The formation of Kirkendall voids in Cu_3Sn layer is related to the immersion Ag, but the detailed reason is still unclear.

5. The IMCs formed in the solder joints are brittle, and when their size becomes large they are easily broken by an externally applied force.

8.5 Micro-mechanical properties

1. Al or Cu has quite different mechanical properties compared to the Si and EN coating at the interfaces, and Sn-Ag-Cu solder had quite different mechanical properties compared to the IMCs.
2. Assembly and thermal ageing did not change the mechanical properties of phases in the solder joints significantly.
3. The mechanical properties of lead free solders decreased significantly with an increase in temperature. The related modulus and hardness of IMCs from nanoindentation tests decreased as well, which is contributed to the mechanical degradation of solders at high temperatures.
4. The indentations in lead free solders showed some 'pile-up' and those in IMCs showed 'sink-in', although the degree of sink-in was insignificant.
5. Solder volume and cooling rate did not influence the mechanical properties of the phases in solders significantly.

8.6 Creep properties

1. Sn-3.5Ag, Sn-0.7Cu and Sn-3.8Ag-0.7Cu lead free solders had similar creep properties and solder volume did not influence the creep property significantly.
2. A distribution of small particles in lead free solders can increase their creep property through dislocation climb. Creep exponents showed that the creep testing with nanoindentation at room temperature presented in a high stress regime and the creep testing at high temperatures (125°C, 150°C and 175°C) presented in a low stress regime.

3. When nanoindentation is used for creep testing, a flat punch is recommended other than sharp indenters because creep with sharp indenters cannot easily reach a steady state condition due to the decreasing of loading stress.

8.7 Shear strength

1. For the ASH wafer solder bumps, when the shear height was 10 μm, solder bumps failed in bulk solder and at solder/IMC interfaces, and the failure of solder bumps exhibited mixture of ductile and brittle fracture. When the shear height was higher than 10 μm, solder bumps failed in bulk solder, and the failure of solder bumps was solely ductile fracture. When the shear height was lower than 25 μm and higher than 10 μm the first part of the fracture surface is smooth and the later part is rough.
2. The shear force of solder bumps increased both with the increase of shear speed and with the decrease of shear height. Cooling regimes did not influence the shear strength of solder bumps significantly.
3. When the shear height was 15 μm, the shear strength of solder bumps decreases after 20 days ageing at 80°C; however, it decreases at a much earlier stage during ageing at 150°C and 175°C. The coarsening of Ag_3Sn particles in the solder caused a decrease of shear strength during high temperature ageing, but this influence was not significant. When using the shear height of 10 μm, the shear strength of solder bumps did not change during the ageing at 175°C.

8.8 Thermal cycling and reliability

1. After assembly, $AuSn_4$ IMCs formed both in the bulk solder and at the interface, due to the immersion Au finish on the board side. $AuSn_4$ IMCs formed in the solder joints on the pads with micro-via were in greater abundance than those formed in the solder joints on bare pads or pads with a solder mask.
2. IMC growth during thermal cycling was not significant.
3. During thermal cycling, the cracks may initiate at $AuSn_4$/solder and Ag_3Sn/solder interfaces, the sharp points, voids and poor wetted areas.

4. The solder joints on bare pads had the best reliability and those on pads with micro-via showed the poorest. The poor reliability of solder joints on pads with a solder mask might be caused by board distortion during reflow.
5. The main failure position was at the $AuSn_4$/solder interface on the chip side for the solder joints on the pads with micro-via, and some other failure was present in the bulk solder. For the solder joints on bare pads or pads with solder mask, the possible failure position was in the bulk solder, and for the solder joints on bare pads another failure position could be at the solder/pad interface due to misalignment and poor wetting.

8.9 Corrosion properties

1. When passivation films formed on the surface of solders, lead free solders had better corrosion resistance than Sn-Pb solder in 3.5wt.% NaCl solution, due to the lower passivation current density, lower corrosion current density after the breakdown of passivation film and more stable passivation film on the surface.
2. The corrosion resistance of Sn-3.5Ag and Sn-0.7Cu was a little better than that of Sn-3.8Ag-0.7Cu.
3. The corrosion products on the solders after potentiodynamic polarization tests in 3.5wt.% NaCl solution were a mixture of the oxide, hydroxide and chloride of Sn. They were the same for different lead free and Sn-Pb solders at different scanning rates.

8.10 Suggestions for future work

8.10.1 Influence of size, morphology and distribution of Ag_3Sn IMCs

In this research, the size, morphology and distribution of Ag_3Sn IMCs have been studied and it was shown that the coarsening of Ag_3Sn IMCs during ageing can degrade the shear strength of Sn-3.8Ag-0.7Cu solder bumps. However, because the formation of Ag_3Sn IMCs is very complicated, i.e., different sizes and morphologies can exist in different solder bumps on the same chip, it is difficult to determine the influence of size and distribution on mechanical properties and reliability.

Modelling is a useful method that can be used to penetrate these complicated issues, since each possibility can be studied individually. In addition, other information can be obtained from modelling, such as distributions of stress, strain and temperature. Some researchers have studied the influence of thickness and morphologies of $(Cu,Ni)_6Sn_5$ IMCs on the mechanical properties of Sn-Ag-Cu solder joints, both from experiments and modelling [129, 156, 158, 166, 181, 182], and this research has shown that the thickness increase of $(Cu,Ni)_6Sn_5$ IMCs did not influence the shear strength of Sn-Ag-Cu solder bumps during ageing. However, few researchers have studied the influence of size, morphology and distribution of Ag_3Sn IMCs on the mechanical properties and reliability of solder joints through modelling.

Based on the mechanical properties obtained here through nanoindentation and the observed morphologies and distributions of Ag_3Sn IMCs in Sn-Ag-Cu solder bumps, the influence of Ag_3Sn IMCs on the properties of solder joints could be simulated. Due to the complicated morphologies of Ag_3Sn IMCs, a substantial 3D model is required and the construction of such a model is a significant challenge in itself. However, such a model would provide a basis upon which the process, alloy, substrate and life time issues could be explored concurrently and as such lead to an optimisation of the Pb-free solder joint design and manufacturing route.

8.10.2 Influence of surface finishes and pad size

During the migration of solder materials from Sn-Pb to lead free, the surface finishes on the board needs to be lead free as well. One of the purposes of a surface finish is to control the surface reactions and improve the pad solderability. There are several kinds of surface finishes available in PCB manufacturing, such as organic preservatives, immersion Ag, immersion Sn and immersion Au. Some research has been done regarding the influence of surface finishes on the properties of solder joints, but few have studied and compared this influence systematically. There are three areas in which this work has identified to further the optimisation of alloy, substrate and process. These are as follows:

Substrate vs. Alloy vs. Size/Geometry effects

In this research, the interface reactions between different lead free solders and different substrates have been studied. However, the size effects and shear strength of these solder bumps have not been studied. The size and volume influence is an issue that causes concern for electronics manufacturers.

In order to understand the influence of pad size and surface finish on the properties of solder bumps on a board, a test board and relevant stencil with different pad sizes can be designed and different surface finishes, including immersion Ag, immersion Sn, electroless Ni and electroless Ni immersion Au, can be used for the pads. The volume of surface finish will affect the amount and size of IMCs formed in the solder bumps during interfacial reactions, so different thicknesses of immersion Ag, Sn and Au would be deposited on the pads. This research has already shown that the amount of $AuSn_4$ IMCs formed in the solder joints is critical and control of the immersion Au/solder ratio becomes very important.

Avoidance of Kirkendall voids: Substrate vs. Alloy vs. Process and Ageing

This study has shown that when immersion Ag on Cu is used as the surface finish, many Kirkendall voids form in Cu_3Sn layer but no Kirkendall voids can be found when bare Cu pads (99.9%) are used. It seems that the formation of Kirkendall voids in a Cu_3Sn layer is related to surface finishes on the Cu. The research of Laurila et al. [130] showed that the purity of Cu influenced the formation of Kirkendall voids. With pure Cu, no Kirkendall voids could be observed under SEM inspection; however, when electrochemically deposited Cu and Cu-laminate with chemical Cu deposition were used, Kirkendall voids can be detected. It was noticed that the Cu coatings mentioned above contained various amount of impurities. From this point of view, the trace elements from surface finishes may exist in Cu_3Sn layer as an impurity and stimulate the formation of Kirkendall voids. Further investigation is needed to study the influence of surface finishes on the formation of Kirkendall voids, and as such to avoid the formation of these voids.

Minimising the influence of PCB materials: Substrate vs. Process

The melting temperature of lead free solders is much higher than that of eutectic Sn-Pb solder, resulting in an even higher reflow temperature, which might not be compatible with the current infrastructure. The highest temperature that a low T_g FR-4 can survive in an air atmosphere is about 230°C for 90 s. This research has shown that a PCB made from low T_g FR-4 material can become overheated easily during reflow and result in the deformation of board during processing and the early failure of the solder joints. In order to avoid this kind of problem and improve the reliability, a high T_g PCB should be used. A systematic study of substrate and lead free solders for optimisation of substrate properties (e.g. percentage glass fibre weave, resins etc.) and behaviour during different reflow processes (inert vs. normal atmosphere, heating and soaking times and cooling curves) is valuable at this time.

References

1. Lau, J.H., *Low cost flip chip technologies*. 2000, New York: McGraw-Hill.
2. Abtew, M. and G. Selvaduray, *Lead-free solders in microelectronics*. Materials Science and Engineering, R: Reports, 2000. **27**: p. 95-141.
3. *Directive 2002/95/EC of the European Parliament and the Council, 'The restriction of the use of certain hazardous substances in electrical and electronics equipment'*. RoHS Directive, 2000/0159 (COD) C5-0487/2002, LEX 391, PE-CONS 3662/2/02 Rev 2, ENV581, CODEC 1273, 2003.
4. Lau, J.H. and S.W.R. Lee, *Chip scale package*. 1999, New York: McGraw-Hill.
5. Lau, J.H., *Flip chip technologies*. 1996: McGraw-Hill.
6. Qi, G., X. Chen, and Z. Shao, *Influence of bath chemistry on zincate morphology on aluminum bond pad*. Thin Solid Films, 2002. **406**(1-2): p. 204-209.
7. Hutt, D.A., et al., *Electroless nickel bumping of aluminium bondpads--part I: surface pretreatment and activation*. IEEE Transactions on Components and Packaging Technologies, 2002. **25**(1): p. 87-97.
8. Hutt, D.A., et al., *Electroless nickel bumping of aluminium bondpads--part II: electroless nickel plating*. IEEE Transactions on Components and Packaging Technologies, 2002. **25**(1): p. 98-105.
9. Liu, C.Q., et al., *Under bump metallization of fine pitch flip-chip using electroless nickel deposition*. Journal of Electronics Manufacturing, 2000. **10**(3): p. 161-170.
10. Zhang, S., et al., *Stabilizer concentration and local environment: their effects on electroless nickel plating of PCB micropads*. Journal of the Electrochemical Society, 1999. **146**(8): p. 2870-2875.
11. Lin, K.L. and J.W. Hwang, *Effect of thiourea and lead acetate on the deposition of electroless nickel*. Materials Chemistry and Physics, 2002. **76**(2): p. 204-211.
12. Cheong, W.J., B.L. Luan, and D.W. Shoesmith, *The effects of stabilizers on the bath stability of electroless Ni deposition and the deposit*. Applied Surface Science, 2004. **229**(1-4): p. 282-300.
13. Jiang, X.X. and W. Shen, *The fundamentals and practice of electroless plating*. 2000, Beijing: National Defence Industry Press.

14. Chen, Z., et al., *Effect of plating parameters on the intrinsic stress in electroless nickel plating.* Surface & Coatings Technology, 2003. **167**(2-3): p. 170-176.
15. Jeon, Y.D. and K.W. Paik, *Stresses in electroless Ni-P films for electronic packaging applications.* Ieee Transactions on Components and Packaging Technologies, 2002. **25**(1): p. 169-173.
16. Mallory, G.O., *The Relationship between Stress and Adhesion of Electroless Nickel-Phosphorus Deposits on Zincated Aluminum.* Plating and Surface Finishing, 1985. **72**(6): p. 86-95.
17. van der Putten, A.M.T. and J.W.G. de Bakker, *Geometrical effects in the electroless metallization of fine metal patterns.* Journal of the Electrochemical society, 1993. **140**(8): p. 2221-2228.
18. Kloeser, J., et al., *Fine pitch stencil printing of Sn/Pb and lead free solders for flip chip technology.* Ieee Transactions on Components, Packaging, and Manufacturing Technology-Part C, 1998. **21**(1): p. 41-50.
19. Kloeser, J., et al., *Bump formation for flip chip and CSP by solder paste printing.* Microelectronics Reliability, 2002. **42**(3): p. 391-398.
20. Manessis, D., et al., *Technical challenges of stencil printing technology for ultra fine pitch flip chip bumping.* Microelectronics Reliability, 2004. **44**(5): p. 797-803.
21. Kloeser, J., et al., *Low cost bumping by stencil printing: process qualification for 200 mu m pitch.* Microelectronics Reliability, 2000. **40**(3): p. 497-505.
22. Zeng, K. and K.N. Tu, *Six cases of reliability study of Pb-free solder joints in electronic packaging technology.* Materials Science and Engineering, R: Reports, 2002. **38**: p. 55-105.
23. Massalski, T.B., et al., *Binary alloy phase diagram.* Vol. 1. 1986, Metals Park, Ohio: American Society for Metals.
24. Committees, A.I.A.P.D.a.H., *Alloy phase diagrams.* ASM Handbook. Vol. 3. 1992.
25. Glazer, J., *Metallurgy of Low-Temperature Pb-Free Solders for Electronic Assembly.* International Materials Reviews, 1995. **40**(2): p. 65-93.
26. Tu, K.N. and D. Turnbull, *Direct observation of twinning in tin lamellae.* Acta Metallurgica, 1970. **18**(8): p. 915-929.
27. Moffatt, W.G., G.W. Pearsall, and J. Wulff, *The structure and properties of materials: Vol. 1 - Structure.* 1964.

28. Manko, H.H., *Solders and soldering: materials, design, production, and analysis for reliable bonding.* 3rd ed. 1992, London: McGraw-Hill.
29. McCormack, M. and S.H. Jin, *Progress in the Design of New Lead-Free Solder Alloys.* Jom-Journal of the Minerals Metals & Materials Society, 1993. **45**(7): p. 36-40.
30. Ramirez, A.G., H. Mavoori, and S. Jin, *Bonding nature of rare-earth-containing lead-free solders.* Applied Physics Letters, 2002. **80**(3): p. 398-400.
31. Wang, L., et al., *Improvement of wettability and tensile property in Sn-Ag-RE lead-free solder alloy.* Materials Letters, 2002. **56**(6): p. 1039-1042.
32. Tojima, K., *Wetting characteristics of lead free solders.* 1999, Senior project report, Department of Materials Engineering, San Jose State University.
33. Collazo, J., *Effect of surface stresses on wetting of copper by solder.* 1997, Senior project report, Department of Materials Engineering, San Jose State University.
34. Winterbottom, W.L., *Converting to lead-free solders: an automotive industry perspective.* JOM, July, 1993: p. 20-24.
35. Tu, K.N., *Cu/Sn interfacial reactions: Thin-film case versus bulk case.* Materials Chemistry and Physics, 1996. **46**(2-3): p. 217-223.
36. Tu, K.N. and K. Zeng, *Reliability issues of Pb-free solder joints in electronic packaging technology*, in *52nd Electronic Components & Technology Conference, 2002 Proceedings.* 2002, I E E E: New York. p. 1194-1200.
37. Choi, W.J., et al., *Tin whiskers studied by synchrotron radiation scanning X-ray micro-diffraction.* Acta Materialia, 2003. **51**(20): p. 6253-6261.
38. Lau, J.H. and S.H. Pan, *3D nonlinear stress analysis of tin whisker initiation on lead- free components.* Journal of Electronic Packaging, 2003. **125**(4): p. 621-624.
39. Osenbach, J.W., et al., *Lead free packaging and Sn-whiskers*, in *54th Electronic Components & Technology Conference, Vols 1 and 2, Proceedings.* 2004. p. 1314-1324.
40. Lee, J.C.B., et al., *Characterization study of lead-free Sn-Cu plated packages*, in *52nd Electronic Components & Technology Conference, 2002 Proceedings.* 2002, I E E E: New York. p. 1238-1245.

41. Winterstein, J.P., J.B. LeBret, and M.G. Norton, *Characteristics of tin whiskers formed on sputter-deposited films - an aging study.* Journal of Materials Research, 2004. **19**(3): p. 689-692.

42. Oliver, W.C. and G.M. Pharr, *An improved technique for determining hardness and elastic modulus using load and displacement sensing indentation experiments.* Journal of Materials Research, 1992. **7**(6): p. 1564-1583.

43. Sneddon, I.N., *The relation between load and penetration in the axisymmetric Boussinesq problem for a punch of arbitrary profile.* International Journal of Engineering Science, 1965. **3**: p. 47-56.

44. Pharr, G.M., W.C. Oliver, and F.R. Brotzen, *On the Generality of the Relationship among Contact Stiffness, Contact Area, and Elastic-Modulus During Indentation.* Journal of Materials Research, 1992. **7**(3): p. 613-617.

45. King, R.B., *Elastic Analysis of Some Punch Problems for a Layered Medium.* International Journal of Solids and Structures, 1987. **23**(12): p. 1657-1664.

46. Pethica, J.B., R. Hutchings, and W.C. Oliver, *Hardness Measurement at Penetration Depths as Small as 20-Nm.* Philosophical Magazine a-Physics of Condensed Matter Structure Defects and Mechanical Properties, 1983. **48**(4): p. 593-606.

47. Doerner, M.F. and W.D. Nix, *A method for interpreting the data from depth-sensing indentation instruments.* Journal of Materials Research, 1986. **1**(4): p. 601-609.

48. Oliver, W.C., *Alternative technique for analyzing instrumented indentation data.* Journal of Materials Research, 2001. **16**(11): p. 3202-3206.

49. Oliver, W.C. and G.M. Pharr, *Measurement of hardness and elastic modulus by instrumented indentation: Advances in understanding and refinements to methodology.* Journal of Materials Research, 2004. **19**(1): p. 3-20.

50. Jang, J.W., et al., *Solder reaction-assisted crystallizaton of electroless Ni-P under bump metallization in low cost flip chip technology.* Journal of Applied Physics, 1999. **85**(12): p. 8456-8463.

51. Liu, P.L. and J.K. Shang, *Thermal stability of electroless-nickel/solder interface: Part B. Interfacial fatigue resistance.* Metallurgical and Materials Transactions a-Physical Metallurgy and Materials Science, 2000. **31**(11): p. 2867-2875.

52. Zeng, K., V. Vuorinen, and J.K. Kivilahti, *Intermetallic reactions between lead-free SnAgCu solder and Ni(P)/Au surface finish on PWBs*, in *51st Electronic Components & Technology Conference*. 2001. p. 693-698.

53. Li, M., et al., *Interfacial microstructure evolution between eutectic SnAgCu solder and Al/Ni(V)/Cu thin films.* Journal of Materials Research, 2002. **17**(7): p. 1612-1621.

54. Kang, S.K., et al., *Interfacial reaction studies on lead (Pb)-free solder alloys.* IBM Research Report, 2001.

55. Kang, S.K., et al., *Interfacial reaction studies on lead(Pb)-free solder alloys*, in *51st Electronic Components & Technology Conference*. 2001. p. 448-454.

56. Lee, K.Y., et al., *Microstructure, joint strength and failure mechanism of Sn-Ag, Sn-Ag-Cu versus Sn-Pb-Ag solders in BGA packages*, in *51st Electronic Components & Technology Conference*. 2001. p. 478-485.

57. Li, M., et al., *Microstructure, joint strength and failure mechanisms of SnPb and Pb-free solders in BGA packages.* Ieee Transactions on Electronics Packaging Manufacturing, 2002. **25**(3): p. 185-192.

58. Taguchi, T., et al., *Lead free interfacial structures and their relationship to Au plating (Including accelerated thermal cycle testing of non-leaden EGA spheres)*, in *51st Electronic Components & Technology Conference*. 2001. p. 675-680.

59. O'Sullivan, E.J., et al., *Electrolessly deposited diffusion barrier for microelectronics.* IBM Journal of Research and Development, 1998. **42**: p. 607-620.

60. Lea, C., *Quantitative solderability measurement of electronic components Part 1: the wetting balance.* Soldering & Surface Mount Technology, 1990. **4**: p. 8-13.

61. Lea, C., *Quantitative solderability measurement of electronic components Part 2: An index of solderability.* Soldering & Surface Mount Technology, 1990. **4**: p. 14-22.

62. Lea, C., *Quantitative solderability measurement of electronic components Part 3: Surface of standard solderability.* Soldering & Surface Mount Technology, 1990. **5**: p. 46-55.

63. Lea, C., *Quantitative solderability measurement of electronic components Part 4: Wetting balance instrument thermal design.* Soldering & Surface Mount Technology, 1990. **6**: p. 4-9.

64. Nysaether, J.B., P. Lundstrom, and J. Liu, *Measurements of solder bump lifetime as a function of underfill material properties.* Ieee Transactions on Components Packaging and Manufacturing Technology Part A, 1998. **21**(2): p. 281-287.

65. Gektin, V., A. BarCohen, and J. Ames, *Coffin-Manson fatigue model of underfilled flip-chips.* Ieee Transactions on Components Packaging and Manufacturing Technology Part A, 1997. **20**(3): p. 317-326.

66. Chou, W.J., G.P. Yu, and J.H. Huang, *Corrosion resistance of ZrN films on AISI 304 stainless steel substrate.* Surface & Coatings Technology, 2003. **167**(1): p. 59-67.

67. Quartarone, G., T. Bellomi, and A. Zingales, *Inhibition of copper corrosion by isatin in aerated 0.5 M H2SO4.* Corrosion Science, 2003. **45**(4): p. 715-733.

68. Park, J.J. and S.I. Pyun, *Pit formation and growth of alloy 600 in Cl- ion-containing thiosulphate solution at temperatures 298-573 K using fractal geometry.* Corrosion Science, 2003. **45**(5): p. 995-1010.

69. Zuo, Y., P.H. Zhao, and J.M. Zhao, *The influences of sealing methods on corrosion behavior of anodized aluminum alloys in NaCl solutions.* Surface & Coatings Technology, 2003. **166**(2-3): p. 237-242.

70. Lin, K.L., F.C. Chung, and T.P. Liu, *The potentiodynamic polarization behavior of Pb-free XIn-9(5Al- Zn)-YSn solders.* Materials Chemistry and Physics, 1998. **53**(1): p. 55-59.

71. Fujiwara, M. and M. Otsuka, *Indentation creep of beta-Sn and Sn-Pb eutectic alloy.* Materials Science and Engineering a-Structural Materials Properties Microstructure and Processing, 2001. **319**: p. 929-933.

72. Yang, F.Q. and J.C.M. Li, *Impression test of 63Sn-37Pb eutectic alloy (vol 201, pg 40, 1995).* Materials Science and Engineering a-Structural Materials Properties Microstructure and Processing, 1996. **210**(1-2): p. 135-135.

73. Liang, J., et al., *Effects of load and thermal conditions on Pb-free solder joint reliability.* Journal of Electronic Materials, 2004. **33**(12): p. 1507-1515.

74. Wade, N., et al., *Effect of microalloying on the creep strength and microstructure of an eutectic Sn-Pb solder alloy.* Journal of Electronic Materials, 1999. **28**(11): p. 1286-1289.

75. Wade, N., et al., *Effects of Cu, Ag and Sb on the creep-rupture strength of lead-free solder alloys.* Journal of Electronic Materials, 2001. **30**(9): p. 1228-1231.

76. Mei, Z., et al., *Superplastic Creep of Eutectic Tin-Lead Solder Joints.* Journal of Electronic Materials, 1990. **19**(11): p. 1273-1280.
77. Nix, W.D., *Mechanical properties of thin films.* Metallurgical Transactions A, 1989. **20A**: p. 2217-2245.
78. Brotzen, F.R., *Mechanical testing of thin films.* International Materials Reviews, 1994. **39**(1): p. 24-45.
79. Lucas, B.N. and W.C. Oliver, *Indentation power-law creep of high-purity indium.* Metallurgical and Materials Transactions a-Physical Metallurgy and Materials Science, 1999. **30**(3): p. 601-610.
80. Sattiraju, S.V., et al., *Wetting performance Vs. board finish and flux for several Pb-free solder alloys.* 26th IEMT Symposium, 2000.
81. Elbert, J. *Is Nitrogen Necessary for Lead-Free.* in *NEPCON West; proceedings of the technical program.* 2000. Anaheim, CA: Reed Exhibition Companies.
82. Wagner, C.D., et al., *Handbook of x-rayphotoelectron spectroscopy.* 1979, Norwalk: Perkin-Elmer Corp.
83. Zhang, B.C., et al., *Characterization of nickel phosphorus surface by ToF-SIMS.* Applied Surface Science, 2004. **231-2**: p. 868-873.
84. Li, D.Z., C. Liu, and P.P. Conway, *Solderability of electroless deposited Ni-P coatings with Sn-3.8Ag-0.7Cu and Sn-3.5Ag lead-free solder alloys.* Circuit World, 2005. **31**(3): p. 32-39.
85. Chen, Y.-Y., J.-G. Duh, and B.-S. Chiou, *The effect of substrate surface roughness on the wettability of Sn-Bi solders.* Journal of Materials Science: Materials in Electronics, 2000. **11**: p. 279-283.
86. Shuttleworth, R. and G.L.J. Bailey, *The spreading of a liquid over a rough solid.* Discussions of the Faraday Society, 1948. **3**: p. 16-22.
87. Ochoa, F., J.J. Williams, and N. Chawla, *Effects of cooling rate on the microstructure and tensile behavior of a Sn-3.5wt.%Ag solder.* Journal of Electronic Materials, 2003. **32**(12): p. 1414-1420.
88. Kim, K.S., S.H. Huh, and K. Suganuma, *Effects of cooling speed on microstructure and tensile properties of Sn-Ag-Cu alloys.* Materials Science and Engineering a-Structural Materials Properties Microstructure and Processing, 2002. **333**(1-2): p. 106-114.
89. Wickham, M., *Voiding: Occurrence and Reliability issues with lead-free.* 2003, National Physical Laboratory.

90. Biocca, P., *Lead-free defects in reflow soldering*. 2005, Kester.

91. AIM, *Reducing BGA voiding through process optimization*, www.aimsolder.com.

92. Yunus, M., et al., *Effect of voids on the reliability of BGA/CSP solder joints*. Microelectronics Reliability, 2003. **43**(12): p. 2077-2086.

93. Ciampolini, L., et al., *Modelling thermal effects of large contiguous voids in solder joints*. Microelectronics Journal, 1999. **30**(11): p. 1115-1123.

94. Chang, S.M., et al., *Investigation of electroplating NiUBM for Pb-free solders*, in *53rd Electronic Components & Technology Conference, 2003 Proceedings*. 2003. p. 1209-1214.

95. Tai, S.F., et al., *Effect of phosphorus content and solid state ageing on intermetallic formation between lead free Sn-Ag-Cu solder and electroless nickel / immersion gold under bump metallurgy*. 2002 International Symposium on Electronic Materials and Packaging, 2002: p. 267-270.

96. Zheng, Y., C. Hillman, and P. McCluskey, *Intermetallic growth on PWBs soldered with Sn3.8Ag0.7Cu*, in *52nd Electronic Components & Technology Conference, 2002 Proceedings*. 2002, I E E E: New York. p. 1226-1231.

97. Choi, W.K., et al., *Characterization of PBGA laminates attached with Sn-Ag-Cu Pb-free BGA solder balls*. IBM Research Report, 2001.

98. Jang, J.W., et al., *Morphology of interfacial reaction between lead-free solders and electroless Ni-P under bump metallization*. Journal of Applied Physics, 2000. **88**(11): p. 6359-6363.

99. Zribi, A., et al., *The kinetics of formation of ternary intermetallic alloys in Pb-Sn and Cu-Ag-Sn Pb-free electronic joints*, in *51st Electronic Components & Technology Conference*. 2001. p. 687-692.

100. Jeon, Y.D., et al., *Studies on the interfacial reactions between electroless Ni UBM and 95.5Sn-4.0Ag-0.5Cu alloy*, in *52nd Electronic Components & Technology Conference, 2002 Proceedings*. 2002, I E E E: New York. p. 740-746.

101. Jeon, Y.D., et al., *A study on interfacial reactions between electroless Ni-P under bump metallization and 95.5Sn-4.0Ag-0.5Cu alloy*. Journal of Electronic Materials, 2003. **32**(6): p. 548-557.

102. Jeon, Y.D., et al., *Comparison of interfacial reactions and reliabilities of Sn3.5Ag, Sn4.0Ag0.5Cu, and Sn0.7Cu solder bumps on electroless Ni-PUBMs*,

in *53rd Electronic Components & Technology Conference, 2003 Proceedings*. 2003. p. 1203-1208.

103. Jeon, Y.D., et al., *Studies of electroless nickel under bump metallurgy-solder interfacial reactions and their effects on flip chip solder joint reliability.* Journal of Electronic Materials, 2002. **31**(5): p. 520-528.

104. Kang, S.K., et al., *Studies of the mechanical and electrical properties of lead-free solder joints.* IBM Research Report, 2002.

105. Kang, S.K., et al., *Studies of the mechanical and electrical properties of lead-free solder joints.* Journal of Electronic Materials, 2002. **31**(11): p. 1292-1303.

106. Zeng, K.J., V. Vuorinen, and J.K. Kivilahti, *Interfacial reactions between lead-free SnAgCu solder and Ni(P) surface finish on printed circuit boards.* IEEE Transactions on Electronics Packaging Manufacturing, 2002. **25**(3): p. 162-167.

107. Luo, W.-C. and C.R. Kao, *Liquid/solid and solid/solid reactions between SnAgCu lead-free solder and Ni surface finish.* 2002 International Symposium on Electronic Materials and Packaging, 2002: p. 330-334.

108. Protsenko, P., et al., *The role of intermetallics in wetting in metallic systems.* Scripta Materialia, 2001. **45**(12): p. 1439-1445.

109. Pratt, R.E., E.I. Stromswold, and D.J. Quesnel, *Effect of solid-state intermetallic growth on the frature toughness of Cu/63Sn-37Pb solder joints.* Ieee Transactions on Components, Packaging, and Manufacturing Technology-Part a, 1996. **19**(1): p. 134-141.

110. Frear, D.R., et al., *The mechanics of solder alloy interconnects.* 1994, New York: Van Nostrand Reinhold.

111. Xiao, G.-W., et al., *Effect of Cu stud microstructure and electroplating process on intermetallics compound growth and reliability of flip-chip solder bump.* IEEE Transactions on Components and Packaging Technologies, 2001. **24**(4): p. 682-690.

112. Lee, Y.G. and J.G. Duh, *Interfacial morphology and contration profile in the unleaded solder/Cu joint assembly.* Journal of Materials Science: Materials in Electronics, 1999. **10**: p. 33-43.

113. Guan, Z.-M., G.-X. Liu, and T. Liu, *Kinetics of interface reaction in 40Sn-Bi/Cu and 40Sn-Bi-2Ag/Cu systems during ageing in solid state.* IEEE Transactions on Advanced Packaging, 2000. **23**(4): p. 737-742.

114. He, M., Z. Chen, and G.J. Qi, *Solid state interfacial reaction of Sn-37Pb and Sn-3.5Ag solders with Ni-P under bump metallization.* Acta Materialia, 2004. **52**: p. 2047-2056.

115. Chang, T.C., M.C. Wang, and M.H. Hon, *Crystal growth of the intermetallic compounds at the Sn-9Zn- xAg/Cu interface during isothermal aging.* Journal of Crystal Growth, 2003. **252**(1-3): p. 401-412.

116. Balkan, H., et al., *Flip-chip reliability: Comparative characterization of lead free (Sn/Ag/Cu) and 63Sn/Pb eutectic solder*, in *52nd Electronic Components & Technology Conference, 2002 Proceedings*. 2002, I E E E: New York. p. 1263-1269.

117. Kang, S.K., et al., *Formation of Ag3Sn plates in Sn-Ag-Cu alloys and optimization of their alloy composition*, in *53rd Electronic Components & Technology Conference, 2003 Proceedings*. 2003. p. 64-70.

118. Allen, S.L., et al., *Microstructural evolution in lead-free solder alloys: Part II. Directionally solidified Sn-Ag-Cu, Sn-Cu and Sn-Ag.* Journal of Materials Research, 2004. **19**(5): p. 1425-1431.

119. Henderson, D.W., et al., *Ag3Sn plate formation in the solidification of near ternary eutectic Sn-Ag-Cu alloys.* Journal of Materials Research, 2002. **17**(11): p. 2775-2778.

120. Prakash, K.H. and T. Sritharan, *Interface reaction between copper and molten tin-lead solders.* Acta Materialia, 2001. **49**(13): p. 2481-2489.

121. Blair, H.D., T.Y. Pan, and J.M. Nicholson, *Intermetallic compound growth on Ni, Au/Ni, and Pd/Ni substrates with Sn/Pb, Sn/Ag, and Sn solders*, in *48th Electronic Components & Technology Conference - 1998 Proceedings*. 1998. p. 259-267.

122. Huang, M.K., P.L. Wu, and C. Lee, *Effects of different printed circuit board surface finishes on the formation and growth of intermetallics at thermomechanically fatigued small outline J leads/Sn-Pb interfaces.* Materials Chemistry and Physics, 2004. **85**(1): p. 63-67.

123. Sharif, A. and Y.C. Chan, *Dissolution kinetics of BGA Sn-Pb and Sn-Ag solders with Cu substrates during reflow.* Materials Science and Engineering B-Solid State Materials for Advanced Technology, 2004. **106**(2): p. 126-131.

124. Ghosh, G., *A comparative study of the kinetics of interfacial reaction between eutectic solders and Cu/Ni/Pd metallization.* Journal of Electronic Materials, 2000. **29**(10): p. 1182-1193.

125. Kim, J.H., M.S. Suh, and H.S. Kwon, *The formation of Cu-Sn intermetallic compound and its effect on the fracture behavior of 80Sn-20Pb electrodeposits on Cu-based leadframe alloy.* Surface & Coatings Technology, 1996. **82**(1-2): p. 23-28.

126. Schaefer, M., R.A. Fournelle, and J. Liang, *Theory for intermetallic phase growth between Cu and liquid Sn- Pb solder based on grain boundary diffusion control.* Journal of Electronic Materials, 1998. **27**(11): p. 1167-1176.

127. Chan, Y.C., A.C.K. So, and J.K.L. Lai, *Growth kinetic studies of Cu-Sn intermetallic compound and its effect on shear strength of LCCC SMT solder joints.* Materials Science and Engineering B-Solid State Materials for Advanced Technology, 1998. **55**(1-2): p. 5-13.

128. Lee, T.Y., et al., *Morphology, kinetics, and thermodynamics of solid-state aging of eutectic SnPb and Pb-free solders (Sn-3.5Ag, Sn-3.8Ag-0.7Cu and Sn-0.7Cu) on Cu.* Journal of Materials Research, 2002. **17**(2): p. 291-301.

129. Yoon, J.W., S.W. Kim, and S.B. Jung, *Effect of reflow time on interfacial reaction and shear strength of Sn-0.7Cu solder/Cu and electroless Ni-P BGA joints.* Journal of Alloys and Compounds, 2004. **385**: p. 192-198.

130. Laurila, T., V. Vuorinen, and J.K. Kivilahti, *Interfacial reactions between lead-free solders and common base materials.* Materials Science & Engineering R-Reports, 2005. **49**: p. 1-60.

131. Oh, M., *Growth kinetics in intermetallic phases in the Cu-Sn binary and Cu-Ni-Sn ternary systems at low temperatures*, in *Materials Science and Engineering.* 1994, Lehigh University: Bethlehem, PA.

132. Deng, X., et al., *Deformation behavior of (Cu, Ag)-Sn intermetallics by nanoindentation.* Acta Materialia, 2004. **52**(14): p. 4291-4303.

133. Dao, M., et al., *Computational modeling of the forward and reverse problems in instrumented sharp indentation.* Acta Materialia, 2001. **49**(19): p. 3899-3918.

134. Malzbender, J. and G. de With, *Indentation load-displacement curve, plastic deformation, and energy.* Journal of Materials Research, 2002. **17**(2): p. 502-511.

135. Choi, Y., H.S. Lee, and D. Kwon, *Analysis of sharp-tip-indentation load-depth curve for contact area determination taking into account pile-up and sink-in effects.* Journal of Materials Research, 2004. **19**(11): p. 3307-3315.

136. Durst, K., M. Goken, and H. Vehoff, *Finite element study for nanoindentation measurements on two- phase materials.* Journal of Materials Research, 2004. **19**(1): p. 85-93.

137. Saha, R. and W.D. Nix, *Effects of the substrate on the determination of thin film mechanical properties by nanoindentation.* Acta Materialia, 2002. **50**(1): p. 23-38.

138. Maneiro, M.A.G. and J. Rodriguez, *Pile-up effect on nanoindentation tests with spherical-conical tips.* Scripta Materialia, 2005. **52**(7): p. 593-598.

139. Giannakopoulos, A.E. and S. Suresh, *Determination of elastoplastic properties by instrumented sharp indentation.* Scripta Materialia, 1999. **40**(10): p. 1191-1198.

140. Beegan, D., S. Chowdhury, and M.T. Laugier, *The nanoindentation behaviour of hard and soft films on silicon substrates.* Thin Solid Films, 2004. **466**(1-2): p. 167-174.

141. Soare, S., et al., *Nanoindentation assessment of aluminium metallisation; the effect of creep and pile-up.* Surface & Coatings Technology, 2004. **177**: p. 497-503.

142. Cheng, Y.T. and C.M. Cheng, *What is indentation hardness?* Surface & Coatings Technology, 2000. **133**: p. 417-424.

143. Goldstein, J.L.F. and J.W. Morris, *Microstructural Development of Eutectic Bi-Sn and Eutectic in- Sn During High-Temperature Deformation.* Journal of Electronic Materials, 1994. **23**(5): p. 477-486.

144. Kerr, M. and N. Chawla, *Creep deformation behavior of Sn-3.5Ag solder/Cu couple at small length scales.* Acta Materialia, 2004. **52**(15): p. 4527-4535.

145. Dutta, I., C. Park, and S. Choi, *Impression creep characterization of rapidly cooled Sn-3.5Ag solders.* Materials Science and Engineering a-Structural Materials Properties Microstructure and Processing, 2004. **379**(1-2): p. 401-410.

146. Wiese, S. and K.J. Wolter, *Microstructure and creep behaviour of eutectic SnAg and SnAgCu solders.* Microelectronics Reliability, 2004. **44**: p. 1923-1931.

147. Wu, K.P., et al., *Microstructural effect on the creep strength of a Sn-3.5%Ag solder alloy.* Journal of Electronic Materials, 2003. **32**(1): p. 5-8.

148. Lucas, J.P., et al., *Mechanical properties of intermetallic compounds associated with Pb-free solder joints using nanoindentation.* Journal of Electronic Materials, 2003. **32**(12): p. 1375-1383.

149. Huang, M.L., L. Wang, and C.M.L. Wu, *Creep behavior of eutectic Sn-Ag lead-free solder alloy.* Journal of Materials Research, 2002. **17**(11): p. 2897-2903.

150. Yang, W.G., L.E. Felton, and R.W. Messler, *The Effect of Soldering Process Variables on the Microstructure and Mechanical-Properties of Eutectic Sn-Ag/Cu Solder Joints.* Journal of Electronic Materials, 1995. **24**(10): p. 1465-1472.

151. Murty, K.L., F.M. Haggag, and R.K. Mahidhara, *Tensile, creep, and ABI tests on Sn5%Sb solder for mechanical property evaluation.* Journal of Electronic Materials, 1997. **26**(7): p. 839-846.

152. Song, H.G., J.W. Morris, and F. Hua, *Anomalous creep in Sn-rich solder joints.* Materials Transactions, 2002. **43**(8): p. 1847-1853.

153. Song, H.G., J.W. Morris, and F. Hua, *The creep properties of lead-free solder joints.* Jom-Journal of the Minerals Metals & Materials Society, 2002. **54**(6): p. 30-32.

154. Sherby, O.D. and J. Weertman, *Diffusion-Controlled Dislocation Creep - Defense.* Acta Metallurgica, 1979. **27**(3): p. 387-400.

155. Alam, M.O., Y.C. Chan, and K.C. Hung, *Reliability study of the electroless Ni-P layer against solder alloy.* Microelectronics Reliability, 2002. **42**(7): p. 1065-1073.

156. Deng, X., et al., *Influence of reflow and thermal aging on the shear strength and fracture behavior of Sn-3.5Ag Solder/Cu joints.* Metallurgical and Materials Transactions a-Physical Metallurgy and Materials Science, 2005. **36A**(1): p. 55-64.

157. Tsui, Y.-K., S.W.R. Lee, and X. Huang, *Experimental investigation on the degradation of BGA solder ball shear strength due to room temperature aging.* 2002 International Symposium on Electronic Materials and Packaging, 2002: p. 478-481.

158. Popelar, S., A. Strandjord, and B. Niemet, *A compatibility evaluation of lead-based and lead-free solder alloys in conjunction with electroless nickel/immersion gold flip chip UBM,* in *2001 International Symposium on*

Microelectronics, Proceedings. 2001, SPIE-INT SOCIETY OPTICAL ENGINEERING: Bellingham. p. 575-580.

159. Kim, J.W. and S.B. Jung, *Experimental and finite element analysis of the shear speed effects on the Sn-Ag and Sn-Ag-CuBGA solder joints.* Materials Science and Engineering a-Structural Materials Properties Microstructure and Processing, 2004. **371**(1-2): p. 267-276.
160. Minges, M.L., ed. *Electronic Materials Handbook, Vol. 1, Packaging*. 1989, Materials Park: OH. p. 640.
161. Erich, R., et al., *Shear testing and failure mode analysis for evaluation of BGA ball attachment.* 1999 IEEE/CPMT int'l Electronics Manufacturing Technology Symposium, 1999: p. 16-22.
162. Huang, X.J., S.W.R. Lee, and C.C. Yan, *Experimental investigation on the progressive failure mechanism of solder balls during ball shear test*, in *52nd Electronic Components & Technology Conference, 2002 Proceedings*. 2002, I E E E: New York. p. 968-973.
163. Lee, H.T., et al., *Influence of interfacial intermetallic compound on fracture behavior of solder joints.* Materials Science and Engineering a-Structural Materials Properties Microstructure and Processing, 2003. **358**(1-2): p. 134-141.
164. Pang, J.H.L., et al., *Bulk solder and solder joint properties for lead free 95.5Sn-3.8Ag- 0.7Cu solder alloy*, in *53rd Electronic Components & Technology Conference, 2003 Proceedings*. 2003. p. 673-679.
165. Kim, J.W., et al., *Effect of shear speed on the shear force of low melting point BGA solder joints.* EMAP 2003 Proceeding, 2003: p. 282-288.
166. Lin, K.L. and Y.C. Liu, *Reflow and property of Al/Cu/electroless nickel/Sn-Pb solder bumps.* Ieee Transactions on Advanced Packaging, 1999. **22**(4): p. 568-574.
167. Hou, Z., et al., *Lead-free solder flip chip-on-laminate assembly and reliability.* Ieee Transactions on Electronics Packaging Manufacturing, 2001. **24**(4): p. 282-292.
168. Tu, P.L., Y.C. Chan, and J.K.L. Lai, *Effect of intermetallic compounds on the thermal fatigue of surface mount solder joints.* Ieee Transactions on Components Packaging and Manufacturing Technology Part B-Advanced Packaging, 1997. **20**(1): p. 87-93.

169. Nurmi, S., et al., *The effect of solder paste composition on the reliability of SnAgCu joints.* Microelectronics Reliability, 2004. **44**(3): p. 485-494.

170. Schubert, A., et al., *Reliability assessment of flip-chip assemblies with lead-free solder joints*, in *52nd Electronic Components & Technology Conference, 2002 Proceedings*. 2002, I E E E: New York. p. 1246-1255.

171. Moreau, S., T. Lequeu, and R. Jerisian, *Comparative study of thermal cycling and thermal shocks tests on electronic components reliability.* Microelectronics Reliability, 2004. **44**(9-11): p. 1343-1347.

172. Amagai, M., Y. Toyoda, and T. Tajima, *High solder joint reliability with lead free solders*, in *53rd Electronic Components & Technology Conference, 2003 Proceedings*. 2003. p. 317-322.

173. Chen, L., et al., *The effects of underfill and its material models on thermomechanical behaviors of a flip chip package.* Ieee Transactions on Advanced Packaging, 2001. **24**(1): p. 17-24.

174. Huang, M.L., et al., *Microstructural evolution of a lead-free solder alloy Sn-Bi-Ag- Cu prepared by mechanical alloying during thermal shock and aging.* Journal of Electronic Materials, 2000. **29**(8): p. 1021-1026.

175. Gowda, A., et al., *Rework and reliability of underfilled CSP assemblies*, in *52nd Electronic Components & Technology Conference, 2002 Proceedings*. 2002. p. 458-466.

176. Chung, C.K., et al., *The interactions of lead (Pb) in lead free solder (Sn/Ag/Cu) system*, in *52nd Electronic Components & Technology Conference, 2002 Proceedings*. 2002. p. 168-175.

177. Wiegele, S., et al., *Reliability and process characterization of electroless nickel-gold/solder flip chip interconnect technology.* 1998 Electronic Components and Technology Conference, 1998: p. 861-866.

178. Stepniak, F., *Conversion of the under bump metallurgy into intermetallics: the impact on flip chip reliability.* Microelectronics Reliability, 2001. **41**: p. 735-744.

179. Lin, K.L. and T.P. Liu, *The electrochemical corrosion behaviour of Pb-free Al-Zn-Sn solders in NaCl solution.* Materials Chemistry and Physics, 1998. **56**(2): p. 171-176.

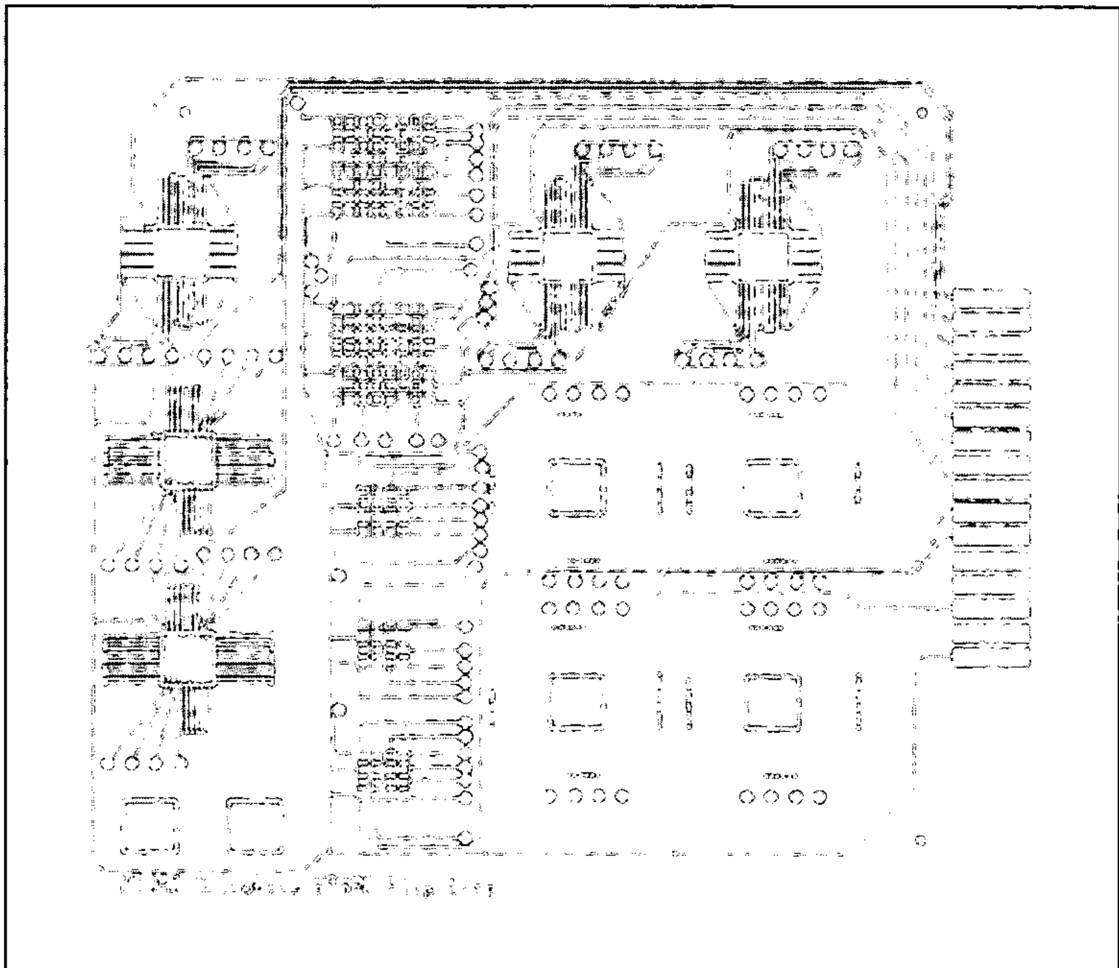
180. Oulfajrite, H., et al., *Electrochemical behavior of a new solder material (Sn-In-Ag).* Materials Letters, 2003. **57**(28): p. 4368-4371.

181. Erinc, M., et al., *Characterization and fatigue damage simulation in SAC solder joints.* Microelectronics Reliability, 2004. **44**(9-11): p. 1287-1292.

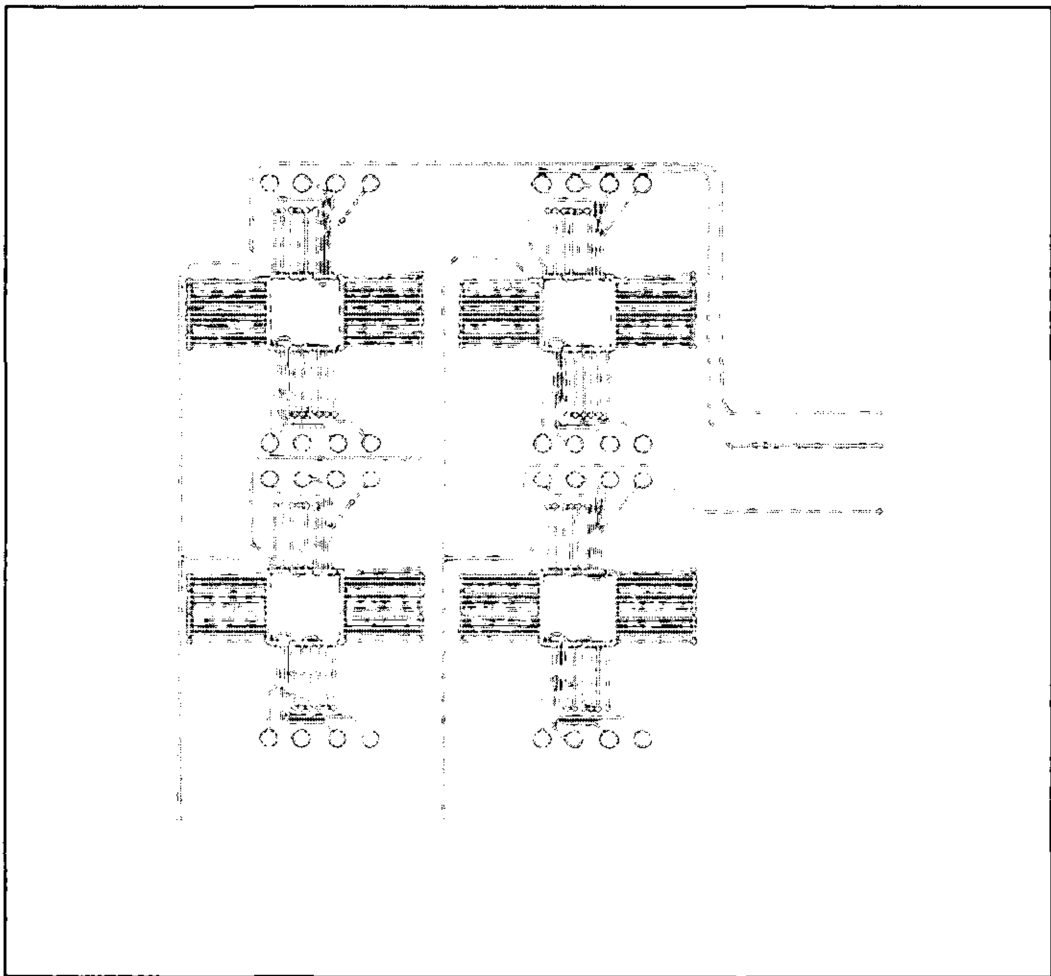
182. Vandevelde, B., et al., *Parameterized modeling of thermomechanical reliability for CSP assemblies.* Journal of Electronic Packaging, 2003. **125**(4): p. 498-505.

Appendix 1

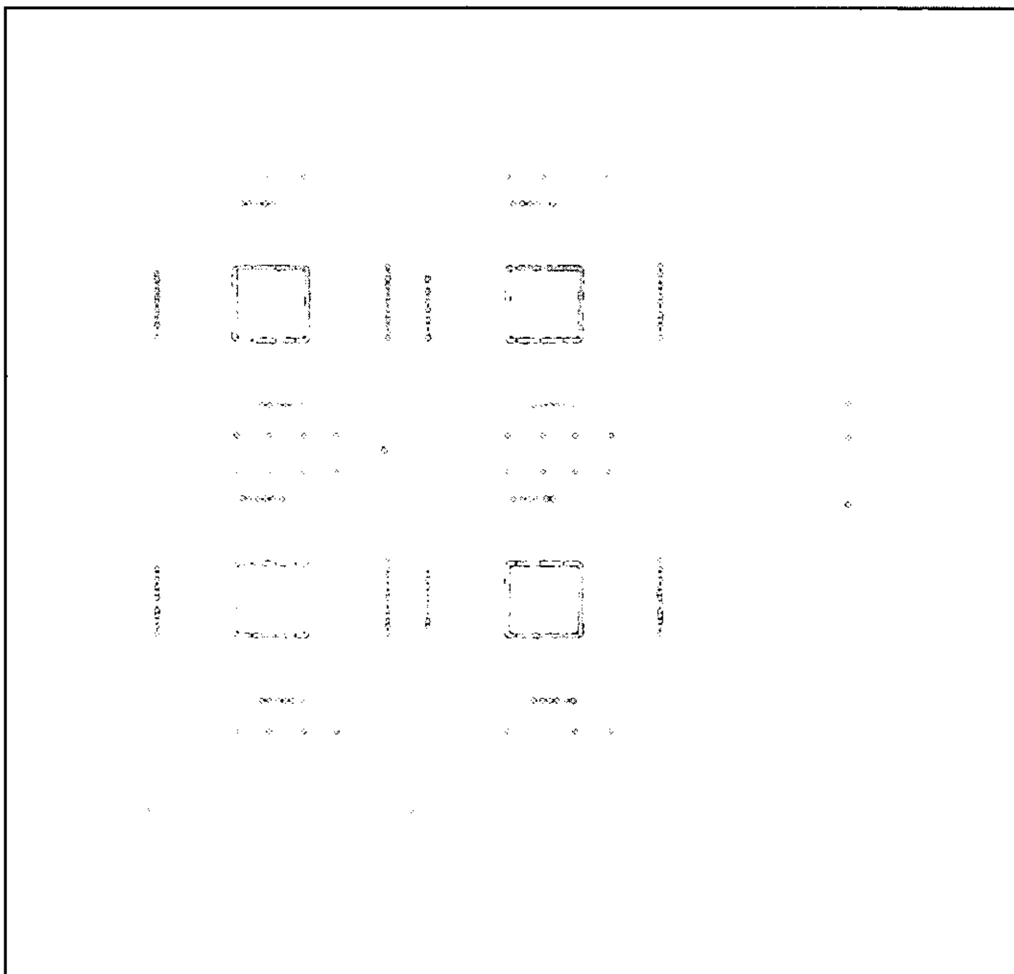
Gerber files of MT030 test board



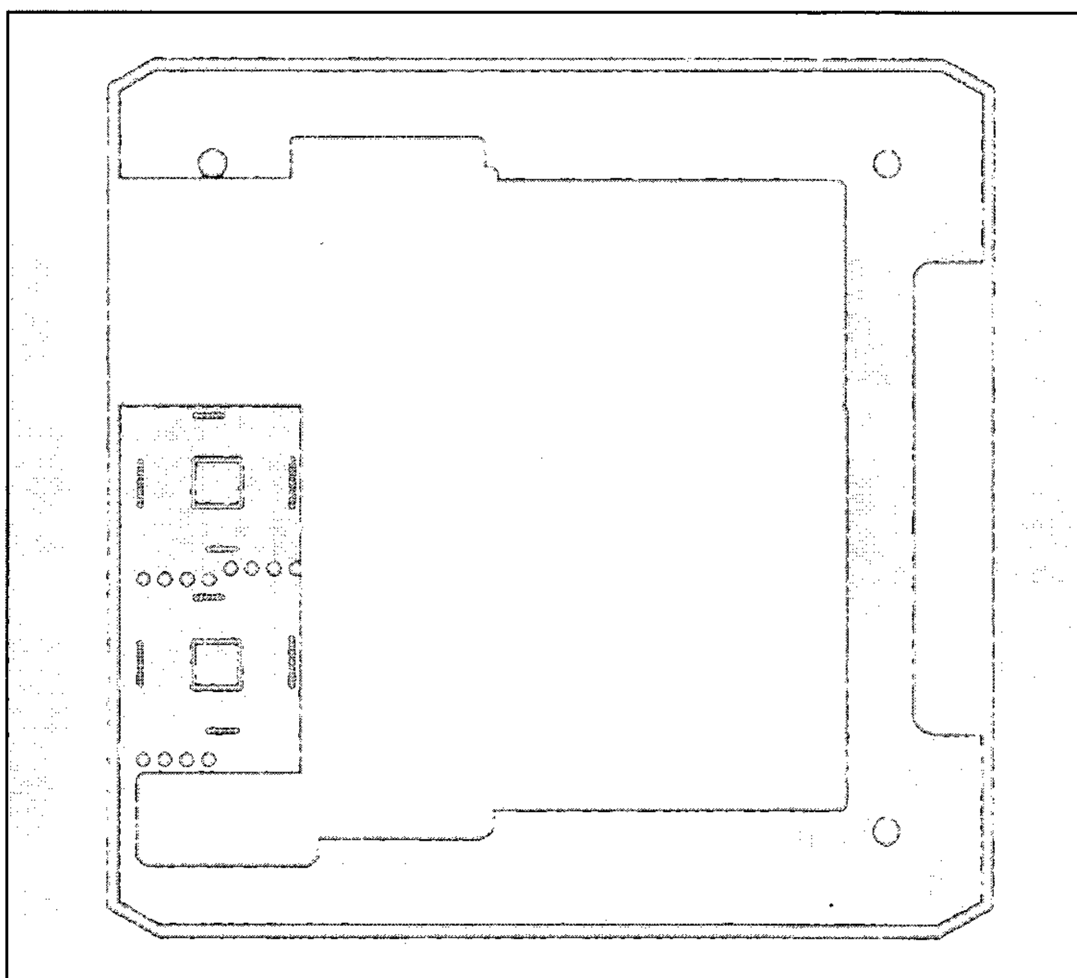
Top metal layer



Inner metal layer



Micro-via layer



Solder mask layer

Appendix 2

Publications

1. **Dezhi Li**, Changqing Liu, Paul P. Conway, Characteristics of intermetallics and micromechanical properties during thermal aging of Sn-Ag-Cu flip-chip solder joints, *Materials Science and Engineering-A*, 2004. 391: p. 95-103.
2. **Dezhi Li**, Changqing Liu, Paul P. Conway, Solderability of Electroless Deposited Ni-P Coatings with Sn-3.8Ag-0.7Cu and Sn-3.5Ag Lead Free Solder Alloys, *Circuit World,* 2005. 31(3): p. 32-39.
3. C. Liu, P.P. Conway, **D.Z. Li**, M. Hendriksen, Analysis of the micro-mechanical properties in aged lead-free, fine pitch flip chip joints, *Journal of Electronic Packaging,* 2004. 126(3): p. 359-366.
4. Changqing Liu, **Dezhi Li** and Paul Conway, Characterisation of Intermetallic Ageing in Flip Chip Solder Bumps, *53rd Electronics Components and Technology Conference*, 27-30 May, 2003, New Orleans, USA, pp 1767-1771.
5. Changqing Liu, Paul Conway, **Dezhi Li** and Michael Hendriksen, Analysis of the micro- mechanical properties in aged lead-free, fine pitch flip chip joints, *International Electronic Packaging Technical Conference and Exhibition*, July 6-11, 2003, Maui, Hawaii, USA, Paper No. 35130.
6. **D.Z. Li**, C. Liu, P.P. Conway, Direct sldering onto the UBM of electroless deposited Ni-P with Pb-free alloys, *Proceedings of EMAP 2003* (*International symposium on electronic materials and packaging*), 17-20 Nov. 2003, Singapore, pp 269-276.
7. **D.Z. Li**, C. Liu, P.P. Conway, Micromechanical Characterisation of Sn-Ag-Cu Solder FCOB Interconnects at Ambient and Elevated Temperatures, *54th Electronics Components and Technology Conference*, June 1-4, 2004, Las Vegas, Nevada, USA, pp 128-133.

8. **Dezhi Li**, Changqing Liu, Paul P. Conway, Interfacial Reactions between Pb-free Solders and Metallised Substrate Surfaces, *Proceeding of International Conference on Electronics Packaging Technology (ICEPT)*, 2005, Shenzhen, China, pp 360-365.
9. **Dezhi Li**, Changqing Liu, Paul P. Conway, Microstructure and Shear Strength Evolution during Ageing at Different Temperatures, accepted by *Journal of Electronic Materials.*
10. Changqing Liu, David A. Hutt, **Dezhi Li**, Paul P. Conway, Effect of microstructural characteristics of electroless nickel metallization on solderability, accepted by *InterPACK 2005*, 17-22 July 2005, San Francisco, USA.
11. **Dezhi Li**, Changqing Liu, Paul P. Conway, Reliability of Sn-Ag-Cu solder joints with different connection pads during thermal cycling, to be submitted.
12. **Dezhi Li**, Changqing Liu, Paul P. Conway, The potentiodynamic polarization behaviour of Sn-Pb and lead free solders in NaCl solution, to be submitted.