A DELTA-SIGMA MODULATED SPEED CONTROL SYSTEM FOR INDUCTION MOTORS

by

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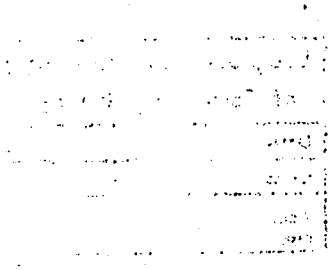
"To AKSEL and DEVELIOGLU Families"



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SYNOPSIS

The electronic control techniques used in static frequency changers differ considerably, depending on the type of system considered and the particular specifications and requirements. Mark-space ratio control and pulse-width modulation are among techniques already well-established for use with induction motors to provide a variable-speed a.c. drive.

The project is concerned with the applicability of delta-sigma modulation as the basis of a novel method of electronic speed control. The techniques involved are well-known in communication systems, where they are extensively used in the transmission of speech signals. With a sine wave at the input, a delta-sigma modulator produces an output quantised in both voltage and frequency, which enables power control to be achieved from a fixed d.c. supply using only a single power controller. This feature is of considerable potential importance in the field of a.c. drives, as is the fact that the harmonic components of the voltages and currents in the circuit are much lower than obtained with most existing techniques. Since the frequency of encoding is high, a transistor inverter is more suitable than a thyristor inverter for amplifying the control signal before feeding to the motor.

The project aims to outline the main features of a delta-sigma modulated speed-control system. Characteristics of induction motors and different speed control methods are discussed. Delta modulation techniques are investigated, with consideration given to their potential use for speed control purposes. A computer simulation is employed to investigate the characteristics of delta-sigma modulation, and the design and performance of delta-sigma modulators are outlined. The problems associated with the design of the inverter and the driving circuitry are discussed. Experimental results are presented from a prototype equipment, which provides continuous and reversible speed variation, with controllable acceleration and deceleration. Results are discussed and suggestions for future research are included.

LIST OF PRINCIPAL SYMBOLS

$s_{(m)}$	=	slip, for maximum torque
p	=	number of poles
V	=	voltage
I	=	current
T	=	torque developed by motor, time constant of RC integrator
I_t	=	stator current per phase
f	=	frequency
ω	=	angular frequency
R_r	=	rotor resistance
ω_s	=	supply frequency in rad/sec.
N_s	=	supply frequency in rev/min, secondary turns ratio of a transformer
α,θ	=	phase angle
ΔM	=	delta modulation
Δ-ΣM	=	delta sigma modulation
Δv	=	central delta step
f_0	=	characteristic frequency of integrator
i(t)	=	input to the modulator
o(t)	=	output of the modulator
ϵ	=	error
f_c	=	frequency of the clock signal
X(I),Y(I),Z(I)	=	3-phase inputs to Δ-Σ modulation simulator
ϕ	=	flux
V_{CE}	=	collector-emitter voltage of a transistor
$V_{CE(SAT)}$	=	saturation value of V_{CE}

I_B	=	base current of a transistor
I_C	=	collector current of a transistor
I_{CO}	=	leakage current of a transistor
V_{EB}	=	emitter-base voltage of a transistor
$V_{(BR)EBO}$	=	breakdown emitter-base voltage
h_{FE}	=	forward current transfer ratio
t_{on}	=	turn-on time
t_{off}	=	turn-off time
t_s	=	storage time
t_d	=	delay time
τ	=	time constant
T1	=	transistor 1
dV/dt	=	rate of rise of voltage

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CHAPTER 1

INTRODUCTION

1.1 GENERAL

There are many special-purpose industrial drives which require variable-speed operation. In general, variable-speed motor systems have used D.C. and/or A.C. commutator motors where a large speed range is required. In this respect, the Ward-Leonard system using a D.C. generator-motor combination is the traditional drive. The outstanding advantage of these machines is the ease with which their speed may be controlled, and yet provide a suitable torque at all speeds. Their major weakness is the commutator and brushgear assembly, giving rise to commutation problems and the need for regular servicing.

By contrast, the A.C. induction motor, which usually operates at an almost fixed speed, has a number of distinct advantages. In particular, in its Squirrel Cage form it is brushless, cheap, simple, reliable and requires little servicing. It can be operated in practically any environment, and run at a higher speed and over a wider temperature range than the commutator motor.

It can be seen that a variable-speed A.C. induction motor is the most desirable solution to many industrial problems. For this reason, the use of induction motors for variable-speed drive systems has attracted a lot of attention in the past.

Induction motors[1] are fundamentally single-speed machines, that speed being dependent on the frequency of the power supply. The speed of an induction motor is given by the following expression:

$$n = \frac{f}{p}(1-s) \qquad (1.1)$$

where,

n = Speed in rev/sec

f = Frequency of supply

p = Number of poles

s = Slip

It is obvious from equation (1.1) that there are three possible methods of varying the speed;

a) Varying the number of poles, p

The speed can be varied in steps by changing the number of poles, whilst maintaining a constant supply frequency. Pole-changing motors are specially wound and widely used for this purpose.

b) Varying the slip, s

In order to vary the slip at a constant torque, resistors can be connected in the rotor circuit of slip-ring induction motors. This means of control is, however, largely dependent on load, and cannot be applied to squirrel-cage motors.

c) Varying the supply frequency, f

Since the speed is approximately proportional to the frequency, the speed of a squirrel-cage induction motor can be varied by variation of the frequency.

1.2 ROTATING MACHINE SYSTEM

In the past the solution to the problem of a variable-frequency supply lay in the use of rotating machines, (Figure 1.1). A D.C. motor, the speed of which was controlled by varying the field excitation, was used to drive a 3-phase alternator, which produced the required supply voltage at a controlled frequency. This output was used to drive the induction motor.

The disadvantages of this system are the high cost and maintenance requirements, coupled with the fact that the system has a limited frequency range.

1.3 STATIC INVERTER SYSTEM

Static inverters[2-3] enable a supply of direct current or alternating current of one frequency to be converted to a supply of alternating current at some other frequency. The conversion of very large powers can be accomplished with thyristor inverters, which have now replaced much of the rotating electrical machinery that was previously used for frequency changing.

The static inverter system, which uses high-power electronic components to produce a 3-phase supply of variable frequency, first became realisable with the development of the thyratron, a thermionic device capable of conducting in one direction only, and then only after an "enabling" pulse has been applied to the gate terminal. However, the use of thyratron systems was limited by both the very high price of these devices (typically a 12 A thyratron could cost £50), and their short service life (typically one or two years).

The advent of the silicon controlled rectifier, or thyristor, enabled practical systems for static inversion to be developed. Thyristors have electrical characteristics similar to thyratrons, but cost only one tenth of the price. Theoretically they have an infinite service life, provided that they are operated within their ratings, and being solid-state devices they require no maintenance and they can be directly controlled electronically. These advantages have resulted in thyristor-based systems superceding motor-generator systems, and the installation of thyristor-controlled induction motor drive systems is now growing at a rapidly-increasing rate.

With the appearance on the market of medium-power, high-voltage, fast-switching transistors, the application of transistorized inverters for the speed control of A.C. machines has become a practical reality. Transistors offer some important advantages over thyristors. Since they can be switched off easily, by the removal of base drive and the application of a

voltage of reverse polarity to the base-emitter junction, there is no need for any commutation components, and the problem of trapped energy is solved. They can also be operated at very high frequencies.

1.4 OBJECT OF INVESTIGATION

The object of the present investigation is to determine the applicability of delta-sigma modulation to the control of a small 3-phase induction motor. The work falls mainly into the following categories:

(i) Investigation of the characteristics of delta-sigma modulation, from the point of view of speed control.

(ii) Design and construction of a satisfactory wide-range speed control system which has the facilities of speed reversal, acceleration and deceleration control and the facility for operation in a closed-loop mode.

(iii) Design and construction of a suitable driver and power transistor inverter for the amplification of delta-sigma modulated signals to supply an induction motor.

(iv) Investigation of the performance of the induction motor when fed from a delta-sigma modulated inverter.

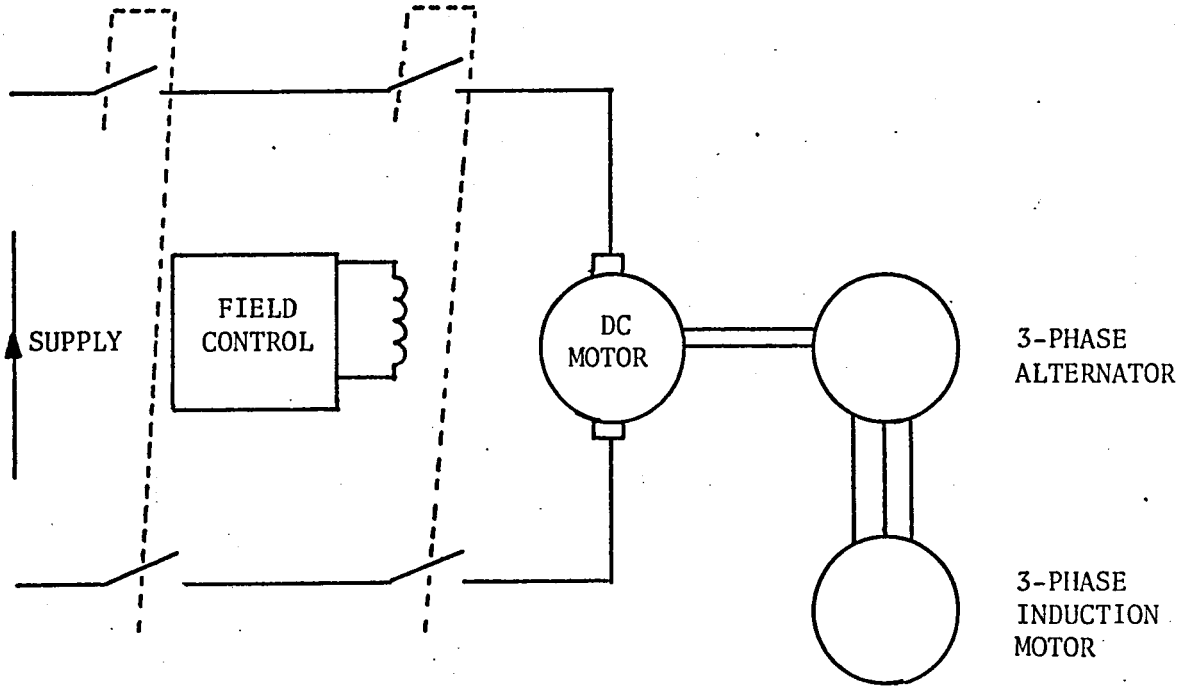


Figure 1.1: INDUCTION MOTOR SPEED CONTROL USING ROTATING MACHINES

CHAPTER 2

CHARACTERISTICS OF INDUCTION MOTORS AND SPEED CONTROL TECHNIQUES

2.1 INDUCTION MOTOR CHARACTERISTICS

2.1.1 Torque-Speed Characteristics

Before elaborating on the methods of static inversion which can be used to drive induction motors, it is worthwhile considering the behaviour of such motors on sinusoidal supplies, and for this purpose it is helpful to study the equivalent circuits of the motor shown in Figure 2.1.

In Figure 2.1.a we have the basic per-phase equivalent circuit[4] at a slip s. Considering the motor reduced to standstill with the mechanical power output represented by the power loss in a resistance equal to $R_r\frac{1-s}{s}$, leads to the equivalent circuit shown in Figure 2.1.b. By referring the motor impedances to the stator, and assuming the transformer to be ideal, we obtain the equivalent circuit shown in Figure 2.1.c. Finally, by applying Thevenin's theorem, the equivalent circuit shown in Figure 2.1.d is obtained, where:

$$E_t = \frac{jXE_1}{R_1+j(X_1+X_0)} \quad , \tag{2.1}$$

$$R_t+jX_t = \frac{jX_0(R_1+jX_1)}{R_1+j(X_0+X_1)} \quad , \tag{2.2}$$

in which:

E_1 = input voltage per phase

R_1 = resistance of stator per phase

X_1 = leakage reactance of stator per phase

X_0 = magnetising reactance

Assuming the power required for the core loss is included in the mechanical output, the stator current/phase is:

$$I_t = \frac{E_t}{\sqrt{(R_t+\frac{R_2}{s})^2+(X_t+X_2)^2}} \quad . \tag{2.3}$$

The torque developed by the motor is calculated by equating the actual mechanical output at a speed ω_s to the electrical power dissipated in the equivalent resistor $R_2\frac{(1-s)}{s}$ of Figure 2.1.c.

i.e. $$T.\omega_s(1-s) = I_t^2 R_2\frac{(1-s)}{s} \quad .$$

Substituting for I_t from equation (2.3)

$$T = \frac{E_t^2 R_2 s}{\omega_s (sR_t+R_2)^2+s^2(X_t+X_2)^2} \quad , \tag{2.4}$$

The maximum or pull-out torque is found by differentiating equation (2.4) with respect to s and equating to zero, giving the slip for maximum torque as

$$s_m = \frac{\pm R_2}{\sqrt{R_t^2+(X_t+X_2)^2}} \quad , \tag{2.5}$$

and, by substituting this in equation (2.4), the maximum torque as,

$$T_{max} = \pm \frac{E_t^2}{2\omega_s (R_t+\sqrt{R_t^2+(X_t+X_2)^2}} \quad , \tag{2.6}$$

Equations (2.5) and (2.6) show that the rotor resistance does not effect the maximum torque produced by the motor, but only the speed or slip at which this occurs. If, for simplicity the stator parameters are neglected, the equations for the current and torque reduce to:

$$I = \frac{E_2}{\sqrt{X_2^2 + \frac{R_2^2}{s^2}}} \quad , \tag{2.7}$$

and

$$T = \frac{E_2^2 R_2 s}{\omega_s (R_2^2+X_2^2 s^2)} \quad , \tag{2.8}$$

respectively. Equation (2.8) has two asymptotes; for s large $T \alpha \frac{1}{s}$ and for s small $T \alpha s$. The characteristics are shown in Figure 2.2. The operating region for motor action is between zero speed (s=1) and synchronous speed (s=0), and if the motor runs above synchronous speed (by being driven externally) it acts as an asynchronous generator feeding power to the supply. For a slip greater than 1, the machine is in a braking mode, a possibility exploited either by disconnecting the machine from the a.c. supply and injecting d.c. at the stator terminals (dynamic braking) or by interchanging any two of the three stator connections (plugging).

2.1.2 Induction Motor Drive Stability

The matching of a motor with the load characteristics is of prime importance in any electrical drive, and a simple assessment of the ability of an induction motor to cope with a particular load situation may be considered with the assistance of Figure 2.2.

Assuming the motor is operating against a constant load torque, such that a balance is obtained when the motor and load characteristics intersect at A, it can be seen that should the speed decrease by a small increment (say to B), there is an excess of torque available to raise the speed back to that at A. Correspondingly, if the speed increases, insufficient torque is available to maintain the increase and the speed falls back to that at A. In both cases, the initial conditions are restored and the system is stable. However, operating at C does not fulfill this requirement, since a fall in speed to D is accompanied by a fall in the torque produced by the motor, resulting in a continued and rapid decelaration to standstill.

The above arguement shows qualitatively that the only stable operating region for an induction motor is on the negative slope region of its characteristics, so that for the motor to be driven over the widest possible speed range the region of negative slope must be extended to the whole of that range.

2.1.3 Effect of Input Voltage and the Rotor Resistance on the Torque-Speed Characteristics

Before discussing efficient methods of extending the negative-slope region of the torque-speed characteristic, it is valuable to consider the effect of input voltage and rotor resistance on this characteristic.

Increasing the rotor resistance increases the slip at which maximum torque is produced, and modifies the characteristic as shown in Figure 2.3. It can be seen that the negative slope region of the characteristics can be much extended, enabling the speed to be controlled over a wide range simply

by varying the voltage applied to the stator. However, although a given variation in the supply voltage produces a significantly greater speed change for a high resistance rotor, it involves excessive rotor-heating and requires the motor to be down-rated to prevent thermal damage. Such drives are therefore uneconomic, and the use of low resistance rotors for all drives exceeding about 1/2 hp is universal.

2.1.4 Extension of Negative Slope Region by Variation of Supply Frequency

The negative slope region of a low rotor-resistance motor can be extended over the full speed range desired by changing the frequency of the supply. With the applied voltage assumed to be almost equal to the induced emf, then

$$V = k\Phi f \quad , \tag{2.9}$$

where:

k = constant involving the form factor, the winding factor and the number of turns of the winding,

Φ = maximum flux per pole,

V = r.m.s. voltage applied.

Since an induction motor is designed to work at a given magnetic loading, the applied voltage must be varied in proportion to the frequency if the flux is to be kept constant. If V, but not V/f, is kept constant, and the frequency is decreased below the design frequency, the magnetic circuit saturates, whereas if the frequency is raised above the design frequency the iron circuit is not used to its fullest capabilities. Under the condition of V/f constant, the normalised form of the torque-speed characteristic is substantially unchanged by any variation of this ratio, being primarily dependent on the slip speed, until the frequency is sufficiently low for the magnetising reactance to become comparable with the rotor circuit impedance.

The characteristics of the induction motor as the supply frequency is changed can be derived from the equivalent circuit, with the supply

frequency (ω_s) treated as a variable, and the overall slip calculated to a base of the new maximum frequency (ω_1). Since the supply frequency is varied X_2 is no longer constant, and when it is replaced with the more explicit impedance term $\omega_s L_s$, equation (2.7) becomes,

$$I = \frac{E_2}{\sqrt{\frac{R_2^2}{s^2} + \omega_s^2 L_2^2}} \quad , \tag{2.10}$$

where s = slip = $(\omega_s - \omega_r)/\omega_s$.

Since the torque is given by,

$$T = \frac{I^2 R_2}{\omega_s s}$$

it follows that,

$$T = \frac{E_2^2}{\omega_s^2} \cdot \frac{(\omega_s - \omega_r) R_2}{R_2^2 + L_2^2 (\omega_s - \omega_r)^2} \quad , \tag{2.11}$$

If

s_1 = slip to base frequency $\omega_1 = (\omega_1 - \omega_r)/\omega_1$

s_s = synchronous speed slip to base frequency $\omega_1 = (\omega_1 - \omega_s)/\omega_1$

s_r = rotor slip to base frequency $\omega_1 = (\omega_s - \omega_r)/\omega_1$

then

$$s_r = s_1 - s_s$$

and from equation (2.11)

$$T = \frac{E_2^2}{\omega_s^2} \cdot \frac{\omega_1 R_2 s_r}{R_2^2 + \omega_1^2 L_2^2 s_r^2}$$

and letting $X_a = \omega_1 L_2 = \omega_1 X_2 / \omega_s$,

$$T = \frac{E_2^2}{\omega_s^2} \cdot \frac{\omega_1 R_2 s_r}{R_2^2 + X_a^2 s_r^2} \quad , \tag{2.12}$$

Equation (2.12) has the same form as equation (2.8) and it therefore gives a torque/slip characteristic of the same shape, provided that E_2/N_s is maintained constant, as shown by the family of curves in Figure 2.4 for various values of s_s.

2.2 DIFFERENT SPEED CONTROL TECHNIQUES

The past decade has seen the development of many techniques suitable for the variable-speed control of a.c. motors in general and induction motors in particular. Different design requirements such as speed range, efficiency and maximum allowable losses, torque requirements, speed reversal, dynamic response, environmental and economic considerations, and accuracy of control are some of the factors which affect the choice between the different methods available.

Induction motors can have either a slip-ring, a squirrel-cage or a solid-iron rotor. Each has its particular area of application, in which different control techniques may be adapted. In drives where the speed normally varies only within a small range in the vicinity of the maximum value (for instance, in continuous rolling mills, blowers and marine propulsion), the preference is for slip-ring motors. For drives in dirty atmospheres, where corrosive vapours are present, or where there is a risk of explosion, squirrel-cage motors are mainly used. Some special loads may demand ultra-high speed drives, and when conventional laminated rotors with squirrel cages may not withstand the high centrifugal stresses involved a solid iron rotor structure is adopted. These and many other factors affect the choice of control techniques to be used.

Generally speaking, the frequency and the supply voltage must be controlled in harmony for a satisfactory speed control system. However, the exact relationship may depend on the purpose to which the motor is put. The torque produced depends on the magnitude of the rotating magnetic field and the rotor current, which in turn depends on the slip frequency and is reflected in the stator current. Hence, if the maximum rated torque of the motor is required at all speeds, the control system should be designed to maintain a constant flux density under all conditions. Over most of the speed range, this demands a voltage approximately proportional to frequency, but at very low speeds the voltage must be increased somewhat above the

proportional value. In some applications, it is necessary for the motor to be capable of generating a starting torque in excess of the normal full-load torque, when it is advantageous to increase the flux density at low frequencies by an increase in the voltage-to-frequency ratio. These two conditions are illustrated respectively in Figure 2.5.a and Figure 2.5.b, while a further mode of control that might be employed in, for example, a traction control system[5], is shown in Figure 2.5.c. This application requires a particularly high starting torque at low frequencies, which is facilitated by an increased voltage-to-frequency ratio. Above a certain frequency the ratio is kept constant, and remains so until near one-half maximum speed. However, beyond this speed the voltage is kept constant, and as the frequency and speed increase the stator flux and the available torque, fall.

Static frequency changers, incorporating either power transistors or thyristors as the switching elements, provide a particularly convenient means of fulfilling the above speed control requirements, and any others which are likely to arise. The voltage and frequency can be adjusted independently in two separate control blocks, or alternatively a single power controller can be employed. The supply can be either d.c. or a.c., which is a significant factor influencing the choice of control method.

2.2.1 Phase Angle Control

A high-frequency a.c. supply can easily be transformed to a low-frequency supply by phase angle control, which permits certain parts of the input voltage to appear at the output, as in Figure 2.6. Such a power controller is called a cycloconverter[6], with the required control exercised by suitable alteration of the angle α, as in Figure 2.6.d. For a limited speed range, or for certain special torque requirements, either the frequency or the output voltage of the cycloconverter can be fixed, with the speed controlled by changing only the other parameter. The resulting torque-speed

characteristics are as shown in Figure 2.7.a and 2.7.b.

The two characteristics of Figure 2.7 can be combined for simultaneous control of voltage and frequency, with the quantities controlled through the angle α. The frequency at which α is varied determines the output frequency but the time variation of α determines the total area under the voltage-time curve over an output cycle and hence the average and r.m.s. values.

Although this technique can be adapted to 3-phase systems, as shown in Figure 2.8, it has several disadvantages. Proportional control of voltage and frequency requires complex control circuitry and a minimum of eighteen switching components. The range of speed available is not very wide, with the upper frequency normally limited to about one third of the supply frequency by the increasing harmonic level of the output. Frequencies higher than the supply frequency can be obtained[7], but forced commutation of the switching elements is required with is attendant difficulties. Since the range of speed variation is limited, it is perhaps not surprising that cycloconverter and phase angle control techniques have found little application in the speed control of induction motors.

2.2.2 Rectifier-Inverter Control[8-10]

D.C. power is conveniently converted to a.c. power through an inverter. A 3-phase bridge arrangement is shown in Figure 2.9, in which the switching elements are assumed to be thyristors.

An ideal switch in series with a load fed from a d.c. supply would produce a rectangular voltage waveform across the load. For a 3-phase load, such as an induction motor, it is necessary to have a switching configuration to produce three separate voltages mutually displaced by 120^{o} in time. If the switching elements are numbered 1 to 6 as in Figure 2.9, the conduction sequence for each thyristor is as shown in Figure 2.10.a. Although the on and off time of each thyristor is shown as a half cycle, in

practice switching pulses appear every 1/6th of a cycle. This is explained in Figure 2.11.a and 2.11.b.

The basic inverter circuit of Figure 2.9 is made to provide a variable frequency 3-phase supply simply by changing the rate at which the conduction sequence of the thyristors change.

In inverter systems which employ thyristors as switching elements, the problem of commutation is very important and requires special attention to ensure satisfactory operation.

When thyristors are switched on, they remain so until turned off by some external means. Most inverters employ forced commutation techniques[11], in which a charged capacitor provides a reverse bias to block the particular thyristor and holds this on until the thyristor turns off. For low and medium power work, the inverter thyristors may all be switched off simultaneously, and having changed the conduction sequence by adjustment of the firing circuitry they may be switched on again. For high power work, the thyristors are usually switched off separately, to ensure reliability of the system. The charge required on the capacitor may be supplied from the d.c. supply feeding the inverter or, alternatively, from a quite separate external supply. An inverter controlled in this way will only change the frequency of the output; control of the voltage must be accomplished by different means.

One method of voltage control requires, the additional phase-controlled rectifier shown in Figure 2.12, to vary the voltage fed to the inverter. The main disadvantage of this is that it is difficult to provide reliable inverter commutation over a wide range of input voltages. At low voltages either large commutating capacitors are required to store sufficient energy for commutation or, as is usually the case, an auxiliary voltage supply is necessary, as shown in Figure 2.12. When the voltage level is low the controlled rectifier is likely to be in discontinuous conduction and a

smoothing LC filter is also required. This will result in a slow response system.

Figure 2.13 shows an alternative means of controlling the d.c. input to the inverter, where a 3-phase uncontrolled rectifier is followed by a chopper and a filter. This circuit has the advantage of a good power factor at the a.c. input, and a possibly faster response due to the smaller LC filter time constant on the output of a high-frequency chopper.

In both methods, the power delivered by the inverter is handled twice, once by the d.c. voltage control and once by the inverter, which means an increased number of components. A further disadvantage is the need for a separate commutation capacitor supply. The harmonic content of the output voltage contains a high proportion of both 5th and 7th components, which limits its use for low-speed control applications.

Instead of using two separate units, control can be accomplished by a single power unit controlled by pulse-width-modulation techniques[12-13]. A rectifier can supply a constant d.c. voltage to the inverter, with both the voltage and the frequency being controlled by the circuit of Figure 2.14. The harmonic content in the output is much reduced, and filtering is accomplished by the inherent time delays of the motor. The P.W.M. circuit has the advantages of good power factor to the a.c. line, fast response, no auxiliary rectifier supply and a low number of switching components. Regeneration to the d.c. supply is immediately possible, but regeneration to an a.c. bus requires another power controller.

2.2.3 Modulation Techniques[14]

The choice of the particular method of pulse width modulation rests on the requirements of the application. When high-frequency switching is necessary for an improved performance and for reduced losses in the motor, the switching losses in the inverter (due to the high operating frequency) must be kept to a minimum.

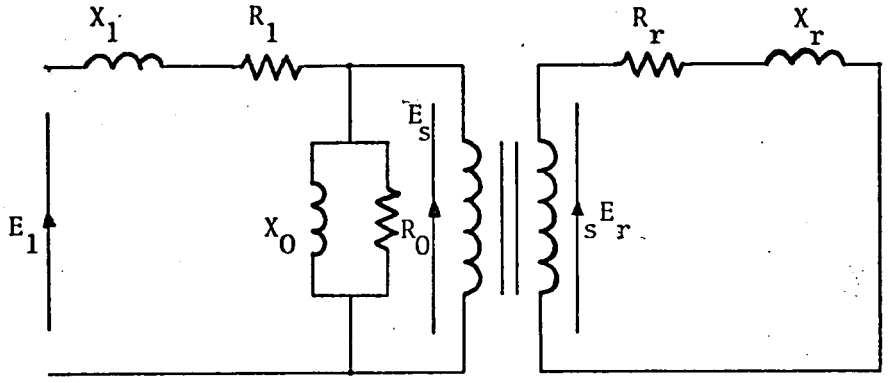
The basic method of voltage control is provided by the pulse width modulated square wave shown in Figure 2.15. The output waveform contains all odd harmonics of the fundamental, and these become large with respect to the fundamental at low output when the pulse width is very narrow. Under this condition the amplitude of the harmonic voltages approaches that of the fundamental, and the technique is only suitable for systems which do not require control down to very low speeds.

To reduce harmonics further, the number of pulses per cycle needs to be increased. Figure 2.16 shows the magnitudes of the harmonics of three pulse and ten pulse per half cycle systems. As the figure shows, the magnitudes of the harmonics are substantially reduced. As the number of pulses per half cycle is increased, the amplitudes of some higher harmonics become significantly greater, but such harmonics produce negligible current in a motor.

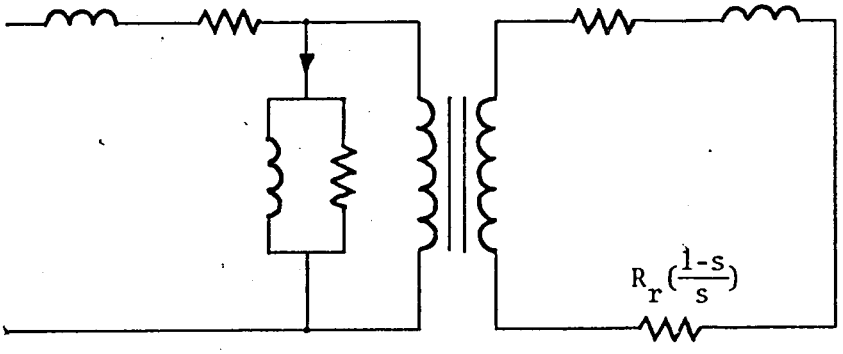
As more pulses are used the harmonic magnitudes are reduced further, although it also becomes more and more difficult to generate the required inverter sequencing. However, this technique can be used in conjunction with harmonic cancelling systems without increasing the number of inverters.

An improved modulation technique involves a sine wave envelope, and can be formed by the action of a comparator which mixes a sawtooth waveform with a reference sine wave, as shown in Figure 2.17.a. As can be seen from Figure 2.17.b, the harmonic level is reduced considerably and a much better approximation to a sine wave results.

However, additional problems may arise if the sawtooth waveform is not synchronized to the reference sine wave. In such cases, especially if the switching frequency of the inverter is low (which is the case if the switching element is a thyristor) the resulting waveform "jitters" and consequently contains even harmonics and a d.c. component. A high switching to output frequency ratio can eliminate this problem, but if this cannot be achieved (as is the case with thyristors) it is better to synchronize the two waveforms.



(a)



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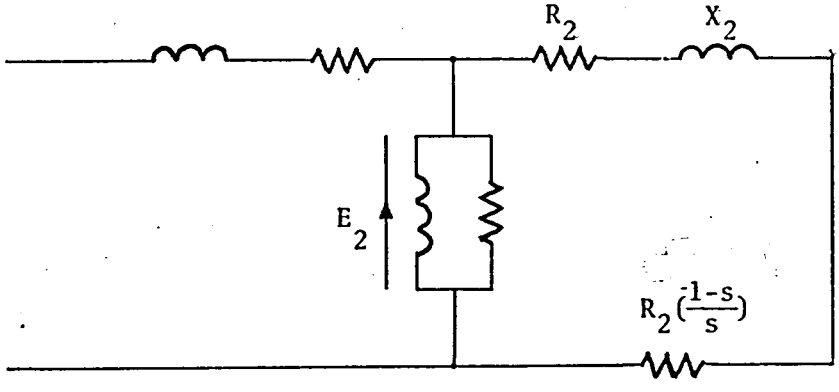
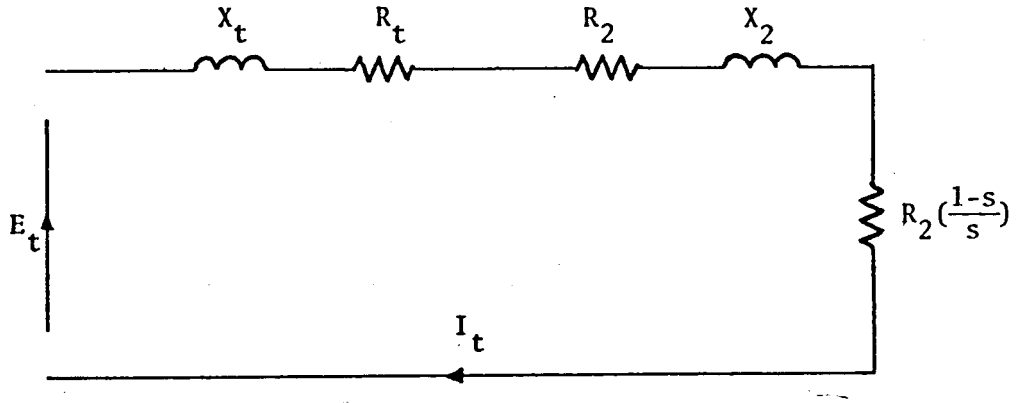


(c)



(d)

Figure 2.1: INDUCTION MOTOR EQUIVALENT CIRCUITS

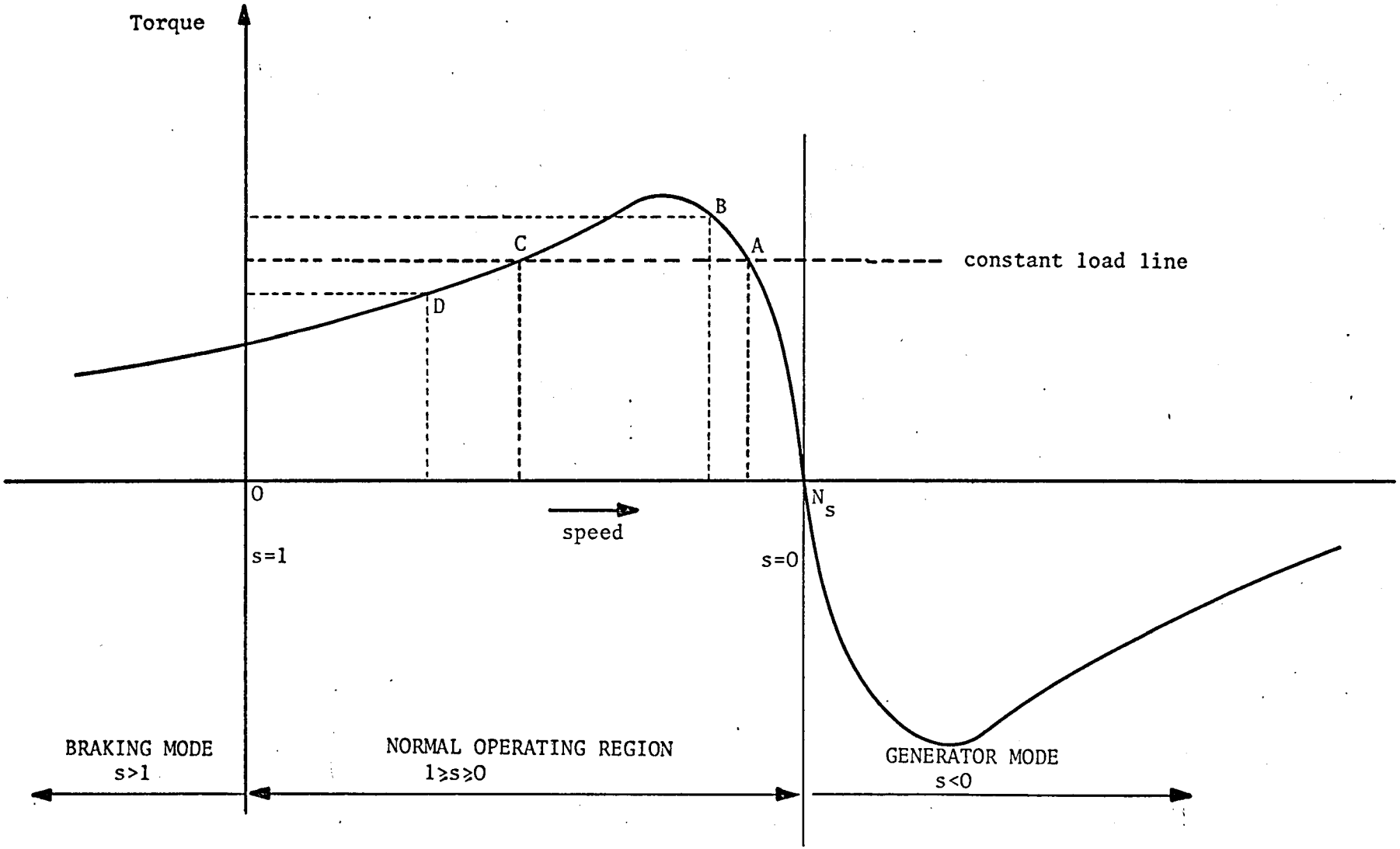


Figure 2.2: TORQUE SPEED CHARACTERISTICS OF AN INDUCTION MOTOR

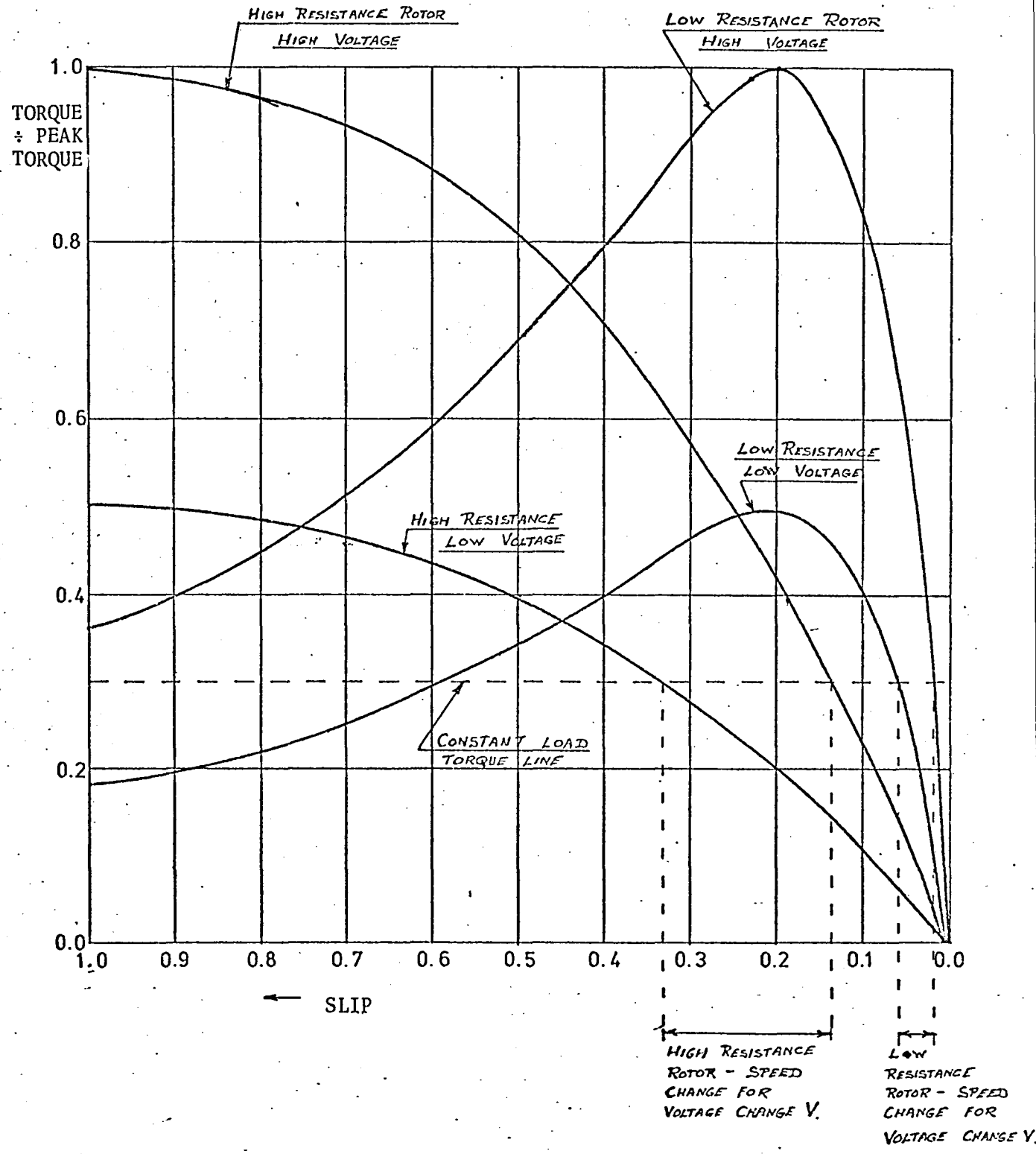


Figure 2.3: RELATIVE SPEED CHANGES FOR HIGH AND LOW RESISTANCE ROTORS SUBJECTED TO THE SAME VOLTAGE CHANGE

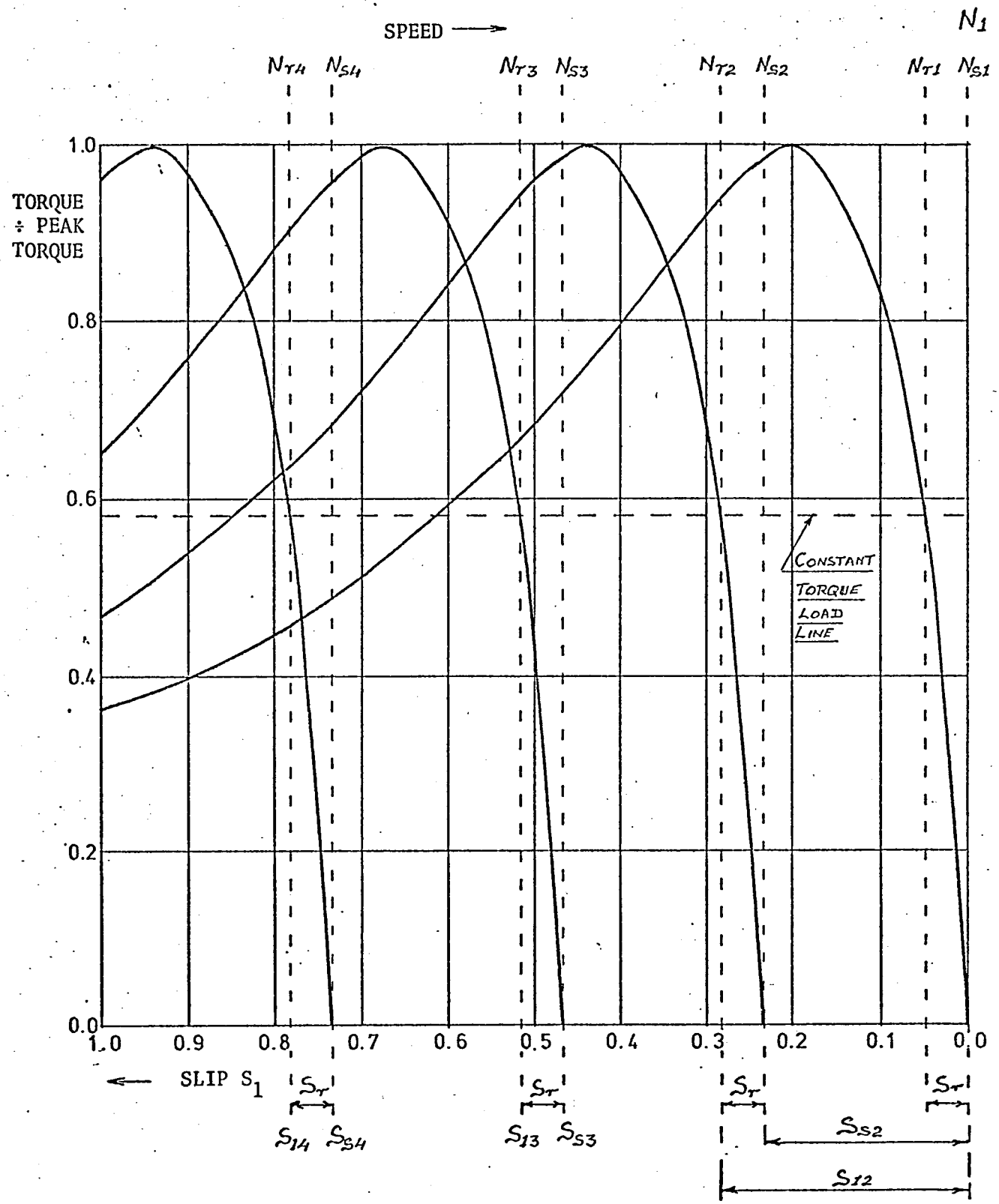
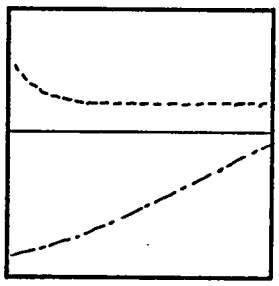
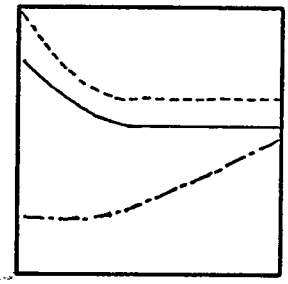


Figure 2.4: TORQUE-SLIP CURVES FOR VARIABLE FREQUENCY



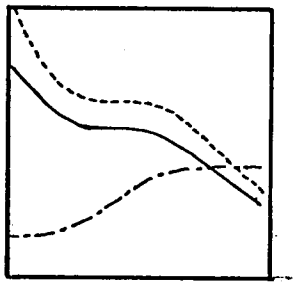
(a)

Rated Torque At All Speeds



(b)

High Torque At Low Speeds



(c)

High Torque At Low Speeds,
Low Torque At High Speeds

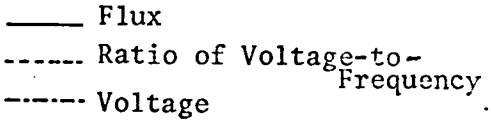


Figure 2.5: VARIATION OF MOTOR VOLTAGE AND FLUX WITH SPEED

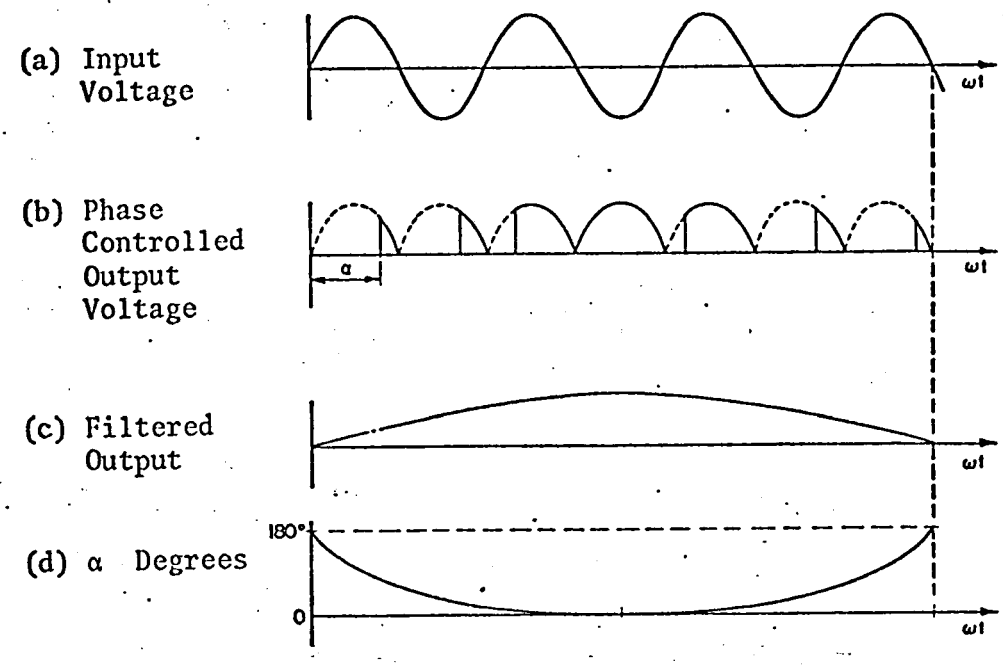
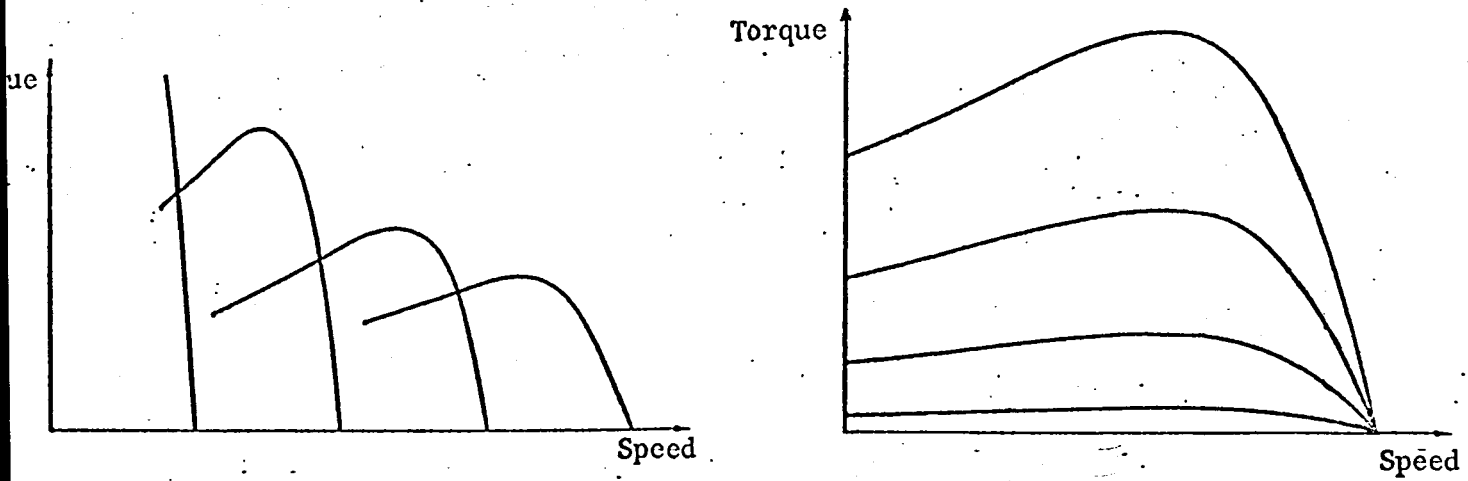


Figure 2.6: FREQUENCY CONTROL WITH A CYCLOCONVERTER



(a) Voltage Fixed Frequency Variable

(b) Frequency Fixed Voltage Variable

Figure 2.7: TORQUE-SPEED CHARACTERISTICS

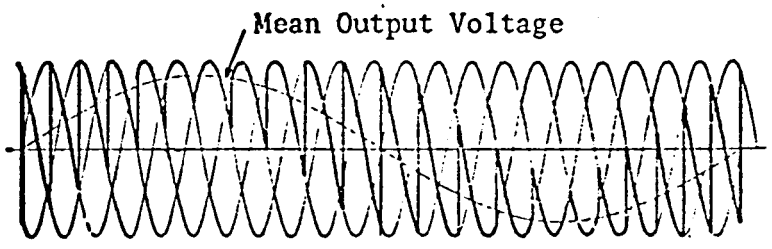


Figure 2.8: 3-PHASE CYCLOCONVERTER

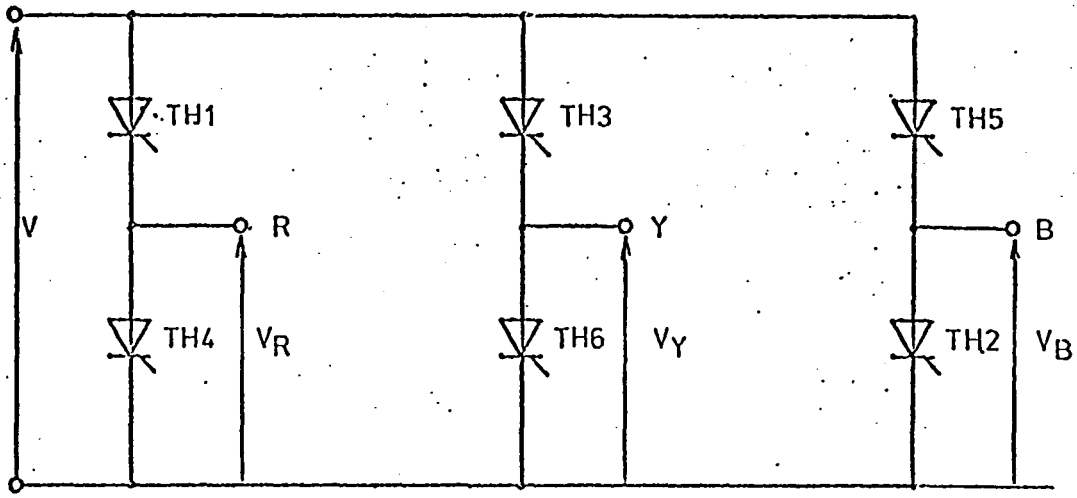
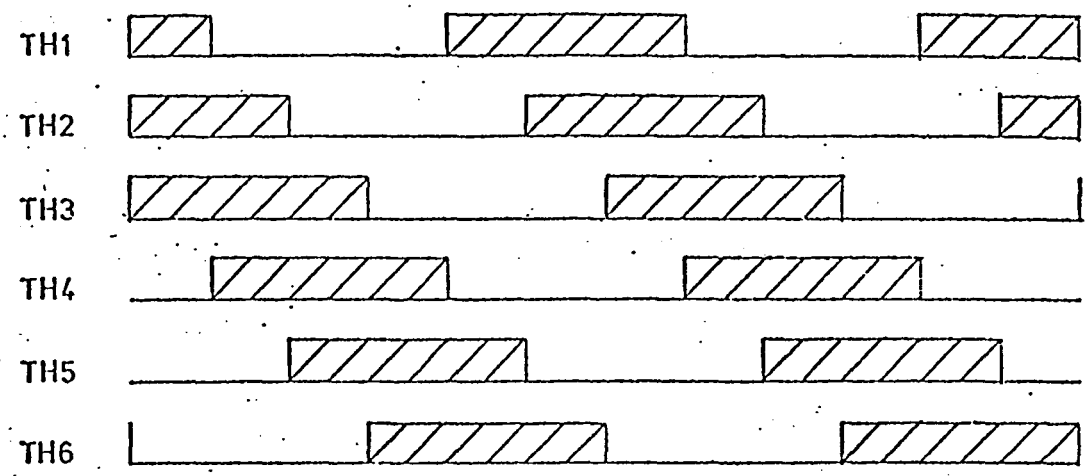
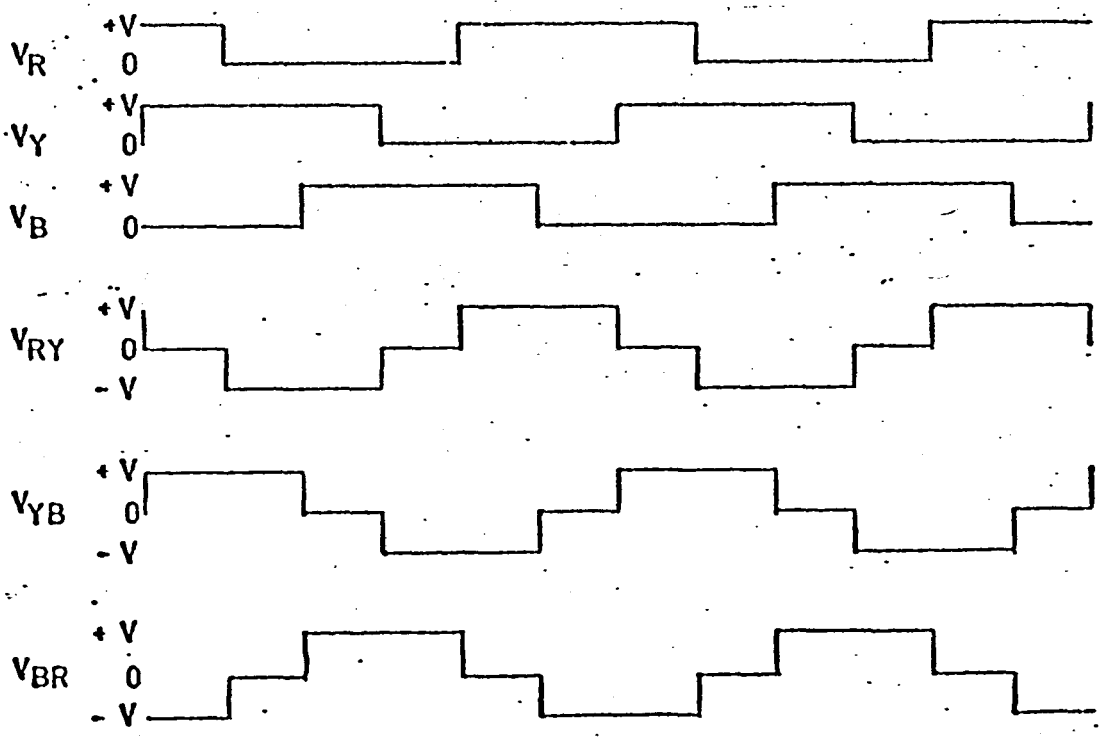


Figure 2.9: BASIC 3-PHASE INVERTER

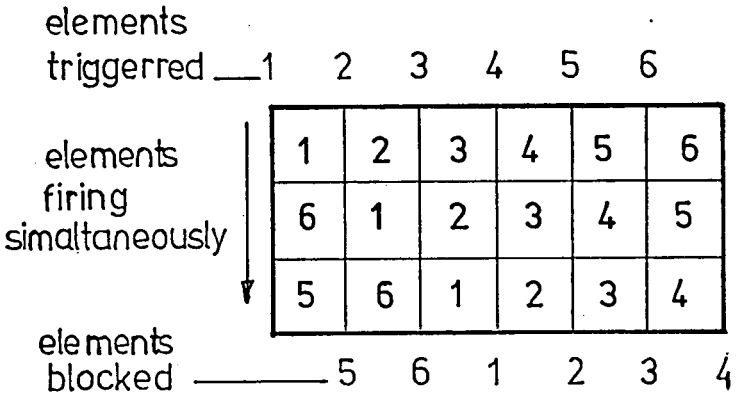


(a) Conduction Sequence

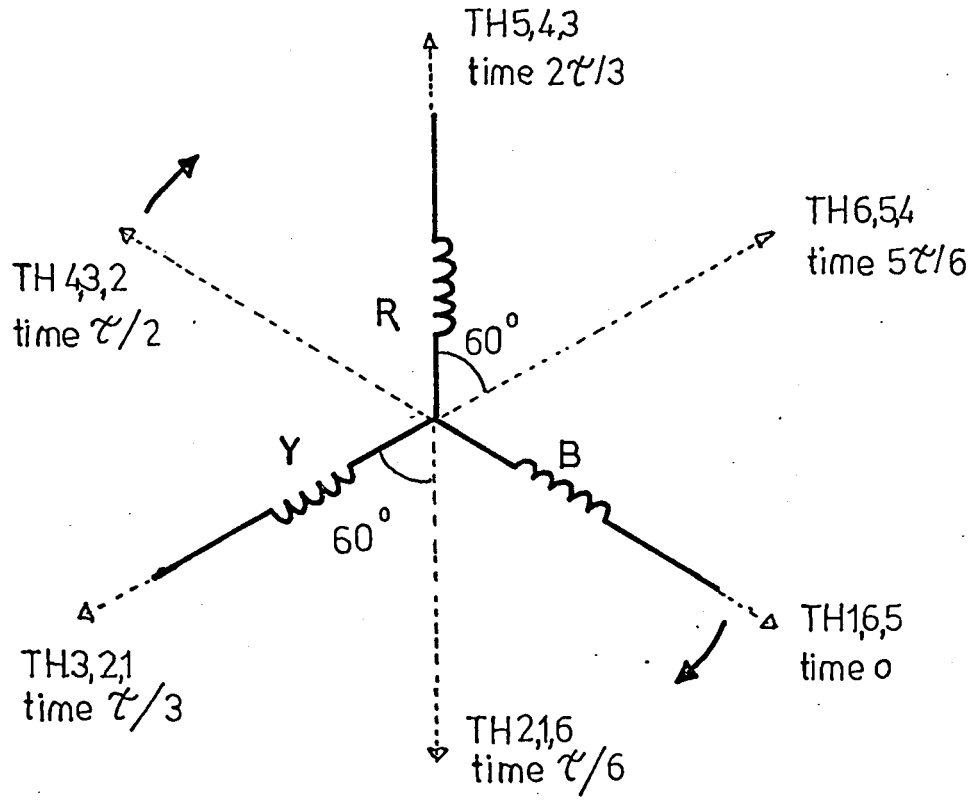


(b) Output Waveforms

Figure 2.10: INVERTER CONDUCTION SEQUENCE AND OUTPUT WAVEFORMS



(a) Conduction Sequence



(b) Stepped mmf. axes

Figure 2.11: Mmf IN SPACE W.R.T. WINDINGS AND THE THYRISTOR SWITCHING SEQUENCE
The six steps are displaced in time by π/3 radians.
The frequency is $1/\tau$

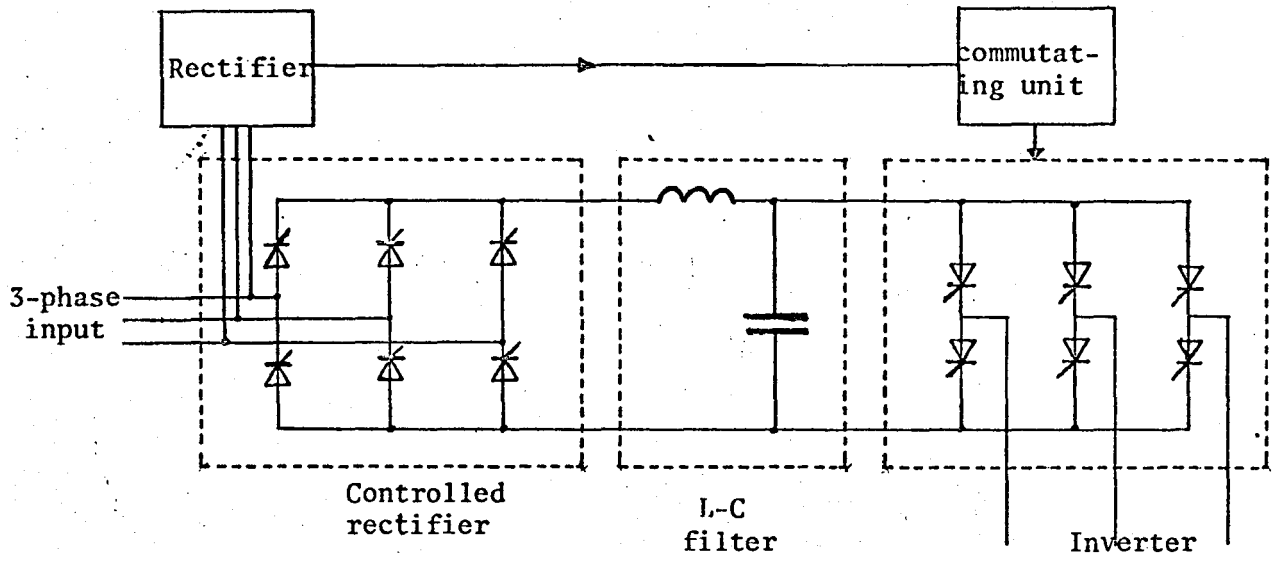


Figure 2.12: CONTROLLED RECTIFIER AND INVERTER

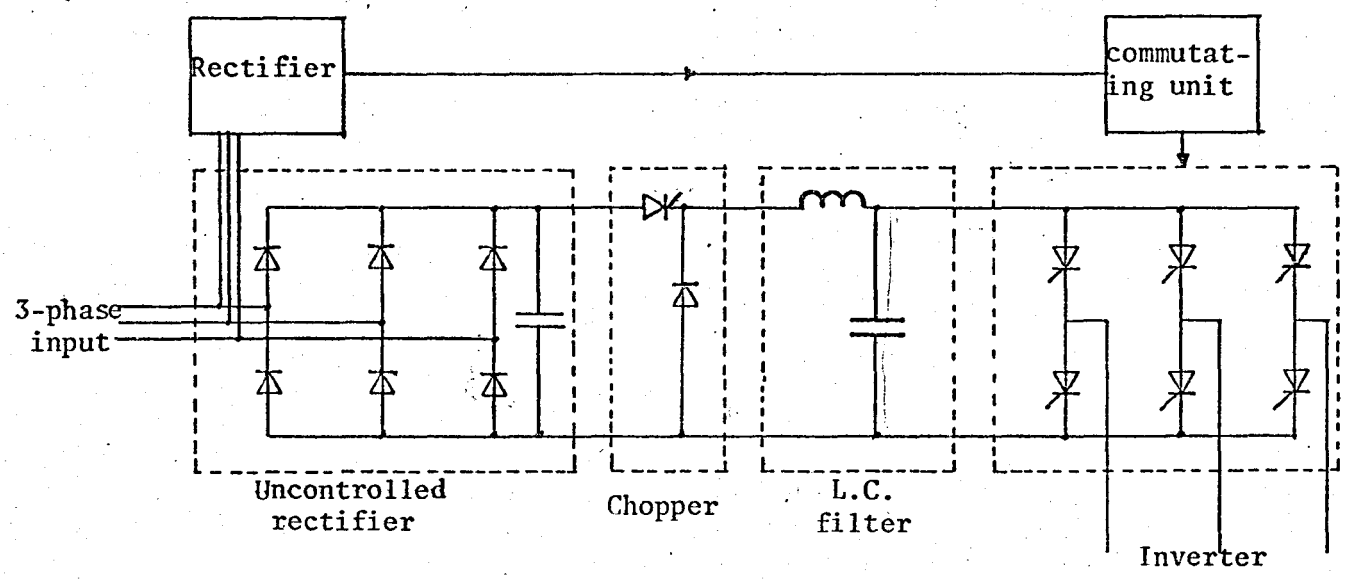


Figure 2.13: CHOPPER-INVERTER

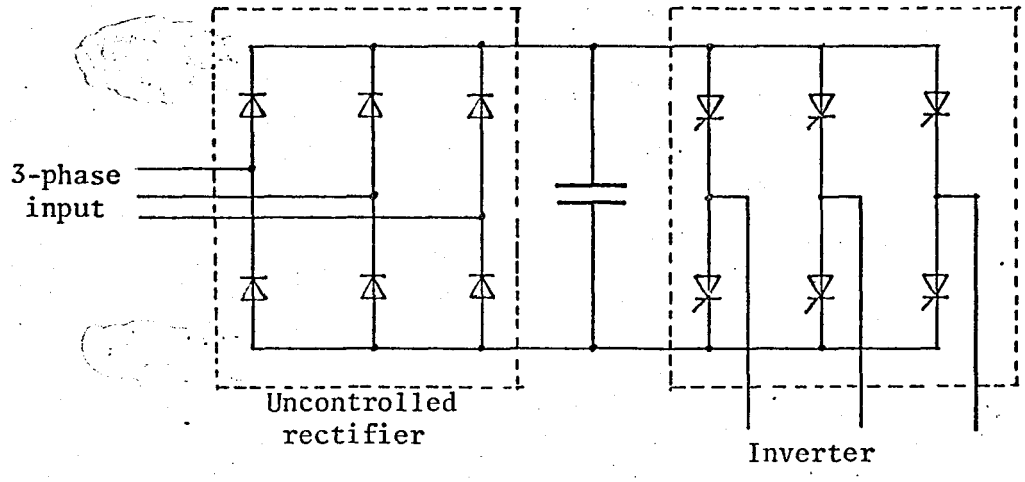
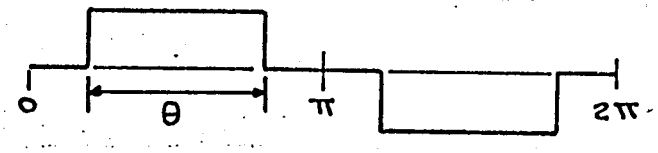


Figure 2.14: P.W.M. INVERTER



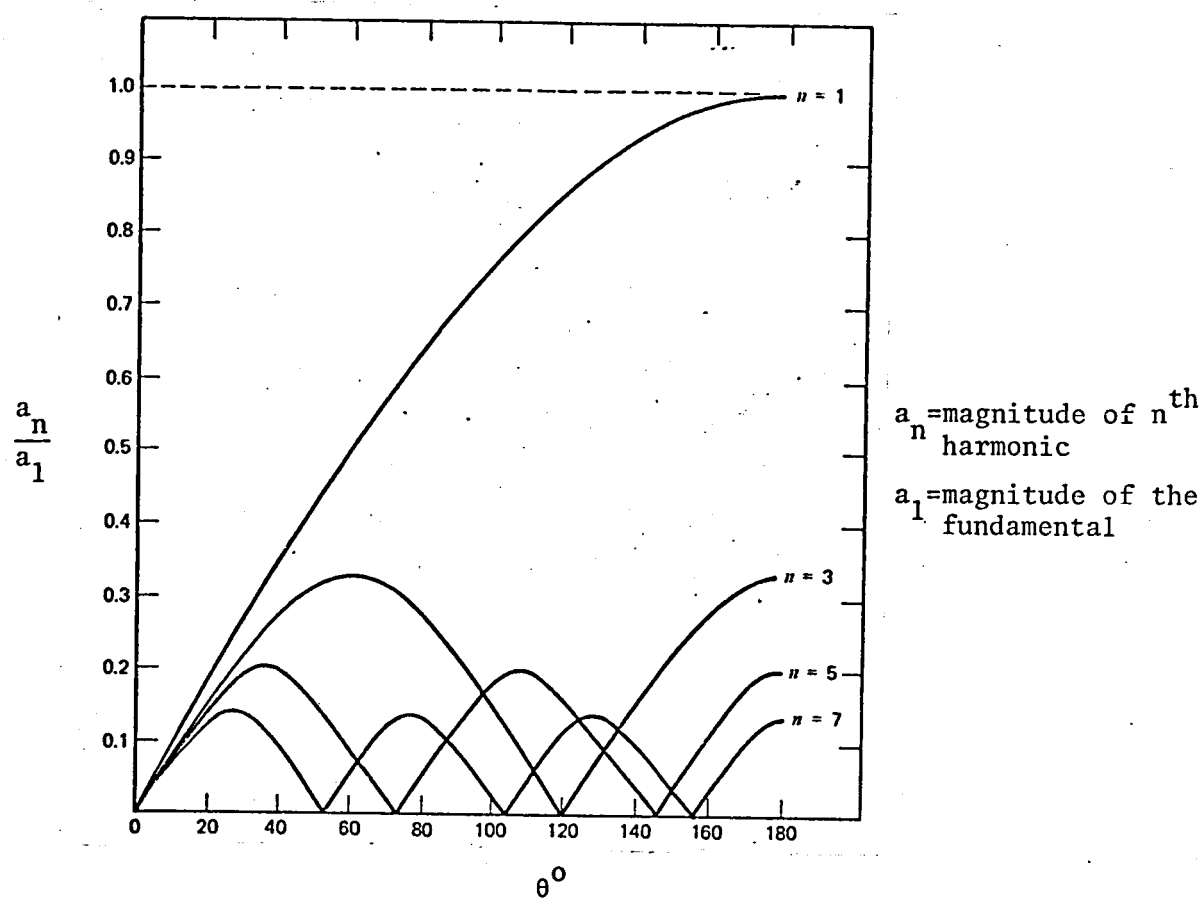


Figure 2.15: PULSE WIDTH MODULATED SQUARE WAVE AND HARMONIC CONTENT

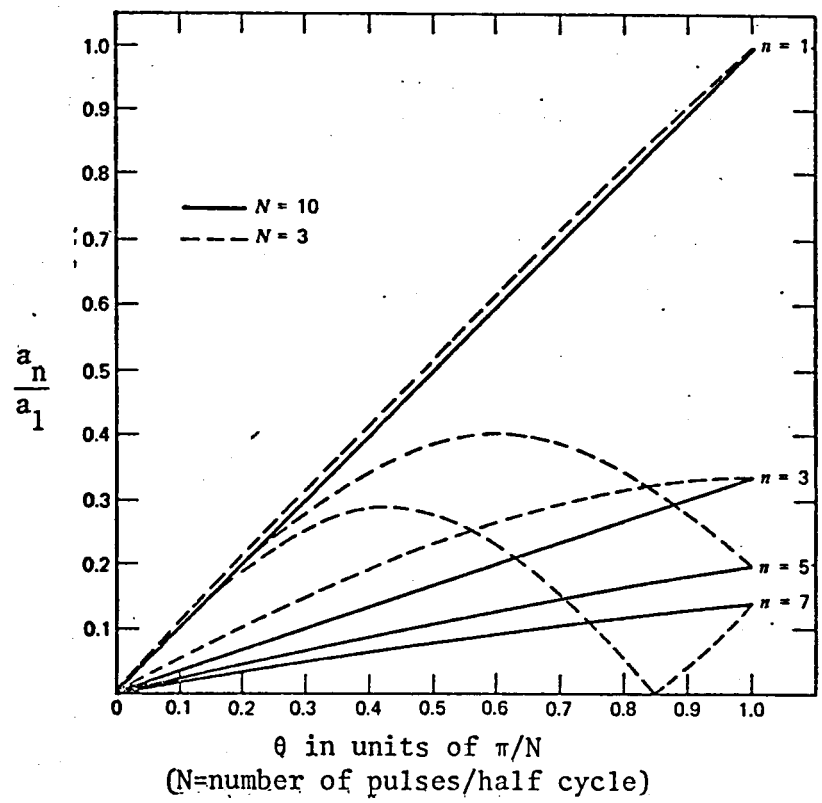
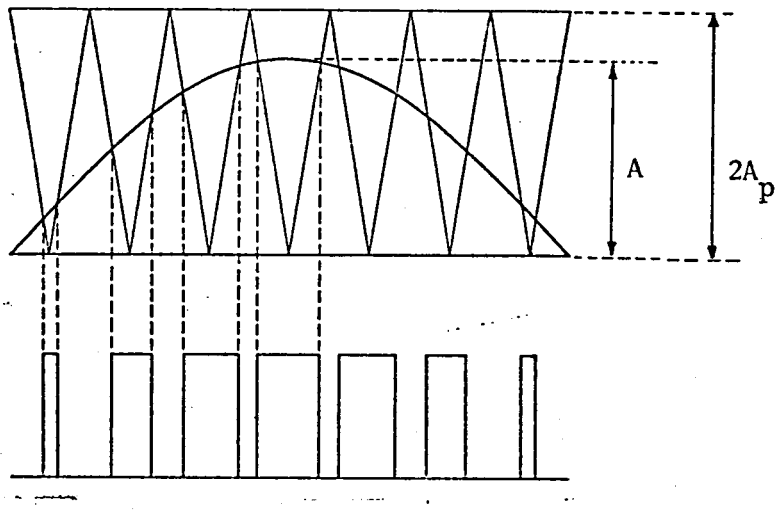
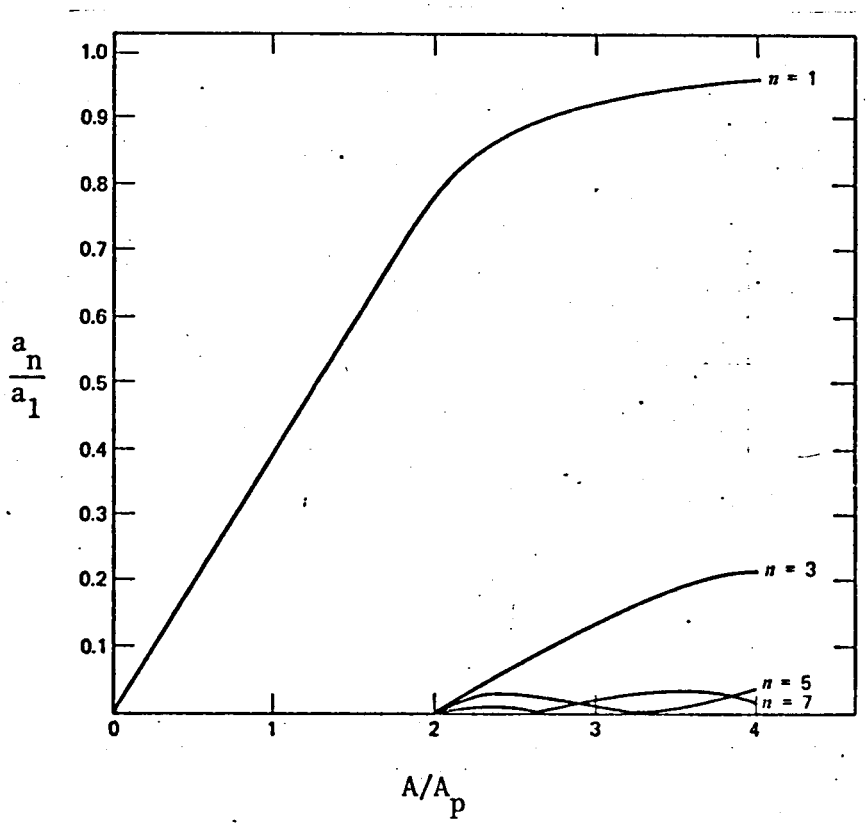


Figure 2.16: HARMONIC CONTENT OF THREE PULSE AND TEN PULSE PER HALF CYCLE SQUARE WAVE



(a) Sinusoidal Pulse Modulation



(b) Harmonic Content

FIGURE 2.17: SINUSOIDAL PULSE MODULATION

CHAPTER 3

DELTA MODULATION TECHNIQUES

3.1 DELTA MODULATION

Delta-modulation techniques[15-16] are well known in communication systems, where they are extensively used for the transmission of speech signals in binary form. The principles of operation and the behaviour of a delta-modulated system can easily be understood by consideration of Figure 3.1. Here, P.M. is a pulse modulator which passes pulses from the pulse generator P.G. to the network F_1, with one polarity if the voltage ε is positive and with the opposite polarity if ε is negative. The output signal e_1 of this network is compared with the signal e_0 to be transmitted, and the difference signal ε is applied to the modulator. If the network F_1 is chosen such that the system is stable, each pulse attempts to reverse the polarity of the difference signal ε, with the result that the mean difference between the information signal e_0 and the output signal e_1 of the feedback network F_1 is small.

Details of the system may be developed from the simple feedback circuit shown in Figure 3.2, containing a clipping amplifier A and a periodically operated switch S. Figure 3.3 shows the characteristics of four possible feedback systems where

a) A is linear and switch S permanently closed, so that V is normal, and continuous.

b) Switch S is closed periodically, so that V is quantised in time.

c) Amplifier A is used to clip the input, so that with S permanently closed V is quantised in amplitude.

d) Voltage V is quantised both in time and in amplitude, by the clipping amplifier A and the periodically operated switch S.

Thus, if a suitable integrating network is incorporated in the feedback loop this becomes a delta modulation system. A delta modulator coder and decoder are shown in schematic form in Figure 3.4.a and 3.4.b respectively.

The coder is seen to be a non-linear sampled data control system, in which the comparator compares the analog input signal i(t) with the integrated

version of the digitally encoded signal obtained from the modulator f(t), to decide which of the two has the larger amplitude. Although the comparison process is continuous, the digital output signal e(t) shows only the difference at a particular instant, and the term "delta" arises from this difference. If, at any instant of time, $i(t)>f(t)$, a "high" or "positive" output will result, but if $i(t)<f(t)$ the output is "low" or "negative". The analog signal i(t) thus results in the coder producing at its output a stream of binary pulses, of duration τ and amplitude +V or -V. Integration of these pulses gives f(t), and since the pulses are very narrow, f(t) consists of steps of magnitude $\gamma=V\tau$. For every positive pulse at the coder output f(t) increases by γ, and every negative pulse results in f(t) decreasing by γ. The value of the output O(t) is decided at regular clock instants, such that O(t) is given by,

$$O(t) = V \text{ sign } (i_r - f_r)$$

at the r^{th} sampling instant.

Suppose i(t) increases suddenly, causing e(t) to be positive for a number of clock periods. During this time s(t) is +V, and at each sampling instant a positive pulse is passed to the integrator causing f(t) to increase by γ. Eventually, when $f(t) > i(t)$, the error changes sign, and provided that $e(t)<0$ at the next sampling instant, a negative pulse is produced at the output of the modulator. This negative pulse reduces f(t) by γ, and for as long as $e(t)<0$ at each sampling instant, f(t) is decreased by γ until the error changes sign. The action of the modulator is thus to produce a waveform f(t) which tracks the input i(t), with a "step like" waveform which never differs from i(t) by more than $\pm\gamma$. This process is illustrated in Figure 3.5.

It can also be seen from Figure 3.5 that the rate of occurrence of the binary pulses at the output of the modulator is proportional to the instantaneous value of the slope of the input signal i(t). Thus, when the

slope of i(t) is positive, the output O(t) consists of more positive pulses than negative ones, and vice versa when the slope of i(t) is negative. When the magnitude of the slope of i(t) is small the pulses in the O(t) waveform frequently alternate, and when the slope of i(t) is zero, the O(t) waveform consists of pulses of alternate polarity. Figure 3.6 shows the waveforms at various points of the modulator, when a sine wave is present at the input.

In the previous analysis the integrator has been assumed ideal. In practice, the output pulses are of finite duration, and the response of an RC integrating network to these pulses is exponential rather than increasing in steps.

In Figure 3.4.b a delta modulation decoder is shown. As seen, the input is integrated and the function f(t) obtained. High frequency effects contained in the rising and falling parts of each f(t) step are removed by filtering f(t), by a filter whose frequency band is identical to the frequency band occupied by i(t).

As described, delta modulation contains information on the slope of the input signal, which means that d.c. signals cannot be encoded. Consideration of Figure 3.6 indicates that the output from a delta modulator must first be integrated, to recover the original signal, before it can be applied to a motor for speed-control purposes. However, following integration the delta-modulated signal becomes an analog signal, and since subsequent amplification requires a normal amplifier with biassed transistor elements, delta modulation is not suitable for the speed control of an induction motor.

However, this difficulty is easily overcome by integrating the input signal before it leaves the modulator, so as to generate output pulses carrying the information corresponding to the amplitude of the input signal. Delta-sigma (Δ-Σ) modulation is a realization of this principle, but before going into the behaviour and operation of Δ-Σ modulators it will

be useful to derive some of the parameters which are necessary for a better understanding of its use.

3.1.1 Derivation of the Overload Characteristic

An important aspect of delta modulation is the problem of overloading. Assuming an RC network is used for the integrator, the slope of the exponential response to a step input determines the maximum rate at which the integrator output can move. If either the amplitude or the frequency, or both, of the signal are raised sufficiently, its slope exceeds that of the exponential curve, when the modulator can no longer track the input signal and increased distortion will result. However, as long as the slope of the input signal is equal to or less than the slope of the exponential curve at the amplitude common to both, there will be an output from the coder which closely follows the input signal. By referring to Figure 3.7, and considering the two points A and B respectively on the exponential response leading to +V with time constant T and on the sine wave E sinωt of the same amplitude, and assuming the digitised levels of O(t) to be ±V, the slope of the exponential at amplitude v is

$$= \frac{V-v}{T}$$

and the slope of the sine wave at the same amplitude is

$$= \omega(E^2-v^2)^{\frac{1}{2}}.$$

The difference in slopes,

$$D = \frac{(V-v)}{T} - \omega(E^2-v^2)^{\frac{1}{2}}$$

which is a function only of v. The minimum difference occurs when

$$v = \frac{E}{(1+\omega^2T^2)^{\frac{1}{2}}}$$

and the value of D for this minimum condition is

$$D_{min} = \frac{V-E(1+\omega^2T^2)^{\frac{1}{2}}}{T}$$

The overload condition is given by $D_{min}=0$, when

$$E = \frac{V}{(1+\omega^2T^2)^{\frac{1}{2}}} \qquad (3.1)$$

which identifies the relation between E and ω and specifies the overload characteristic.

3.1.2 Derivation of the Threshold of Coding

In Figure 3.8 the "central delta step" is the change in the integrator voltage during one clock pulse period. The minimum amplitude below which the input fails to excite the modulator occurs when the peak-to-peak amplitude of the signal is smaller than the central delta step. The threshold of coding is defined as

$$E_{min} = \frac{\Delta v}{2}$$

where Δv is related to other parameters by

$$\Delta v = \frac{V}{T} \cdot \frac{1}{f_c}$$

and $$E_{min} = \frac{V}{Tf_c^2} \qquad T = \frac{1}{2\pi f_0}$$

where f_0 is the characteristic frequency of the integrator.

By substitution:

$$E_{min} = \frac{\pi V f_0}{f_c} \qquad (3.2)$$

and with the input dynamic range of the system defined as the ratio of the overload level to the threshold of coding:

$$\frac{E_{max}}{E_{min}} = \frac{V/(1+\omega^2T^2)^{\frac{1}{2}}}{\frac{\pi V f_0}{f_c}} = \frac{f_c}{\pi(f_0^2+f^2)^{\frac{1}{2}}} \qquad (3.3)$$

3.1.3 Quantisation Noise[17]

Quantisation noise arises as the reconstructed signal f(t) attempts to follow the original signal by successive approximations. Although it is normally defined as the difference or error between the input signal i(t) and the reconstructed signal f(t), it may also be defined as the

difference between i(t) and the final filtered output. The first of these will give a larger error signal and since there is no exact relation between i(t) and f(t) the difference signal will have a random variation.

When the input to the modulator is zero, the pattern of the digital output is 1010101. The integrator output is thus a triangular wave with peaks of $\pm\frac{\Delta v}{2}$, and the mean square difference between this and the input is $\frac{(\Delta v)^2}{12}$. This is the total error energy, and is contained in a line spectrum of the multiples of f_c. When a sine wave input is applied the error is greater.

3.1.4 Characteristics of Delta Modulation

The equations so far derived characterise the performance of a basic delta modulator. Reference to equations 3.1, 3.2 and 3.3 suggests that for the best performance the characteristic frequency f_0 of the integrator should be as small as possible. But (from equation 3.1) this may cause the overload characteristic to fall within the bandwidth of the input signal. In order to have a flat dynamic range, f_0 must be chosen to be either equal to or greater than the maximum input signal frequency.

The equations also suggest that the best modulator performance is obtained with a high clock frequency. Figure 3.9 shows the characteristics of a basic delta modulator, and it will be seen that for low frequencies amplitude overloading is dominant, and that as the frequency of the input sine wave increased the slope overload effect prevails.

3.2 DELTA-SIGMA MODULATION

To avoid differentiation of the input signal, an integrator can be included at the input to the delta modulator, when the output becomes coded with information on the amplitude of the input signal. This modification results in delta sigma modulation (Δ-Σ M) which, although similar to pulse code modulation, differs in that P.C.M. involves the

generation of an n-digit code, whereas since Δ-Σ M requires[18] only a single-digit code it is therefore much less complex.

The block diagram of a Δ-Σ modulator is shown in Figure 3.10, and the modulator operates as follows:

The quantiser produces an output of +V when e(t)>0 and -V when e(t)<0, and the output s(t) appears at sample times with a sampling interval T. The comparator combines the integrated analog input signal with the integrated version of the digitally encoded signal, to decide which of the two has the larger amplitude. Since the encoder functions in such a way that the output follows the input, the analogue input is converted to a digital signal.

Noting that

$$e(t) = \int i(t)dt - \int O(t)dt$$

$$= \int [i(t) - O(t)]dt$$

we can replace the two separate integrators in the block diagram of Figure 3.10 by a single integrator in the forward path, leading to the simplified block diagram shown in Figure 3.11.

Figure 3.12 shows the output of a Δ-Σ modulator, for a staircase input. As seen, the output contains information on the level of the input amplitude. When no input signal is applied, the modulator is said to be idling, and Figure 3.13 shows the corresponding wave forms at different parts of the circuit. As can be seen from the figure, the output consists of pulses with a frequency of one-half the clock rate, where the clock rate is the frequency of the switch. The mean output of the modulator when idling is zero.

3.2.1 Derivation of the Overload Characteristic

By applying the same argument as in 3.1.1, the slope of the exponential at an amplitude v is $\frac{V-v}{T}$, and the slope of the output from the

RC integrator at the modulator input is

$$\frac{dV}{dt} = \frac{\omega E\cos\omega t}{(1+\omega^2T^2)^{\frac{1}{2}}} = \frac{\omega}{(1+\omega^2T^2)^{\frac{1}{2}}} \cdot [E^2-v^2(1+\omega^2T^2)]^{\frac{1}{2}}$$

The difference D is

$$D = \frac{V-v}{T} - \frac{\omega}{(1+\omega^2T^2)^{\frac{1}{2}}} \cdot [E^2-v^2(1+\omega^2T^2)]^{\frac{1}{2}}$$

which must be equal to or greater than zero to avoid overloading. By differentiating D with respect to v, and equating to zero, we obtain

$$v = \frac{E}{1+\omega^2T^2}$$

and substituting this into the above equation and putting $D_{min}=0$ the limit of the non-overload condition is obtained as

$$E = E_{max} = V \quad . \tag{3.4}$$

This result illustrates the advantage of Δ-Σ modulation, in providing an overload characteristic independent of the input signal frequency.

3.2.2 Derivation of the Threshold of Coding

With Δ-Σ modulation the threshold of coding is modified, although it still remains related to the central step size Δv, where

$$\Delta v = \frac{V}{T} \cdot \frac{1}{f_c} = \frac{2\pi V f_0}{f_c}$$

With an input signal $i(t)=E\sin\omega t$, the peak output from the input RC integrator is $E/(1+\omega^2T^2)^{\frac{1}{2}}$, so that using the definition of the threshold of coding

$$\frac{E}{(1+\omega^2T^2)^{\frac{1}{2}}} = \frac{\Delta v}{2} = \frac{\pi V f_0}{f_c} \quad ,$$

or

$$E = E_{min} = (1+\omega^2T^2)^{\frac{1}{2}}\pi V f_0 \quad . \tag{3.5}$$

The input dynamic range of the modulator is given by

$$\frac{E_{max}}{E_{min}} = \frac{V}{(1+\omega^2T^2)^{\frac{1}{2}}\pi V f_0} = \frac{f_c}{\pi f_0(1+\omega^2T^2)^{\frac{1}{2}}}$$

or
$$\frac{E_{max}}{E_{min}} = \frac{f_c}{\pi(f_0^2+f^2)^{\frac{1}{2}}} \qquad (3.6)$$

It will be seen that, unlike the overload characteristic, the threshold of coding is frequency dependent, and that it increases with the input signal frequency. However, comparison of equations (3.3) and (3.6) shows that the input dynamic range is the same as that of the basic delta modulator.

3.2.3 Characteristics of Delta Sigma Modulation

Although Δ-Σ modulation has the flat overload characteristic specified by equation (3.4), and is limited only by the digital levels ±V, the threshold of coding is not flat and varies with the input signal frequency. At frequencies above the cut-off frequency of the integrator f_0, the threshold of coding increases, and the value of the time constant T is therefore dependent on the input signal bandwidth.

Reference to equation (3.5) indicates that reducing V reduces the threshold of coding and increases the dynamic range. However, for stable operation of the comparator, V cannot be reduced below a minimum voltage. Figure 3.14 shows the characteristics of Δ-Σ modulation, and it is clear that as the frequency increases the threshold of coding approaches the overload level.

3.3 DELTA SIGMA MODULATION WITH DOUBLE INTEGRATION

The performance of delta sigma modulators can be improved by using a second integrator immediately following the first, both to reduce the quantisation noise and to increase the dynamic range at high frequencies. The integrator required is shown in Figure 3.15, for which the transfer function is

$$H(f) = \frac{1+j\ f/f_3}{(1+j\ f/f_1)(1+j\ f/f_2)} \qquad (3.7)$$

where,

$$f_1 = \frac{1}{2\pi R_1 C_1 (1+C_2/C_1)} \tag{3.8}$$

$$f_2 = \frac{1}{2\pi R_2 C_2 [1-\frac{1}{4}(1+\frac{R_1}{R_2})^2 \frac{R_2 C_2}{R_1 C_1}]} \tag{3.9}$$

$$f_3 = \frac{1}{2\pi r C_2} \tag{3.10}$$

The magnitude of H(f) is,

$$|H(f)| = \frac{f_1 f_2 \left(1+\frac{f^2}{f_3^2}\right)^{\frac{1}{2}}}{[(f_1^2+f^2)(f_2^2+f^2)]^{\frac{1}{2}}}$$

which reduces to,

$$|H(f)| = \frac{f_1 f_2}{[(f^2+f_1^2)(f^2+f_2^2)]^{\frac{1}{2}}} \tag{3.11}$$

if f_3 is large.

3.3.1 Overload Level

The condition for the overload level is given by

$$E_{max} = V|H(f)|.|H^{-1}(f)| = V \tag{3.12}$$

where V is the level of the digital sequence and $|H(f)|$ is given by equation (3.11).

3.3.2 Threshold of Coding

$E|H(f)| = \Delta v/2$, is the condition for the threshold of coding.

Thus,

$$\frac{E f_1 f_2}{(f^2+f_1^2)^{\frac{1}{2}}(f^2+f_2^2)^{\frac{1}{2}}} = \frac{\Delta v}{2} = \frac{16 V f_1 f_2}{\pi f_c^2}$$

or $$E = E_{min} = \frac{16V(f^2+f_1^2)^{\frac{1}{2}}(f^2+f_2^2)^{\frac{1}{2}}}{\pi f_c^2} \tag{3.13}$$

The dynamic range is determined by E_{max}/E_{min}, as

$$\frac{E_{max}}{E_{min}} = \frac{\pi f_c^2}{16(f^2+f_1^2)^{\frac{1}{2}}(f^2+f_2^2)^{\frac{1}{2}}} \tag{3.14}$$

3.3.3 Characteristics of Delta Sigma Modulation with Double Integration

The equations derived in the sections above characterise the performance of Δ-Σ modulators with double integration. The input dynamic range of a Δ-Σ modulator with double integration is proportional to the square of the clock frequency (equation 3.14), whereas in the case of a single integration it is proportional only to the clock frequency (equation 3.6).

The signal-to-quantisation noise of Δ-Σ modulation with a single integration is derived in Appendix 1 as

$$\frac{S}{N_q} = \frac{3}{4\pi^2} \frac{(f_c)^3}{(B)^3} \quad \text{for } f_0 \ll B \tag{3.15}$$

where B is the low-pass filter bandwidth in the decoder. In the same Appendix, the signal-to-noise ratio with double integration is shown to be

$$\frac{S}{N_q} = \frac{f_c^5}{12.888B^3(3B^2+5f_c^2)} \tag{3.16}$$

with the quantisation noise for single and double integration being

$$N_q = \frac{2\pi^2 V^2 (B)^3}{3(f_c)^3} \tag{3.17}$$

and

$$N_q = \frac{6.144B^3V^2}{f_c^5} .(3B^2+5f_2^2) \tag{3.18}$$

respectively.

As can be seen from equations 3.17 and 3.18, the quantisation noise is decreased by using a Δ-Σ modulator with a double integrator. It is inversely proportional to the fifth power of the clock frequency and proportional to the fifth power of the low-pass filter bandwidth. In both cases increasing the clock frequency will therefore give a much better dynamic range.

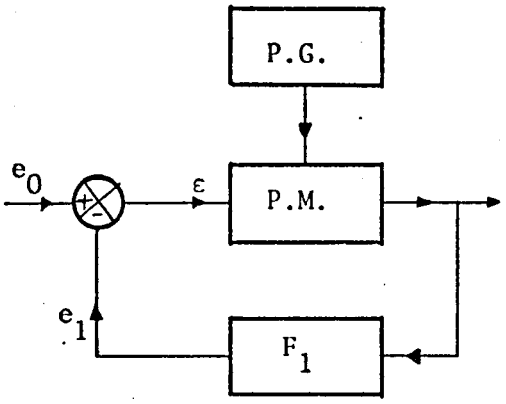


Figure 3.1: BASIC DELTA MODULATION SYSTEM

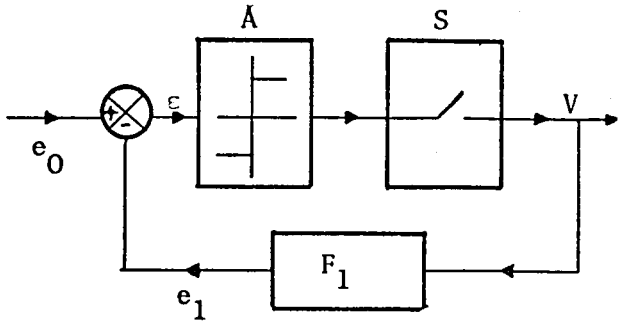


Figure 3.2: THE SIMPLE FEEDBACK CIRCUIT

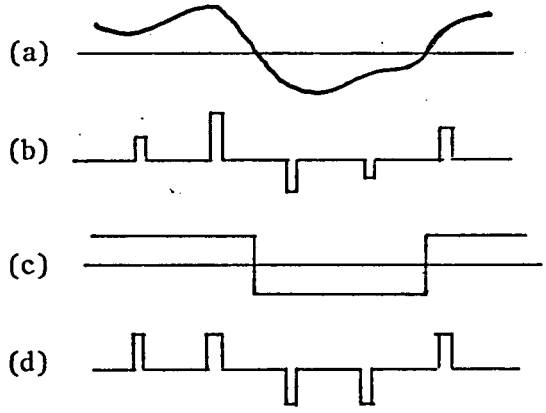


Figure 3.3: THE FORM OF THE VOLTAGE V IN FIGURE 3.2

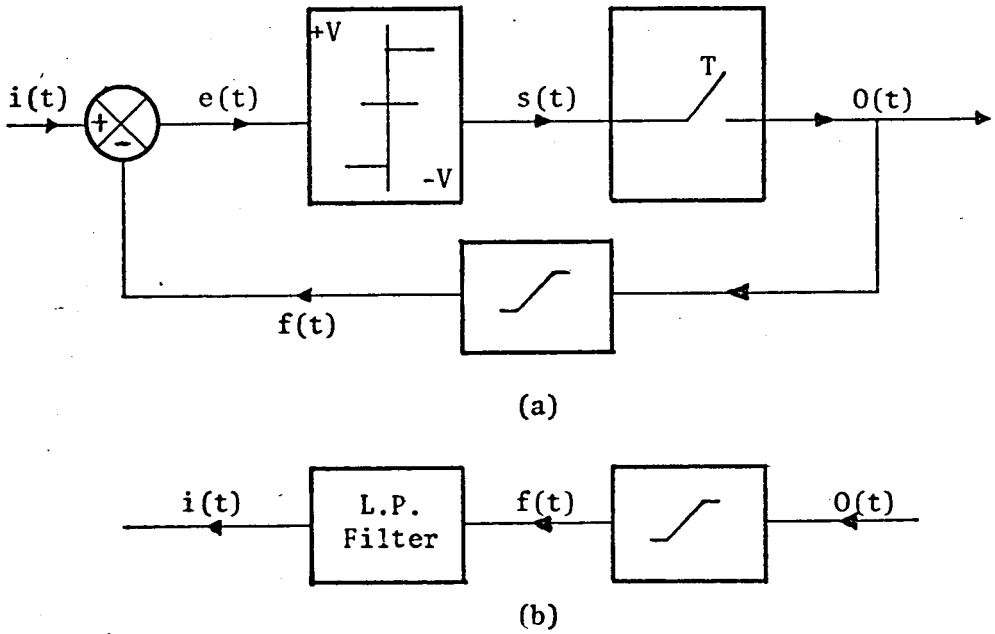


Figure 3.4: DELTA MODULATOR CODER AND DECODER

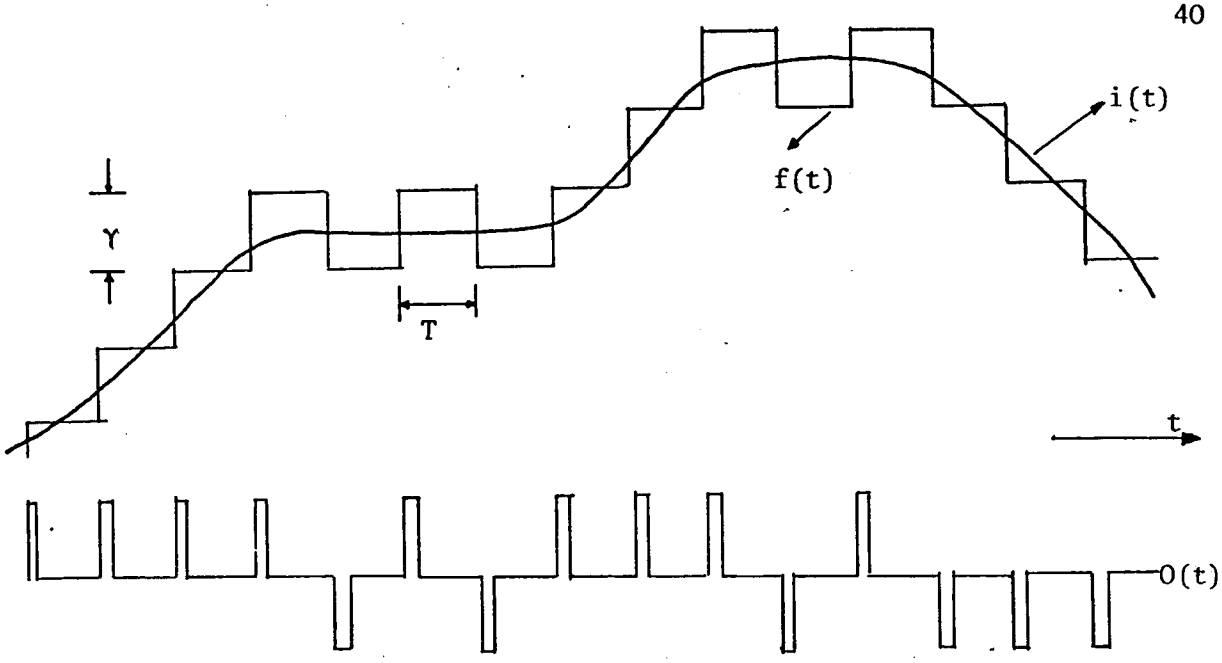


Figure 3.5: BEHAVIOUR OF DELTA MODULATOR

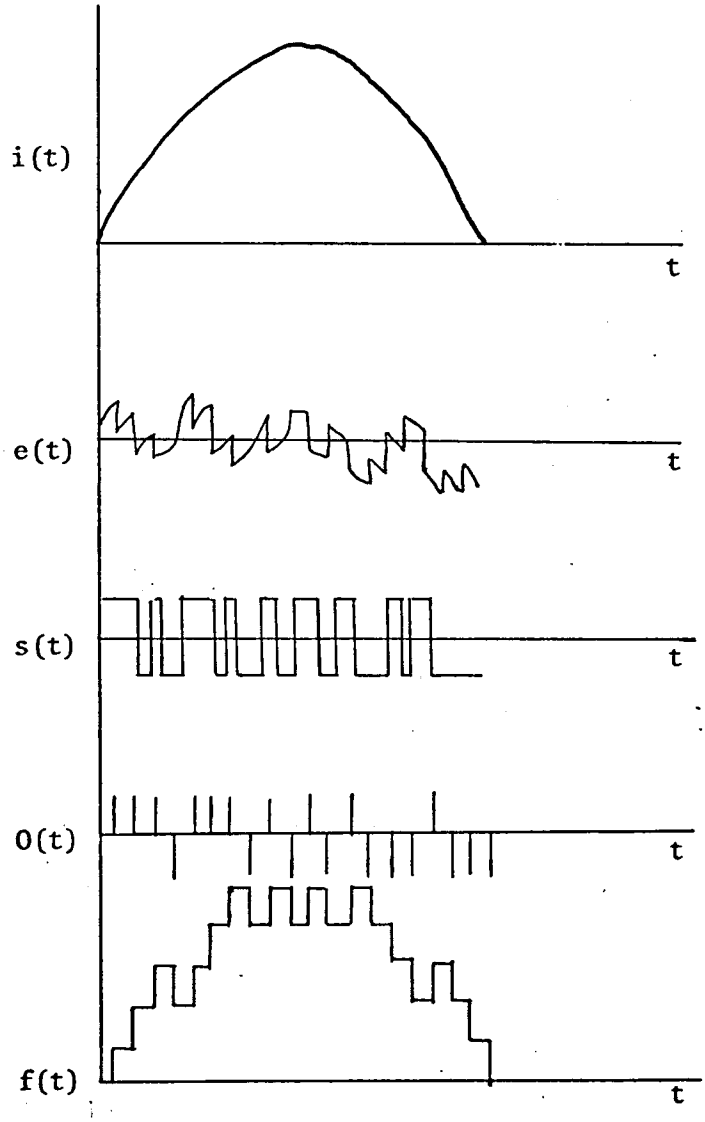


Figure 3.6: WAVEFORMS AT VARIOUS POINTS OF DELTA MODULATOR WITH SINE WAVE INPUT

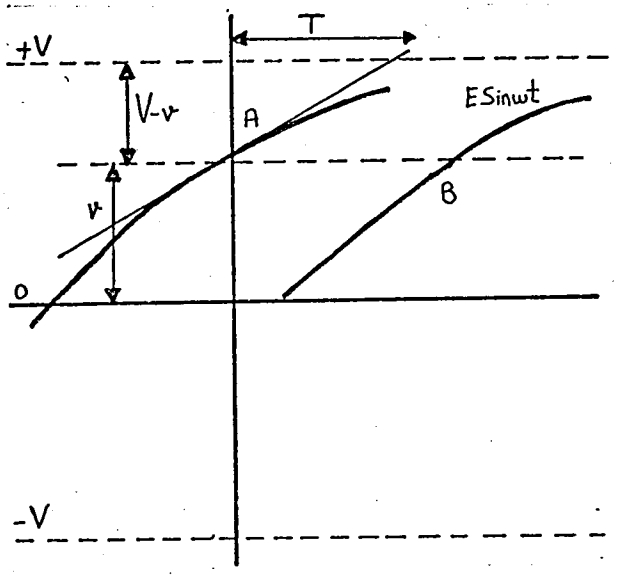


Figure 3.7: OVERLOAD CHARACTERISTIC

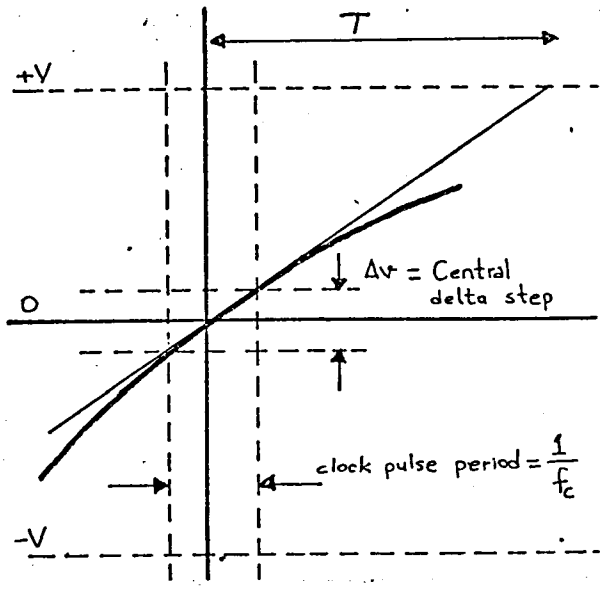


Figure 3.8: THRESHOLD OF CODING

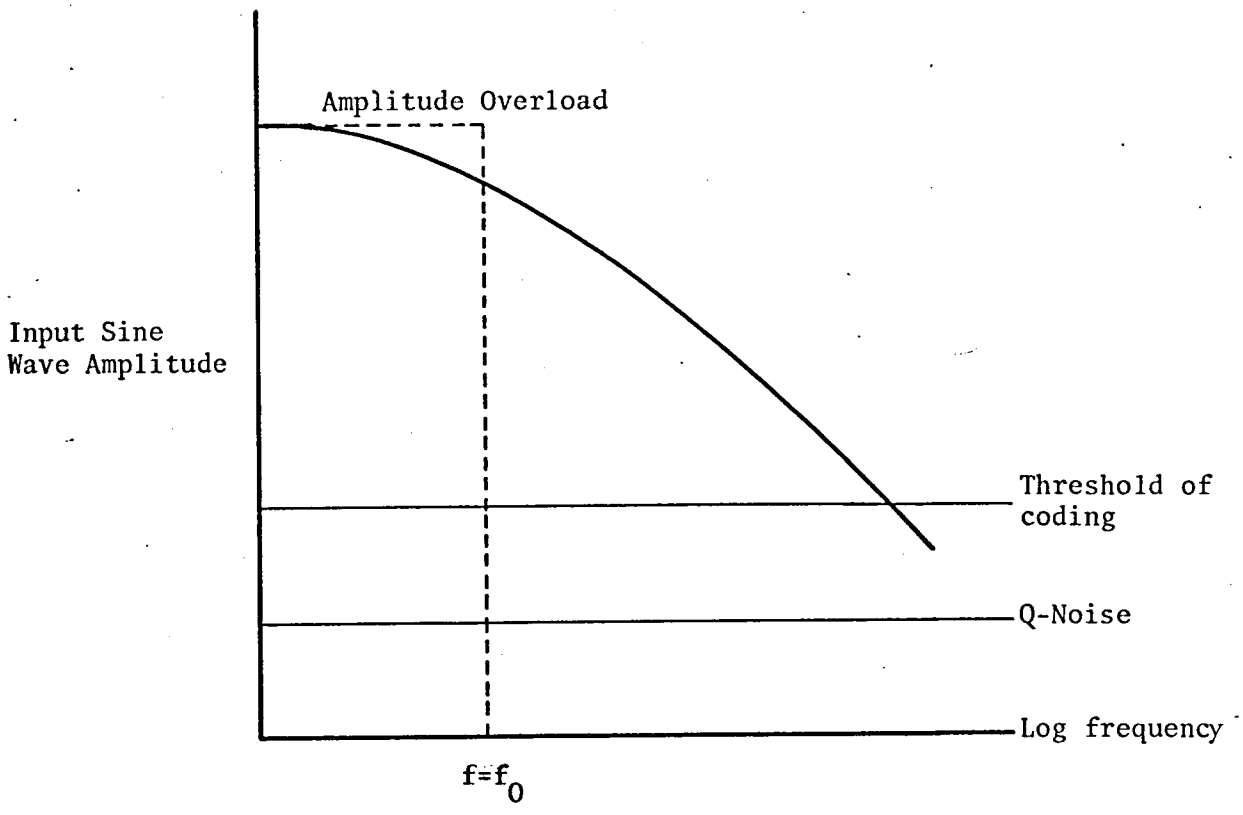


Figure 3.9: CHARACTERISTICS OF DELTA MODULATOR

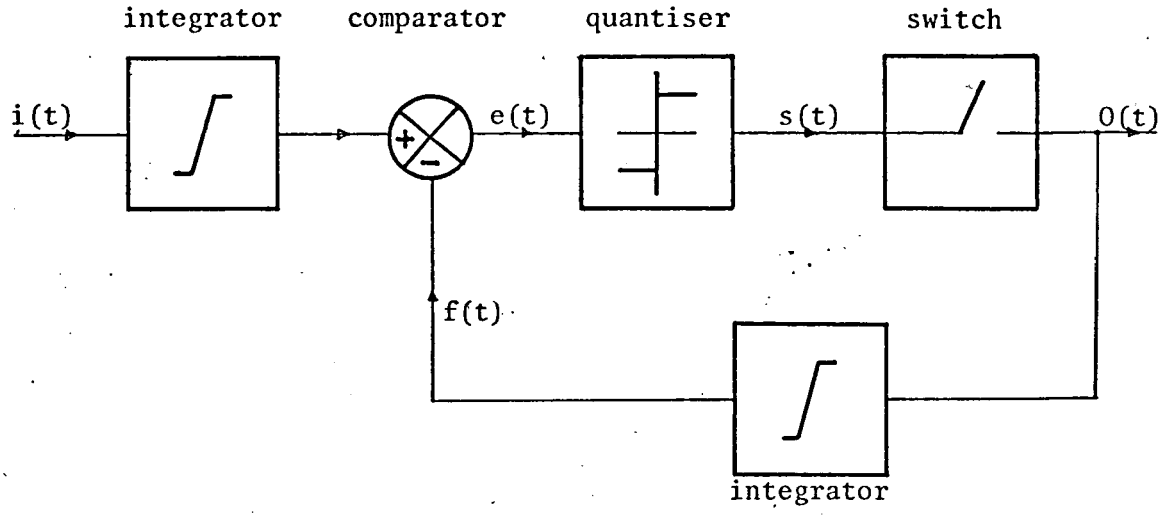


Figure 3.10: BLOCK DIAGRAM OF Δ-Σ MODULATOR

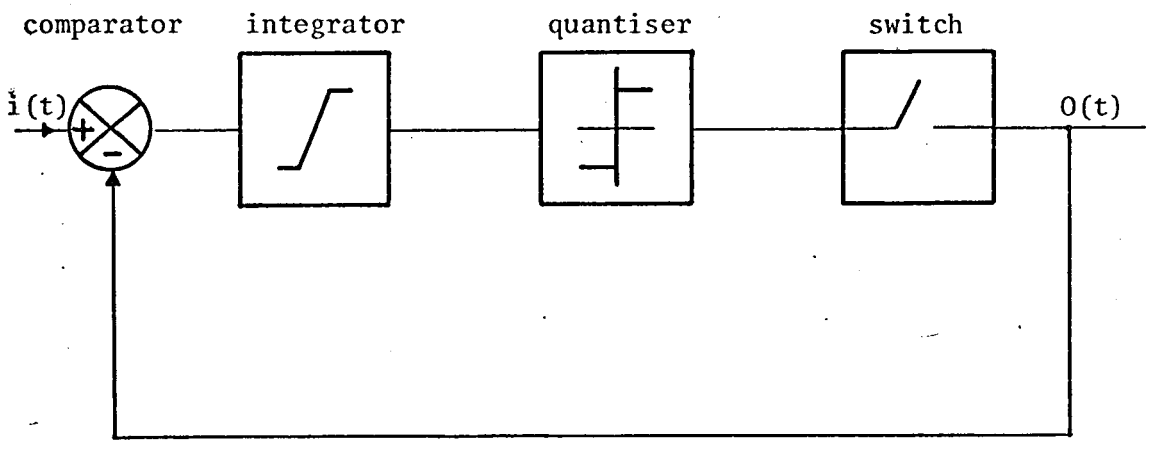


Figure 3.11: SIMPLIFIED BLOCK DIAGRAM OF Δ-Σ MODULATOR

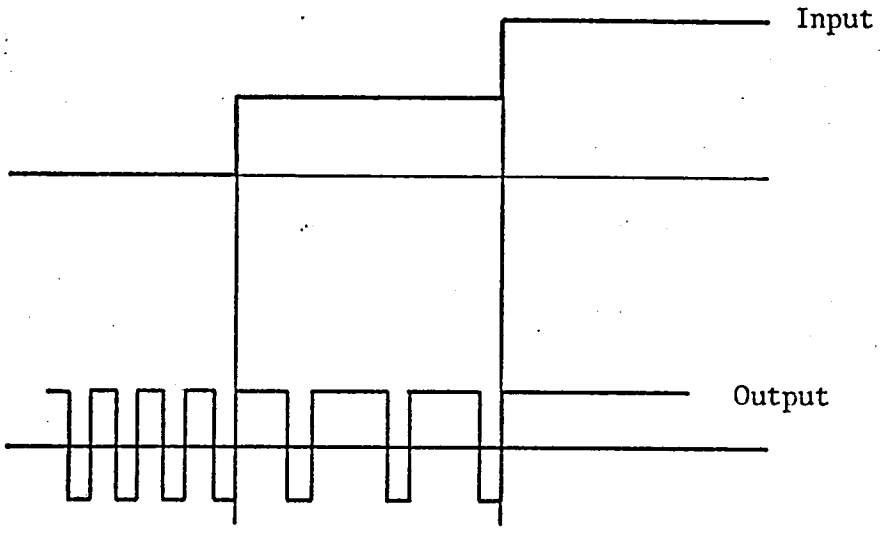


Figure 3.12: THE OUTPUT OF Δ-Σ MODULATOR FOR A STAIRCASE INPUT

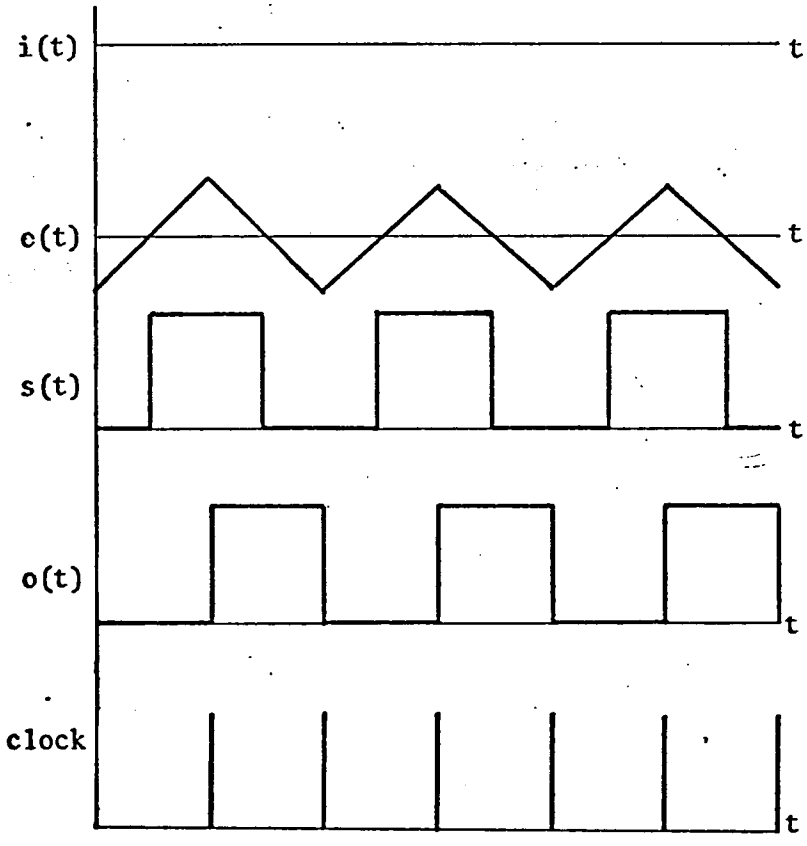


Figure 3.13: WAVEFORMS AT IDLING

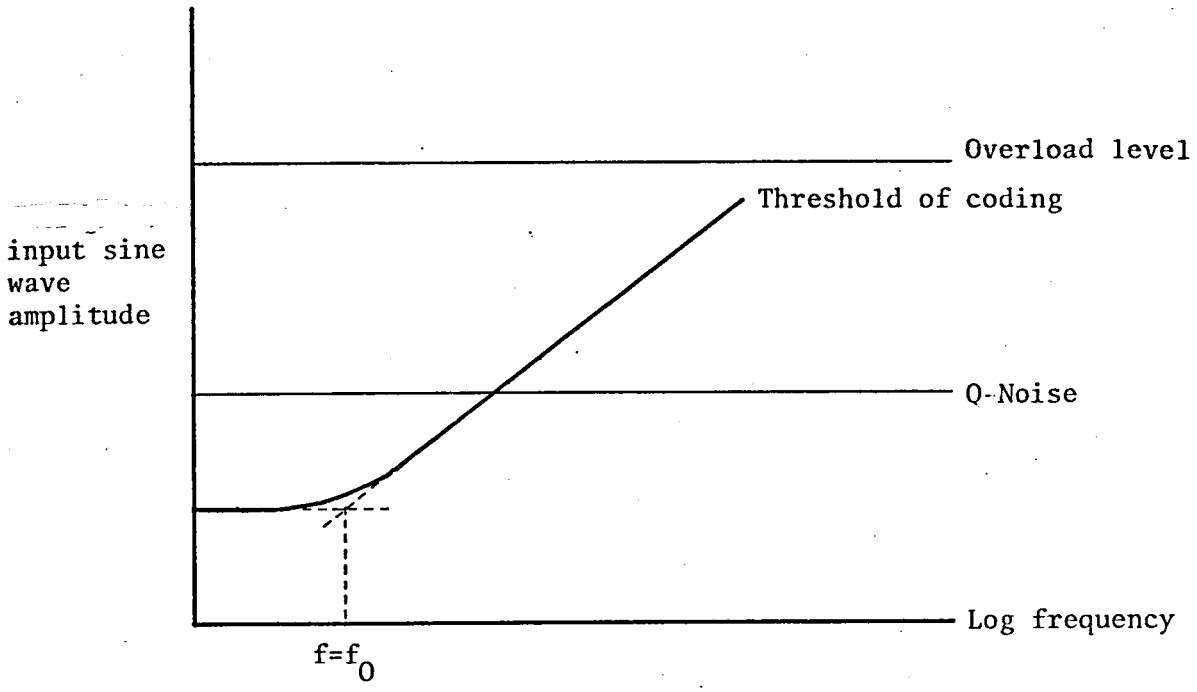


Figure 3.14: CHARACTERISTICS OF Δ-Σ MODULATION WITH SINGLE INTEGRATION

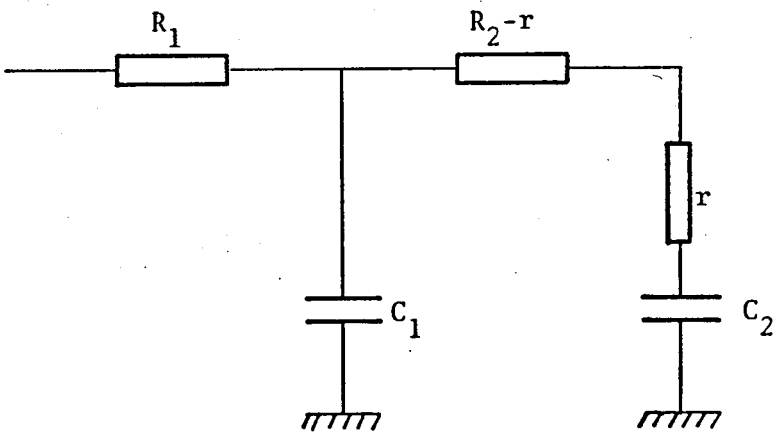


Figure 3.15: INTEGRATOR

CHAPTER 4

DIGITAL COMPUTER SIMULATION OF DELTA SIGMA MODULATION

There are various parameters upon which the operation and performance of a delta-sigma modulator depend. These include the amplitude and the rate-of-change of the input signal, the frequency of encoding (i.e. the clock rate), the method of integration and its characteristics, the level of the binary sequence at the output and the central step size. The design of a satisfactory modulator depends upon a careful choice of the circuit components and a thorough knowledge of how various parameters affect the operation, as well as on a full definition of the performance requirements.

Digital computer techniques are most suitable for an analysis concerned with the effect of changing one or more parameters on the characteristics under investigation. The techniques also yield to easy analysis, and by providing useful information on the different aspects of the system they make possible a complete and thorough understanding of the performance of the system.

This chapter is concerned with the digital computer simulation of delta-sigma modulation. A general description of the simulation technique is made and the important aspects of the program are illustrated with the aid of a flowchart. The complete program is included in Appendix 2. Results obtained from the simulation in the form of both numerical and graphical printouts are included and discussed.

4.1 BASIC FLOWCHART OF THE SIMULATION

Figure 4.1.a and.b show the flowchart of the computer simulation, which is broken down into blocks corresponding to both the physical system and the subroutines used.

The program starts with the reading of the first set of input data values, and the input to the modulator is then generated. Having generated the input sine wave forms, various parameters are given initial values. These include the first set of comparator, integrator and quantiser output values. Then, for each value of the input, the program computes a value

for the output, and stores this in the memory. Having finished all the input values, the program goes on to print the calculated values and plots these as graphs on the line printer for initial investigation purposes.

The second part of the program is concerned with the calculation of the Fourier components of the digitally-encoded output signal. Two sub-routines are used for this purpose, to provide a mutual check. Changes in the fundamental and the harmonic components as a function of the input sine wave amplitude and the clock frequency are printed by the line printer, and plotted by the offline plotter for detailed investigation. The program, having checked if any more data is present, ends. The details of the computer program is included in Appendix 2.

4.1.1 Input Wave form Generation

The input generated for the delta-sigma modulator is a sine wave, since it is this sort of waveform which is modulated and applied to the motor. Since it is necessary to change the amplitude of the input sine wave, and to investigate the effect produced in the output, it must be generated in such a way that its amplitude can be changed easily.

Assuming that the sine wave is simulated discretely by N points on each complete cycle, it may be defined by the following expression

$$X(I) = C \times SIN\left(PI \times \frac{M}{N/2}\right)$$

where

$PI = \pi$

$M = I-1$

C = is the amplitude of the input sine wave

and I changes from 1 to N+1.

With the above presentation of the sine wave amplitude, the required information is easily obtained by changing the value of C and repeating the process. The program computes values of X(I) for a series of time

intervals, and stores these in the memory for use as inputs to the delta-sigma modulator.

Since N determines the number of comparisons to be made by the comparator, the clock frequency is also determined by N. For different clock frequencies N should be changed. To generate 3-phase input sine waves the following expressions are used;

$$X(I) = C \times SIN\left(PI \times \frac{M}{N/2}\right)$$

$$Y(I) = C \times SIN\left(PI \times \frac{M}{N/2} + \frac{2 \times PI}{3}\right)$$

$$Z(I) = C \times SIN\left(PI \times \frac{M}{N/2} - \frac{2 \times PI}{3}\right)$$

Figure 4.2 shows the output of the delta-sigma modulator for different input wave shapes and Figure 4.3 shows the outputs for 3-phase input sine waves.

4.1.2 Delta-Sigma Modulation

The modulator consists of a comparator, an integrator, a quantiser and a bistable. Since the computer functions digitally, operation of the bistable (which functions as a sampler) is taken care of automatically and is inherent in the simulation.

The comparator performs the subtraction between the amplitude of the sine wave $X(I) = C \times SIN\left(PI \times \frac{M}{N/2}\right)$ and the output of the switch Z1(I-1). Since there can be no output before there is an input, the output lags the input by one clock pulse period. Taking this into account implies a subtraction following integration; thus A1(I) = X(I) - Z1(I-1) rather than X(I) - Z1(I).

The difference between the two signals is fed to the quantiser. This acts as a level detector, and decides which of the two possible levels the output Z1(I) should take. Thus, if the input B(I) is positive the output (R) is positive and if B(I) is negative then it is negative.

Having completed the computation for each of the N points, the program ends with the corresponding values of the outputs of the comparator, the integrator and the quantiser stored in the memory.

Figure 4.4 shows the outputs of the comparator, the integrator and the quantiser when no input signal is present i.e. the idling situation and Figure 4.5 shows the same outputs for a sine wave at the input.

4.1.3 Graph Plotting

The values obtained at various points of the program are plotted on the line printer for initial investigation purposes, by means of the subroutine PLOTM which can be used to draw a maximum number of ten graphs on the same set of axes.

The final results are presented as graphs, drawn by the offline plotter using the GRAF subroutines available in the NAG (Nottingham Algorithms Group) library at the University of Loughborough Computer Centre. The UTP subroutines used in the program include UTPOP - to open the plotter, UTPCL - to close the plotter, UTP4A - to draw and scale a set of axes and UTP4B - to join a set of points with either straight lines or curves.

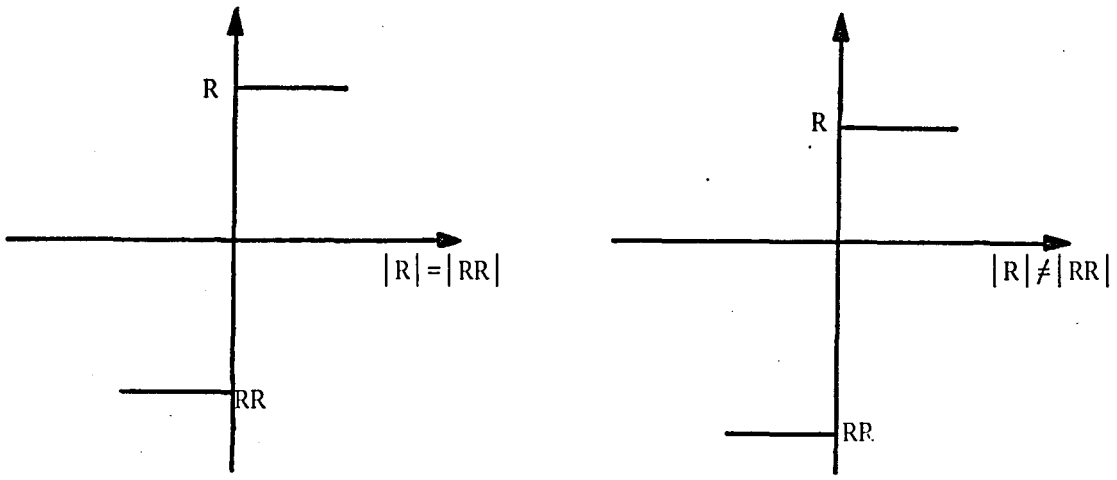
A special subroutine (Subroutine HISTOG) has been developed to scale input data for UTP4B, so that the output of the delta-sigma modulator can be drawn by the offline plotter in the form of an histogram.

4.1.4 Noise and Distortion

Random numbers with a Gaussian probability-density function are used as noise for the purpose of investigating the effects of noise on the output waveform and harmonics. Subroutine UTR1 of the USUB subgroup of the NAG library is employed for this purpose.

Distortion is added in the form of asymmetry introduced at the quantiser. The two levels of the quantiser are R and RR, and for distortion to be present the values of R and RR should be different and of opposite signs.

The change in the characteristics of the quantiser is explained below.



4.1.5 Fourier Analysis

The Fourier components of the digitally encoded output of the delta-sigma modulator are found by means of two subroutines, the first of which gives the amplitudes of the harmonic components relative to the fundamental. This subroutine (FOURY) gives an output of N1 harmonics, where $N1 \leq N/2$ and N is the number of ordinates, which must be even. The subroutine FOURY is included in Appendix 2.

The output of the second subroutine (NAG Library Subroutine CØGAAF) provides not only the relative harmonic components but also their absolute values, thereby making it possible to plot the absolute values as a function of the input signal level for different clock frequencies. The subroutine calculates the finite Fourier transform of $2^{M1/2}$ real data values, using the Cooley-Tukey algorithm, where M1 is an even integer not less than 4. Apart from this the inputs and outputs of the subroutine can be interchanged, which can be used as a check on the results.

4.2 RESULTS

The levels of the fundamental and the harmonic components of the digitally encoded signal were computed as a function of both the clock frequency and the input sine wave amplitude. Assuming an input sine wave frequency of 50Hz, the clock frequency f_1 is $2^7 \times 50 = 6.4$kHz. The clock

frequency was increased by a factor of 2 and the computation repeated at clock frequencies of 6.4kHz, 12.8kHz, 25.6kHz and 51.2kHz. A base of 2 is necessary in the subroutine CØ6AAF which is used to compute the harmonic components.

4.2.1 Effect of the Clock Frequency and the Input Sine Wave Amplitude C on the Harmonic Content

Figure 4.6 to Figure 4.19 show the first 40 harmonics as a percentage of the fundamental, for four different clock frequencies and for different values of the input sine wave amplitude C between 0.2 to 1.5V. The figures also show the input to the modulator and its output for the two different clock frequencies (i.e. sampling rate) f_1 and $f_1/2$. These figures establish how encoding is affected by the clock frequency, and show that at higher clock frequencies encoding is greatly improved. When C is low the harmonics are very large, especially at lower clock frequencies, and as the order of the harmonic increases so too does its relative magnitude. For instance, Figure 4.6 shows that all harmonics above the 19th are greater than of all the lower harmonics. This is due, at least in part, to the fact that since C is low it is difficult for the modulator to encode properly. A further reason is that, since the clock frequency is also low, the effect of the harmonics created by the sample action of the bistable plays an increasingly greater role on the overall harmonic content of the wave form as the order of the harmonics increases (the total harmonic spectrum consists of the fundamental and its odd-order components plus the clock frequency component and its components). This effect is clearly seen in Figure 4.6.

However, as the clock rate increases the level of the higher harmonics drop significantly, but that of the lower harmonics remain more or less the same (refer to Figure 4.6.c), indicating that as the clock frequency is increased not only do the harmonics generated by the sampling action of the

switch (bistable) drop but also since the input level C is low and the encoding is not satisfactory the lower harmonics remain substantially unchanged. This indicates that an increase of clock frequency when the input level is very low has very little effect on the operation of the modulator.

When C increases all the lower-order harmonics are considerably reduced, although the higher-order harmonics still remain of a considerable amplitude for lower clock frequencies. This is shown clearly by an investigation of harmonics higher than the 19th in Figures 4.9 to 4.14, for a clock frequency f_1. It is also clear that as the clock frequency increases the level of these harmonics drops considerably.

For the case of overmodulation, when C is greater than 1.0 (Figures 4.15 to 4.19), the level of the lower-order harmonics increases steadily, with the 3rd-harmonic being dominant. The output is almost a square wave and, unlike the higher-order harmonics, which still reduce as the clock rate increases, the third does not depend significantly on the clock frequency.

The results of Figures 4.6 to 4.19 and the above discussion lead to the conclusion that, for optimum encoding, the cases of overmodulation and undermodulation should be avoided.

Figures 4.20, 21, 22 and 23 show the change in the fundamental, 3rd, 5th and 7th harmonics as the input sine wave amplitude C is varied, for four different clock rates. Consideration of the fundamental shows that it passes through an initial nonlinear region before entering a linear region. This is as expected, since, when the threshold of coding has been reached, the encoding characteristics are not correctly achieved. The point at which the fundamental intersects the y-axis is -22.49dB for C = 0.1 and -0.7dB for C = 1.05.

It will also be noted from Figure 4.20 that the harmonics tend to increase towards both ends of the x-axis scale. This is again as expected, since at one end the threshold level is approached and at the other end the

modulator is becoming overloaded. The three harmonics shown follow more or less the same pattern, being 13dB less than the fundamental at the lower end of the x-axis and about 35dB less at the upper end. Between the two ends the level of the harmonics is even lower, and in this region where encoding is satisfactory all the harmonics are at least 35dB down on the fundamental.

At lower clock frequencies, the fundamental remains the same, but the level of the harmonics increases steadily. Furthermore, a comparison between Figures 4.20, 21, 22 and 23 shows that as the clock rate reduces the effect of the higher order harmonics increases. This is clearly evident in Figure 4.23, where the level of the 5th and 7th harmonics exceeds that of the 3rd. Comparison of Figure 4.20 and Figure 4.23 reveals that the level of harmonics is increased roughly by a factor of 10dB by reducing the clock frequency by a factor of eighth.

4.2.2 Effect of Noise

In Figure 4.24, the sine wave input with added noise and the corresponding output of the modulator are plotted for three different input amplitudes C, corresponding to undermodulation, normal modulation and overmodulation.

Figures 4.25, 26, 27 and 28 show the fundamental, 3rd, 5th and 7th output harmonic components as a function of the amplitude C at four different clock frequencies. Comparison with Figures 4.20, 21, 22 and 23 shows clearly that the fundamental is the same and that the harmonics follow the same pattern as in the absence of noise. However, as the clock frequency is reduced the effect of harmonics increase rapidly, and at a clock rate of $3f_1$, the level of the 5th and 7th harmonics exceeds that of the 3rd harmonic. A comparison of the levels of the harmonics with and without noise reveals that they are higher for the former, with the difference being about 10dB.

Increasing further the level of noise will thus result in a further increase in the level of harmonics.

4.2.3 Effect of Distortion

Distortion is introduced into the modulator by a change in the characteristics at the quantiser. Normally the level here is either ±1V, depending on the input, and changing these levels to +0.7V and -1.3V will cause asymmetry on the characteristics of the quantiser. This is illustrated in Figure 4.29, where the delta-sigma modulated outputs are plotted for three different values of the input sine wave, which is itself contaminated by noise. The response of the delta-sigma modulator is clearly affected by the asymmetry introduced between the positive and negative cycles of output, and both even and odd order components are now present.

Figures 4.30, 31, 32 and 33 show the variation of fundamental and the first three order harmonics with C, and comparison of these with Figures 4.25, 26, 27 and 28 reveals that they are higher than when only noise is present. Furthermore, investigation of the computer printout reveals that there is now present a d.c. component, which is about equal in amplitude to the fundamental.

The result of this section indicates that an improper adjustment or design of a delta-sigma modulator may lead to the presence of additional and unwanted distortion at the output, and this must clearly be avoided in any system which is constructed for a speed control application.

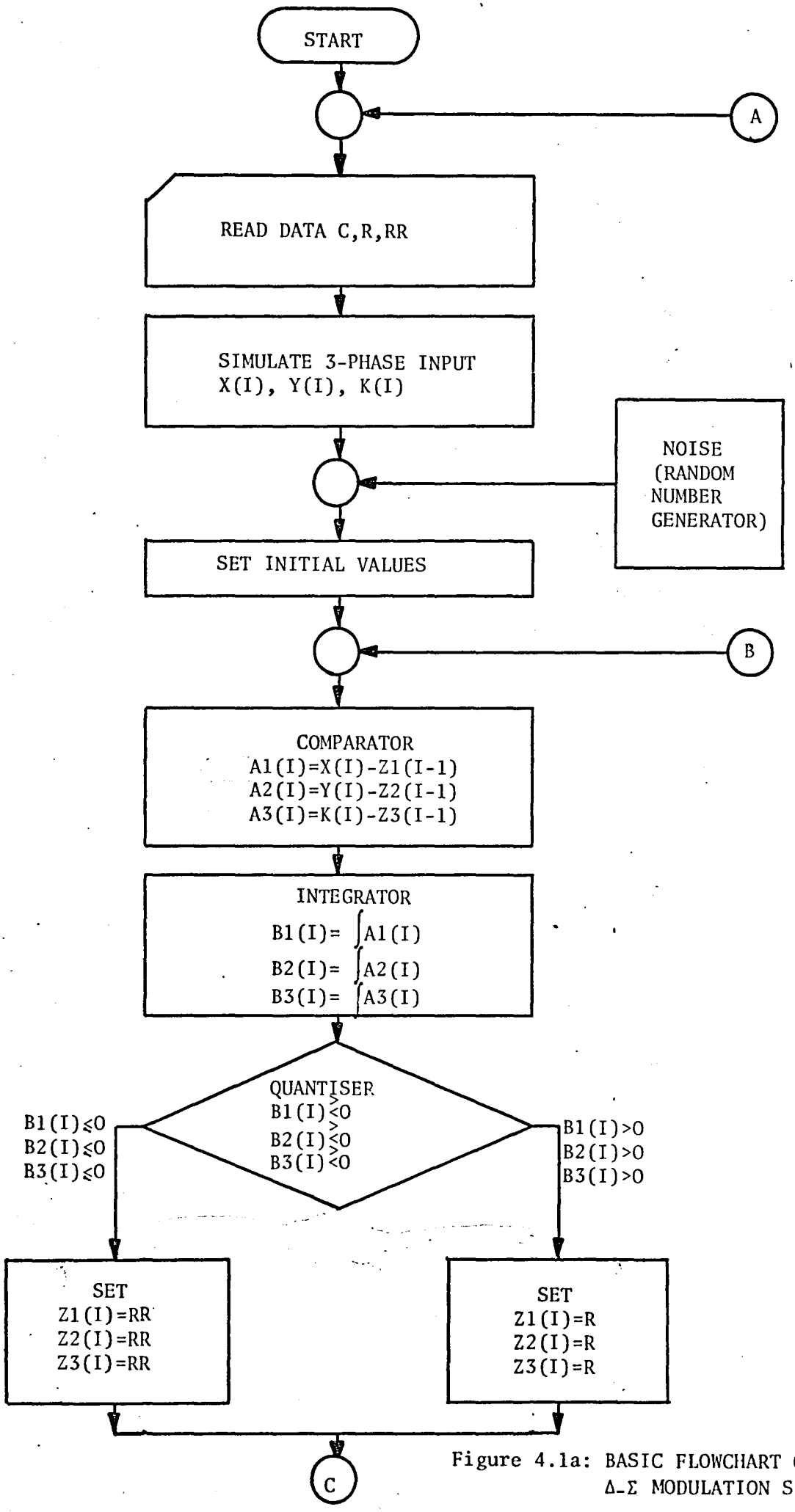


Figure 4.1a: BASIC FLOWCHART OF THE Δ-Σ MODULATION SIMULATION

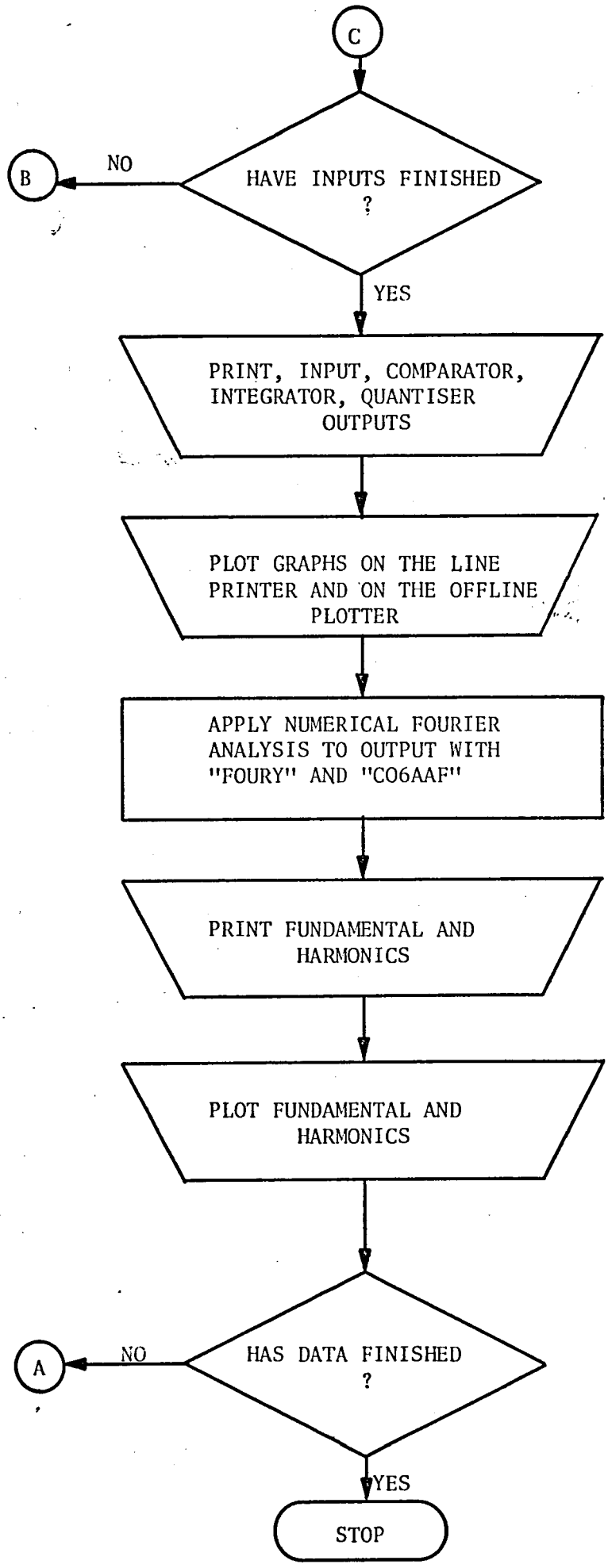

C
HAVE INPUTS FINISHED ?
NO
B
YES
PRINT, INPUT, COMPARATOR, INTEGRATOR, QUANTISER OUTPUTS
PLOT GRAPHS ON THE LINE PRINTER AND ON THE OFFLINE PLOTTER
APPLY NUMERICAL FOURIER ANALYSIS TO OUTPUT WITH "FOURY" AND "C06AAF"
PRINT FUNDAMENTAL AND HARMONICS
PLOT FUNDAMENTAL AND HARMONICS
HAS DATA FINISHED ?
NO
A
YES
STOP

Figure 4.1b

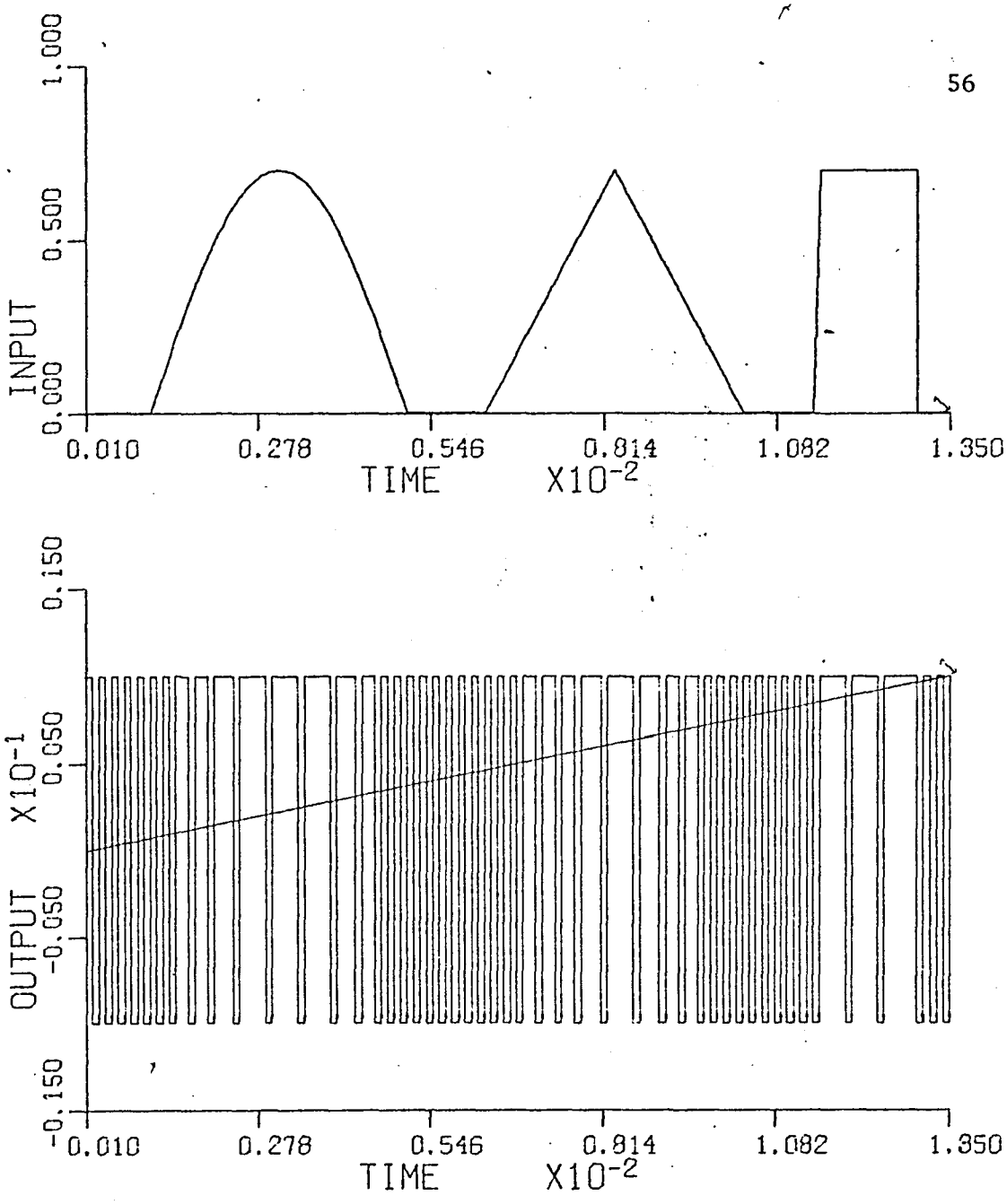
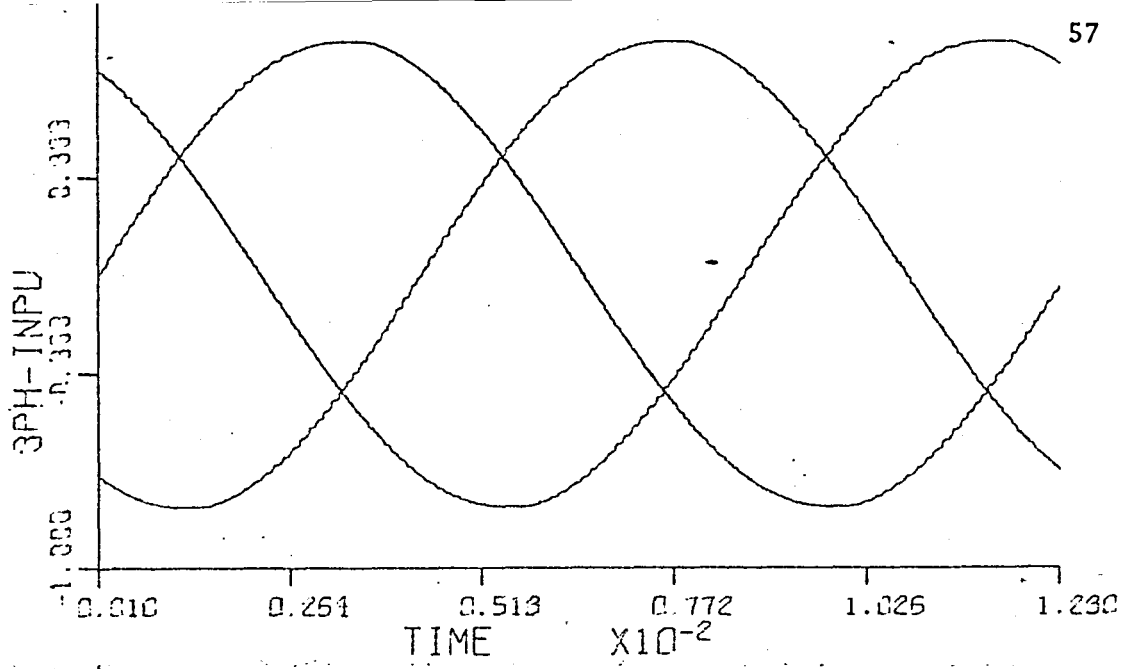
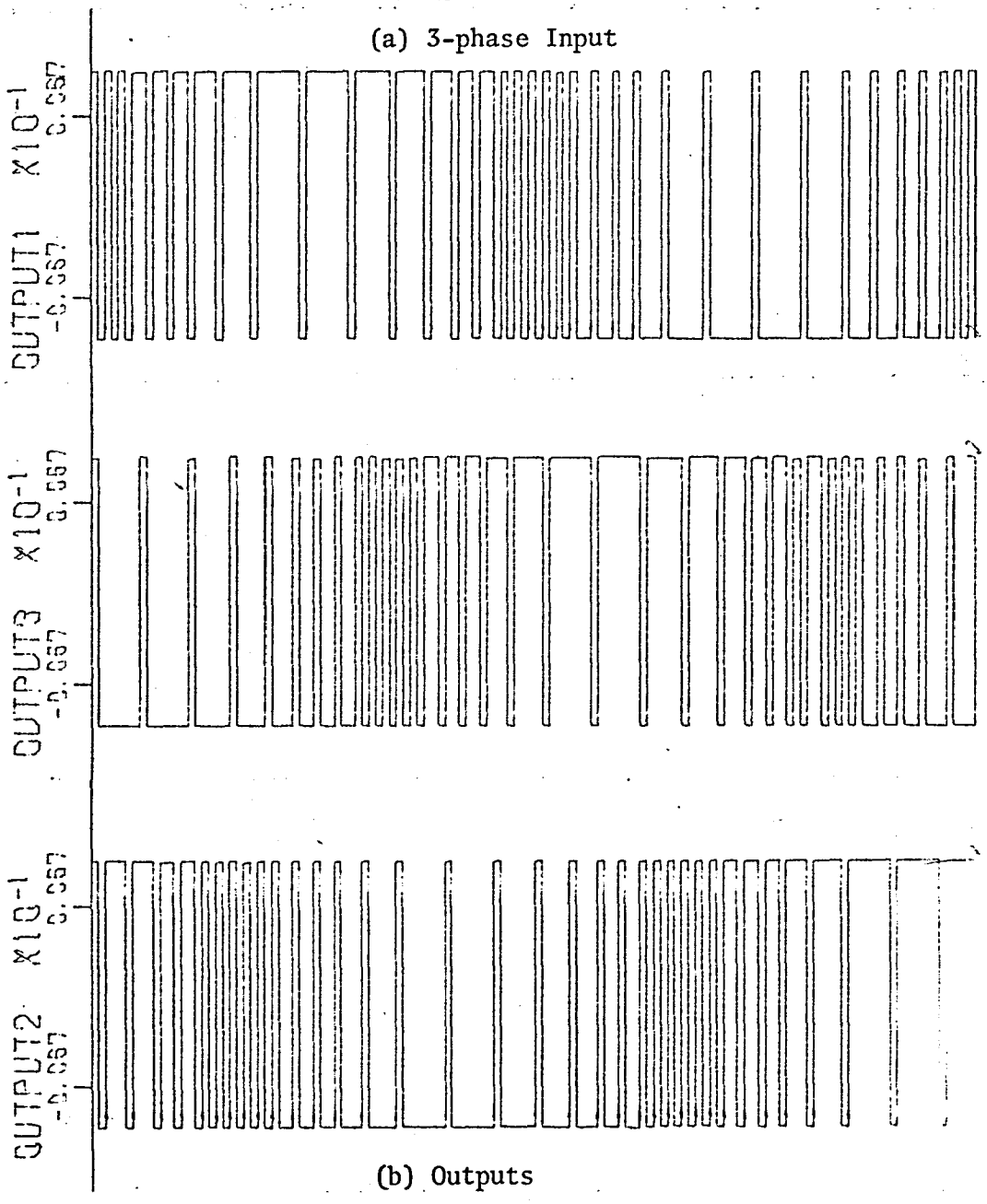


Figure 4.2: OUTPUT OF THE Δ-Σ MODULATOR FOR DIFFERENT INPUTS



(a) 3-phase Input



(b) Outputs

Figure 4.3: Δ-Σ MODULATION FOR 3-PHASE INPUT

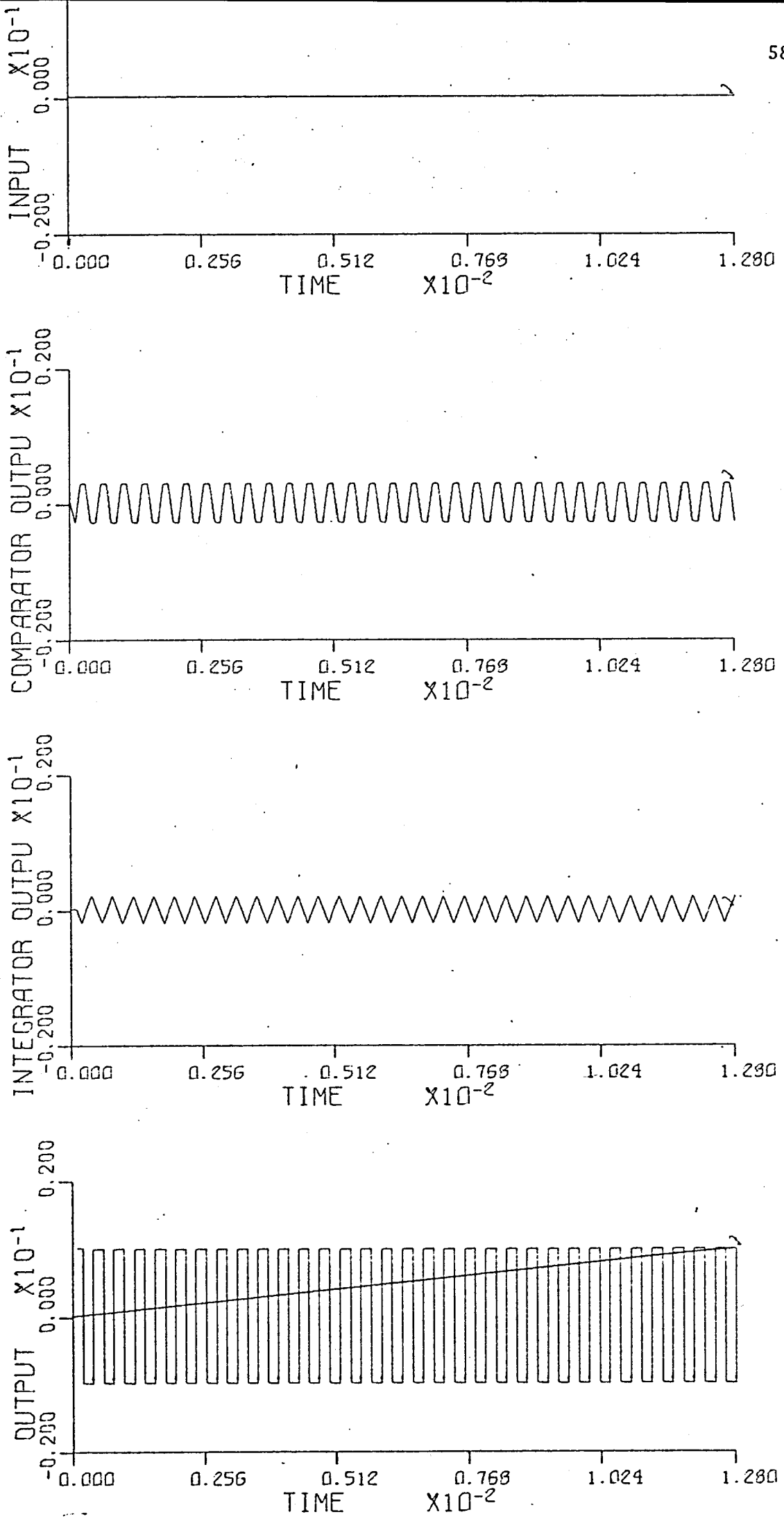
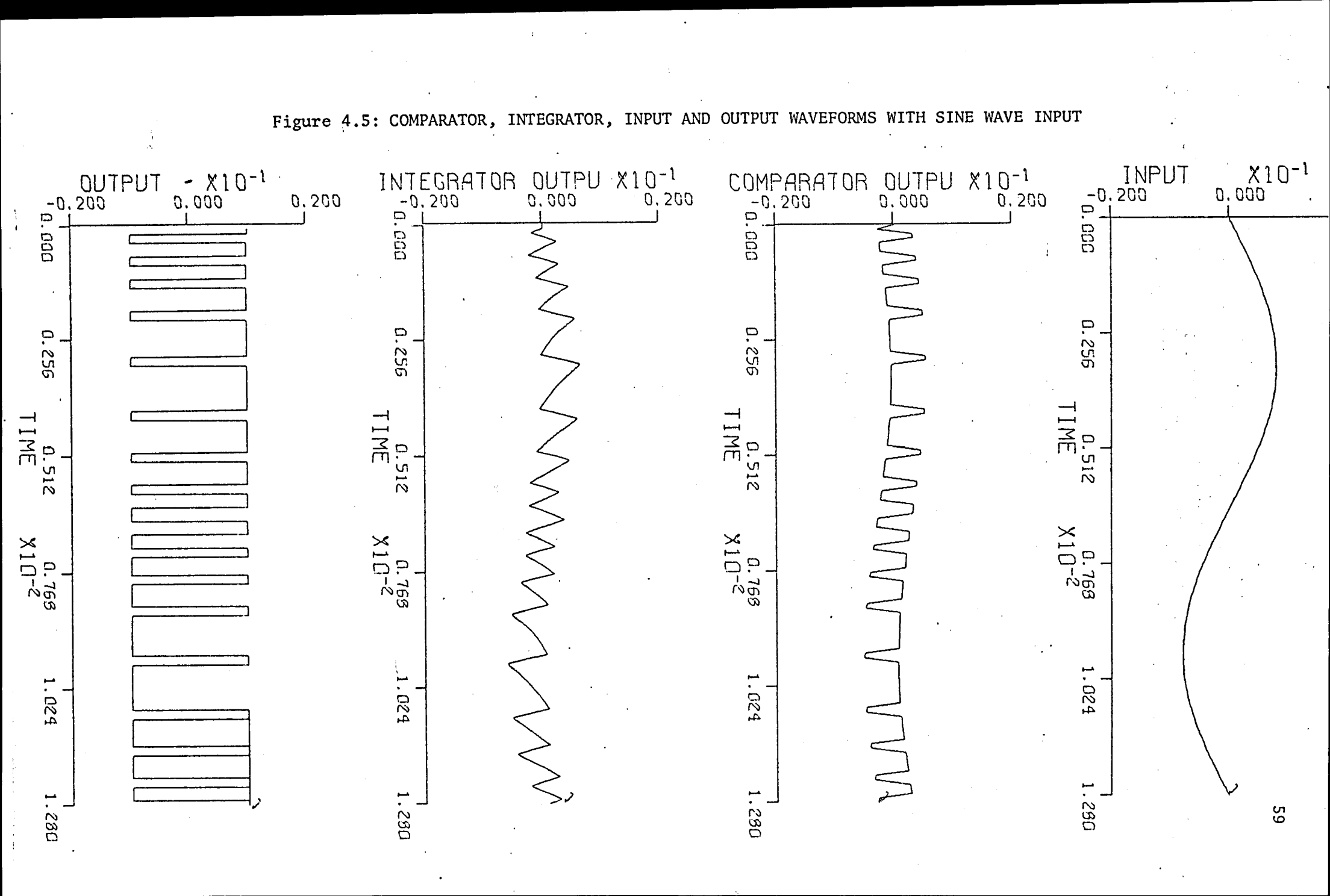


Figure 4.4: COMPARATOR, INTEGRATOR, INPUT AND OUTPUT WAVEFORMS (input = 0)

Figure 4.5: COMPARATOR, INTEGRATOR, INPUT AND OUTPUT WAVEFORMS WITH SINE WAVE INPUT



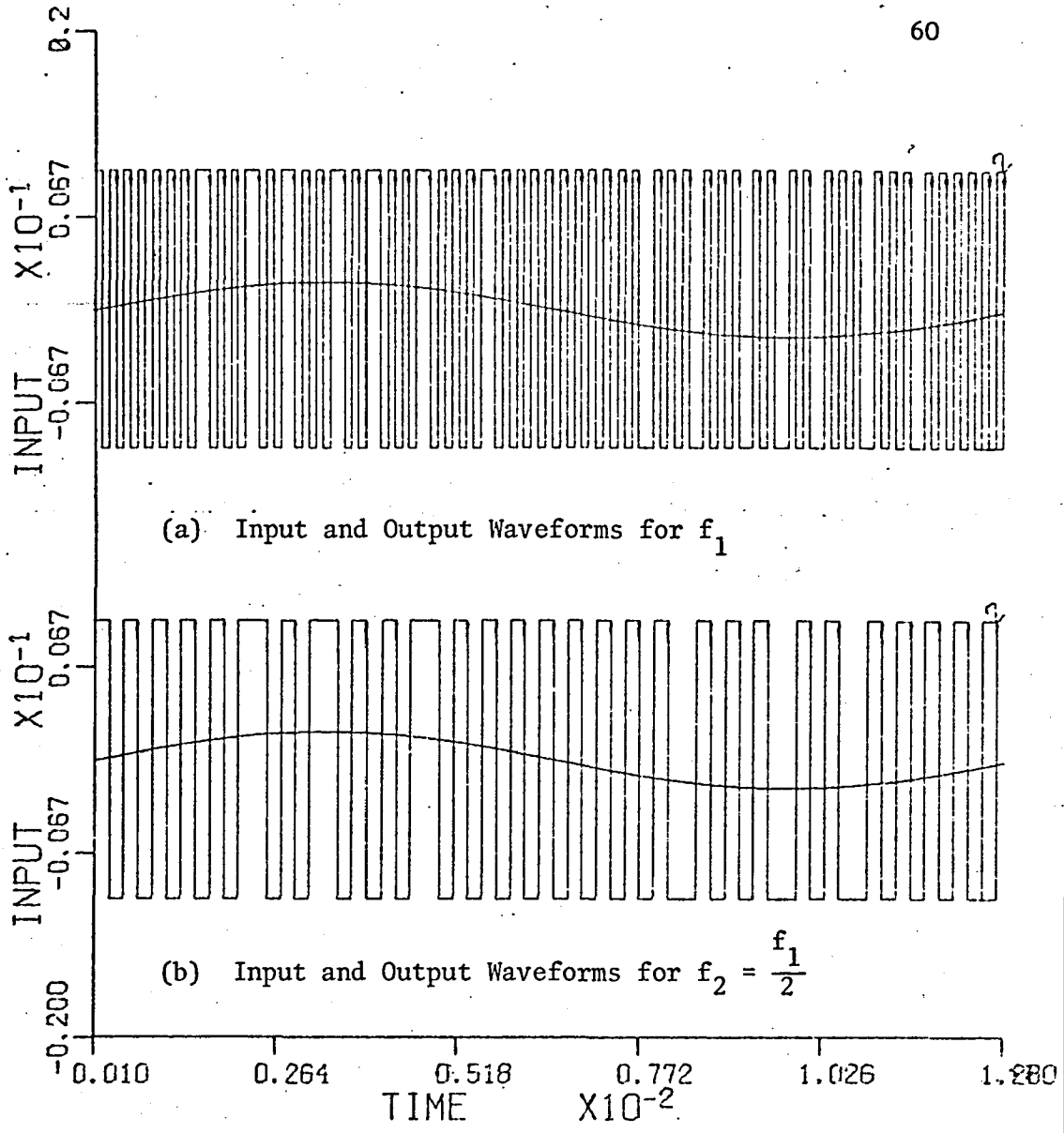


Figure 4.6: INPUT AND OUTPUT WAVEFORMS AND THE HARMONIC COMPONENTS EXPRESSED AS PERCENTAGES

HARMONIC ANALYSIS
C=0.20

NO	PERCENTAGE fclock = $8f_1$	PERCENTAGE fclock = $4f_1$	PERCENTAGE fclock = $2f_1$	PERCENTAGE fclock = f_1
1	100.0000	100.0000	100.0000	100.0000
3	5.7891	3.9399	3.6897	5.4726
5	4.5966	3.8335	3.1270	12.5796
7	5.6179	5.1711	8.5812	22.6957
9	4.3778	4.0036	7.5748	17.4814
11	2.3731	2.9661	8.1488	19.3983
13	2.0162	3.5983	3.0991	13.6207
15	0.9534	1.9292	8.0555	17.8983
17	2.4654	2.8751	15.9863	30.5761
19	2.1627	0.5498	12.1670	41.1958
21	0.6676	5.2305	7.0057	60.6157
23	2.0435	3.9519	18.2769	57.5328
25	0.8344	7.1869	23.2074	7.6424
27	0.9141	10.4147	2.8349	43.8343
29	1.8584	2.9150	40.4240	9.9492
31	3.0446	11.7668	17.8401	28.8042
33	1.8473	3.0134	34.5712	48.8084
35	0.7641	7.6507	26.1316	14.8434
37	0.4582	4.9019	47.1257	59.4976
39	2.0351	16.6130	36.8677	6.6650
41	5.2588	3.7848	30.6050	31.6859

(c)

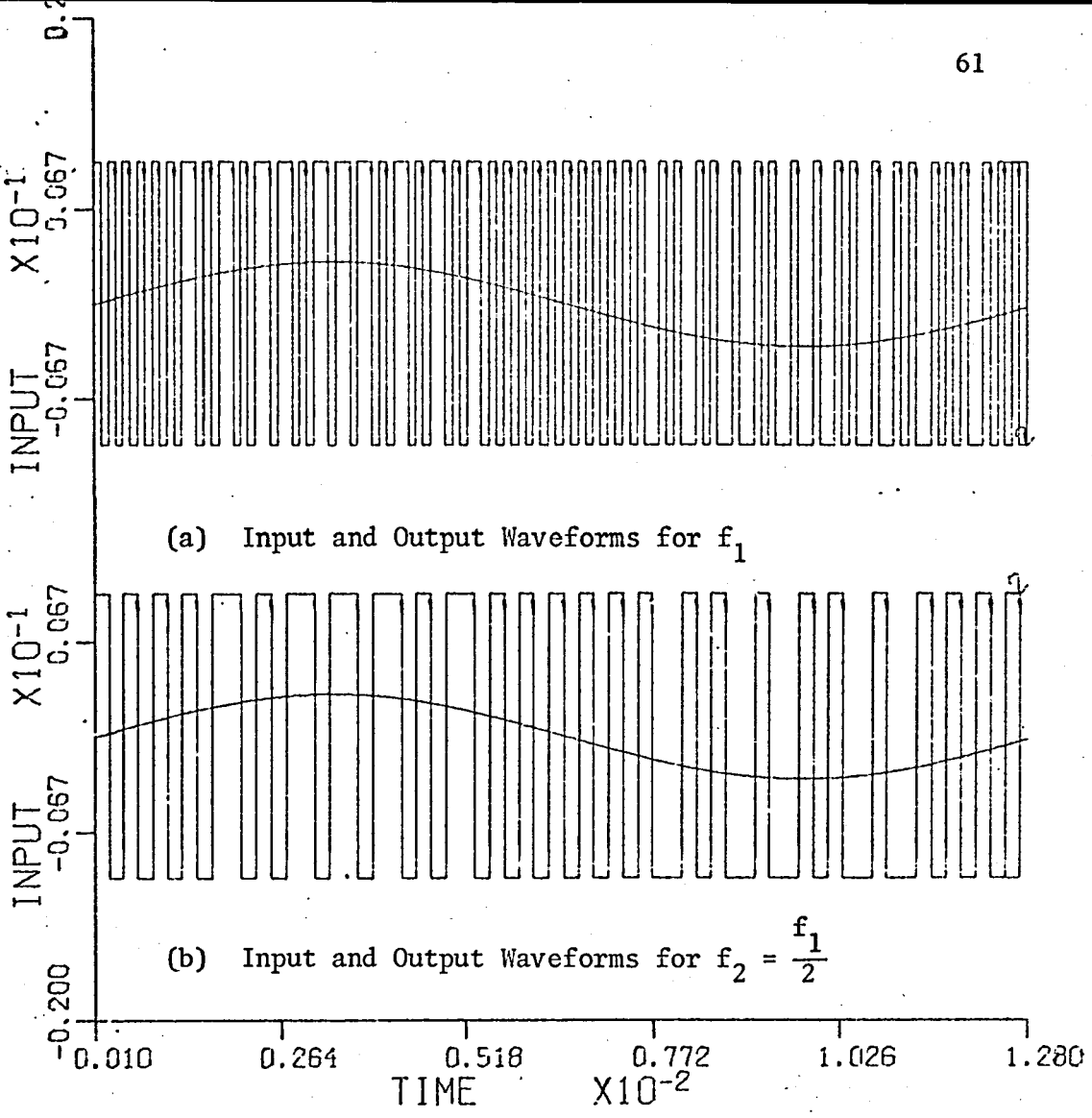


Figure 4.7: INPUT AND OUTPUT WAVEFORMS AND THE HARMONIC COMPONENTS EXPRESSED AS PERCENTAGES

HARMONIC ANALYSIS
C=0,30

NO	PERCENTAGE fclock = $8f_1$	PERCENTAGE fclock = $4f_1$	PERCENTAGE fclock = $2f_1$	PERCENTAGE fclock = f_1
1	100.0000	100.0000	100.0000	100.0000
3	2.2169	2.3200	4.1558	4.9103
5	1.6696	1.4110	4.3291	5.6548
7	2.5157	2.6752	6.6940	11.3808
9	2.2530	3.3400	8.6654	2.1927
11	1.4280	2.9882	4.9521	15.9350
13	1.5243	2.7638	4.0391	20.7478
15	2.3646	2.7832	2.8491	11.3857
17	1.3685	1.0357	4.0773	16.7169
19	0.1649	2.0971	10.3954	13.2099
21	1.4252	3.0400	6.2339	39.5028
23	0.9000	1.1296	6.5559	24.4296
25	1.0814	4.6594	14.9683	30.8983
27	1.1768	5.1557	25.7051	32.7507
29	0.5471	5.0190	13.4419	38.1371
31	0.8733	1.2832	13.9258	27.0761
33	1.9307	1.7809	17.3840	45.0608
35	1.7839	4.6936	20.2835	56.7056
37	0.4432	6.1900	16.8390	11.7494
39	1.0554	6.6472	34.9934	28.2420
41	0.5559	7.9080	26.8228	35.5210

(c)

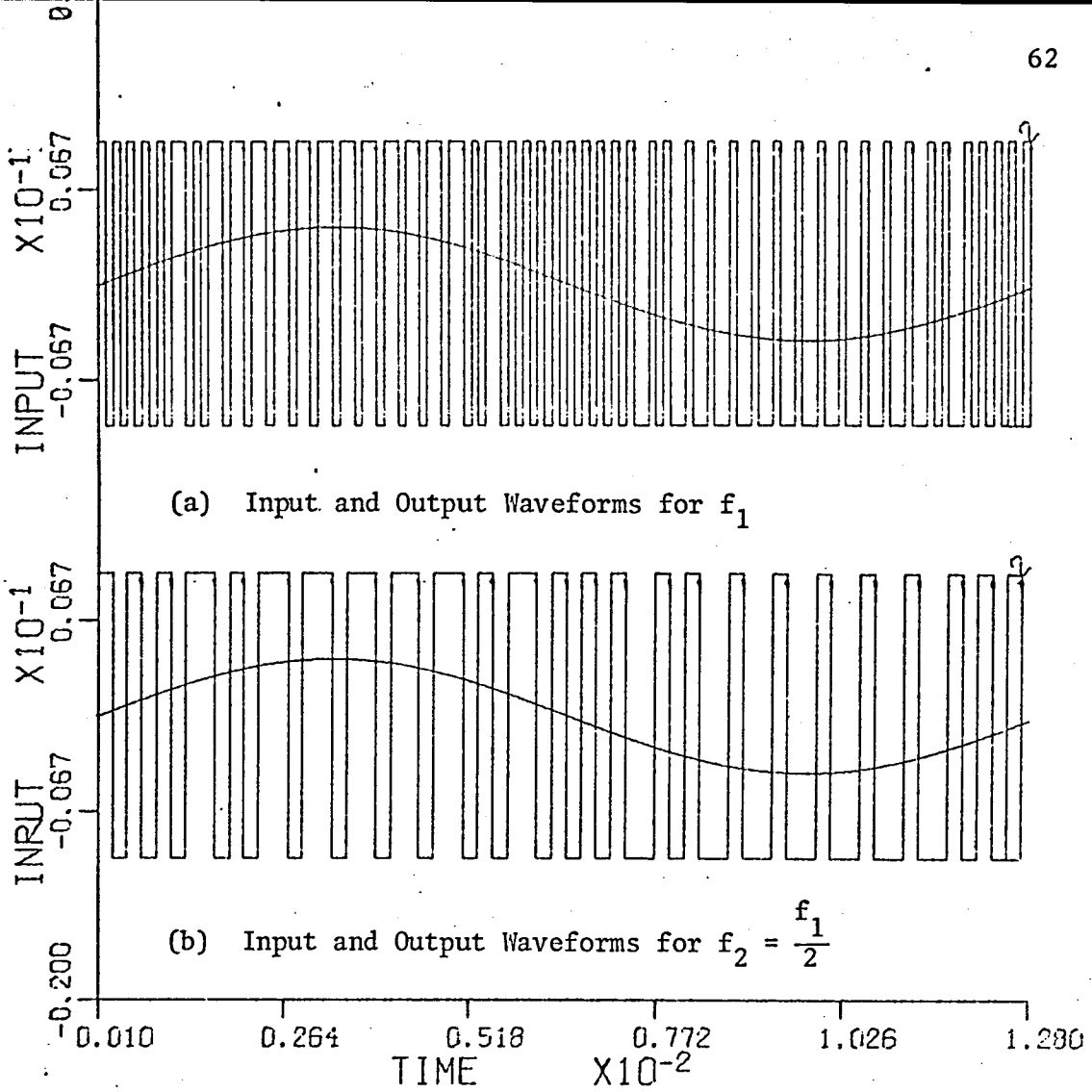


Figure 4.8: INPUT AND OUTPUT WAVEFORMS AND THE HARMONIC COMPONENTS EXPRESSED AS PERCENTAGES

HARMONIC ANALYSIS
C=0,40

NO	PERCENTAGE fclock = $8f_1$	PERCENTAGE fclock = $4f_1$	PERCENTAGE fclock = $2f_1$	PERCENTAGE fclock = f_1
1	100.0000	100.0000	100.0000	100.0000
3	1.5843	2.1099	3.1034	4.6398
5	4.4217	3.4495	3.5336	14.9940
7	1.0941	1.2584	1.5532	8.0706
9	1.9993	2.3268	1.4551	5.9954
11	3.0360	2.3587	1.9969	8.7620
13	1.0289	0.6037	2.1803	5.5449
15	1.2733	1.9883	5.1267	10.3550
17	1.7617	3.0303	5.8327	15.2839
19	0.6873	1.5893	3.9535	3.9100
21	0.5632	1.8163	6.0187	22.1438
23	1.3874	3.0296	8.0927	22.7192
25	0.6203	2.8211	6.7028	4.1150
27	1.6017	3.1997	14.6198	23.6615
29	0.4391	2.3266	10.5719	14.3954
31	0.5564	0.8451	3.8704	16.8224
33	1.4254	1.9055	3.8727	30.3700
35	1.2619	1.0942	8.6873	8.7081
37	1.7917	1.0129	12.8860	21.1013
39	2.5233	4.1134	19.5789	10.0858
41	1.3471	2.2106	4.6214	61.2842

(c)

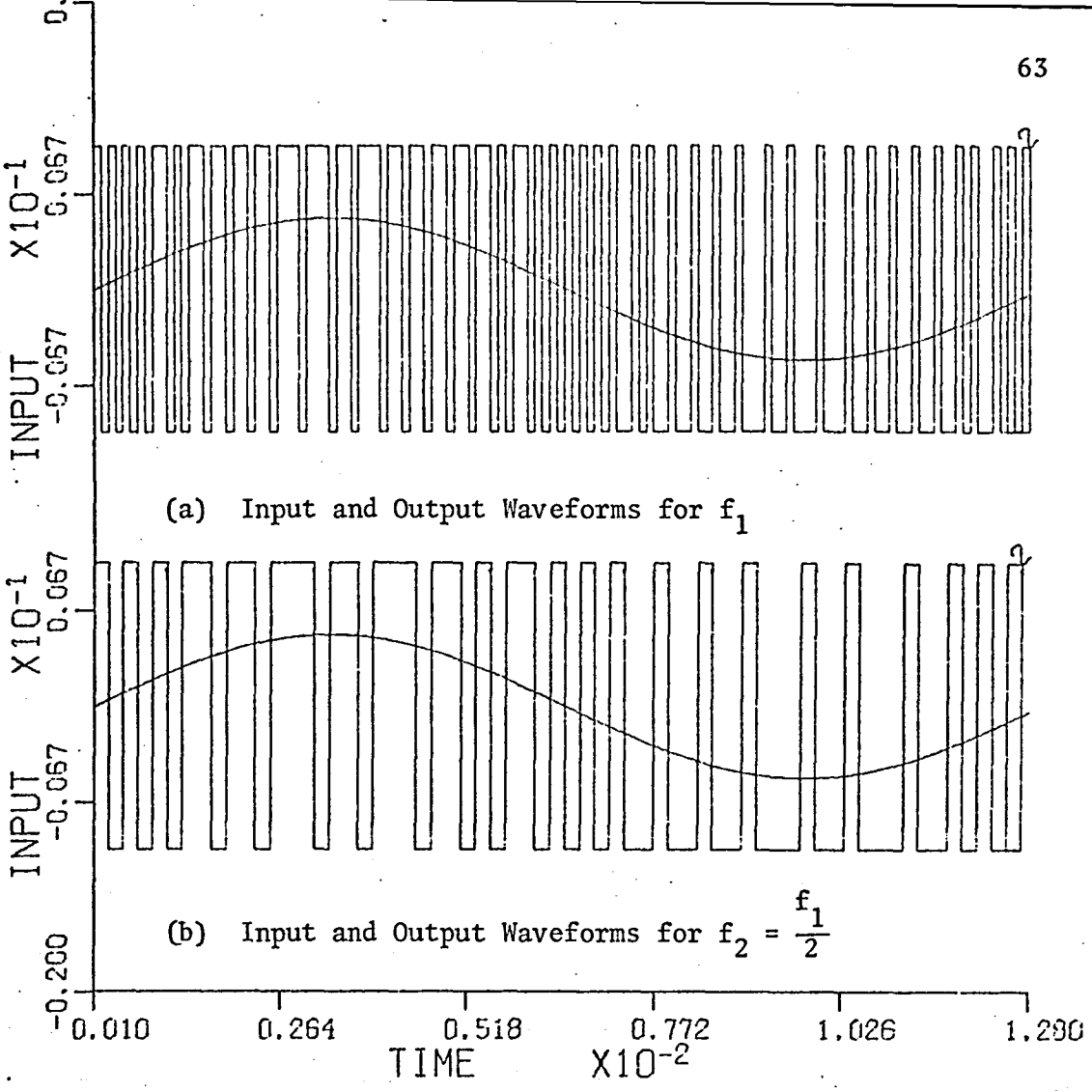


Figure 4.9: INPUT AND OUTPUT WAVEFORMS AND THE HARMONIC COMPONENTS EXPRESSED AS PERCENTAGES

HARMONIC ANALYSIS
C=0.50

NO	PERCENTAGE fclock = $8f_1$	PERCENTAGE fclock = $4f_1$	PERCENTAGE fclock = $2f_1$	PERCENTAGE fclock = f_1
1	100.0000	100.0000	100.0000	100.0000
3	0.2325	0.9726	1.3582	1.1876
5	0.2309	0.1260	2.1290	5.7357
7	1.2230	0.7564	1.4663	7.3581
9	0.4550	0.9750	2.6628	5.2218
11	0.3310	0.3243	1.5117	6.3409
13	0.6666	0.3301	2.4245	13.6429
15	1.4028	1.4943	4.9084	14.1068
17	1.0160	0.9611	1.0139	10.6080
19	0.1854	0.9939	3.7194	7.7157
21	0.5994	2.4073	6.7667	18.7405
23	0.7766	2.3466	8.1110	23.4178
25	0.7884	1.2639	6.9612	13.5393
27	0.3777	1.3336	3.7353	14.1684
29	0.5091	4.5358	5.6261	25.5592
31	2.3766	2.8533	6.0359	26.0352
33	0.7531	2.6647	6.0273	19.5746
35	0.5044	3.9209	6.9220	15.1815
37	1.0339	1.8656	6.1215	52.9369
39	1.9337	1.6283	18.9706	38.7425
41	1.7277	1.0852	15.4420	17.2226

(c)

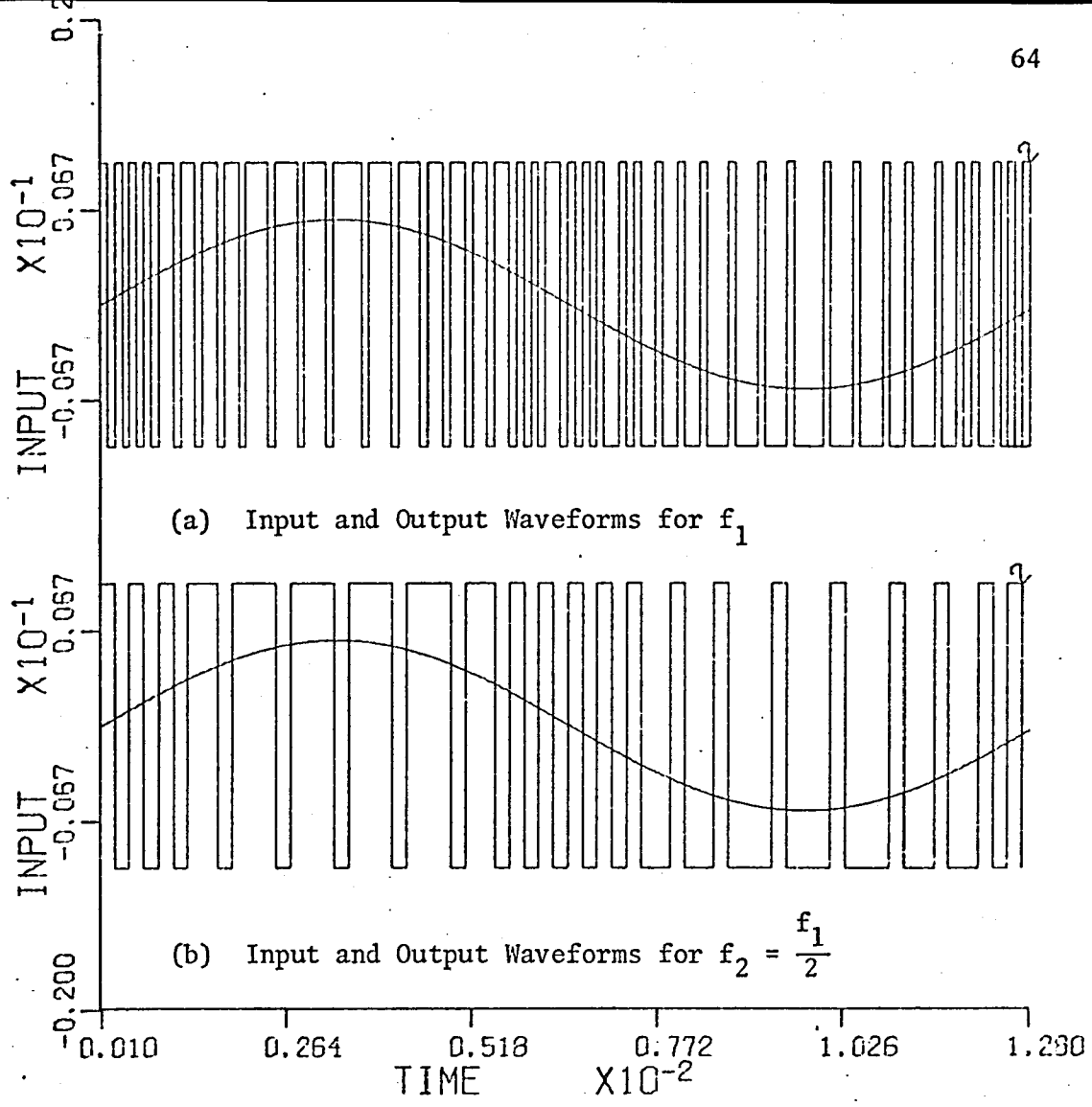


Figure 4.10: INPUT AND OUTPUT WAVEFORMS AND THE HARMONIC COMPONENTS EXPRESSED AS PERCENTAGES

HARMONIC ANALYSIS
C=0.60

NO	PERCENTAGE fclock = $8f_1$	PERCENTAGE fclock = $4f_1$	PERCENTAGE fclock = $2f_1$	PERCENTAGE fclock = f_1
1	100.0000	100.0000	100.0000	100.0000
3	0.7382	0.8324	0.6657	2.2025
5	0.9215	0.8762	0.5643	1.0015
7	0.6150	0.2734	0.8245	3.8209
9	0.8843	1.1156	1.4319	4.4714
11	1.4867	2.6124	2.6962	5.1814
13	0.3928	1.4728	0.8538	6.3880
15	1.0327	1.9763	1.1947	5.3393
17	1.5100	1.8768	3.7310	7.7532
19	0.9689	0.7723	0.5753	10.1937
21	1.5810	3.4012	5.8251	4.0783
23	0.5863	0.5018	0.9503	11.0994
25	0.3139	1.9496	5.9117	6.6488
27	1.1830	0.7492	6.5369	34.1556
29	0.4553	1.7362	6.5258	33.5990
31	0.4388	1.2754	5.2836	39.9572
33	0.5460	2.6833	1.6619	42.0794
35	0.3088	2.5478	6.5961	2.1411
37	1.2899	3.4795	9.7068	47.2014
39	1.1184	2.6623	9.7734	43.1675
41	0.9178	5.3200	6.8356	40.3835

(c)

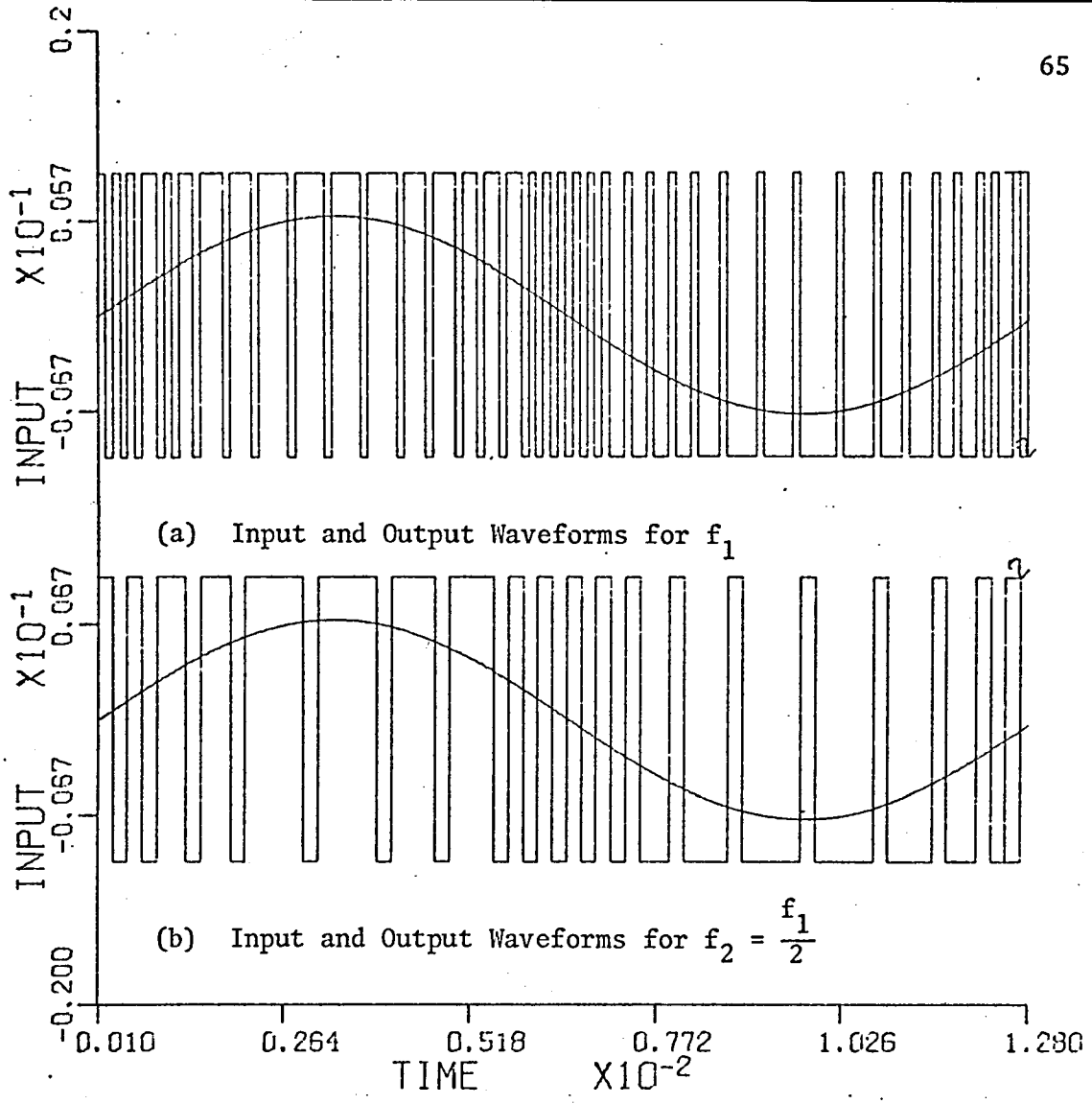


Figure 4.11: INPUT AND OUTPUT WAVEFORMS AND THE HARMONIC COMPONENTS EXPRESSED AS PERCENTAGES

HARMONIC ANALYSIS
C=0,70

NO	PERCENTAGE fclock = $8f_1$	PERCENTAGE fclock = $4f_1$	PERCENTAGE fclock = $2f_1$	PERCENTAGE fclock = f_1
1	100.0000	100.0000	100.0000	100.0000
3	0.1706	0.9540	1.0184	0.3817
5	0.4635	0.7443	0.8513	0.2652
7	0.4476	1.0609	1.3528	0.6184
9	0.2049	1.4754	2.0390	2.8782
11	0.5619	1.3187	3.9770	1.8634
13	0.2764	1.2915	3.6670	3.2075
15	0.8500	1.4876	3.9099	5.7399
17	0.5243	0.7430	3.5016	3.1895
19	0.5832	1.0177	1.4770	12.3602
21	0.9297	1.9566	3.2499	9.5006
23	0.3856	1.1694	3.8018	26.8018
25	1.0051	0.7721	2.4426	38.8157
27	0.3784	1.2699	1.3055	47.2064
29	0.5808	0.9793	4.2974	27.8497
31	0.6187	0.7143	1.2193	33.4135
33	0.6990	1.3531	7.7735	25.7696
35	1.5774	2.3406	4.0108	16.9733
37	0.4154	1.7725	2.6747	26.6485
39	0.6291	2.8082	8.8543	13.4317
41	0.8471	1.5687	5.9496	43.2451

(c)

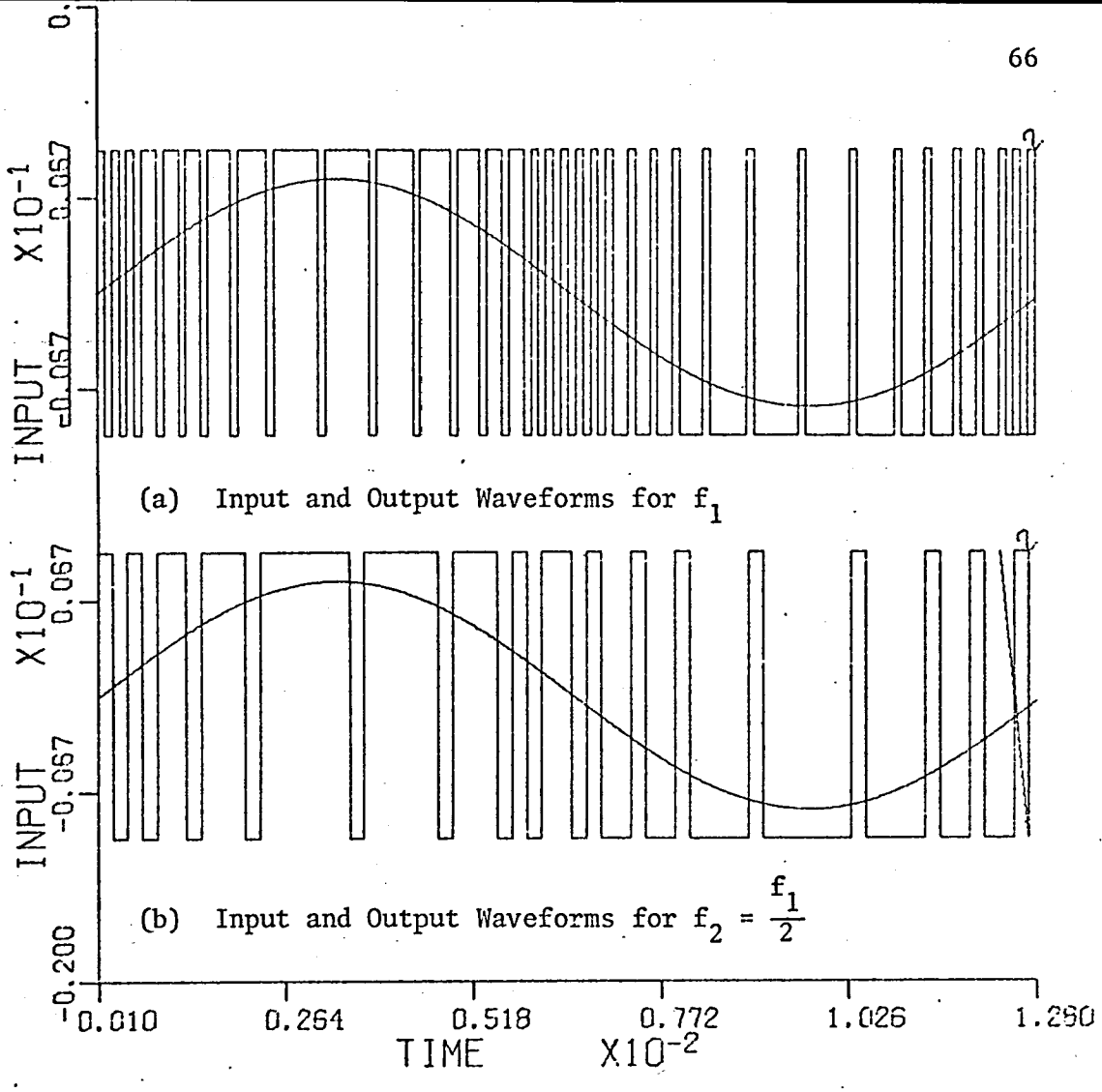


Figure 4.12: INPUT AND OUTPUT WAVEFORMS AND THE HARMONIC COMPONENTS EXPRESSED AS PERCENTAGES

HARMONIC ANALYSIS
C=0.80

NO	PERCENTAGE fclock = $8f_1$	PERCENTAGE fclock = $4f_1$	PERCENTAGE fclock = $2f_1$	PERCENTAGE fclock = f_1
1	100.0000	100.0000	100.0000	100.0000
3	0.4936	0.5111	1.0873	3.4906
5	0.3487	0.6735	1.3965	5.1827
7	0.2122	0.7823	1.1414	2.2496
9	0.4736	0.4677	2.4846	4.8232
11	0.1127	0.1611	2.5172	5.5505
13	0.2947	0.7731	1.9047	7.2933
15	0.6485	0.5513	1.0173	9.5085
17	0.7639	0.5947	1.8047	16.1865
19	0.1975	0.6118	1.1699	26.5435
21	0.2422	0.7679	1.6160	27.1769
23	1.1162	1.1097	1.1013	18.8468
25	1.3479	1.0724	1.6926	23.5376
27	1.1009	1.7837	1.7938	23.7638
29	0.3167	1.2715	3.4714	11.3541
31	0.3390	1.4558	4.7091	28.5608
33	0.3140	1.3629	1.0154	5.7078
35	0.0845	1.4073	7.7622	42.4734
37	0.4729	1.4565	4.3425	29.7169
39	0.9973	2.7970	8.8872	34.9511
41	1.3034	1.4776	6.4390	51.3003

(c)

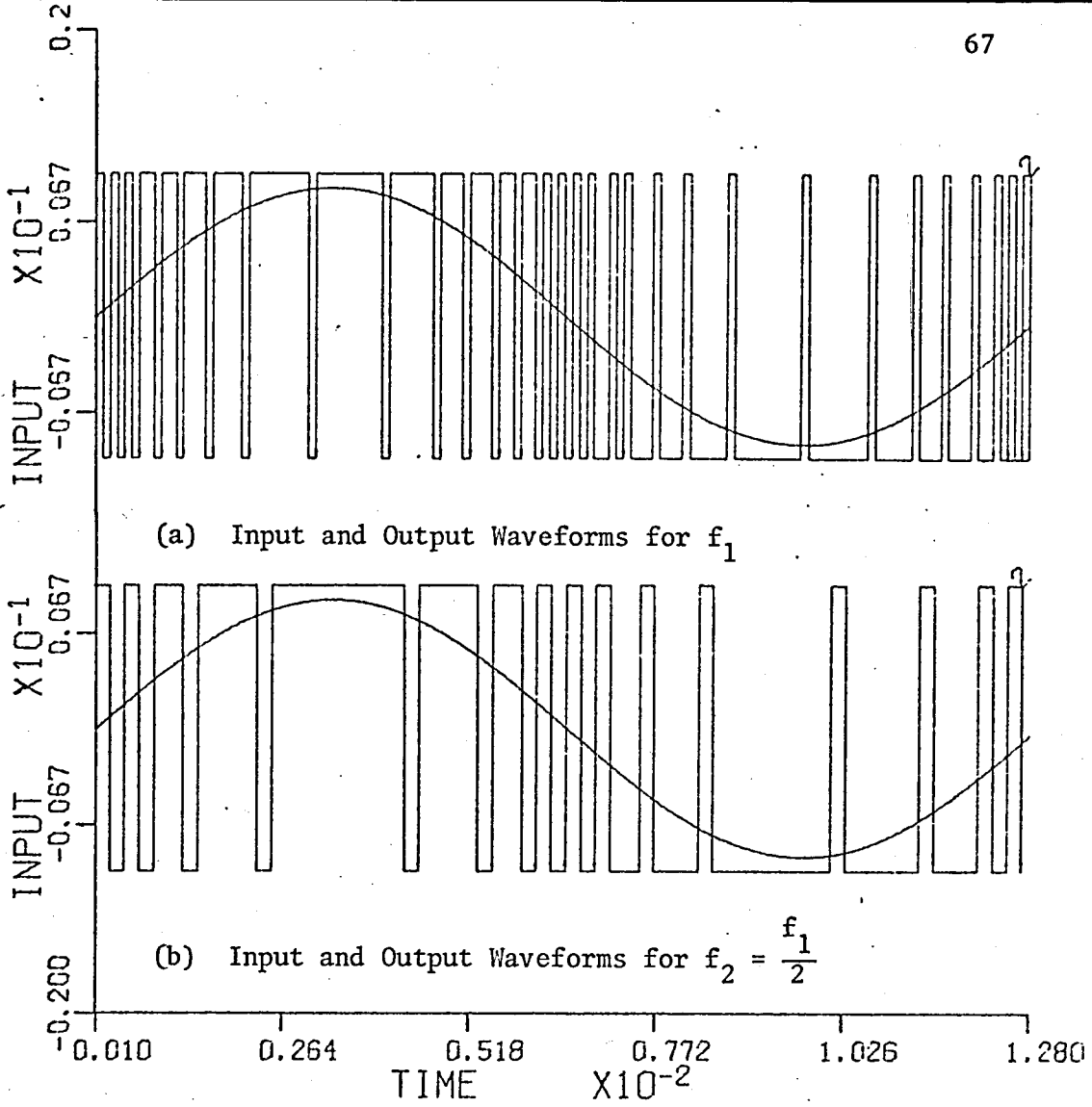


Figure 4.13: INPUT AND OUTPUT WAVEFORMS AND THE HARMONIC COMPONENTS EXPRESSED AS PERCENTAGES

HARMONIC ANALYSIS
C=0.90

NO	PERCENTAGE fclock = $8f_1$	PERCENTAGE fclock = $4f_1$	PERCENTAGE fclock = $2f_1$	PERCENTAGE fclock = f_1
1	100.0000	100.0000	100.0000	100.0000
3	0.9247	0.8809	0.6253	1.0326
5	0.1592	0.6218	0.9006	3.2272
7	0.2065	0.6866	0.5039	3.0869
9	0.3546	0.5282	0.8090	6.9622
11	0.6246	0.3542	0.5368	5.5987
13	0.5350	0.4697	1.1577	11.3140
15	0.7007	0.6055	1.6242	14.7117
17	0.5380	0.3731	1.6337	10.5752
19	0.2217	0.8451	1.8203	9.0621
21	0.5959	0.9387	1.0298	12.6258
23	0.2776	1.3887	0.5361	8.7900
25	0.2607	1.1991	1.0674	9.0372
27	0.5664	0.8394	5.1598	14.9426
29	0.7849	1.4204	2.3228	23.6152
31	1.1433	0.9264	1.9447	12.1216
33	0.5197	1.0854	1.6629	24.9364
35	0.0977	1.5858	3.9718	8.4068
37	0.3740	0.6492	5.2911	27.4718
39	0.6630	2.8990	1.2793	16.9191
41	0.4927	1.7074	5.4155	12.3760

(c)

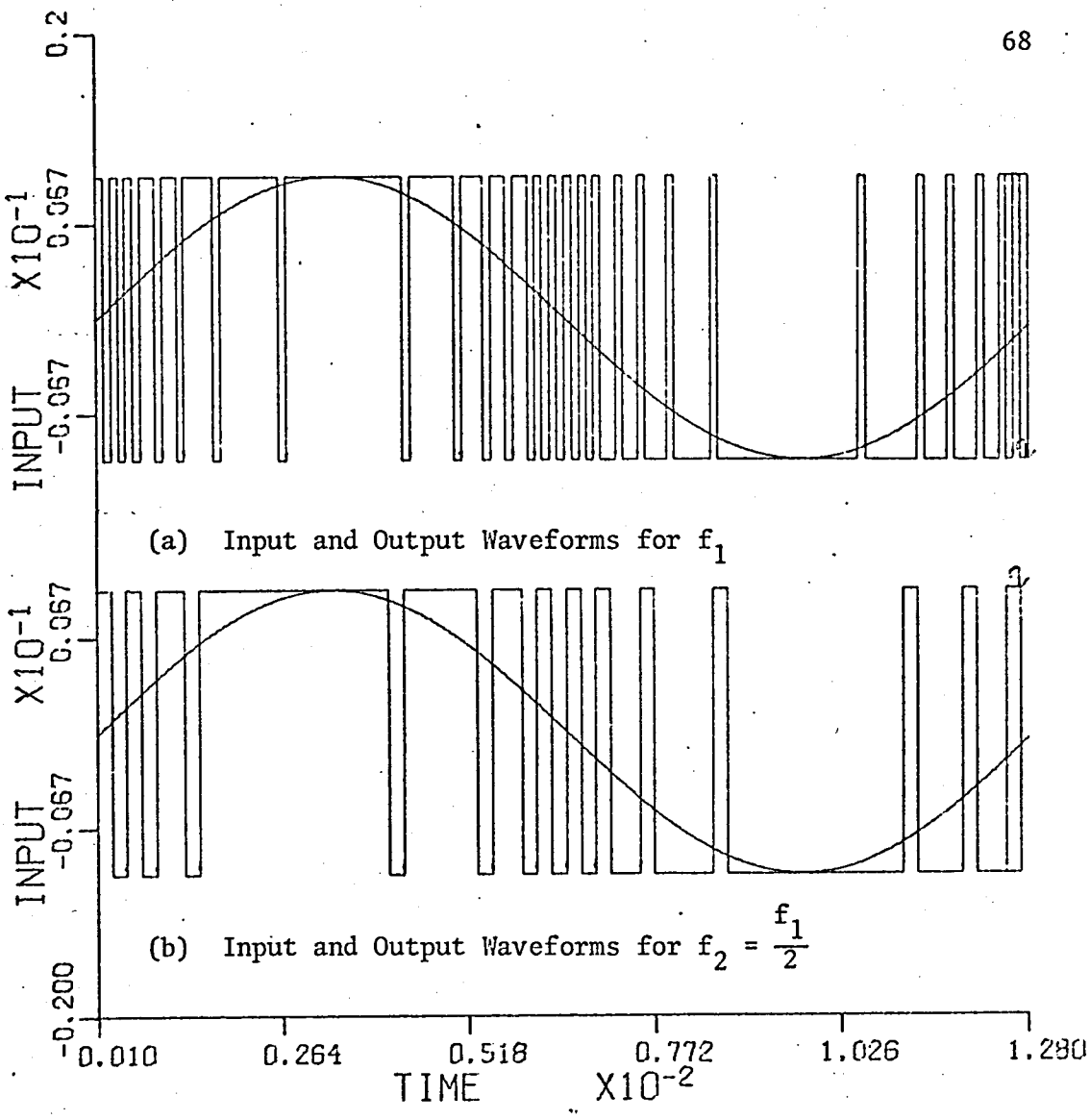


Figure 4.14: INPUT AND OUTPUT WAVEFORMS AND THE HARMONIC COMPONENTS EXPRESSED AS PERCENTAGES

HARMONIC ANALYSIS
C=1.00

NO	PERCENTAGE fclock = $8f_1$	PERCENTAGE fclock = $4f_1$	PERCENTAGE fclock = $2f_1$	PERCENTAGE fclock = f_1
1	100.0000	100.0000	100.0000	100.0000
3	1.7212	1.6994	2.3627	3.0703
5	0.8181	1.3165	0.6304	1.5097
7	0.5364	0.6092	1.4338	5.5057
9	0.3183	1.2985	0.3257	4.0297
11	0.3521	1.1247	2.1127	7.6417
13	0.2206	1.1048	1.8738	7.4408
15	0.5704	1.7541	4.9287	7.0638
17	0.1596	1.7550	3.3451	11.1707
19	1.1395	1.8692	3.1962	6.9294
21	0.8021	1.3533	1.4758	3.7097
23	0.2990	2.3163	3.1850	14.4999
25	1.2958	0.8722	4.8384	7.8337
27	1.4266	1.8842	2.3256	9.6423
29	1.6367	2.3148	2.3697	13.0080
31	1.9342	4.0675	0.7661	16.8178
33	1.3322	3.4864	5.0684	14.2611
35	1.9882	1.9855	5.2565	13.3382
37	1.1551	2.3731	5.4552	23.9745
39	0.4544	2.4534	3.7040	16.4469
41	0.4050	4.7627	4.6083	6.3813

(c)

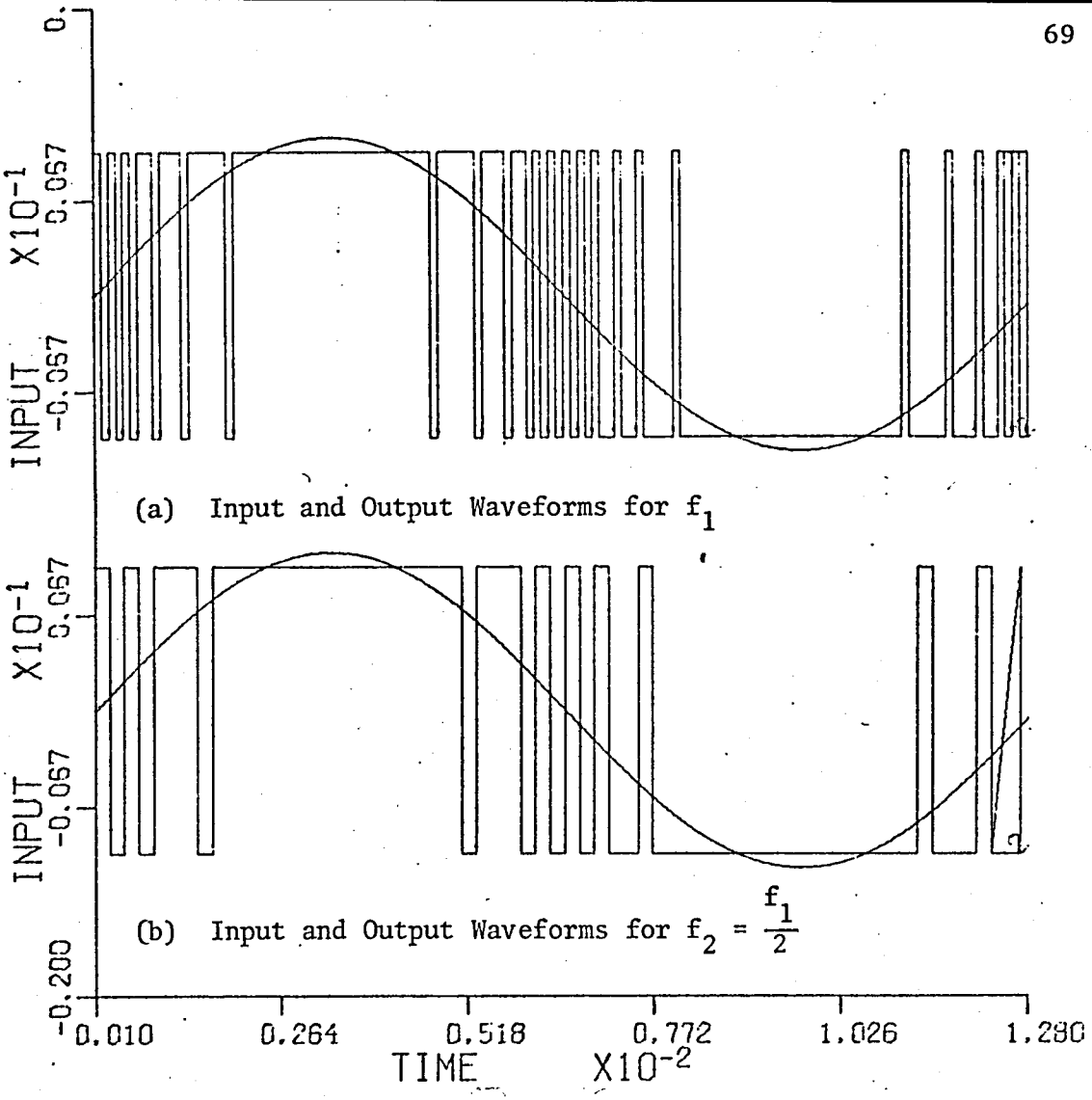


Figure 15: INPUT AND OUTPUT WAVEFORMS AND THE HARMONIC COMPONENTS EXPRESSED AS PERCENTAGES

HARMONIC ANALYSIS
C=1,10

NO	PERCENTAGE fclock = $8f_1$	PERCENTAGE fclock = $4f_1$	PERCENTAGE fclock = $2f_1$	PERCENTAGE fclock = f_1
1	100.0000	100.0000	100.0000	100.0000
3	1.1117	1.3306	2.0376	2.5221
5	0.5718	0.2870	1.1587	1.0575
7	1.2228	0.9827	2.7751	2.0285
9	1.3998	1.0353	2.4881	7.6946
11	0.7070	1.4160	0.2758	1.3508
13	0.4796	1.0605	1.1413	3.7718
15	0.4144	0.8841	4.0387	7.8699
17	0.4951	1.1968	1.1778	7.5404
19	1.0278	1.4741	2.9349	9.4573
21	0.5436	0.4429	3.2298	10.2089
23	0.3975	1.0909	1.8784	11.5296
25	0.7862	1.2140	7.9406	8.6189
27	0.2261	1.1907	4.0616	15.5502
29	0.7732	1.9640	9.2421	12.9652
31	0.2420	2.7566	2.6439	9.7538
33	0.3517	1.0813	4.9251	2.7386
35	0.9655	1.8410	7.6607	14.8184
37	0.7529	4.5442	8.6053	23.8675
39	0.3424	1.2386	9.9186	9.0765
41	0.7358	3.2488	9.6472	19.3540

(c)

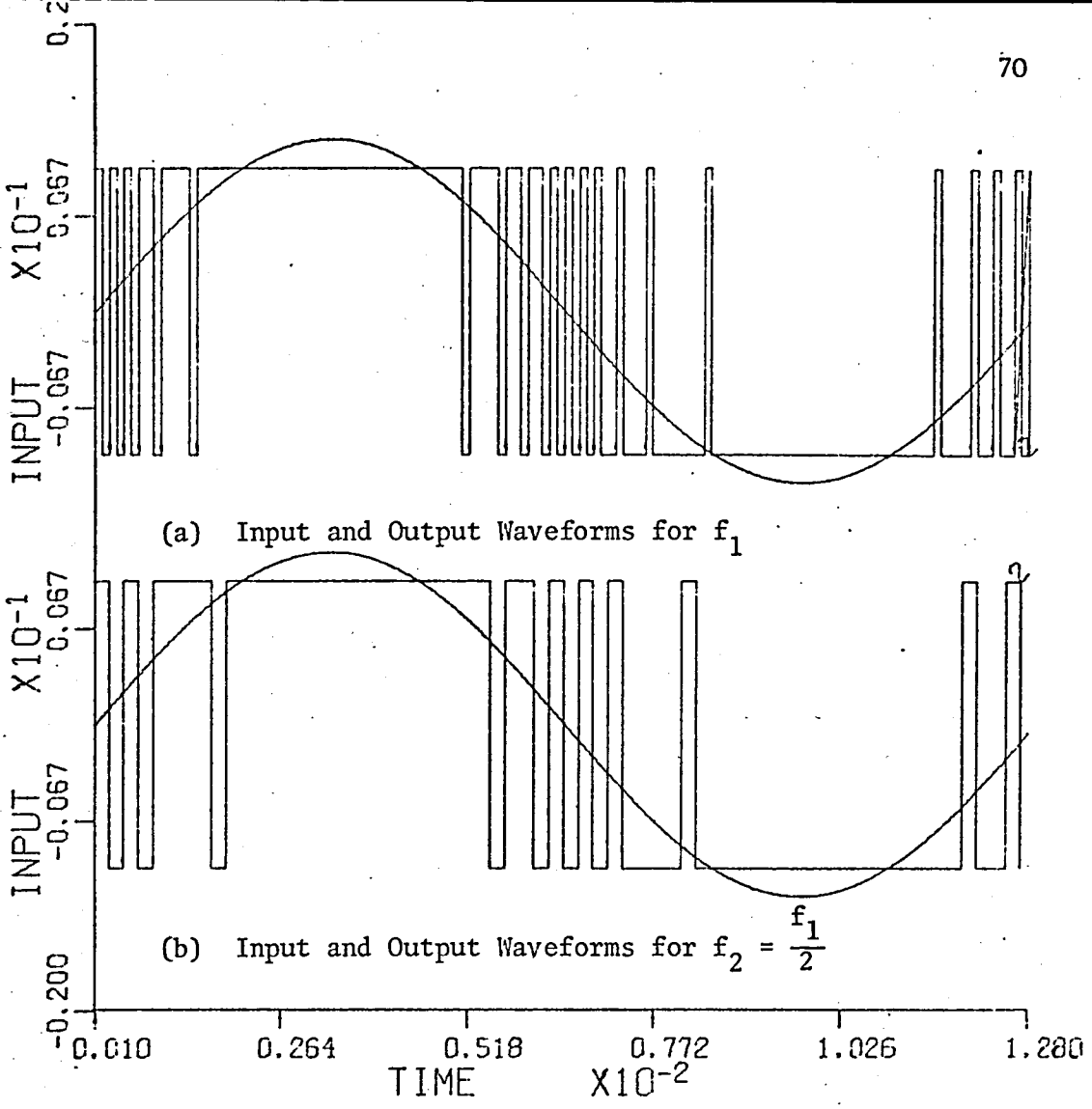


Figure 4.16: INPUT AND OUTPUT WAVEFORMS AND THE HARMONIC COMPONENTS EXPRESSED AS PERCENTAGES

HARMONIC ANALYSIS
C=1,20

NO	PERCENTAGE fclock = $8f_1$	PERCENTAGE fclock = $4f_1$	PERCENTAGE fclock = $2f_1$	PERCENTAGE fclock = f_1
1	100.0000	100.0000	100.0000	100.0000
3	2.4973	2.6990	2.7555	3.1684
5	3.1808	3.1176	4.4253	4.2181
7	1.8045	2.0121	2.8950	2.4824
9	0.3485	0.6228	1.8372	3.5681
11	0.9979	1.6961	1.6086	2.2005
13	0.7983	0.9152	0.8017	4.3600
15	0.3497	0.5207	2.2394	3.7492
17	0.8812	1.7765	1.5196	11.9608
19	0.2619	0.1101	1:4591	3.5434
21	0.4159	0.3185	3.2110	13.7417
23	0.9015	2.3475	3.2473	4.6233
25	0.0744	1.4319	3.9077	11.3794
27	0.3784	0.6038	3.8301	10.0846
29	0.7445	1.3496	5.0591	7.6411
31	0.0232	2.1996	8.5990	8.7602
33	0.3565	1.4114	2.8910	17.8767
35	0.8666	1.5379	6.5449	9.6706
37	0.8136	2.5582	1.4611	6.8550
39	0.2140	1.6448	6.9146	7.7214
41	1.0825	1.8525	5.0594	12.0834

(c)

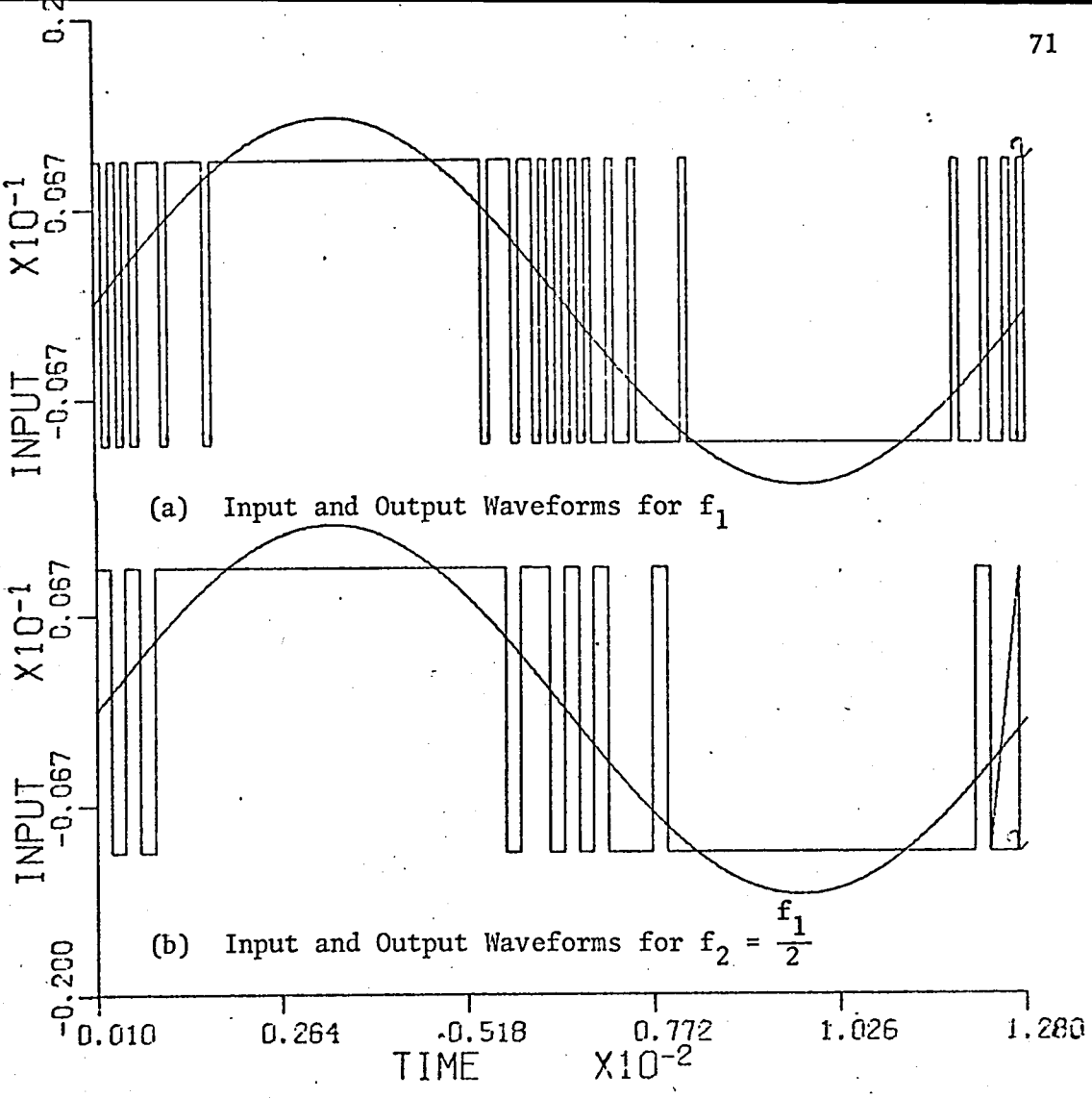


Figure 4.17: INPUT AND OUTPUT WAVEFORMS AND THE HARMONIC COMPONENTS EXPRESSED AS PERCENTAGES

HARMONIC ANALYSIS
C=1.30

NO	PERCENTAGE fclock = $8f_1$	PERCENTAGE fclock = $4f_1$	PERCENTAGE fclock = $2f_1$	PERCENTAGE fclock = f_1
1	100.0000	100.0000	100.0000	100.0000
3	6.1275	6.3464	6.2162	7.4412
5	4.0597	4.4486	4.5779	5.6097
7	0.7438	0.8541	0.8247	3.4979
9	1.0187	1.6805	2.0636	3.2151
11	1.2030	1.4580	2.1129	7.8763
13	0.4577	1.2300	0.8306	6.0834
15	0.6674	1.0860	1.2769	5.4994
17	0.3093	0.6694	1.1358	11.2143
19	0.6481	0.9307	1.9451	7.3176
21	0.1403	0.4391	0.7154	12.3592
23	0.3025	0.9480	1.0895	7.2044
25	0.6276	0.7237	3.7326	7.4373
27	0.3501	2.1148	5.7609	13.2176
29	0.1950	0.5303	0.8575	7.9306
31	0.9403	1.8475	4.3817	7.9123
33	1.0187	1.1559	0.9521	9.7040
35	0.3114	1.9632	7.9623	20.0563
37	0.3349	0.2750	4.9284	17.5926
39	0.8710	1.7080	5.4652	1.3286
41	0.5769	1.1648	6.3179	18.3525

(c)

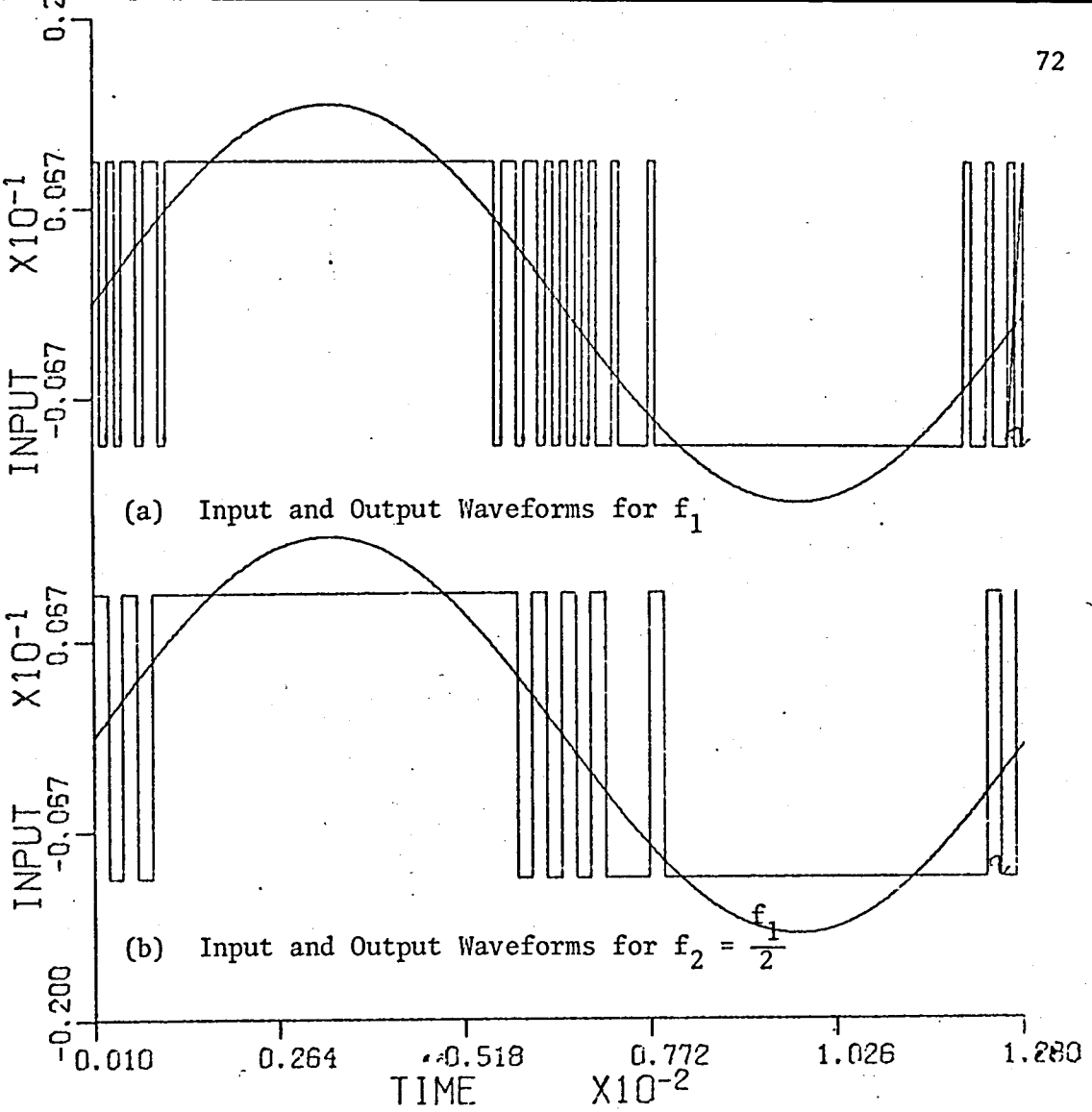


Figure 4.18: INPUT AND OUTPUT WAVEFORMS AND THE HARMONIC COMPONENTS EXPRESSED AS PERCENTAGES

HARMONIC ANALYSIS
C=1,40

NO	PERCENTAGE fclock = $8f_1$	PERCENTAGE fclock = $4f_1$	PERCENTAGE fclock = $2f_1$	PERCENTAGE fclock = f_1
1	100.0000	100.0000	100.0000	100.0000
3	9.4152	9.3306	10.2728	10.8515
5	4.1041	4.6038	5.7123	6.6047
7	0.7608	1.1586	2.9335	5.1770
9	1.9204	2.0343	2.3846	2.4693
11	0.3296	0.5448	2.3836	3.7969
13	1.2252	1.3645	1.3625	2.6448
15	0.3710	0.5111	2.8385	4.8272
17	0.7498	1.3298	0.6861	4.4542
19	0.4255	0.8699	1.7876	3.8852
21	1.0122	1.6756	0.4407	5.0230
23	0.2186	1.2124	3.3141	2.7603
25	0.4342	0.1536	4.9006	4.5007
27	0.3831	0.7428	2.4419	6.7012
29	0.8983	1.6688	0.9485	3.1627
31	0.4671	1.0743	0.8393	3.3245
33	0.3366	0.6013	2.3265	6.5690
35	0.3802	0.8157	3.8111	7.2007
37	0.6534	1.2106	0.4360	12.6211
39	0.0292	1.5330	5.0460	14.9543
41	0.4423	0.1090	6.2765	9.1777

(c)

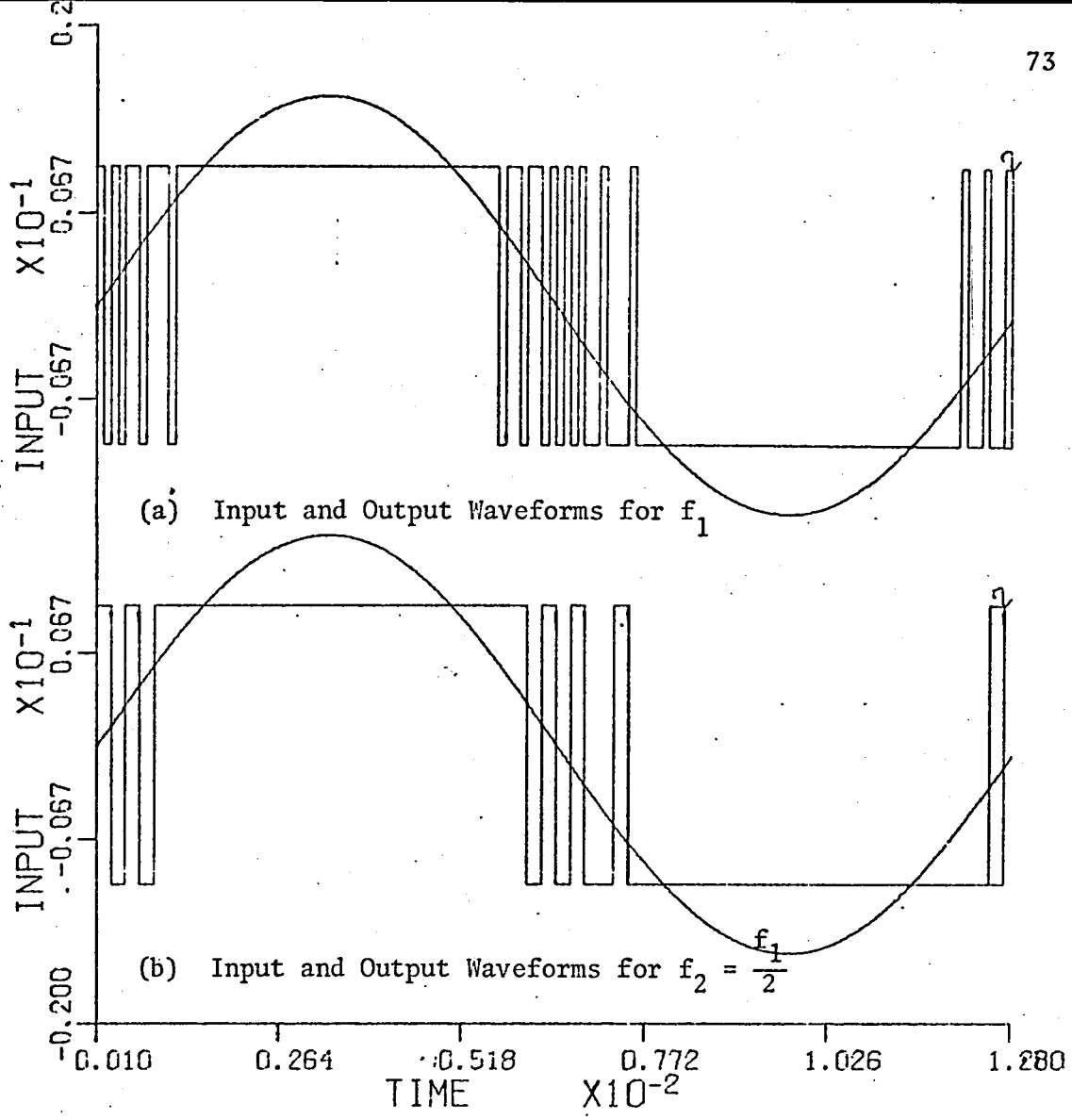


Figure 4.19: INPUT AND OUTPUT WAVEFORMS AND THE HARMONIC COMPONENTS EXPRESSED AS PERCENTAGES

HARMONIC ANALYSIS
C=1,50

NO	PERCENTAGE fclock = $8f_1$	PERCENTAGE fclock = $4f_1$	PERCENTAGE fclock = $2f_1$	PERCENTAGE fclock = f_1
1	100.0000	100.0000	100.0000	100.0000
3	11.9311	12.2875	12.6400	13.5022
5	3.5523	3.6372	3.9689	5.5715
7	1.9564	2.4210	2.7516	5.7643
9	1.4788	1.2838	1.2822	0.7213
11	1.1499	1.3110	1.1100	4.5581
13	0.6297	0.7707	1.8275	2.6368
15	0.6660	1.2811	2.1842	3.4301
17	0.4332	0.4701	1.2970	8.2509
19	0.4964	0.6315	3.8520	7.7019
21	0.4697	0.4335	3.0744	2.2641
23	0.7968	0.5647	3.3478	4.2659
25	0.2042	1.1238	4.2031	6.5248
27	0.2800	0.9290	0.7314	7.2016
29	0.4218	0.6056	4.0305	12.4028
31	0.7804	1.3649	4.6647	15.3914
33	0.3308	0.4232	2.6979	10.3585
35	0.6872	1.5265	5.7951	3.1770
37	0.4039	1.3427	4.6889	15.8984
39	0.4068	0.8163	3.8301	22.8849
41	0.4361	2.3012	7.4889	20.0701

(c)

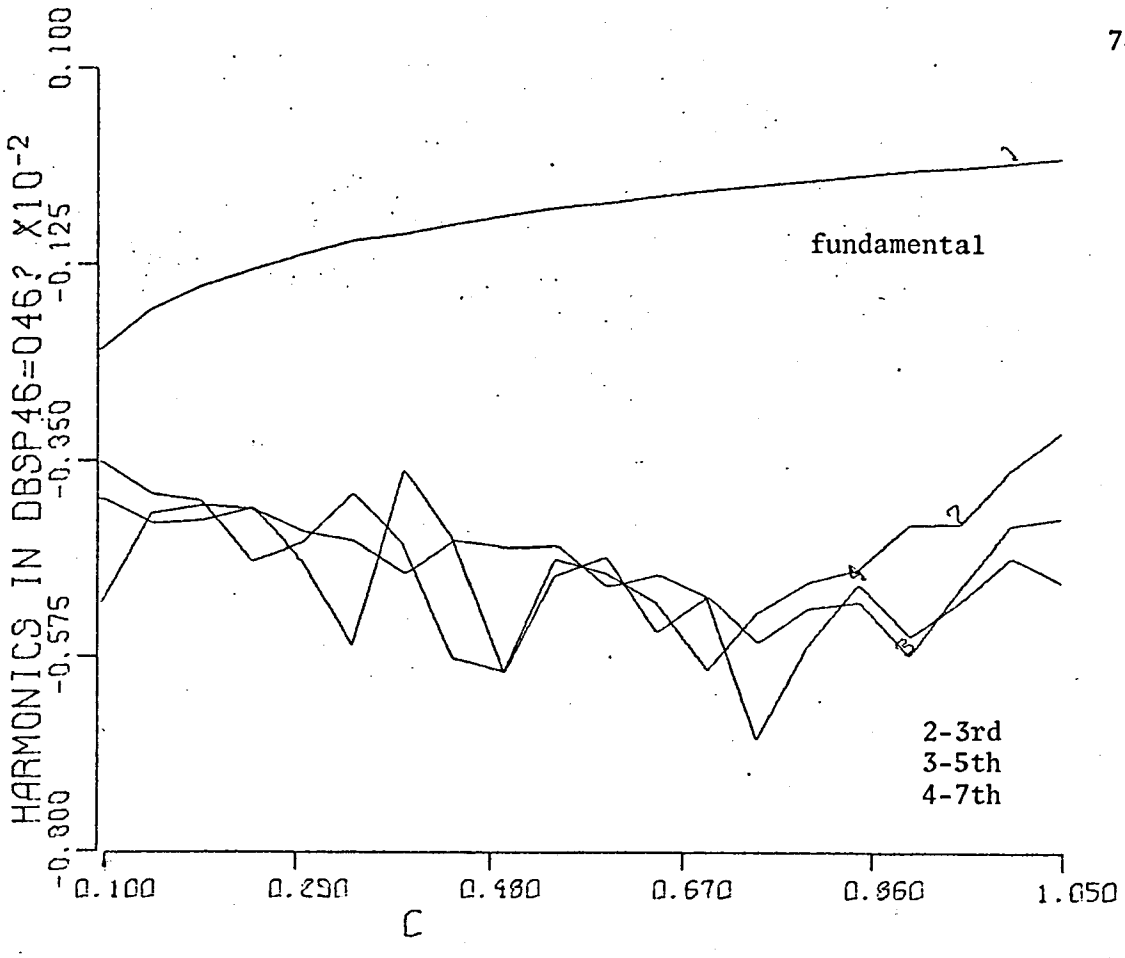


Figure 4.20: VARIATION OF HARMONICS WITH INPUT SINE WAVE AMPLITUDE, C
fclock=8f_1

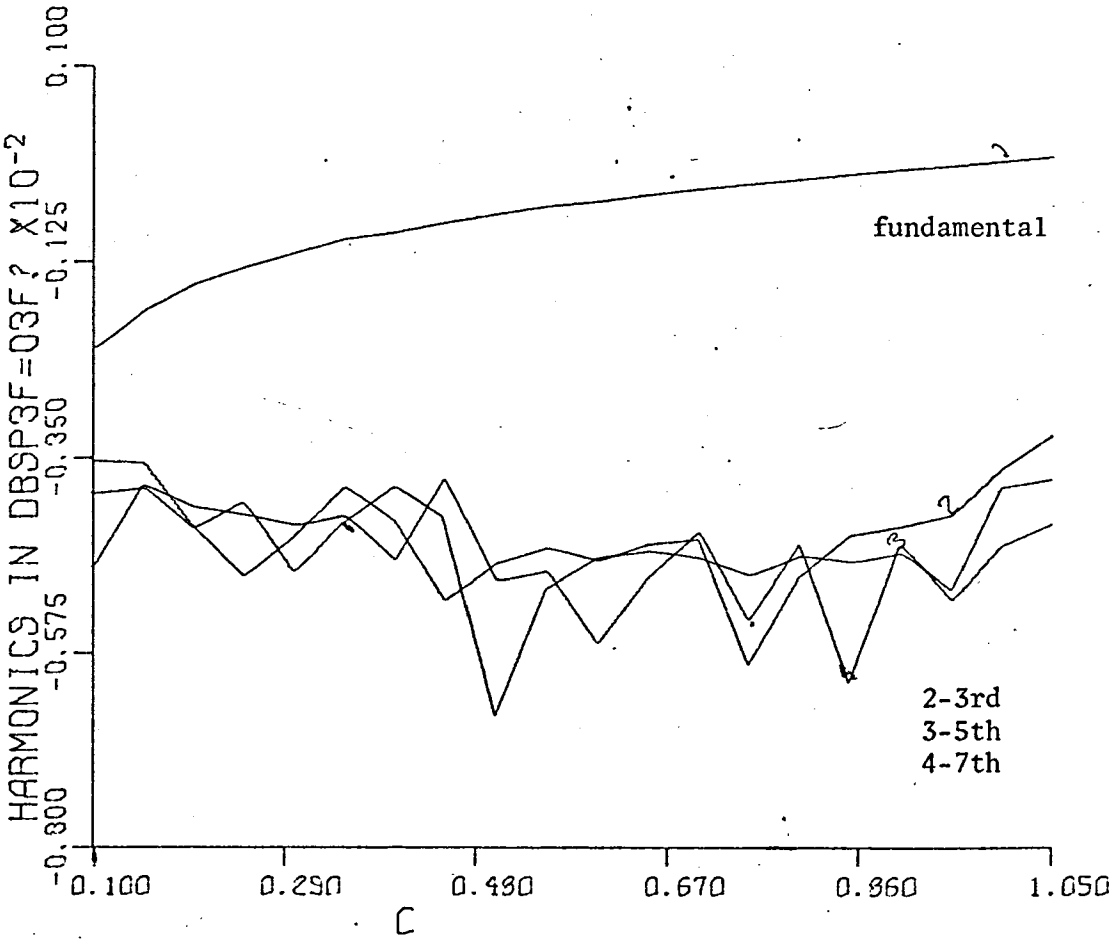


Figure 4.21: VARIATION OF HARMONICS WITH INPUT SINE WAVE AMPLITUDE, C
fclock=4f_1

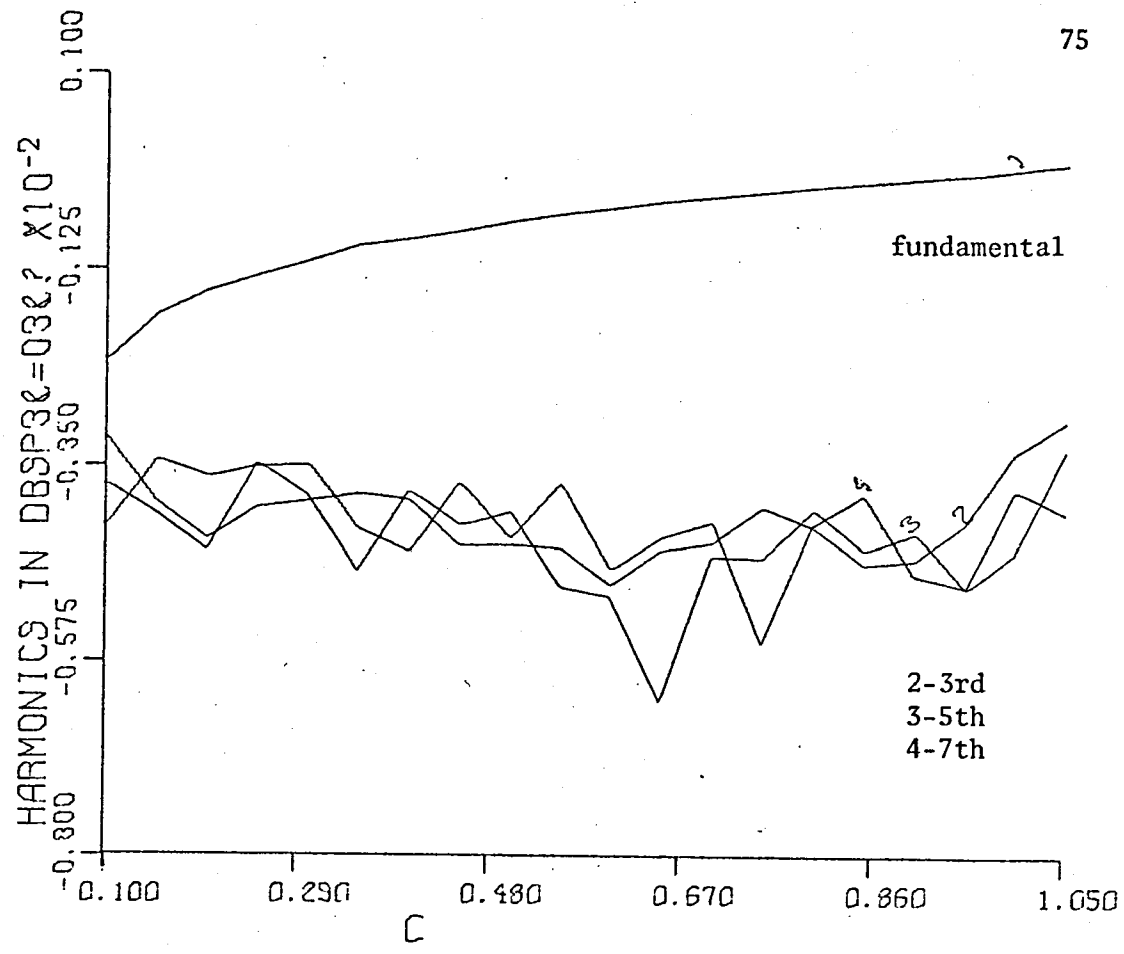


Figure 4.22: VARIATION OF HARMONICS WITH INPUT SINE WAVE AMPLITUDE, C
fclock=$2f_1$

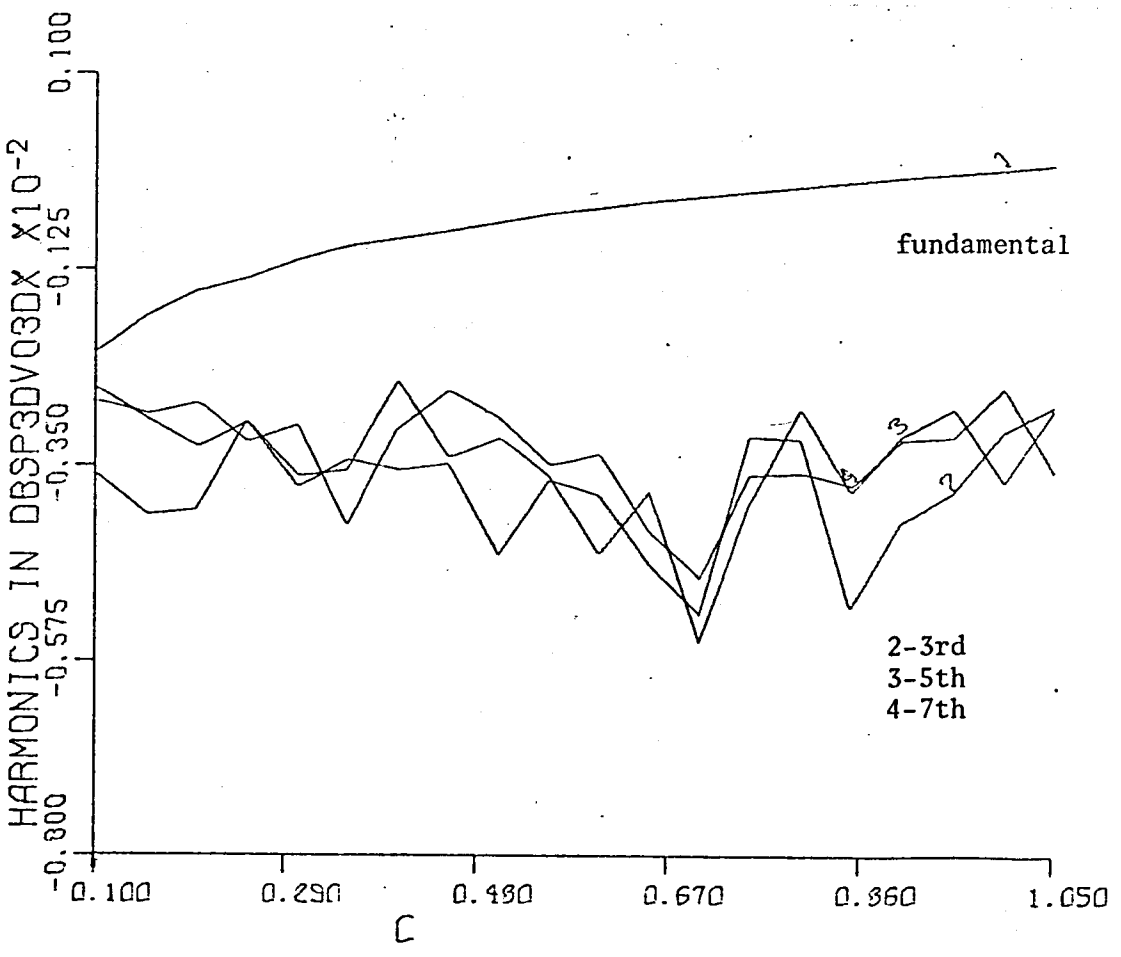
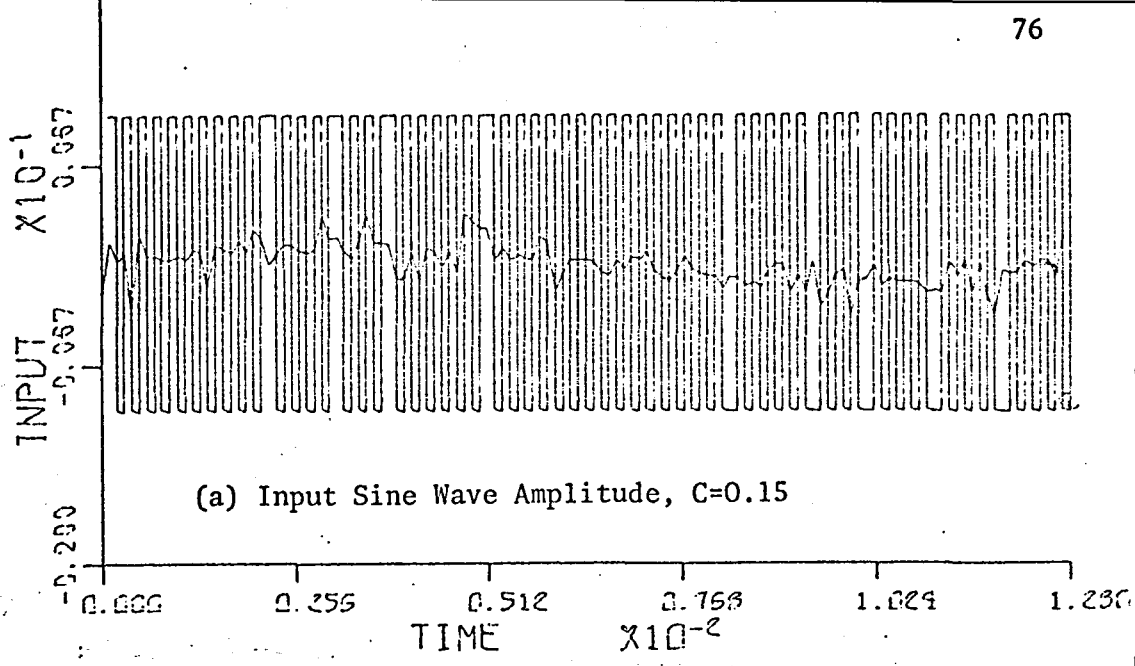
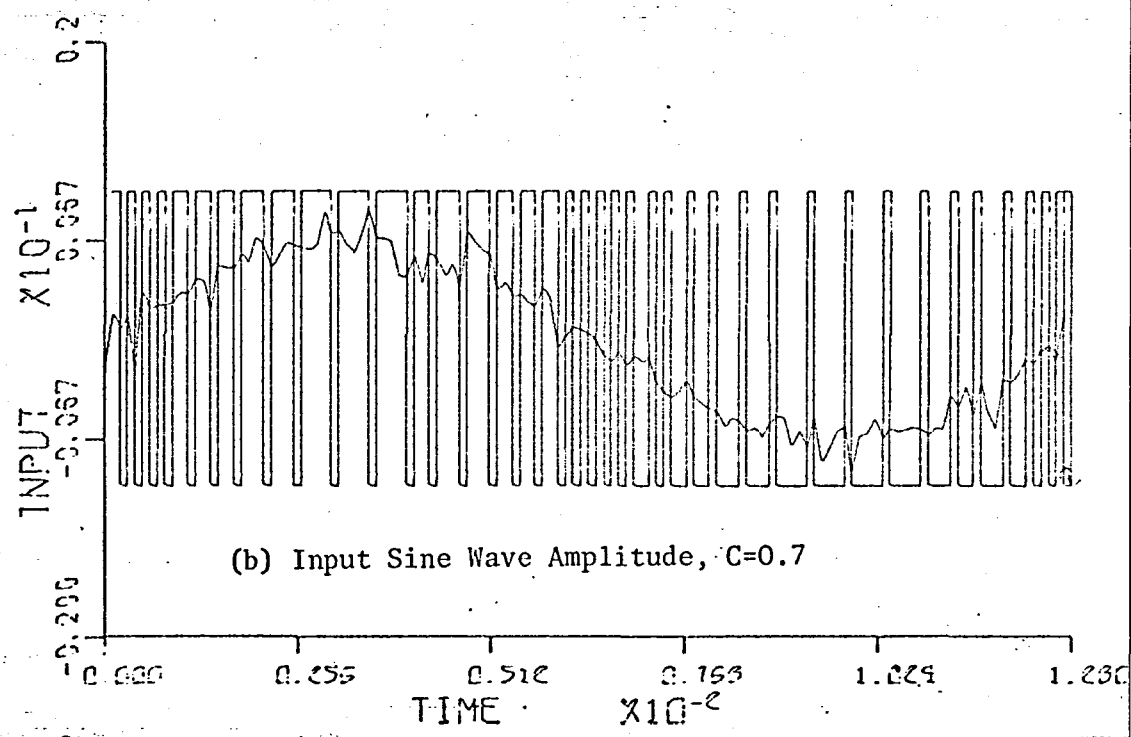


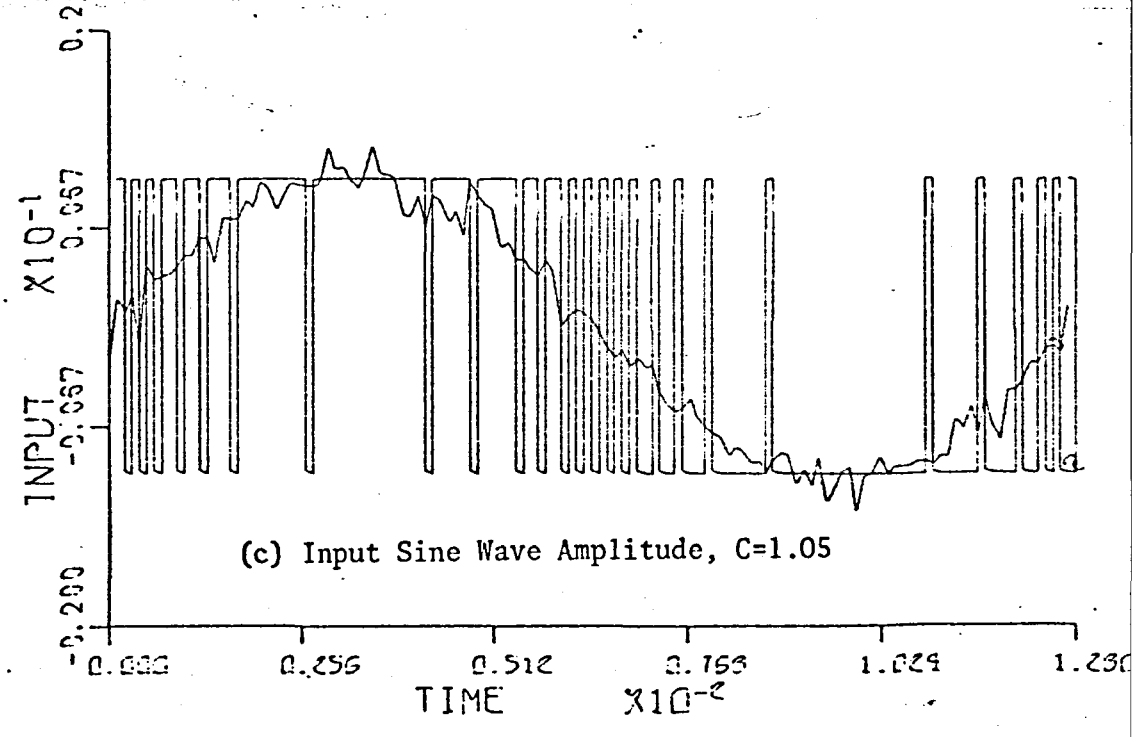
Figure 4.23: VARIATION OF HARMONICS WITH INPUT SINE WAVE AMPLITUDE, C
fclock=f_1



(a) Input Sine Wave Amplitude, C=0.15



(b) Input Sine Wave Amplitude, C=0.7



(c) Input Sine Wave Amplitude, C=1.05

Figure 4.24: INPUT AND OUTPUT WAVEFORMS OF Δ-Σ MODULATOR WHEN INPUT CONTAINS NOISE

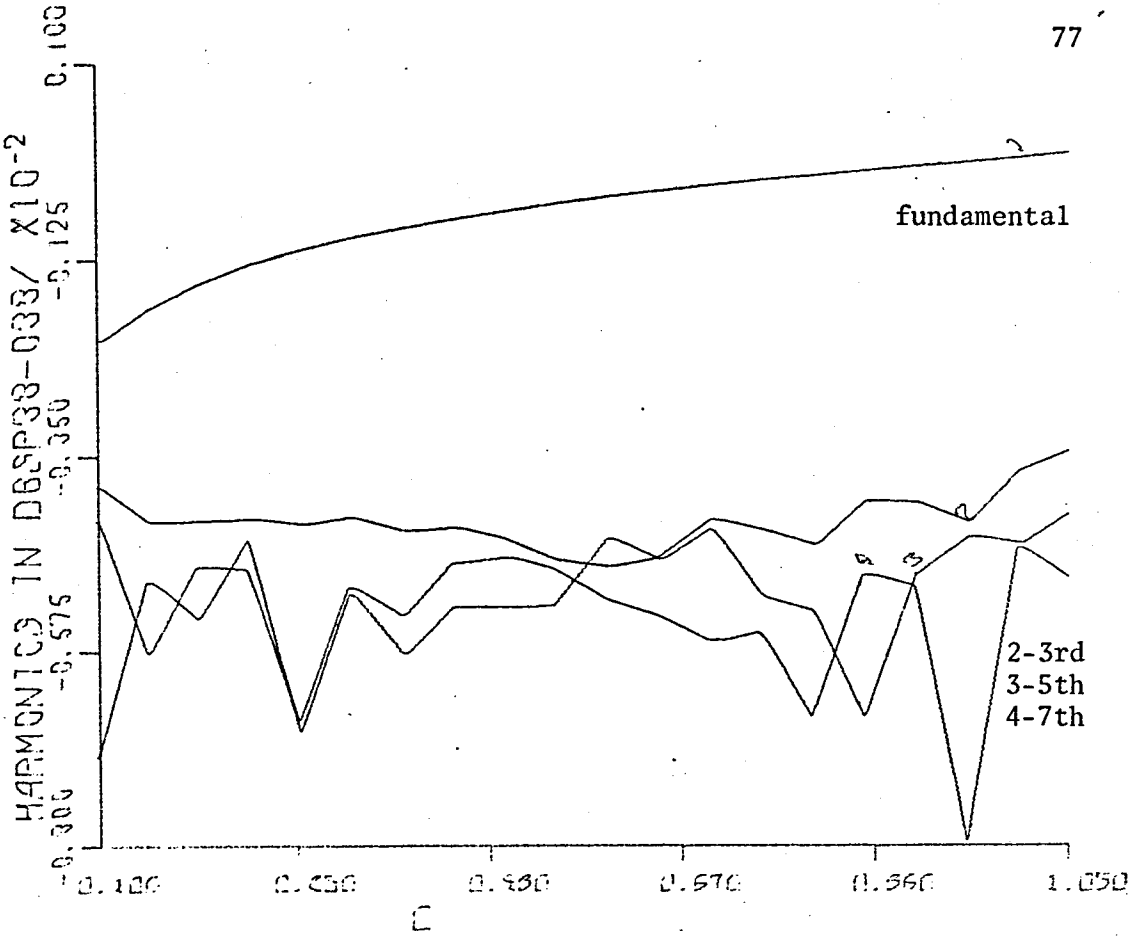


Figure 4.25: VARIATION OF HARMONICS WITH INPUT SINE WAVE AMPLITUDE, C (when input contains noise), fclock=8f_1

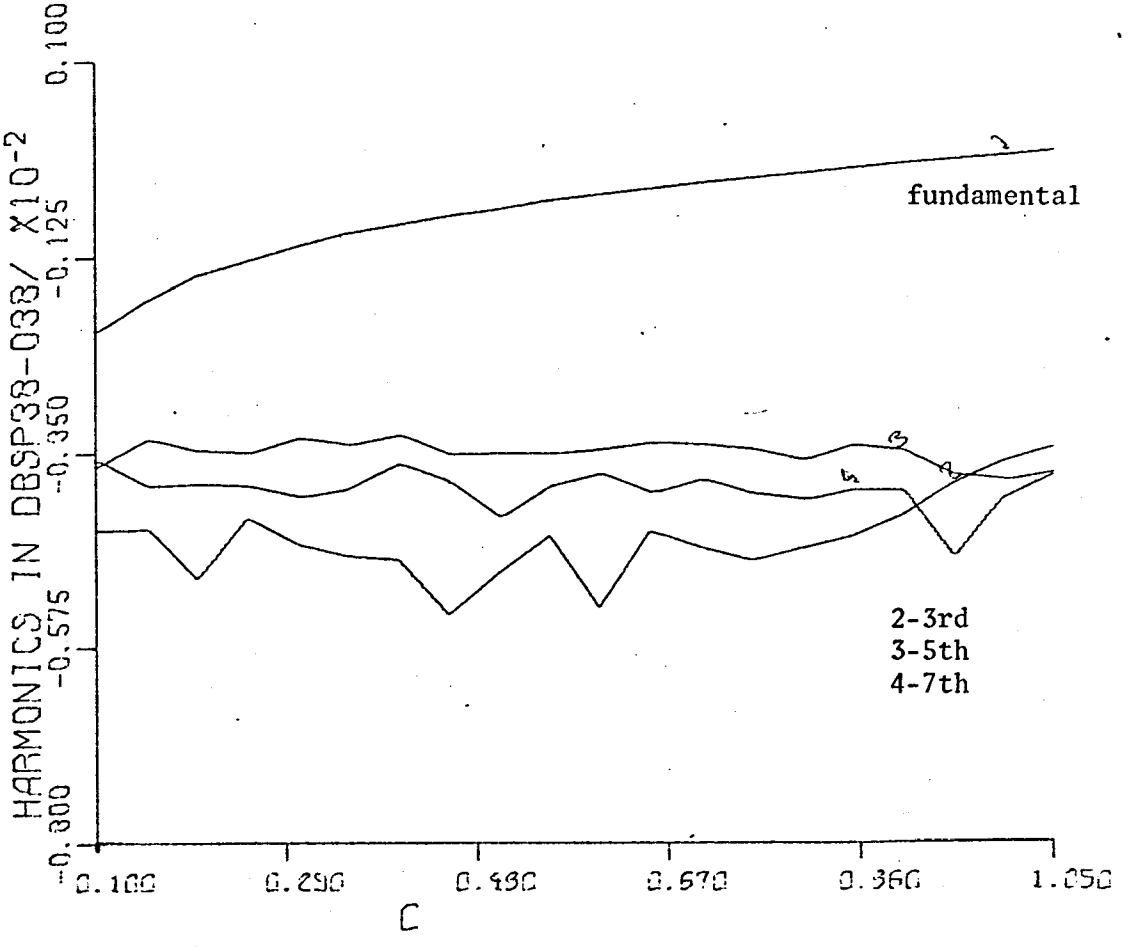


Figure 4.26: VARIATION OF HARMONICS WITH INPUT SINE WAVE AMPLITUDE, C (when input contains noise), fclock=4f_1

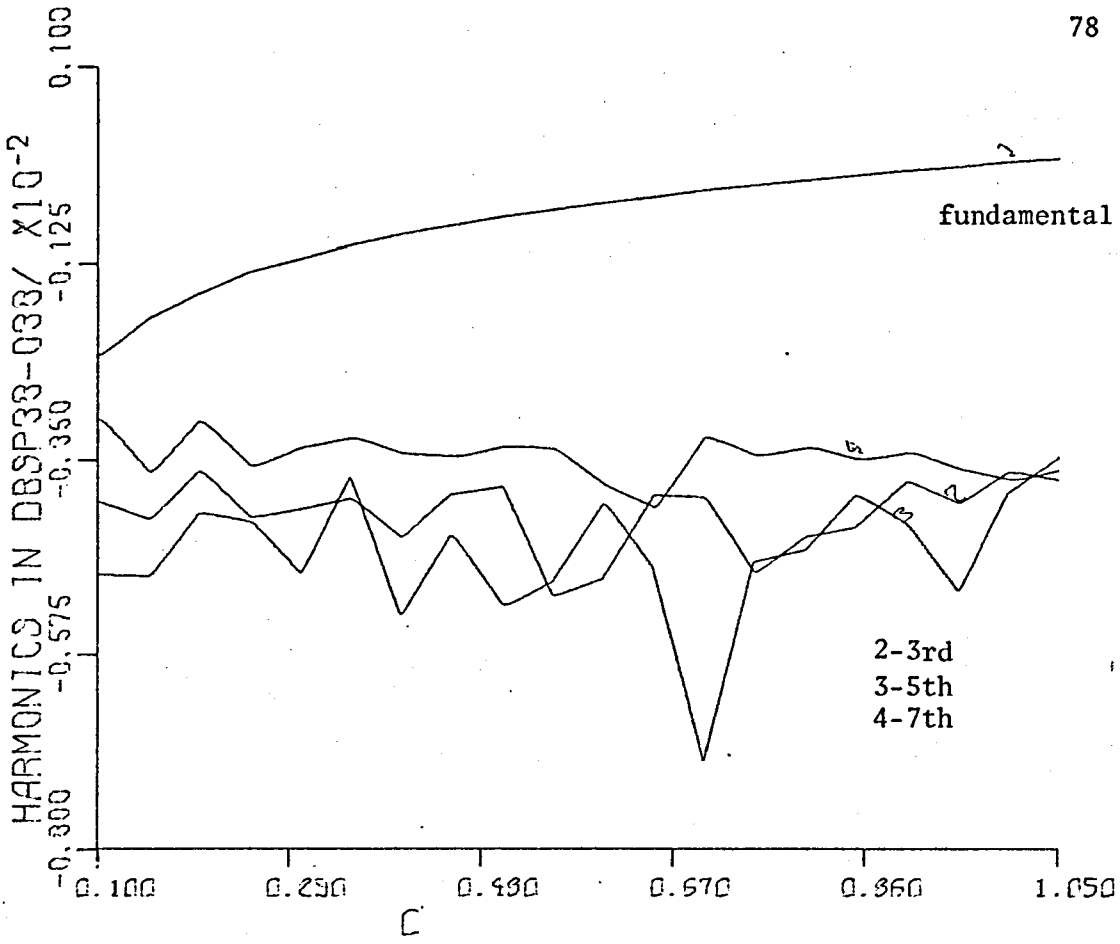


Figure 4.27: VARIATION OF HARMONICS WITH INPUT SINE WAVE AMPLITUDE, C (when input contains noise), fclock=$2f_1$

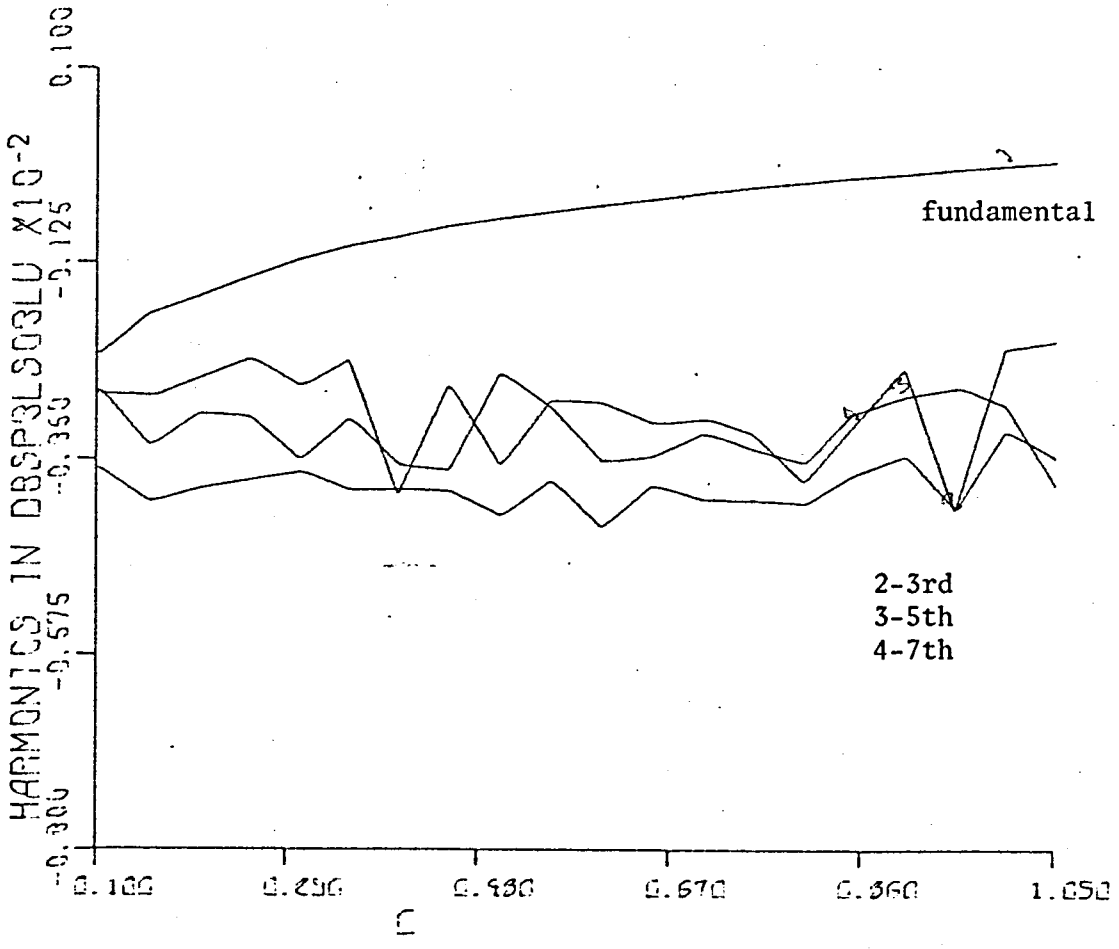
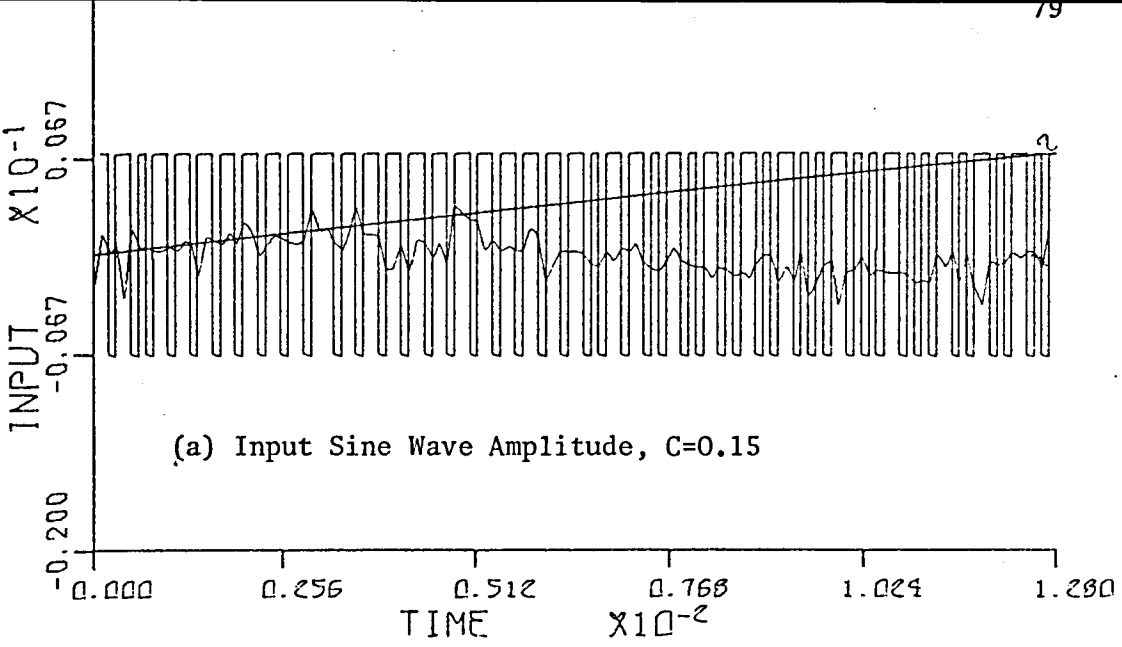
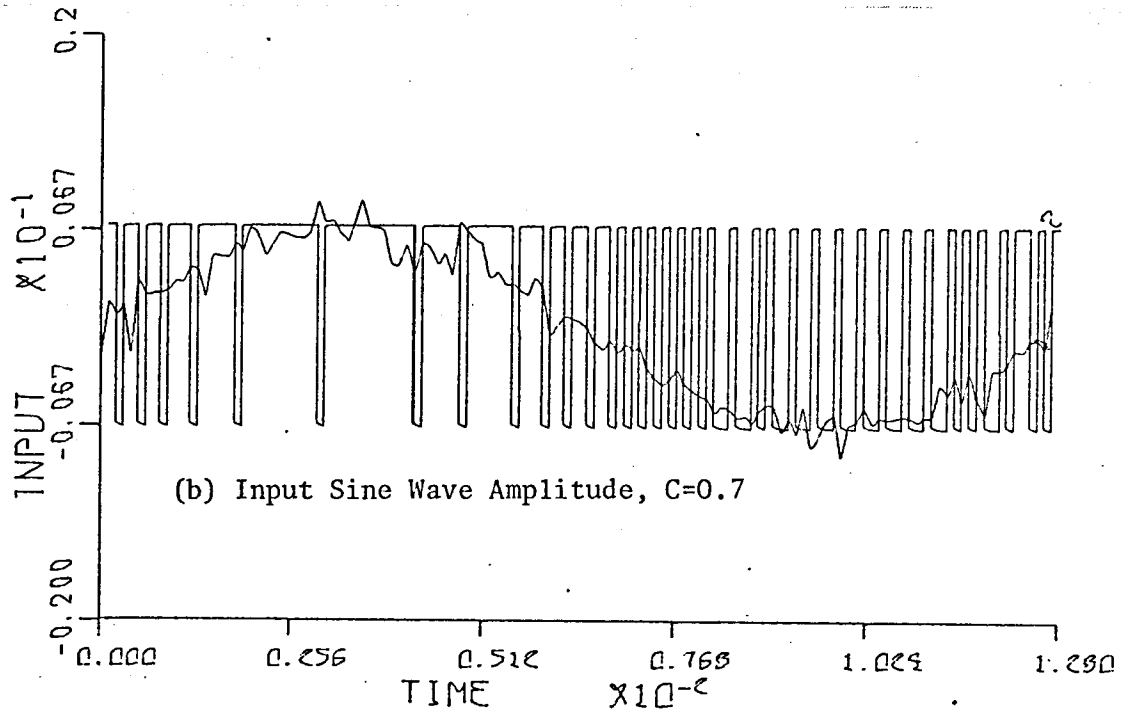


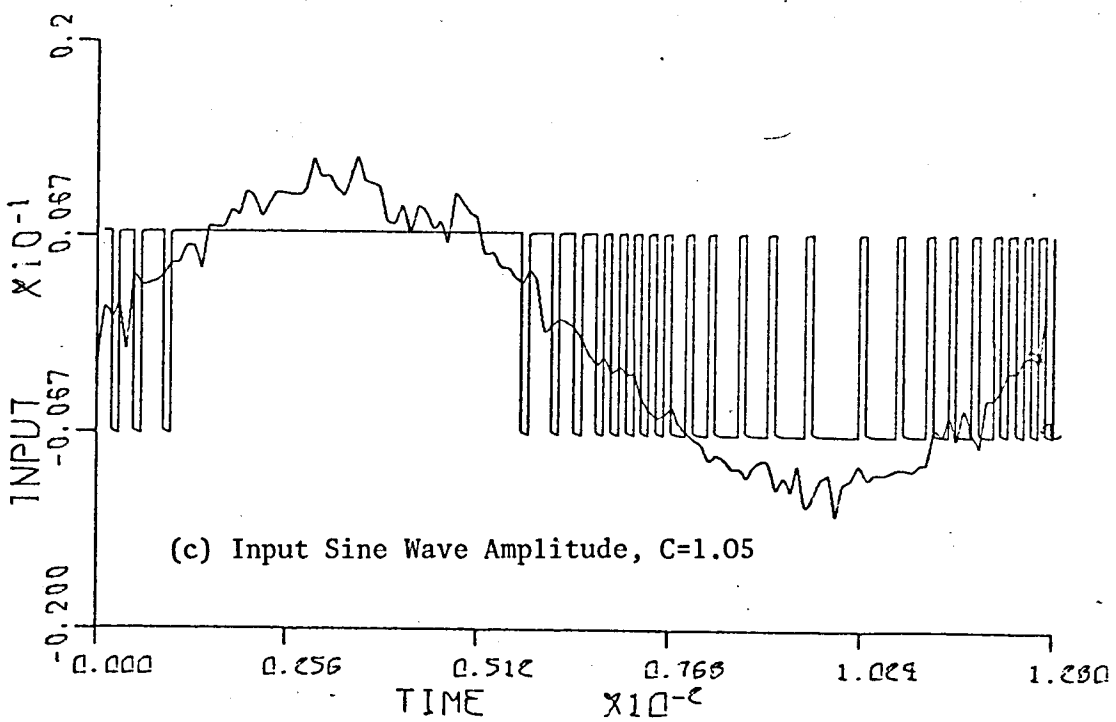
Figure 4.28: VARIATION OF HARMONICS WITH INPUT SINE WAVE AMPLITUDE, C (when input contains noise), fclock=f_1



(a) Input Sine Wave Amplitude, C=0.15



(b) Input Sine Wave Amplitude, C=0.7



(c) Input Sine Wave Amplitude, C=1.05

Figure 4.29: INPUT AND OUTPUT WAVEFORMS OF Δ-Σ MODULATOR WHEN INPUT CONTAINS NOISE AND DISTORTION IS PRESENT

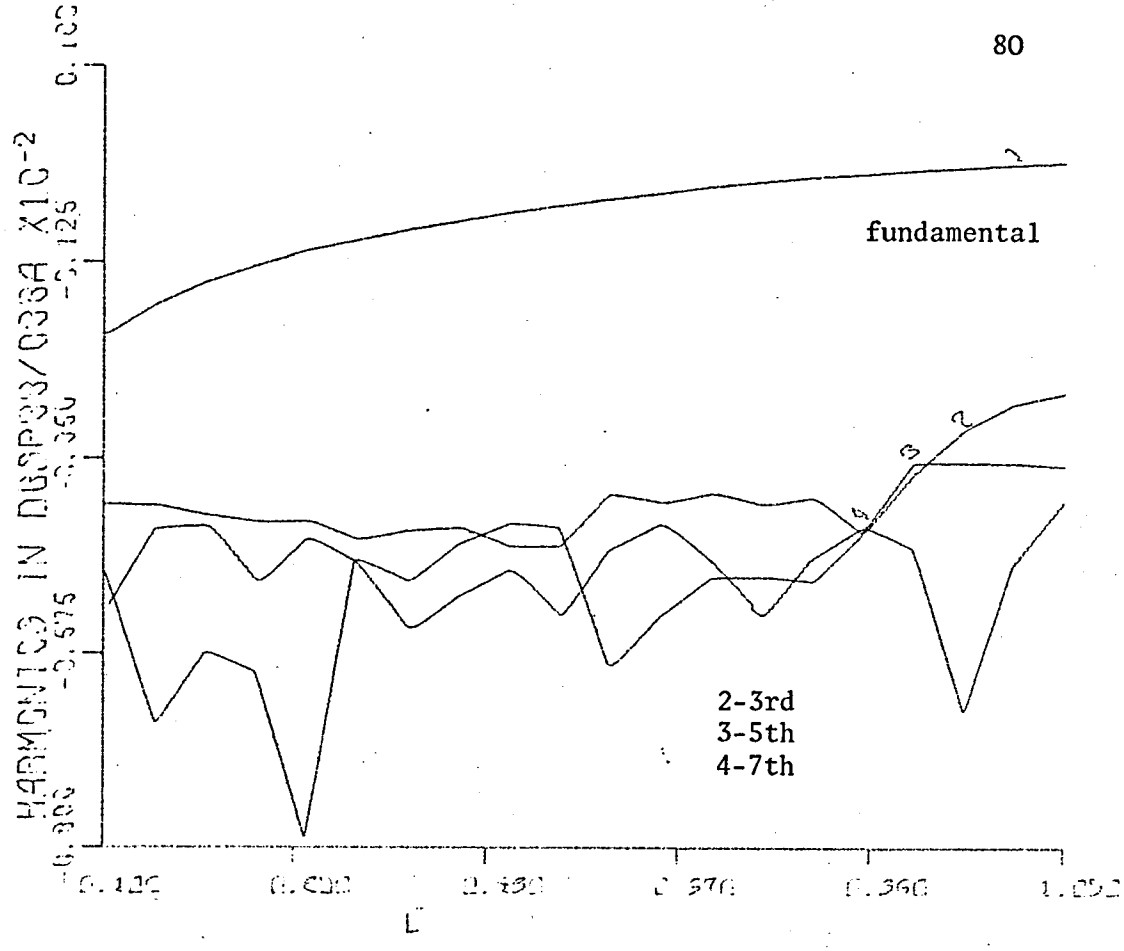


Figure 4.30: VARIATION OF HARMONICS WITH INPUT SINE WAVE AMPLITUDE, C (with noise and distortion), fclock=8f_1

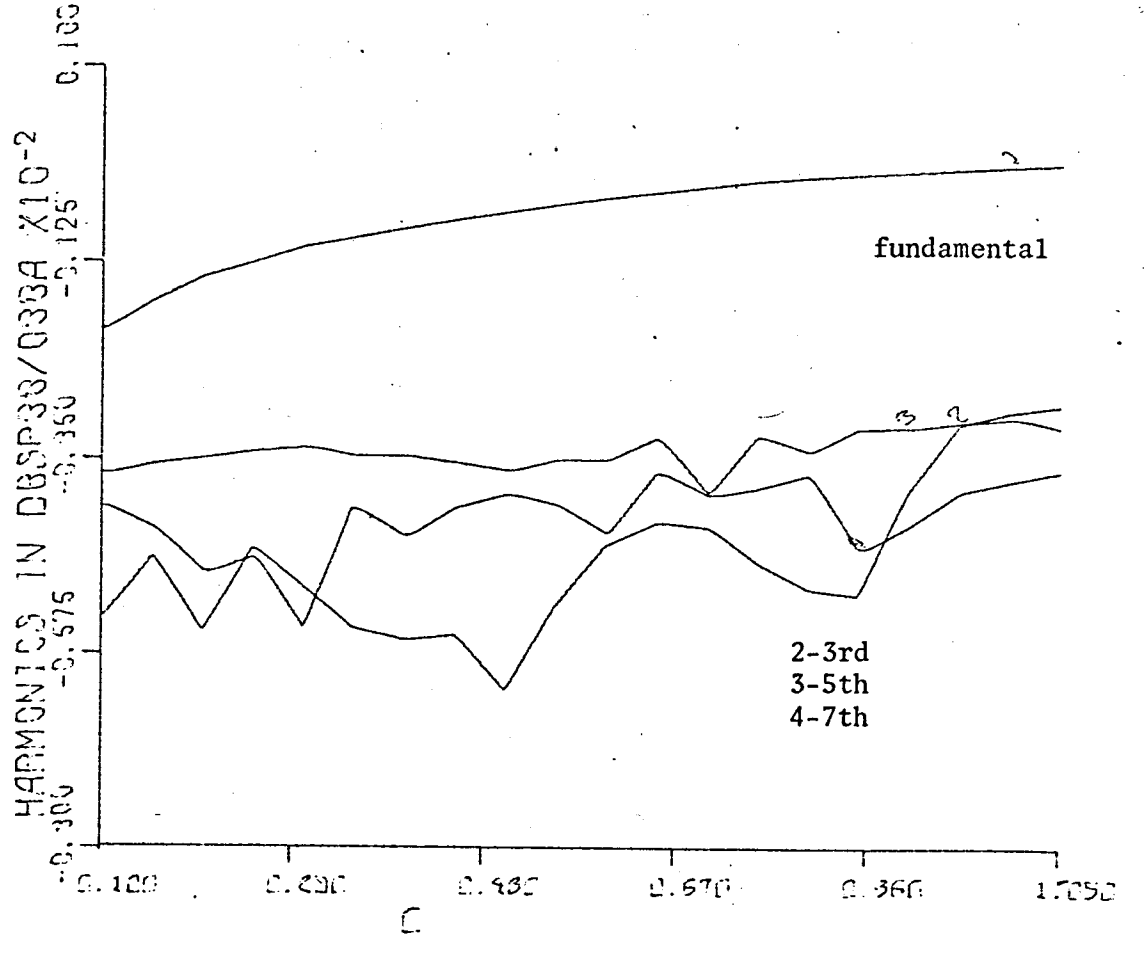


Figure 4.31: VARIATION OF HARMONICS WITH INPUT SINE WAVE AMPLITUDE, C (with noise and distortion), fclock=4f_1

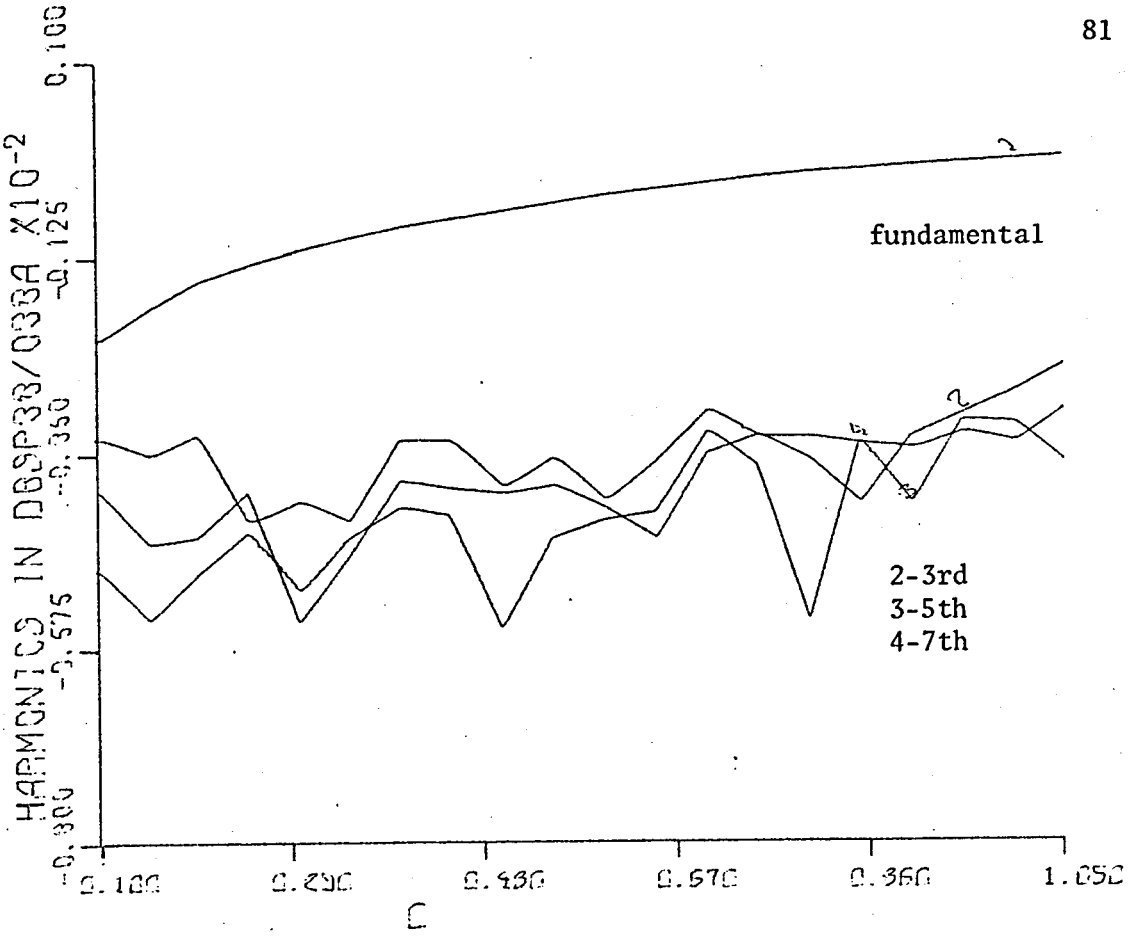


Figure 4.32: VARIATION OF HARMONICS WITH INPUT SINE WAVE AMPLITUDE, C (with noise and distortion), fclock=$2f_1$

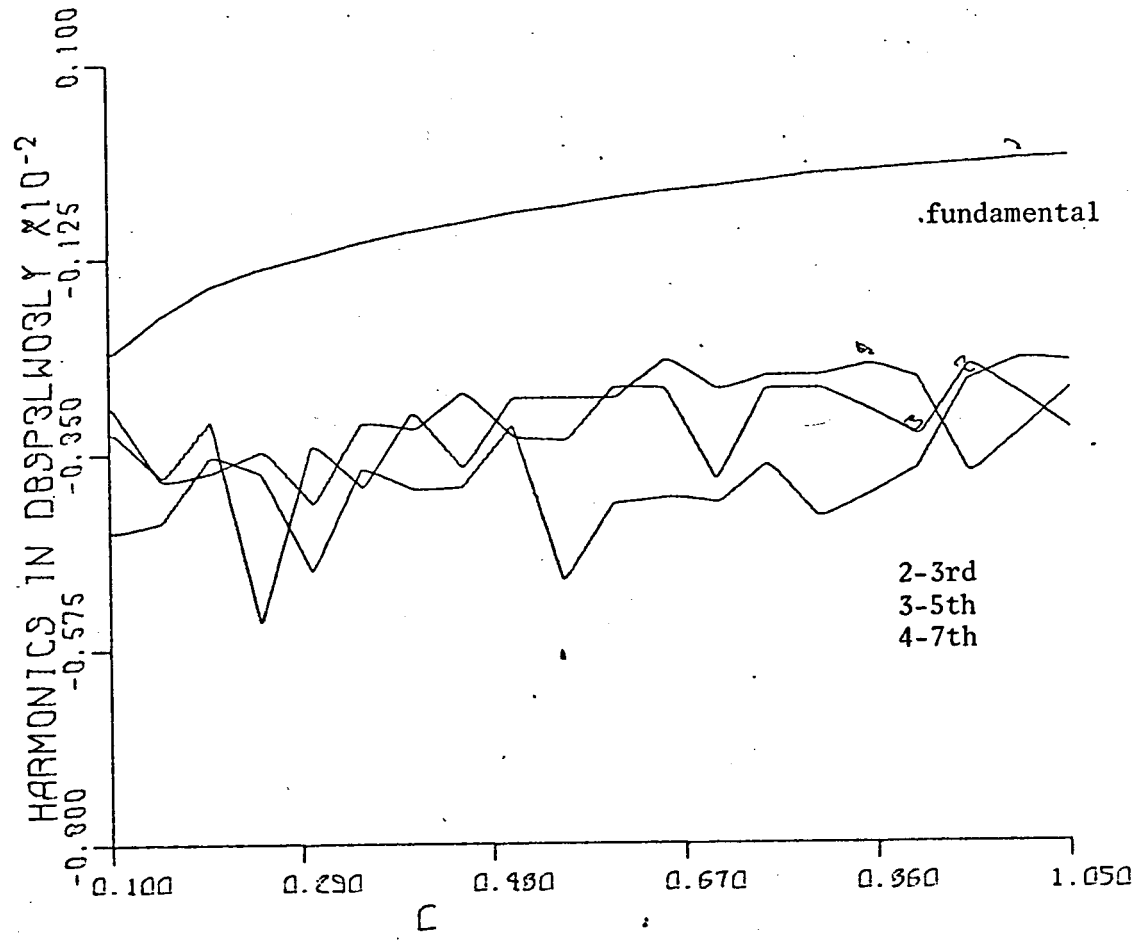


Figure 4.33: VARIATION OF HARNOMICS WITH INPUT SINE WAVE AMPLITUDE, C (with noise and distortion), fclock=f_1

CHAPTER 5

DESIGN AND PERFORMANCE OF DELTA SIGMA MODULATORS

5.1 DESIGN OF DELTA SIGMA MODULATOR WITH SINGLE INTEGRATION[20-21]

A block diagram for a Δ-Σ modulator is shown in Figure 5.1. The modulator consists of an input amplifier, a comparator, a D-type flip-flop, a binary level converter and two RC integrators.

5.1.1 Input Amplifier

The inclusion of an input amplifier enables the exploitation of the full input dynamic range of the modulator (since the peak amplitude of the signal obtained from the signal generator cannot reach the overload level) and, since it has two input terminals it also makes possible the superposition of two input signals, thereby permitting an intermodulation test to be performed should this be needed.

The 741 operational amplifier used at the input was designed to give a gain of ten, sufficient to increase the input signal amplitude to the overload level. The amplifier circuit is shown in Figure 5.2. For a gain of 10

$$10 = -\frac{R_2}{R_1}$$

and the values of R_1 and R_2 were chosen as

$$R_1 = 10k\Omega$$

$$R_2 = 100k\Omega$$

5.1.2 Comparator

An operational amplifier μA710 is used to compare the input analog signal with the integrated version of the digitally encoded signal. A minimum of about 5mV was needed for stable operation.

5.1.3 Flip-Flop

A 7474N D-type edge-triggered flip-flop is used to encode the output of the comparator in a digital sequence. As this employed TTL compatible logic

it can feed or be fed by other TTL circuits. Supply voltages of +5V and OV are needed, and high level and low level outputs of 3.6V and 0.3V are obtained. The flip-flop is triggered by clock pulses taken directly from a signal generator, and it functions such that the input to the flip-flop appears at the output at clock times, and is held there for one clock period (i.e. a sample and hold action).

5.1.4 Binary Level Converter

A μA709 operational amplifier is used as a binary level converter, to enable the high and low voltage levels of the digital sequence to be obtained symmetrically disposed relative to zero. This makes the mean level of the digital signal the same as that of the input analog signal, which is taken as zero, and supply voltages of ±12V give a voltage swing of ±12V relative to zero. The inverting terminal of the μA709 is kept at +2V, to provide a high level output of 12V when the input to its non-inverting terminal is high (3.6V) and a low level output of -12V when the input is low (0.3V). The circuit of the binary level converter is shown in Figure 5.3.

5.1.5 RC Integrator

The modulator design depends basically on the time constant of the RC integrator and the minimum voltage necessary for stable operation of the comparator. The cut-off frequency f_0 should be chosen as small as possible for the greatest input dynamic range, although making it too small may cause instabilities in the comparator since the minimum voltage for stable operation of a μA709 comparator is about 5mV.

Using the equations derived in Chapter 3

$$Emin = 5mV$$

$$Emin = \frac{\Delta V}{2} = \frac{\pi V f_0}{f_c} \quad , \quad \text{where } f_0 = \frac{1}{2\pi T}$$

$$5\times10^{-3} = \frac{\pi V}{f_c} \cdot \frac{1}{2\pi T} \quad \text{gives}$$

$$T = 3.75\times10^{-2}s$$

$$T = RC = 3.75\times10^{-2}s$$

choosing $C = 4.7\mu F$ gives $R = 8k\Omega$ and

$$f_0 = \frac{1}{2\pi T} = 4Hz.$$

The nearest values for R and C are

$$R = 7.5k\Omega$$

$$C = 4.7\mu F$$

The complete Δ-Σ modulator with a single integrator is shown in Figure 5.4, with Figure 5.5 showing the theoretical characteristics, obtained using the equations for the overload level, threshold of coding and the quantisation noise.

5.2 DESIGN OF A DELTA-SIGMA MODULATOR WITH DOUBLE INTEGRATION

The block diagram of a Δ-Σ modulator with double integration is the same as that in Figure 5.1, except that a double integrator now replaces the single integrator. The design still depends on the choice of the cut-off frequencies of the double integrator, and the minimum voltage which can be applied to the comparator while still retaining stable operation. In Chapter 3 the characteristics frequencies were derived as,

$$f_1 = \frac{1}{2\pi R_1 C_1 (1 + C_2/C_1)} \tag{5.1}$$

$$f_2 = \frac{1}{2\pi R_2 C_2 \left[1 - \frac{1}{4}\left(1 + \frac{R_1}{R_2}\right)^2 \frac{R_2 C_2}{R_1 C_1}\right]} \tag{5.2}$$

$$f_3 = \frac{1}{2\pi_r C_2} \tag{5.3}$$

The minimum input voltage to the comparator is $5mV\left(=\frac{\Delta v}{2}\right)$, and using the equations in Section 3.2

$$5\times10^{-3} = \frac{16Vf_1f_2}{\pi f_c^{\,2}}$$

Substituting ±12 Volts for V, and 32kHz for f_c,

$$f_1f_2 = 85\times10^3$$

from which f_1 and f_2 were selected respectively as

$$f_1 = 100Hz \quad \text{and} \quad f_2 = 850Hz.$$

The characteristic frequency f_3 was assumed large compared with the highest signal frequency, which was taken as 1.5kHz, and therefore

$$f_3 = 24kHz \text{ was chosen.}$$

From equation (5.3) for f_3

$$rC_2 = 6.6\times10^{-6}s .$$

hence

$$r = 200\Omega \ , \ C_2 = 0.033\mu F.$$

Using equation (5.1) for f_1

$$100 = \frac{1}{2\pi R_1C_1(1+C_2/C_1)} \ ,$$

or

$$R_1(C_1+C_2) = \frac{1}{200\pi}$$

choosing R_1 as 1kΩ gives

$$C_1+C_2 = 1.6\mu F$$

so that $C_1 = 1.567\mu F$ is obtained.

By substituting the values obtained above for R_1, C_1, C_2 and f_2 in equation (5.2) for f_2, R_2 was found as (approximately) 6kΩ. Thus, summarising the results so far obtained

$f_1 = 100Hz$	$f_2 = 850Hz$	$fc = 24kHz$
$R_1 = 1k\Omega$	$R_2 = 6k\Omega$	$r = 200\Omega$
$C_1 = 1.567\mu F$	$C_2 = 0.033\mu F$	

The nearest standard values for the components of the double integration RC network are

$R_1 = 1k\Omega$ $\quad R_2 = 5.6k\Omega$ $\quad r = 280\Omega$

$C_1 = 1.5\mu F$ $\quad C_2 = 0.033\mu F$

and the complete Δ-Σ modulator circuit with a double integrator is shown in Figure 5.6. Figure 5.7 shows theoretical results for the overload level, together with the threshold of coding and the quantisation noise.

5.3 THEORETICAL ASSESSMENT OF THE TWO MODULATORS

It can be seen from Figures 5.5 and 5.7 that, although the overload level is the same for both forms of the Δ-Σ modulator, they differ in respect of the quantisation noise and the threshold of coding. In fact, the quantisation noise with double integration is about 20dB less than that with single integration.

Another advantage of using double integration in Δ-Σ modulation is the increased input dynamic range at high frequencies. With double integration, the threshold of coding is controlled by the two characteristic frequencies, so that the change in the threshold level is not felt until 100Hz. Although after this the threshold of coding rises with a slope steeper than with single integration, the input dynamic range is still greater.

Although the use of Δ-Σ modulators with double integrators promise improved results, further investigation of its characteristics also reveals disadvantages which are important when a speed control system is being considered.

5.4 EXPERIMENTAL TESTS ON THE TWO MODULATORS

In order to decide which Δ-Σ modulator is most suitable for speed-control purposes, a series of experiments was carried out on the two specially designed and constructed units.

5.4.1 Harmonic Content

For this test, an input signal at a given frequency was applied at the system input, and the output signal from the modulator was measured by wave analysers tuned to the signal frequency and to its 3rd-harmonic component. The signal amplitude was varied from the overload level to the threshold of coding and the procedure was repeated for various input frequencies.

Figures 5.8, 5.9, 5.10 and 5.11 show results for the Δ-Σ modulator with a single integrator, and it can be seen that as the input signal frequency increases the point on the fundamental at which the linearity of the system breaks down also increases (i.e. moves towards the overload level) thereby reducing the total linear range. The overload level can be seen by the increased harmonic distortion (i.e. the rapid increase in the 3rd-harmonic at overload level).

The 3rd-harmonic variation follows almost the same pattern throughout, becoming more pronounced as the lower limit of the linear range is neared. Furthermore, as the input signal frequency increases, the relative magnitude of the 3rd-harmonic also increases, which results in a reduced dynamic range. This effect is shown by consideration of a line 20dB below the fundamental, which cuts the harmonic curve closer and closer to the overload level as the input signal frequency increases.

Figures 5.12, 5.13, 5.14, 5.15 and 5.16 show the results of the same test for the Δ-Σ modulator with a double integrator. From careful consideration of these figures the same general conclusions obtained above can again be reached.

On comparing the results for single and double integration, it is seen that a much greater linear range is achieved in the latter case. Thus, in Figure 5.11, the lower limit of the linear range is at -14dB relative to 1, whereas in Figure 5.16 it is at -18.5dB, an improvement of 4.5dB. Figure 5.17 shows the lower limit of the linear range plotted against the input signal

frequency.

Further comparison of the two sets of results shows that the level of harmonics is higher when double integration is used. This can be explained by the complexity of the double integrator, since the threshold of coding is related to the transfer function of the integrating network. Thus the 20dB-below-fundamental line cuts the harmonics at -8.5dB relative to 1 in Figure 5.11 and at +2.5dB in Figure 5.16, a difference of 11dB.

5.4.2 Quantisation Noise

To measure the quantisation noise, the difference circuit shown in Figure 5.18 was used. The output of this circuit is

$$V_0 = V_2 - V_1$$

where the two inputs V_1 and V_2 are taken from the two comparator inputs. The output of the difference circuit, which is the quantisation noise, was measured by varying the clock frequency, input signal frequency and input signal level. Figure 5.19 shows the variation of the quantisation noise of the Δ-Σ modulator with single integration (measured with a r.m.s. voltmeter), with the clock frequency. As can be seen, the quantisation noise decreases with increasing clock frequency, and the amount of the decrease as the clock frequency varies from 10kHz and 50kHz is more than the decrease in the quantisation noise as the clock frequency varies between 50kHz and 90kHz. Throughout this test the input signal frequency was 1kHz and the input signal level (amplifier output) was kept at 6V r.m.s.

The variation of the quantisation noise with the input signal frequency is shown in Figure 5.20. As will be seen, the quantisation noise does not vary with the input signal frequency, provided that the clock frequency and the input signal level are kept constant.

5.4.3 Discussion

Comparison of the performance of the two modulators shows that, although the overload level for both is the same and is dependent only on the digital levels ±V, the threshold of coding and hence the input dynamic range is different.

Δ-Σ modulation with double integration provides a lower threshold of coding and hence a greater linear range. The input dynamic range with single integration is proportional to the clock frequency, whereas with double integration it is proportional to the square of the clock frequency. Thus, at high clock frequencies, the latter gives a greater linear range. However, in a speed-control system, the bandwidth of the input signal (50Hz for a speed change corresponding to a frequency change from 0 to 50Hz) is not very large, and since the highest frequency to be modulated is not greater than 100Hz, this feature is of little value as long as the clock frequency is high and good encoding is ensured. The clock frequency will be limited only by the maximum switching frequency of the inverter used to amplify the modulated signal for feeding to the motor.

From the quantisation noise point of view, Δ-Σ modulation with double integration gives better results (see Figures 5.5 and 5.7). As Figures 5.19 and 5.20 show, the quantisation noise falls with increasing clock frequency and increases with the level of the input signal, but does not vary with the input signal frequency. The experimental results show that the level of the quantisation noise is very low, and for speed control purposes this will have negligible effect on the choice of the modulator.

Figures 5.8, 5.9, 5.10 and 5.11 for single integration and Figures 5.12, 5.13, 5.14, 5.15 and 5.16 for double integration show that the harmonic levels are higher for a double-integration modulator. Although the experimental results favour the use of Δ-Σ modulation with double integration in a signal processing system, since this gives a greater linear range, the higher harmonics level may limit its use. If, by some means, the

modulation technique to be used reduces the effect of the harmonics, it is preferable to use double integration, but if there is no means of reducing the harmonics level Δ-Σ modulation with single integration is better.

Furthermore, Δ-Σ modulators with double integration tend to exhibit undesirable oscillatory properties. Reducing the frequency of the input signal or including some damping element in the feedback loop prevents this. In speed control applications, the level of the harmonics is a major parameter affecting the performance of the motor. To reduce the losses, the level of harmonics should be made as small as possible.

For all the reasons stated above, it is better to use Δ-Σ modulation with only single integration in a speed-control application, and it was therefore decided to proceed with the project on this basis.

5.5 BISTABLE DELTA SIGMA MODULATOR

In section 5.1 a design was given for a Δ-Σ modulator with a single integrator, in which the bandwidth of the input signal was assumed to be 0 to 1.5kHz and the clock frequency was chosen as 32kHz.

The bandwidth of the input signal (i.e. the frequency range the input signal has to cover) depends on the required speed range of the motor, and a rule of thumb for good encoding is that the clock frequency must be at least twenty times the input signal frequency. This fixes a minimum of 1kHz for the clock frequency of a system with an input frequency bandwidth of 50Hz. The upper limit for the clock frequency is determined by the rate at which the inverter can be switched without incurring excessive switching losses.

Taking the above details into account, and noting that, as shown in Chapter 3, a single unit can replace the integrators in the feedback and forward paths, a simpler Δ-Σ modulator can be designed. The input amplifier in Figure 5.2 is not now needed, and the output of the D type flip-flop is used directly to integrate the output of the modulator, without the binary level converter shown in the block diagram of Figure 5.21.

Since the output of the D type flip-flop is stable at either +V or at zero volts, the quantiser must be changed so as to have a threshold level. This should be variable so that it can be adjusted for best encoding. Noting that from Figure 5.21,

$$\varepsilon = i(t) + \overline{Q(t)}$$

it follows that by correct design, and with ε made small, $\overline{Q(t)}$ is almost equal to $i(t)$. All the decoder is then required to do is to remove the high-frequency components not present in the original signal $i(t)$, which means that a simple filter will suffice.

The complete circuit diagram of the bistable Δ-Σ modulator is shown in Figure 5.22, where the potentiometer at the non-inverting input of the operational amplifier μA709 sets the variable threshold level. The modulator is set for best encoding by shortcircuiting the input terminal of the modulator and adjusting the potentiometer until the output is a series of pulses at half the clock frequency, i.e. the modulator is in the idling mode.

The comparator is a simple addition circuit instead of a subtractor since the inverse output $\overline{Q(t)}$ is used.

5.5.1 Clock Pulse Generator

The clock pulse signal generator used with the Δ-Σ modulator is shown in Figure 5.23. Operation is very simple, with IC1 acting as an integrator and IC2 as a level detector. Potentiometer VR1 adjusts the rate at which capacitor C1 charges and the frequency of the pulse generator is adjusted between 2kHz and 10kHz.

5.5.2 Performance of the Modulator

The photographs of Figure 5.24 illustrate operation of the modulator when idling. The clock frequency is 5kHz and the output shown in Figure 5.24.a can be seen to be of a frequency of one half this. Figure 5.24.b

shows the output of the modulator and the integrated difference.

The photographs of Figure 5.25.a and .b show the input, the output and their integrated difference, for an input frequency of 25Hz and a clock rate of 1.5Hz. Figure 5.26.a and .b show the same details when the clock rate is 10.358kHz. It can be seen clearly that the encoding is a lot better at a higher clock rate, and that the integrated input/output difference has been very much reduced.

The photographs of Figures 5.27 and 5.28 show the same details where the input frequency is 50Hz, and the amplitude of the input sine wave has been increased to illustrate the effect of overloading. Considerations of Figure 5.27.b and Figure 5.28.b indicate that for a lower clock frequency the effect of loading is much more evident.

5.5.3 Synchronisation of the Clock Signal to the Input Signal

Since the sine wave input to the Δ-Σ modulator is not synchronised to the square wave clock signal, the modulator output will be subject to jitter. For high clock frequencies, the effect is negligible, but for low frequencies it may affect the quality of the modulator output as mentioned in section 2.2.3. The system shown in Figure 5.29, consisting of a phase measuring unit, a low pulse filter, an amplifier, a voltage controlled oscillator and a divider was designed to remove any jitter. The P.M.U. (phase measuring unit) produces an error signal proportional to the phase difference between the input and the output of the divider, and the signal is passed through the low-pass filter and the amplifier to correct the frequency of the voltage controlled oscillator. In this way the input signal and the divider output are locked, and the frequency of the output of $n \times f_{input}$ can be used as the clock signal for the Δ-Σ modulator.

Figure 5.30 shows the phase measuring unit, low pass filter and the amplifier, with the signal from the divider entering at B and the input at A. The phase measuring unit is a flip-flop, with its operation depending on

the fact that when the frequency at A exceeds that at B the average collector voltage of T2 is positive, and when the frequency at A is less than that at B this voltage is negative. In either case, the error voltage tends to maintain the collector of T2 at an average voltage of zero, as explained in Figure 5.31.

The pulse signal appearing at the collector of T2 is filtered by a resistor capacitor, combination and the resulting d.c. voltage is applied to the base of transistor T3. This transistor, in an emitter follower connection, acts to provide a d.c. shift, and the error voltage of the output is used to correct the oscillator frequency.

The circuit of the voltage controlled oscillator is shown in Figure 5.32, with the design details given in Chapter 6. The divider comprises two decade counters SN7490 as shown in Figure 5.33.

The overall system functions satisfactorily over a range of input frequency from 10Hz to 70Hz. Since the division is by a factor of 100, the corresponding range of output frequency from the voltage controlled oscillator is from 1kHz to 7kHz. This output signal is used as the clock signal for the Δ-Σ modulator.

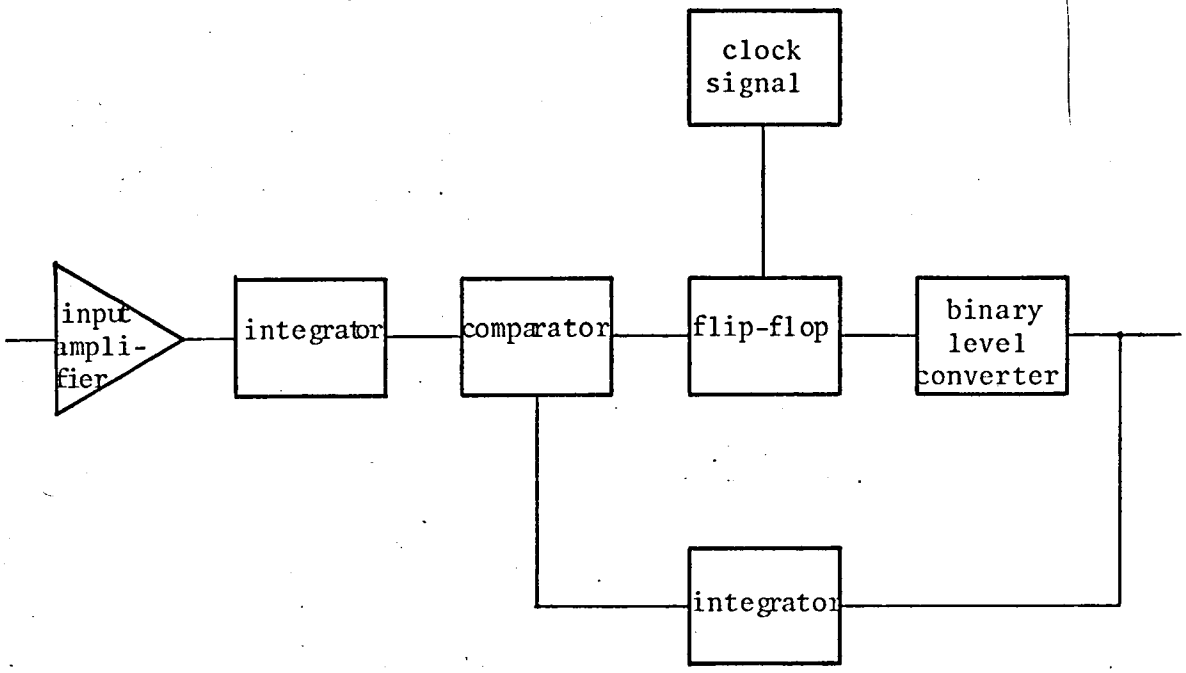


Figure 5.1: BLOCK DIAGRAM OF A Δ-Σ MODULATOR

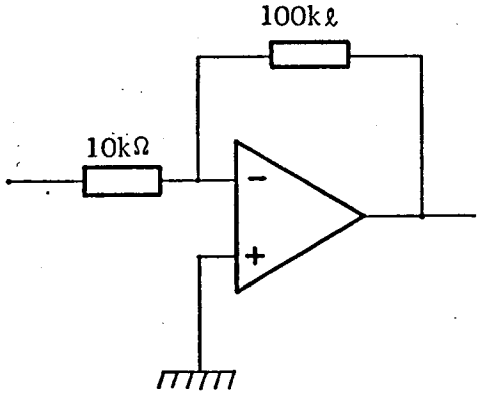


Figure 5.2: INPUT AMPLIFIER

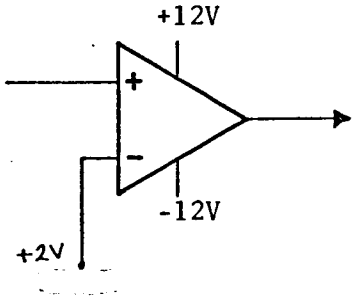


Figure 5.3: BINARY LEVEL CONVERTER

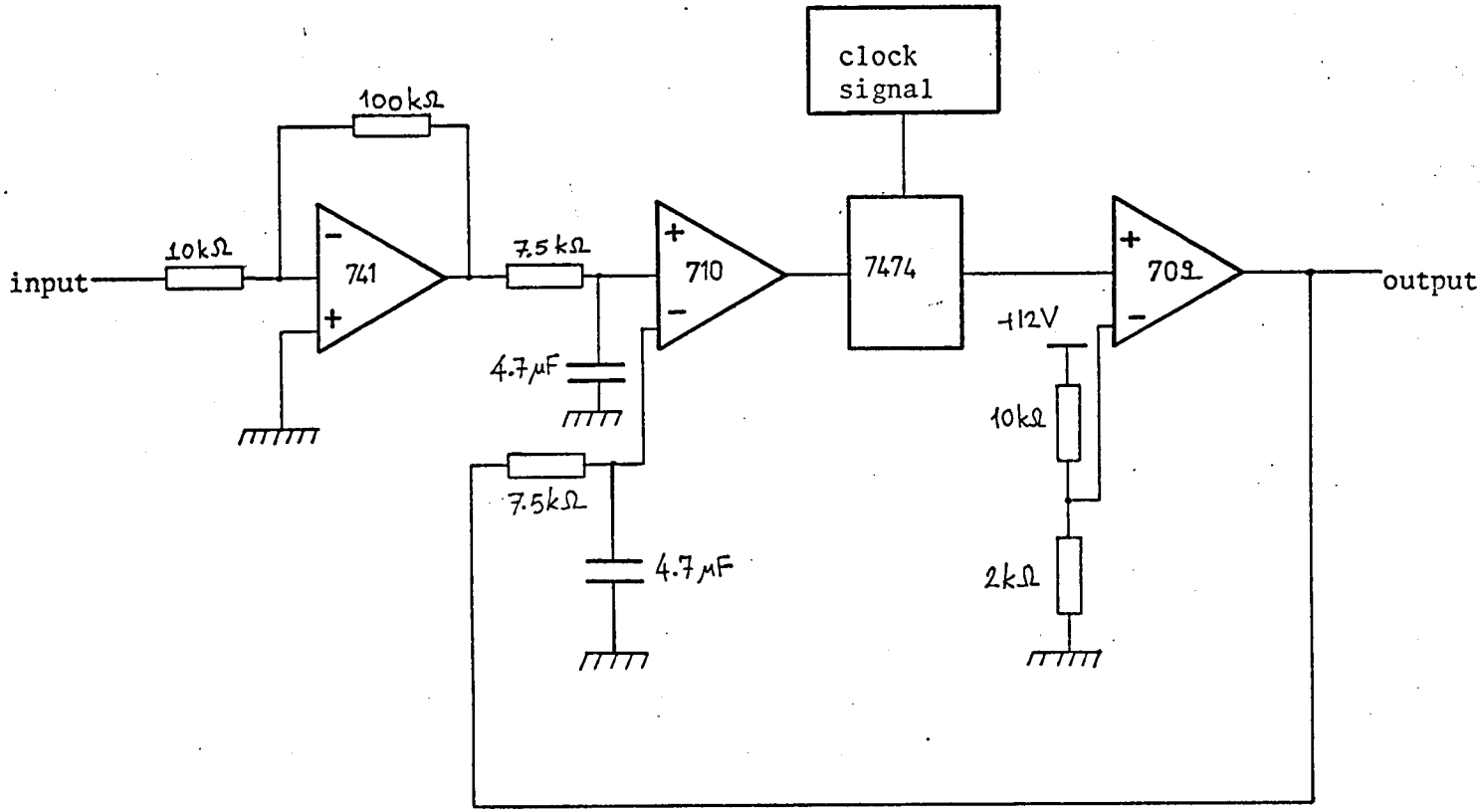


Figure 5.4: DESIGNED Δ-Σ MODULATOR WITH A SINGLE INTEGRATOR

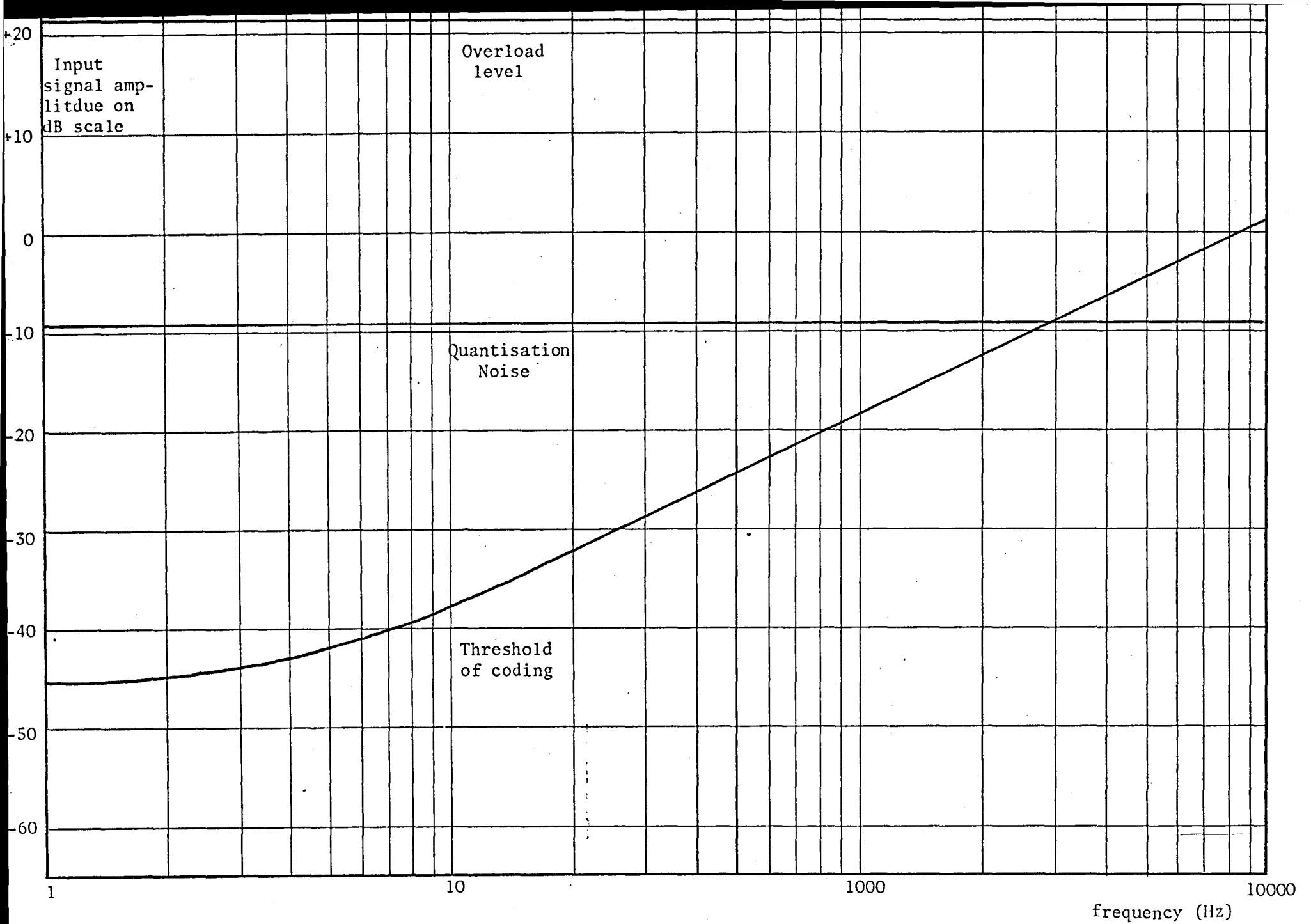


Figure 5.5: CHARACTERISTICS OF Δ-Σ MODULATION WITH SINGLE INTEGRATION

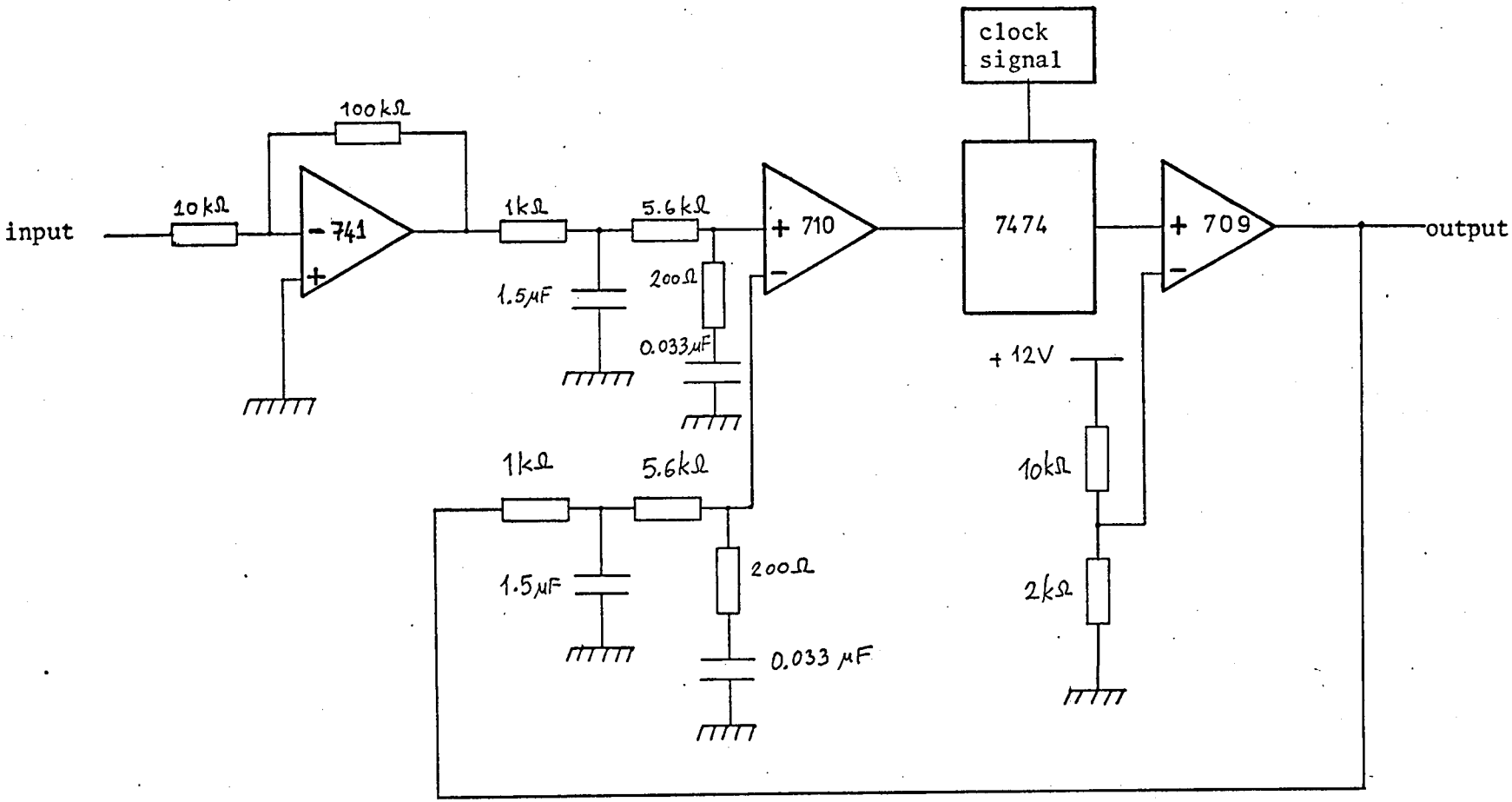


Figure 5.6: DESIGNED Δ-Σ MODULATOR WITH A DOUBLE INTEGRATOR

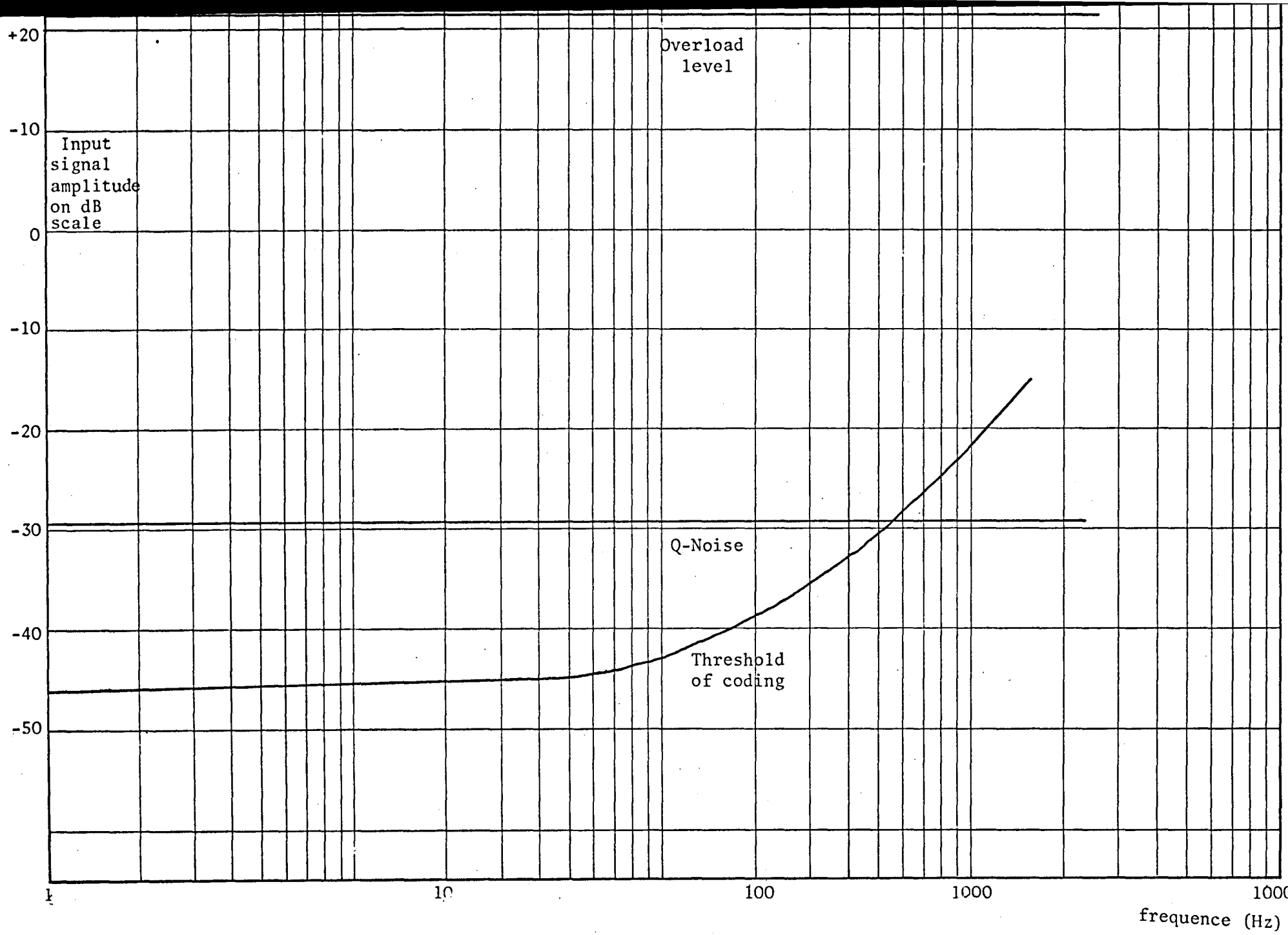


Figure 5.7: CHARACTERISTICS OF Δ-Σ MODULATION WITH DOUBLE INTEGRATION

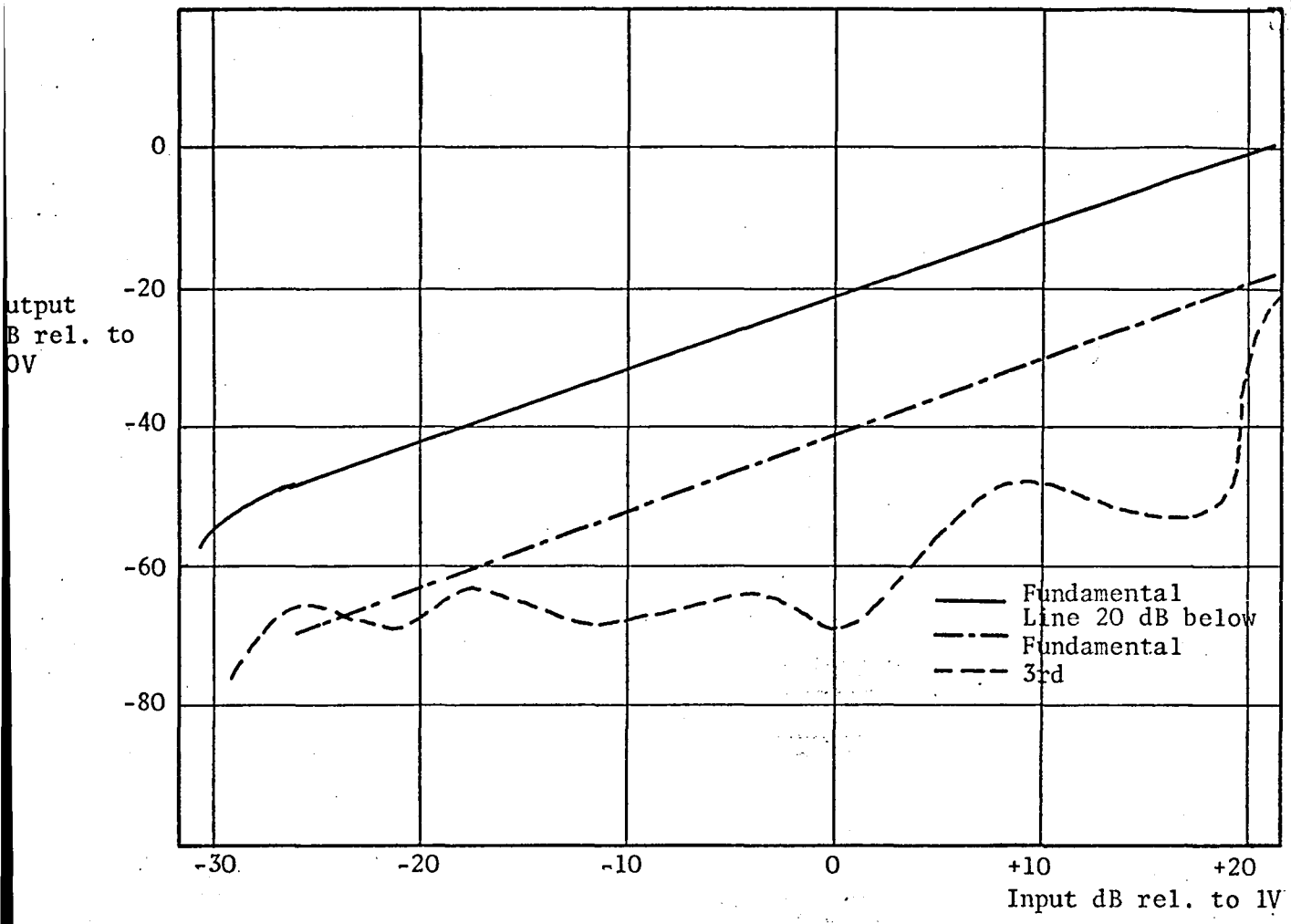


Figure 5.8: SINLGE INTEGRATION, f_{in} = 100 Hz, f_c = 32 kHz

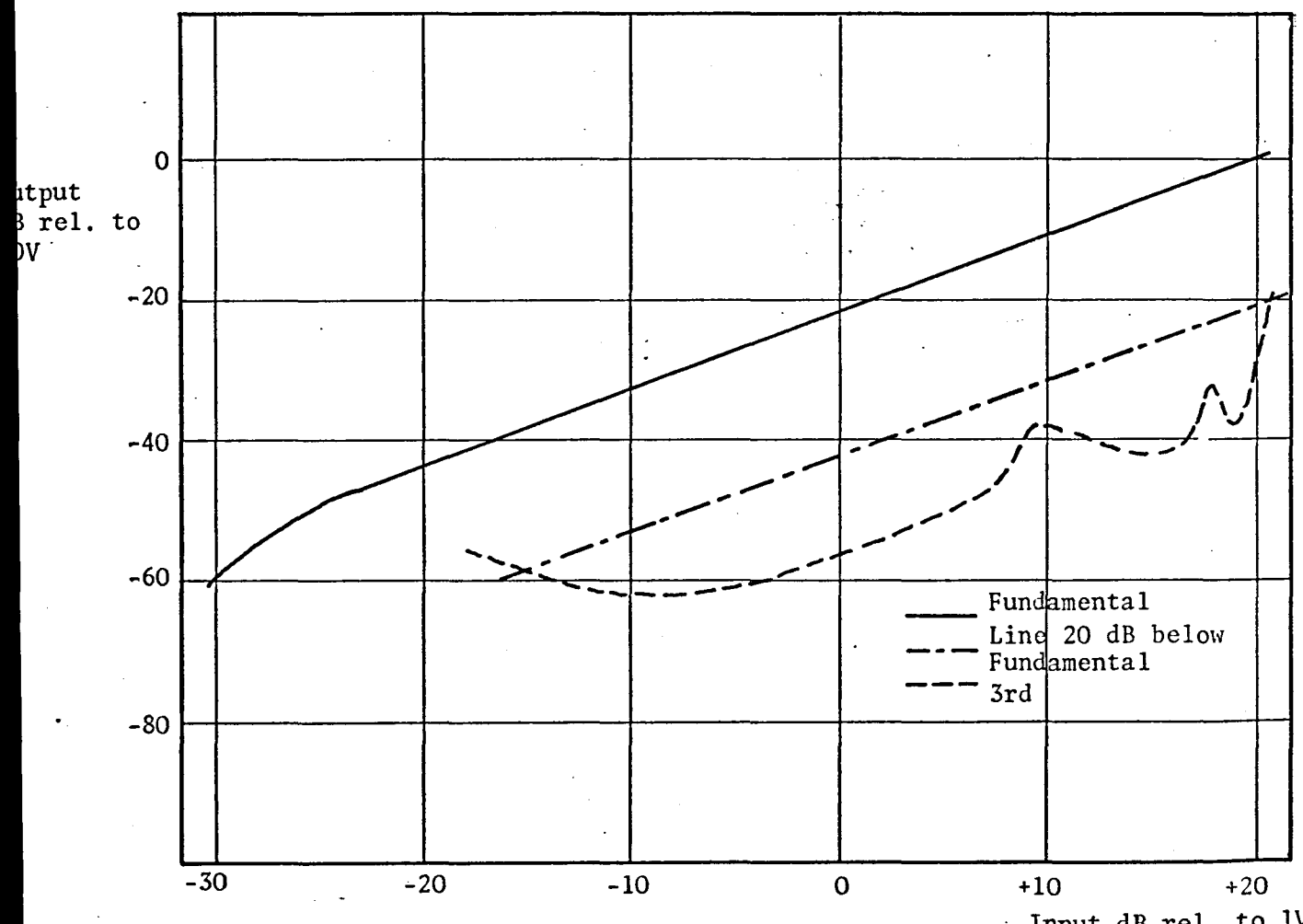


Figure 5.9: SINLGE INTEGRATION, fin = 400 Hz, fc= 32 kHz

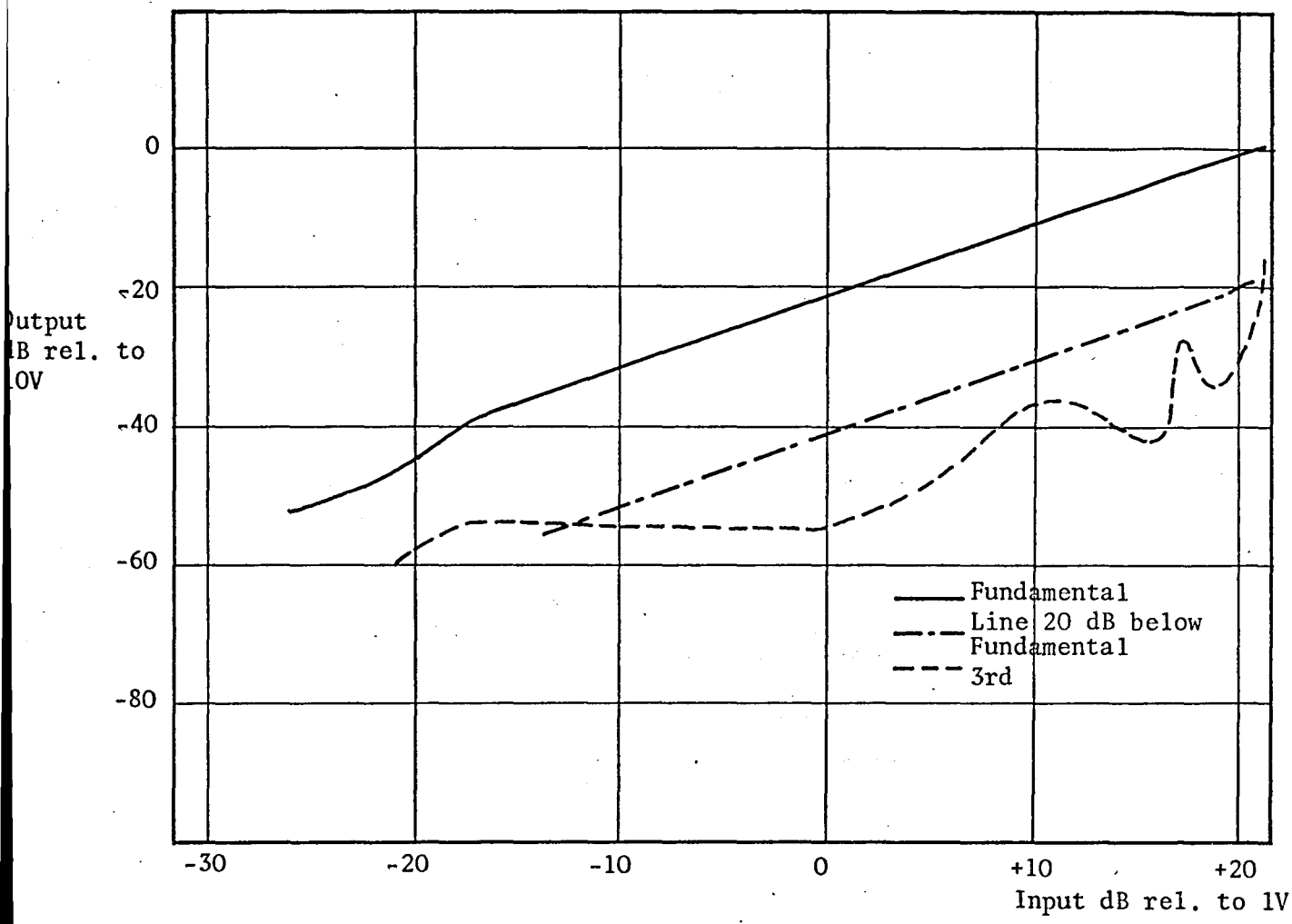


Figure 5.10: SINLGE INTEGRATION, fin = 800 Hz, fc = 32 kHz

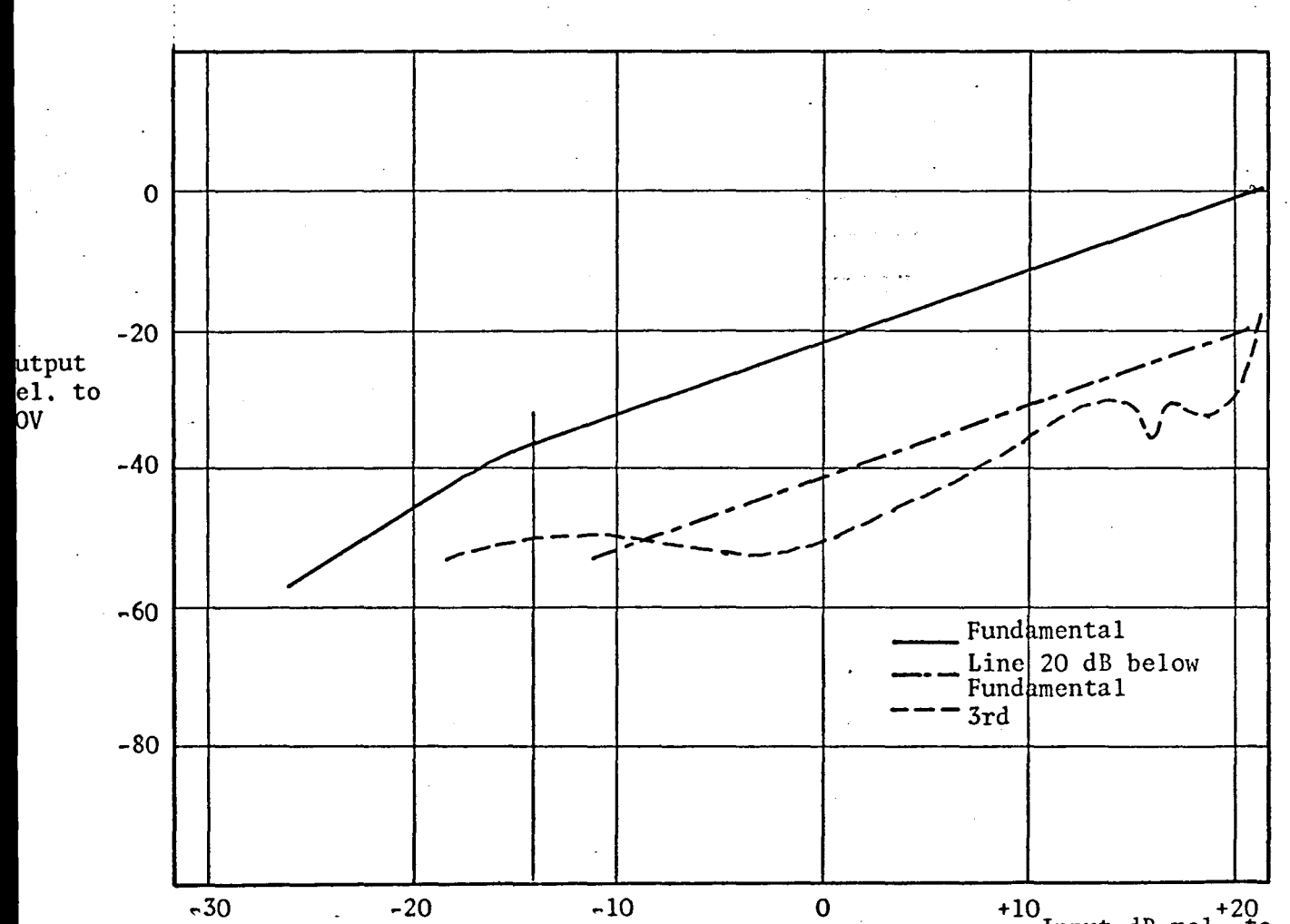


Figure 5.11: SINGLE INTEGRATION, fin = 1000 Hz, fc = 32 kHz

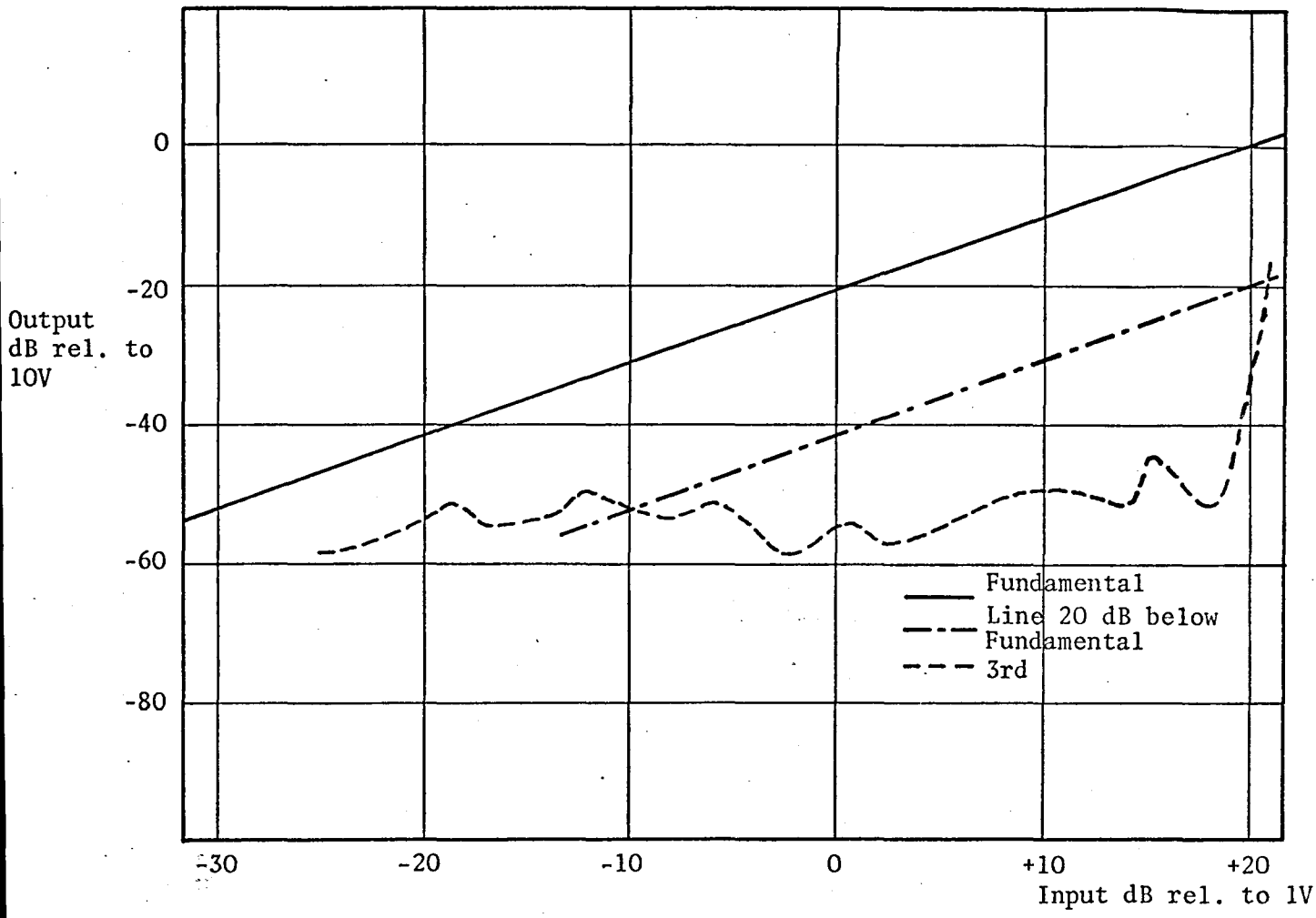


Figure 5.12: DOUBLE INTEGRATION, fin = 150 Hz, fc = 32 kHz

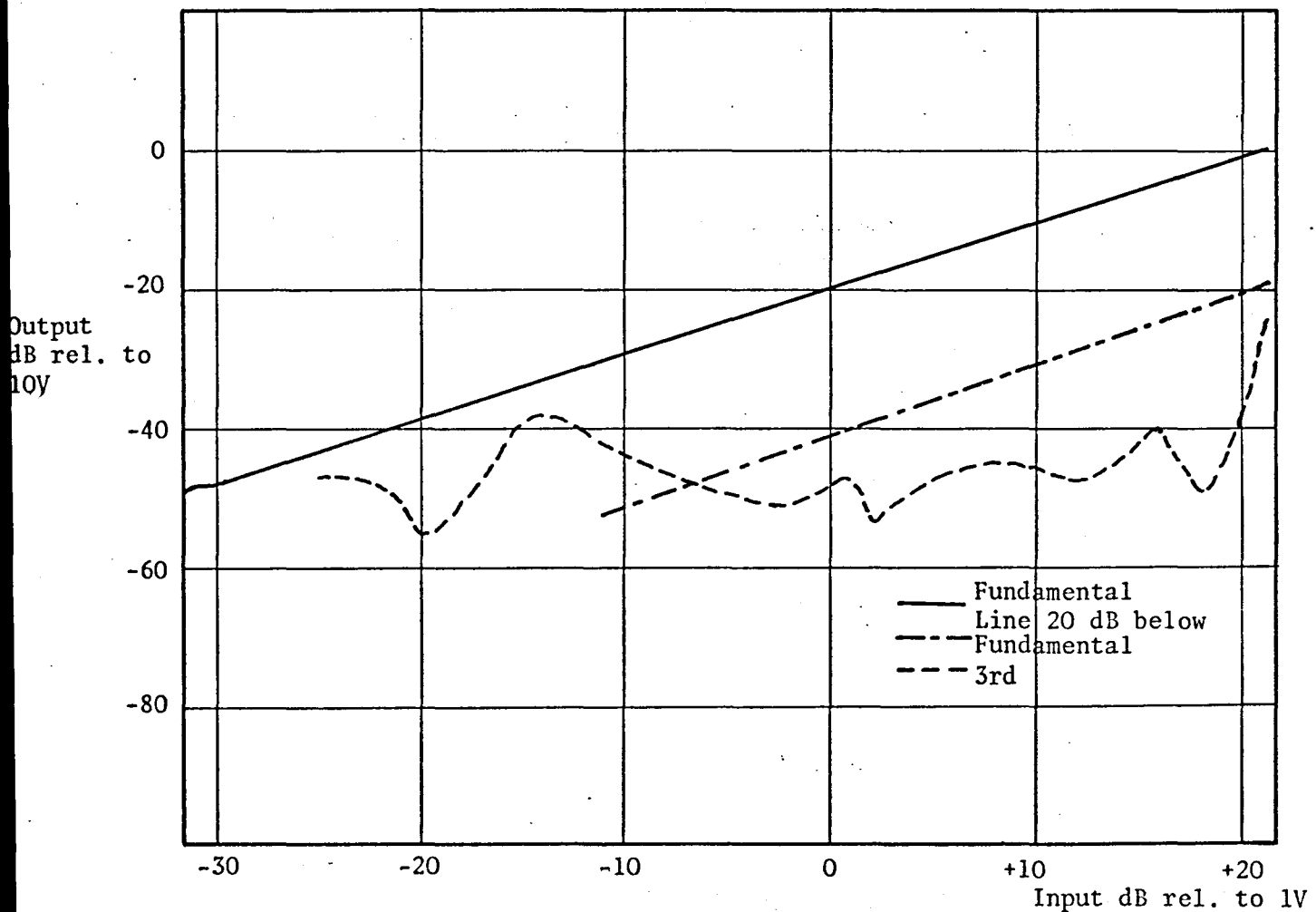


Figure 5.13: DOUBLE INTEGRATION, fin = 500 Hz, fc = 32 kHz

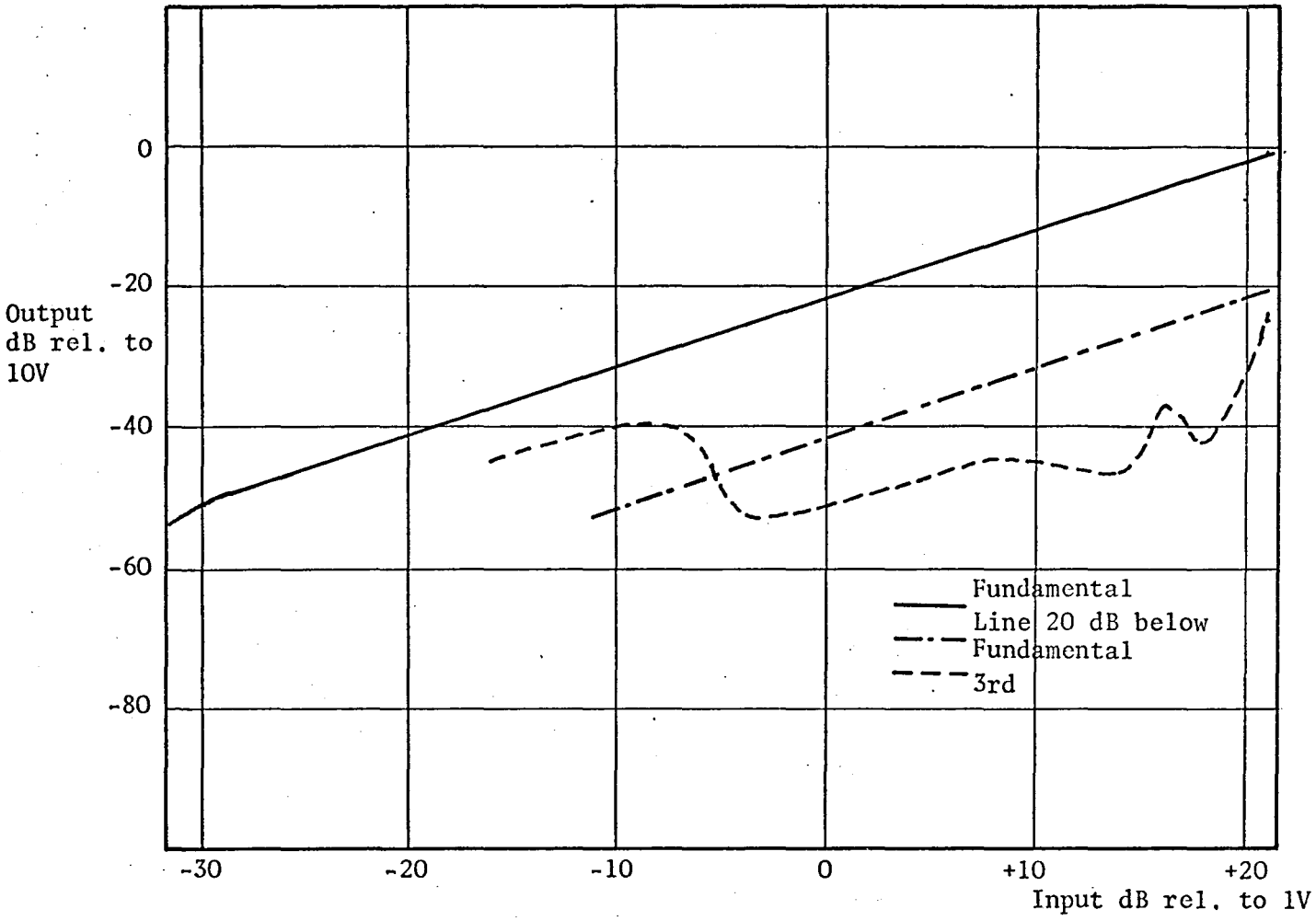


Figure 5.14: DOUBLE INTEGRATION, fin = 500 Hz, fc = 32 kHz

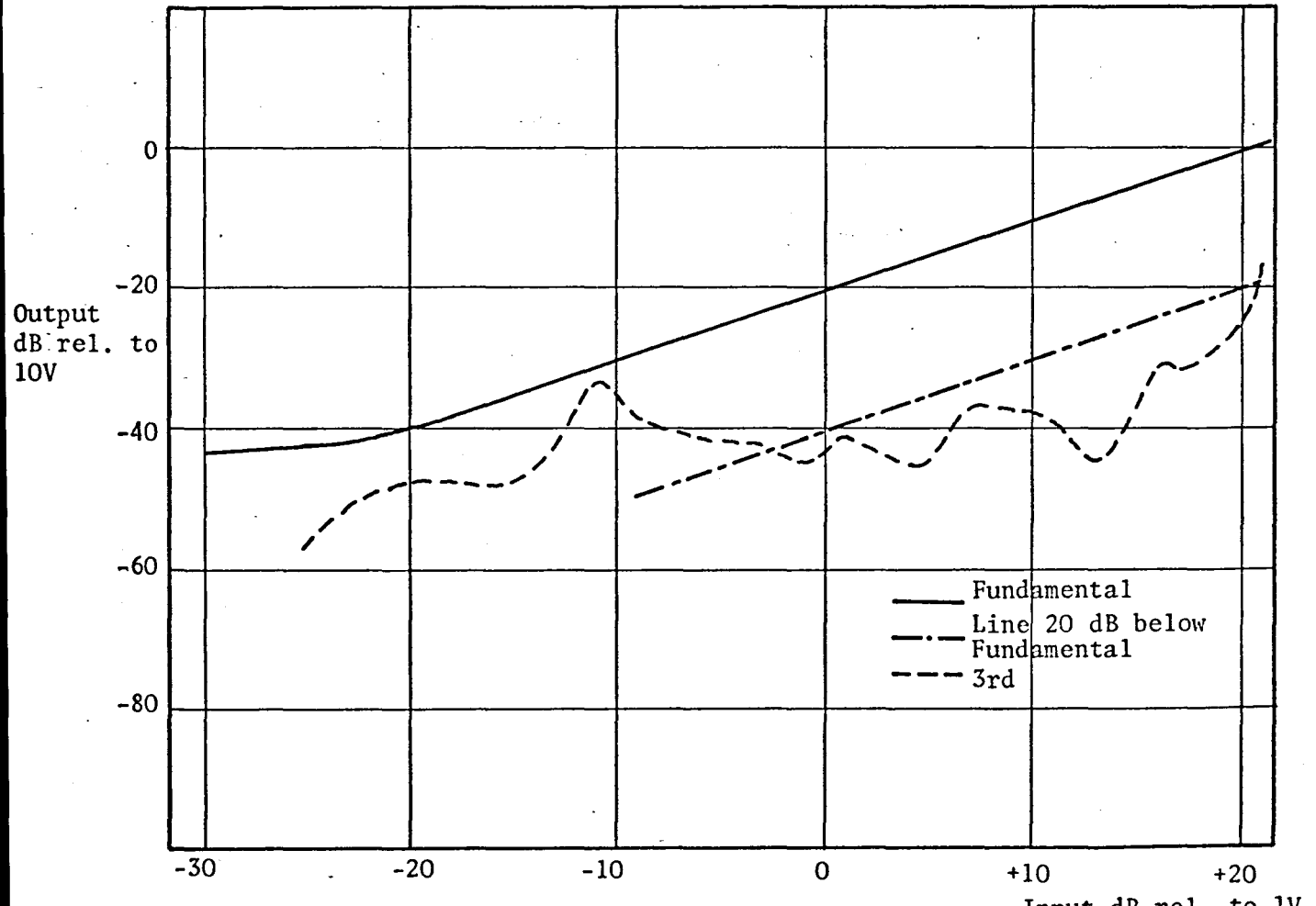


Figure 5.15: DOUBLE INTEGRATION, fin = 700 Hz, fc = 32 kHz

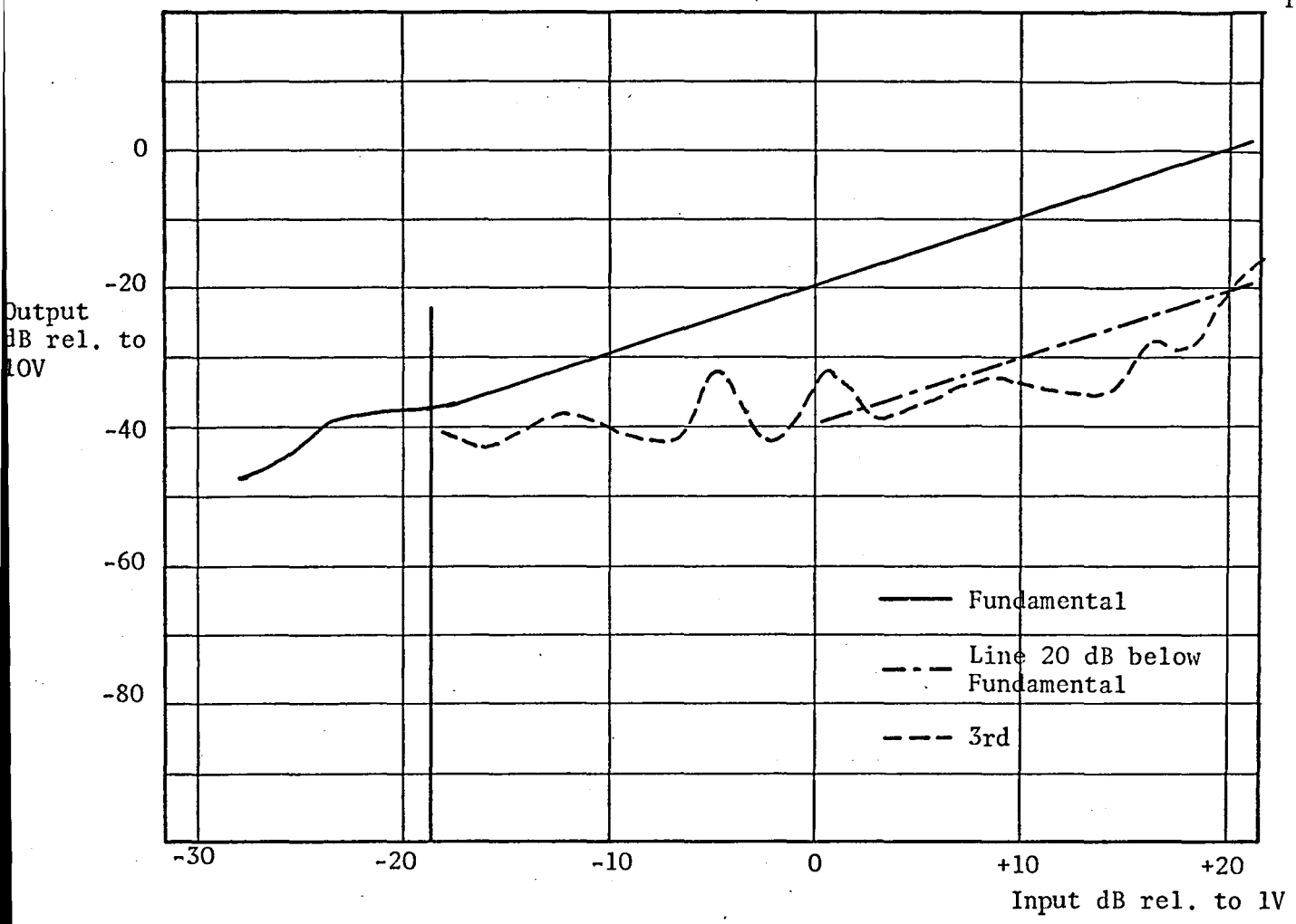


Figure 5.16: DOUBLE INTEGRATION, f_{in} = 1000 Hz, f_c = 32 kHz

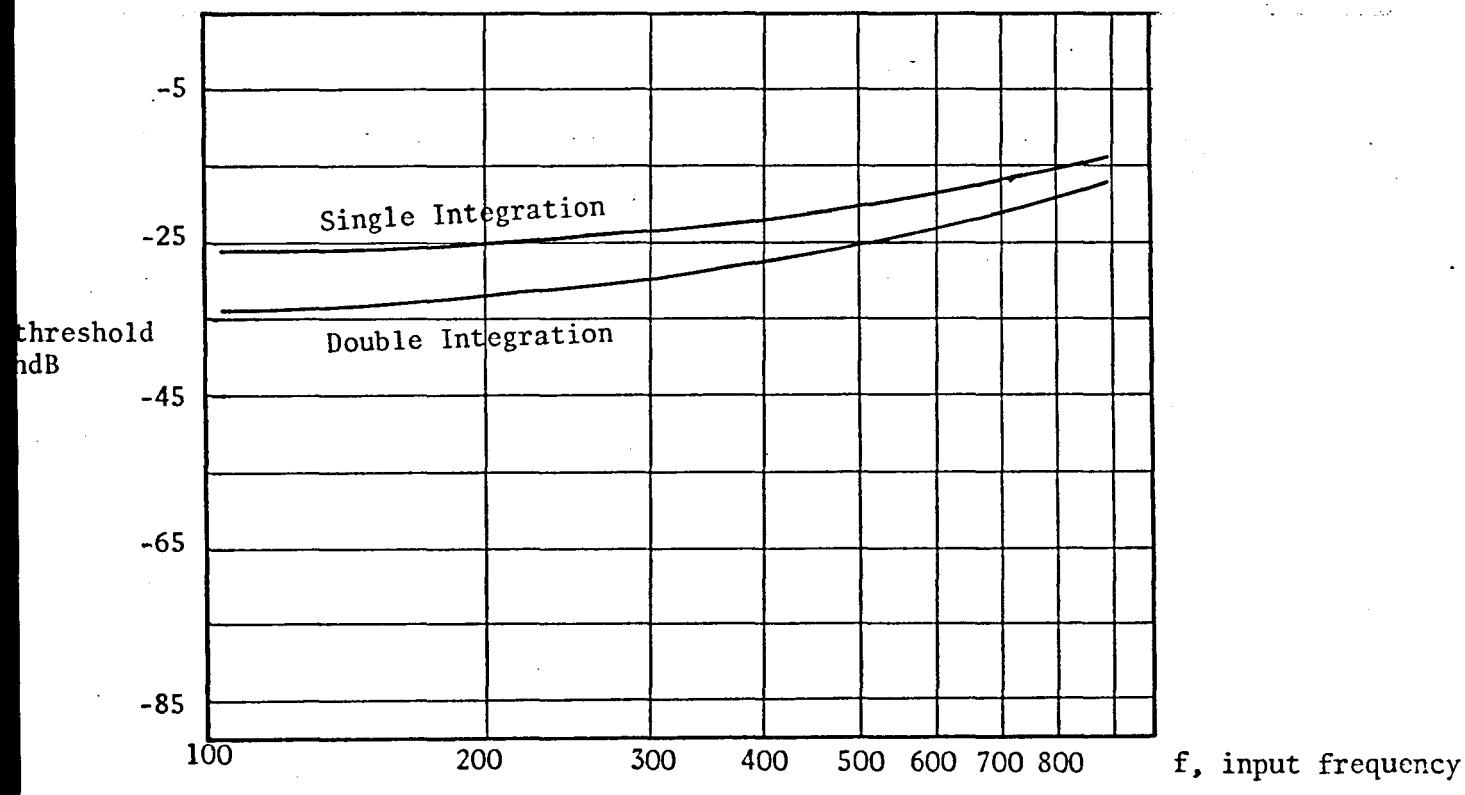


Figure 5.17: VARIATION OF LOWER LIMIT OF LINEAR RANGE, WITH INPUT SIGNAL FREQUENCY

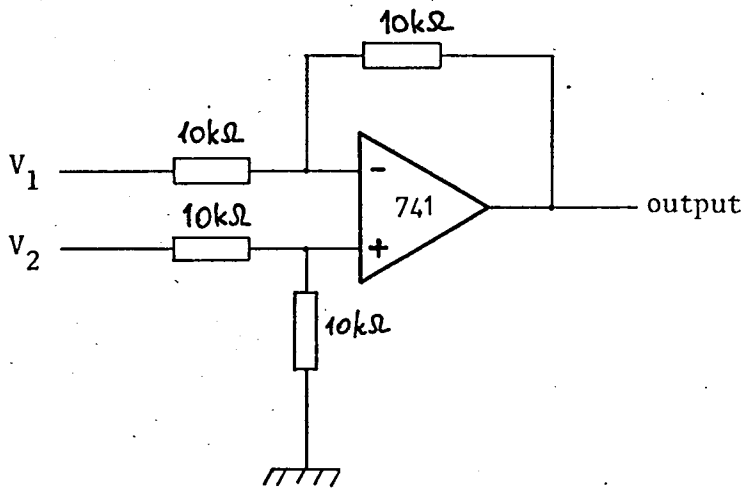


Figure 5.18: DIFFERENCE CIRCUIT TO INVESTIGATE Q-NOISE

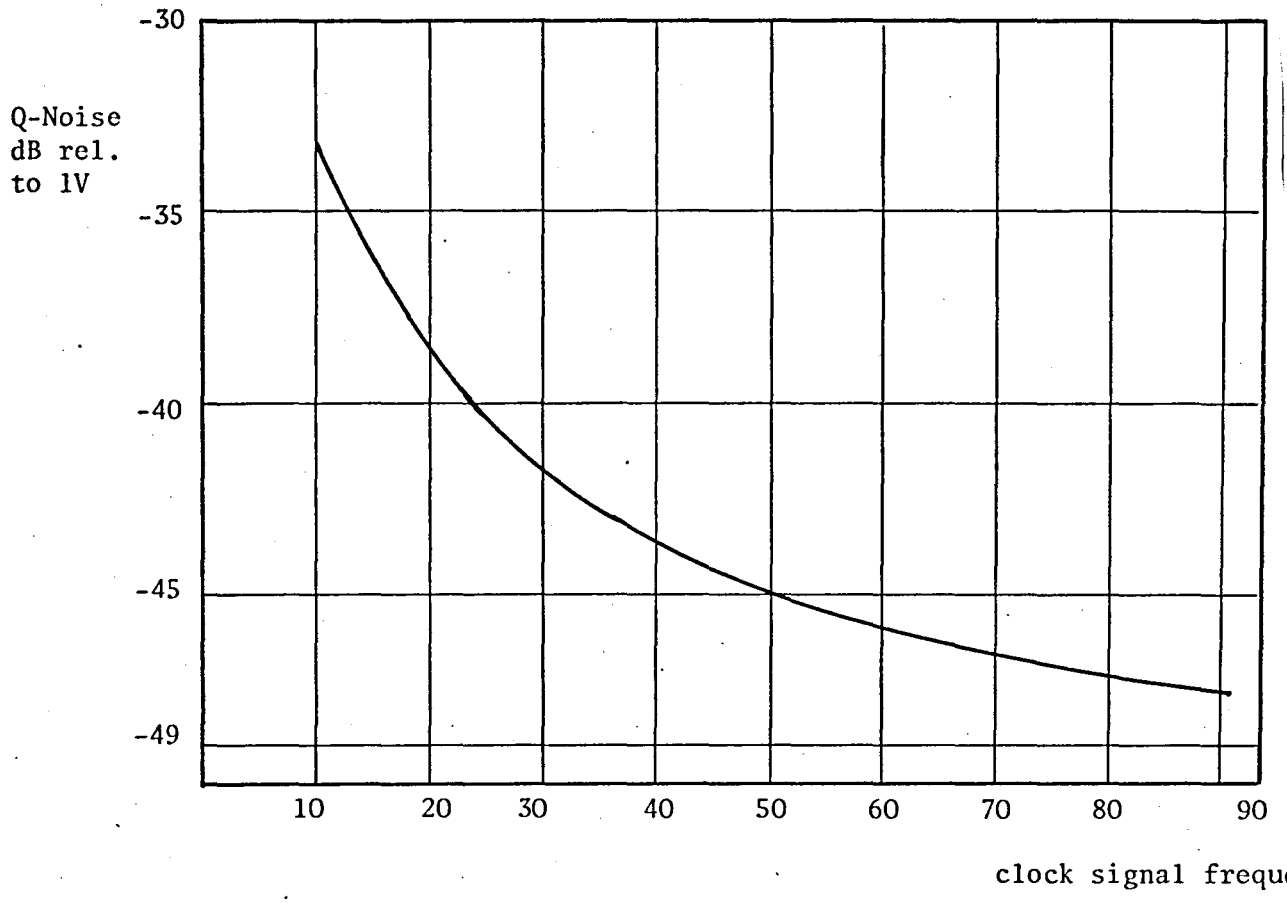


Figure 5.19: VARIATION OF Q-NOISE WITH CLOCK FREQUENCY
fin=100Hz, amplifier output=6V rms

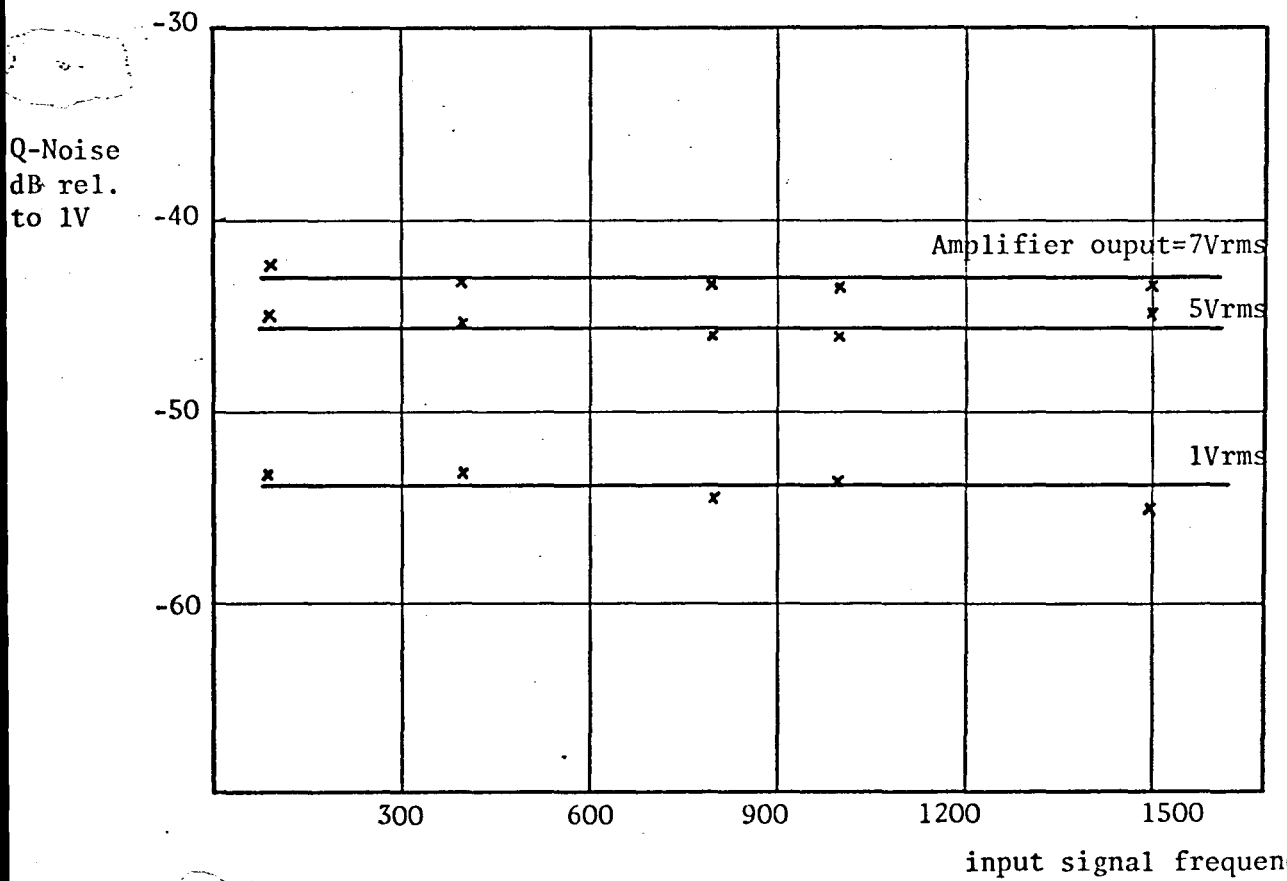


Figure 5.20: VARIATION OF Q-NOISE WITH INPUT SIGNAL FREQUENCY

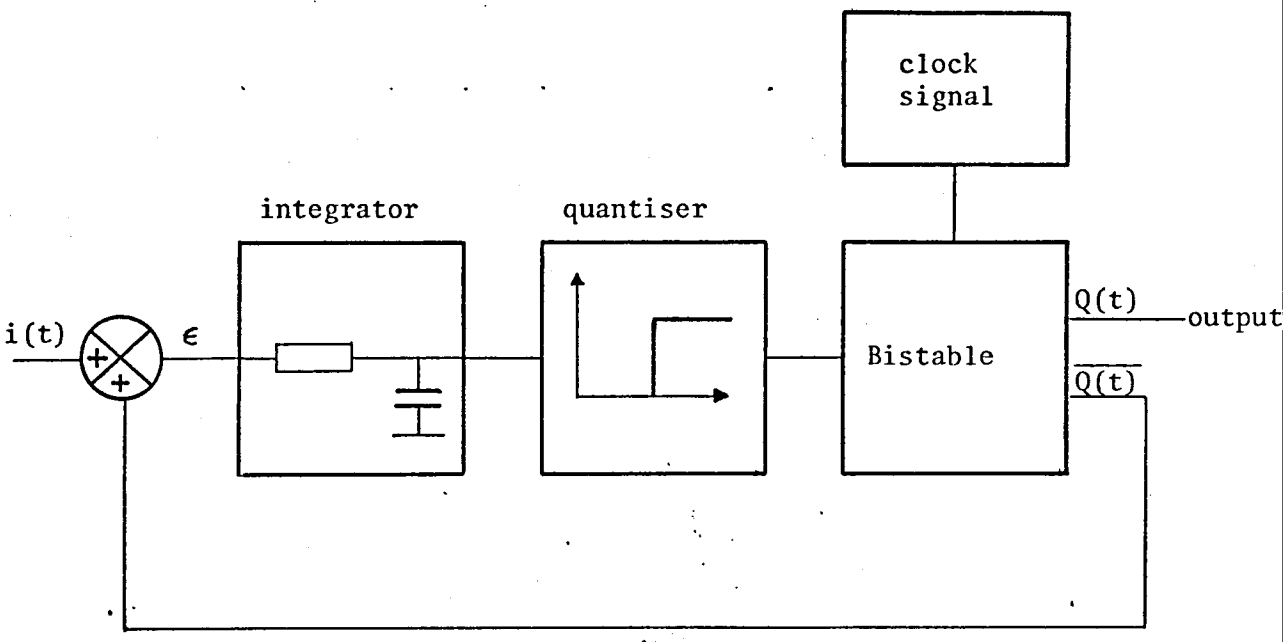


Figure 5.21: BLOCK DIAGRAM OF BISTABLE Δ-Σ MODULATOR

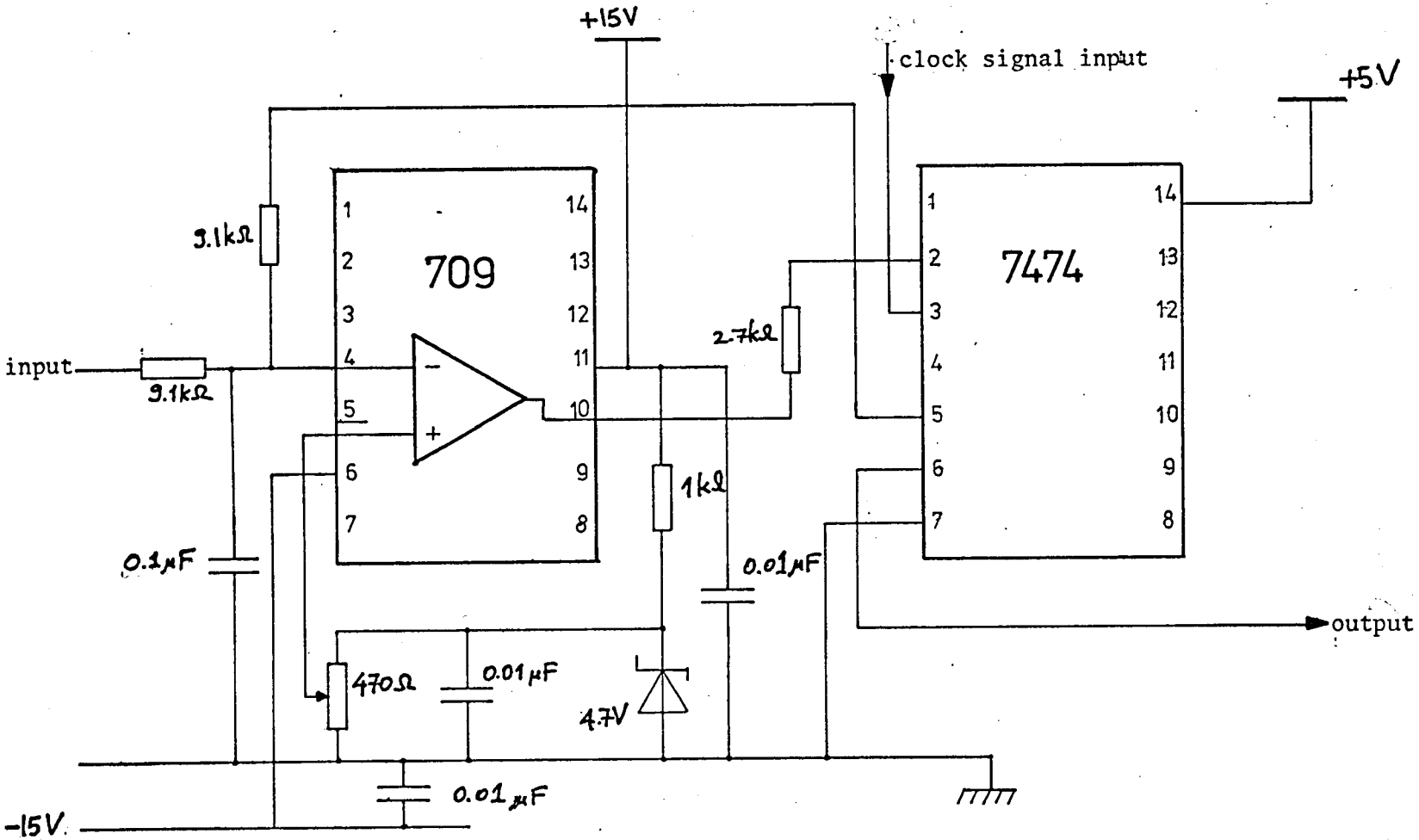


Figure 5.22: CIRCUIT DIAGRAM OF BISTABLE Δ-Σ MODULATOR

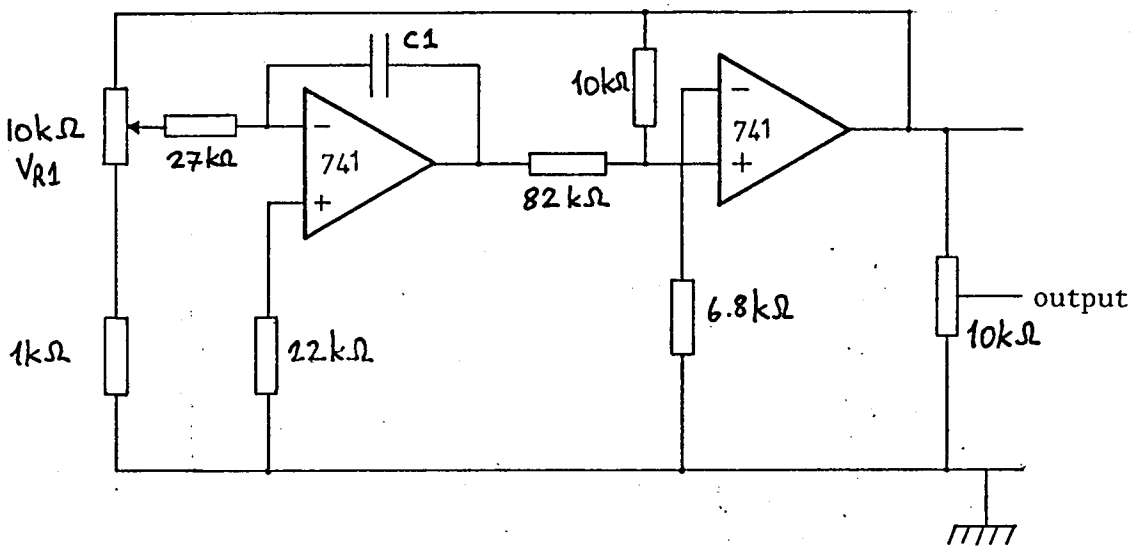
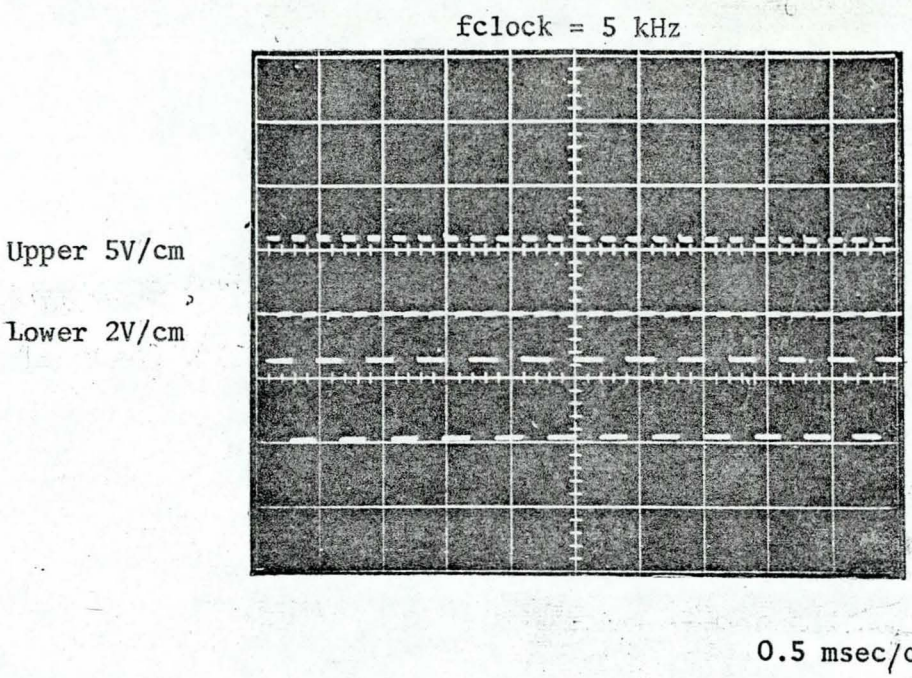
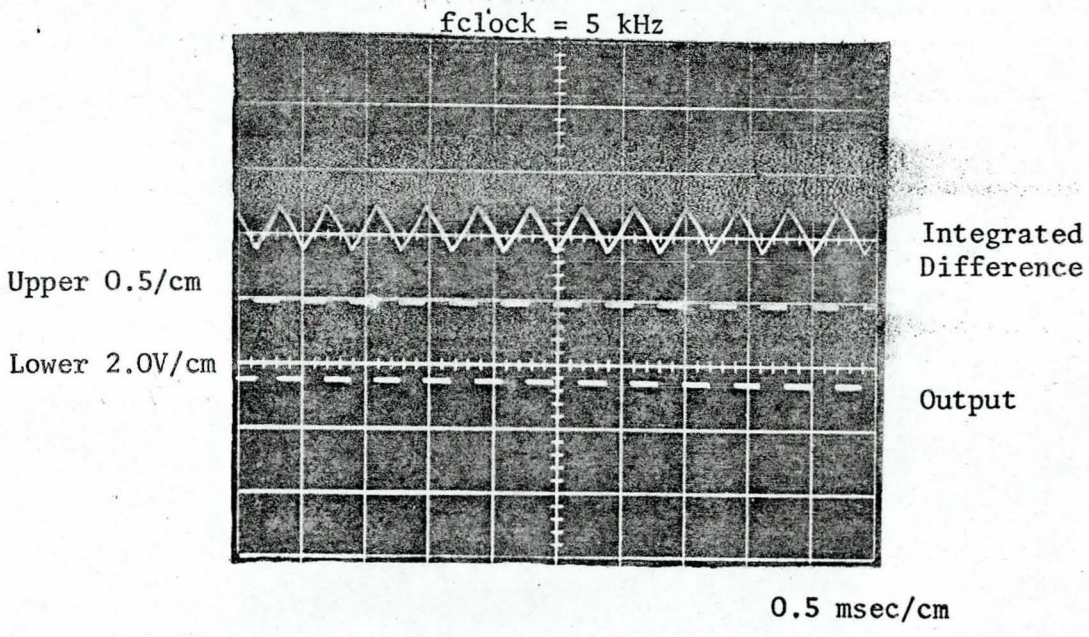


Figure 5.23: CLOCK SIGNAL GENERATOR

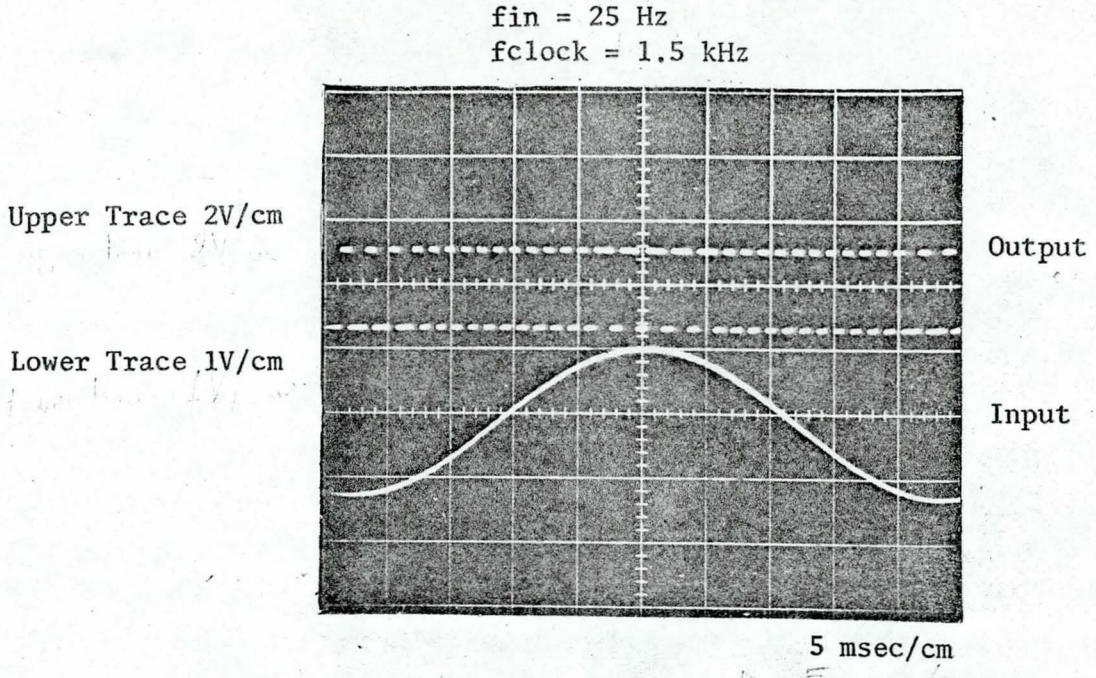


(a) Clock Signal Input and Output of Δ-Σ Modulator

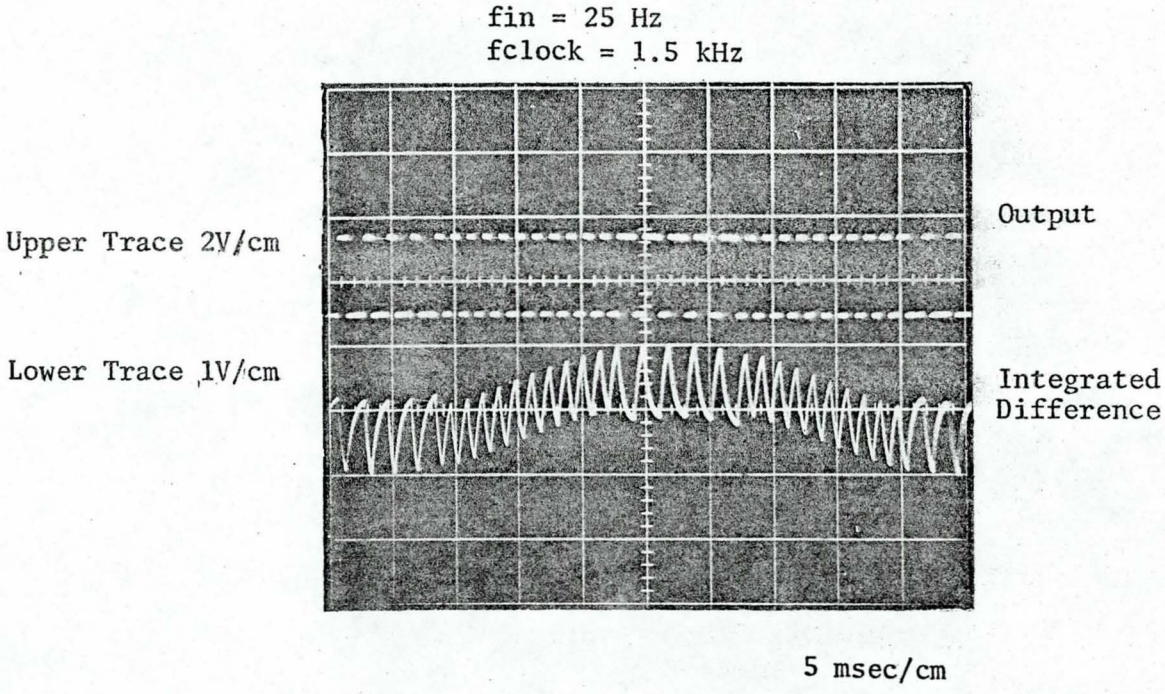


(b) The Integrated Difference and Output of Δ-Σ Modulator

Figure 5.24: THE IDLING PATTERN OF Δ-Σ MODULATOR

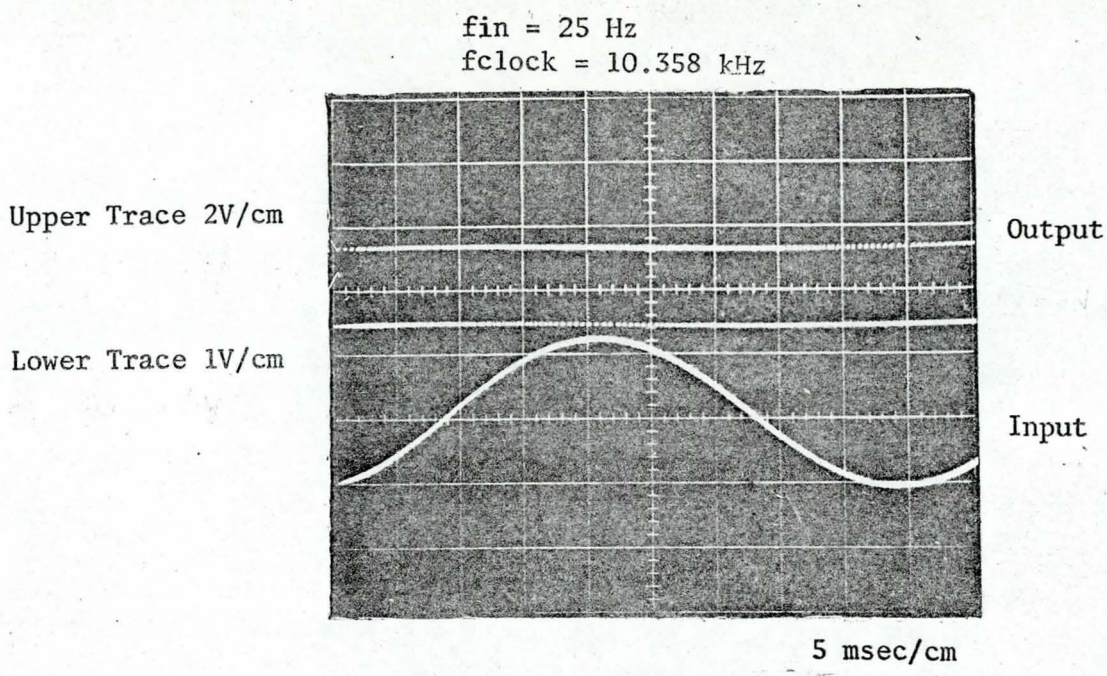


(a) The Input and Output Waveforms

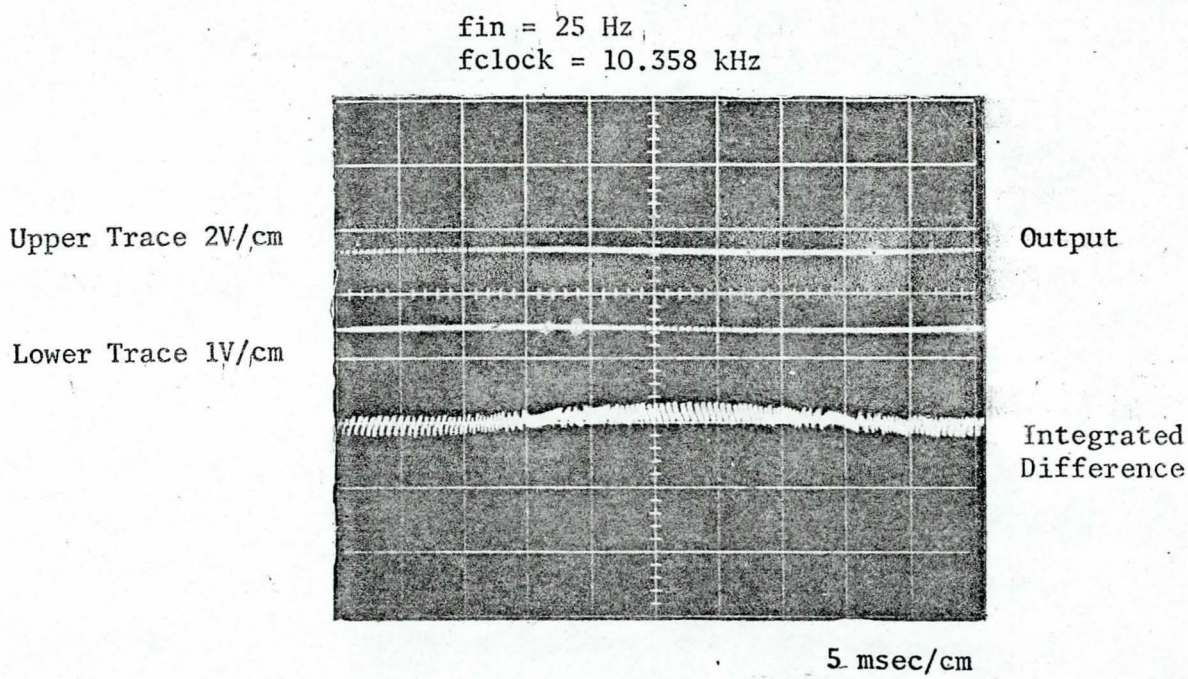


(b) The Output and the Integrated Difference

Figure 5.25: WAVEFORMS OF Δ-Σ MODULATOR WITH A SINE WAVE INPUT

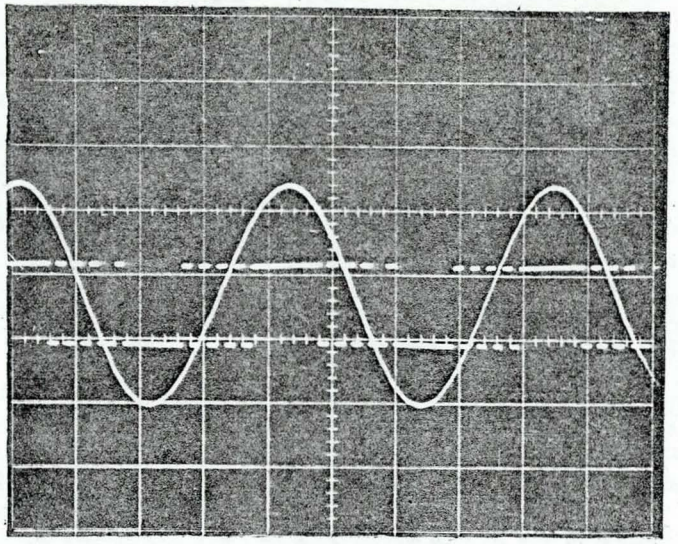


(a) The Input and Output Waveforms

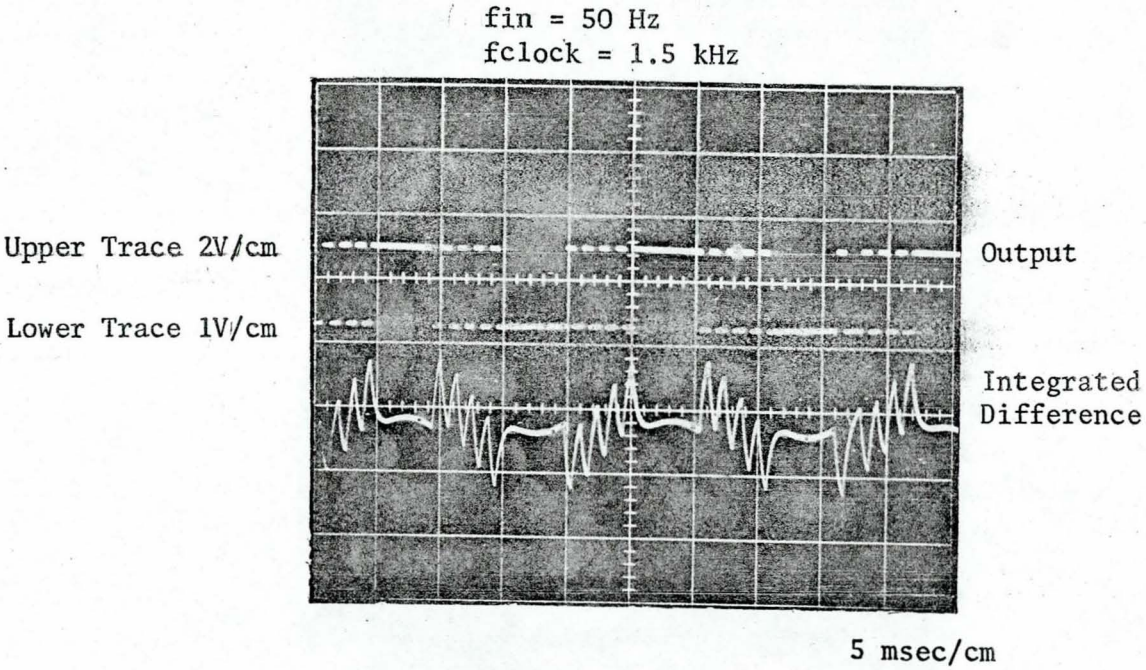


(b) The Output and Integrated Difference

Figure 5.26: WAVEFORMS OF Δ-Σ MODULATOR WITH A SINE WAVE INPUT AND INCREASED CLOCK FREQUENCY

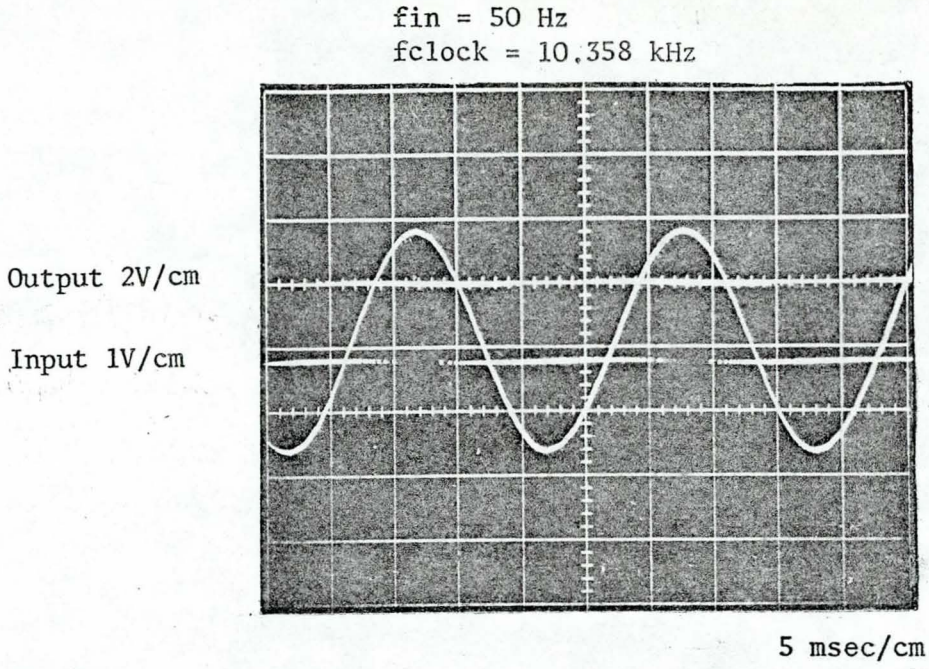


(a) The Input and Output Waveforms

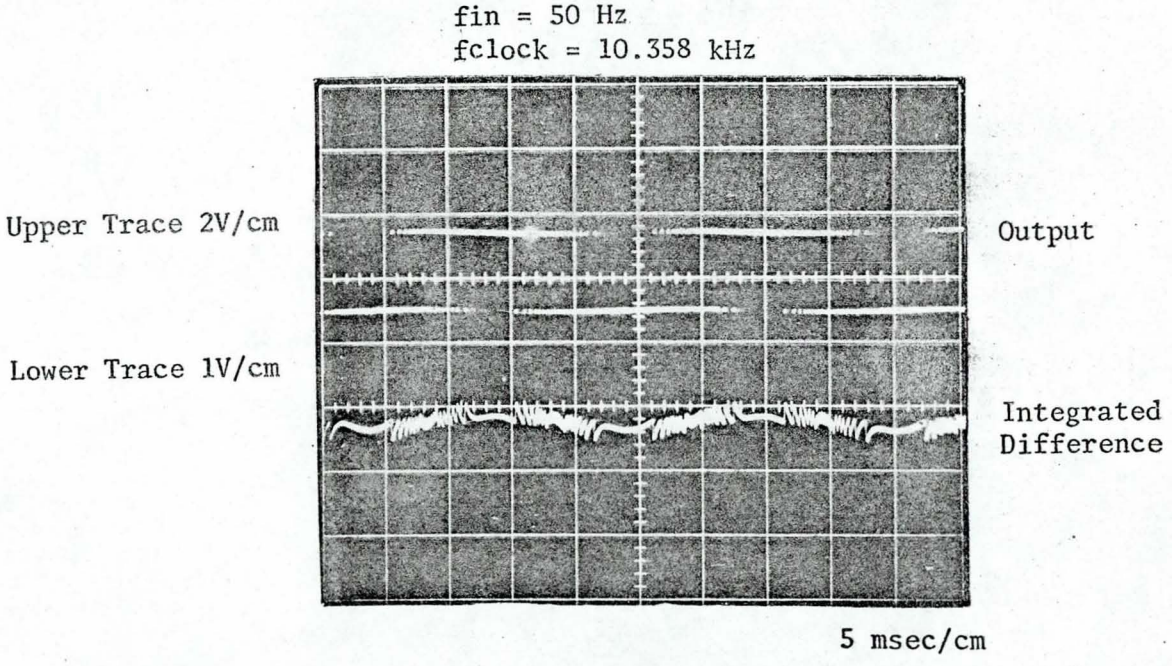


(b) The Output and Integrated Difference

Figure 5.27: WAVEFORMS OF Δ-Σ MODULATOR WITH INCREASED INPUT SINE WAVE FREQUENCY



(a) The Input and Output Waveforms



(b) The Output and Integrated Difference

Figure 5.28 WAVEFORMS OF Δ-Σ MODULATOR WITH INCREASED SINE WAVE INPUT FREQUENCY AND CLOCK SIGNAL FREQUENCY

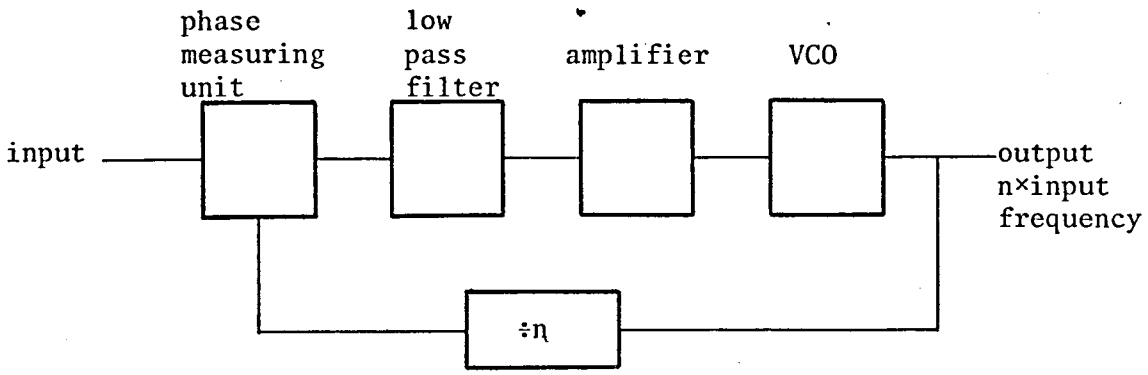


Figure 5.29: BLOCK DIAGRAM OF SYNCHRONISATION UNIT

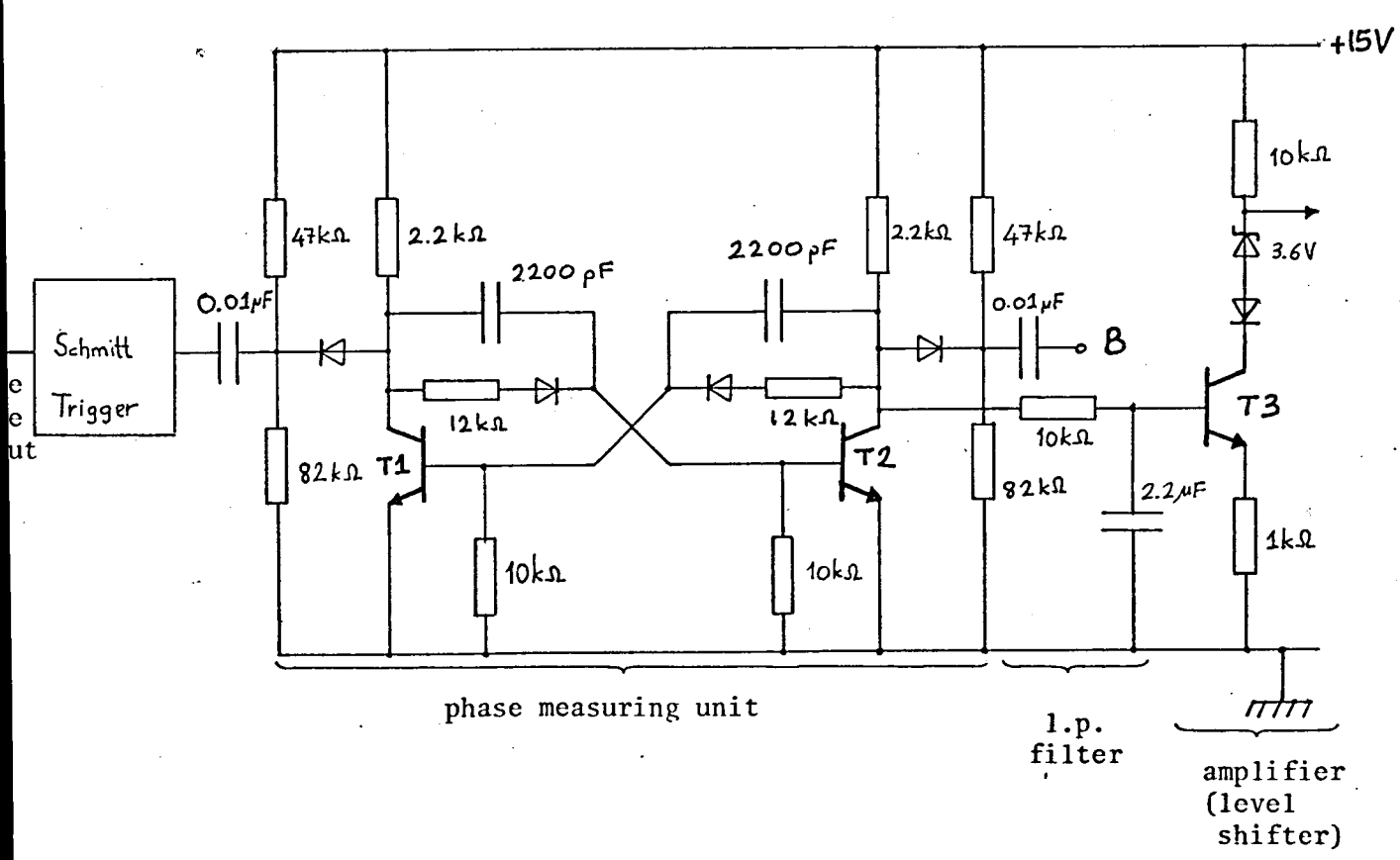


Figure 5.30: CIRCUIT DIAGRAM OF P.M.U., L.P.F. AND AMPLIFIER

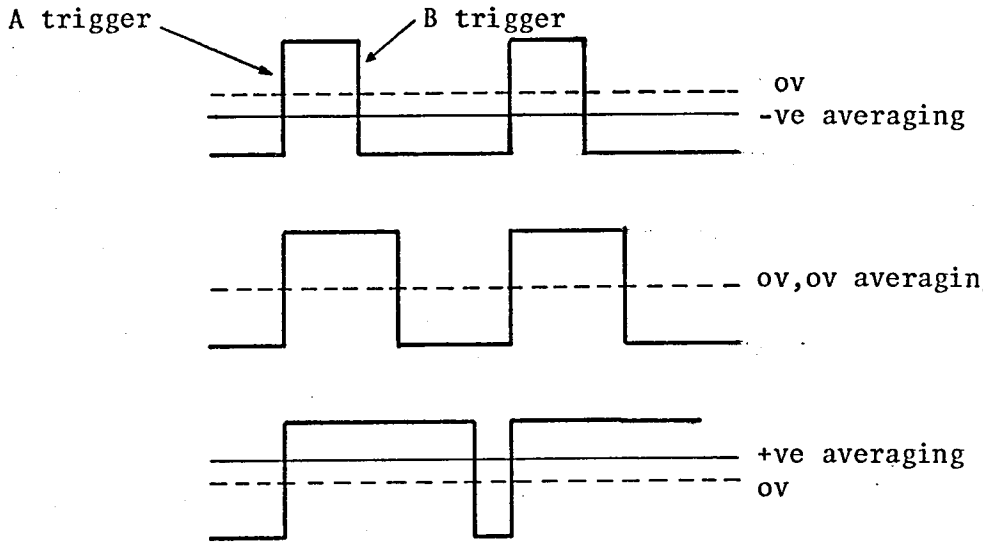


Figure 5.31: WAVEFORMS AT P.M.U.

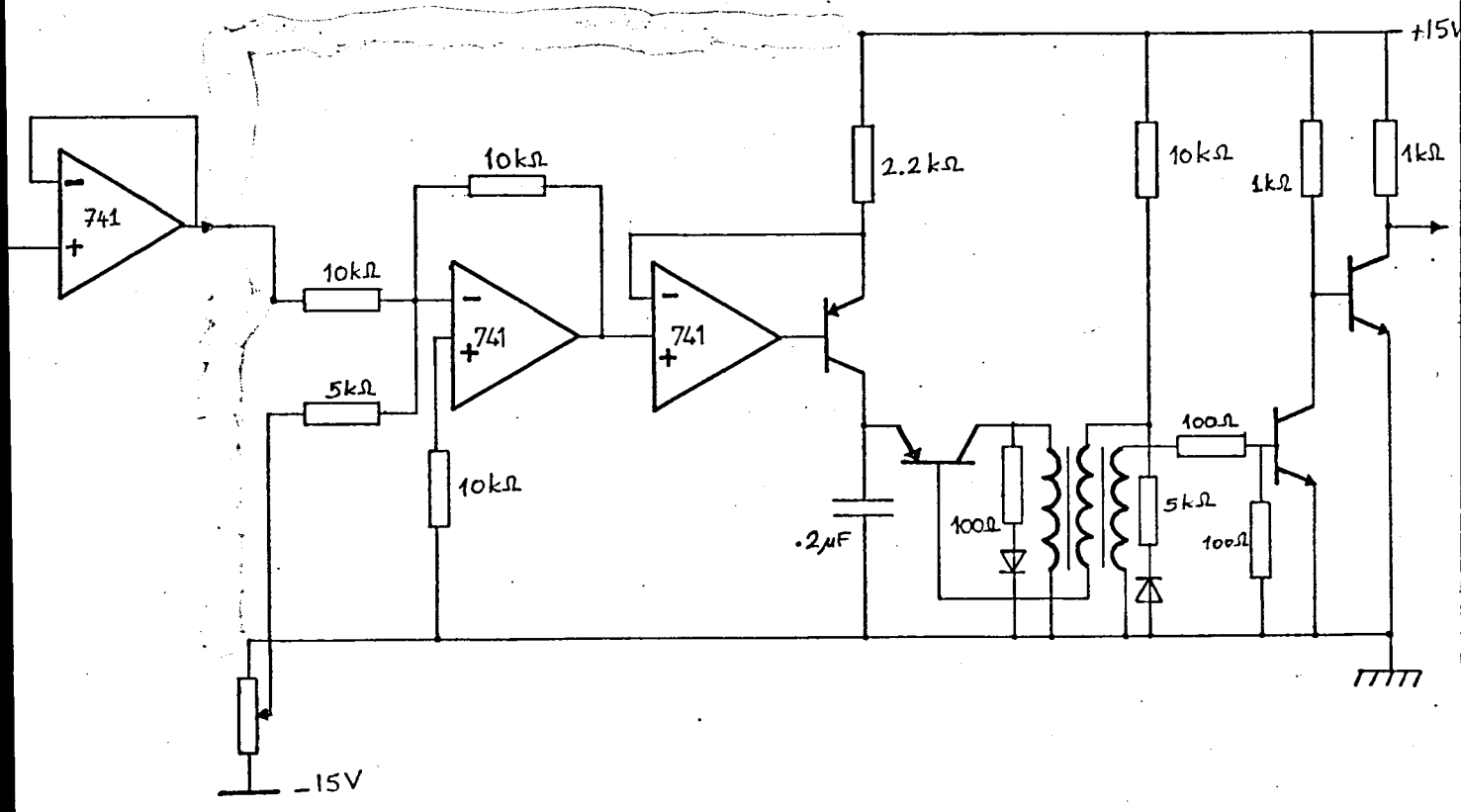


Figure 5.32: CIRCUIT DIAGRAM OF VCO

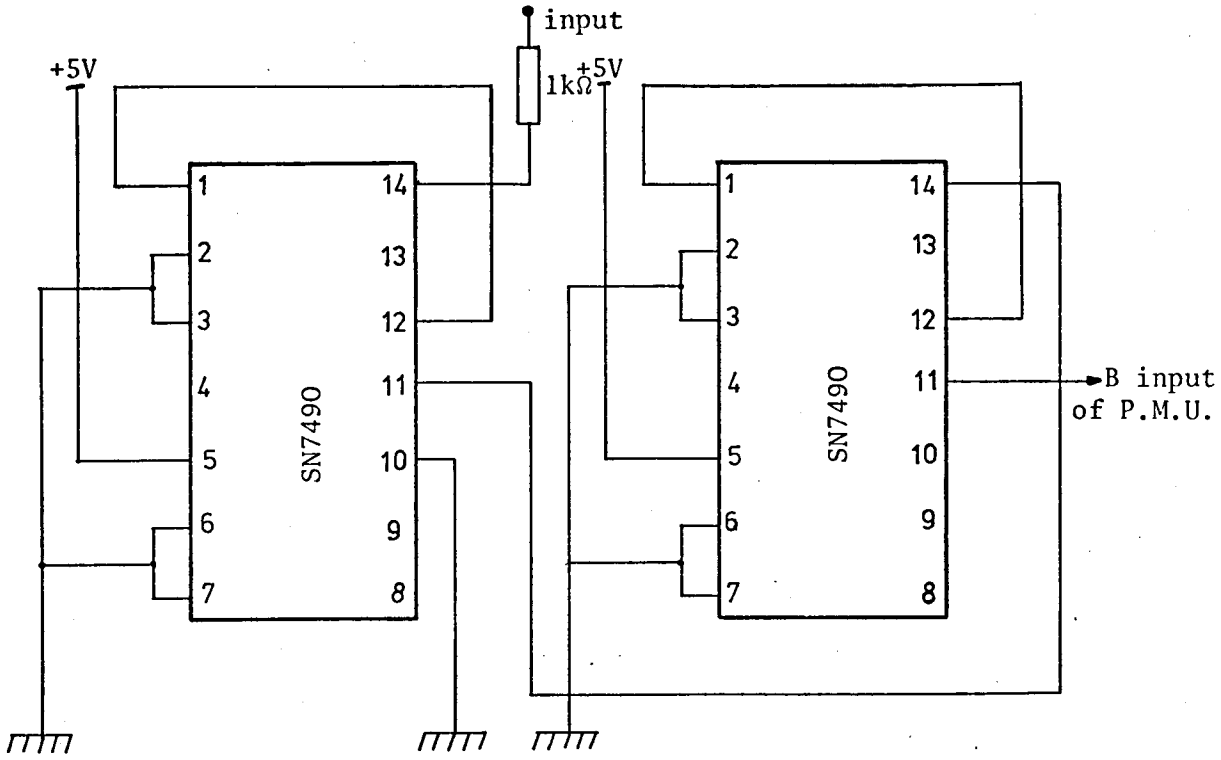


Figure 5.33: DIVIDE BY 100 NETWORK

CHAPTER 6

THE DEVELOPMENT OF THE SPEED CONTROL SYSTEM

This chapter is concerned with the design of a satisfactory speed control system for a 3-phase induction motor. A prototype control scheme built for initial investigational purposes is also described. A discussion of the disadvantages of this system leads to an account of an alternative and improved open-loop system, which may easily be adapted to closed-loop control techniques. The system also has the facilities of speed reversal and acceleration and deceleration control.

6.1 PROTOTYPE SYSTEM

A block diagram of the prototype system is shown in Figure 6.1. It comprises a 3-phase variable frequency oscillator, three V/f control circuits and Δ-Σ modulators, the driver circuit for switching the power transistors and the inverter itself. The sine waves are modulated, and following amplification, they are fed to the induction motor.

6.1.1 3-ph Variable Frequency Oscillator

The circuit diagram of the 3-ph oscillator in shown in Figure 6.2. It is a self-oscillating circuit, made by cascading two inverter integrators with three inverter amplifiers. The time constant is made slightly larger than RC, so that the circuit is slightly unstable. The bounding circuit consists mainly of diodes to stabilise the amplitude of the inverter output, without seriously distorting the sinusoidal waveform. The outputs of the inverting integrators are fed to other inverting amplifiers with outputs a' and b', and on to a summing amplifier to obtain c' the required third sine wave. Resistors R_1 and R_2 are ganged, and used to control the output frequency.

6.1.2 V/f Control Circuit

The V/f control circuit is the simple RC lead network shown in Figure 6.3.a, for which the transfer function is,

$$\left|\frac{V_o}{V_i}\right| = \frac{1}{\sqrt{1+\left(\frac{1}{\omega CR}\right)^2}}$$

with a Bode plot of the characteristics being given in Figure 6.3.b. In order to minimise the effect of the loading of the modulator, R should be kept small. If the break frequency is taken as 100Hz, then

since $\omega RC = 1$

$R = 2.2k\Omega$

and $C = 0.72\mu F$.

This circuit has a response which approximates closely to the required voltage-to-frequency characteristic, so that the level of flux in the airgap of the motor is kept near constant.

6.1.3 Modulator Unit

The modulator unit consists of three bistable Δ-Σ modulators, one for each phase as described in Section 5.5. A square wave generator produces the necessary clock pulses.

6.1.4 The Driver and The Inverter

The driver and the inverter circuits are shown in Figures 6.4 and 6.5 respectively. The output of the transformer drive circuit provides the isolation required from the inverter, with the inputs to the driver circuit consisting of the output of one Δ-Σ modulator and its inverse.

The inverter consists of 6 power transistors, with 6 diodes to return the energy from the windings of the motor back to the supply. The outputs of the three Δ-Σ modulators are fed to the transistors in the upper branches of the bridge (T1, T3 and T5), with the inverse outputs fed to those in the lower branches (T4, T6 and T2). The d.c. power supply for the inverter is obtained from a standard supply capable of producing 2A output current at 50V. The circuit design and other considerations associated with the driver and inverter circuits are treated in detail in Chapter 7.

6.1.5 Discussion

The system described above was designed to be capable of driving a small 3-phase induction motor of rating: 50V, 50Hz, 2500/2750 r.p.m. However, no measurements were taken from this prototype system because of various disadvantages and problems, which may be summarised as

a) Since the 3-phase oscillator is self-oscillating it cannot be used in a closed-loop system, since its frequency cannot be changed by a d.c. level.

b) The amplitudes of the 3-phase sine waves are dependent on their respective frequencies, and the modulation level of the waveforms has an undesirable frequency dependence.

c) The driver circuit is unsuitable (refer to Chapter 7).

6.2 IMPROVED SPEED CONTROL SCHEME

A second prototype system was developed which did not suffer from the above disadvantages. This has the facility for reversible drive, the ability to soft start/stop and it may easily be adapted for closed-loop operation. The control circuitry has been designed and exhaustively tested, and functions satisfactorily.

6.2.1 System Block Diagram

The overall block diagram for the open-loop system is shown in Figure 6.6. The soft start/stop unit which follows the speed selector adjusts the rate at which the speed can be increased or decreased, and in a sense functions as an acceleration or deceleration control circuit. Control Unit 1 has basically two paths, one which changes the frequency and the other which controls the amplitudes of the 3-phase sine waves to keep the ratio V/f constant. Control Unit 2 consists of the Δ-Σ modulators together with delay and driving units for the inverter. The d.c. voltage to the inverter is obtained from a 3-phase supply, after rectification and

filtering. A short circuit prevention unit is included as part of the system.

6.2.2 Soft Start/Stop Unit

Speed changing should be performed continuously, rather than step by step, to ensure minimum acceleration time to load. However, it must also be ensured that the instantaneous slip frequency never reaches or exceeds the pull-out value corresponding to the instantaneous frequency supplied.

Assume that the motor is supplied with a sine wave, such that n_1 is its synchronous speed, and that the rotor speed corresponds to point A of Figure 6.7. Reference to this figure shows that a step change in frequency to produce a synchronous speed of n_3 gives curve 3 as the new torque/speed relationship. The torque will instantly increase to that corresponding to point B and the resulting acceleration to the new speed is determined by curve 3. Suppose, alternatively, that the frequency is increased to that corresponding to point C, so that curve 2 now determines the resulting acceleration. It can be seen that a greater initial torque is available to accelerate the motor, and that by a suitable subsequent switch to curve 3, this can be picked up to provide the minimum acceleration time. By making the changes continuous, the process can obviously be more efficiently performed in a much shorter time.

Figure 6.8 shows an extreme case when too big a change is made in the supply frequency. When an adjustment of frequency changes the synchronous speed from n_1 to n_2, the new motor speed is determined by curve 2 and the torque developed is reduced to that corresponding to point B. This is on the unstable region of the torque/speed characteristics, and since the load torque is greater than the available motor torque the motor decelerates rapidly to standstill.

The soft start/stop unit prevents the possibility of the motor stalling, and acts in such a way that the speed variations are continuous. It also

controls the rates of increase and decrease of frequency in order

a) to provide smooth changes in the signal frequency to the modulator unit

b) to limit the motor acceleration and deceleration to specified values.

The operation of the soft start/stop circuit can be understood by considering a forward limiter circuit as shown in Figure 6.9. Voltages V_1 and V_2 provide the limiting conditions for the operation of amplifiers A_1 and A_2, and they have positive and negative levels respectively. When the input voltage is such that $V_2<V_{in}<V_1$, amplifiers A_1 and A_2 are limited and diodes D_1 and D_2 are turned off, so that in this range the output voltage follows the input. If the input voltage goes outside the operating region, the differential input voltage of amplifier A1 is reduced to zero and $V_{out}=V_1$ if $V_{in}>V_1$. An analogous but negative limiting function applies if $V_{in}>V_2$. Operation of the limiter is then such that the output voltage cannot assume a positive value higher than the positive set point V_1, or a negative value higher than the negative set point V_2. Between these limits the output voltage is equal to the input voltage.

Figure 6.10 shows a complete circuit diagram of the soft start/stop unit. The speed selector sets the reference value for the speed, with a positive setting of VR1 for one direction of rotation and a negative setting for the other. The output of the limiter is linearly integrated by IC4, with the resulting output coupled with the input of IC1 in such a way that, as soon as the resultant output reaches the reference speed voltage (i.e. the input to the soft start/stop unit), a feedback circuit clamps the output until a further change occurs in the reference voltage. Potentiometer VR2 controls the positive slope of the output (and hence the acceleration), while potentiometer VR3 controls the negative slope of the output (and hence the deceleration). With different values of integrating capacitor C, very long delays can be introduced in the circuit.

Figure 6.11 shows ultra-violet recordings of the output voltage of the soft start/stop unit for a square wave input, i.e. a positive and a negative step change in the speed selector of Figure 6.10 for different

settings of VR2 and VR3.

6.2.3 Phase Sequence Reversible, Voltage Controlled 3-Phase Oscillator[22]

If a sine wave of frequency f_{in} is sampled and held as shown in Figure 6.12, a further sine wave of lower frequency may be obtained. The relationship between the frequencies and the phases of the input and the output signals is easily obtained. Assuming the frequency of the waveform which is sampled to be f_{in} and the phase to be ϕ_{in}, the output can be represented by a sine wave of frequency f_{out} and phase ϕ_{out}. Then for all sampling instants,

$$\sin(\omega_{in}t+\phi_{in}) = \sin(\omega_{out}t+\phi_{out}) \tag{6.1}$$

$$\sin(2\pi f_{in}t+\phi_{in}) = \sin(2\pi f_{out}t+\phi_{out}) \tag{6.2}$$

If sinA=sinB then $A=B+2n\pi$ where n=0,1,2,..., so that one solution of equation (6.2) is:

$$2\pi f_{in}t = 2\pi f_{out}t+2n\pi \quad \text{and} \quad \phi_{in} = \phi_{out}$$

$$f_{in}t = f_{out}t+n$$

$$f_{out} = f_{in} - \frac{n}{t} \tag{6.3}$$

and if the sampling frequency is f_s, samples are taken at intervals of $\frac{1}{f_s}$. Sampling instants occur therefore at times

$$t = \frac{k}{f_s} \quad \text{where} \quad n=0,1,2$$

and substituting in equation (6.3)

$$f_{out} = f_{in} - \frac{n}{\frac{k}{f_s}} = f_{in} - \frac{n}{k}f_s \text{ and letting } N = \frac{n}{k},$$

where N=1,2,3,...

$$f_{out} = f_{in} - Nf_s \tag{6.4}$$

$$\phi_{out} = \phi_{in} \tag{6.5}$$

It will be seen from equations (6.4) and (6.5), that, if $f_{in}>Nf_0$, an increase in ϕ_{in} produces a corresponding increase in ϕ_{out}. If, on the other hand, $f_{in}<Nf_s$, the solution to equation (6.2) is

$$f_{out} = Nf_s - f_{in} \tag{6.6}$$

$$\phi_{out} = -\phi_{in} + \pi \tag{6.7}$$

When $f_{in}<Nf_s$, f_{out} thus has a positive value as in the previous case, but an increase in ϕ_{in} produces a corresponding decrease of ϕ_{out}. A numerical example will clarify the principle further.

Assuming N = 1, f_{in} = 120Hz, and f_s = 100Hz

then f_{out} = 120-100 = 20Hz.

and an increase of 120^o in the phase of the input will produce the same phase shift in the output. If f_{in} is 80Hz, the output frequency will still be 20Hz, but an increase of 120^o in the phase of the input will now produce a corresponding decrease of 120^o in the phase of the output.

If the instant of sampling is delayed by a fraction x of a sampling period, this corresponds to an advance in the phase of the input waveform of $f_{in}\frac{x}{f_s}2\pi$ rads, plus a time delay of $\frac{x}{f_s}$ secs. If $f_{in}>Nf_s$, an advance in phase of the input waveform will produce a corresponding advance in phase of the output waveform, and the total phase shift of the output waveform is the algebraic sum of this phase advance plus the phase lag due to the time delay of $\frac{x}{f_s}$. That is,

$$\theta = \frac{x}{f_s} f_{in} 2\pi - \frac{x}{f_s} f_{out} 2\pi$$

$$\theta = \frac{x}{f_s} f_{in} 2\pi - \frac{x}{f_s} (f_{in} - Nf_s) 2\pi$$

$$\theta = xN2\pi \tag{6.8}$$

which shows that the phase shift of the output waveform is independent of the frequency of the input.

Hence when a single phase sine wave is sampled by a 3-phase set of sampling waves, for which x=0, x=1/3 and x=2/3 respectively, the result is three waveforms shifted from each other by $2\pi/3$ rad. or $-2\pi/3$ rad. depending on whether $f_{in}>Nf_s$ or $f_{in}<Nf_s$.

Figure 6.13 shows a block diagram of a practical 3-phase oscillator, designed according to the above principles. The voltage controlled oscillator produces a set of pulses, with a frequency range of

$$6(f_1-f_2) \lesssim f \lesssim 6(f_1+f_2)$$

The 3-stage Johnson counter divides the input from the VCO by 6, and gives a set of 3 outputs mutually displaced by 120^o in phase and with a frequency range:

$$(f_1-f_2) \lesssim f \lesssim (f_1+f_2)$$

When used to sample and hold a sine wave of frequency f_1, these pulses give three sine waves of frequency f_2 mutually displaced by 120^o. An active low-pass filter is employed to remove the high-frequency components.

6.2.3.1 Voltage Controlled Oscillator

The operation of the VCO can be best understood by considering the circuit shown in Figure 6.14. When transistor T1 is fully on a current I flows, and the capacitor C charges until the voltage across it exceeds the level set by R2 and R3. Transistor T2 then conducts, and capacitor C discharges through transistor T2 to the pulse transformer winding. Due to the secondary base connection, the base of transistor T2 falls further, so that this turns on harder and discharges C extremely rapidly. This action causes an output pulse from the second secondary winding to the transformer. When the capacitor C is discharged fully transistor T2 switches off, and the inductive energy in the winding is discharged through D1 and R4. The drift in frequency is negligible, since the level at which T2 turns on is fixed by R2 and R3. Since

$$Q = CV \quad \text{and} \quad It = CV$$

it follows that $t = \frac{CV}{I}$

and that the frequency is:

$$f = \frac{I}{CV} \tag{6.9}$$

It can be deduced from equation (6.9) that the frequency is constant if the current I is kept constant. To have a variable frequency voltage controlled oscillator, the current I must be varied in proportion to a control voltage, and an operational amplifier circuit to accomplish this is shown in Figure 6.15. The op-amp is connected as a voltage follower, with the emitter of transistor T1 following the input to the op-amp i.e. the control voltage V_C. There is a drop of voltage between the base and the emitter of T1 to keep the transistor T1 always in conduction, since

$$I = \frac{V_{CC}-V}{R1} \qquad (6.10)$$

Thus when V_C (and hence V) is changed, the current I and hence the frequency also change. When V_C increases, V also increases and since I has been reduced the frequency is also reduced.

The complete circuit diagram of the oscillator is shown in Figure 6.16. It can be seen from equation (6.10) that the frequency of oscillation is inversely proportional to the control voltage, and to overcome this difficulty the d.c. amplifier circuit using IC2 has been incorporated. Initially a negative voltage is applied to IC2 , and after inversion by IC2 the output is fed through IC3 to increase the emitter potential of transistor T1 and to reduce the current through it. The lowest frequency of the voltage controlled oscillator is adjusted to 5400Hz by the initial setting of VR1, and the upper limit to 6600Hz by the level of input voltage available from the soft start/stop unit. The IC1 works as a voltage follower (i.e. an impedance transformer), with the transistors T3 and T4 shaping the output pulses to be fed to the Johnson counter.

6.2.3.2 3-Stage Johnson Counter

The Johnson counter is basically a ring counter consisting of three J-K flip-flops (SN7473N), as shown in Figure 6.17.a, with the outputs

Q_A,Q_B and Q_C being as shown in Figure 6.17.b. By comparing Q_A,Q_C and $\overline{Q_B}$ it is seen that these have a mutual phase shift of 120^o, and it follows that their positive edges may therefore be used for the sample-and-hold function required in the generation of a 3-phase output. For an input frequency range of $5400Hz \leq f \leq 6600Hz$ the outputs of the Johnson counter have a frequency range of $900Hz \leq f \leq 1100Hz$.

6.2.3.3 Sine Wave Oscillator

As shown in Figure 6.18, the sine wave oscillator consists basically of a Twin-T network connected between the input and the output of the operational amplifier. A conventional Twin-T circuit is said to be balanced when the components have the ratios

$$R3 = R4 = 2(R5+R6) \text{ and}$$

$$C1 = C3 = C2/2$$

when it acts as a frequency-dependent attenuator, giving zero output at a centre frequency of

$$f = 1/6.28\ R3 \times C1$$

and a finite output at all other frequencies.

When the Twin-T network is imperfectly balanced it gives an attenuated but finite output at the centre frequency, with the phase of this signal being dependent on the direction of the imbalance. If the imbalance is caused by R5+R6 being too low, the phase of the output is inverted relative to the input. As can be seen in Figure 6.18, the input of the Twin-T network is taken from the output of the op-amp, and the output of the Twin-T is fed to the inverting input of the op-amp. Resistor R6 is adjusted so that the Twin-T gives a small output at the centre-frequency, which is phase-inverted relative to the input. Zero overall phase inversion thus takes place between the output and the input of the op-amp at the centre-frequency, and the circuit therefore oscillates at this frequency.

The circuit was designed with a centre frequency of 1kHz.

6.2.3.4 Sample and Hold Circuit

The block diagram of the sample-and-hold circuit is shown in Figure 6.19.a. The switch samples the sine wave, while the capacitor C charges instantaneously to the value of the sine wave at the instant of sampling. Since the input impedance of the op-amp is very large, the capacitor C keeps this charge until the next sampling occurs. The op-amp, which is connected as a voltage follower, follows the voltage of the capacitor.

The complete circuit diagram of the sample-and-hold circuit is shown in Figure 6.19.b, with a field effect transistor used as the switching element. When a FET conducts its resistance falls to about 100Ω, so that a time of RC=100×0.01=1μs. is required to charge the capacitor C and the sampling period ≥1μs. The capacitor C1 differentiates the square wave output of the Johnson counter, and by turning on transistor T1 for about 10μs. enables capacitor C to become charged. The complete inverter unit requires three sample-and-hold circuits for each phase of the inverter output.

6.2.3.5 Low-Pass Filter

An active 2nd-order low-pass Butterworth filter as shown in Figure 6.20 was used to remove the high-frequency components introduced by the sampling action. Analysis[23] of Figure 6.21 gives the transfer function of this filter as:

$$\frac{V2(s)}{V1(s)} = \frac{k}{s^2+as+b}$$

where:

$$k = \frac{\mu}{R1\times R2\times C\times C1}$$

$$a = \frac{1}{R2\times C1}(1-\mu) + \frac{1}{R1\times C} + \frac{1}{R2\times C}$$

$$b = \frac{1}{R1\times R2\times C\times C1}$$

$\mu = 1 + R4/R3$ is the gain of the filter.

For a filter gain of 2,R3=R4, and by choosing the cut-off frequency as 250Hz the circuit components are calculated as,

$C = C1 = 0.1\mu F$

$R1 = 4.5k\Omega$

$R2 = 9k\Omega$

$R3 = R4 = 27.5k\Omega$

with the nearest practical components to these being used in the filter circuit.

6.2.3.6 Performance

The frequency of the VCO output varies between 5400Hz and 6600Hz, and this range of frequencies is difficult to record with a UV recorder. To observe the operation of 3-phase oscillator it was necessary to employ an arrangement using two standard oscillators. One of these is kept at 540Hz with its output fed to the Johnson counter. Recordings of two of the corresponding outputs are shown in Figure 6.21. As can be seen, these are phase shifted by 120^{o} and their frequency is reduced by a factor of 6. The other oscillator supplies a sine wave of 100Hz frequency, and its output is connected to the sample-and-hold circuit. Figure 6.22 shows the sine wave input, one of the outputs of the Johnson counter and the low frequency sine wave resulting from sampling and holding the sine wave by the positive edges of the square wave. The frequency of the sine wave output is 10Hz as expected.

Figure 6.23 shows the sine wave input to the sample-and-hold circuit, the output of the Johnson counter and the resulting sine wave obtained from the actual system designed (without the two external oscillators). The output sine wave frequency is 20Hz. Figure 6.24 shows the outputs of the three sample and hold circuits for two different frequencies and Figure 6.25 the outputs of the three low-pass filters.

6.2.4 V/f Control Unit

The function of the V/f control unit was explained in Chapter 2. The output of this unit is fed to the multiplier unit, and since the amplitudes of the 3-phase sine waves are constant before they enter the multiplier, the V/f control unit output determines the amplitudes of the sine waves. The complete circuit of the unit is shown in Figure 6.26.a and the various input/output characteristics that can be obtained are shown in Figure 6.26.b. The operation of the unit is as follows:

When the input is negative the output of IC1 is positive, and diode D2 inhibits action of the feedback loop so that (with the action of D1) the output of IC1 is kept at 0V. IC2 operates as an inverting amplifier of unity gain, with an output equal to input. When the input becomes positive the output of IC1 becomes negative, so that diode D2 is forward biassed and the unity gain feedback causes the output of IC1 to be identical with the input. The positive input and the output of IC1 are fed to IC2, where

$$V_{out} = -\frac{R7}{R3} V_{in} - \left(-\frac{R7}{R4} V_{out} \text{ of IC1}\right)$$

the component values in Figure 6.26.a give,

$$V_{out} = V_{in}$$

The offset V_x in Figure 6.26.b is adjusted by VR1, as necessary for low frequency operation.

Figure 6.27 shows the input and output of the V/f control unit with and without V_x.

6.2.5 Multiplier Unit

The 3-phase sine waves and the output of the V/f control unit are multiplied in the unit shown in Figure 6.28. This comprises one Motorola MC1495 linear integrated circuit and an operational amplifier. The MC 1495 is a monolithic, 4-quadrant multiplier operating on the principle of variable transconductance, and since the maximum input

voltage is limited to ±5V, resistive dividers are included at the input. The initial setting of the multiplier unit is somewhat complex and the following adjustment procedure is used:

1) X-Input Offset

   (a) Connect oscillator (1kHz, 5Vpp sine wave) to the "Y" input (pin 4)

   (b) Connect "X" input (pin 9) to ground

   (c) Adjust X offset potentiometer, P_2, for an a.c. null at the output

2) Y-Input Offset

   (a) Connect oscillator (1kHz, 5Vpp sine wave) to the "X" input (pin 9)

   (b) Connect "Y" input (pin 4) to ground

   (c) Adjust "Y" offset potentiometer, P_1, for an a.c. null at the output

3) Output Offset

   (a) Connect both "X" and "Y" inputs to ground

   (b) Adjust output offset potentiometer, P_4, until the output voltage V_0 is zero volts d.c.

4) Scale Factor

   (a) Apply +10V d.c. to both "X" and "Y" inputs

   (b) Adjust P_3 to achieve +10.00V at the output

5) Repeat steps 1 through 4 as necessary.

The two inputs and the output of one of the multipliers are shown in Figure 6.29.

6.2.6 Modulator Unit

Three Δ-Σ modulators are necessary, one for each phase. The outputs of these go to delay units through interface circuits, which invert the modulated signals and improve the noise immunity. Figure 5.22 and Figure 6.30 respectively show circuit diagrams of the modulator and the interface circuit.

6.2.7 Delay Units

A delay unit is necessary to prevent a short circuit appearing across a branch of the inverter, and Figure 6.31.a and Figure 6.31.b explain how this can be achieved. A comparison of the outputs of $(\Delta\text{-}\Sigma)_1$ and $(\Delta\text{-}\Sigma)_2$ of the delay unit indicates that the positive and negative edges of the pulses are delayed by a time interval Δt, such that sufficient time is allowed for one transistor in the inverter to switch off completely before the next is switched on. Figure 6.32 was developed to replace the circuit Figure 6.31.a. since,

(a) In the former case two monostables, two inverters and two AND gates are needed.

(b) The IC modules performing the above function require 5V supply and hence have less noise immunity.

The operation of delay unit is explained by Figure 6.33.

6.2.8 Power Supplies

Two power supplies were designed for the control circuitry. The +15, -15V voltage supply required for the operational amplifiers was obtained from the circuit shown in Figure 6.34. This provides a short-circuit proof supply with a ripple at 0.5A output current of 5mV (i.e. 0.04%) and at 1A output current of 30mV (i.e. 0.2%). Resistors R1,R2 and diodes D5, D6 are necessary for initial switching on transistor T1 and hence transistor T2, and diode D8 is to minimise thermal drift (diodes D7 and D8 have temperature coefficients of opposite polarity). When a short circuit occurs at the output, the voltage across the zener diode D7 collapses and transistor T1 switches-off, also turning off transistor T2.

A further power supply delivering 1A at 5V was built using the voltage regulator LM 309K, which has internal current limiting and thermal protection. Capacitor C2 improves the ripple rejection of the circuit,

and capacitor C1 is only necessary if the IC is some distance away from the reservoir capacitor. The circuit diagram of this supply is shown in Figure 6.35.

6.3 PERFORMANCE OF THE CONTROL UNIT

Figure 6.36 shows waveforms of the control voltage, the output of the low-pass filter and the output of the multiplier. As can be seen, an increase in the control voltage increases not only the frequency but also the amplitude of the sine wave. Figure 6.37 shows the outputs of the three low-pass filters. The magnitudes of the sine waves are scaled differently so that the phase reversal can be seen. Figure 6.38 shows the outputs of the three multipliers. It can be clearly seen from the above figures, that the control unit functions entirely satisfactorily.

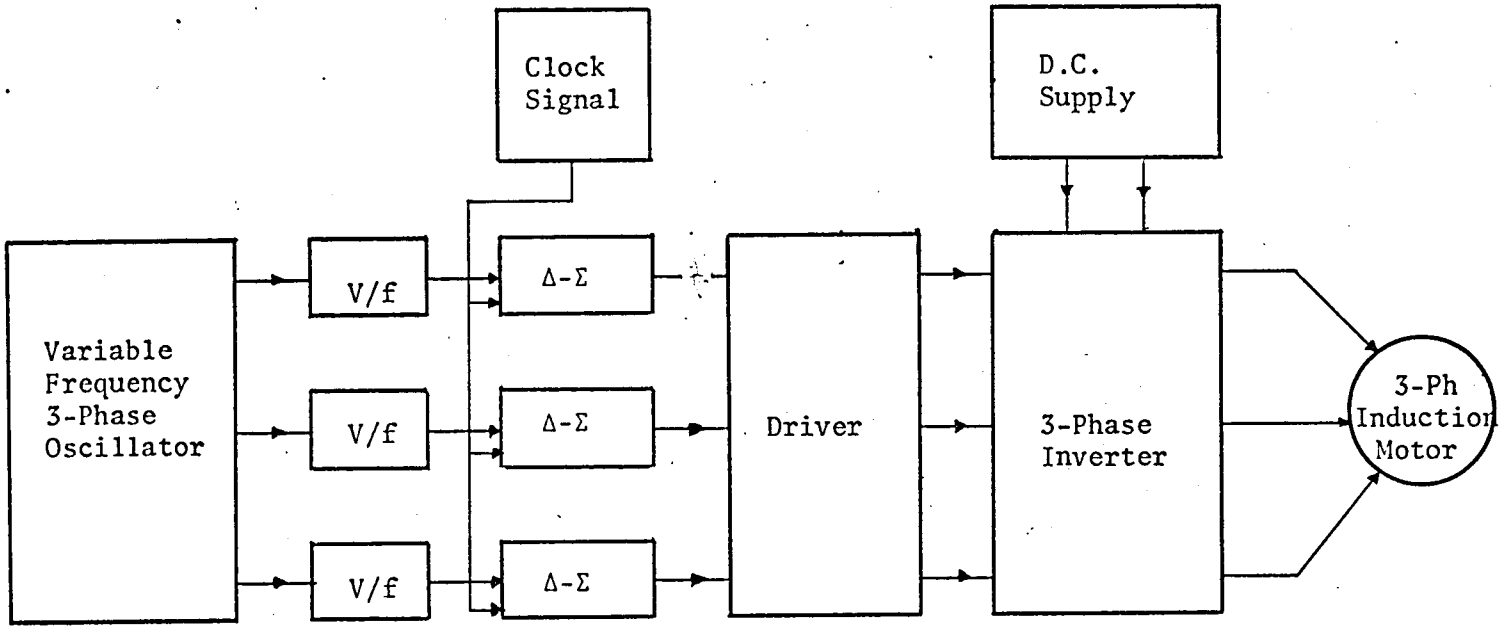


Figure 6.1: BLOCK DIAGRAM OF THE PROTOTYPE SPEED CONTROL SYSTEM

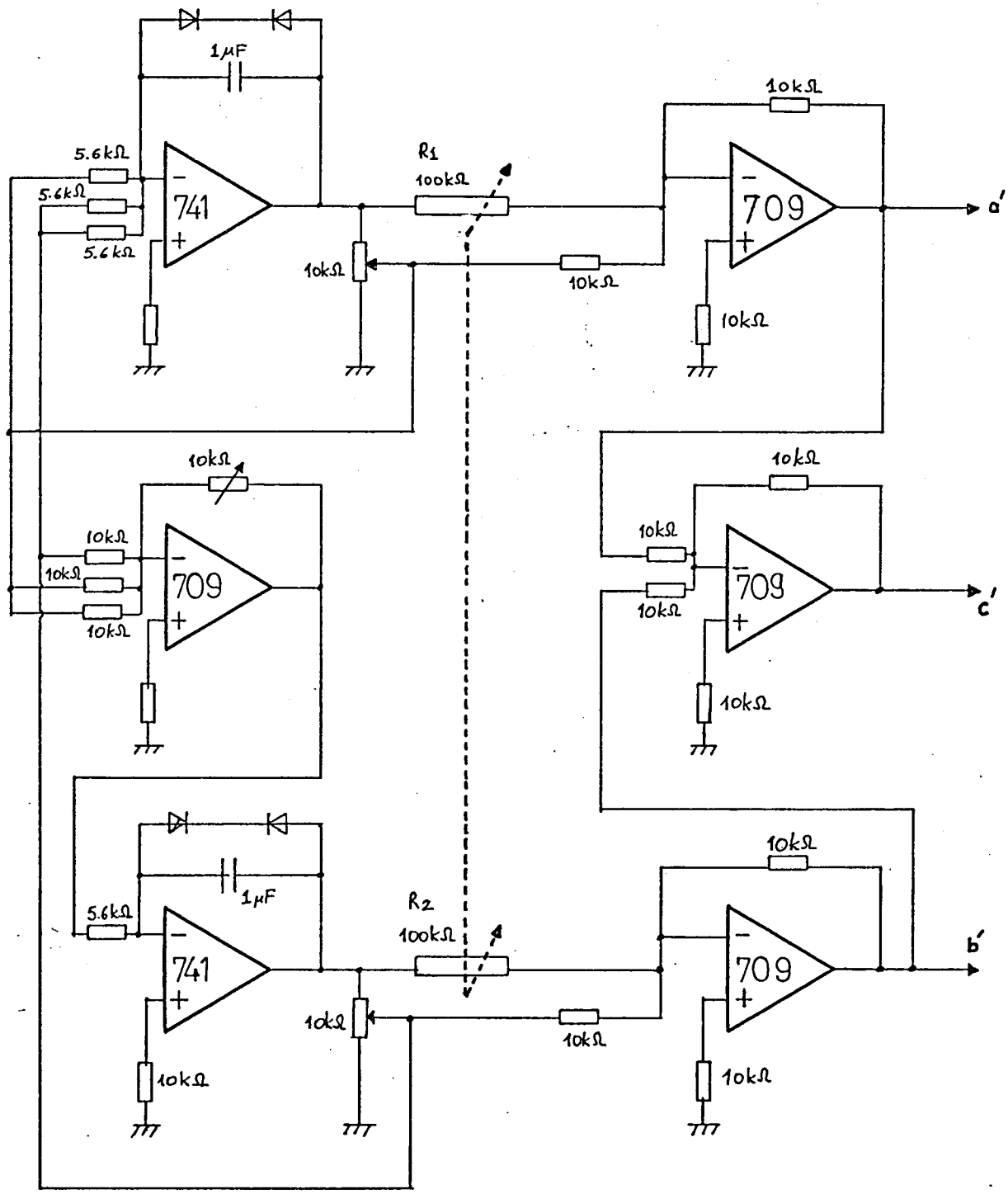
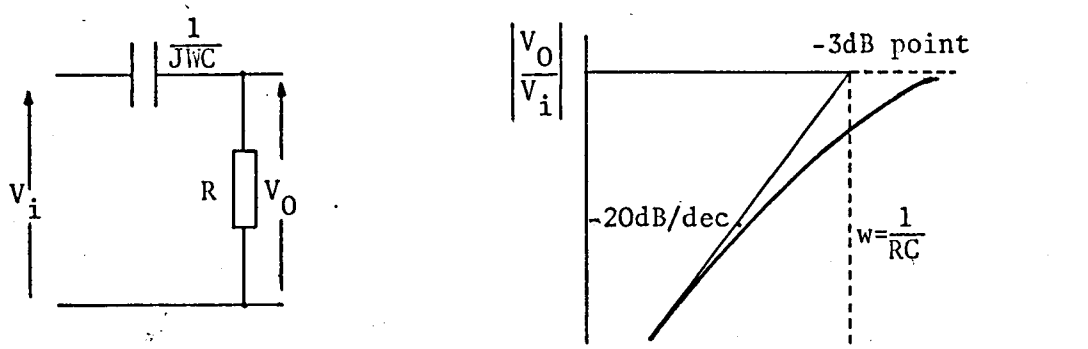


Figure 6.2: CIRCUIT DIAGRAM OF 3-PHASE OSCILLATOR



(a) Lead Network

(b) Bode Plot of Transfer Function

Figure 6.3: V/f CONTROL CIRCUIT AND ITS CHARACTERISTICS

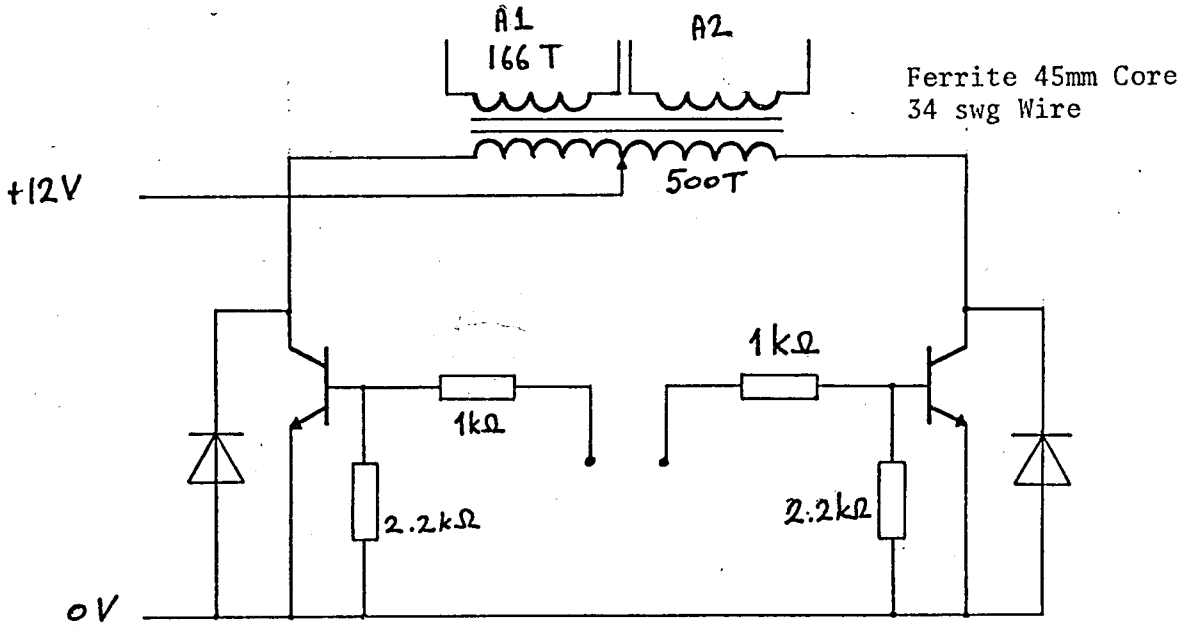


Figure 6.4: THE DRIVER

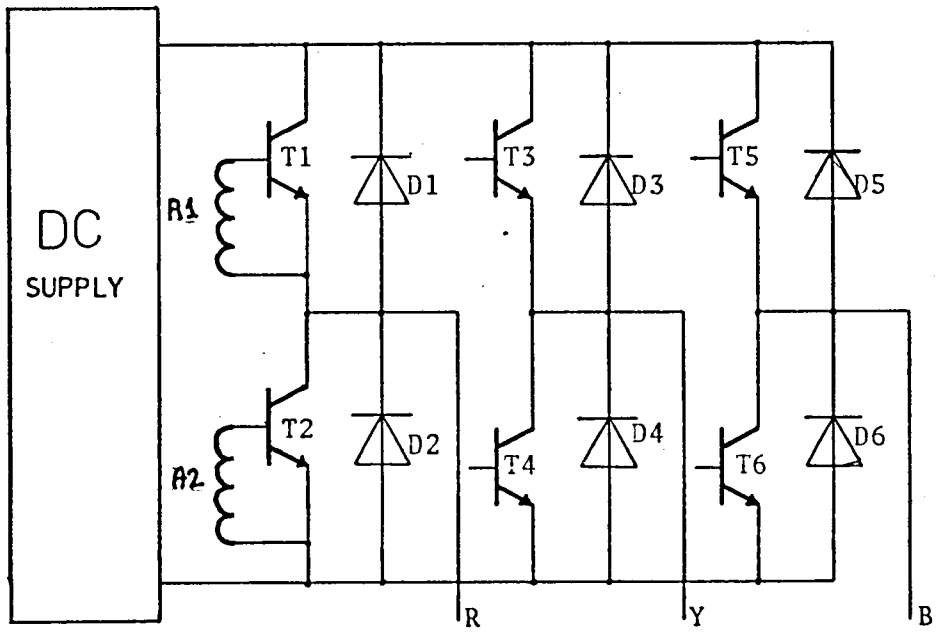


Figure 6.5: 3-PHASE INVERTER

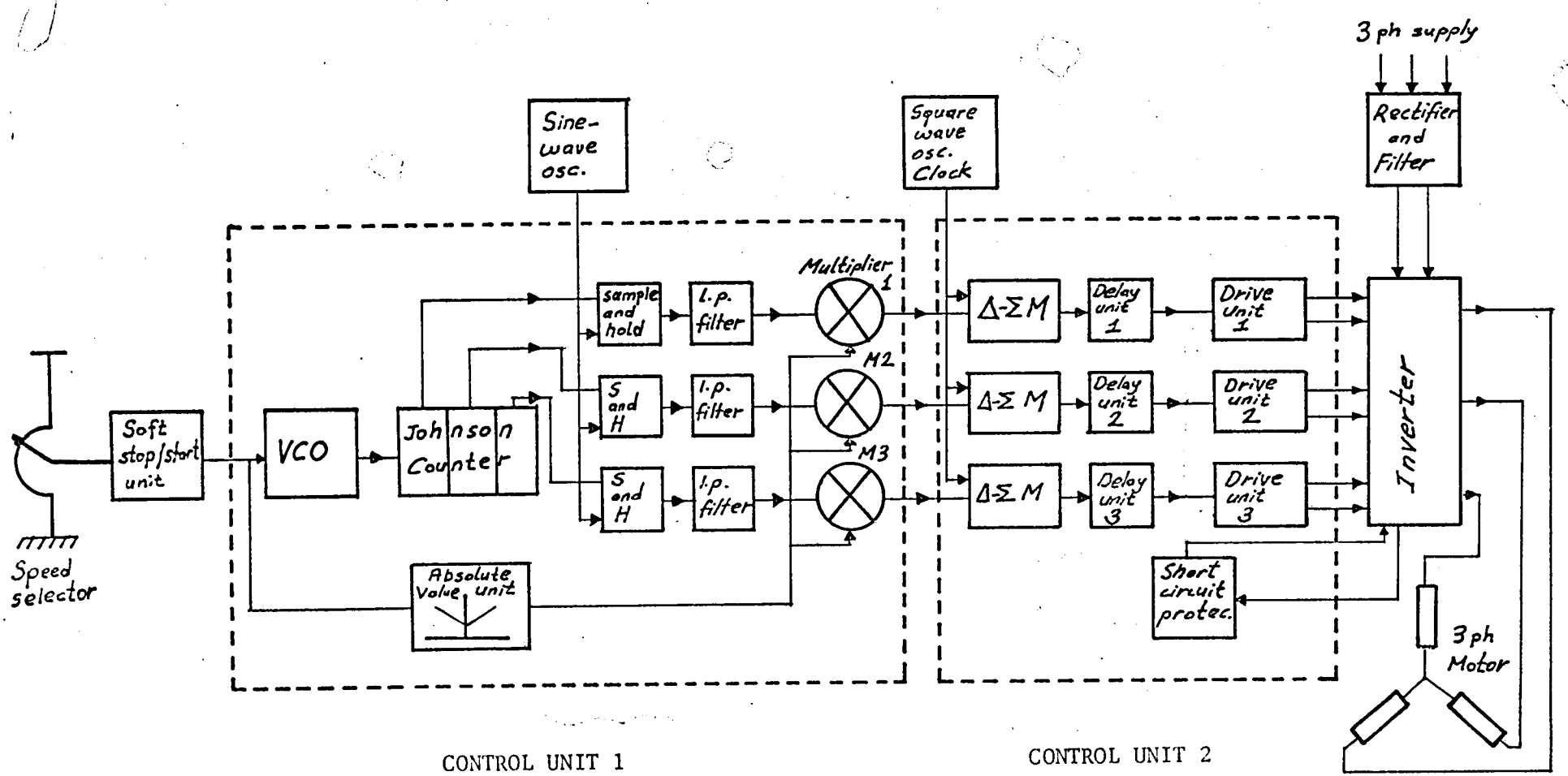


Figure 6.6: BLOCK DIAGRAM OF THE IMPROVED SPEED CONTROL SYSTEM

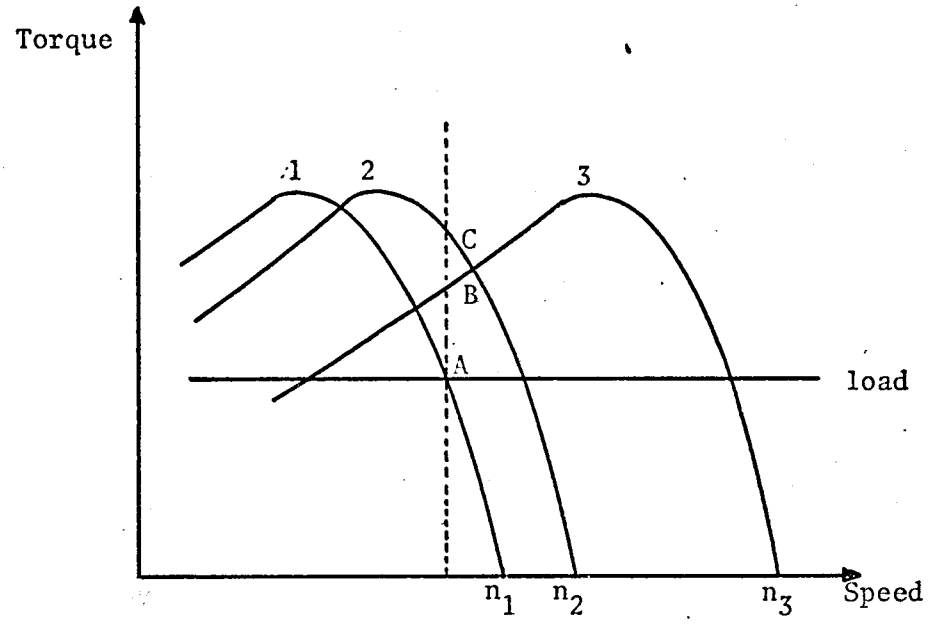


Figure 6.7: TORQUE-SPEED CHARACTERISTICS FOR A STEP CHANGE IN SPEED

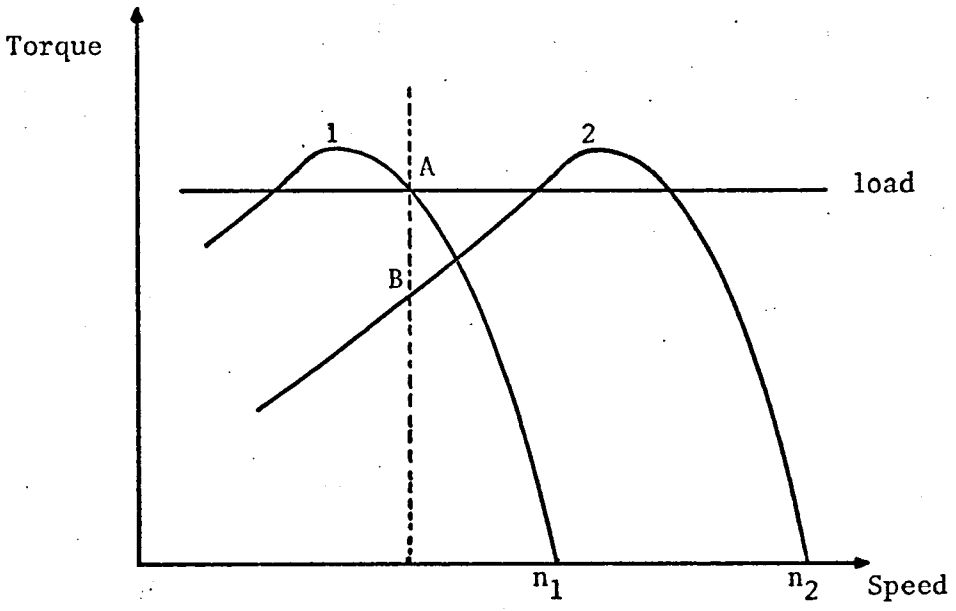


Figure 6.8: TORQUE-SPEED CHARACTERISTICS FOR A VERY LARGE STEP CHANGE IN SPEED

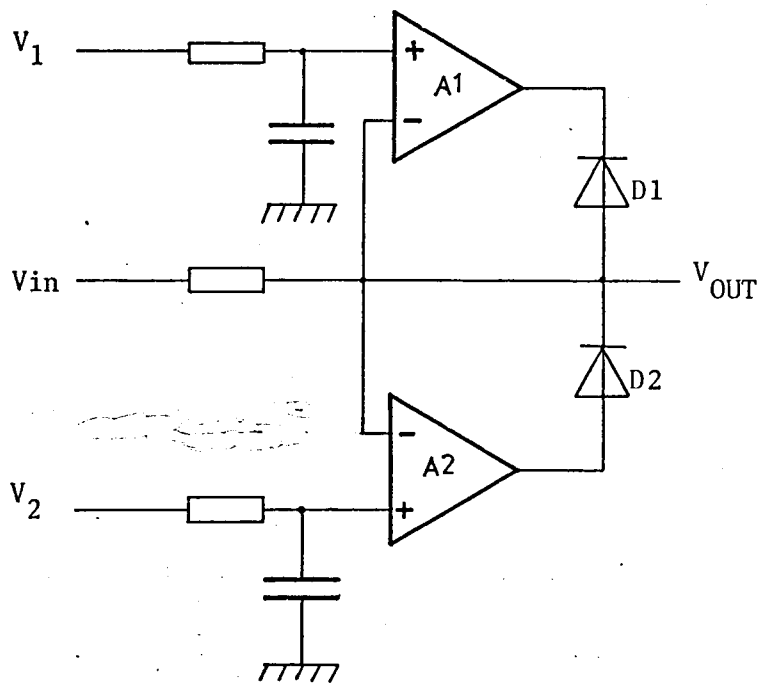


Figure 6.9: BASIC FORWARD LIMITER

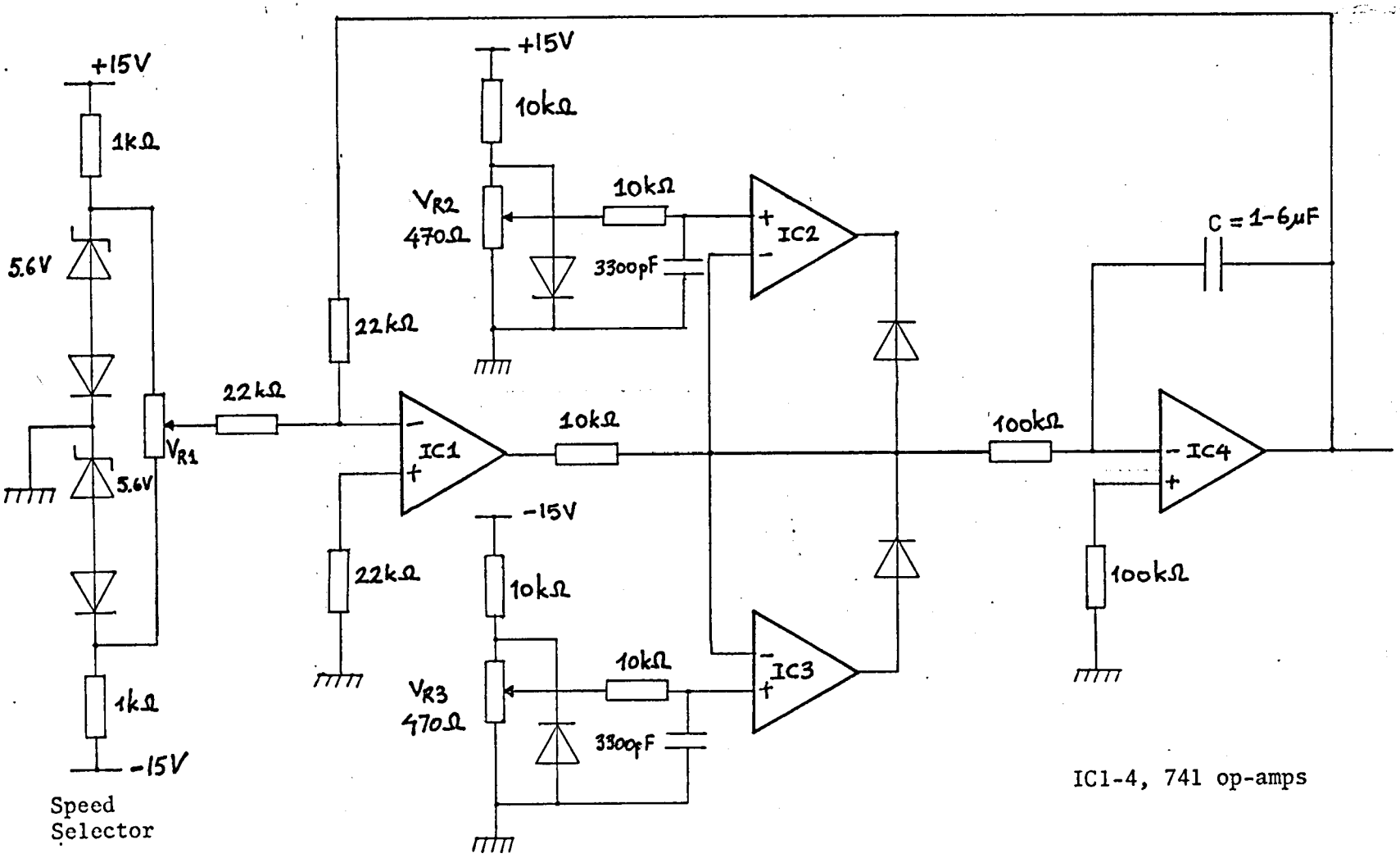


Figure 6.10: CIRCUIT DIAGRAM OF SOFT START/STOP UNIT

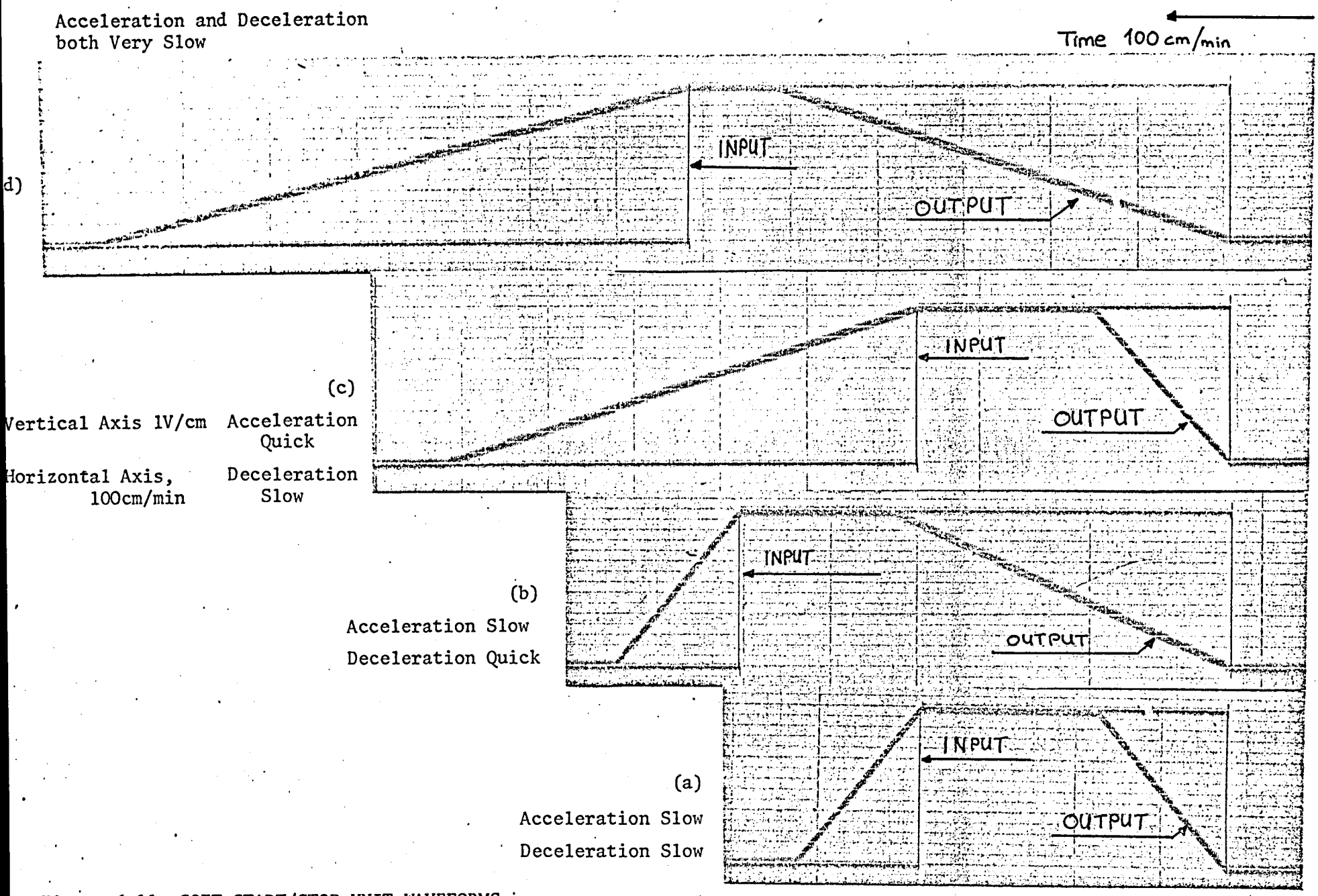


Figure 6.11: SOFT START/STOP UNIT WAVEFORMS

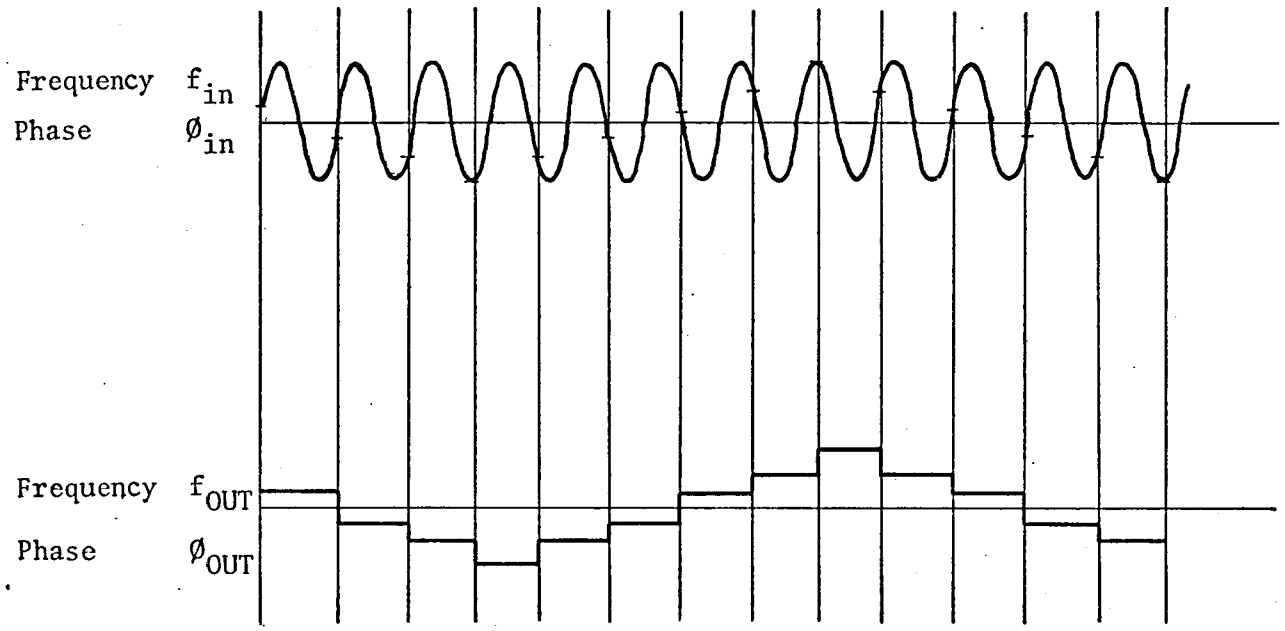


Figure 6.12: GENERATION OF LOW FREQUENCY SINE WAVE BY SAMPLE AND HOLD ACTION

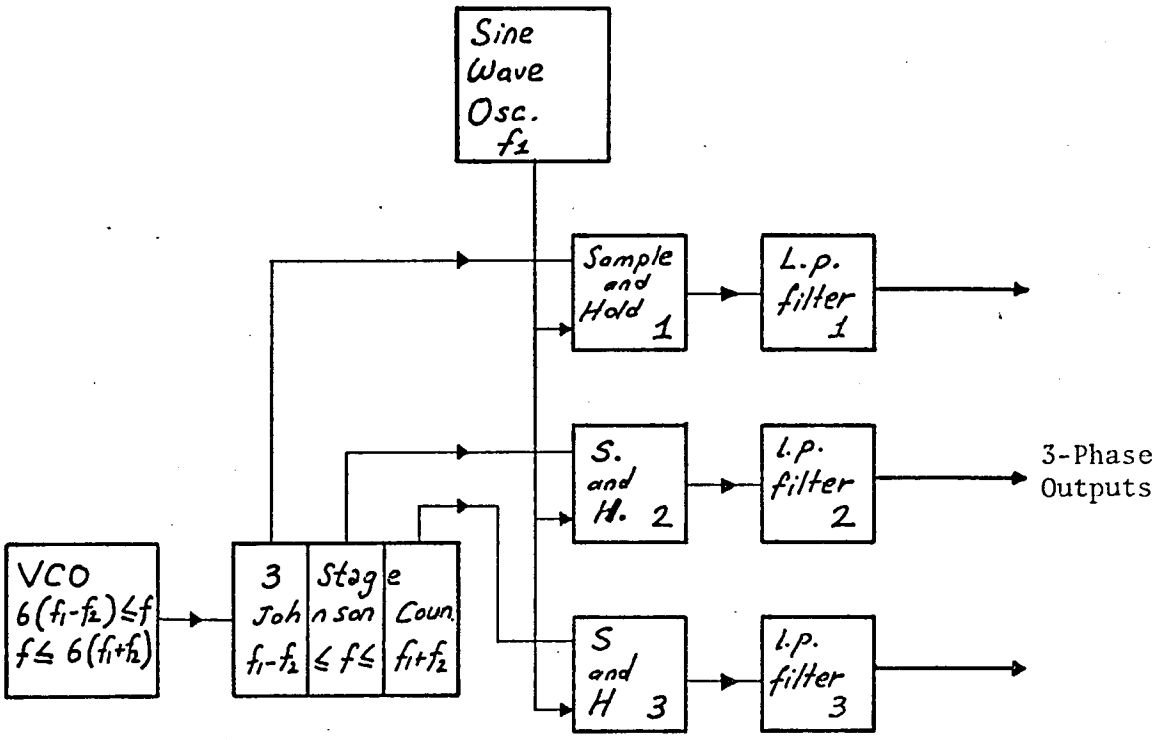


Figure 6.13: BLOCK DIAGRAM OF A 3-PHASE OSCILLATOR

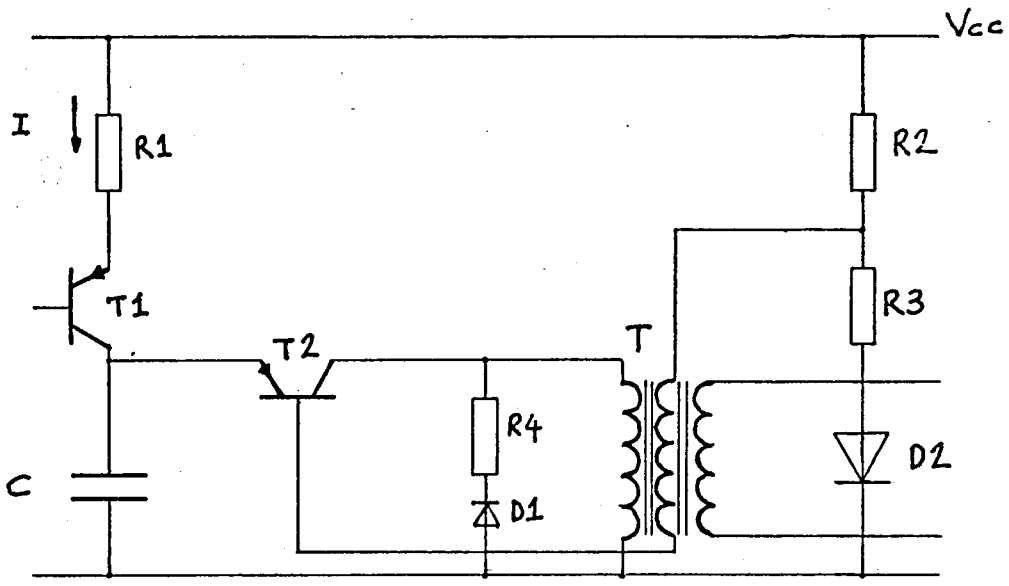


Figure 6.14: VOLTAGE CONTROLLED OSCILLATOR

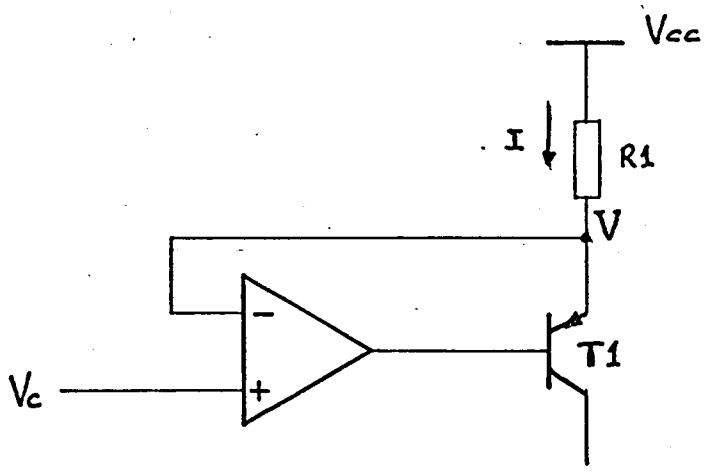
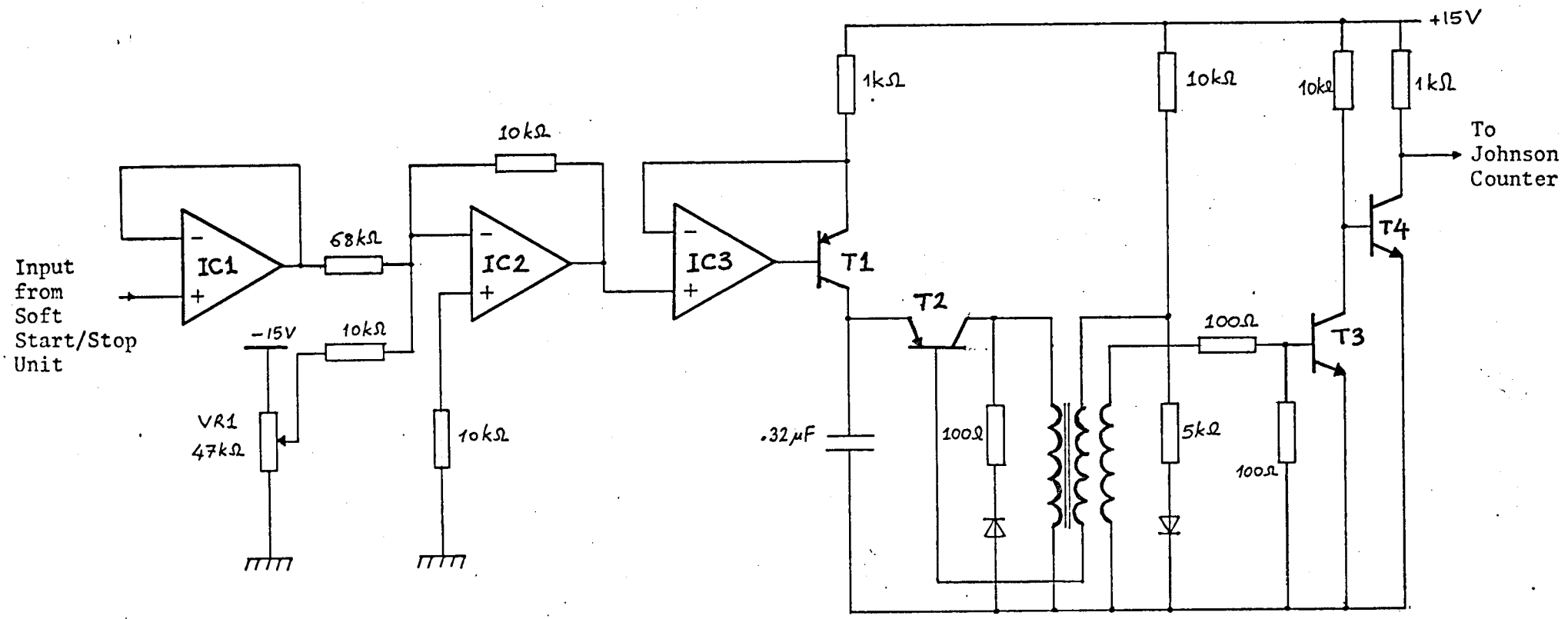
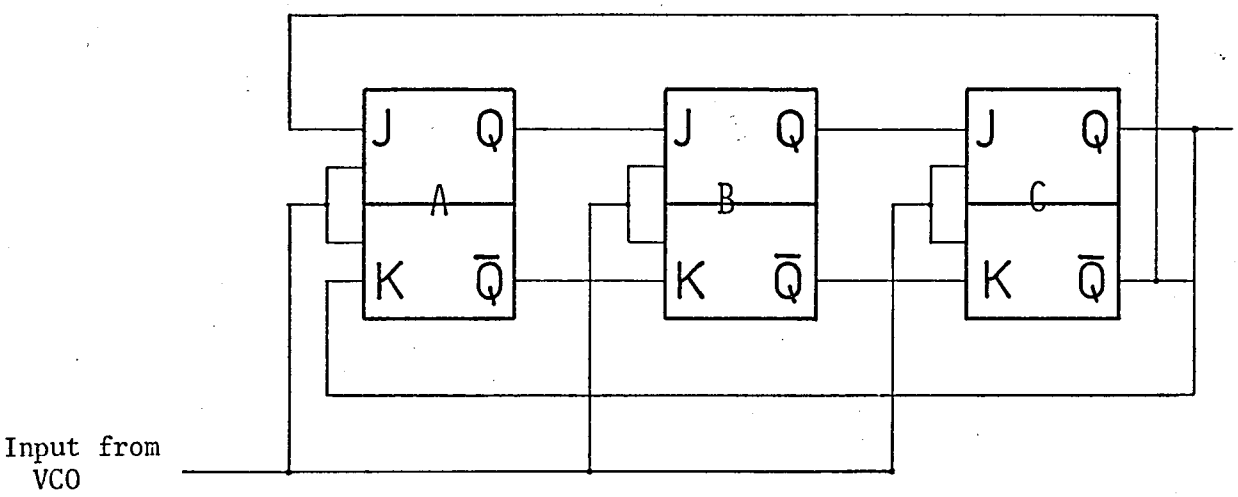


Figure 6.15: VOLTAGE FOLLOWER

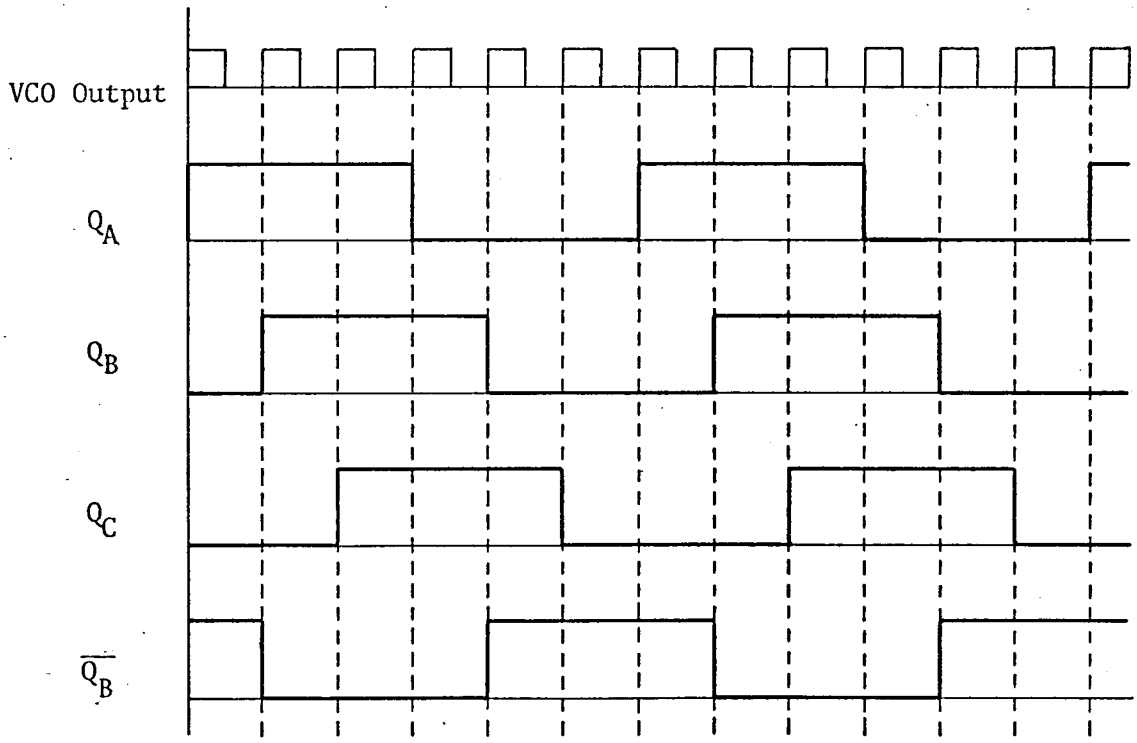


Ferrite E Core
FX1239, each winding has
35T of 30 swg wire
IC1, 2 and 3 - 741 op-amps

Figure 6.16: CIRCUIT DIAGRAM OF VCO



(a) 3-Stage Johnson Counter



(b) Waveforms at Various Points

Figure 6.17: JOHNSON COUNTER

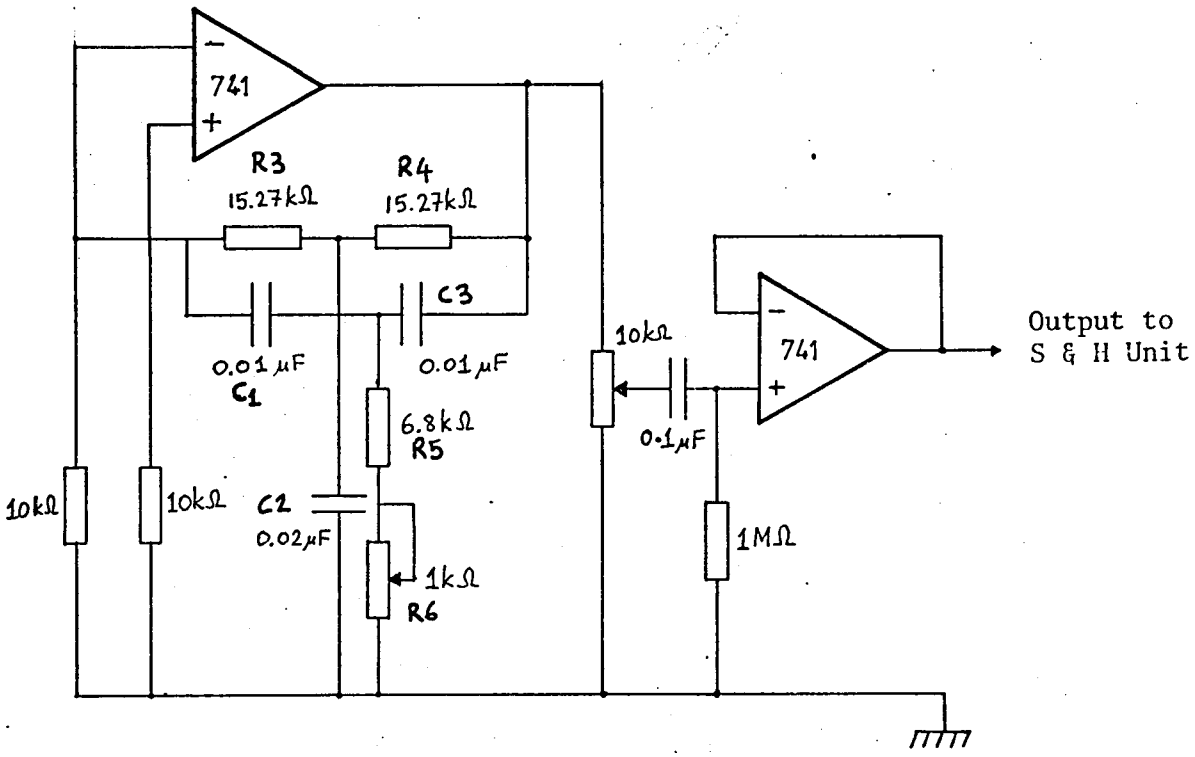
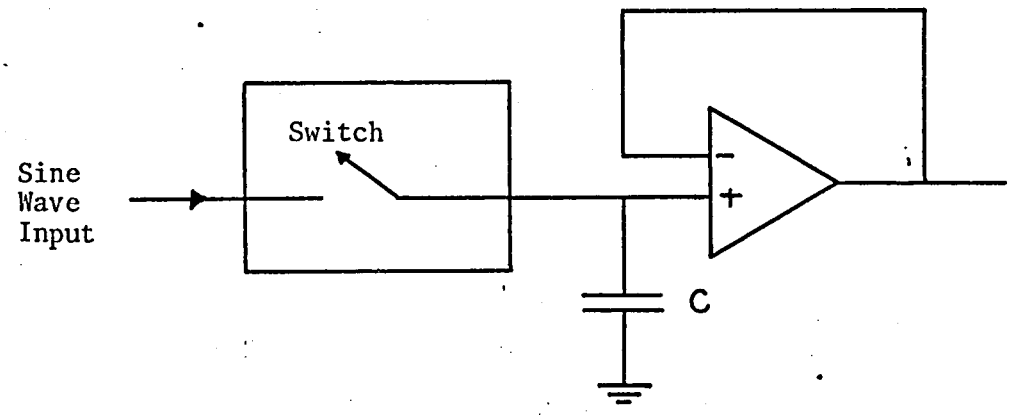
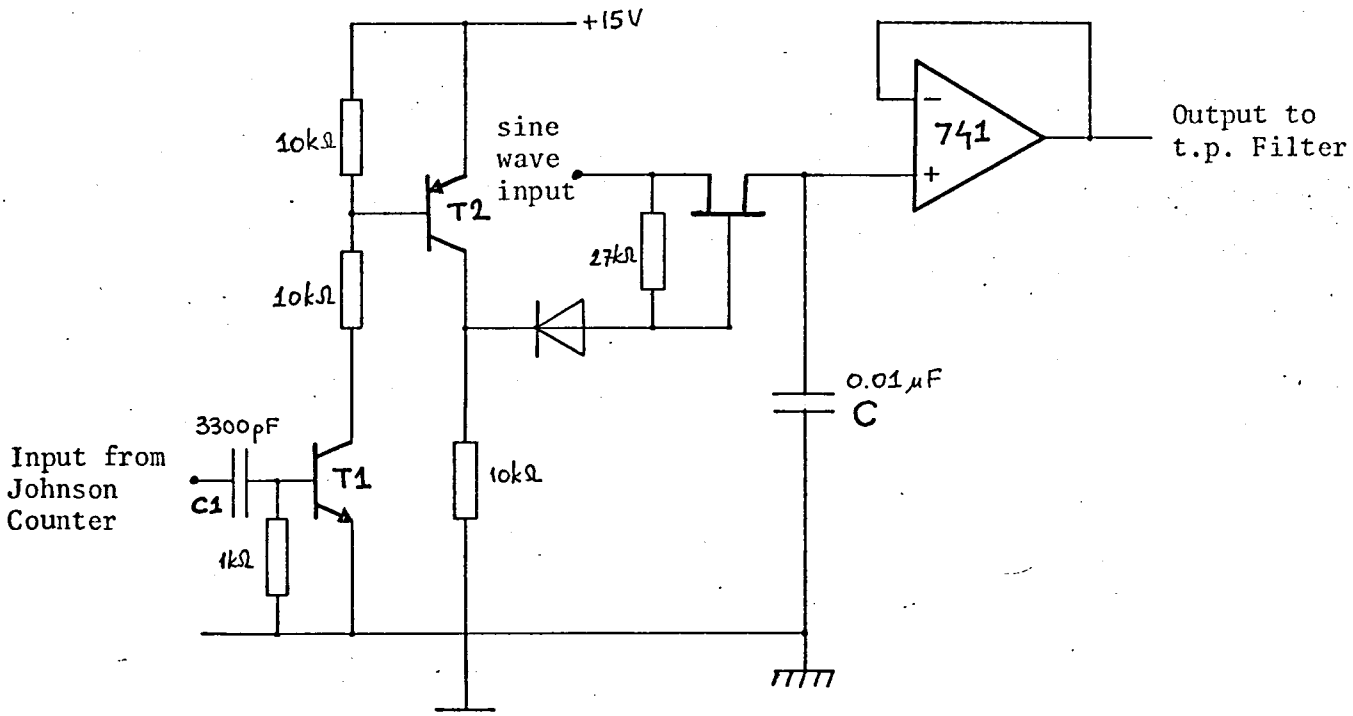


Figure 6.18: SINE WAVE OSCILLATOR



(a) Block Diagram



(b) Circuit Diagram (Three needed, one for each Phase)

Figure 6.19: SAMPLE AND HOLD CIRCUIT

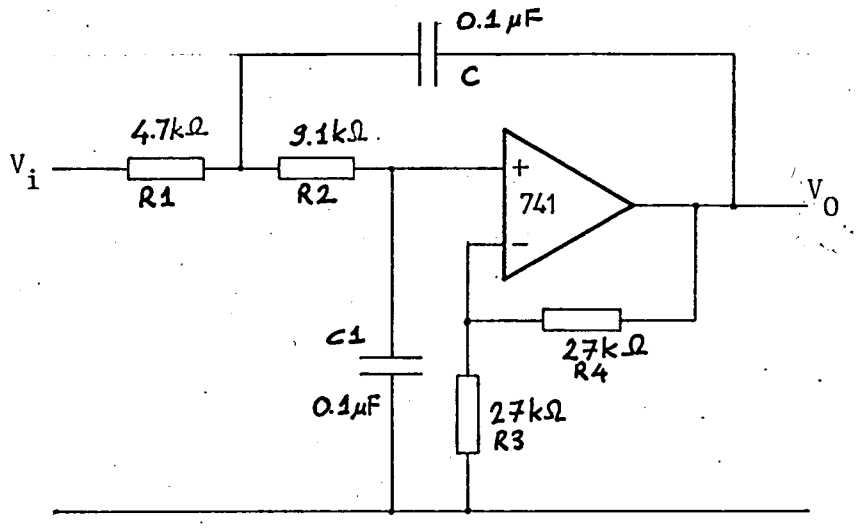


Figure 6.20: SECOND ORDER LOW PASS BUTTERWORTH FILTER

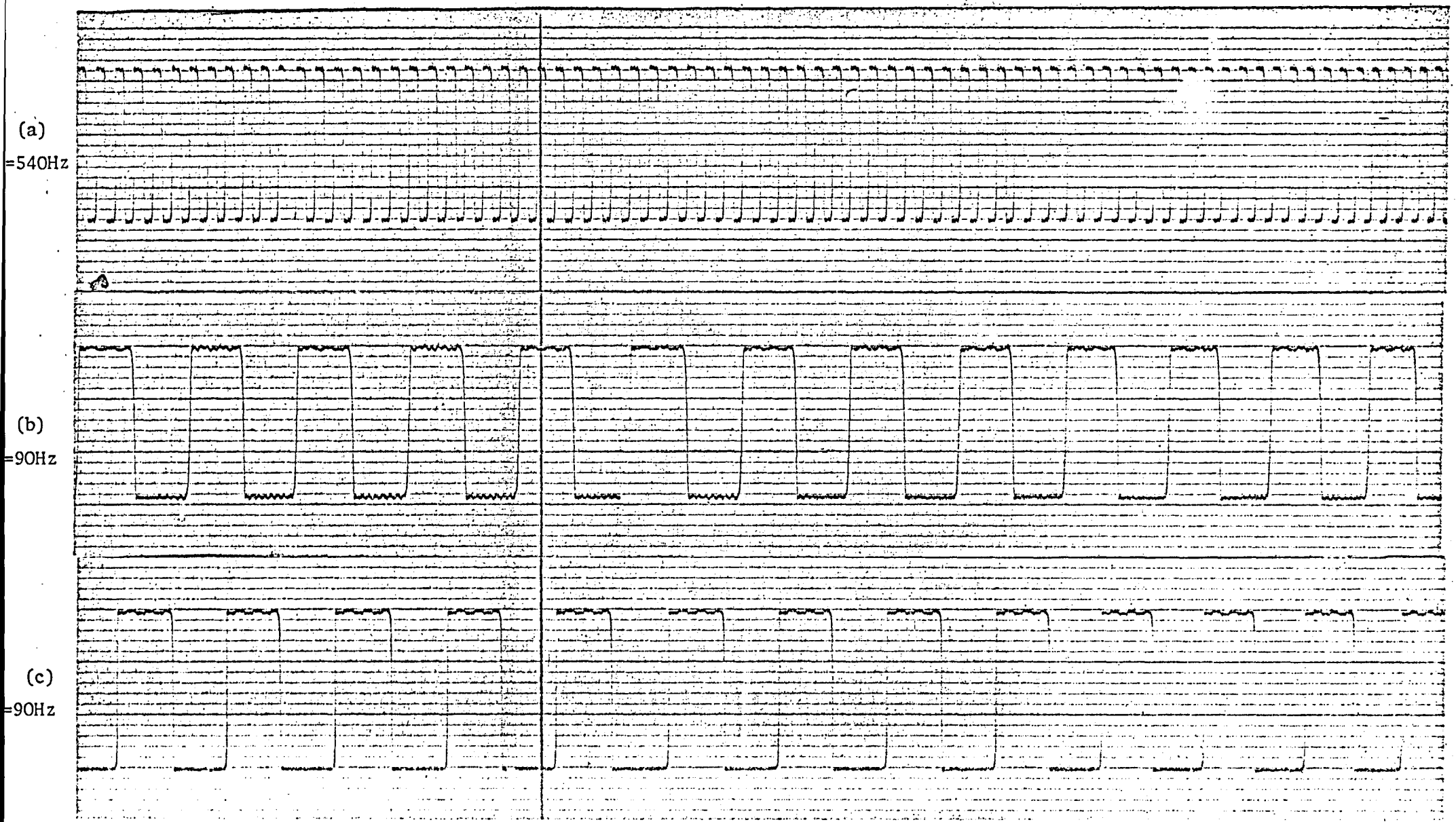


Figure 6.21: JOHNSON COUNTER INPUT AND TWO OUTPUT WAVEFORMS

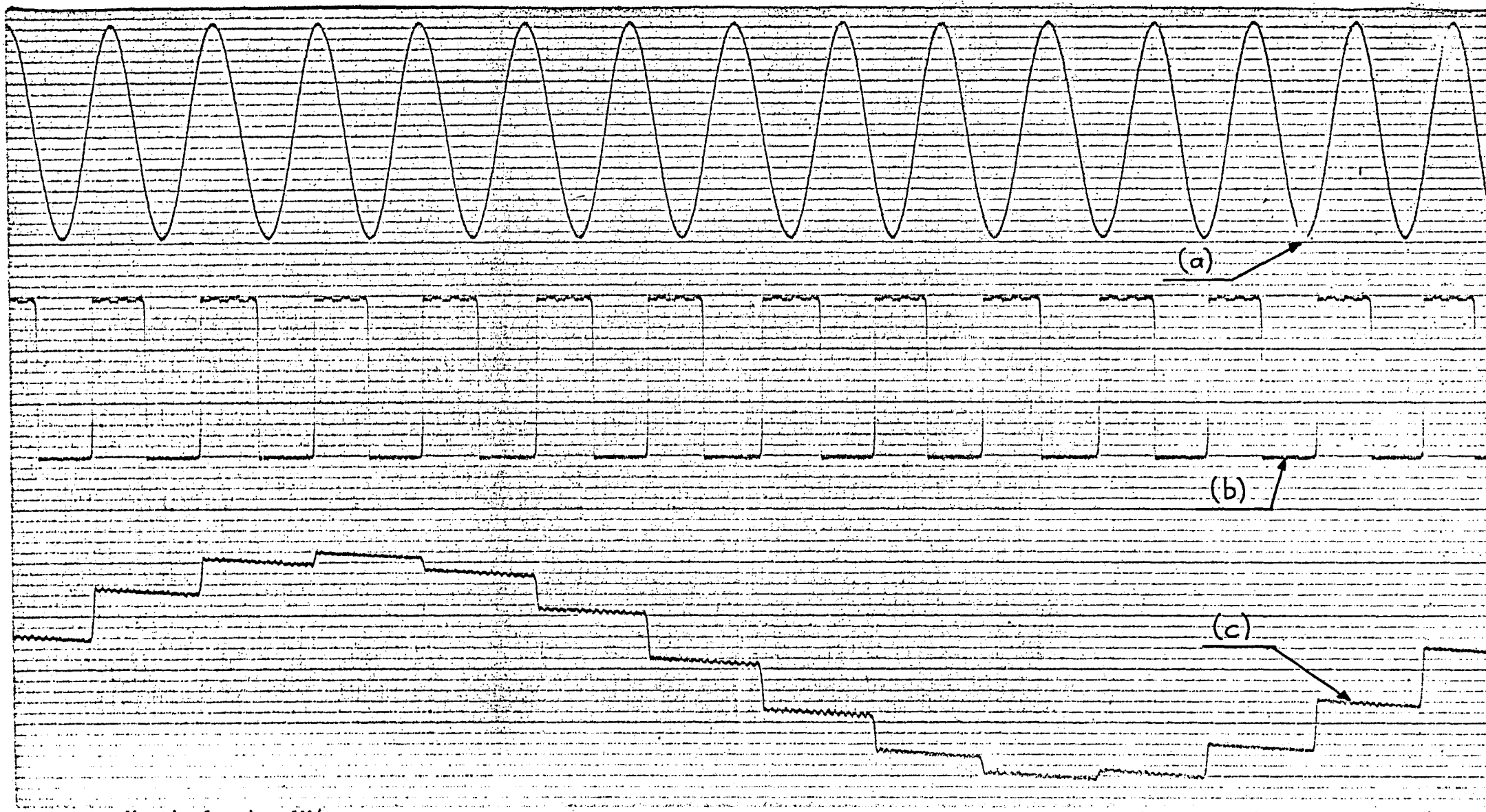


Figure 6.22: SAMPLE AND HOLD CIRCUIT WAVEFORMS
(a) Sine Wave Input, f=100Hz
(b) Square Wave Input from Johnson Counter f=90Hz
(c) Output f=10Hz

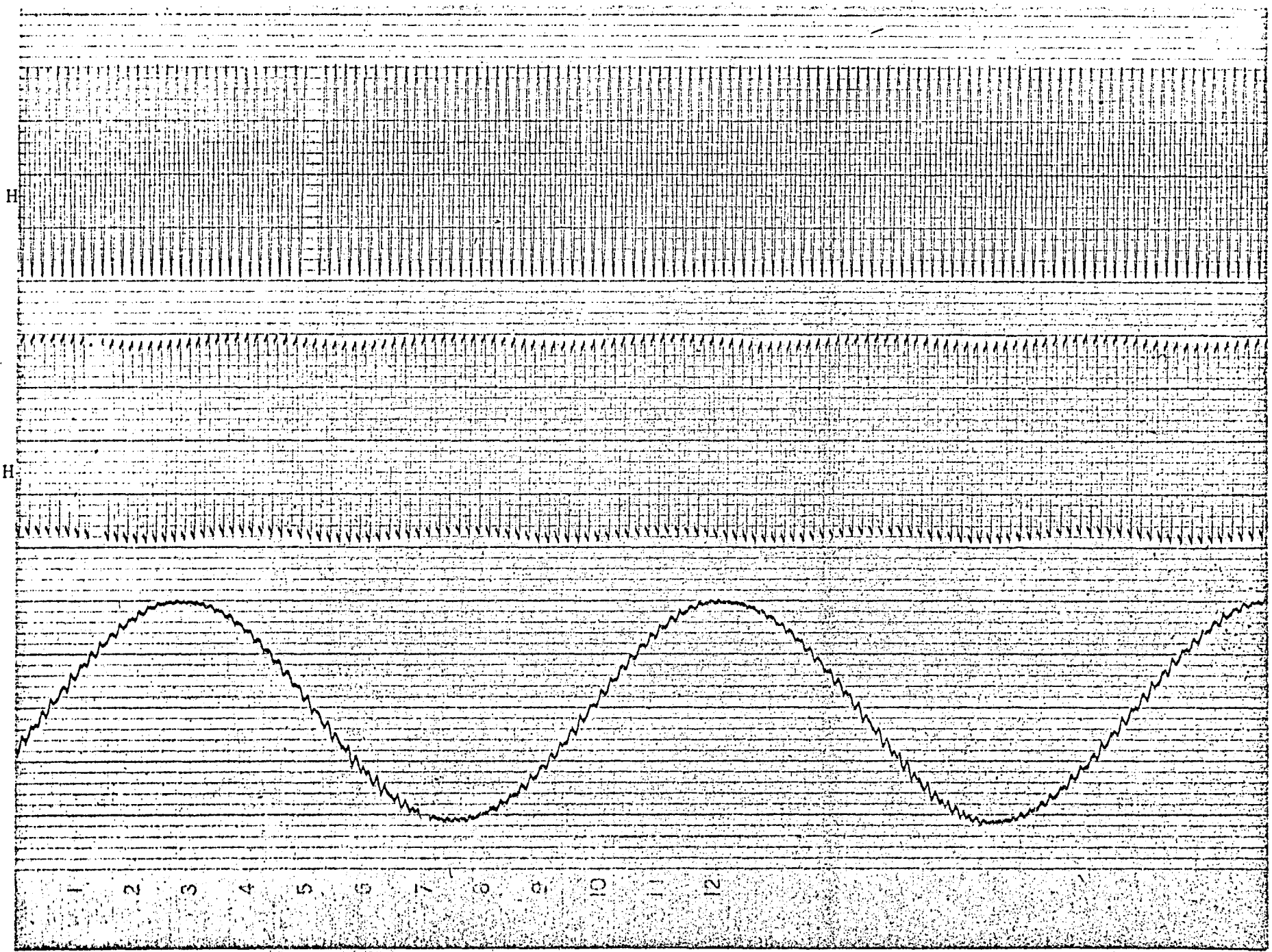
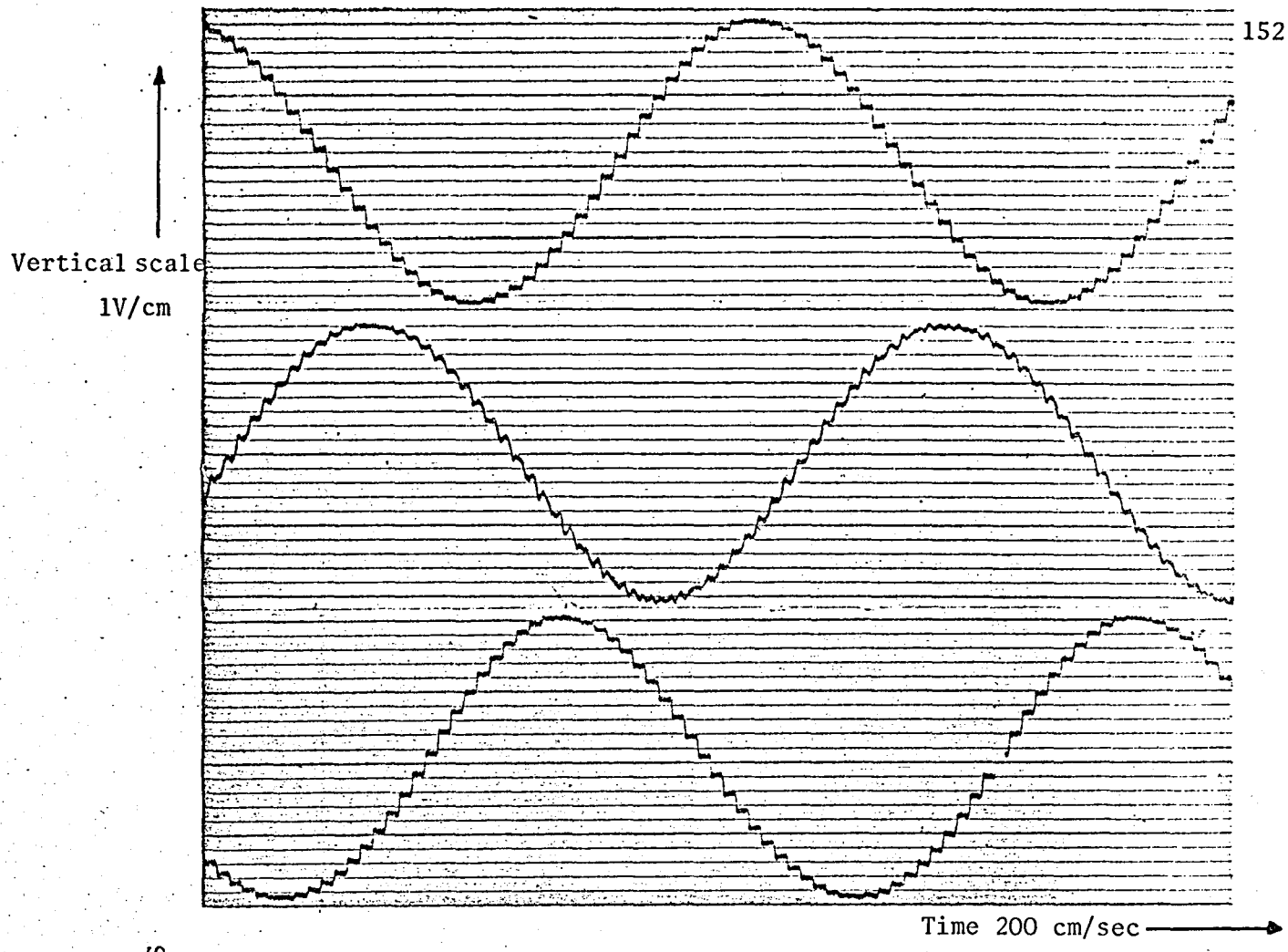


Figure 6.23: SAMPLE AND HOLD CIRCUIT WAVEFORMS



(a) Frequency = 25Hz

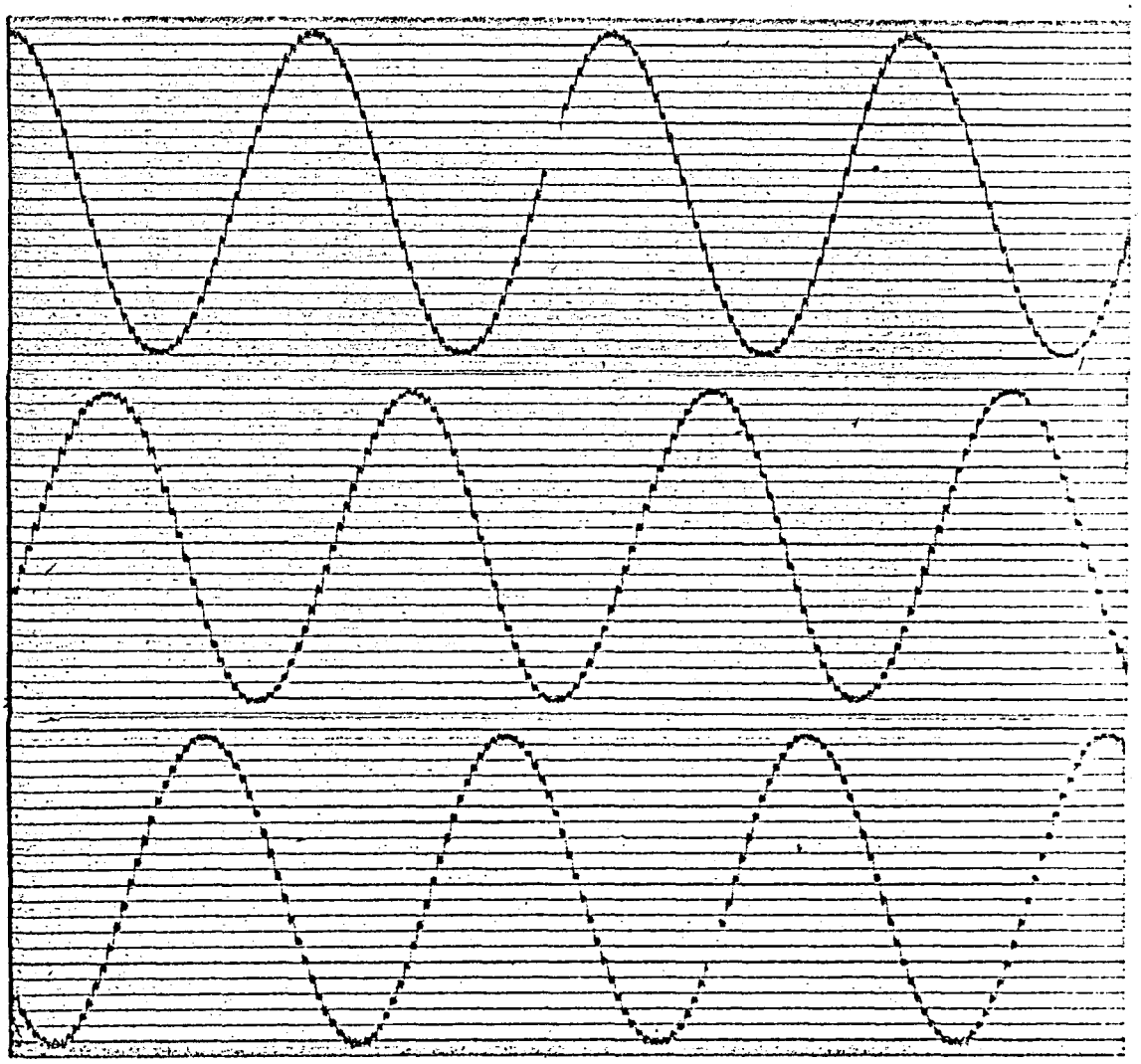


Figure 6.24: OUTPUTS OF THE THREE SAMPLE AND HOLD UNITS

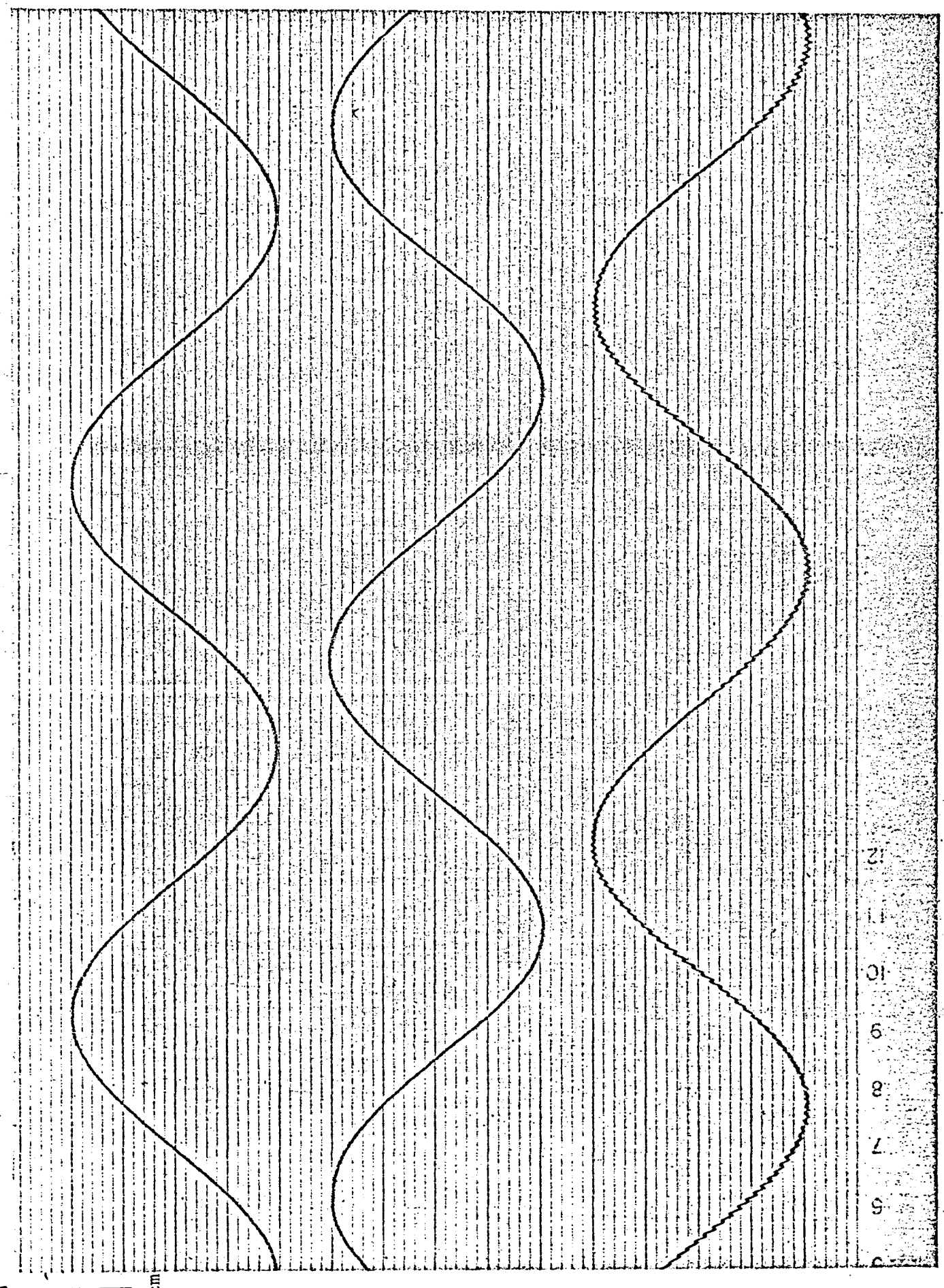
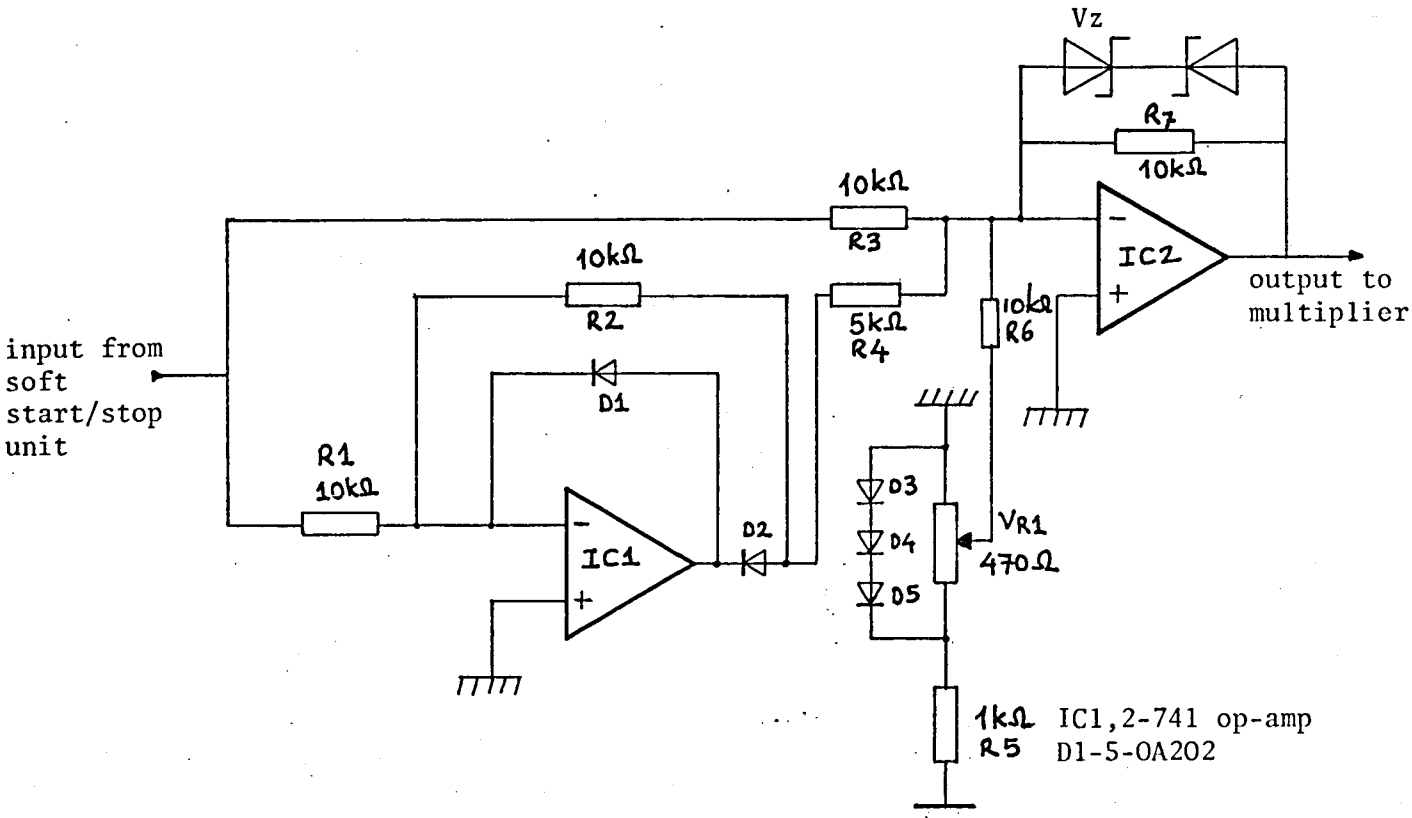
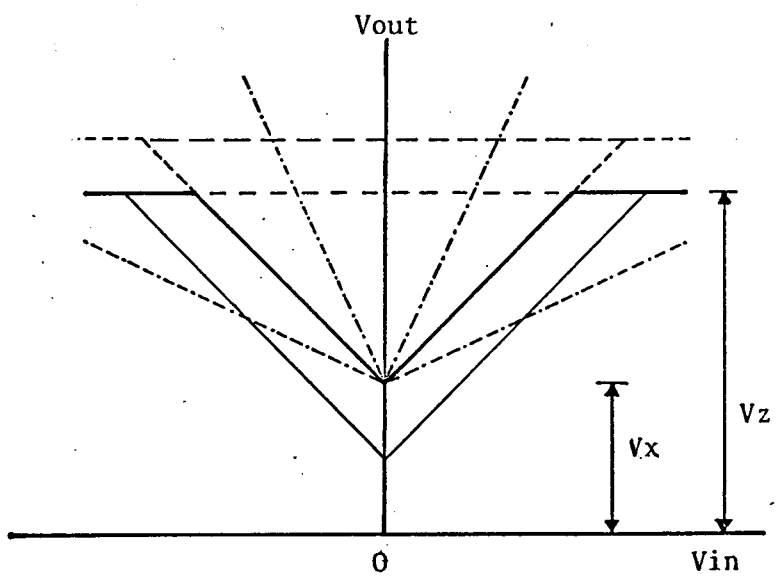


Figure 6.25: OUTPUT WAVEFORMS OF THE THREE L.P. FILTERS



(a) Circuit Diagram



(b) Characteristics

Figure 6.26: V/f CONTROL UNIT

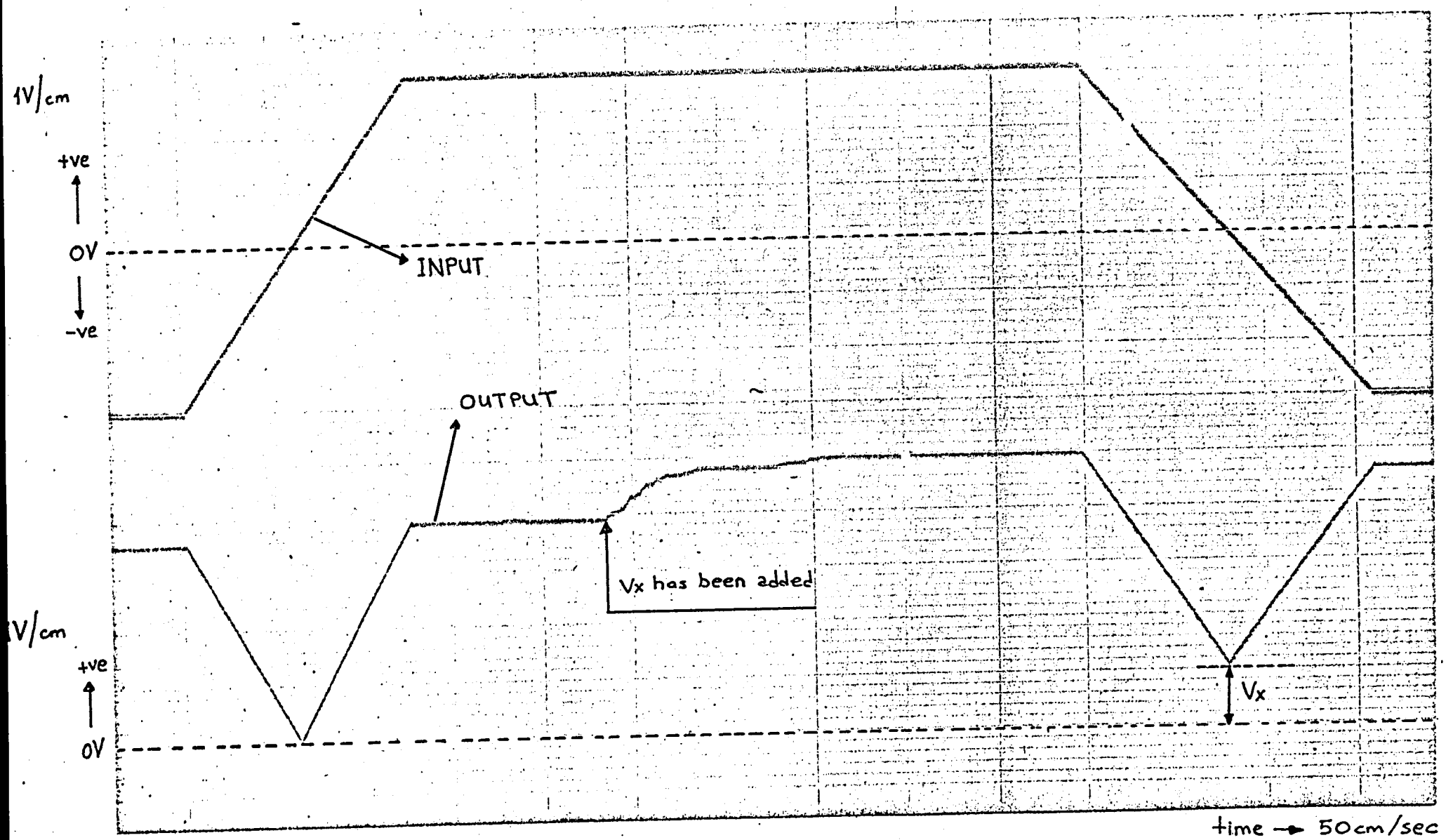


Figure 6.27: V/f CONTROL UNIT INPUT AND OUTPUT WAVEFORMS

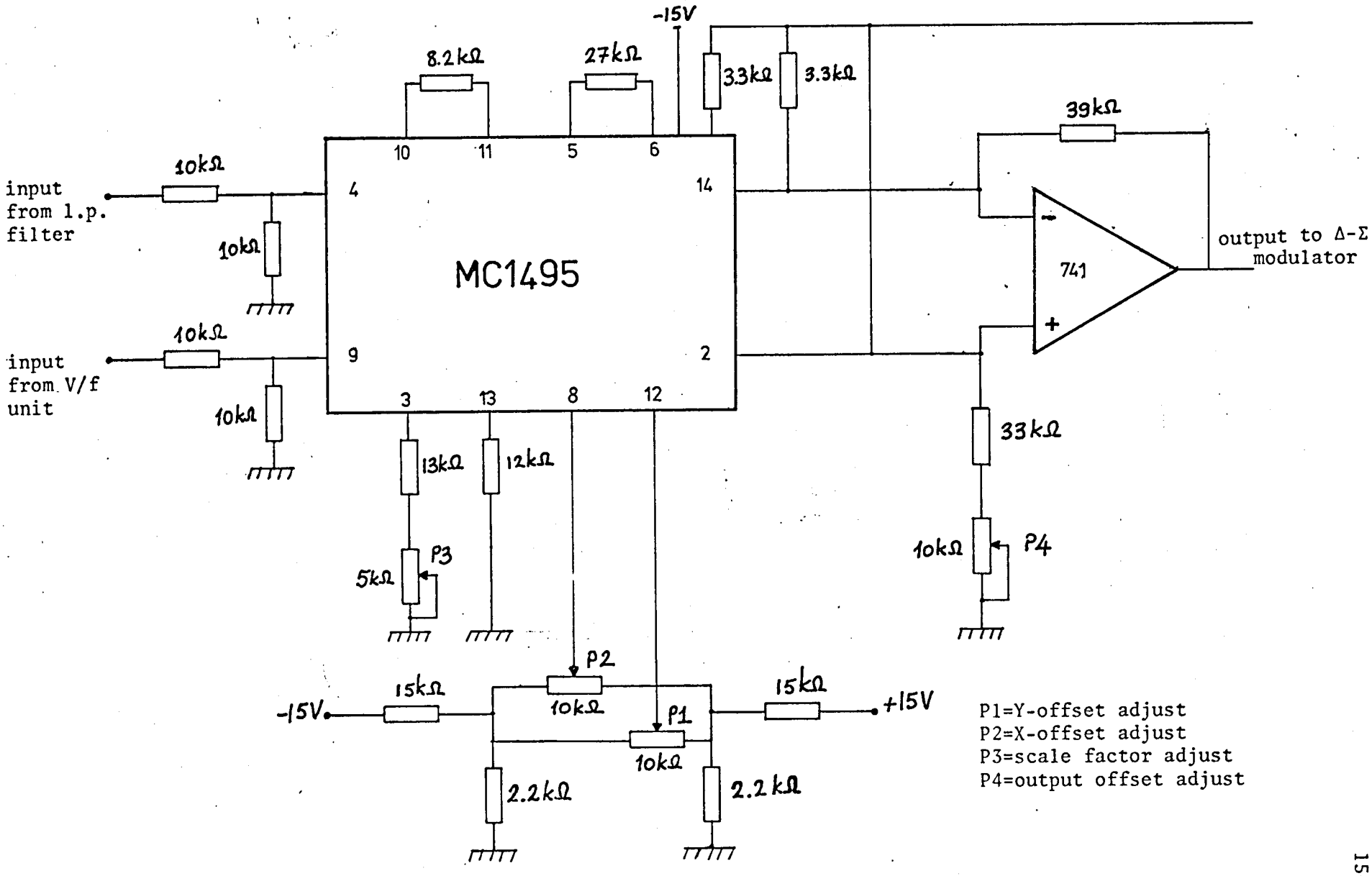


Figure 6.28: MULTIPLIER UNIT (Three needed, one for each phase)

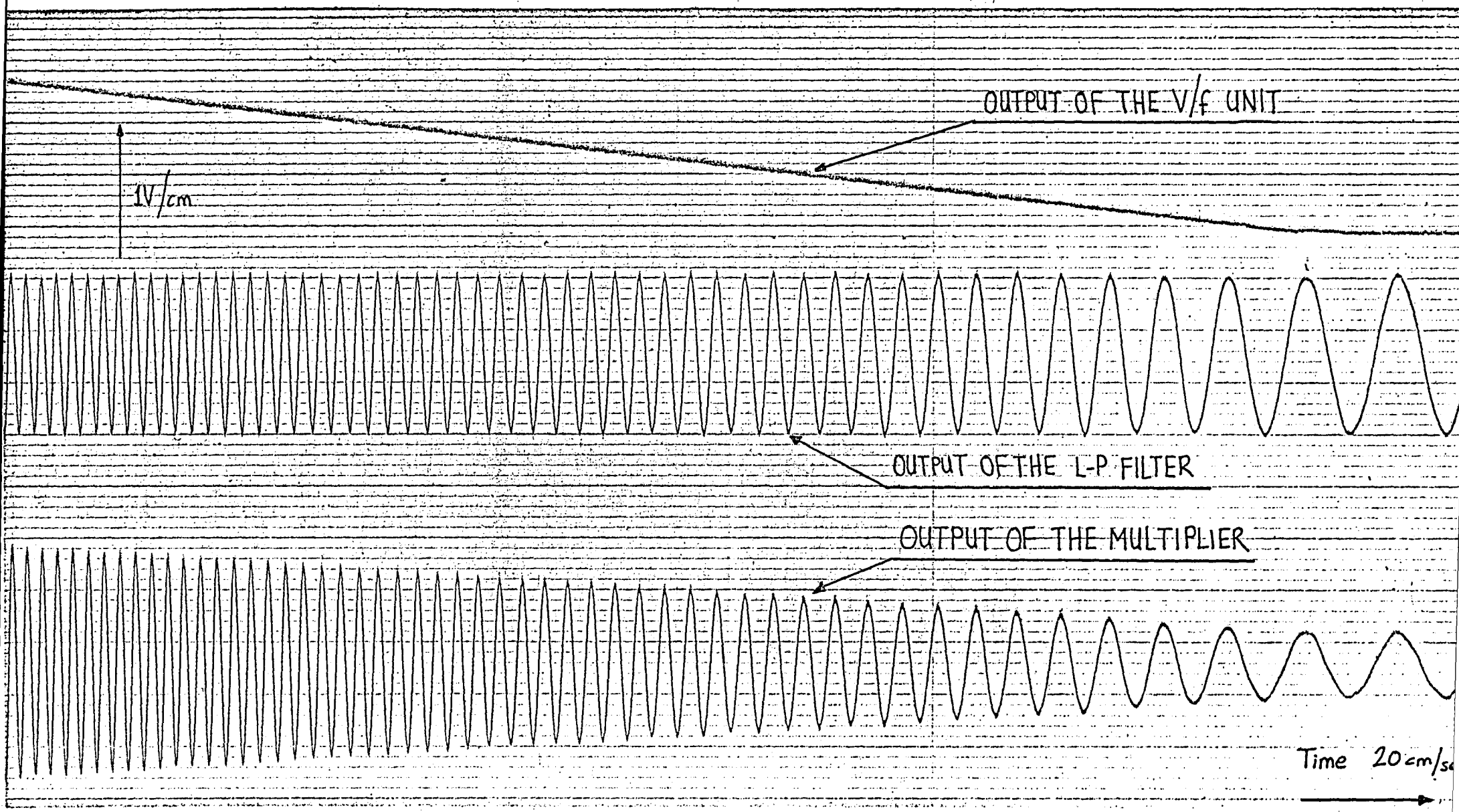


Figure 6.29; ACTION OF THE MULTIPLIER UNIT

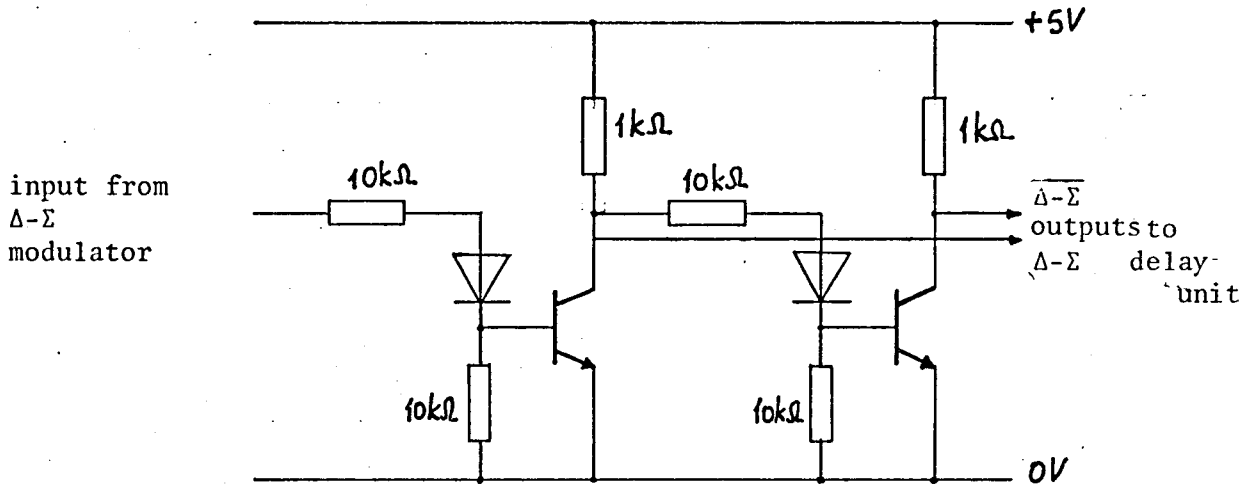
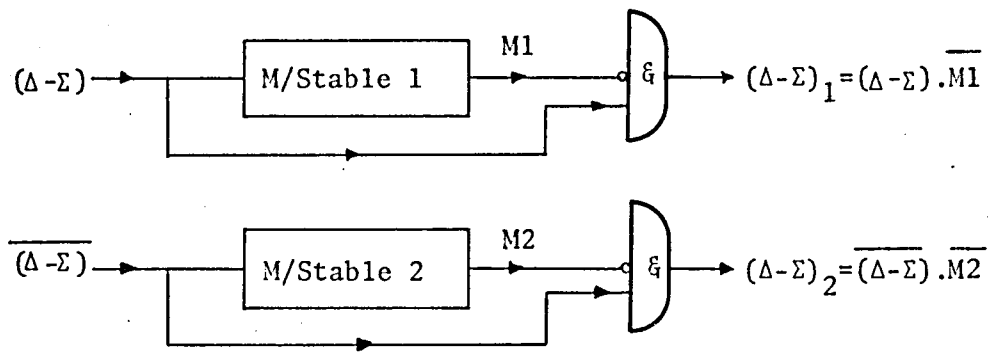
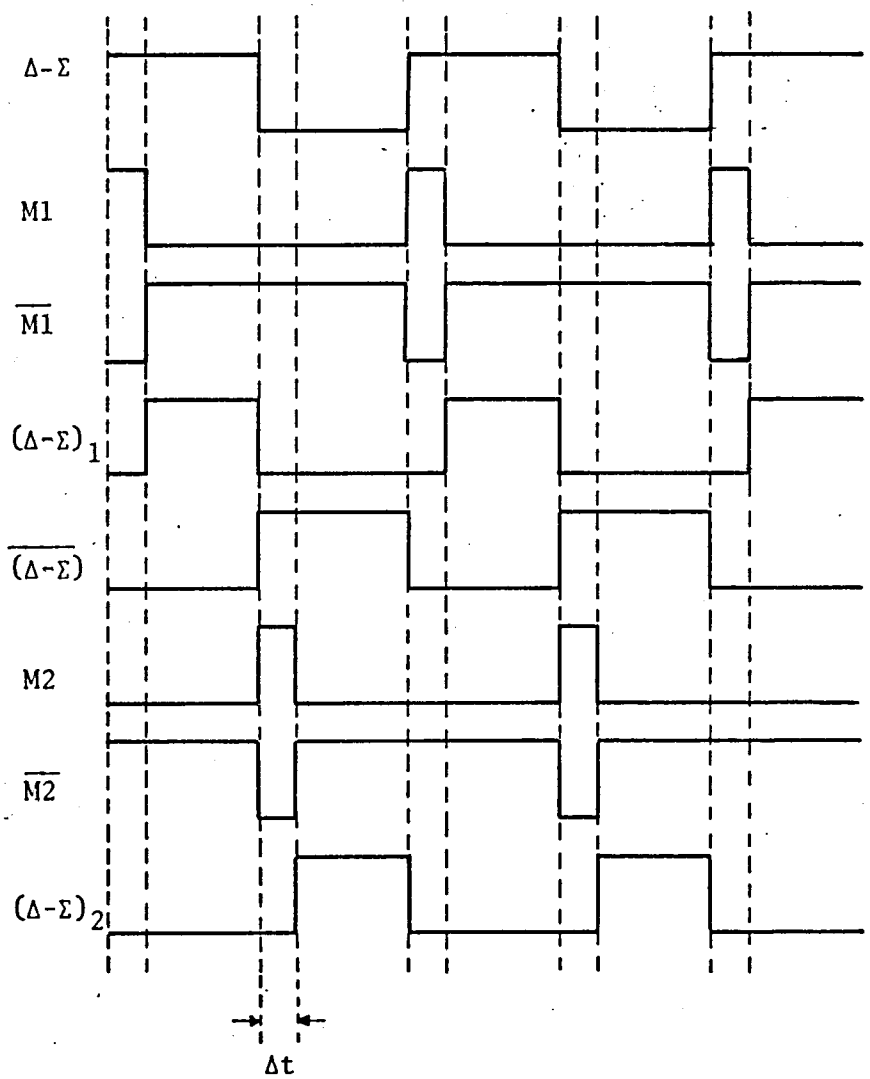


Figure 6.30: INTERFACE CIRCUIT (3 required)



(a) Block Diagram



(b) Waveforms

Figure 6.31: BLOCK DIAGRAM OF DELAY UNIT AND WAVEFORMS

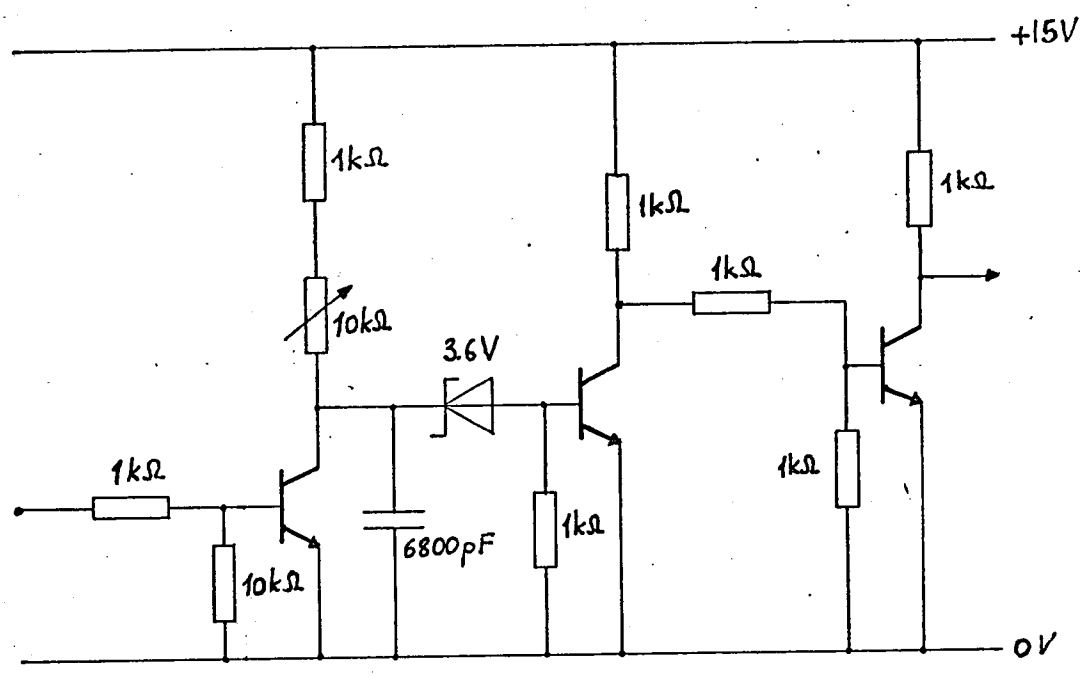
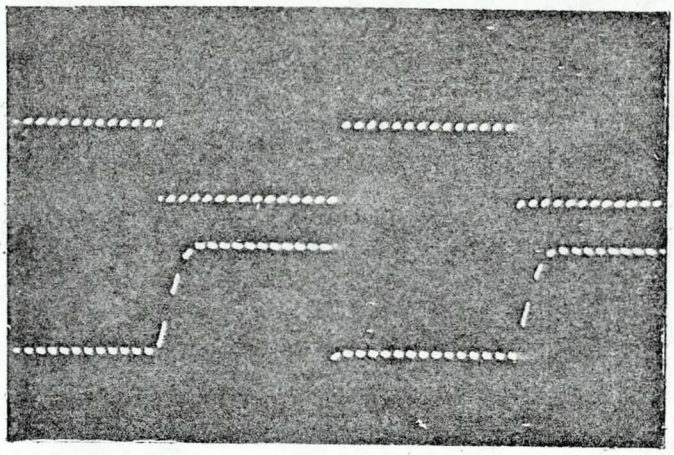


Figure 6.32: DELAY UNIT (6 required)

upper 2V/cm

lower 2V/cm



Vin

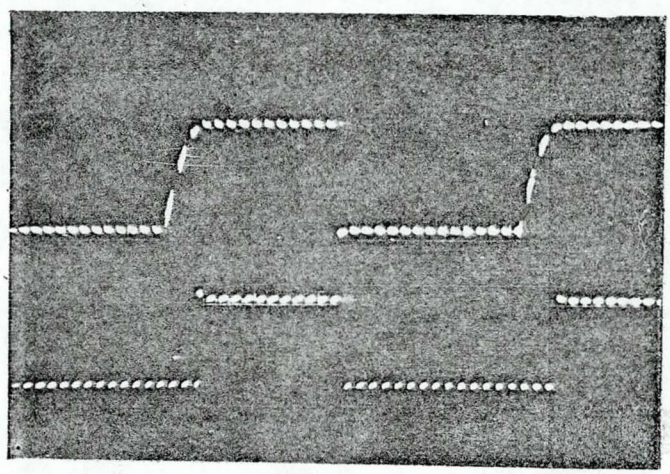
Vcapacitor

Time
50 μs/cm

(a) The Input and Capacitor Voltage Waveforms

upper 2V/cm

lower 5V/cm



Vcapacitor

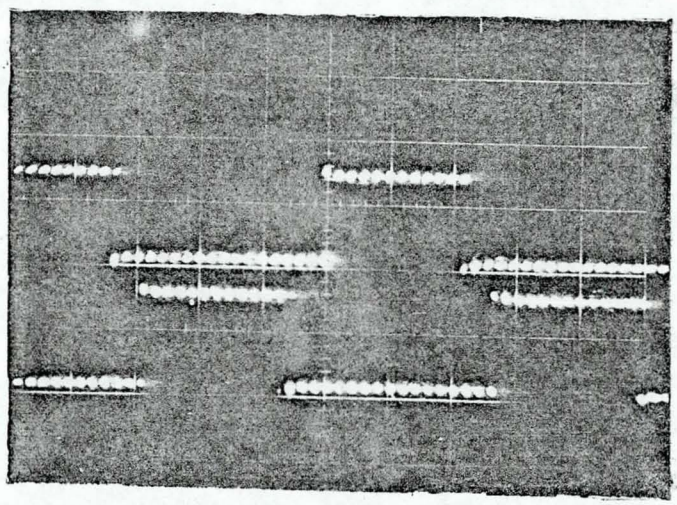
Vout

Time
50 μs/cm

(b) The Capacitor Voltage and Output Waveforms

upper 2V/cm

lower 2V/cm



$(\Delta-\Sigma)_1$

$(\Delta-\Sigma)_2$

Time
50 μs/cm

(c) Two Output Waveforms
Delay Time = 20 μs

Figure 6.33: ACTION OF DELAY UNIT (Oscilloscope in "chop" mode)

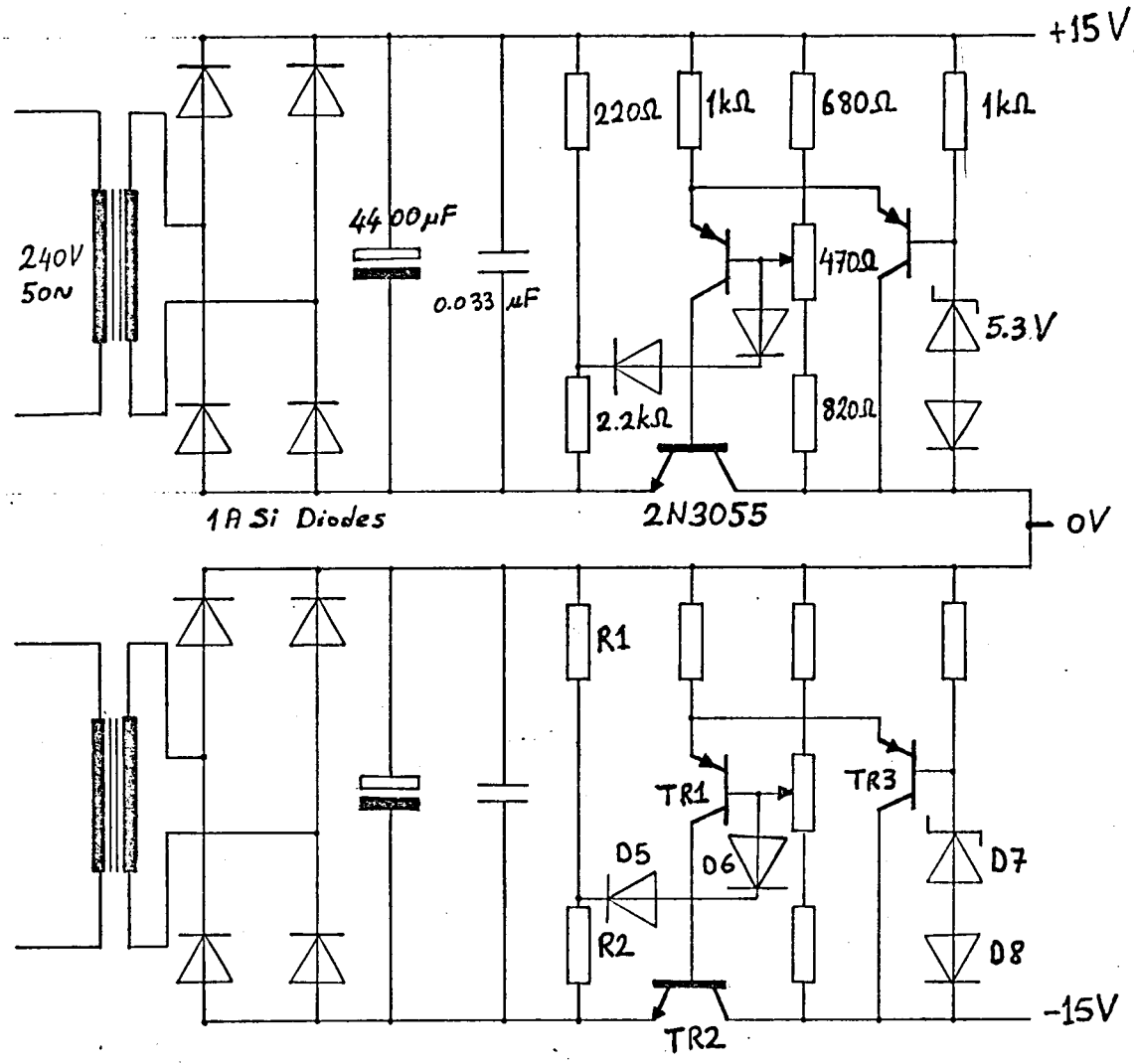


Figure 6.34: ±15V SUPPLY

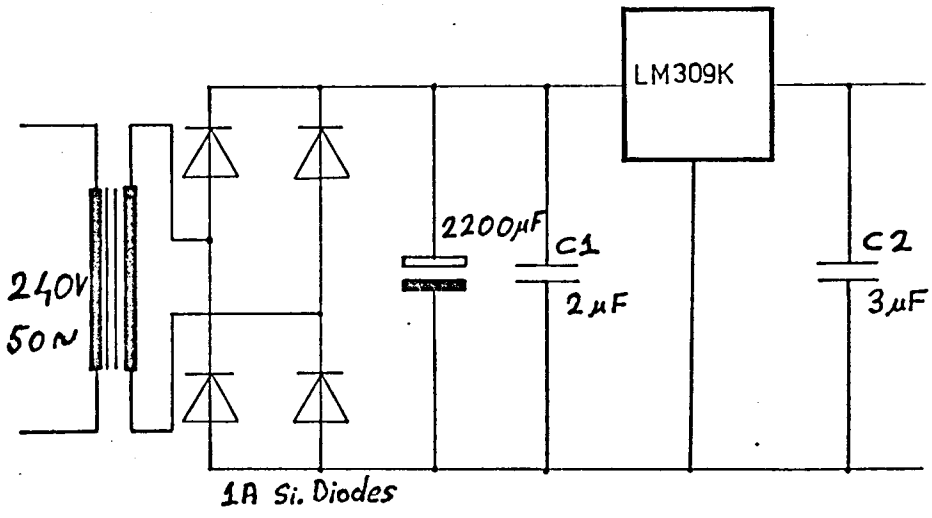


Figure 6.35: 5V/1A SUPPLY

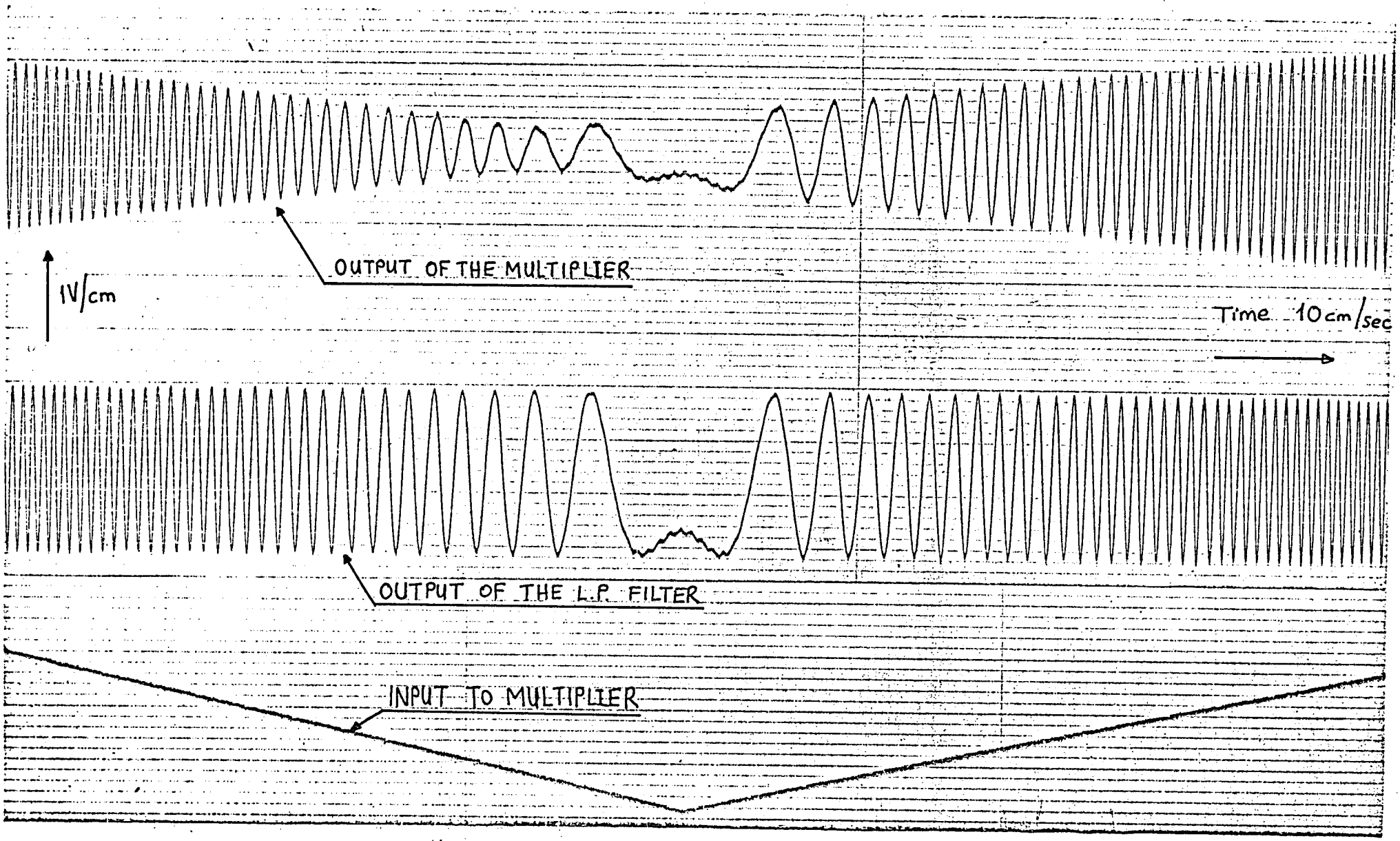


Figure 6.36: PERFORMANCE OF CONTROL UNIT

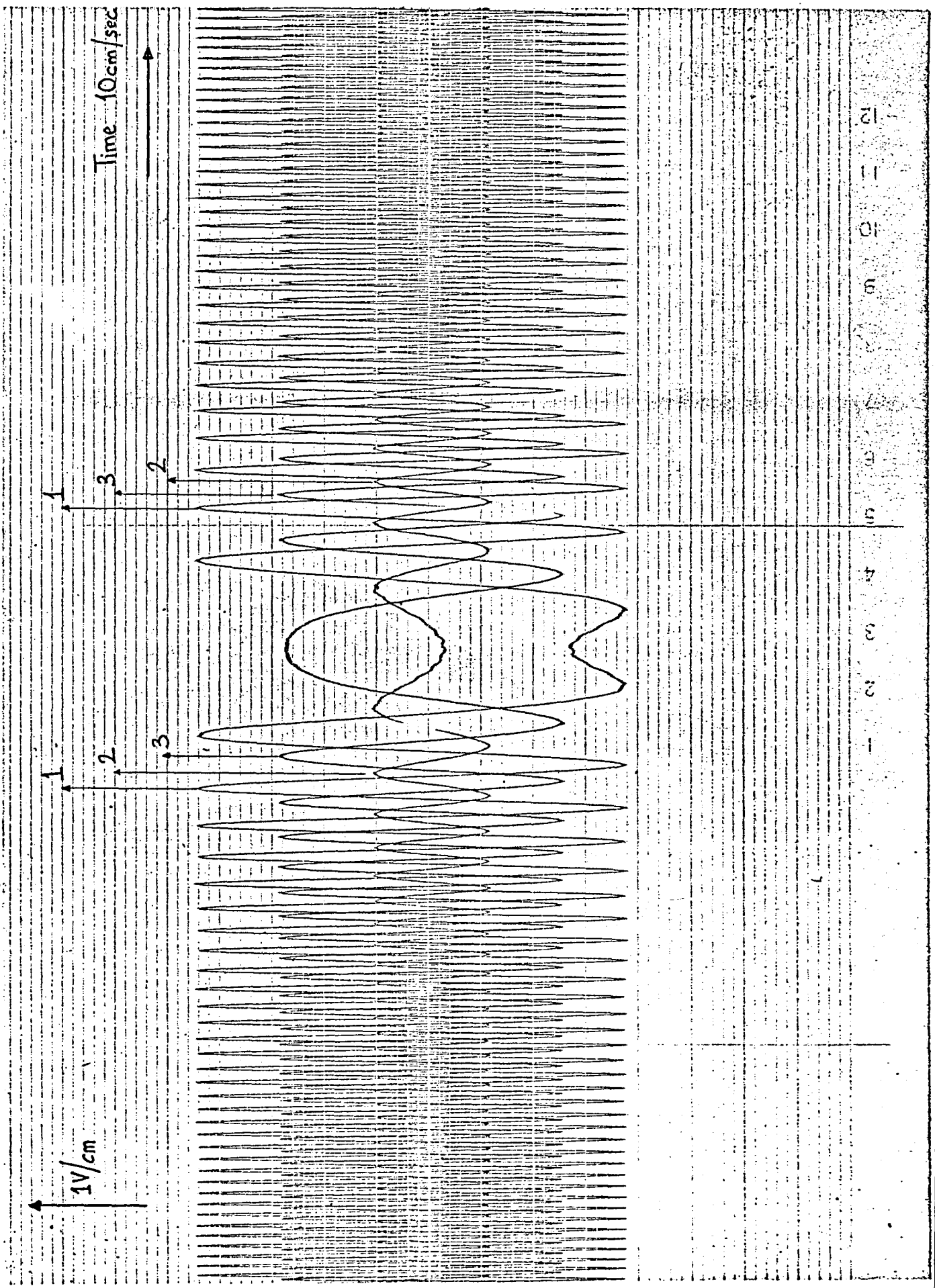


Figure 6.37: OUTPUTS OF THREE LOW PASS FILTER

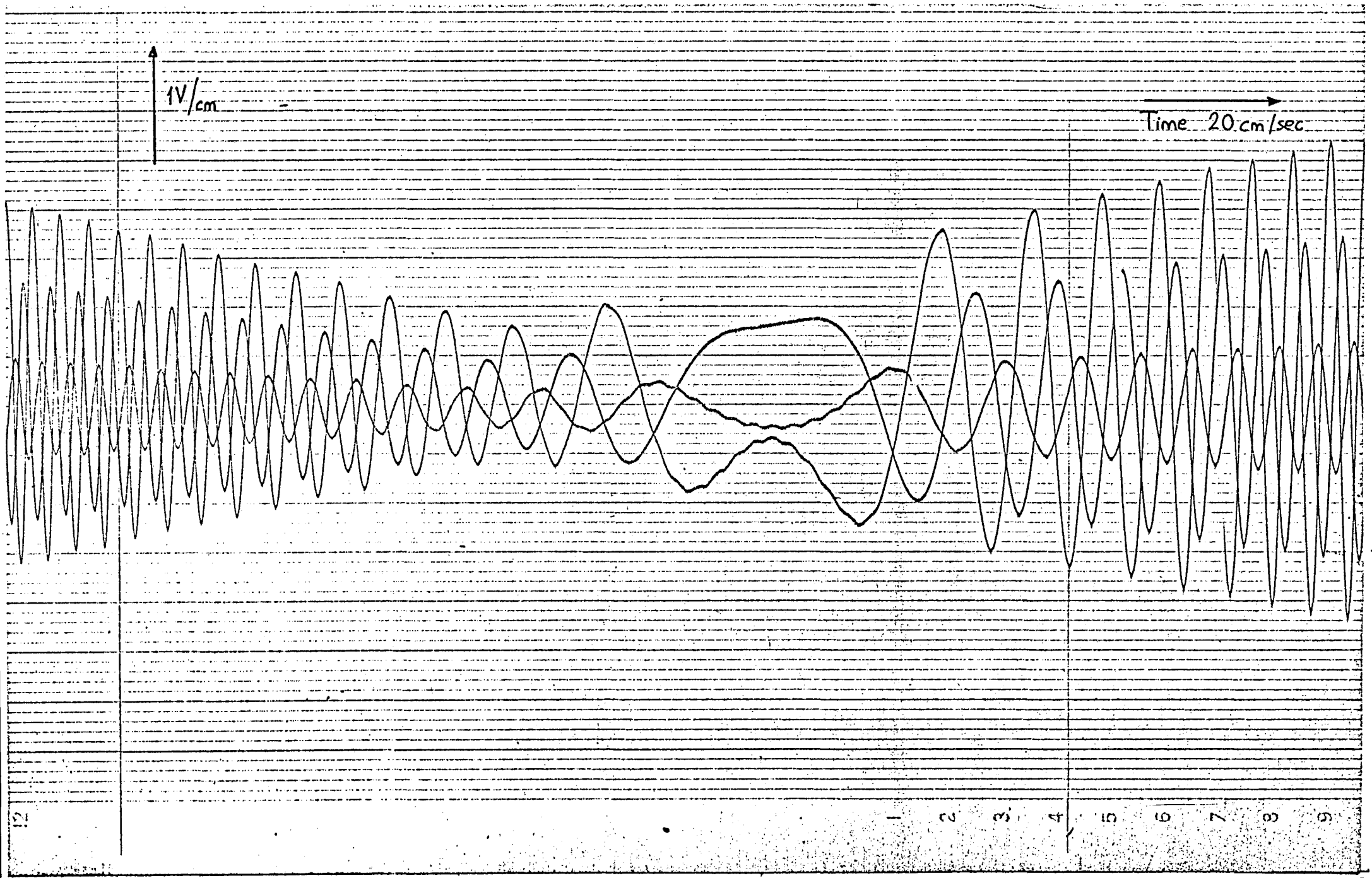


Figure 6.38: OUTPUTS OF THREE MULTIPLIERS

CHAPTER 7

DRIVER AND INVERTER DESIGN

This chapter is concerned with the design of a satisfactory drive unit and inverter for amplification of the delta-sigma modulated signals before these are fed to the motor. Since the clock frequency of the modulated signal should be as high as possible, to achieve the best encoding, a transistorized inverter is best suited to this purpose, entailing a driver capable of switching the power transistors in the inverter such that switching losses are kept to a minimum and the different requirements presented by the power transistors are fully met. The power transistor switching characteristics are investigated to provide an appreciation of the problems involved and different driver requirements are derived. Practical circuits which meet these requirements are designed and tested. Various problems associated with the inverter design are also discussed.

7.1 TRANSISTOR SWITCHING CHARACTERISTICS

7.1.1 Transistor in "On" and "Off" Mode[24]

As opposed to thyristor switching, in which a small positive pulse suffices, switching on of transistors requires a sustained base drive to keep the device in continuous conduction. When a transistor is switched on, both its junctions are forward biassed, and the voltage $V_{CE}(SAT)$ across its terminals is low and only in the order of 0.4-1.0V. A large current may flow,depending on the base drive,and the power loss in the device is very low. The losses during the "on" period depend on the collector current, the bottoming voltage and the base voltage and current. Care must be taken under varying load conditions, since if the load requires more collector current and the base current is below the corresponding value, the device will try to meet the load requirement by climbing up the saturation curve. This will result in an increase in the saturation voltage and the device dissipation, and this in turn may result in device failure.

In the "off" mode the transistors are biassed beyond the cut-off region, and with only a very small leakage current flowing through the device almost all the supply voltage appears across it. Losses during the "off" mode are dependent on the leakage current I_{CO}, and at high temperatures this may be considerable. A careful design of suitable heatsinks minimises the possibility of device failure, by efficiently dissipating the heat created at the junctions.

7.1.2 Transistor During "Turn-On"[25]

The current and voltage waveforms of a transistor during turn-on are shown in Figure 7.1, with the transistor being switched on by a positive base current, I_B. The collector-emitter voltage V_{CE} immediately starts to decrease rapidly, and the collector current I_C starts to increase. Eventually, the rate of fall of V_{CE} drops considerably, but V_{CE} remains comparatively high because of the large I_C component due to discharge of the stray capacitance. This results in a high peak value for the turn-on dissipation (shown by the dotted line in Figure 7.1). Later, as I_C starts to fall V_{CE} also decreases, reaching ultimately the normal saturation voltage corresponding to the values of I_C and I_B.

In Figure 7.2, the effect of a faster rate-of-rise of base current I_B is investigated. Here, the initially fast rate of fall of V_{CE} is maintained, until V_{CE} reaches a lower level than in the previous case. In consequence, both the peak and the average values of the turn-on dissipation are reduced.

Figure 7.3 shows the same waveforms with a very fast-rising I_B, which overshoots somewhat. Here, V_{CE} falls quickly almost to the true saturation voltage of the transistor. Again, the turn-on dissipation peak and average values are greatly reduced.

From the above three examples, it follows that the most desirable conditions at turn-on are obtained when a transistor is driven by a base current with a fast leading edge and some overshoot.

7.1.3 Transistor During "Turn-Off"

The current and voltage waveforms during turn-off are shown in Figure 7.4. In practice, the V_{CE} waveform is determined principally by the collector circuitry. The transistor adds little to the damping effect of this circuitry, except at the beginning of the turn-off period when it delays the rise of V_{CE}.

The energy in the $I_C V_{CE}$ (turn-off dissipation) pulse is dependent on both the turn-off time and the waveform of the collector current during turn-off. This is shown as a broken line in Figure 7.4.

In Figure 7.5, the effect of increasing the negative base drive voltage is shown. As it can be seen, the turn-off energy is reduced. The emitter-base voltage V_{EB} may be increased to $V_{(BR)EBO}$, without any detrimental effect on the operation of high-voltage transistors, provided the reverse base-current ratings are not exceeded.

7.1.4 Driver Requirements

The driving waveforms must have very fast turn-on and turn-off times, corresponding to the high switching rate required of the power transistors incorporated in the inverter. Hence, the base current waveform must have a faster leading edge than that of the collector current waveform, entailing the use of faster transistors in the driver than in the inverter.

The forward current transfer ratio h_{FE} changes considerably with the collector current of the power transistor being driven. Figure 7.6 shows the variation of h_{FE} with I_C for a particular power transistor, and the considerable reduction at higher values of I_C is evident. The characteristic also depends on the case temperature of the power transistor, and the driver must be designed to be capable of providing sufficient base current for high values of collector current, taking the low value of h_{FE} into account. Otherwise, when the load requires excessive current from the inverter, the

power transistors, being short of base drive, will attempt to meet the requirement by climbing the saturation curve into the active region, resulting in a higher device dissipation and possible device failure.

As the collector current increases, the switching times of the power transistor change as shown in Figure 7.7. The delay unit (refer to section 6.2.7) must be adjusted accordingly, to provide sufficient delay so that a short circuit across the supply rails can be avoided.

Generally speaking, the transistor switch-on loss can be neglected compared with the switch-off loss, which is dependent on the turn-off time and the collector current waveform during switch-off. The turn-off time must be minimized to keep the switch-off loss to an acceptable level, and this may be achieved simply by supplying a reverse base current during switching from the "on" state to the "off" state. In this way, excess minority carriers present in the base region are swept quickly away and storage and fall times are reduced. It is thus necessary for the driver to be capable of providing reverse current through the base-emitter junction of the power transistor being driven.

Since high potentials exist on the inverter side, the driver must also be capable of providing electrical isolation so that the electronic circuitry is protected.

7.2 TRANSFORMER DRIVE

Of the several different ways available for driving transistors, transformer drive[26] offers the desirable property that the induced voltage is relative to a particular point, irrespective of the actual voltage held by that point. Also, since the secondary of a transformer is electrically isolated from the primary, it cannot have any effect on the potential levels there. Since the induced voltage in the secondary is proportional to the rate-of-change of flux linkage, the flux must change to provide a drive for the transistor.

The circuit configuration shown in Figure 7.8 may be used to provide a drive for the power transistors in the inverter. It is a simple push-pull circuit, with the transistors operated in the grounded emitter configuration. A square wave input to this circuit causes transistor T1 to conduct for half the time, while transistor T2 is blocking, and vice-versa. In this manner, the current from the supply flows alternately through the two sides of the transformer primary and produces a rectangular voltage across the secondary.

The behaviour of this circuit to a square wave input under no-load conditions may be determined by considering the equivalent circuit shown in Figure 7.9.a. When switch S is closed the conditions in the appropriate half of the primary may be expressed by

$$L \frac{di}{dt} + Ri = E \quad , \tag{7.1}$$

where R and L are respectively the resistance and the inductance of one half of the primary winding and i is the instantaneous value of the current.

Solution of equation (7.1) gives:

$$i = \frac{E}{R}(1 - e^{-\frac{R}{L}t}) \quad , \tag{7.2}$$

so that the self-induced primary voltage is

$$L \frac{di}{dt} = E \, e^{-\frac{R}{L}t} \quad ,$$

and the voltage induced in the secondary winding is,

$$V_2 = n \, E \, e^{-\frac{R}{L}t} \quad \text{where } n = \frac{n_2}{n_1} = \frac{\text{secondary turns}}{\text{primary turns}}$$

and assuming R<<L

$$i = \frac{E}{L}t \quad \text{and} \quad V_2 = n \, E \quad .$$

This analysis shows that primary current rises linearly and the output voltage is rectangular in form. For the conditions considered i is the magnetizing current, and may be expressed as i_m.

The effect of load may be investigated with the help of Figure 7.9.b.

Considering, for the sake of simplicity, a resistive load across the secondary winding:

$$i_m + i_1 = i \tag{7.3}$$

$$Ri + R_1 i_1 = E \tag{7.4}$$

$$Ri + L\frac{di_m}{dt} = E \tag{7.5}$$

and solving for i gives:

$$i = \frac{E}{R}\left[1 - e^{\frac{-RR_1}{L(R+R_1)}t}\right] + \frac{E}{R+R_1} \cdot e^{\frac{-RR_1}{L(R+R_1)}t} \tag{7.6}$$

The first part of equation (7.6) is the magnetizing current and the second part the current in the load. Hence the secondary voltage is:

$$V_2 = \frac{nER_1}{R_1+R} e^{\frac{-RR_1}{L(R+R_1)}t} \quad . \tag{7.7}$$

These results indicate that the effect of the load is to reduce the maximum value of V_2 to $R_1/(R+R_1)$ of that on no-load, and to cause V_2 to fall from its maximum value somewhat more slowly than when the no-load condition exists.

If the time of contact closure (of the switch) is sufficiently short, the primary current may be represented approximately by:

$$i = \frac{E}{R+R_1} + \frac{E}{L}t$$

and the collector current flowing in the transitors is as shown in Figure 7.10.a and 7.10.b, for a non-saturating transformer and a saturating transformer respectively. Since the transformer must not saturate (otherwise the voltage across the winding will collapse and the power transistor in the inverter being driven by the secondary will be short of base drive), the maximum flux density B_m must be held below the saturation level B_s. By Faraday's law,

$$V = \frac{d}{dt}(N\phi) \quad \text{and by integration,}$$

$$N\int_{\phi_r}^{\phi_m} d\phi = \int_0^{\tau} V dt$$

and $$V = \frac{N(\phi_m - \phi_r)}{\tau}$$

since $$\phi_m - \phi_r = (B_m - B_r).A = \Delta B.A$$

$$V\tau = N.\Delta B.A \qquad (7.8)$$

To avoid saturation equation (7.8) must be satisfied.

7.2.1 Design of Transformer

Using equation (7.8) and the following data for a ferroxcube 45mm pot-core transformer,

$$V = 12V$$
$$B = 2\times10^3 \text{ Gauss}$$
$$A = 3.62 \text{ cm}^2$$

and assuming a maximum pulse duration of 2.5ms is passed through the transformer, the number of primary turns is

$$N_p = \frac{V\tau}{A.\Delta B.10^{-8}} = \frac{12\times2.5\times10^{-3}}{3.62\times2\times10^3\times10^{-8}} = 414$$

For 4V to be present across the secondary winding, the turns ratio must be 3, so that the number of secondary turns is,

$$N_s = \frac{1}{3}N_p = 138$$

The leakage inductance should be minimised, since the transformer will be subjected to rapidly changing currents during the switching interval. For this purpose, a bifilar transformer winding is used to obtain tight coupling between the two primary windings.

It is important to incorporate the feedback diodes D1 and D2 in the final arrangement of the circuit shown in Figure 7.11. For reactive loads, these diodes conduct to supply the out-of-phase portion of the load current. When the inverter switches from T1 to T2, an inductive load prevents the main load current from reversing instantaneously, and transformed load current must flow through D2 and back to the d.c. supply

until the load current reverses. The feedback diodes prevent the voltage across either half of the primary winding from exceeding the supply voltage. These diodes not only maintain a square wave output under all load conditions, but also decrease the voltage requirements for T1 and T2.

The d.c. supply should have a low transient impedance, and a capacitor at its output is useful in enabling it to both accept and supply power.

7.2.2 Performance of the Driver

Figure 7.12 shows the current flow when the secondary of the transformer is connected to the base-emitter junction of the power transistor being driven. As can be seen, the maximum forward base current is about 0.5A giving a maximum collector current of 5A for a gain of 10 of the power transistor. It can also be seen that the reverse current flowing through the junction is very small. The rise and fall times of the base current are very long, which will result in excessive dissipation in the power transistor during switching.

When the secondary winding voltage is raised to increase the forward and reverse current through the base-emitter junction, this will result in saturation of the transformer required to pass pulses of different time duration. Since the outputs of the two secondary windings each drive the two power transistors in a branch, there must be a delay between the two driving waveforms, to avoid the occurrence of a short circuit across the supply. The natural delays in the transformer are insufficient, especially when the switching frequency and the output current are high.

Although transformer drive is desirable, the above disadvantages limit its use in this form of application. However, it may be useful for a fixed-frequency system without a strict requirement on the switching times.

7.3 DIRECT DRIVE

As the requirements presented by the power transistors of the inverter for a delta-sigma modulated driving waveform are very difficult to be met with a push-pull circuit incorporating pulse transformers, it is necessary to adopt a different approach to provide a satisfactory drive circuit. A high speed optically-coupled isolator permits the transmission of a signal without direct electrical connection, and it can easily be incorporated into the amplifier design. The transmission of the variable pulse-width square wave switching signal from the low power signal circuits to the base drive circuit (attached to the power transistors) is thereby easily accomplished. A driver designed in this way must be capable of providing sufficient base current to ensure that the power transistor is in saturation. The rise and fall times of the base current must also be short to minimize the switching losses. It is also necessary to provide sufficient reverse base current to switch-off the power transistor quickly.

7.3.1 Design

Figure 7.13 shows the basic driver. The output of the delta-sigma modulator, having been transferred to the amplifier through the opto-isolator, switches a pnp and an npn transistor pair, to connect alternately the positive and negative supply rails to the base-emitter junction of the power transistor.

An opto-isolator type 305-759 comprises an infrared light emitting diode and a silicon photo transistor, and it can be used to accomplish signal transfer with isolation up to a voltage level of ±2500V. A Schmitt trigger is also necessary to shape the transferred signal to provide both fast leading and falling edges. The opto-isolator must be used in a circuit configuration which gives a minimum delay, and that introduced by the circuit shown in Figure 7.14 is only about 2 μs. Since the same delay is

caused by all the drivers (six are needed for the six power transistors in the inverter) the operation of the inverter is not affected.

The driver requires two independent voltage supply rails, and these may be obtained as shown in Figure 7.15. It is important not to exceed the reverse base-emitter-breakdown voltage of the power transistors in the inverter and for this purpose the negative supply rail is limited to -4.7V.

The complete circuit diagram of the driver is shown in Figure 7.16. When transistor TR2 switches on transistor TR8 turns off, and transistor TR7 becomes conducting. Hence, the base of the power transistor is connected to the positive supply rail. When transitor TR2 switches off, transistor TR8 turns on, to apply a negative bias for the base-emitter junction of the power transistor to switch it off. The capacitors and resistors present in the base circuitry of transitors TR7 and TR8 act to speed up the switching process, so that turn-on and turn-off times are both kept to a minimum. The capacitor-resistor combination in the collector of transistor TR7 provides the overshoot of current required by the base of the power transistor when this is switched on.

It is necessary to protect the power transistors, especially if the connecting loads between the driving circuits and the power transistors are long, since transient voltage drops due to the inductance of connecting leads can be significant with microsecond switching speeds at high currents. To limit transient voltages the clamping circuit shown in Figure 7.17 is connected directly to the base-emitter junctions of the power transistors.

7.3.2 Performance

Each driver circuit is connected to the base-emitter junction of a power transistor (2N3055) feeding an inductive load. Figure 7.18 shows the base current and the base-emitter voltage throughout the complete operational cycle, together with the expanded waveforms during the turn-on and turn-off

periods. As can be seen, the driver produces nearly 2A of forward current and about 1.5A of reverse current. From Figure 7.18.c it can be seen that V_{BE} stays positive for some time, although the base current is negative. This is due to the maintenance of charge by the input capacitance of the transistor.

Figure 7.19 shows the collector current and the collector-emitter with no negative voltage applied across the base-emitter junction during the turn-off period, i.e., the transistor turns off by itself. As can be seen, I_C reduces to zero in about 16μs and V_{CE} reaches full supply voltage very quickly. As expected, there is considerable dissipation in the transistor, and the turn-off process is not satisfactory.

In Figure 7.20, I_C and V_{CE} are shown when a negative voltage is applied to the base-emitter junction of the power transistor during the turn-off period. The collector current falls to zero in about 3.0μs and the dissipation in the transistor is considerably reduced. A further improvement can be obtained by connecting an inductor in series with the base-emitter junction, as shown in Figure 7.21, when I_C falls to zero in about 1.5μs and the much faster turn-off process is accompanied by a greater reduction in the power dissipation in the transistor. The inductor in series with the base-emitter junction reduces the rate of fall of base current during the turn-off period. Otherwise, the fast decay causes the emitter current to fall very quickly to zero, when the emitter no longer influences the operation and normal transistor action is entirely absent. In such a case the recovery process is similar to that of the slow reverse recovery of a diode (collector-base). The inductor helps to maintain normal transistor action during the turn-off period, and by reducing the rate of fall of I_B and giving an adequate storage time, it eliminates the collector current tail, as can be seen by reference to Figure 7.22. Since the inductor decreases the rate of change of base current it also increases the turn-on

time of the transistor, and for this reason it should be placed in the negative voltage drive circuit such that it is by-passed by the positive going base current.

Figure 7.23 shows I_C and V_{CE} during the turn-on period, with V_{CE} falling to zero in less than 0.5μs, and the dissipation of the transistor during turn-on being very small. Comparison of Figure 7.18.b and Figure 7.23 shows that the base current turn-on pulse has a considerably shorter rise time than that of the collector current, which is in good agreement with the requirements for the driver.

The variation in the turn-off time with collector current is shown in Figure 7.24; without negative voltage, with negative voltage and with a series inductor. It is clearly seen that the application of negative voltage and the use of an inductor both considerably reduce the turn-off time, making the transistor a much more efficient switch.

The turn-off time is also dependent on the magnitude of the negative voltage applied across the base-emitter junction of the power transistor as shown in Figure 7.25. It follows that to obtain improved results a large reverse voltage should be used, although care must be taken to ensure that the transistor reverse base-emitter voltage and current ratings are not exceeded.

The transistor used in the above tests has a minimum turn-off time of nearly 1.5μs, as would be expected since a 2N3055-type transistor is not a fast switching device. A fast switching transistor type ESM16A gives a minimum turn-off time of less than 0.5μs, and for this reason was incorporated in the inverter. Since the turn-off time is very small an inductor in series with the base drive circuit is unnecessary.

7.3.3 Load Line Shaping to Limit dV/dt

As can be seen from Figures 7.19, 7.20 and 7.21, the collector-emitter voltage rises almost to its full value before the collector current starts

to fall. Although in Figure 7.21 the collector current falls very rapidly to zero, V_{CE} is very high during this time and the dissipation in the transistor is still large. A snubber circuit[27] incorporating a capacitor (see Figure 7.26.a) may be used deliberately to retard the voltage rise, by providing a path for load current during the turn-off period of the inverter transistors and thereby reducing considerably the power dissipated in the transistors. The collector current and collector-emitter voltage during the turn-off period are then as shown in Figure 7.26.b. The snubber circuit does not affect the efficiency of the inverter, since the dissipated power in the resistor is otherwise lost in the transistor.

Figure 7.27.a and 7.27.b show respectively the I_C/V_{CE} excursion during switching without and with a snubber circuit and clearly confirm the arguments advanced above.

7.4 INVERTER DESIGN

7.4.1 Basic Inverter

The basic 3-phase bridge inverter shown in Figure 7.28 comprises six power transistors T1 to T6 and six diodes D1 to D6. The inverter operates such that the direct voltage supply is chopped and applied sequentially to the stator windings of the induction motor. The motor behaves like a filter, and responds mainly to the fundamental of the voltage applied to its stator windings so that the current flowing in the motor approximates closely to a sine wave, with the closeness of the approximation increasing as the switching frequency is raised. For correct operation, transistors 1,3 and 5 are driven by 3-phase signals while transistors 2,4 and 6 are driven by the inverse of these signals. Diodes D1 to D6 are necessary to return the reactive energy in the stator windings to the supply rails when the switching sequence changes.

7.4.2 Voltage Supply

The direct voltage supply for the inverter can be obtained from the 3-phase uncontrolled rectifier shown in Figure 7.29 and a ripple smoothing circuit. The necessary design equations[28] are included in Appendix 3.

Using these equations, the requirement for a voltage supply capable of producing 10A at 300V with a ripple of less than 1% gives,

E_T(r.m.s.) = 128.2V

E_T(max) = 181.3V

E_{max} = 315V

I_0, average current/rectifier leg = 3A

$I_{r.m.s.}$/rectifier leg = 5.77A

I_{peak}/rectifier leg = 10.5A

The 3-phase transformer must thus produce a maximum voltage of 181.3V, while the rectifiers must be capable of withstanding 315V and passing a current of 10A. A smoothing circuit with L=16.2mH and C=2000μFwill easily satisfy the ripple condition, with the bleeder resistor R being less than 300Ω to ensure continuous current flow through the rectifiers. Another function of this resistor is to dissipate the reactive power in the motor windings since, with an uncontrolled bridge rectifier, the reactive energy in the stator windings cannot be returned to the supply rails. If the energy is not dissipated it will charge the capacitor, so that its voltage may increase to a value in excess of the breakdown voltage of the power transistors.

7.4.3 Action of Fast Recovery Diodes

The diodes D1 to D6 in the basic inverter must have a fast recovery time, so as to prevent the occurrence of a short circuit across the input supply.

Figure 7.30.a shows an inverter comprising, for simplicity, only four

transistors. If the bases of these are driven as shown in Figure 7.30.b, transistors T1 and T4 are on (during the period t_1) and the current flow through the inductive load is as in Figure 7.30.c. When transistors T1 and T4 are turned off T2 and T3 are turned on, after a delay time to avoid a short circuit across the supply. During this time t_2, diodes D2 and D3 provide a path for the load current as shown in Figure 7.30.d, and after time t_2, transistors T2 and T3 are turned on for a period of t_3. Assuming operation on the positive half cycle, and that t_3 is very much smaller than t_1, the current in the load will not reduce to zero to allow transistors T2 and T3 to conduct. During this time the current still flows in the direction shown in Figure 7.30.d.

Now, when transistors T1 and T4 are turned on again, there is a short circuit across the supply (as shown in Figure 7.30.e), since diodes D2 and D3 have been conducting previously. The short-circuit lasts until diode D2 has recovered, and unless a fast recovery device is used the energy contained in the current pulse will be sufficient to destroy the power transistor T1. Figure 7.31 shows the current through diode D2 for two different diodes, with the supply voltage being kept low. As can be seen, the current is reduced by 20 times and the time period by 40 times, so that energy contained in the pulse is very greatly reduced.

7.4.4 Inverse Mode Operation of Transistors

It was observed when the inverter was operated that the current flow through the transistors was bi-directional. When investigated further, it was realised that the freewheeling diodes would not conduct, apart from a very small delay time, and that all the current that should flow through the diodes was in fact flowing through the power transistors. This was due to the bi-directional nature of the transistors, since current can flow either from the collector to the emitter junction or vice versa, depending

on the polarity of the applied voltage. The latter is the inverse mode transistor operation[29], as opposed to the normal mode when the current flow is from the collector to the emitter junction.

The situation explained above is illustrated by Figure 7.32, and the path enabling current to flow through the transistor T1 as shown in Figure 7.30.c. When T1 is turned off, current is transferred to the rectifiers D2 and D3, as shown in Figure 7.30.d. After a delay time, transistor T2 is turned on, and if the saturation voltage across transistor T2 is lower than the voltage across diode D2, current will prefer the path through transistor T2. The power transistor ESM16A has a voltage drop of nearly 1V for collector currents in excess of 6A, whereas the fast recovery diode 1N3893 has a voltage drop of 0.9-1.4V. For collector currents less than 6A, current will thus flow through the transistor, avoiding the freewheeling diodes. This situation must however by avoided, since the recovery time of transistors operating in the inverse mode is greater than in the normal mode, which creates the possibility that when transistor T1 is turned on again there will be a short circuit across the supply. Furthermore, since the current gain in inverse operation is very poor, a greater current demand will saturate the transistor, and will result in excessive dissipation. This can easily be avoided with diodes placed in series with the power transistors. The final version of the inverter is shown in Figure 7.33. As can be seen, freewheeling diodes are connected such that if the protection fuse blows the reactive energy in the motor can still be dissipated in the bleeder resistor.

7.4.5 Overcurrent Protection Circuit

Although thyristors of 10A nominal ratings may typically have a 60A rating for 10ms, a 10A power transistor can take, perhaps, 20A for 3μs. Consequently, a fault condition causing the current to increase above the rating of a transistor, even if this persists for only a very short time,

will most certainly destroy the transistor. To prevent overload conditions destroying the inverter transistors, a fault detector is used to operate a "crowbar" thyristor and to blow the supply fuse.

The circuit diagram of the overcurrent protection circuit is shown in Figure 7.34. The 0.1Ω resistor detects the current and, if the voltage appearing across the resistor is greater than the base-emitter voltage drop of transistor T1, the circuit produces a turn on pulse to the gate of thyristor. This then short circuits the supply and the fast acting semi-conductor fuse blows.

7.4.6 Phase Current Monitor Unit

A current monitor unit is necessary to observe the current flow in all three phases of the stator windings. It should be able to provide isolation as well as to pass currents of very low frequency.

The series-chopper circuit[30] designed for this purpose and shown in Figure 7.35.a can be represented as in Figure 7.35.b. Switches A,B,C and D are operated at a very high frequency (at least ten times the input frequency), and two sets are used so that the transformer does not saturate. The switches are operated in pairs, such that A and D close simultaneously while C and D are open, or vice versa. The waveforms at various points in the isolator are shown in Figure 7.35.c.

As can be seen from Figure 7.35.a, the switches are replaced by two series transistors operating in the inverse mode, i.e. passing current in the reverse direction. The reason for this is twofold

a) the V_{CE}(sat) drop is very low, so that when the transistor is on it is nearly a short circuit,

b) the leakage current is very low, so that when the transistor is off it is nearly an open circuit.

The two series transistors act to cancel their V_{CE} voltage drops, thus reducing the error in the output voltage. A filter at the output is also

necessary to remove the high frequency switching components.

The four pulse transformers driving the transistors are driven in turn by the astable multivibrator[29] of Figure 7.36 operating at 10kHz frequency. The primary and the secondary windings of the transformers must be shielded to reduce the effect of switching, and details of the transformer are given in Figure 7.37.

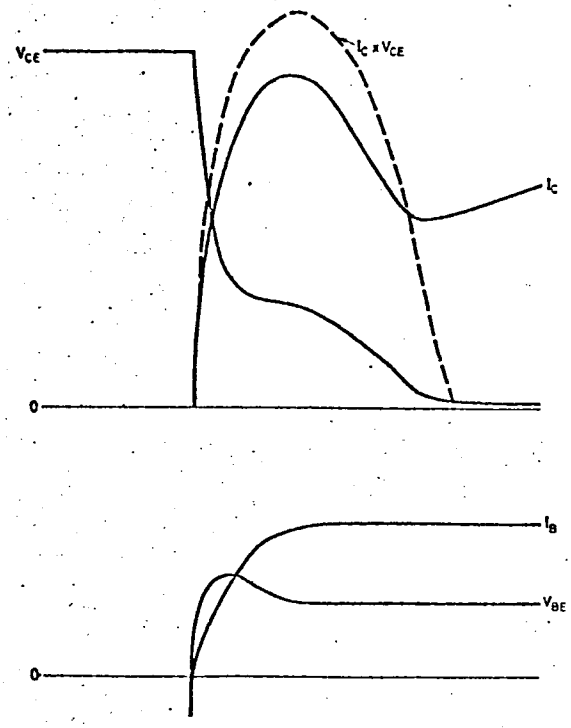


Figure 7.1: TURN-ON WAVEFORMS OF A TRANSISTOR

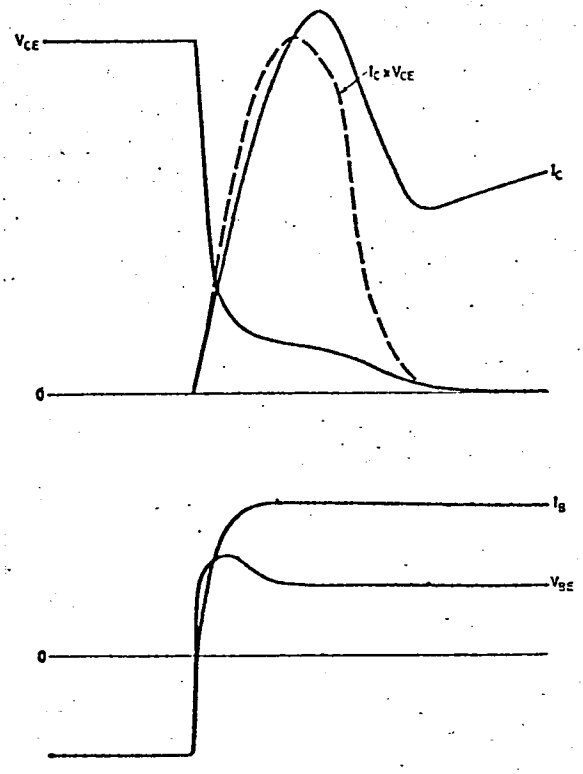


Figure 7.2: TURN-ON WAVEFORMS WITH FAST RISING BASE CURRENT

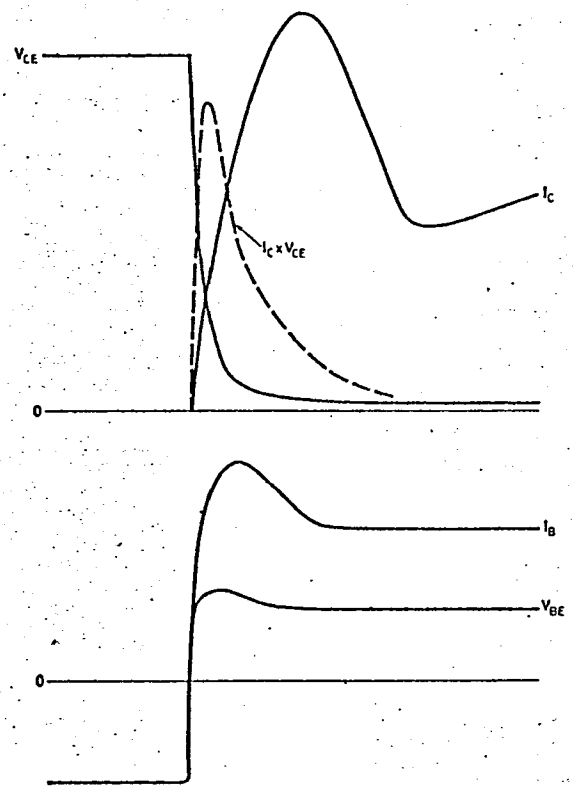


Figure 7.3: TURN-ON WAVEFORMS, FAST RISING BASE CURRENT WITH OVERSHOOT

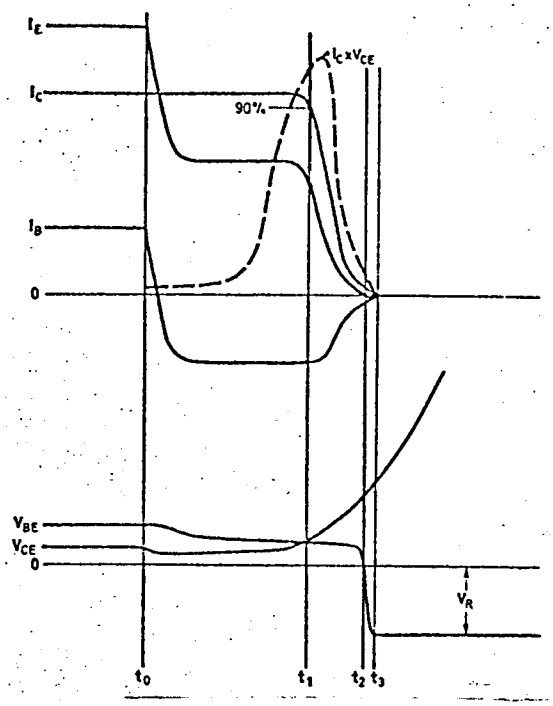


Figure 7.4: TURN-OFF WAVEFORMS

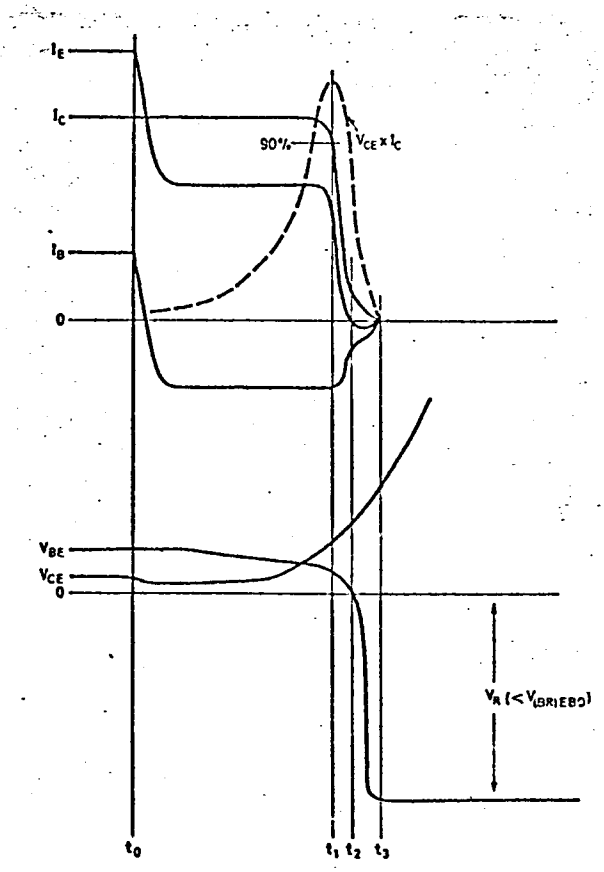


Figure 7.5: TURN-OFF WAVEFORMS WITH INCREASED REVERSE BASE-EMITTER VOLTAGE

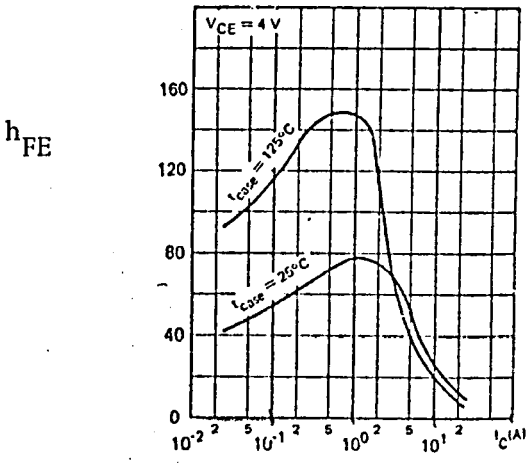
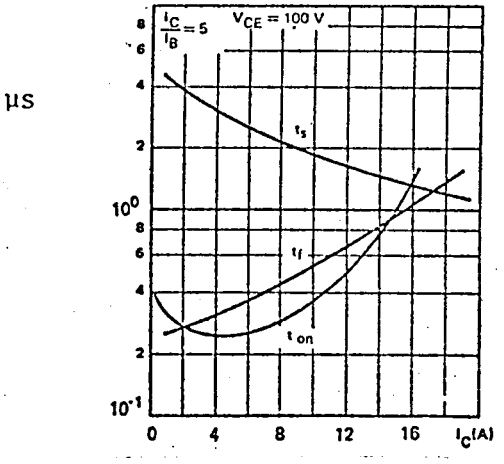


Figure 7.6: FORWARD CURRENT TRANSFER RATIO AS A FUNCTION OF COLLECTOR CURRENT AND THE CASE TEMPERATURE (Data for an npn Silicon Transistor type BUX 24)



t_s=storage time
t_f=fall time
t_{on}=turn-on time

Figure 7.7: SWITCHING TIMES AS A FUNCTION OF COLLECTOR CURRENT (Same Transistor)

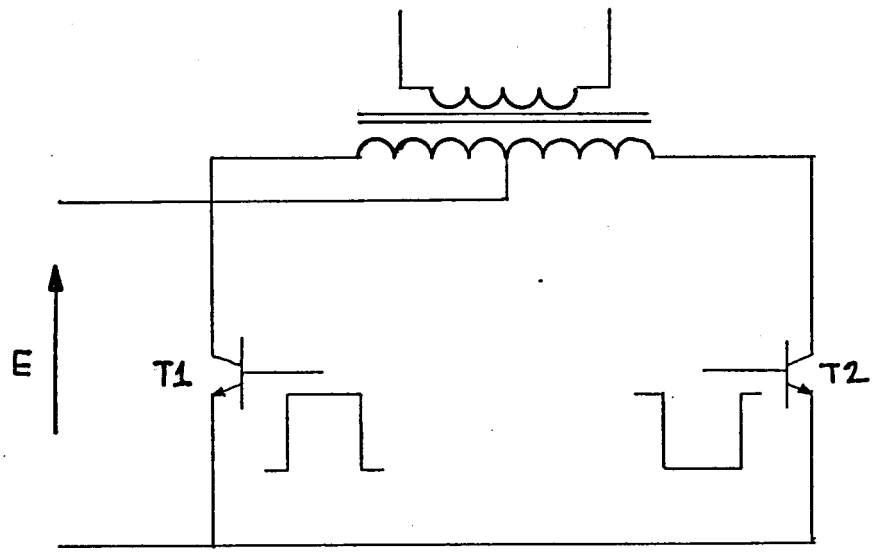


Figure 7.8: BASIC DRIVER

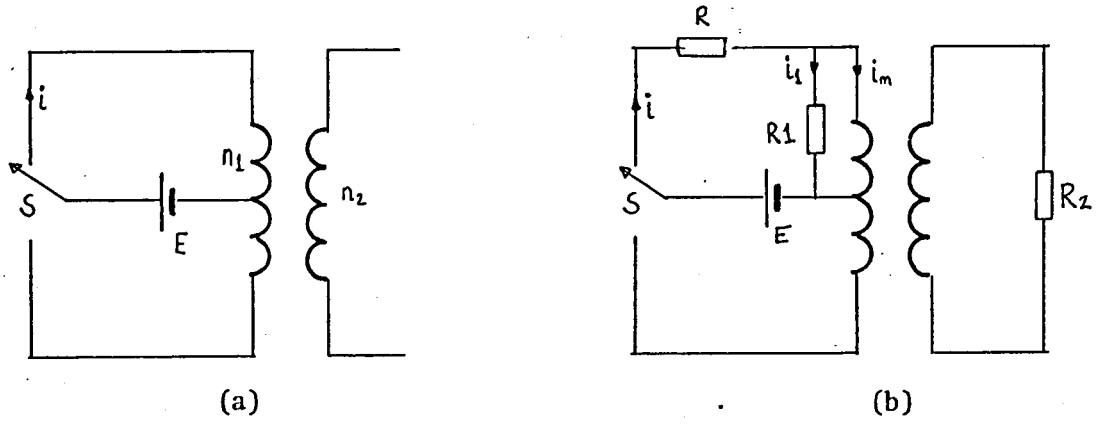


Figure 7.9: EQUIVALENT CIRCUITS OF THE DRIVER
(a) at no-load
(b) at load

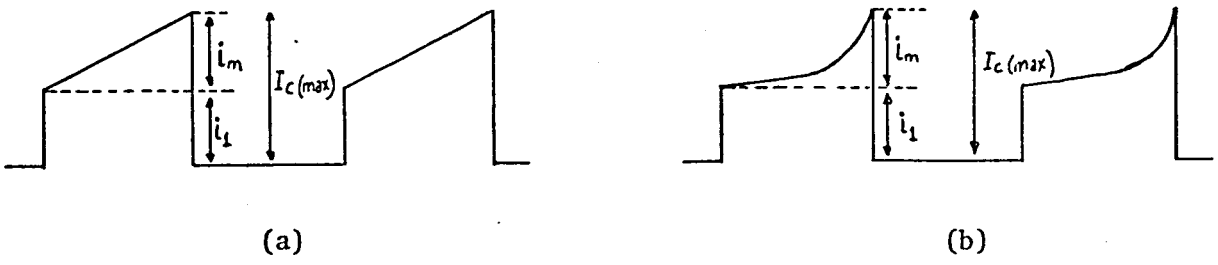


Figure 7.10: COLLECTOR CURRENT WAVEFORMS
(a) non-saturating transformer
(b) saturating transformer

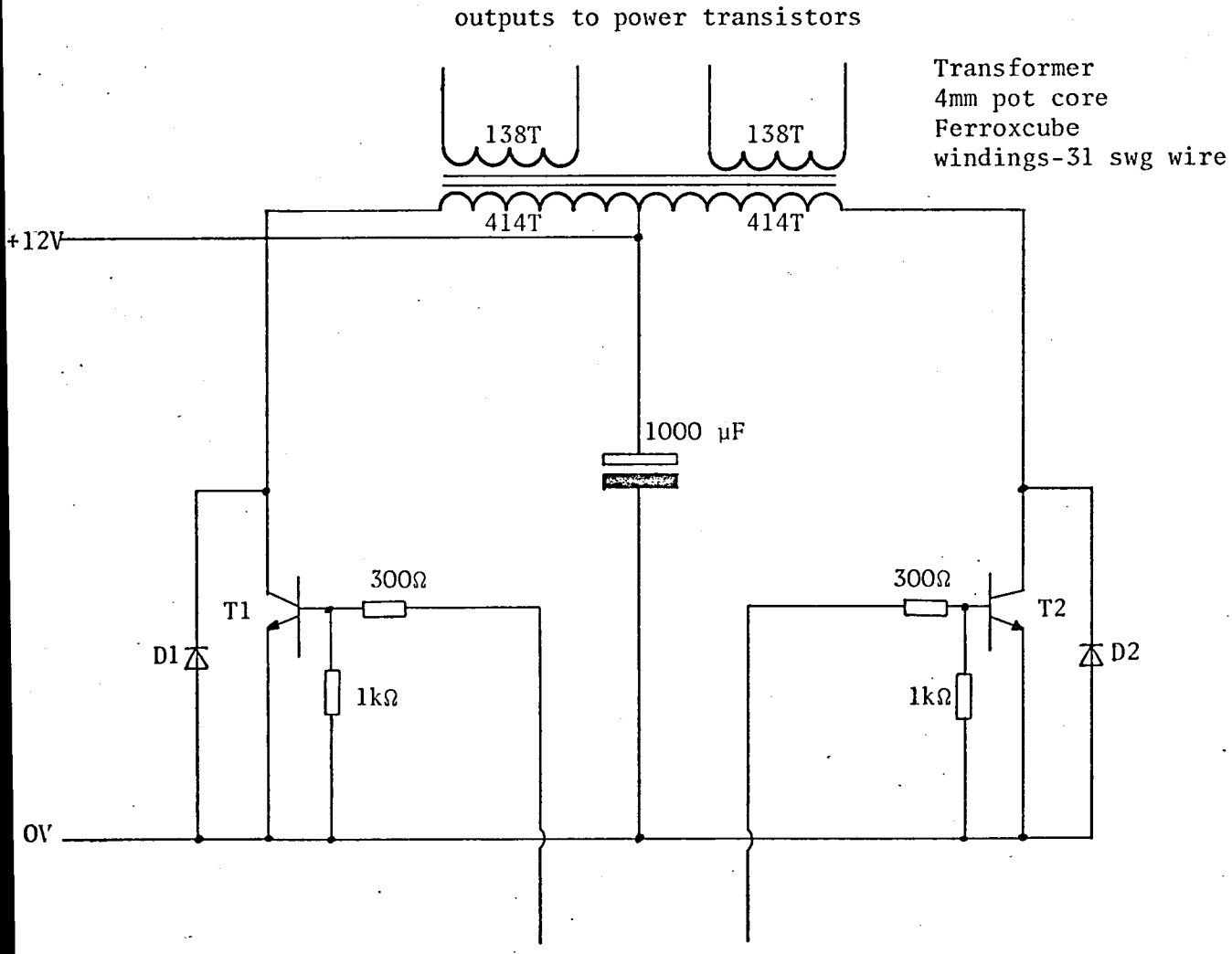


Figure 7.11: COMPLETE CIRCUIT DIAGRAM OF THE DRIVER

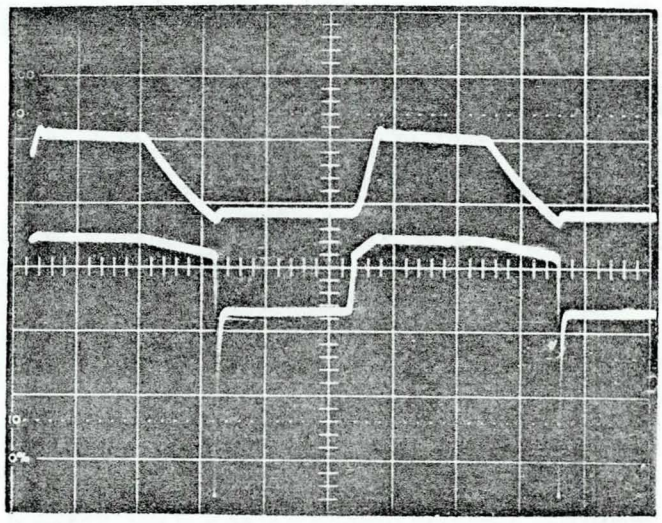


Figure 7.12: BASE DRIVING WAVEFORMS

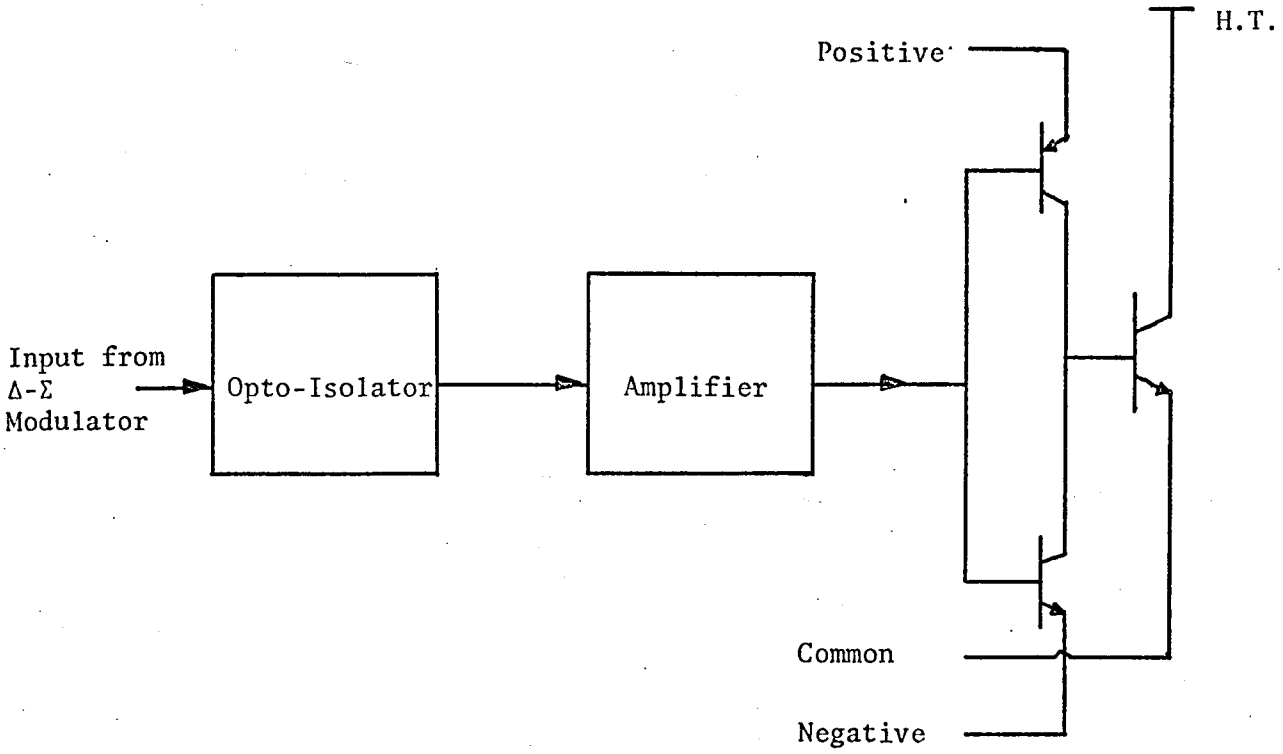


Figure 7.13: BLOCK DIAGRAM OF THE DRIVER

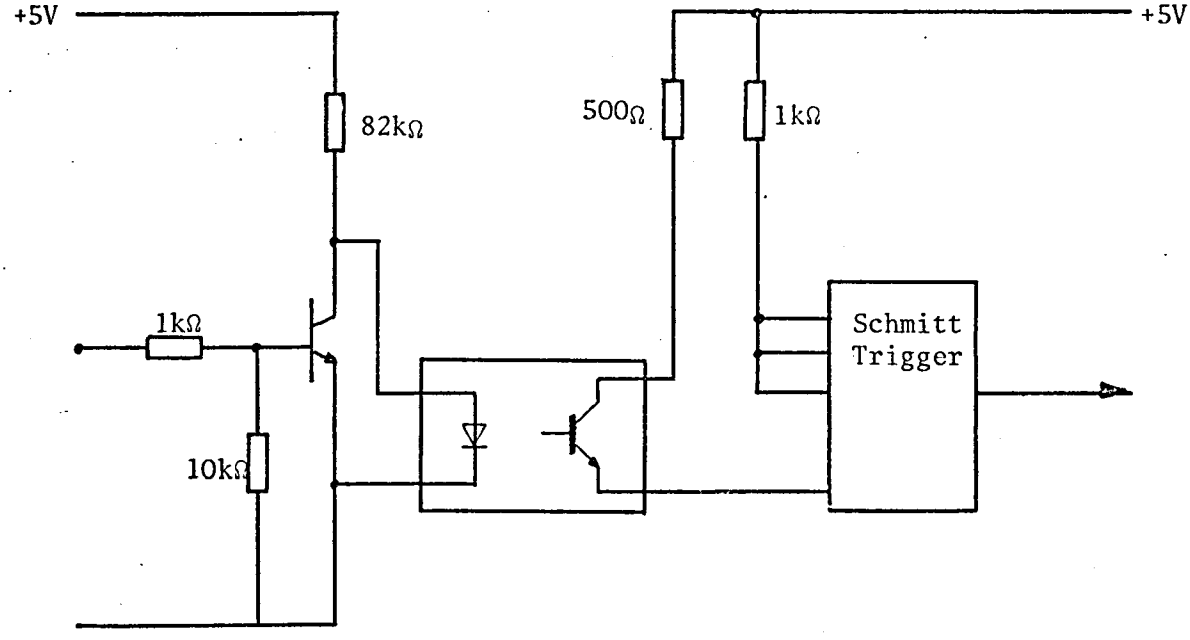


Figure 7.14: OPTO-ISOLATOR CIRCUIT

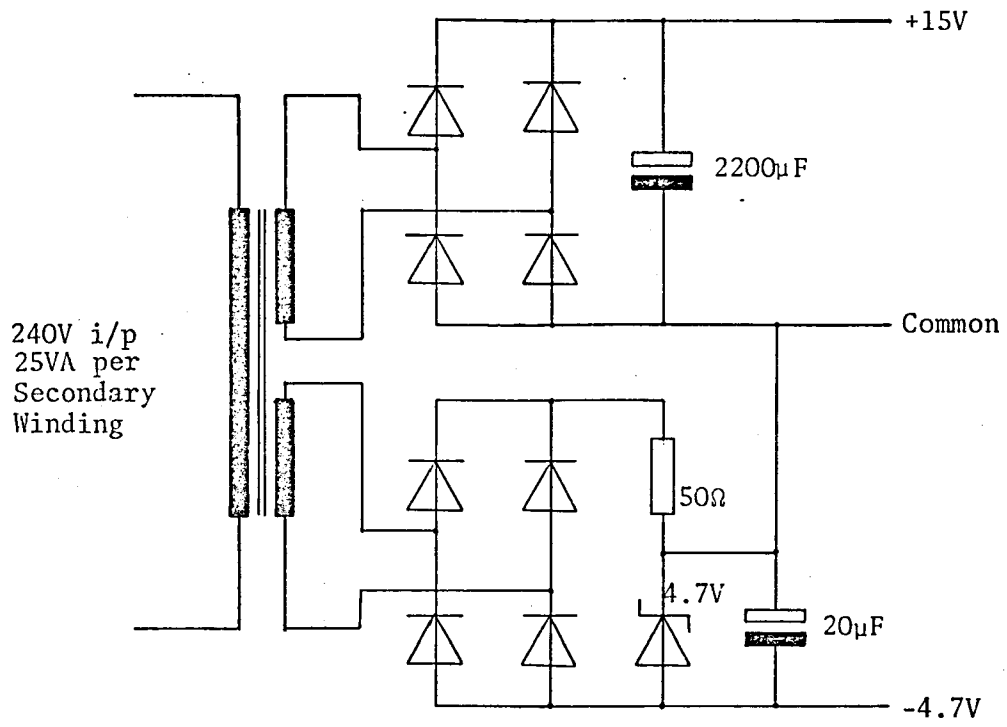


Figure 7.15: VOLTAGE SUPPLY FOR THE CIRCUIT OF FIGURE 7.16

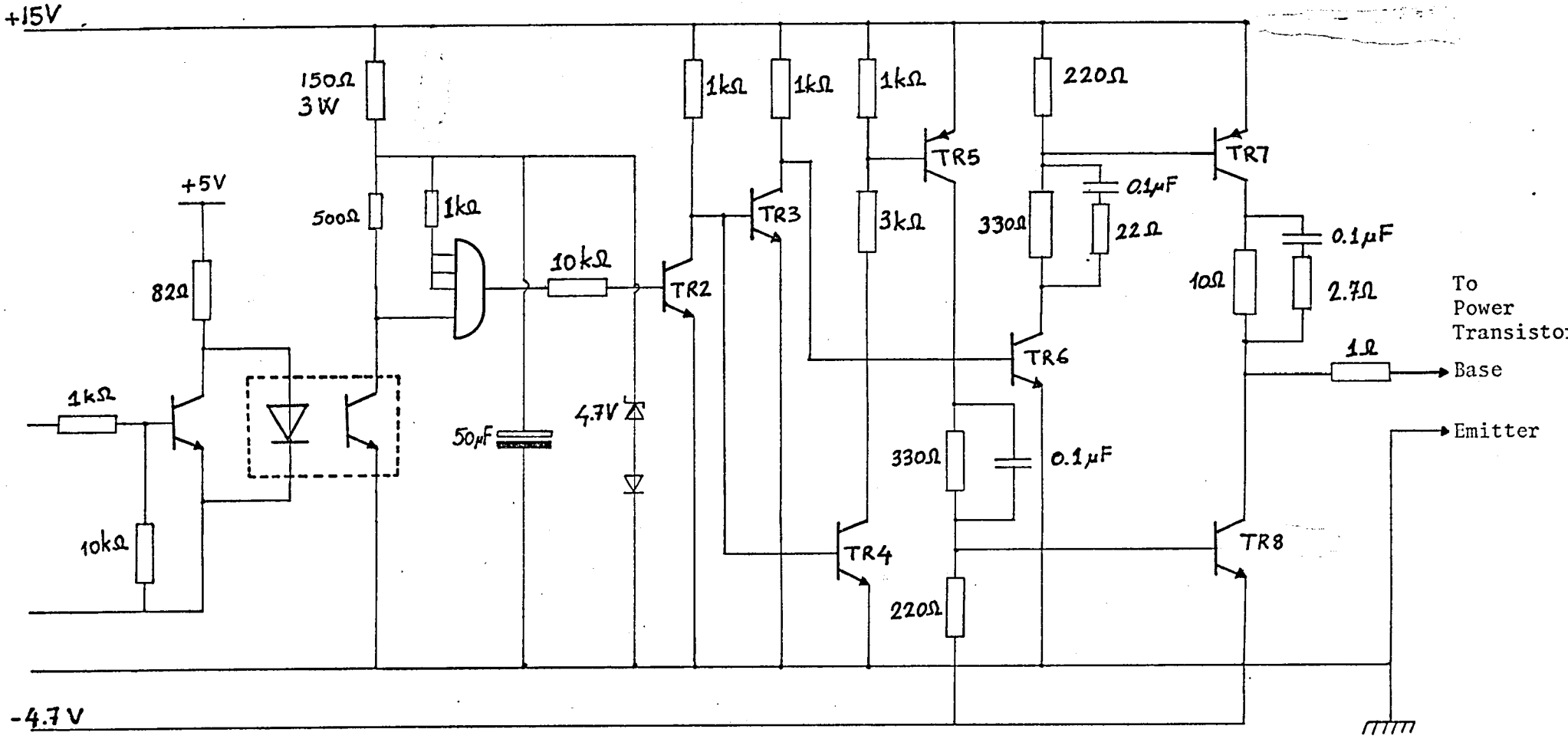


Figure 7.16: COMPLETE CIRCUIT DIAGRAM OF THE DRIVER (Six Needed)

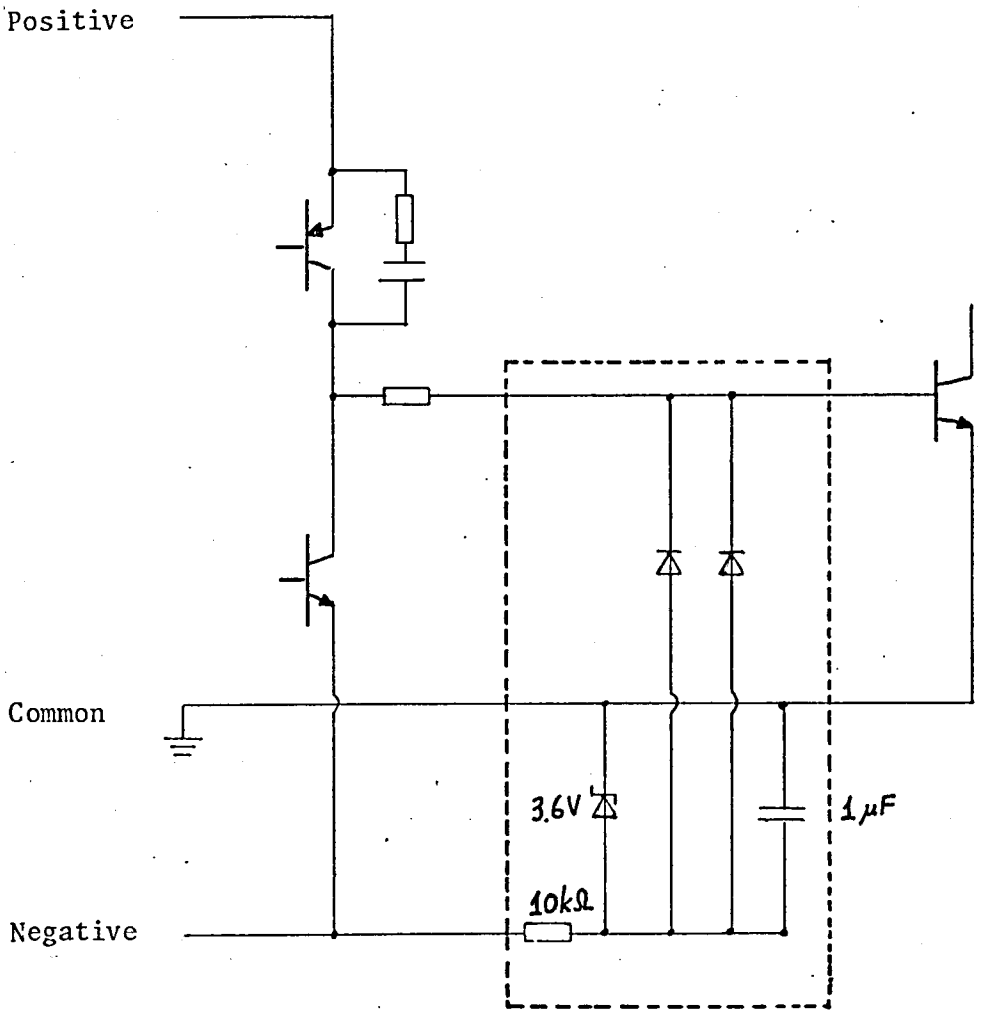
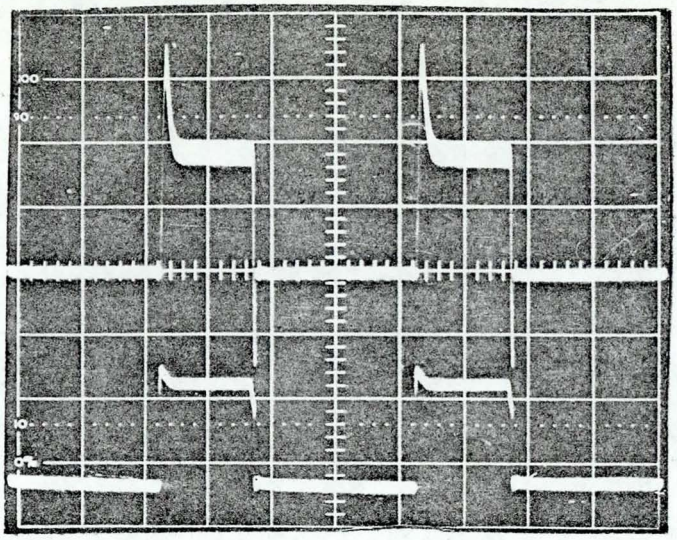
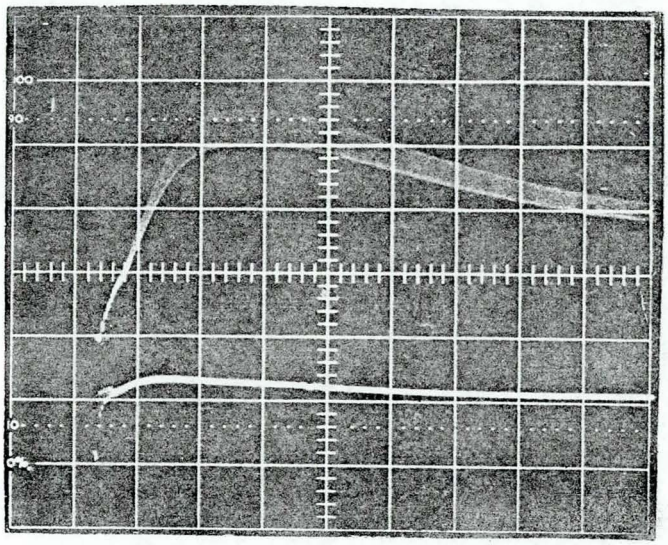


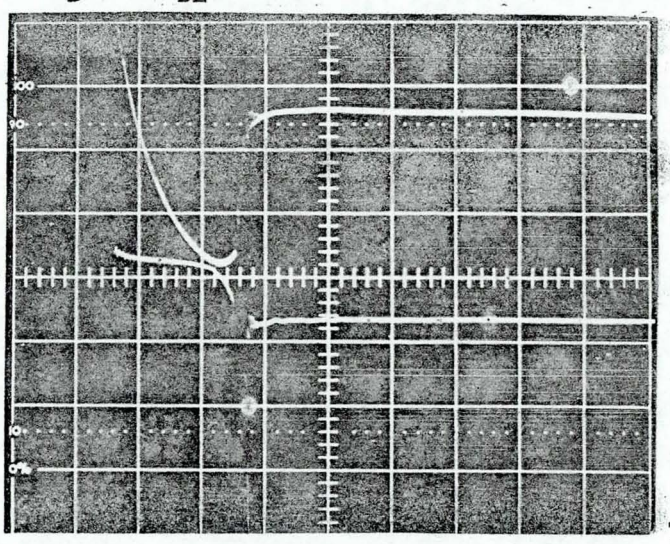
Figure 7.17: POWER TRANSISTOR PROTECTION CIRCUIT



(a) I_B and V_{BE} Waveforms



(b) I_B and V_{BE} Waveforms During Turn-on



(c) I_B and V_{BE} Waveforms During Turn-off

Figure 7.18: BASE DRIVING WAVEFORMS

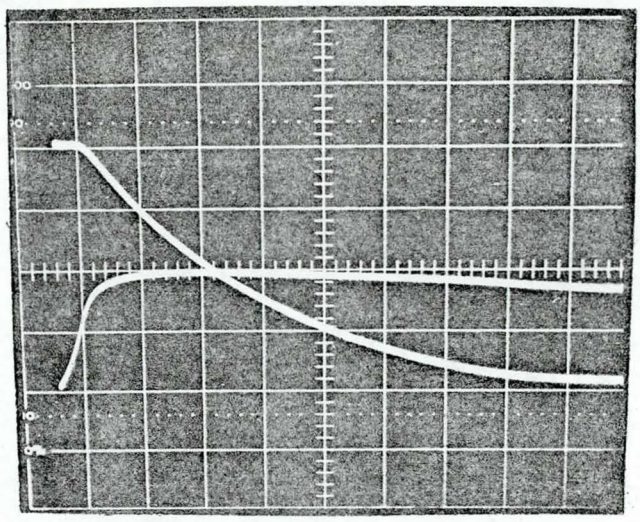


Figure 7.19: COLLECTOR CURRENT AND COLLECTOR-EMITTER VOLTAGE DURING TURN-OFF (WITHOUT NEGATIVE DRIVE)

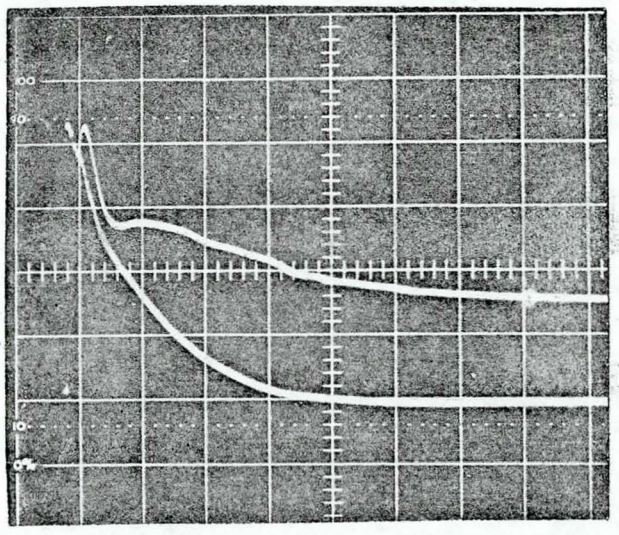


Figure 7.20: COLLECTOR CURRENT AND COLLECTOR-EMITTER VOLTAGE DURING TURN-OFF (WITH NEGATIVE DRIVE)

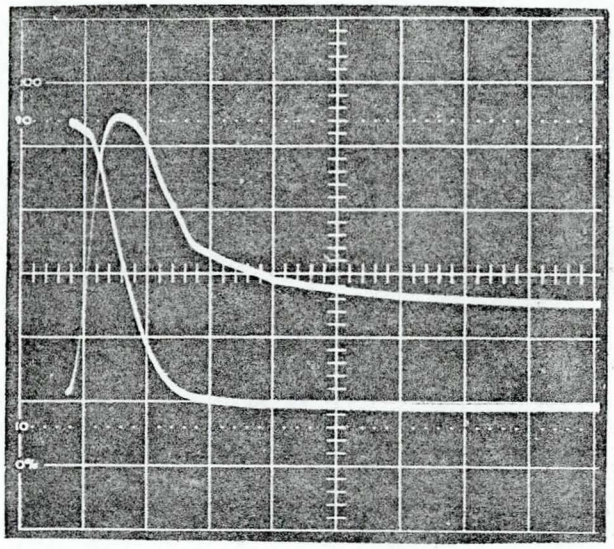


Figure 7.21: COLLECTOR CURRENT AND COLLECTOR-EMITTER VOLTAGE DURING TURN-OFF (WITH NEGATIVE DRIVE AND A SMALL INDUCTOR)

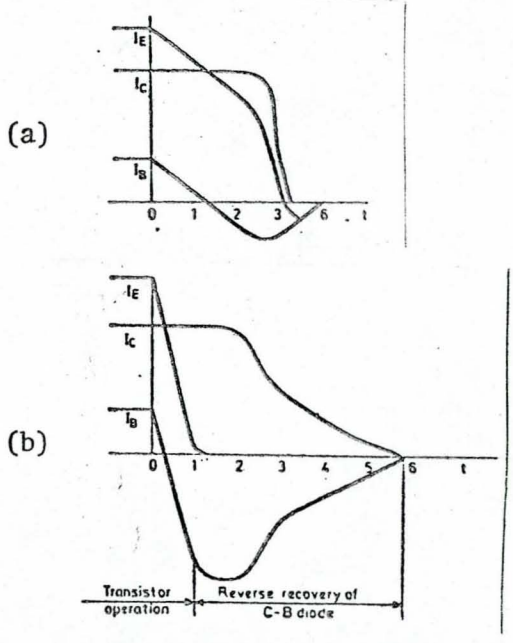


Figure 7.22: TURN-OFF WAVEFORMS

(a) Correct Base Drive

(b) Incorrect Base Drive

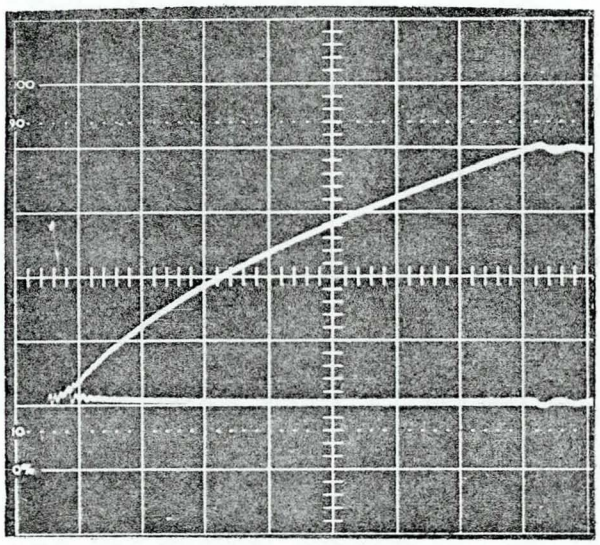


Figure 7.23: TURN-ON WAVEFORMS

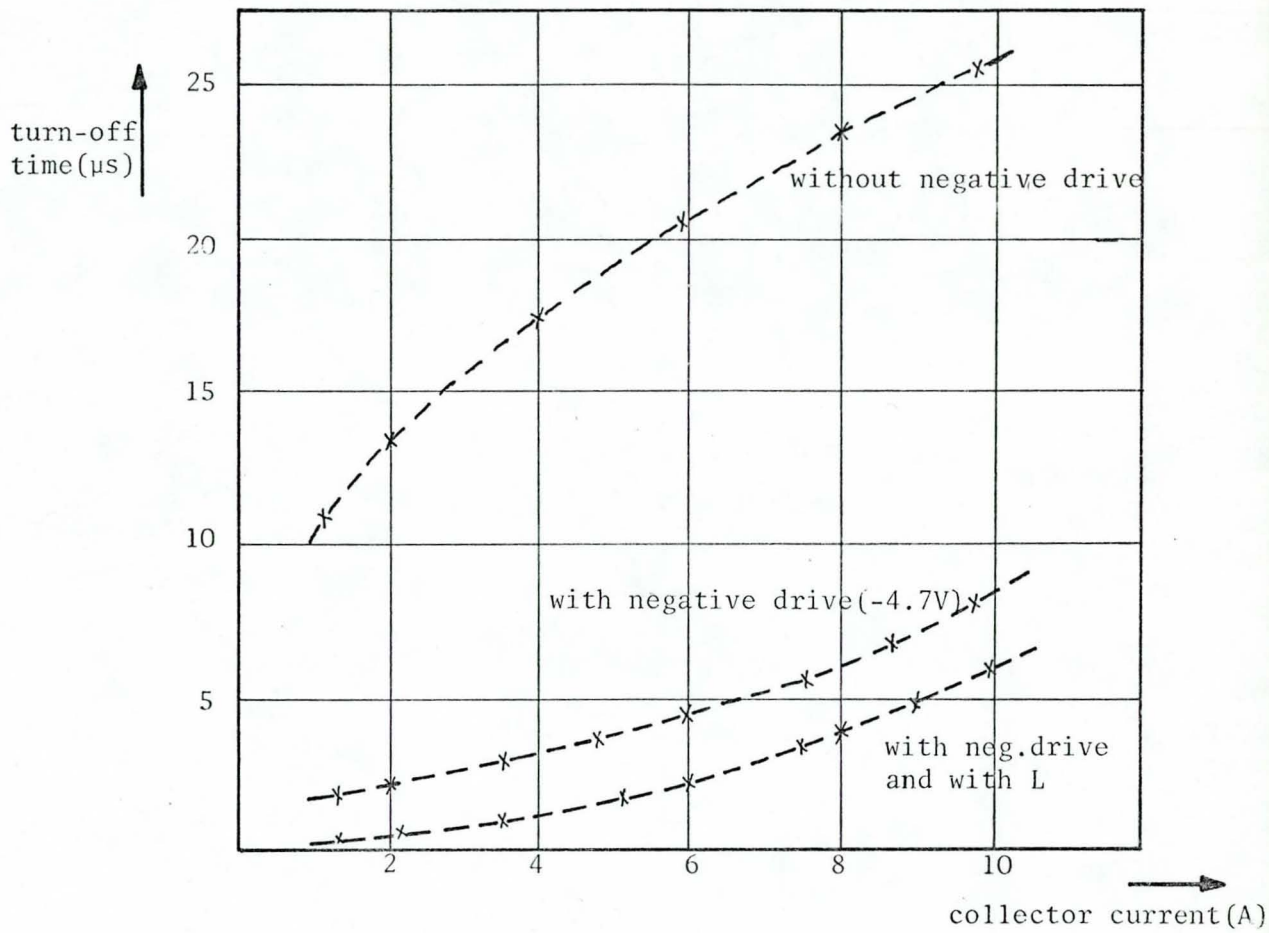


Figure 7.24: VARIATION OF TURN-OFF TIME WITH COLLECTOR CURRENT

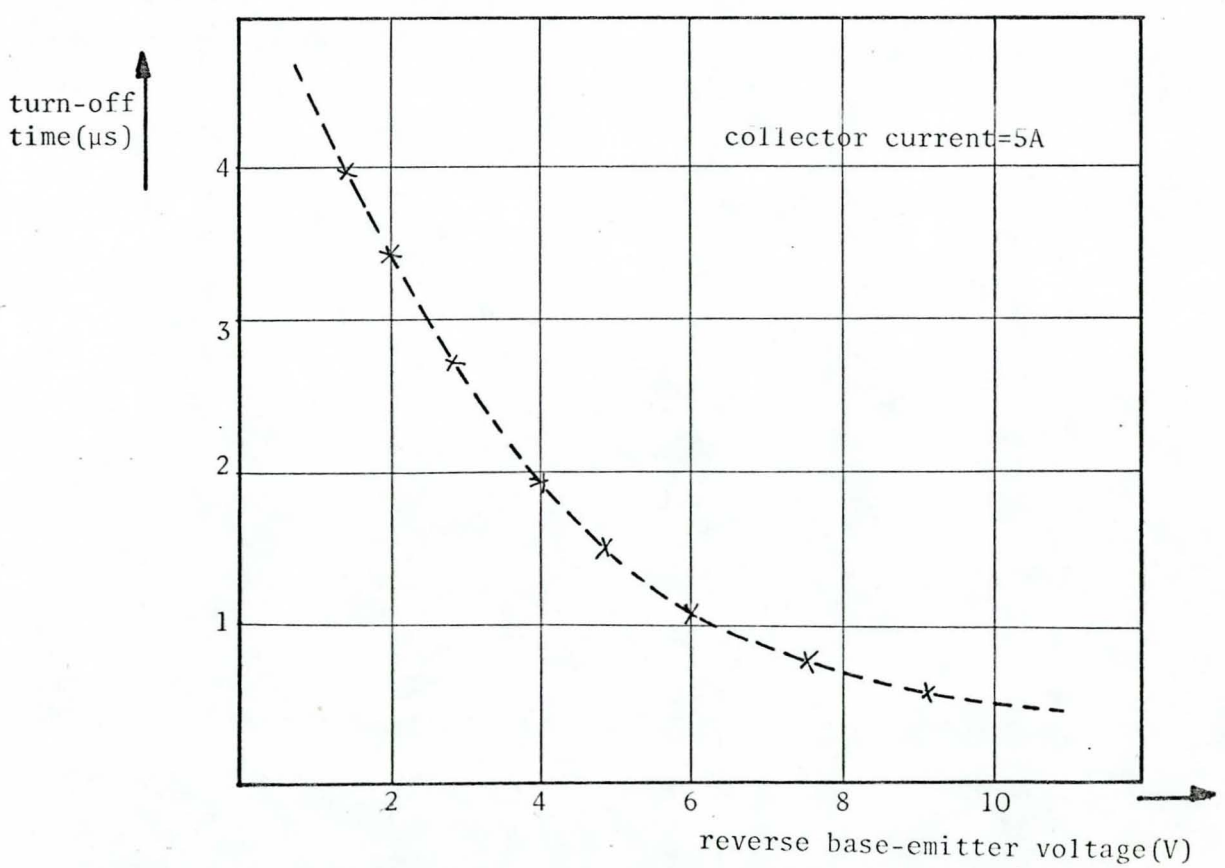
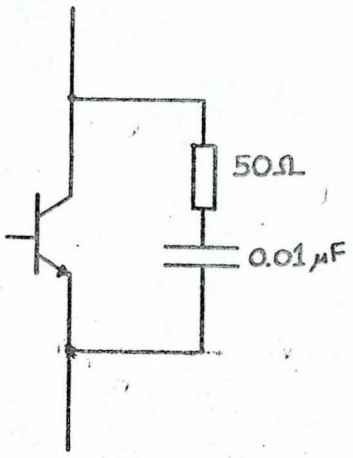
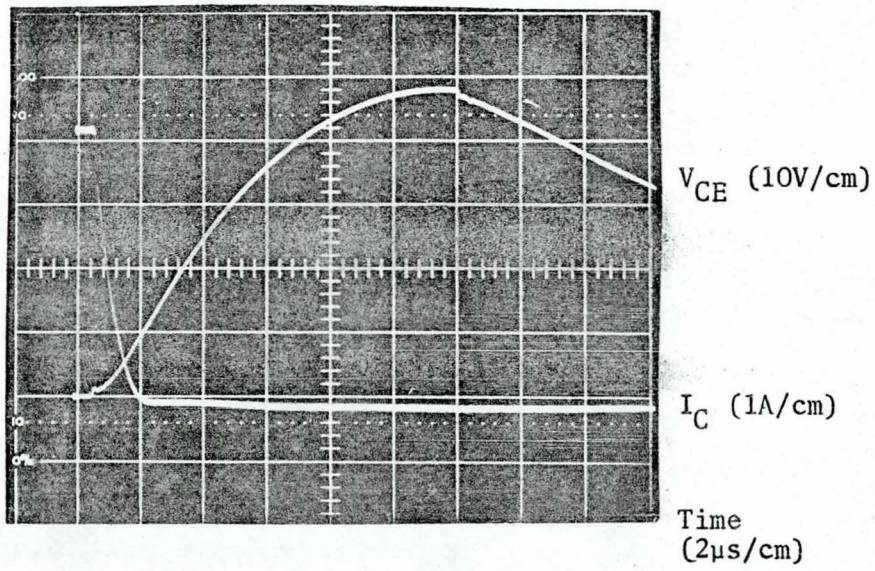


Figure 7.25: VARIATION OF TURN-OFF TIME WITH REVERSE BASE-EMITTER VOLTAGE

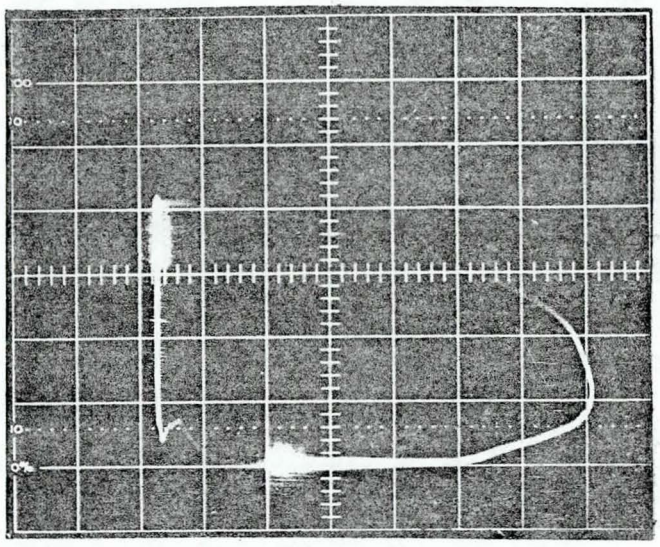


(a) Snubber Circuit

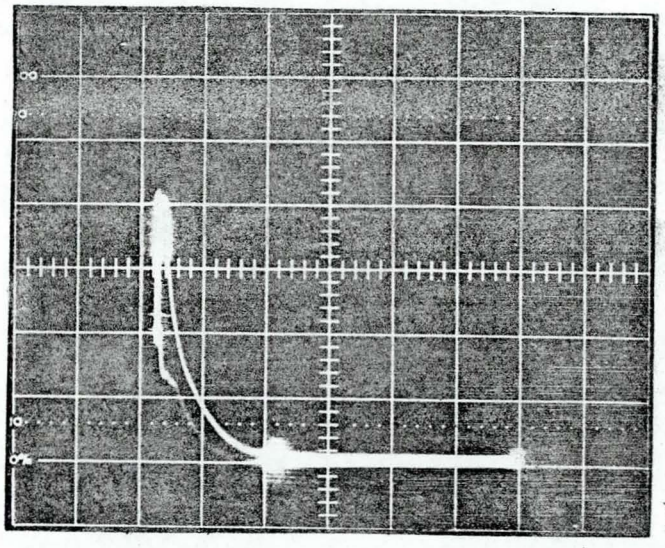


(b) Turn-off Waveforms

Figure 7.26: LOAD LINE SHAPING TO LIMIT dV/dt



(a) Without Snubber



(b) With Snubber

Figure 7.27: I_C/V_{CE} EXCURSION DURING SWITCHING

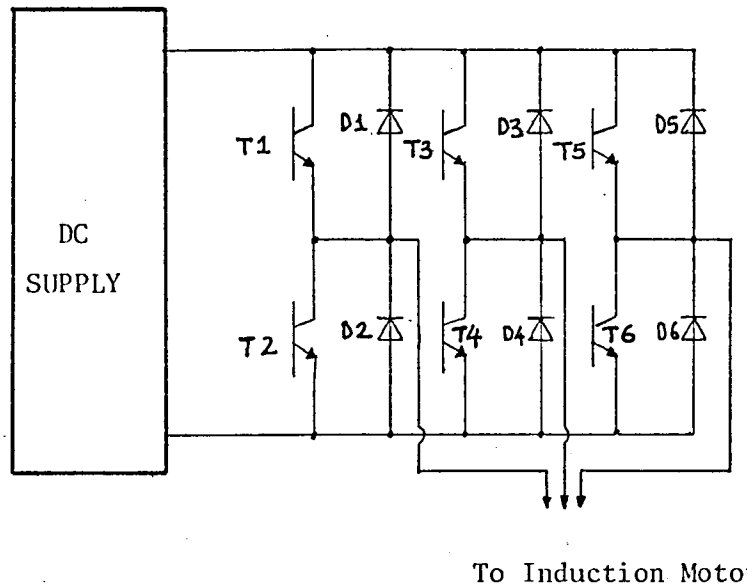


Figure 7.28: BASIC INVERTER

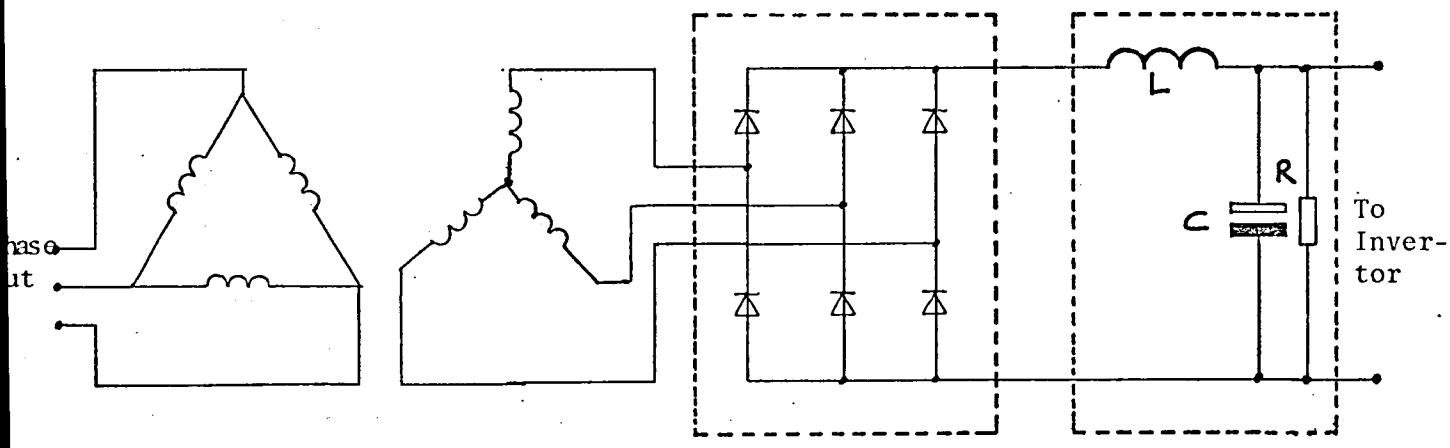
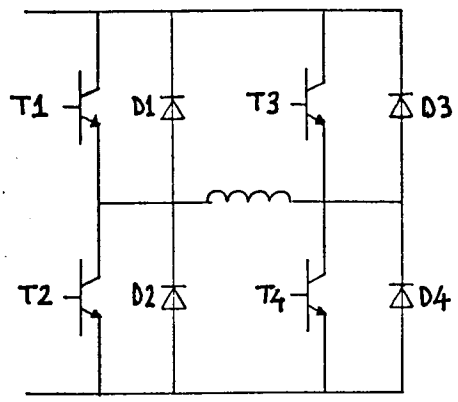
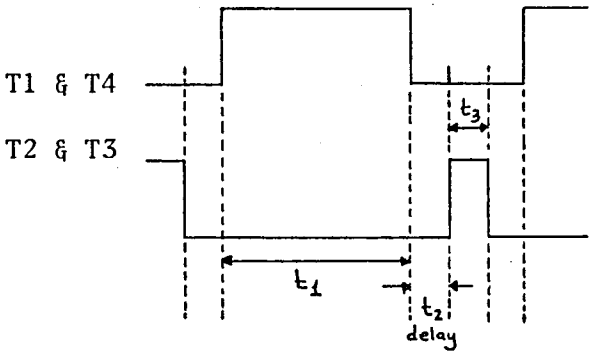


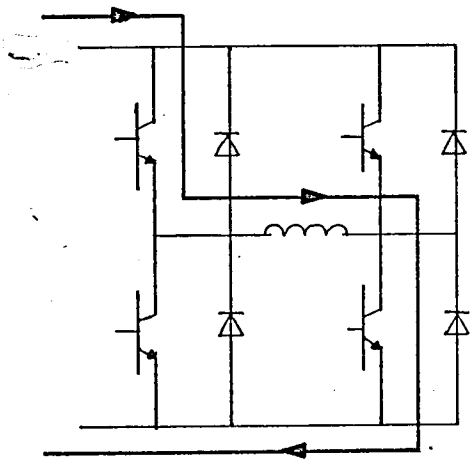
Figure 7.29: VOLTAGE SUPPLY AND SMOOTHING CIRCUIT



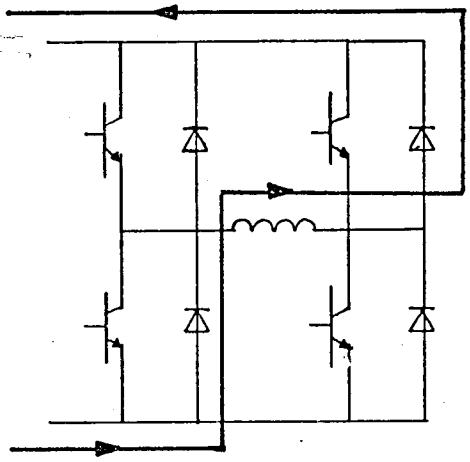
(a) Inverter



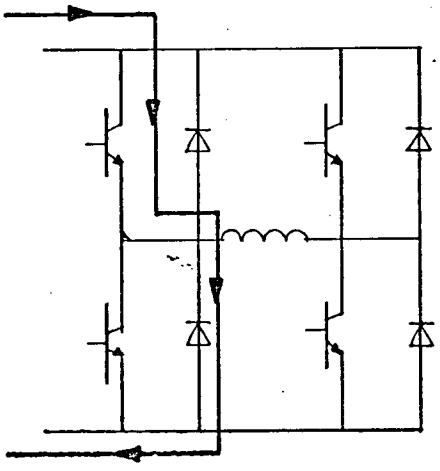
(b) Driving Waveforms



(c)

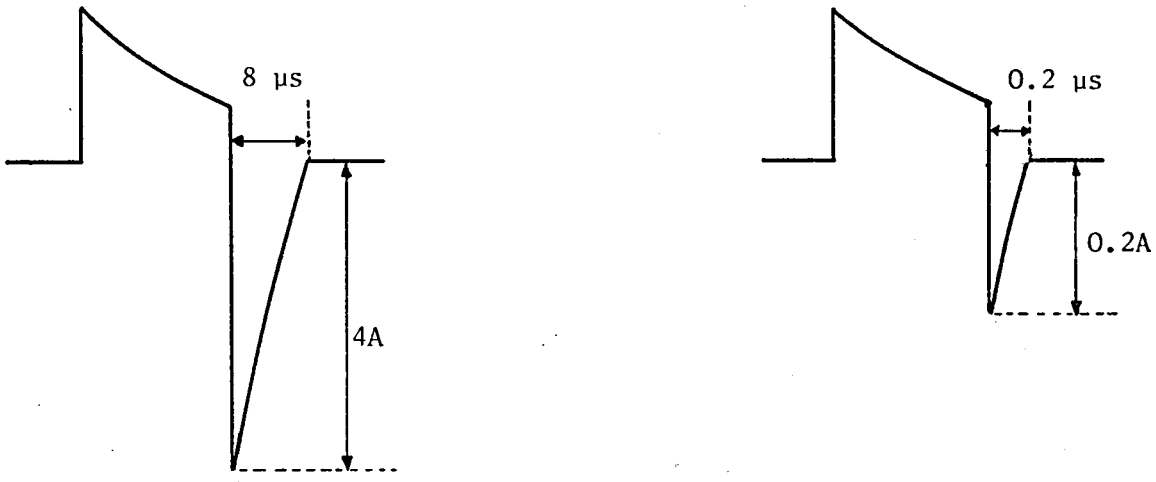


(d)



(e)

Figure 7.30: ACTION OF FAST RECOVERY DIODES



(a) With normal diode (IS425,600V,10A)

(b) With fast recovery diode (IN3893,400V,12A)

Figure 7.31: CURRENT WAVEFORM THROUGH DIODE D2 (at reduced voltage)

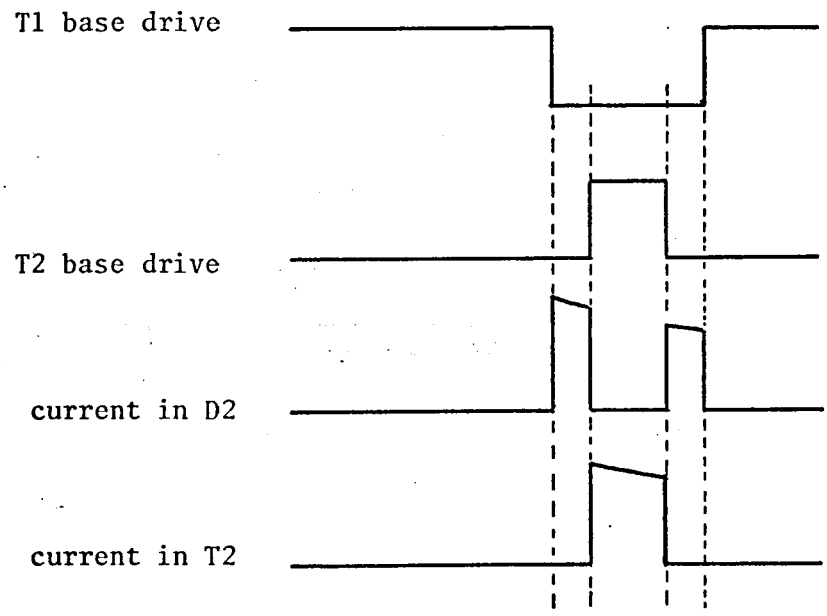


Figure 7.32: INVERSE MODE TRANSISTOR OPERATION, WAVEFORMS

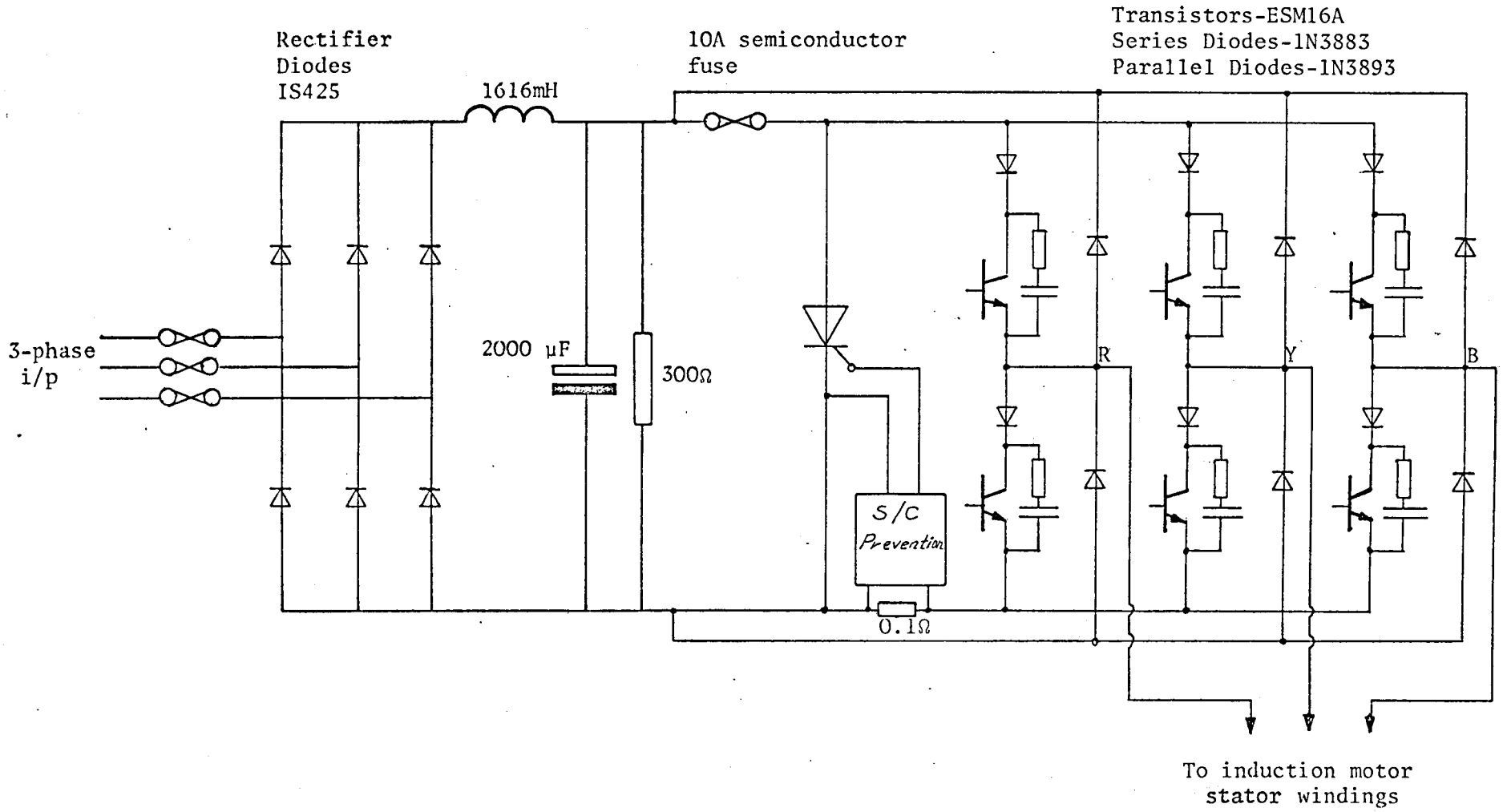


Figure 7.33: CIRCUIT DIAGRAM OF THE INVERTER

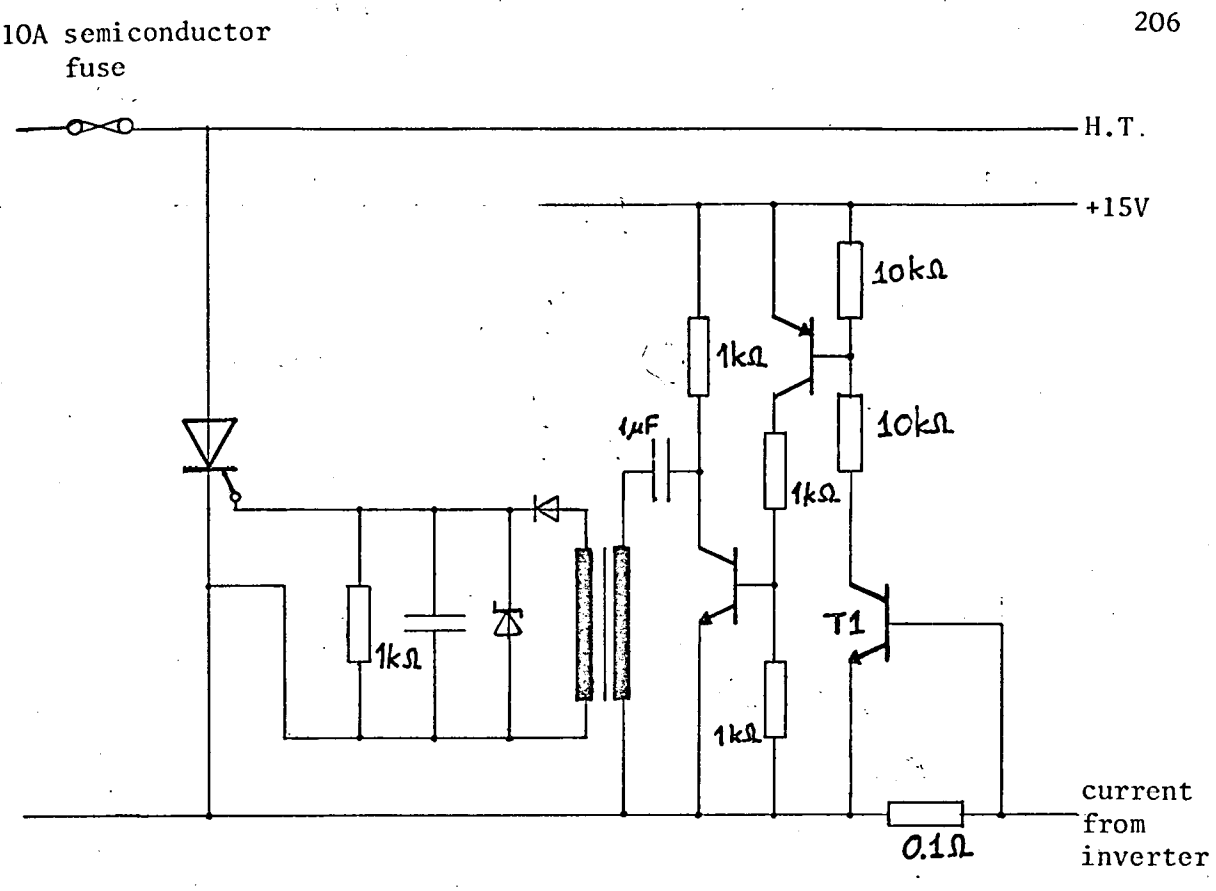
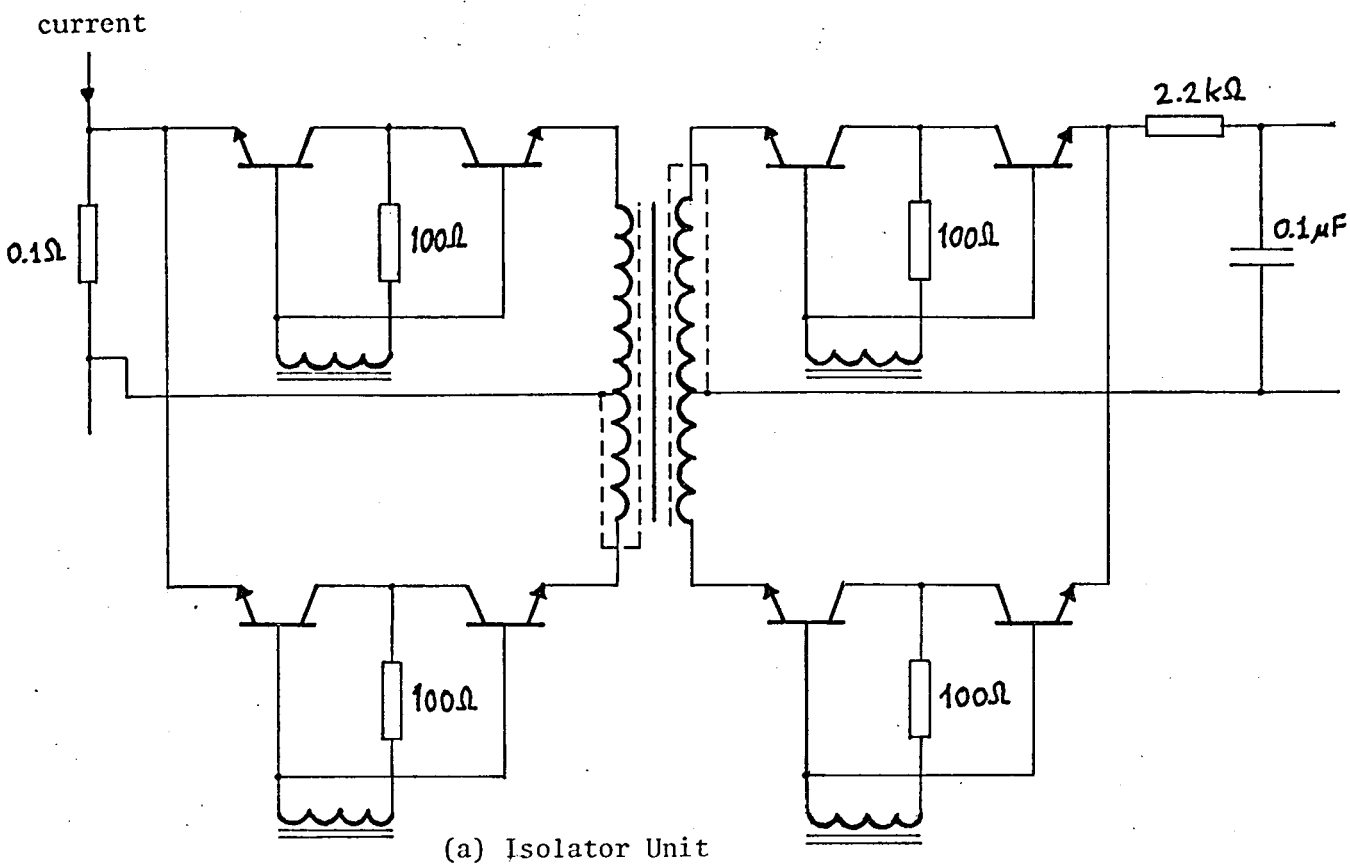
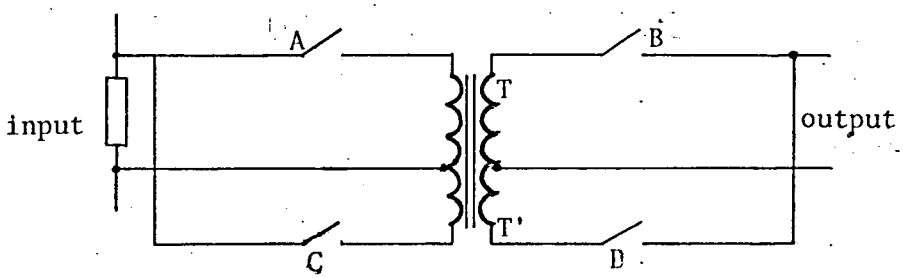


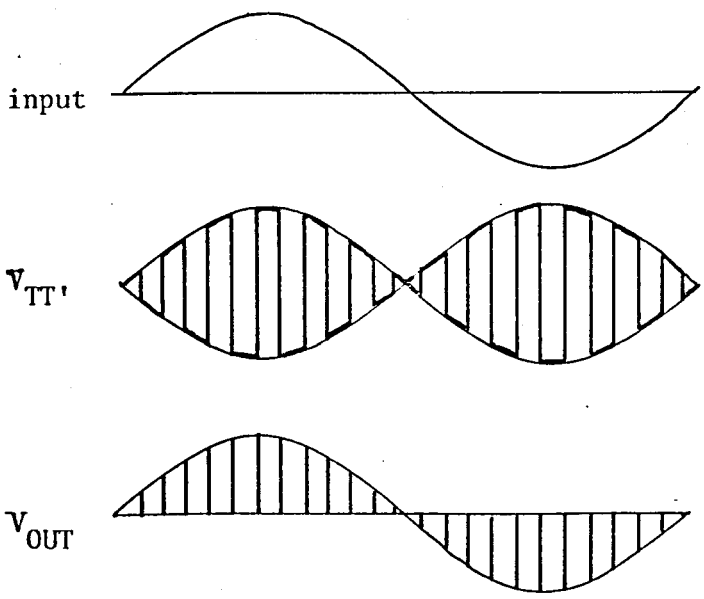
Figure 7.34: OVERCURRENT PROTECTION UNIT



(a) Isolator Unit



(b) Simple Equivalent Circuit



(c) Waveforms

Figure 7.35: CURRENT MONITORING UNIT

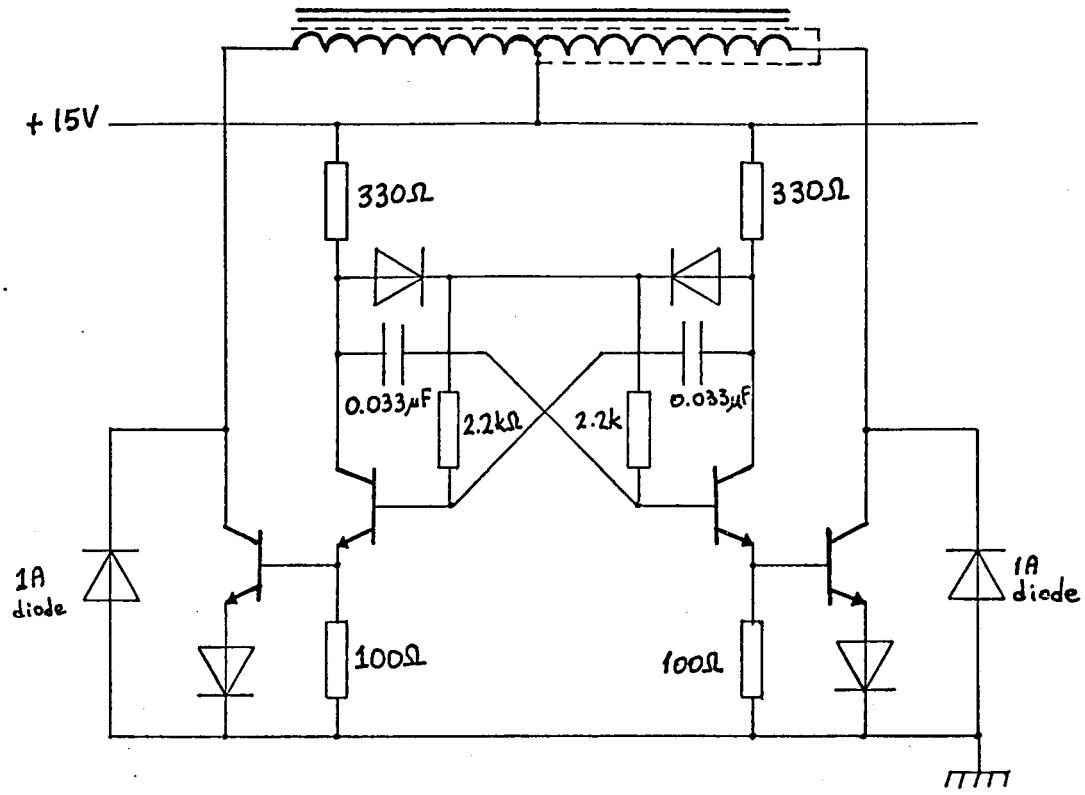
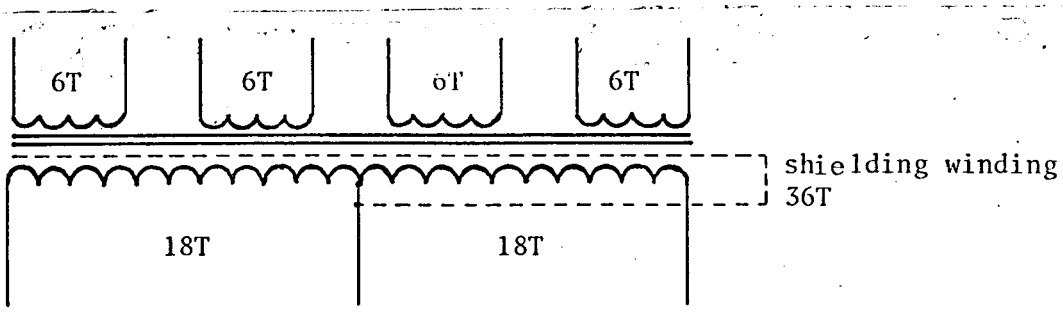


Figure 7.36: ASTABLE MULTIVIBRATOR



transformers are wound on 45mm ferrite pot core
with 27 swg wire

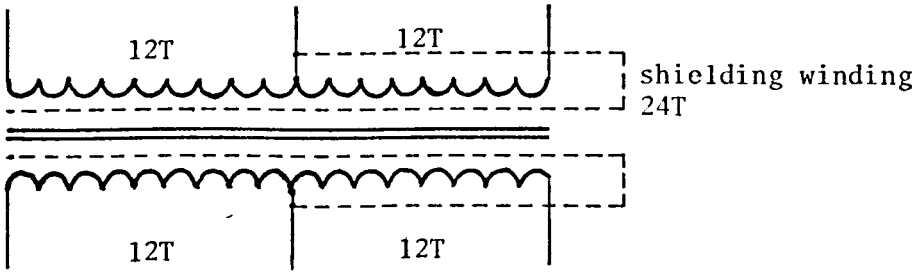


Figure 7.37: WINDING DATA FOR PULSE TRANSFORMERS

CHAPTER 8

EXPERIMENTAL INVESTIGATION AND PERFORMANCE OF INDUCTION MOTOR DRIVEN BY A DELTA-SIGMA MODULATED INVERTER

This chapter is concerned with the performance of an induction motor when supplied by the Δ-Σ modulated inverter, and it describes the results of various tests carried out to assess the potentialities of the system.

At the outset of the chapter, waveforms from different parts of the inverter circuit and with different loads are presented, to provide an appreciation of various operational features associated with the power controller. Since the most efficient use of the inverter is clearly very desirable, switching losses should be kept to a minimum and, with this in mind, these losses are discussed with the aid of experimental data.

The chapter also considers the overall performance of the drive system, along with several relevant and related factors. In particular, the behaviour of an induction motor with a variable-frequency 3-phase sine-wave input is compared with its behaviour when fed with a Δ-Σ modulated input. For this purpose, torque/speed characteristics are presented and discussed.

The Δ-Σ modulated system was designed to enable the motor speed to be controlled continuously and smoothly in both directions, with controllable acceleration and deceleration times. Results presented to illustrate the dynamic performance of the induction motor provide experimental data for an appreciation of the above features in the system developed, as well as of the response of the system to sudden load changes.

8.1 INVERTER WAVEFORMS

Waveforms at various points in the inverter circuit were observed using a Telequipment type DM63 double-beam oscilloscope, with the aid of a current probe and amplifier, when current waveforms were being observed.

8.1.1 Inverter Waveforms with Resistive Load

Figure 8.1 shows waveforms of the voltages across two transistors in different phases of the inverter, with a star-connected resistor bank used

as a 3-phase load. These waveforms are the same as those presented in Figures 5.25.a and 5.26.a, and were obtained at a supply frequency of 50Hz and a clock frequency of 10kHz. Figure 8.2 shows the corresponding line-to-line output voltage waveforms and Figure 8.3 the line-to-neutral output voltage waveforms for two different phases. The action of the power transistors in alternately switching on and off to produce an alternating output is clearly evident.

Line-current waveforms for the two phases are shown in Figure 8.4. Although there is a small inductive effect, due to the use of wire-wound load resistors, the current waveform is not significantly filtered, and the effect of the high switching-frequency is again apparent. With a resistive load, negligible current flows through the freewheeling diodes connected across each power transistor in the inverter, and the power loss in these diodes is very small. Switching the power transistors from one state to another presents no problems with a resistive load.

Figure 8.5 shows the effect of reducing the clock frequency to 5kHz, and Figure 8.6 and 8.7 show the line-to-line output voltage and line current waveforms when the inverter output frequency is 30Hz and the clock frequencies are 10kHz and 5kHz respectively. A comparison of Figures 8.4 and 8.6 reveals that the high switching-frequency effect is more dominant in the line current waveforms at a supply frequency of 30Hz than at 50Hz, although the clock frequency in both cases is the same. The reason for this is the reduced amplitudes of the input sine waves to the Δ-Σ modulators for lower input frequencies. As will be recalled from Section 6.2.4, the absolute value unit increases the amplitudes of the 3-phase sine waves as their frequency is increased, so that for lower output frequencies the action of the Δ-Σ modulators causes more pulses to be present in each period of the output waveforms.

8.1.2 Inverter Waveforms with an Induction Motor Load

Figure 8.8 shows the resulting line-to-line output voltage waveforms and Figure 8.9 the line current waveforms in two different phases of the inverter, with a 3-phase delta-connected induction motor loading the output. Although the voltage waveforms are similar to the resistive load case, the current waveforms are markedly different from those of Figure 8.4. By acting as a low-pass filter, the induction motor eliminates most of the high switching-frequency components, and the current waveshape is very nearly a sine wave.

Figure 8.10 shows the effect of reducing the clock frequency. At lower clock frequencies the modulation is affected, and since some of the higher switching-frequency components are not now filtered by the motor, they cause the motor current waveform to depart somewhat from a sine wave. As the clock frequency is reduced further the motor current harmonics become greater, and significant pulsating torques are produced by interaction between the rotor harmonic currents and the fundamental rotating field. As a result, the motor rotation takes place in a series of jerks or steps, which may set a lower limit to the useful speed range. The clock frequency at which pulsating torques have a noticible effect on the motor speed is observed experimentally at slightly lower than 1kHz. To enable smooth operation at low speeds to be obtained the clock frequency should not be less than this value, and by reducing the harmonic currents this will also keep the motor losses small.

Figure 8.11 shows the line-to-line voltage and line current waveforms for an inverter output frequency of 30Hz with a clock frequency of 10kHz. Comparison of line current waveforms in Figures 8.9 and 8.11 shows that, although the clock frequencies are the same, the lower output frequency gives a current waveform closer to a sine wave, in accordance with the discussion of section 8.1.1. Figure 8.12 shows the effect of increasing

the clock frequency to 20kHz when, as expected, the motor current waveform approximates more closely to a sine wave at the higher clock frequencies. Figure 8.13 shows the current waveforms of the two power transistors in one branch of the inverter, and it will be seen that one transistor carries the load current for one half the period and the other provides a path for the load current during the remaining half period.

With inductive loading, the freewheeling diodes connected across each power transistor return the reactive energy in the motor windings to the supply, when the transistors are turned off and the switching sequence changes. Current waveforms for a transistor and a diode are shown in Figure 8.14, and in expanded form in Figure 8.15 to enable the freewheeling effect to be more easily observed. It will be seen from Figure 8.15 that, when a transistor switches off, current is transferred to the freewheeling diode until the transistor switches on again. During this time the diode current decays slowly, but since the time period is short it does not fall to zero. This confirms the assumptions made in section 7.4.3, where it was pointed out that freewheeling diodes should have a fast recovery time. Since their forward voltage drops affect the efficiency of the inverter, fast-recovery diodes with small forward drops must be used.

The voltage and current waveforms presented above show that the inverter functions satisfactorily, and provides a 3-phase variable-frequency sine wave output suitable for controlling the speed of an induction motor. As the clock frequency is increased the motor currents approximate more closely to the sine wave necessary to keep the losses of the induction motor at an acceptable level.

8.2 EFFICIENCY OF THE INVERTER

This section investigates the inverter losses for both resistive and inductive loading, although since the inverter incorporates fast switching

power transistors, the losses are expected to be small. The inverter losses have three components

a) those during the on state of the transistors, which are proportional to the saturation voltage $V_{CE(SAT)}$ and the collector current I_C.

b) those during the off state of the transistors, which are proportional to the collector-emitter voltage and the leakage current through the transistors.

c) those when transistors switch from the on to the off state or vice versa.

There is an additional although small loss in the series and parallel diodes in the inverter circuit.

The losses under both (a) and (b) can easily be determined from the power transistor characteristics. For a maximum collector-emitter voltage of 200V and a maximum collector current of 5A, this loss is limited to about 15W for all the six transistors (type ESM16A) used in the inverter. Increasing the base currents of the transistors will reduce the collector-emitter saturation voltage $V_{CE(SAT)}$ and hence the loss in case (a). However, it will also increase the storage time of the transistors and thereby limit the maximum switching frequency. Similarly, increasing the negative drive voltage will reduce the leakage current through the transistors,so that the loss in case (b) is kept to a minimum. Nevertheless, since the losses in cases (a) and (b) are only a small proportion of the total loss, an increase in the positive and negative base drive will not have any appreciable effect on the overall efficiency of the inverter. However, the loss in case (c) is one of the most important parameters in the operation of power transistors, especially when the load is inductive. Careful design considerations are needed to limit it to the safe level determined by the maximum power dissipation that will not cause the maximum junction temperature of the power transistors to be exceeded. By preventing excessive dissipation in the power transistors, the snubber circuit described in section 7.3.3 enables

safe operation of the inverter. The snubber circuit does not alter the efficiency, as discussed in Section 7.3.3.

Figure 8.16 shows the variation in the total inverter losses as a function of the switching frequency, for both resistive and inductive loads. The losses are obtained as the difference between the input power as derived from the input voltage and current and the output power as measured by two wattmeters. The inverter output frequency is kept constant at 50Hz and measurements are presented for an input voltage of 200V and an output current of 5A. It can be seen that although for a resistive load the inverter losses are small, they increase linearly with the switching frequency. For an inductive load the inverter losses are larger, and increase more rapidly at higher clock frequencies. Although Figure 8.16 ignores the power loss in the base-emitter junction, this will be negligible in comparison with the total inverter loss. The increase in the inverter loss for inductive loading is mainly due to the increased switching losses discussed above for case (c), although the forward drops of the freehweeling diodes now also contribute to the total inverter losses. Although these losses are not likely to present any problems in normal operating conditions, since they are dissipated in the semiconductor devices, an overload condition may result in inverter failure because the small thermal capacity of the inverter transistors causes them to heat up very rapidly. Although the induction motor may carry large overcurrents for quite considerable intervals of time without undue overheating, these same overloads would cause destructive heating in a transistor in a fraction of a second. For this reason, it must be ensured that power transistors are mounted on efficient heatsinks which conduct heat away from the temperature-sensitive junctions. For the same reason, direct-on line starting is not advisable, especially with a transistorized inverter, unless a current limiter is incorporated as part of the overall system.

Figure 8.17 shows the efficiency of the inverter as a function of the

output power, for three different clock frequencies and with a star-connected inductive load. Since the measurements were taken with moving-coil instruments they are subject to some error, but they do indicate that the efficiency is very high, especially at lower clock frequencies. Despite harmonic currents causing the motor losses to be high at lower frequencies, an optimum situation can be reached with an inverter efficiency of above 90%. Assuming that the inverter efficiency is not to be lower than 90%, Figure 8.17 shows that the maximum switching frequency is limited to about 40kHz. Although this is sufficient to ensure satisfactory encoding and also to keep the motor current as a good approximation to a sine wave, better power transistors with smaller switching losses must be used if higher clock frequencies are required. Figure 8.17 shows further that, as the output power decreases, the fixed losses in the inverter cause the efficiency to drop. The fall in the inverter efficiency at large output powers evident in Figure 8.17 is due to saturation of the power transistors. It will also be noticed in Figure 8.17 that, for higher switching-frequencies, the fall in efficiency begins to occur at smaller output powers.

The inverter efficiency at low output frequencies is slightly less than that given by Figure 8.17, since more pulses are then present in each period of the output waveform. Although the reduction is small, each transistor carries the full input current for an appreciable interval and their rating must be decided accordingly.

8.3 TORQUE-SPEED CHARACTERISTICS

The torque-speed characteristics of an induction motor with a variable-frequency input have been discussed theoretically in section 2.1.4, on the basis of an equivalent circuit. In the present section, experimental torque-speed characteristics are first presented for a motor (details of which are given in Figure 8.18) supplied with a balanced 3-phase sine wave input, so

that the validity of the assumptions made in Chapter 2 is clearly demonstrated. The measurements were taken such that when the stator frequency was reduced the input voltage was also reduced in proportion, and the air-gap flux density was maintained at approximately its rated value. The experiment was then repeated with the Δ-Σ modulated inverter supplying the test motor, to enable a comparison of the two cases to be made and the behaviour of the induction motor with a Δ-Σ modulated input to be evaluated.

8.3.1 Sine Wave Input

A 3-phase variable-frequency sine wave input was obtained for the test induction motor using the experimental set-up of Figure 8.18, with the test motor coupled to a d.c. generator for loading purposes. The speed of the d.c. motor determines the frequency of the alternator output, whereas the field control of the alternator enables the amplitude of the output voltage to be controlled.

Figure 8.19.a shows torque-speed characteristics at the different supply voltages and frequencies detailed in Figure 8.19.b. A comparison between Figures 8.19.a and 2.4 shows that the torque-speed characteristics are as predicted theoretically. One notable feature of the characteristics of Figure 8.19.a is the reduction in pull-out torque at the lower stator frequencies, which may appear unexpected at first since the ratio V/f is kept constant. However, when a machine is controlled according to this relationship, the amplitude of the input voltage is not controlled as a function of the load, and the pull-out torque at a diminished stator frequency is less than at rated frequency since the flux density in the motor then decreases more with load. The resultant deviation of the pull-out torque from the rated-frequency and voltage level is more pronounced at the lower stator frequencies, due to the increased significance of the resistive voltage drops.

8.3.2 Delta-Sigma Modulated Input

Figure 8.20 shows torque-speed characteristics obtained with the motor supplied from the Δ-Σ modulated inverter supply. At each input frequency the fundamental component of the inverter output voltage is made equal to the corresponding voltage with the motor supplied from the sine wave input, by using a wave analyser. As can be seen, the two characteristics of Figures 8.19 and 8.20 are closely similar.

For a further comparison of the behaviour of the machine on the two supplies, the variation of pull-out torque with supply frequency is given in Figure 8.21. The amplitude of the input voltage is here increased somewhat at low frequencies to allow for the increased resistive voltage drops, and the Δ-Σ modulated supply gives almost the same characteristics as the sine wave supply. It will also be seen that when the clock frequency is reduced the pull-out torque is also reduced, because of the affect produced as the modulation is affected. The reduction at higher speeds is caused by overloading of the modulators, and this can easily be avoided by reducing the input to the modulator and increasing the d.c. supply level to the inverter. Adjustment of the gain of the V/f control unit of Figure 6.26 is sufficient for this purpose. This facility for adjustment of the control characteristics to maintain the motor flux density close to its rated value constitutes a very important advantage of static inverter systems over a competitive motor-alternator system. Such systems lack the ability to produce a sufficient increase in the low-speed torque, owing to the inability of rotating generators to provide the necessary increase in the voltage-to-frequency ratio, unless they are considerably increased in size.

Figure 8.22 shows the variation of starting torque with supply frequency, with the voltage-to-frequency ratio again kept constant. Over the upper part of the range of frequency the starting torque decreases with an increase in the supply frequency, whereas for the lower part of the range

it increases with frequency. This is as predicted by theory, and can easily be verified by substituting s=1 in equation 2.12. It should also be noted that if the motor is started at a high voltage and frequency, in a manner corresponding to direct-on-line starting on a normal supply, not only is the starting torque relatively poor, but the starting current is many times the full-load level and the inverter rating required is considerably increased. To avoid this obviously undesirable outcome, the motor should be started by increasing the frequency and voltage gradually from low initial values. As Figure 8.22 shows, the two characteristics obtained with the sine wave and the Δ-Σ modulated supplies are essentially the same.

8.4 EFFICIENCY OF THE INDUCTION MOTOR

In this section the efficiency of the induction motor used in the tests is investigated, with both a sine wave supply and a Δ-Σ modulated supply, to determine qualitatively the additional losses which are present with non-sinusoidal exictation. Figure 8.23 shows the variation of the efficiency with output power at rated input frequency, and when fed from the Δ-Σ modulated inverter, when the motor efficiency is seen to be slightly reduced. This is due mainly to the increased stator losses which arise with non-sinusoidal excitation, when the increased leakage flux produced by the harmonic currents results in a higher magnetising current. The harmonic copper loss in the rotor is also an important factor in the reduced efficiency, and a low-resistance rotor may be needed to significantly reduce this effect.

The above losses cause additional motor heating and, with small motors, the minimum frequency is often limited to about 10Hz by the need to prevent overheating due to the reduced ventilation at low speeds. The upper limit of the speed is restricted by the increased core loss as the frequency of the supply voltage rises, although up to a certain level these can be

dissipated by the built-in fan. However, if the frequency is further increased a drop in torque has to be accepted (the upper limit of the supply frequency to standard induction motors is normally about 150-200Hz).

Although Figure 8.23 shows that the efficiency is slightly reduced with a Δ-Σ modulated supply, keeping the switching frequency high ensures that the losses are kept to a minimum. This will also limit the temperature rise of the motor when prolonged operation at low speeds is required, or if speed reversals are frequently made.

8.5 DYNAMIC PERFORMANCE OF THE SYSTEM

Although induction motors do not usually become unstable on an infinite system, an oscillatory response can be predicted[31-32] if the supply frequency is sufficiently reduced, especially for small motors with a low inertia constant. The stability may be improved by reducing the magnetizing reactance and increasing the stator and rotor resistances in such cases.

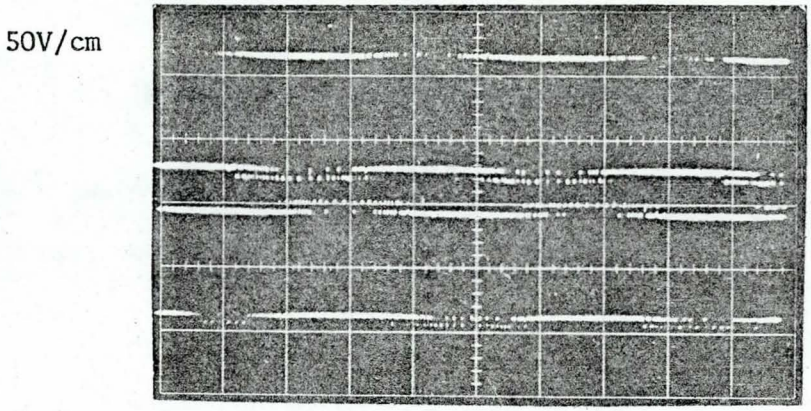
Another source of instability arises from the inveraction between the motor and inverter, since the inverter has a finite source impedance. This impedance may be introduced by a transformer or by the filter which smooths the d.c. supply. At low frequencies instability may occur[33] through an interchange of energy between the motor inertia and the filter inductance and capacitance, although in many cases this may be eliminated by altering the value of the filter capacitance. However, when the test motor was supplied with the Δ-Σ modulated inverter, these effects were not observed. The system was stable over a wide speed range and responded well to sudden load changes in load to speed. To illustrate this, Figure 8.24 shows ultra-violet recordings of the motor speed and current following a step change in speed, for three different settings of the acceleration control. Under the action of this unit, a run-up from standstill can be achieved more quickly than by the usual step application of power at rated frequency. The machine

currents are also smaller, but the optimum rate of change of frequency is dependent on the load inertia.

A complete speed reversal from full speed in one direction to full speed in the opposite direction also takes a shorter time when the voltage and frequency are varied uniformly with time, as is evident from Figure 8.25 which shows the effect of different settings of the acceleration and deceleration control. As can be seen, the system behaves as expected and the acceleration and deceleration times can be controlled. To accelerate the loaded motor requires larger currents than when the motor is unloaded, as shown in Figure 8.26 where the motor speed and currents are shown for two different settings of the acceleration control.

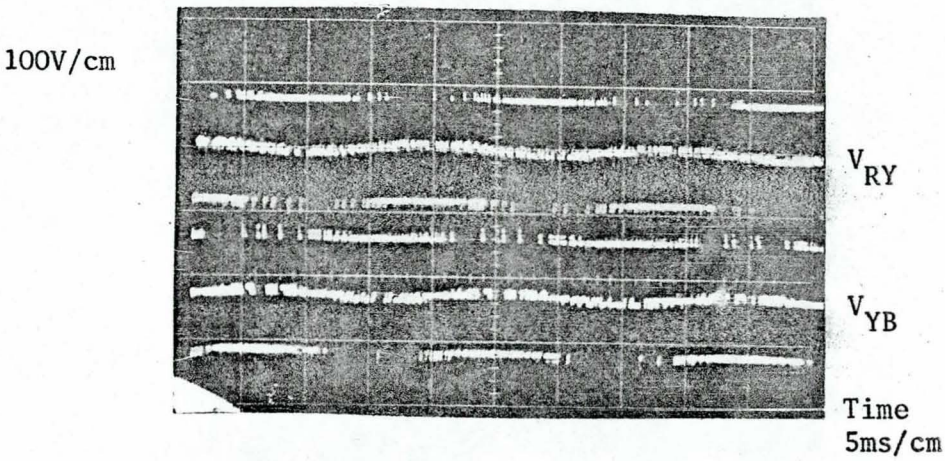
Figures 8.27.a and 8.27.b show the motor current and speed following the sudden application and removal of load. When load is applied the motor speed reduces and the current increases, and the reduction in speed can only be avoided by closed-loop techniques, as described in the next chapter.

As discussed in section 6.2.3, the system developed has the facility of speed reversal by the inherent action of the 3-phase voltage controlled oscillator, and this can be seen from Figure 8.28 which shows the motor currents in two phases of the test motor during a speed reversal.



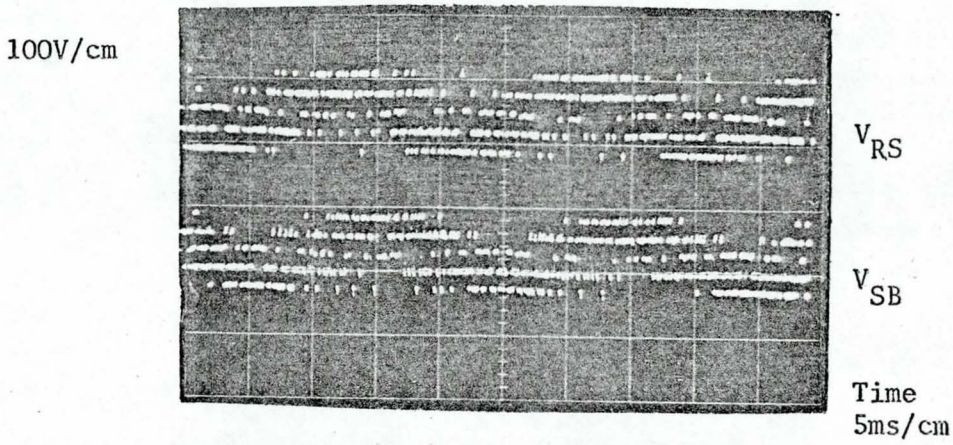
fc = 10kHz, fs = 50Hz

Figure 8.1: VOLTAGE WAVEFORMS ACROSS TWO TRANSISTORS
(Two Different Phases)



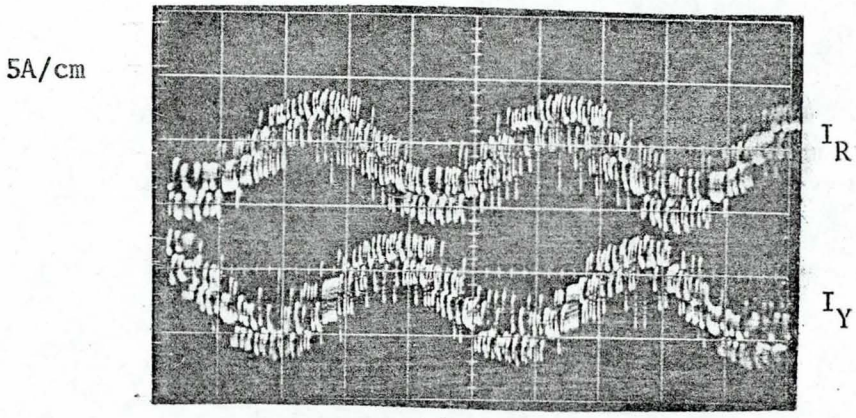
fc = 10kHz, fs = 50Hz

Figure 8.2: LINE TO LINE OUTPUT VOLTAGE WAVEFORMS



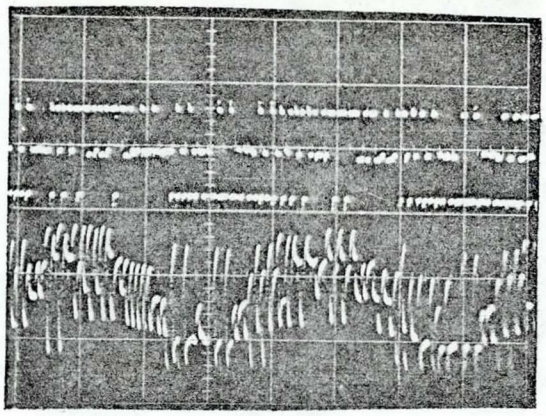
fc = 10kHz, fs = 50Hz

Figure 8.3: LINE TO NEUTRAL OUTPUT VOLTAGE WAVEFORMS



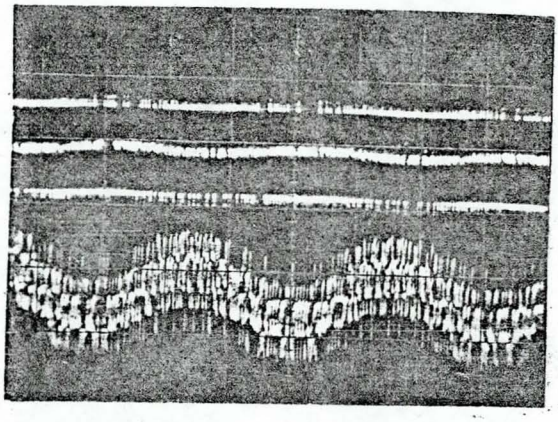
fc = 10kHz, fs = 50Hz

Figure 8.4: LINE CURRENT WAVEFORMS



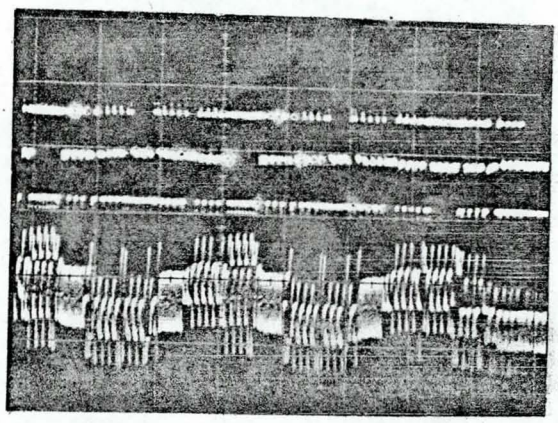
fc = 5kHz, fs = 50Hz

Figure 8.5: LINE TO LINE VOLTAGE AND LINE CURRENT WAVEFORMS



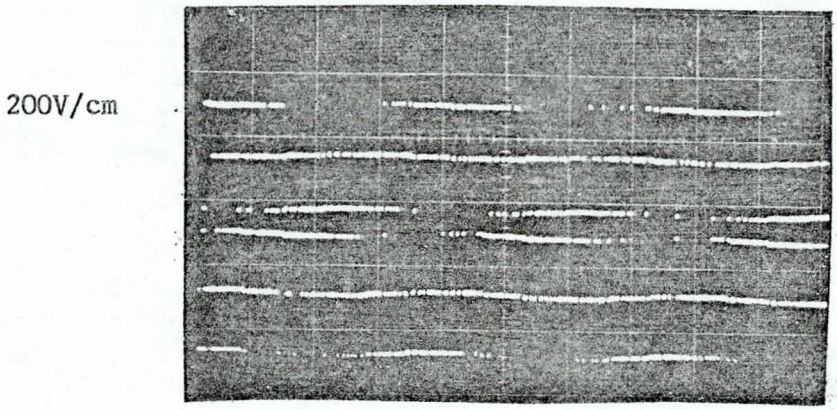
fc = 10kHz, fs = 30Hz

Figure 8.6: LINE TO LINE VOLTAGE AND LINE CURRENT WAVEFORMS



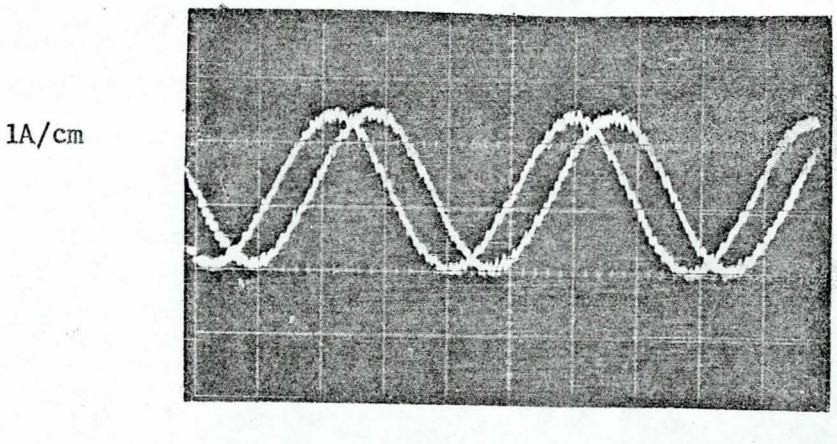
fc = 5kHz, fs = 30Hz

Figure 8.7: LINE TO LINE VOLTAGE AND LINE CURRENT WAVEFORMS



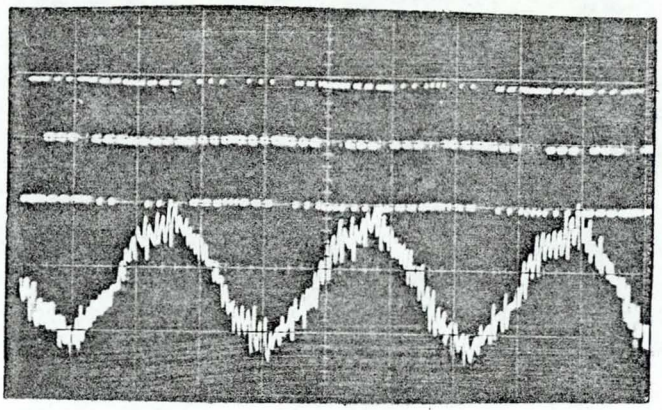
fc = 10kHz, fs = 50Hz

Figure 8.8: LINE TO LINE VOLTAGE WAVEFORMS WITH INDUCTIVE LOAD



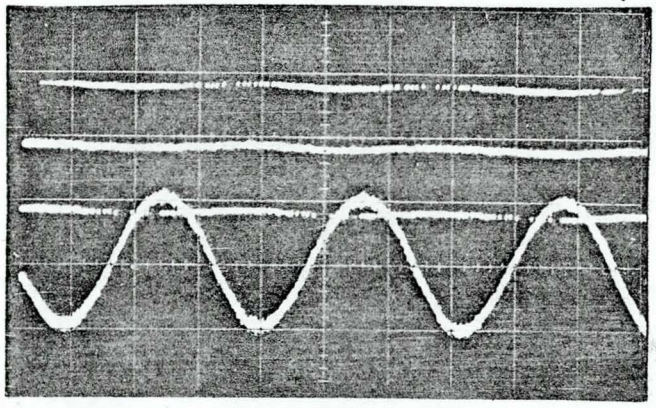
fclock = 10kHz, fs = 50Hz

Figure 8.9: LINE CURRENT WAVEFORMS WITH INDUCTIVE LOAD



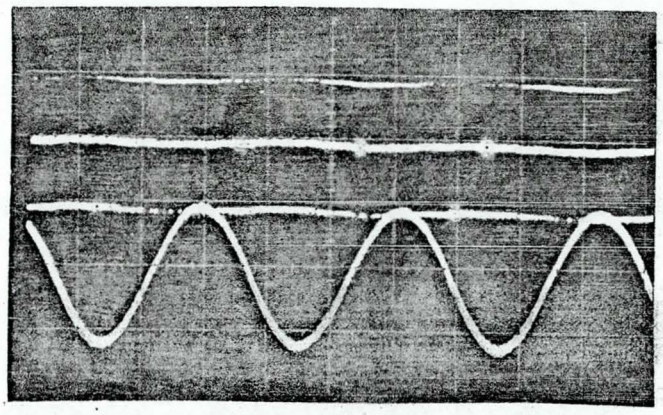
fc = 3kHz, fs = 30Hz

Figure 8.10: LINE TO LINE VOLTAGE AND LINE CURRENT WAVEFORMS WITH INDUCTIVE LOAD



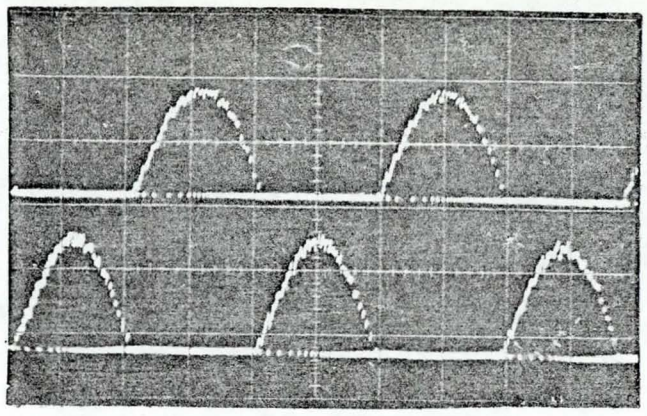
f_c = 10kHz, fs = 30Hz

Figure 8.11: LINE TO LINE VOLTAGE AND LINE CURRENT WAVEFORMS WITH INDUCTIVE LOAD



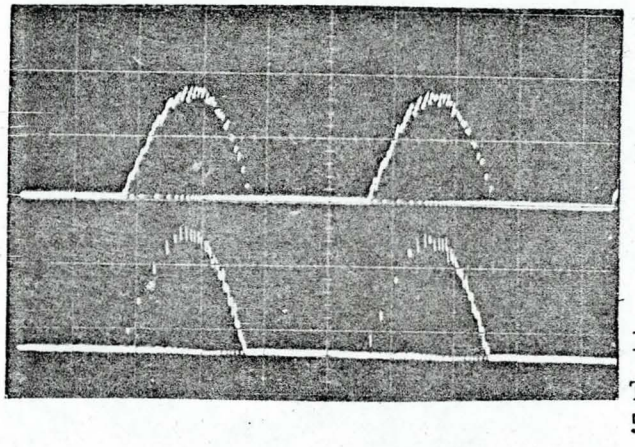
fc = 20kHz, fs = 30Hz

Figure 8.12: LINE TO LINE VOLTAGE AND LINE CURRENT WAVEFORMS WITH INDUCTIVE LOAD



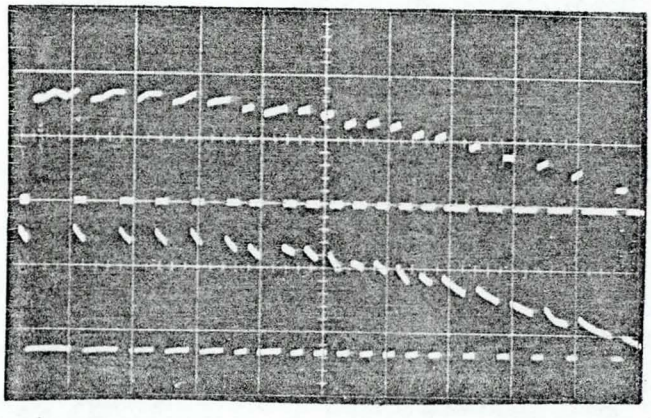
fc = 10kHz, fs = 50Hz

Figure 8.13: CURRENT WAVEFORMS FOR THE TWO TRANSISTORS IN ONE BRANCH OF THE INVERTER



fc = 10kHz, fs = 50Hz

Figure 8.14: TRANSISTOR AND FREWHEELING DIODE CURRENT WAVEFORMS



fc = 10kHz, fs = 50Hz

Figure 8.15: TRANSISTOR AND FREWHEELING DIODE CURRENT WAVEFORMS

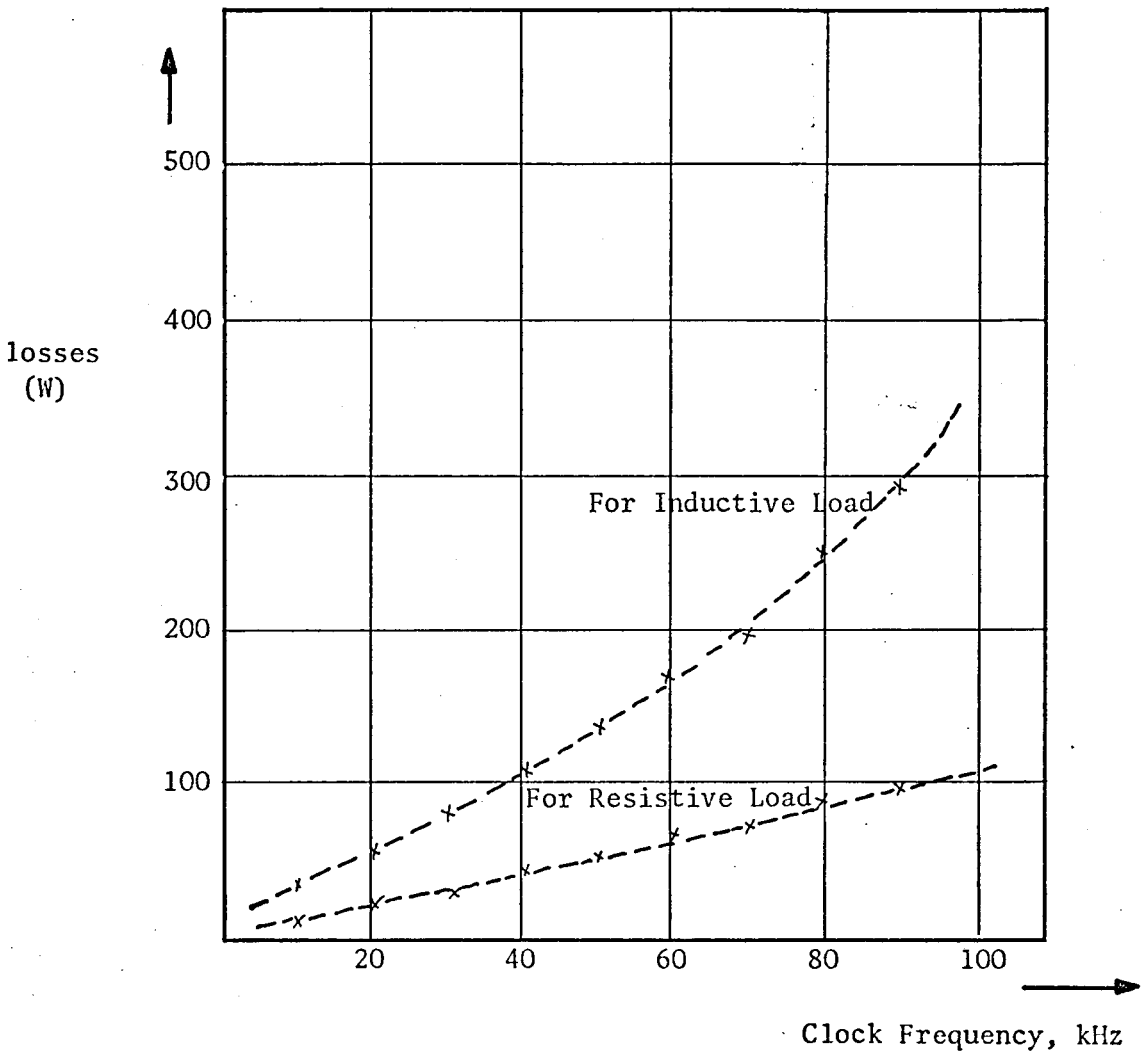


Figure 8.16: LOSSES OF THE INVERTER VS. CLOCK FREQUENCY

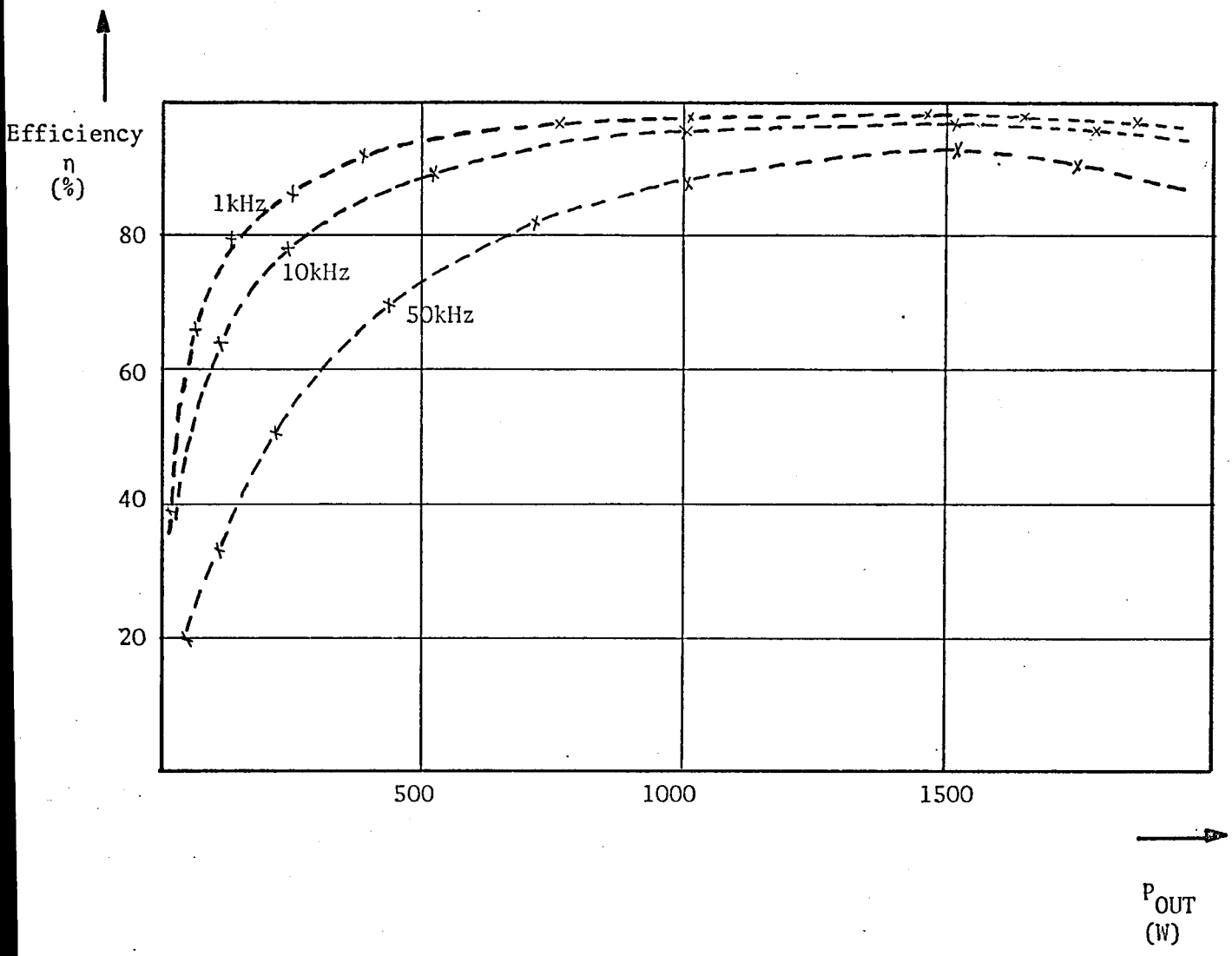
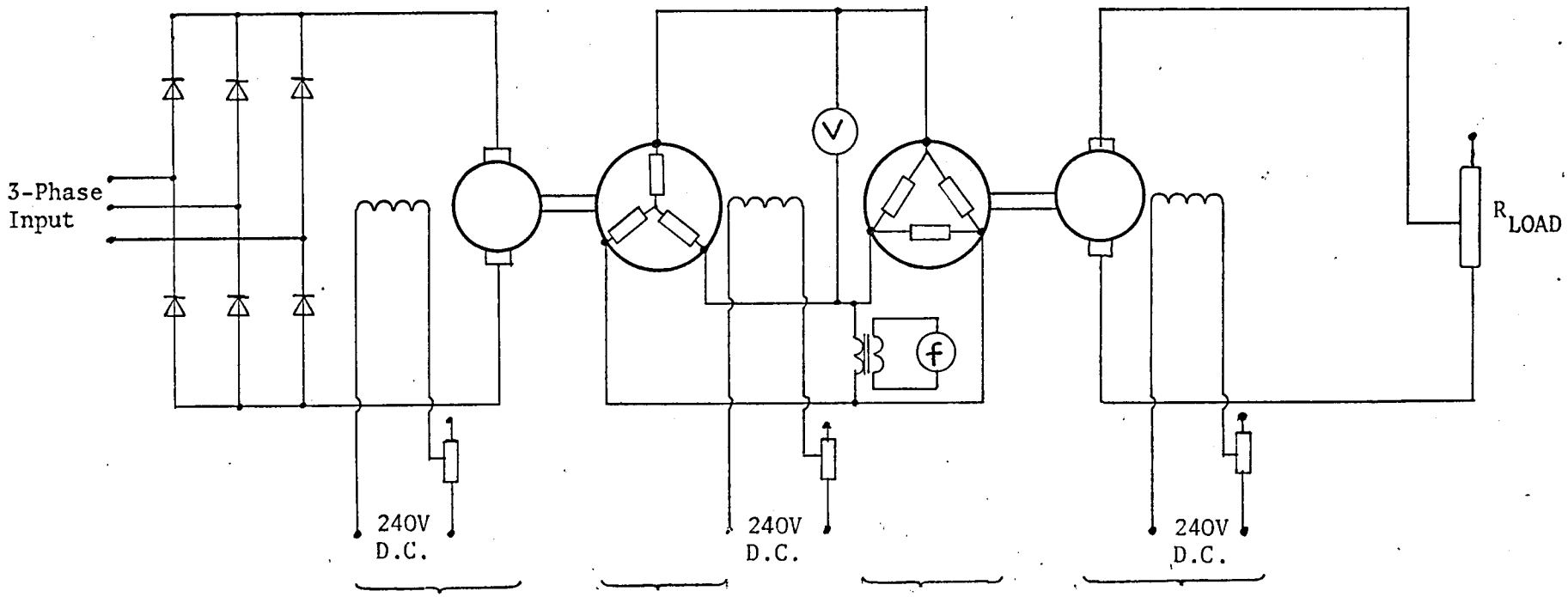
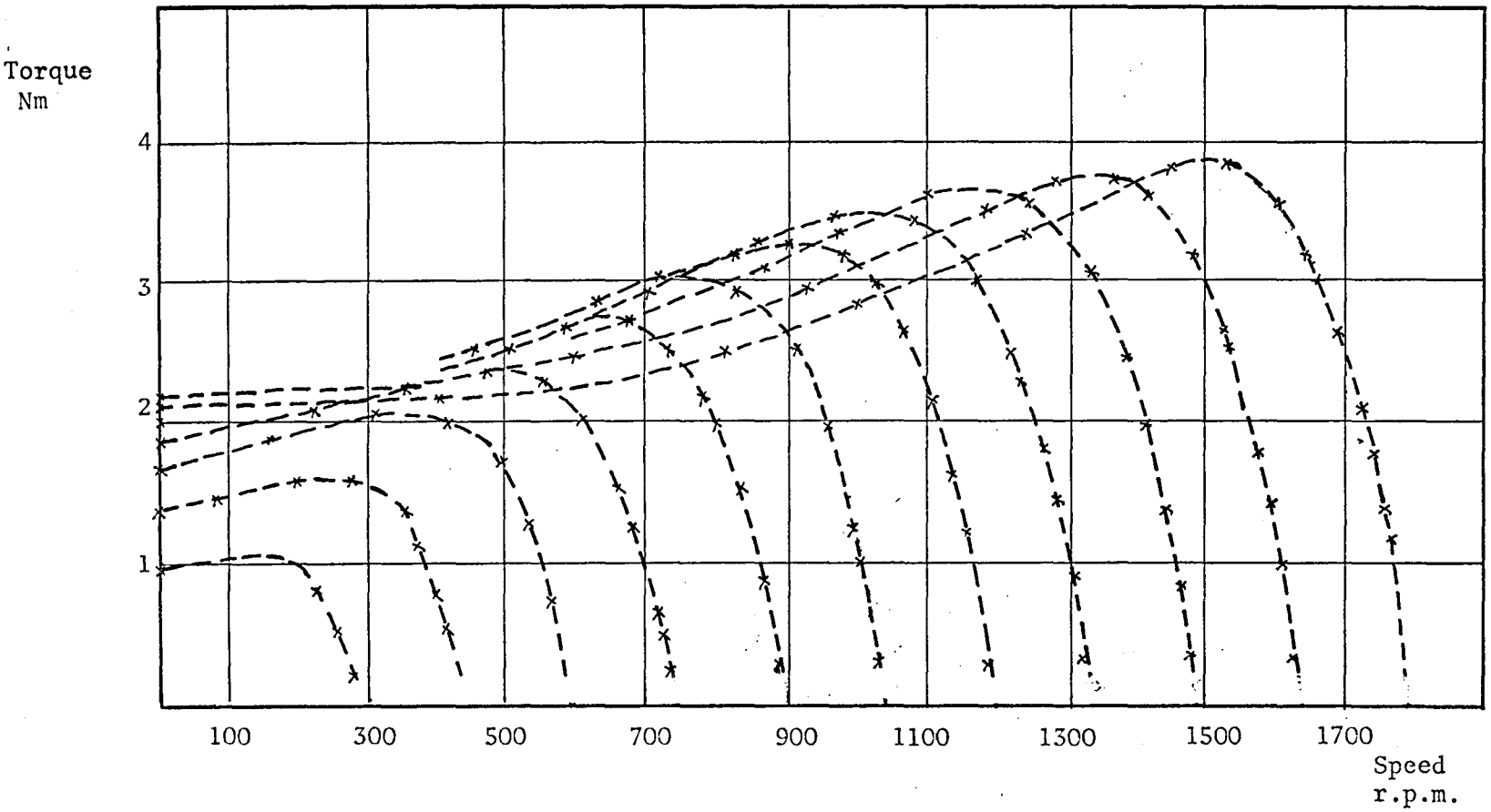


Figure 3.17: INVERTER EFFICIENCY (With Inductive Load)



D.C. Motor	Alternator	Induction Motor	D.C. Generator
230V	5kVA	.25kw	240V
8.5 BHP	3 ph	140V/3-ph	1400 r.p.m.
1750 r.p.m.	240Va.c.	50 ∿/2.1 A	
	1500 r.p.m.	1400 r.p.m.	
		Pole no=2	

Figure 8.18: EXPERIMENTAL SET-UP



(a)

Input Voltage (V)	Supply Frequency (Hz)
168	60
154	55
140	50
126	45
112	40
98	35
84	30
70	25
56	20
42	15
28	10

(b)

Figure 8.19: TORQUE-SPEED CHARACTERISTICS WITH SINE WAVE SUPPLY

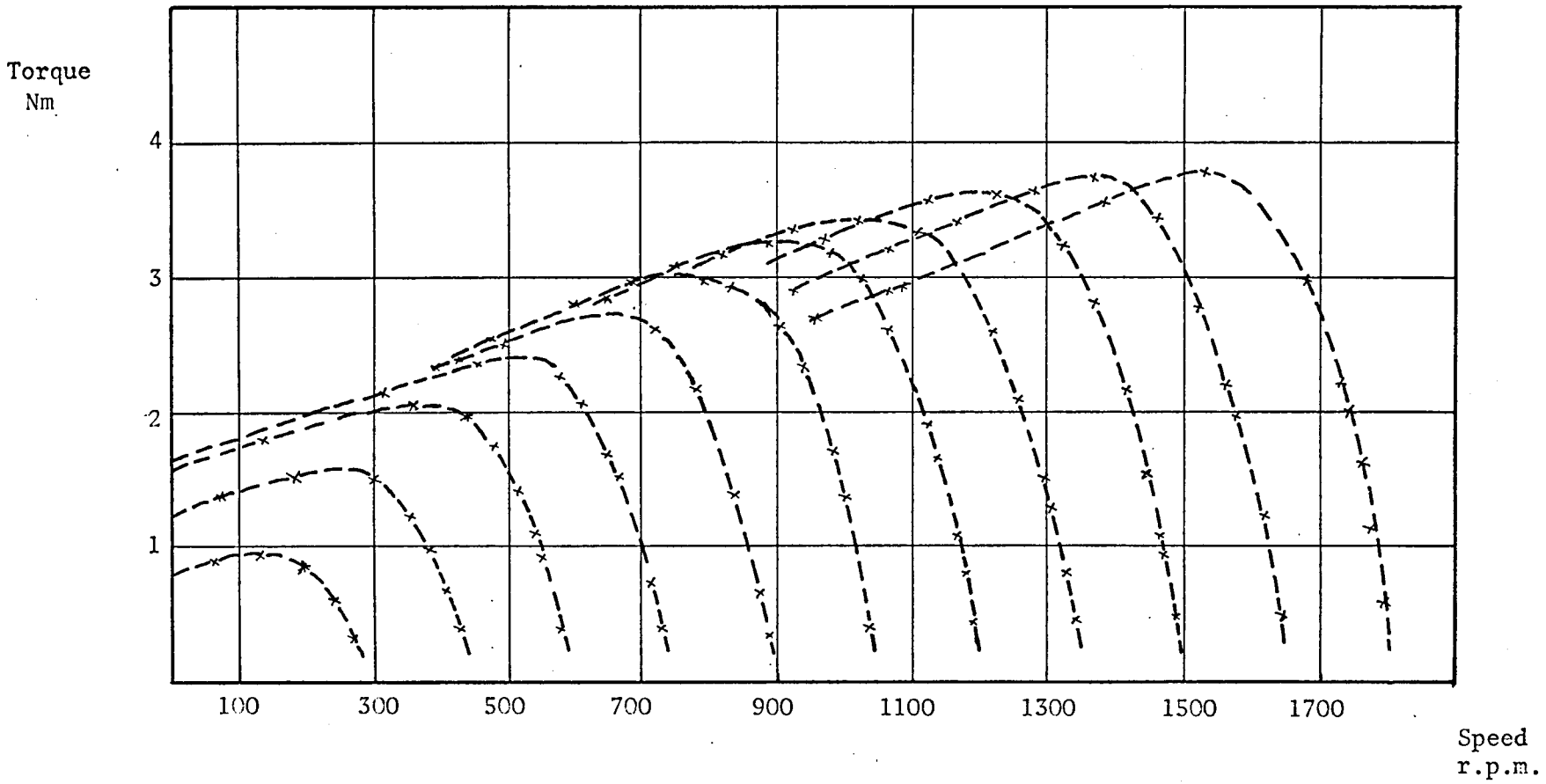


Figure 8.20: TORQUE-SPEED CHARACTERISTICS WITH Δ-Σ MODULATED SUPPLY

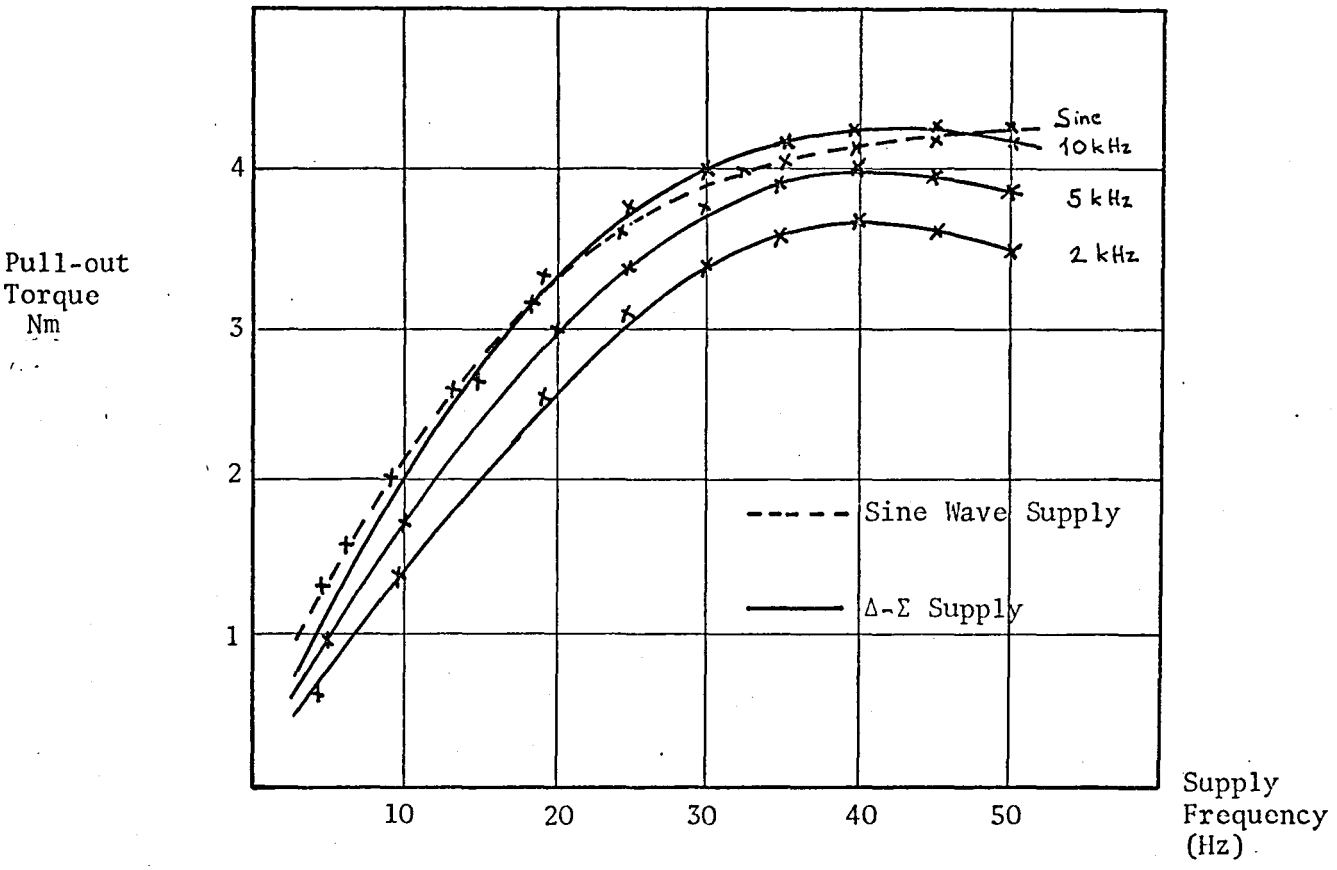


Figure 8.21: VARIATION OF PULL-OUT TORQUE WITH SPEED

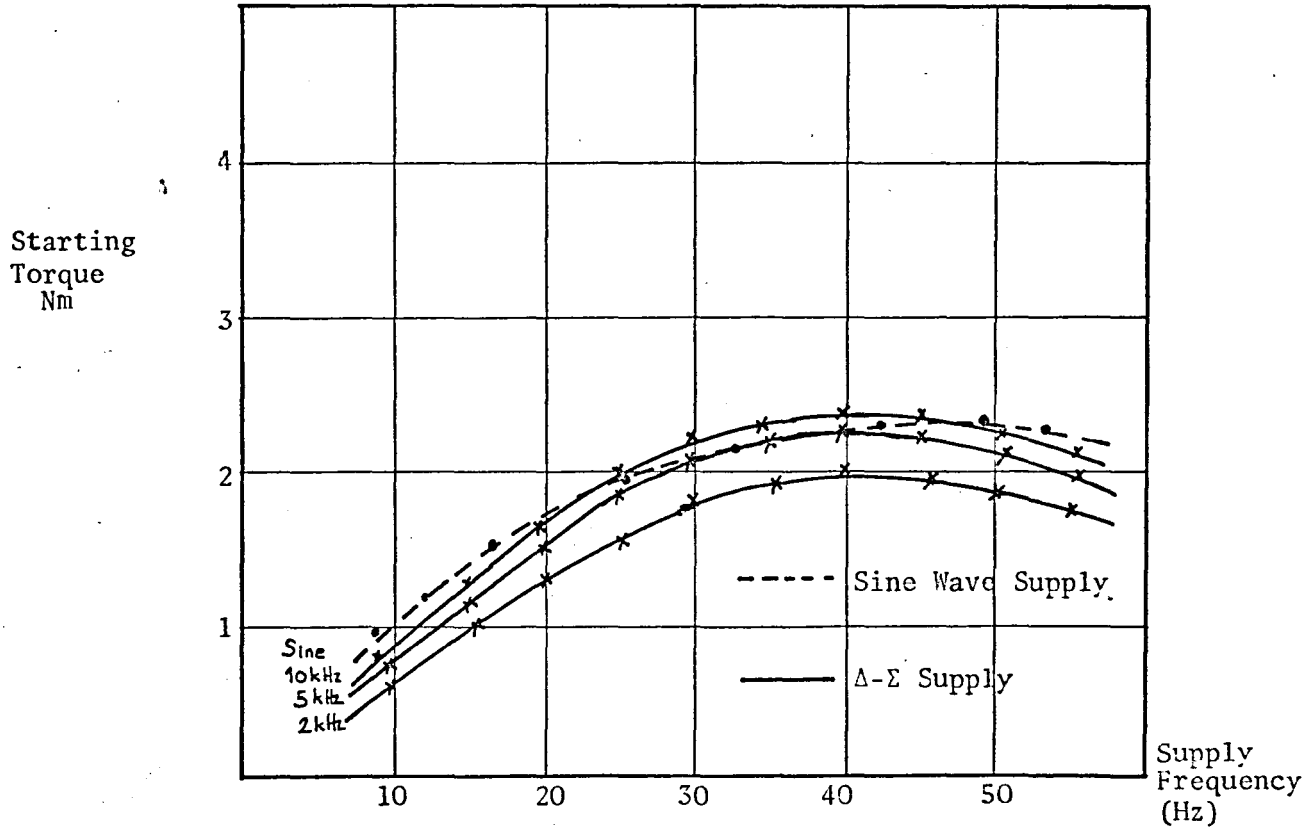
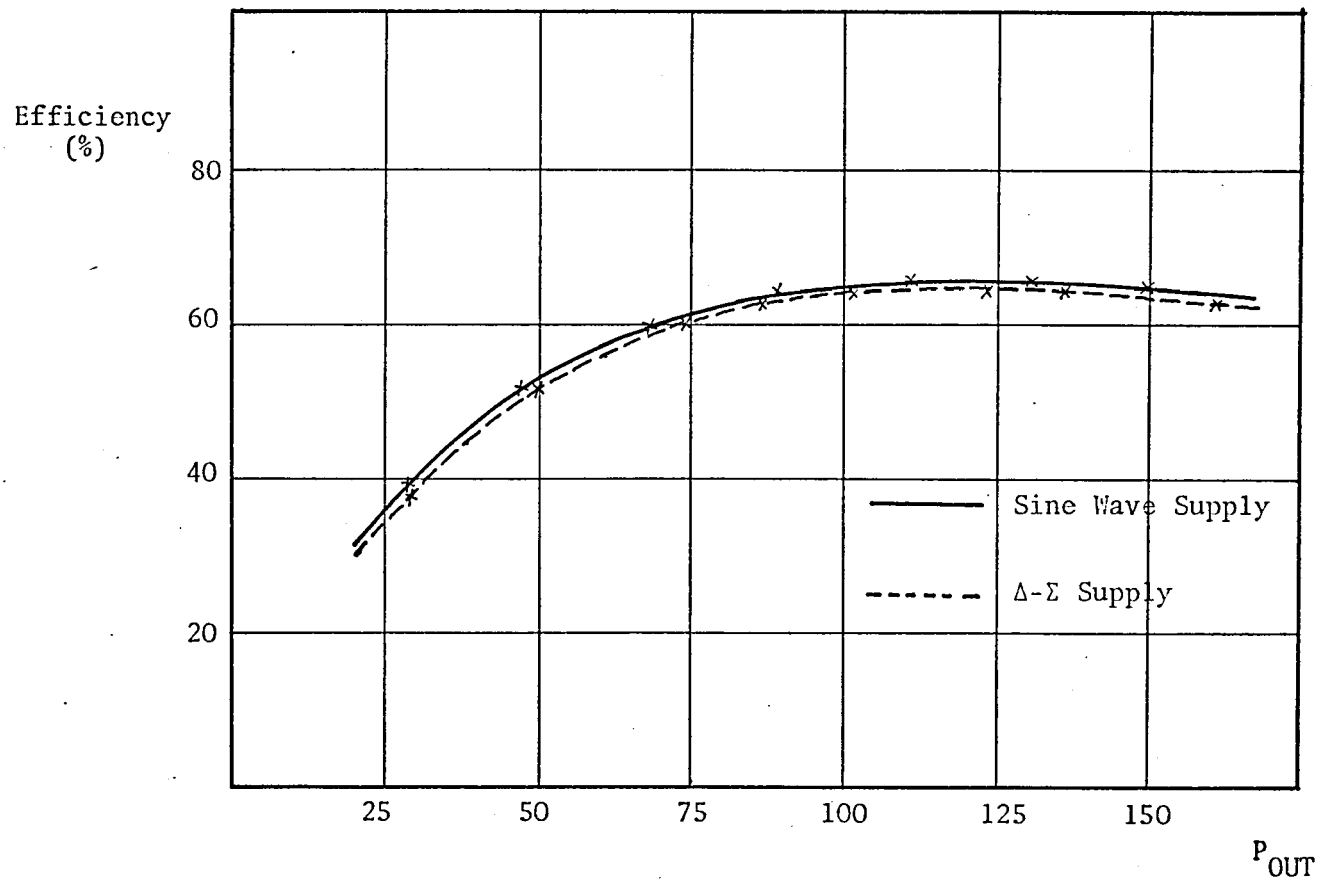


Figure 8.22: VARIATION OF STARTING TORQUE WITH SPEED



50Hz Supply Frequency, 10kHz Clock Frequency

Figure 8.23: INDUCTION MOTOR EFFICIENCY

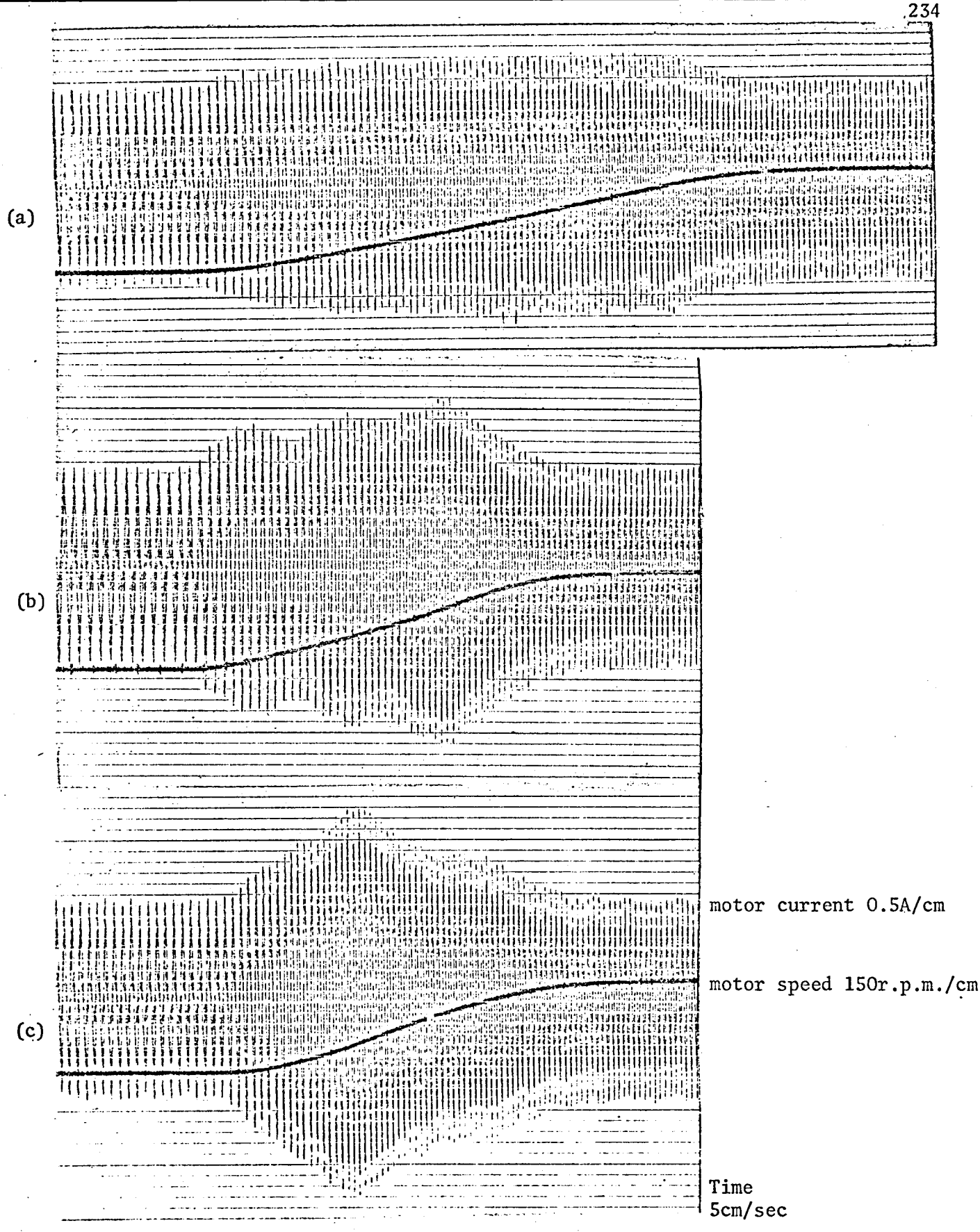
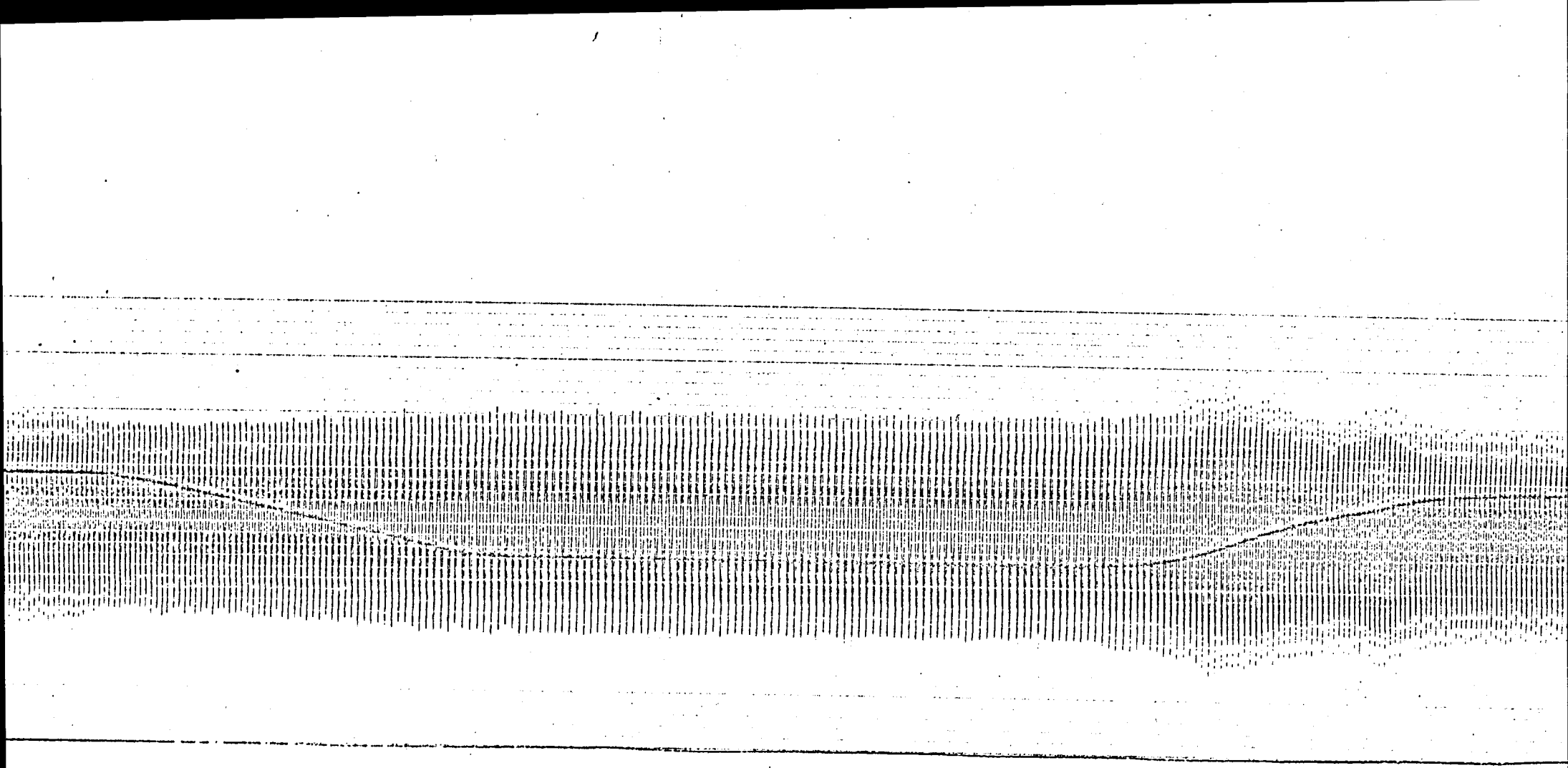


Figure 8.24: MOTOR SPEED AND CURRENT FOR A STEP CHANGE IN SPEED (WITH NO LOAD) WITH THREE DIFFERENT ACCELERATION TIMES

(a) Slow Acceleration Time
(b) Faster Acceleration Time
(c) Fast Acceleration Time



Current, 0.5A/cm

Speed 150r.p.m./cm

Time
5cm/sec

Figure 8.25: MOTOR SPEED AND CURRENT FOR UNEQUAL ACCELERATION AND DECELERATION TIMES (WITH NO LOAD)

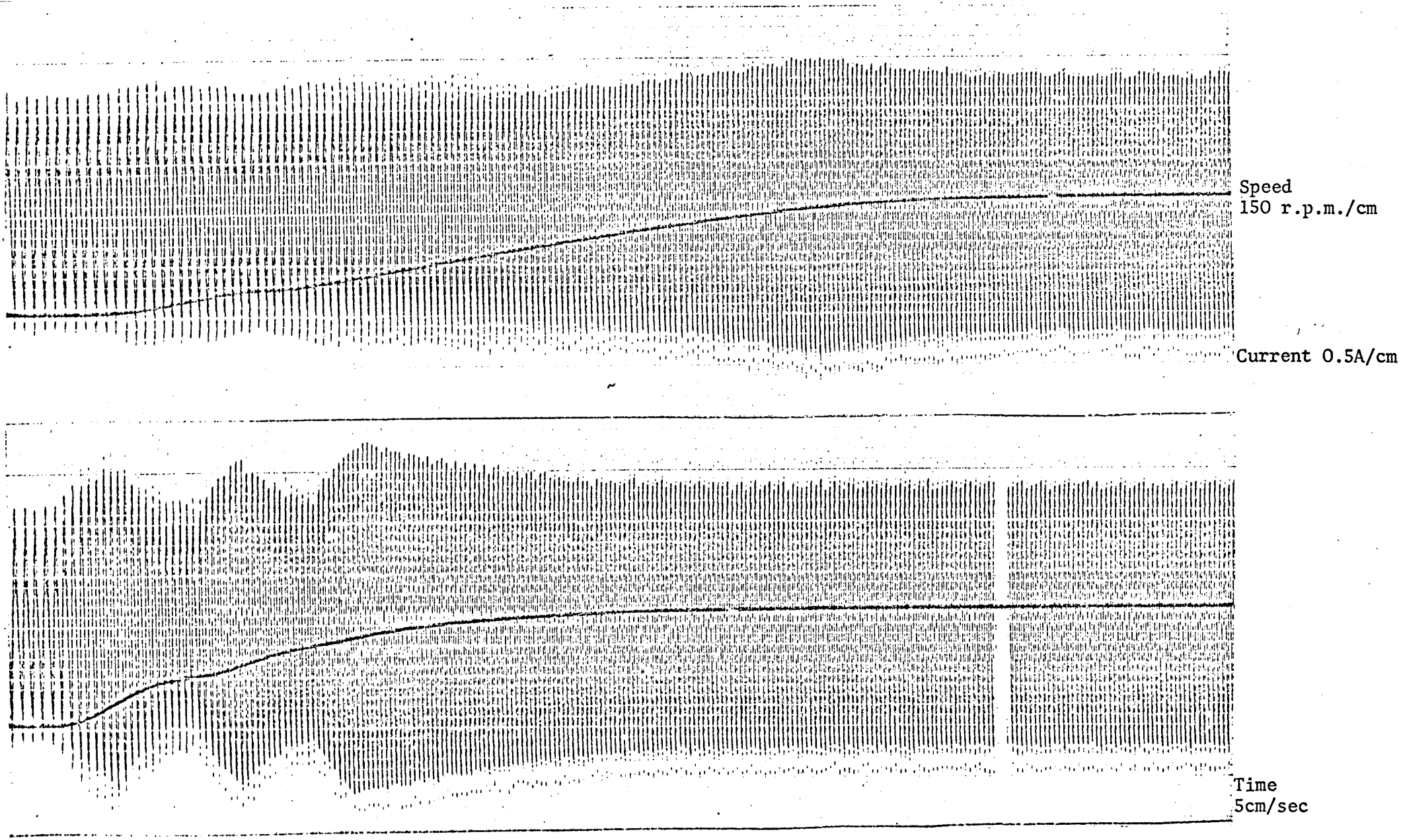
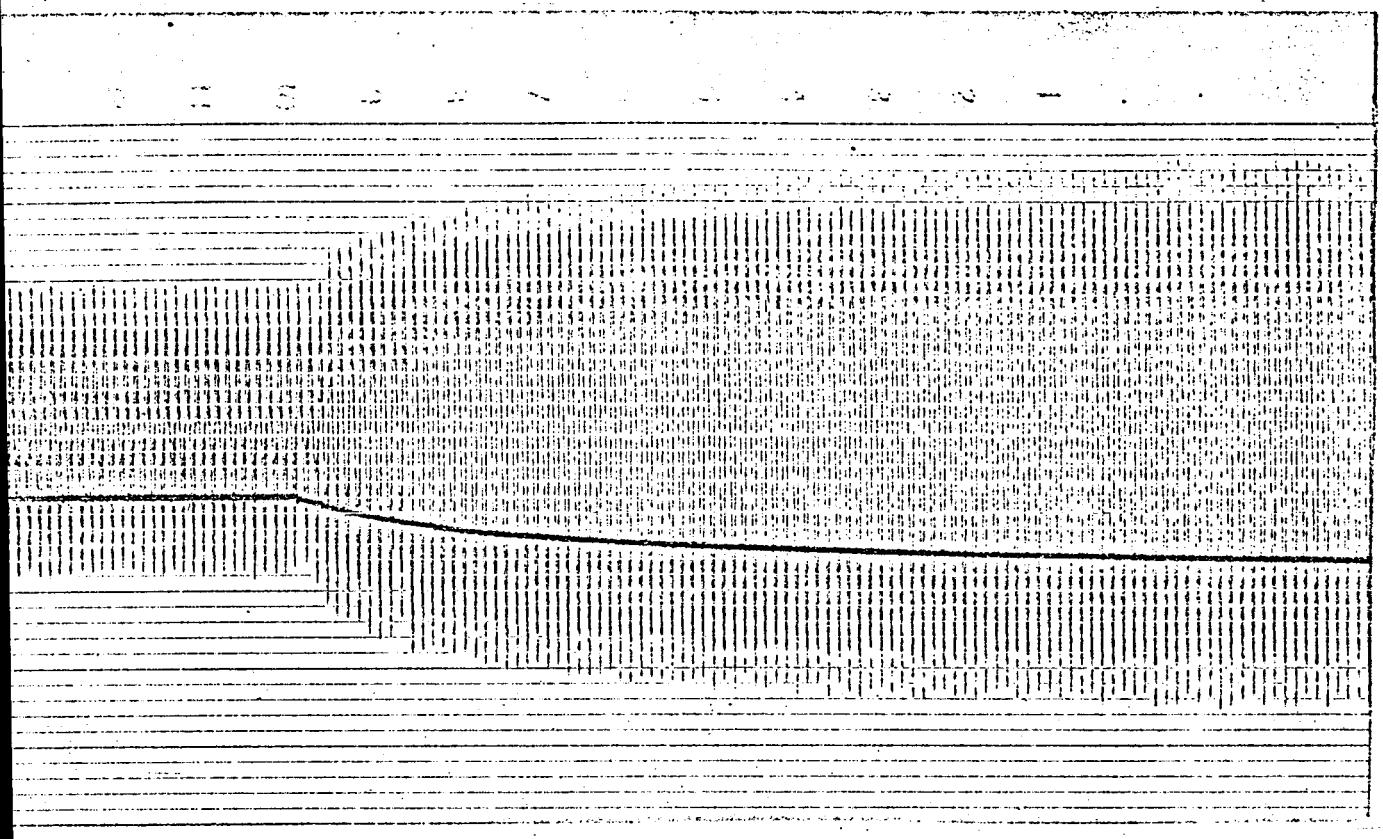
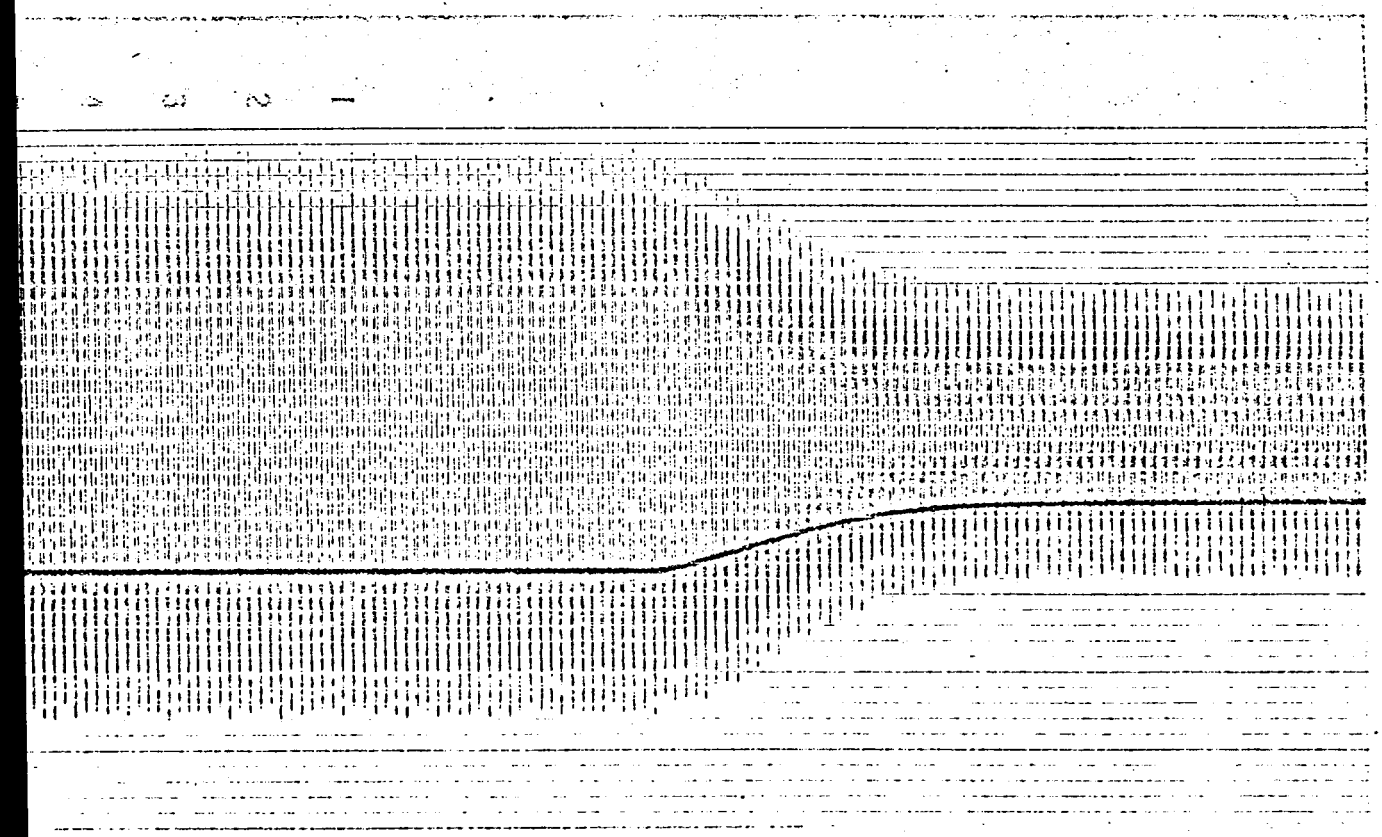


Figure 8.26: MOTOR SPEED AND CURRENT FOR TWO DIFFERENT ACCELERATION TIMES WITH LOAD



(a) Sudden Application of Load, speed 150 r.p.m./cm
current 0.5A/cm

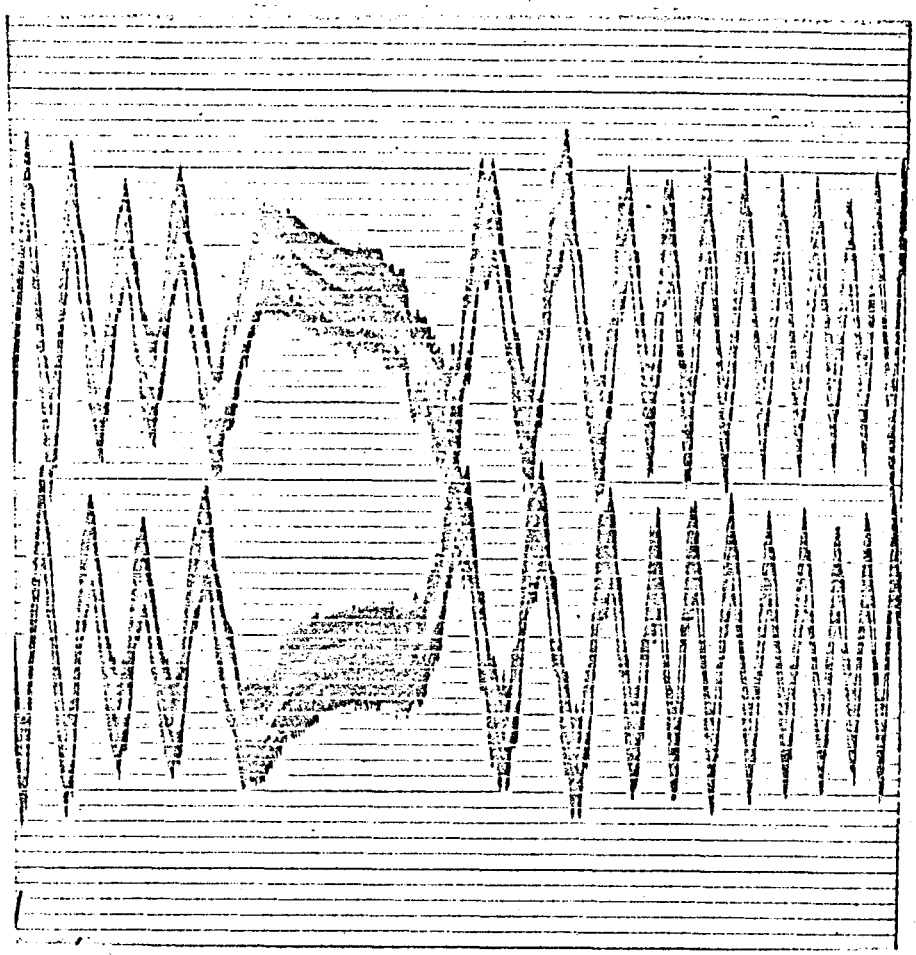
Time
5cm/sec



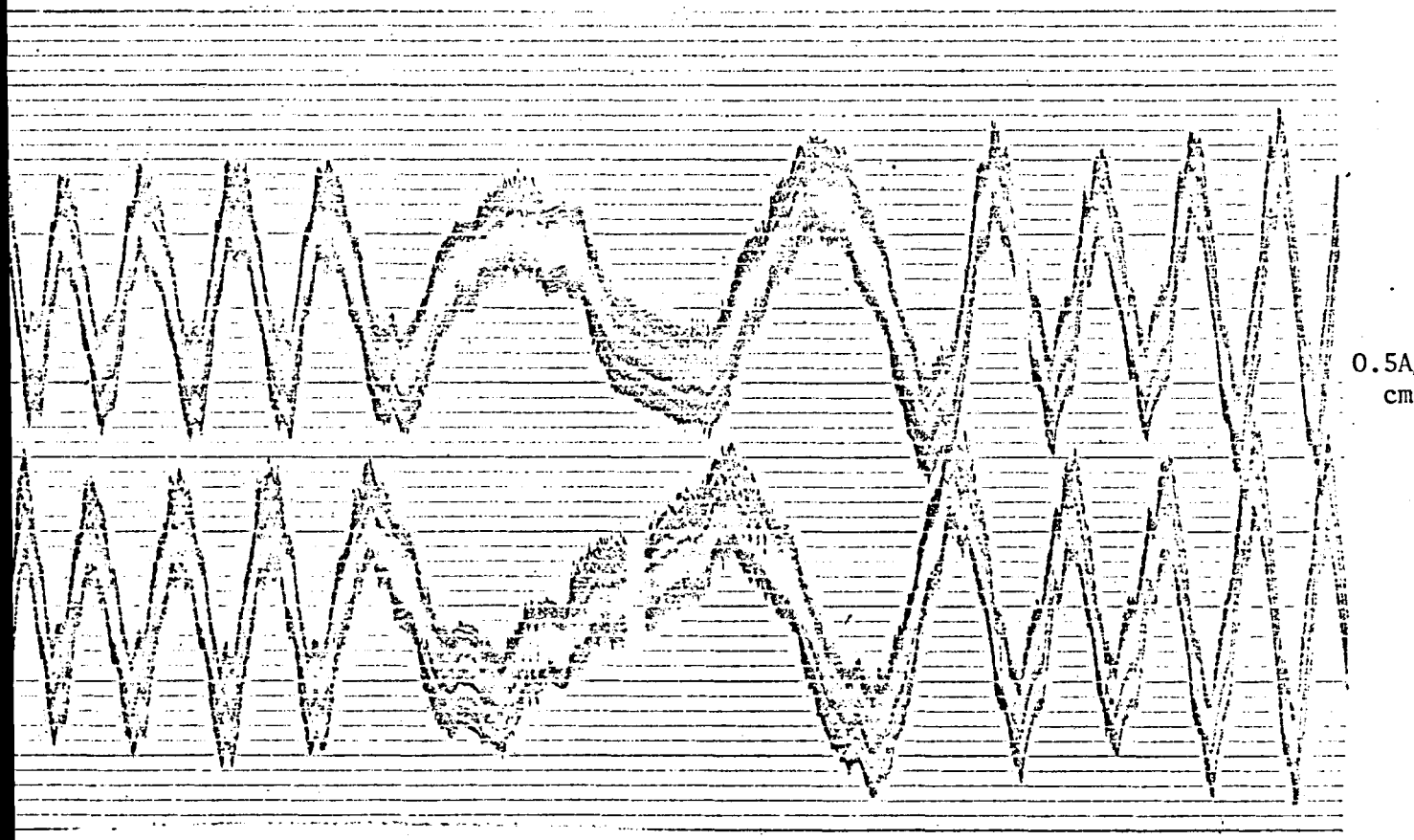
(b) Sudden Removal of Load, speed 150 r.p.m./cm
current 0.5A/cm

Time
5cm/sec

Figure 8.27: MOTOR SPEED AND CURRENT FOR SUDDEN APPLICATION AND REMOVAL OF LOAD



(a) Current Waveforms in Two Different Phases



(b) Expanded Scale

Figure 8.28: CURRENT WAVEFORMS DURING SPEED REVERSAL

CHAPTER 9

OPERATION IN CLOSED LOOP MODE

The open-loop operation of an induction motor at variable frequency provides a satisfactory variable-speed drive when the motor is required to operate at a relatively steady speed for long periods. When the drive requirements include rapid acceleration and deceleration an open-loop system may prove unsatisfactory, since the supply frequency cannot be varied very quickly, or, (as discussed in section 6.2.2) the rotor breakdown frequency is exceeded. Beyond or near the breakdown point (when the pull-out torque is exceeded), the rotor current is large, but the power factor is low and the output torque and efficiency are small. Although this requirement may be partially met by the acceleration and deceleration control unit of Figure 6.10, closed-loop feedback methods are still needed if precise speed control is required.

This chapter is concerned with different closed-loop techniques that are applicable to induction motors. Having discussed qualitatively the performance on such supplies, a simple prototype scheme that can be used with the Δ-Σ modulated inverter system is described, and experimental results which demonstrate the operation of the closed-loop scheme are presented.

9.1 CONTROL TECHNIQUES

As will be recalled from equation 2.12 of section 2.1.4, the torque produced by an induction motor on a variable-frequency supply is

$$T = \frac{E_2^2}{\omega_s^2} \cdot \frac{\omega_1 R_2 s_r}{R_2^2 + X_a^2 s_r^2}$$

where s_r is the rotor slip to a base frequency ω_1 and ω_s is the synchronous frequency. This equation shows that the torque is dependent only on the slip s_r and the excitation E_2/ω_s, and that it can be controlled by adjusting either in isolation or both in combination. The choice of the particular mode of control depends on the load, the motor, and the controller.

The above torque equation is valid for both positive and negative slip

frequencies, corresponding respectively to motor and to generator operation. For motor operation, a predetermined rotor frequency f is obtained by applying a stator frequency $f_s=f_r+f$, where f_r is the rotational frequency of the motor. Negative slip implies generator operation with a supply frequency less than the rotational frequency by an amount f, that is $f_s=f_r-f$. Motor or generator operation with a predetermined rotor frequency can therefore be obtained by closed-loop control of the absolute slip frequency.

The most desirable kind of closed-loop operation is achieved by controlling directly the air-gap flux of the motor. In such a system the air-gap flux is monitored, using either a Hall-effect transducer or a stator search coil, and is adjusted to the desired level by variation of the terminal voltage so that E_2/ω_s has the required value. If the rotor frequency and the air-gap flux are constrained to remain constant, then the rotor current is also constant. Since a constant air-gap flux demands a fixed magnetizing current, the stator current (which is the sum of the referred rotor current and the magnetizing current) is also fixed. Consequently, a closed-loop system with a constant stator current develops a constant shaft torque at all motor speeds. Alternatively, if the stator current is itself adjusted in a feedback loop and the air-gap flux is also controlled, the rotor frequency is automatically determined without being directly controlled. Another possibility is the direct control of the stator current and the rotor frequency, which provides indirect control of the air-gap flux. This mode of control has the advantage of no transient current surges, and a large overcurrent capacity is unnecessary. This makes possible a more economic inverter design, in which the power transistors are fully utilised during normal operation.

The above induction motor drive possibilities in which the rotor frequency is controlled are known as controlled-slip drives. The simplest way to control the slip frequency is to keep it constant. The power factor

of a motor operating at a fixed-slip frequency is approximately constant and is independent of the motor speed, although at low frequencies increased resistive effects cause the power factor to change with speed. If the value of the fixed-slip frequency is chosen for optimum efficiency at the middle of the speed range, a performance with a high efficiency can be maintained through a wide speed range. The efficiency can be improved by programming the slip frequency with speed, although since the gain is small this form of control is usually only recommended for high horsepower systems.

The above discussion shows qualitatively that, in a closed-loop system, operation always occurs at a smaller and controlled slip, thereby yielding a high torque at a high power factor and with low losses. Figures 9.1.a and 9.1.b show two desirable forms of torque-speed characteristics which can be easily obtained by using the above principles.

9.2 DESIGN

Closed-loop techniques are well established[34-37] in the field of a.c. motor control, and a typical system that can be used with a Δ-Σ modulated inverter is shown in Figure 9.2. The system controls the air-gap flux indirectly, by regulating the voltage fed to the machine. The actual motor speed is measured by a tachogenerator, although alternative electronic means[38], in which an analog signal proportional to the slip level is derived from the electrical quantities (i.e. voltages, currents) by performing simple signal-processing operations may also be adopted. Such an arrangement would offer the advantages of simplicity and ruggedness, since a tachogenerator has brushes or slip rings which limit its use in dangerous environments. Although electronic means are normally preferable they require complex circuitry, and a simple tachometer for the purpose of the present investigation is satisfactory.

Assuming the actual speed of the motor is less than the demanded speed

the stator frequency is f_r+f, then on starting a large torque is developed to accelerate the rotor to the desired speed. When the actual speed exceeds the demanded speed the stator frequency is f_r-f, and the machine operates as an induction generator and returns energy to the supply. A slip limiter is also necessary in the control circuitry, so that the demanded rotor frequency can never exceed the breakdown value in either the motoring or the generating regions. This permits stable operation close to the breakdown point, and by providing a large reserve of machine torque improves the dynamic performance of the system for sudden changes in the demanded speed.

Since a change in the polarity of the slip signal causes a reversal of the machine torque, it also reverses the direction of the power flow. The direction of rotation is determined by the phase sequence of the stator supply, and a reversal of the phase sequence is obtained statically by means of the control circuitry (see section 6.2.3). By means of independent control of the direction of rotation and the slip polarity, four-quadrant operation is thus possible, giving motor or generator operation in either direction of rotation.

It was explained in section 8.4 that it is not sufficient to control the amplitude of the stator voltage in proportion to the stator frequency, because the torque available from the induction motor decreases severely when the machine is loaded at low speeds. Figure 9.3 shows a scheme in which a correcting element[36] is incorporated, such that the stator voltage can be varied with load to ensure a requirement of high torque at low speeds can be met. A current-limiting control loop is also included in this scheme, by deriving a current feedback signal from the voltage across the 0.1Ω resistor of Figure 7.33, after isolation and filtering. If the reference current value is exceeded the limiter acts to reduce the input voltage to the multiplier unit of Figure 6.2, and by reducing the amplitudes of the 3-phase sine waves

(which feed the three Δ-Σ modulators) prevents the currents of the motor from becoming excessive.

Figure 9.4 shows the complete circuit diagram for the controller of Figure 9.2. Since the control loop is required to provide both a zero steady-state error and a fast response, a proportional plus integral (PI) controller is used. The limiter which follows the amplifier operates on the same principles described in Figure 6.9. The output of the controller of Figure 9.4 goes to the voltage controlled oscillator and the absolute value unit of Figure 6.6.

9.3 PERFORMANCE OF THE INDUCTION MOTOR ON CLOSED-LOOP

Figure 9.5 shows the torque-speed characteristics obtained with closed-loop operation of the Δ-Σ modulated system. It will be seen that the speed is now constant and independent of load, and that the system behaves as expected. Since the correcting element mentioned in section 9.2 is not incorporated, the pull-out torque decreases as the supply frequency is reduced.

Although the dynamic performance of the open loop system discussed in section 8.5 is stable, the closed loop system may oscillate, unless careful attention is paid to the system of the PI controller. Adjustment of the time constant and the gain factor in the controller enable different performance requirements to be met, such as maximum allowable overshoot and a specified accuracy. Figures 9.6 and 9.7 show motor speed and current waveforms for a large step change in the reference voltage, with the motor on no load and on load respectively, and show that the motor speed reaches the reference value quickly and that the transient performance is satisfactory. The overshoot of current evident in Figure 9.6 may be controlled by the current limiter discussed in the previous section.

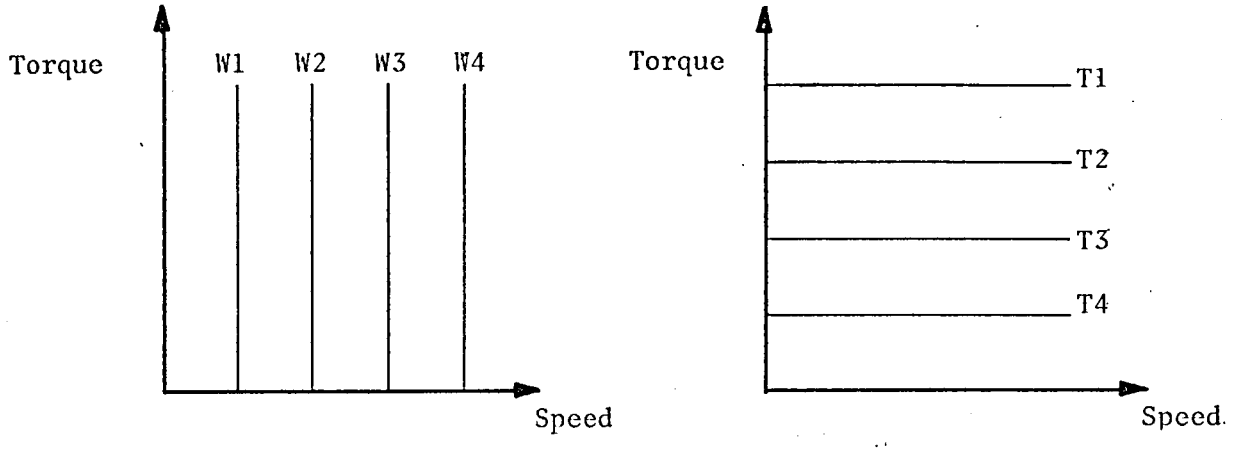
Figures 9.8.a and 9.8.b show the motor speed and current waveforms

following respectively the sudden application and removal of load. When load is applied, the motor current and the input frequency are increased by the controller, so that the motor speed is held constant. When the load is removed the motor speed tries to increase, but the motor current and the input frequency are reduced so that the speed is gain held constant.

9.4 ADVANTAGES OF OPERATION IN CLOSED-LOOP MODE

The results presented in section 9.3 demonstrate that, by operating the induction motor in a closed-loop mode, the slip frequency becomes independent of the loading, and efficient operation is achieved at light loads as well as at the rated load. With a controlled slip frequency the motor cannot pull out of step, and a maximum torque equal to the pull-out torque can safely be obtained.

Another advantage of a variable-speed, closed-loop drive is its adaptability to various control functions, and the overall system characteristics can be adjusted to suit the particular application. Stability of operation is ensured by incorporating a slip limiter.



(a) Constant Speed (b) Constant Torque

Figure 9.1: TORQUE-SPEED CHARACTERISTICS

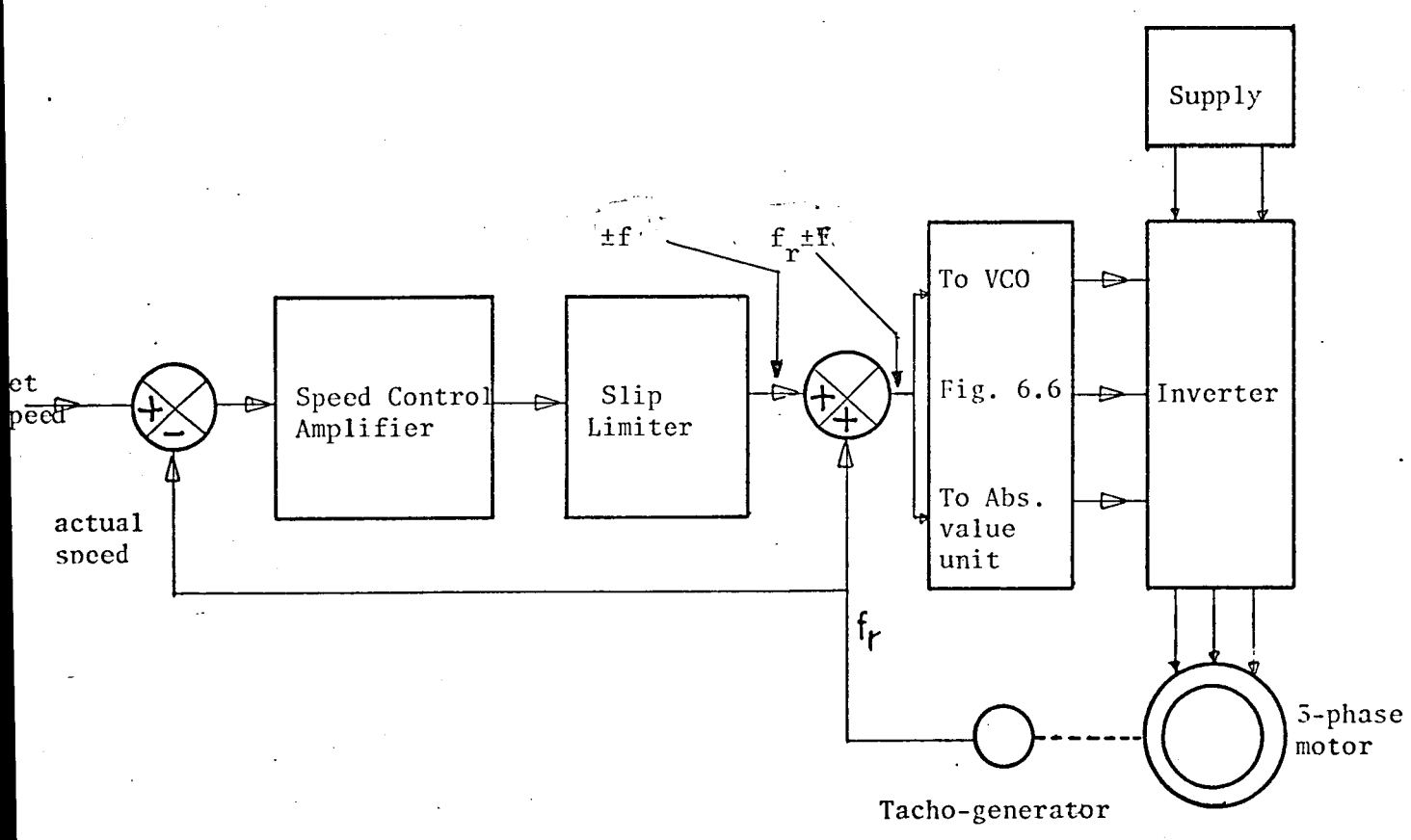


Figure 9.2: BLOCK DIAGRAM OF THE CONTROLLED SLIP Δ-Σ MODULATED INDUCTION MOTOR DRIVE

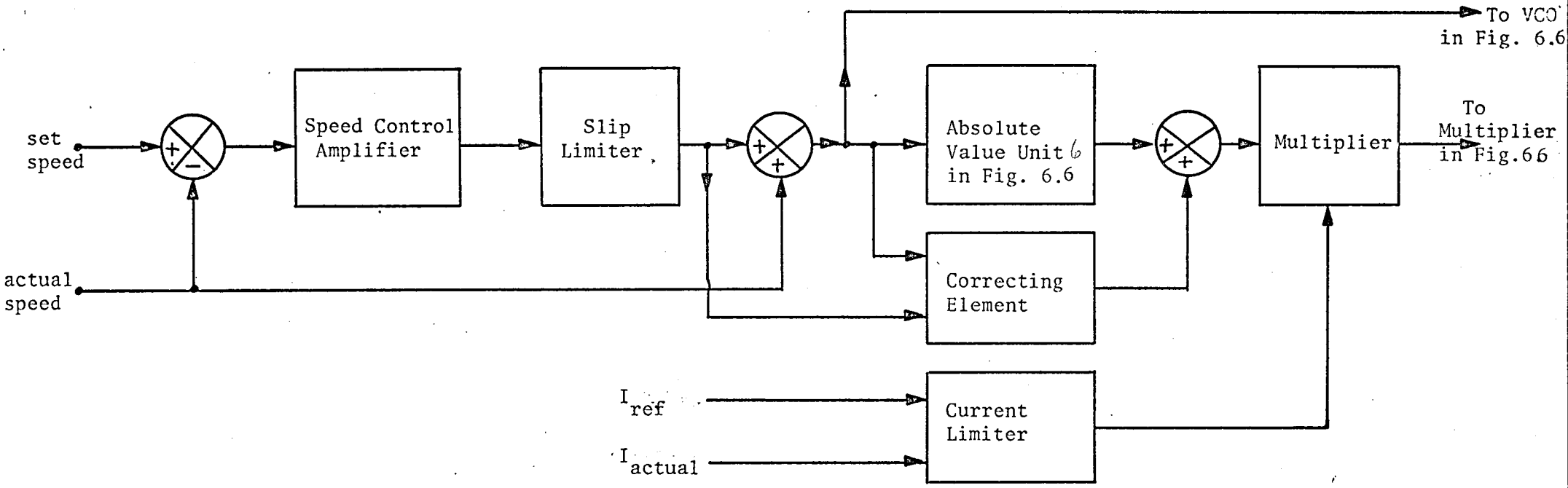


Figure 9.3: BLOCK DIAGRAM OF THE IMPROVED CONTROLLED-SLIP DRIVE

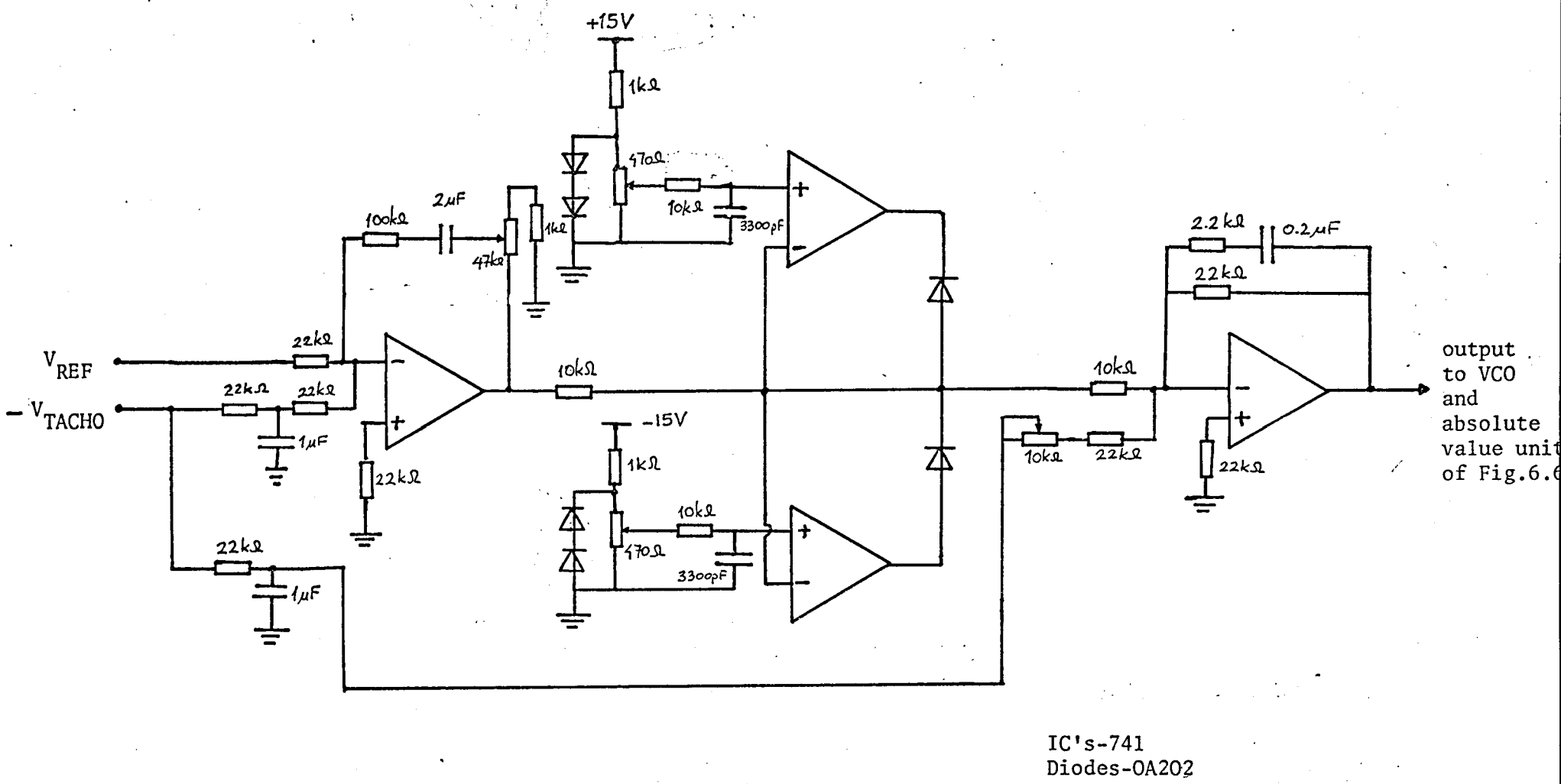


Figure 9.4: CIRCUIT DIAGRAM OF THE CONTROLLER

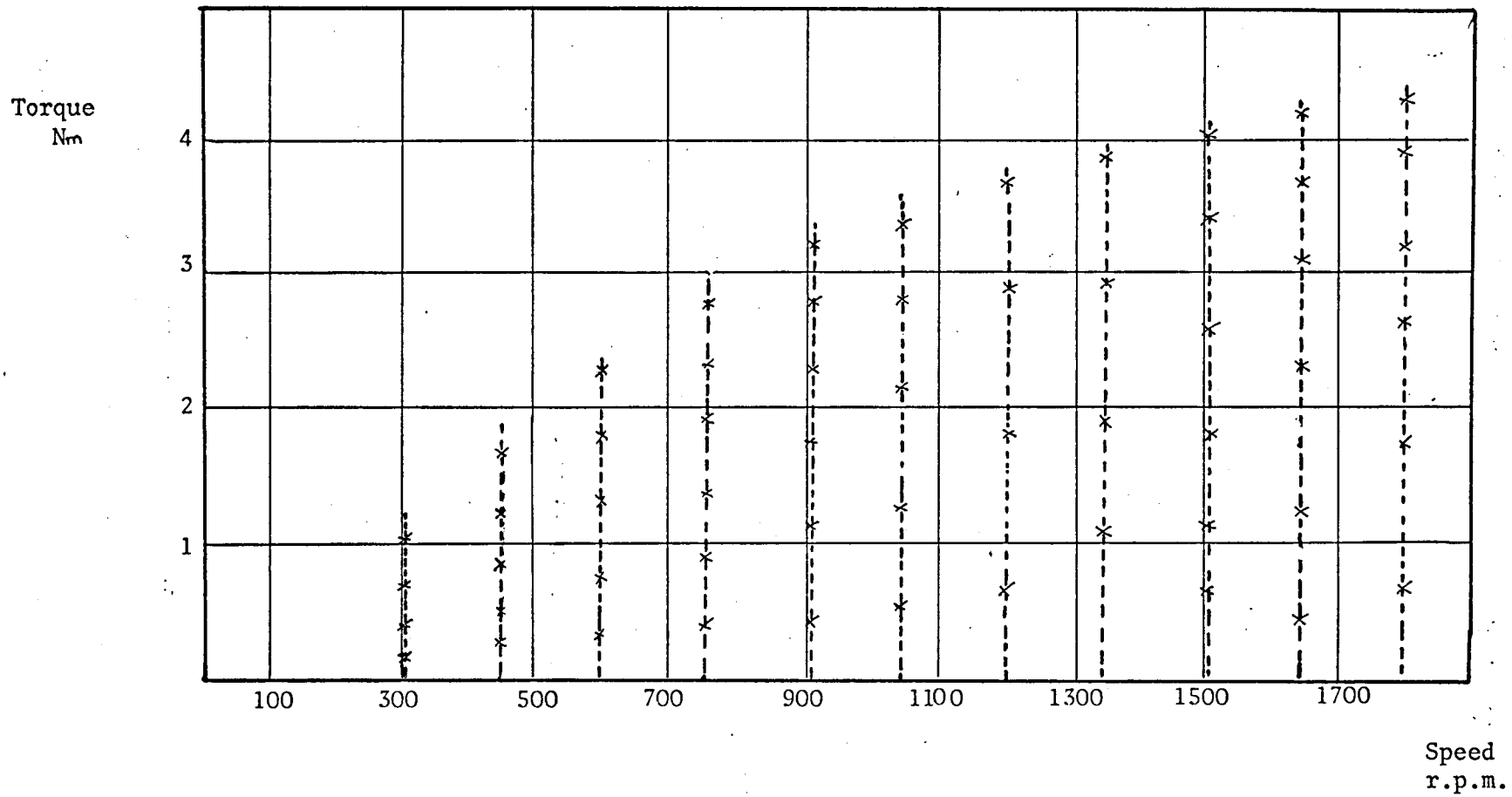


Figure 9.5: TORQUE-SPEED CHARACTERISTICS WITH CLOSED LOOP OPERATION

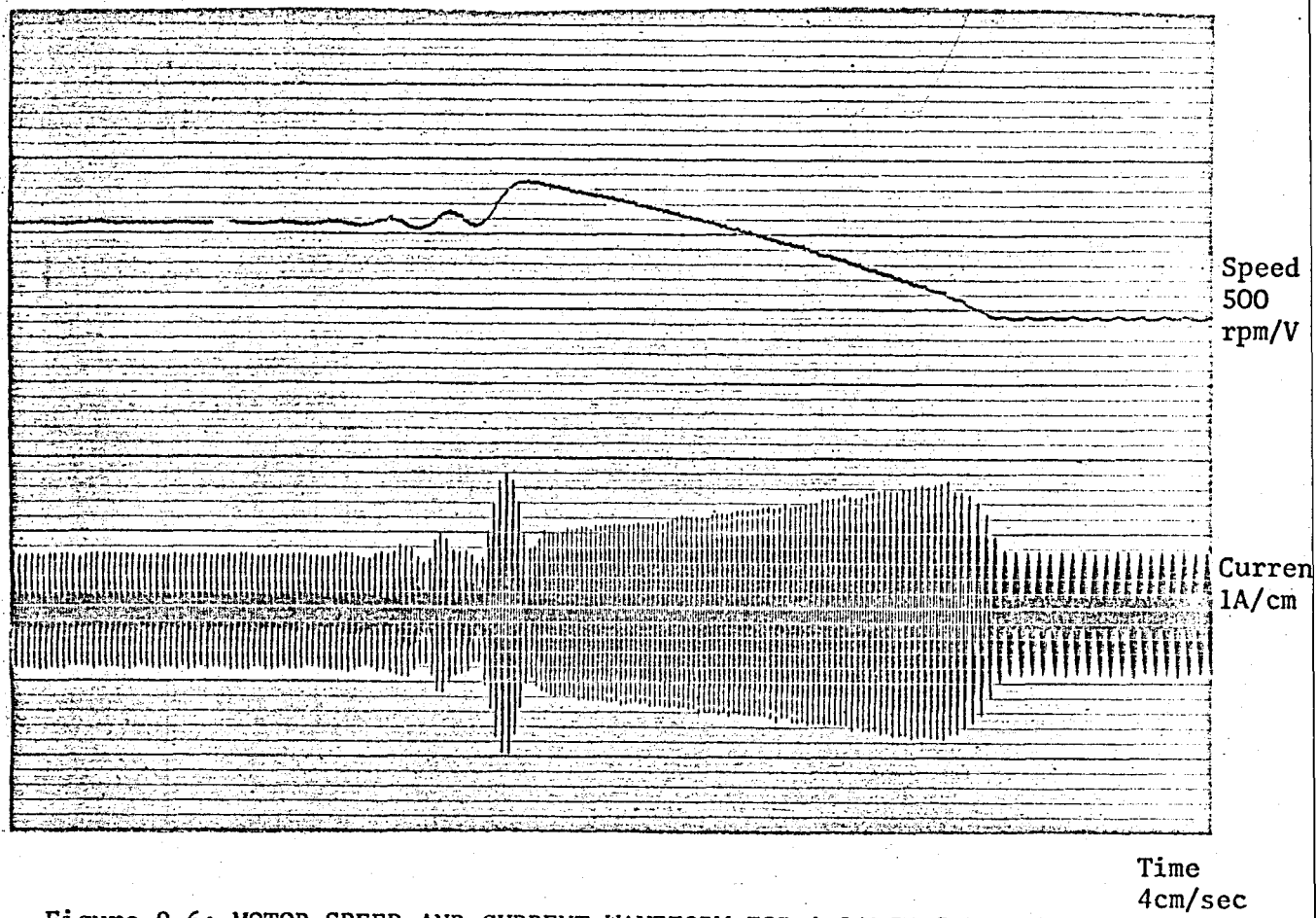


Figure 9.6: MOTOR SPEED AND CURRENT WAVEFORM FOR A LARGE STEP CHANGE IN REFERENCE VOLTAGE, NO LOAD

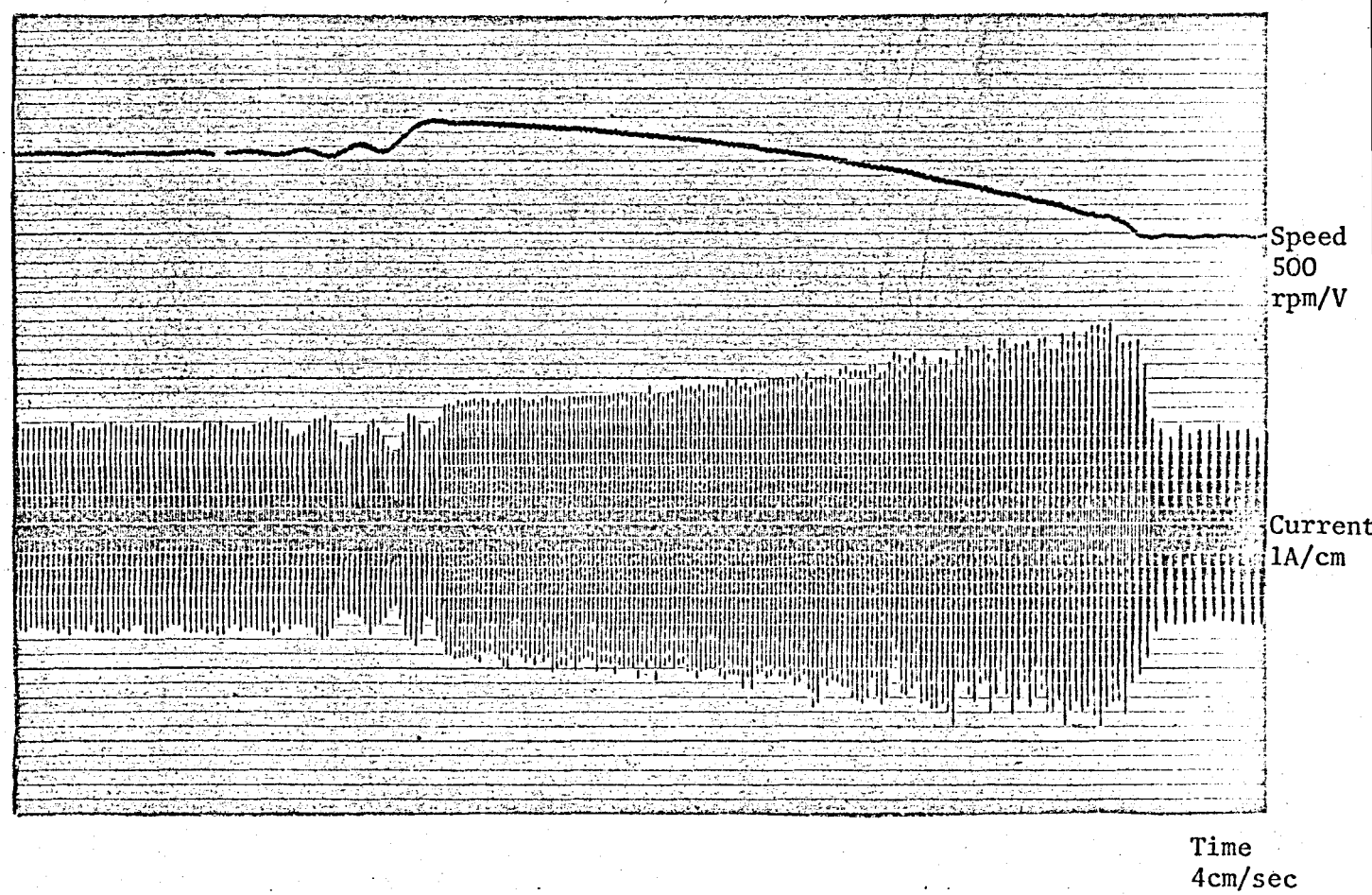
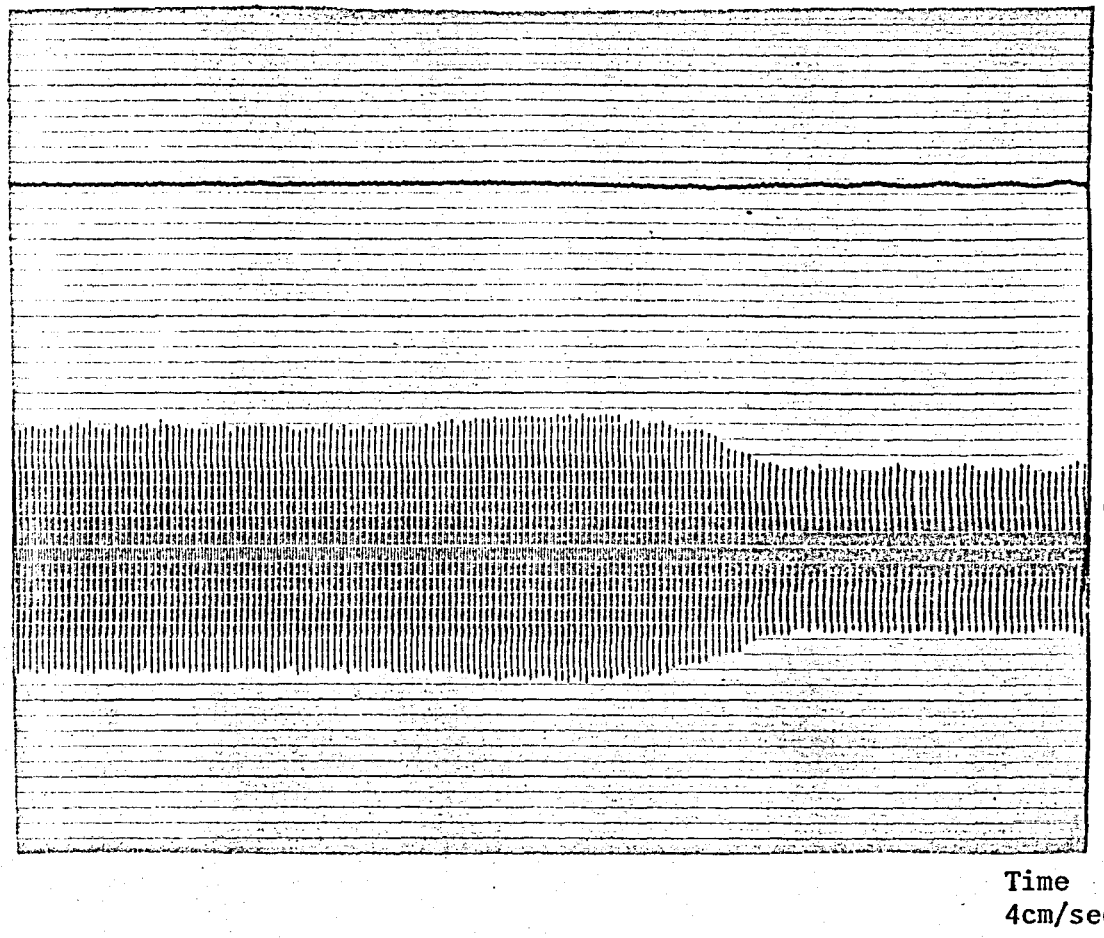
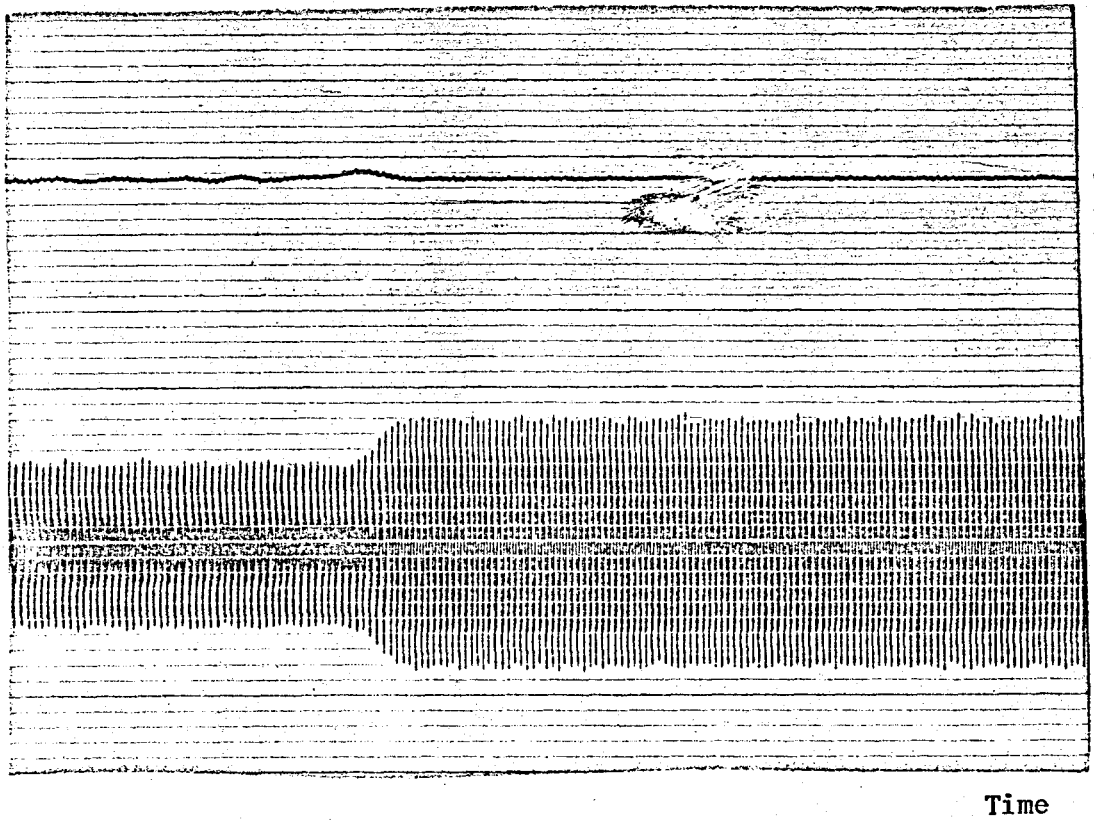


Figure 9.7: MOTOR SPEED AND CURRENT WAVEFORM FOR A LARGE STEP CHANGE IN REFERENCE VOLTAGE, WITH LOAD



(a) Sudden Application of Load



(b) Sudden Removal of Load

Figure 9.8; MOTOR SPEED AND CURRENT FOR SUDDEN APPLICATION AND REMOVAL OF LOAD

CHAPTER 10

CONCLUSIONS

The conclusions arising from the project described in this thesis, together with suggestions for the future extension of the work, may be summarised as:

1. The experimental investigation and the results presented in Chapters 8 and 9 show clearly that the Δ-Σ modulated speed control system developed in the research work offers an attractive possibility for use with small induction motors.

2. Since control of both voltage and frequency are achieved in the same power circuit, the number of switching components is reduced, and the design of the inverter is much simplified, compared with the alternative methods discussed in section 2.2.

3. The use of transistors in the inverter eliminates the need for forced commutation, and solves the problems of trapped energy inherent in thyristor based systems. The power handling capability of the present inverter could be increased by the use of better transistors. With a ESM16A type transistor the total power that can be delivered is limited to about 2.2kW, but the use of XGSR 10040 type transistors would enable this to be increased above 5kW. Very high switching frequencies, of the order of 400kHz, are easily obtained with this device.

4. Although a transistor inverter has low losses and a high efficiency, it suffers from the disadvantage of requiring relatively large base currents for large output currents, which also limits the output power. The base drive may be optimised by careful design considerations, and requires special attention to increase the overall system efficiency. Alternatively, it is also worth mentioning that power FET's

rather than transistors can also be used if very high switching frequencies are needed, and this would avoid the need to provide a large base drive. The disadvantage of the relatively large on state resistances of FET's, along with their low power ratings, are expected to be greatly improved in the near future (at present the rating of one of the best power FET's available in the market is; device type: VN 846A, on resistance = 0.4Ω at 10A current, 80V, 80W dissipation, 20 ns switching time with no storage time).

5. Since the modulated frequency of the inverter output can be very high the upper limit of the motor speed range is also very high, and it depends mainly on the motor characteristics. The Δ-Σ modulated system also provides a satisfactory control down to very low speeds.

6. Since the induction motor performance with the Δ-Σ modulated supply is compared only with that of a sine wave supply, the work presented in the thesis can be extended further by comparing it experimentally with the other methods of speed control discussed in Chapter 2. It can safely be said that only the sinusoidal pulse-width modulation described there will provide results comparable with a Δ-Σ modulated system, and all other methods will prove to be inferior. Furthermore, since sinusoidal pulse-width modulation requires the comparison of a sawtooth waveform with a reference sine wave, Δ-Σ modulation is inherently simpler. The overall system is designed such that, as can be seen from Figure 10.1, only a single veroboard containing modulators needs to be changed for comparison purposes, which makes this a quite simple and straightforward work.

7. Induction motor stability investigations with the Δ-Σ modulated supply is an area of further research with may prove fruitful, especially when the system is in the closed-loop mode of operation.

8. The application of Δ-Σ modulated systems in various other fields needs to be investigated. The induction motor speed control system developed in this research work is certainly not the only area in which the techniques are applicable. For example, applications involving class D audio power amplifiers seem to be an area in which Δ-Σ modulation may prove a very satisfactory technique, especially using FET's rather than transistors.

9. As can be seen from Figure 3.10, the output of the Δ-Σ modulator is first integrated and then compared with an integrated version of the input. One possibility which arises from this is the use of the current wave form in the motor winding instead of the integrated output of the Δ-Σ modulator for comparison purposes. This needs further investigation, since it promises a system in which the motor current can directly be controlled with a reference sine wave.

10. The application of Δ-Σ modulation to induction motor speed control offers the advantage (over most of the existing techniqes) of reducing harmonics in the voltage, current and torque to a tolerable minimum, as well as permitting these to be varied. The torque-speed characteristics may also be adapted to different operational requirements. Speed reversal is feasible and the acceleration and deceleration times of the motor may also be controlled over a wide range.
Finally, it can be said that with the availability of better and cheaper power transistors, Δ-Σ modulated speed control

systems will present themselves as commercially viable techniques amongst the other and better known speed control techniques.

Figures 10.1, 10.2 and 10.3 show the designed and constructed electronic circuitry, the rectifier, filter, driver, inverter and the induction motor used in the experimental tests.

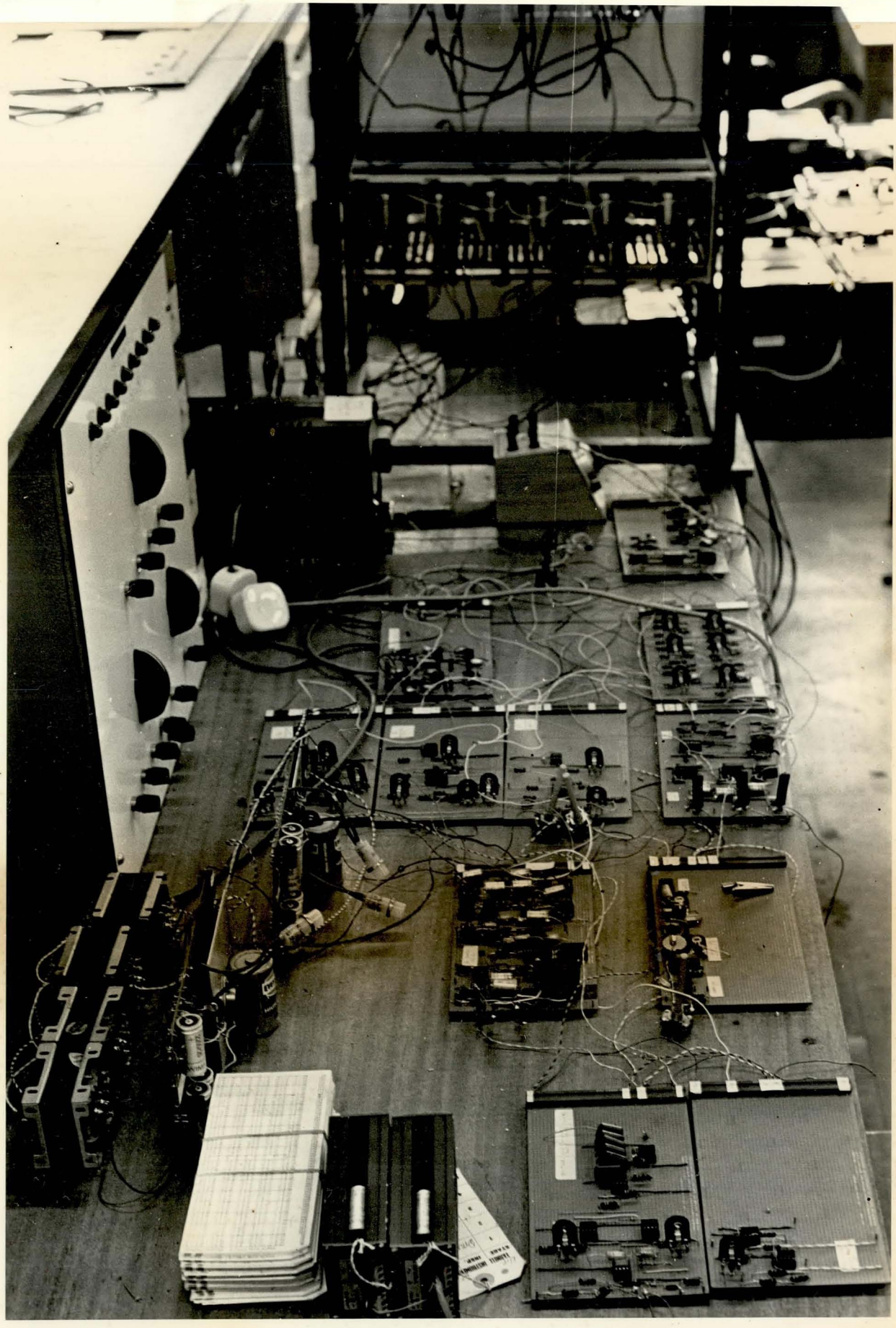


Figure 10.1: THE ELECTRONIC CIRCUITRY

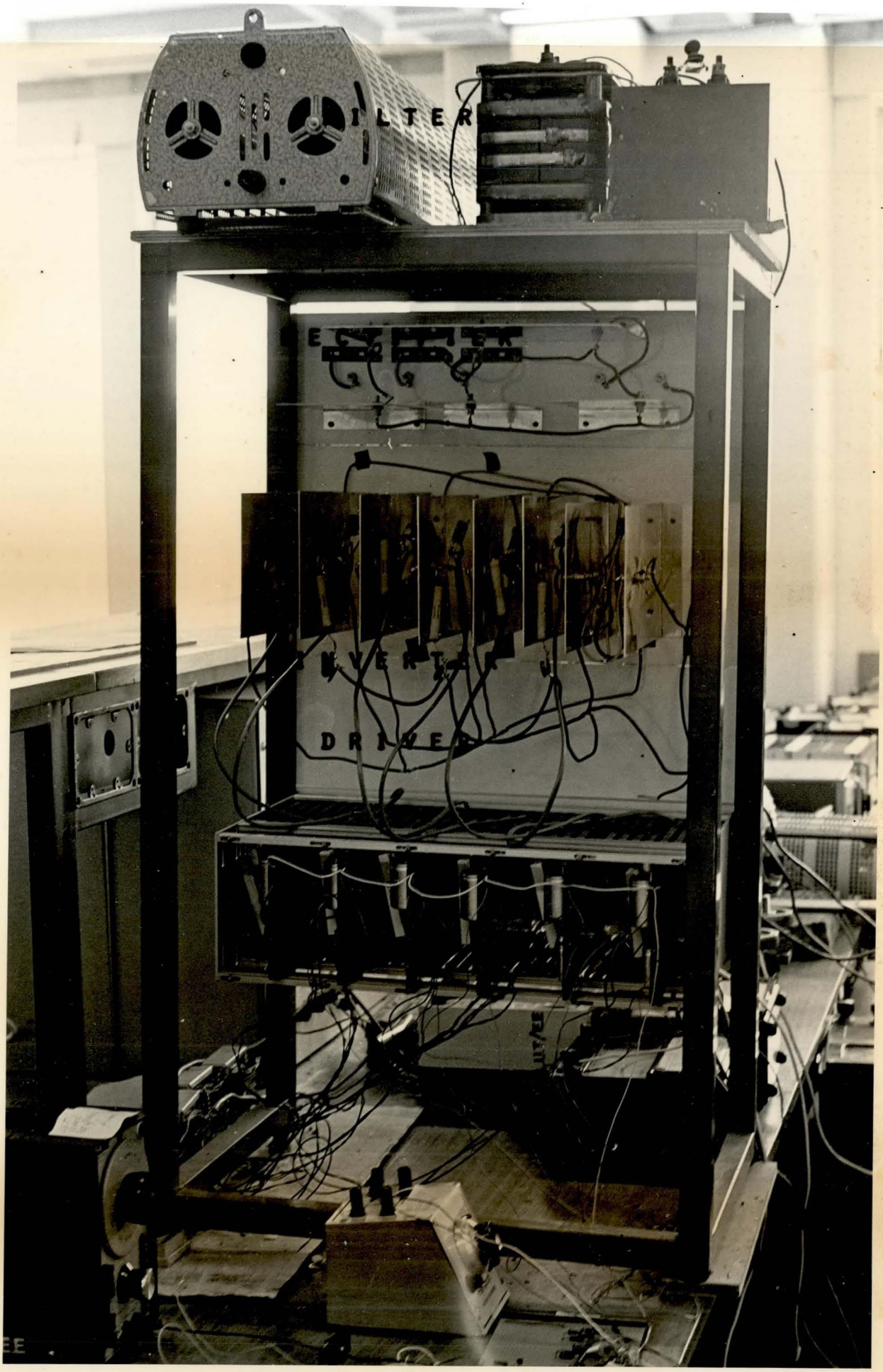


Figure 10.2: THE RECTIFIER, FILTER, INVERTER AND THE DRIVER

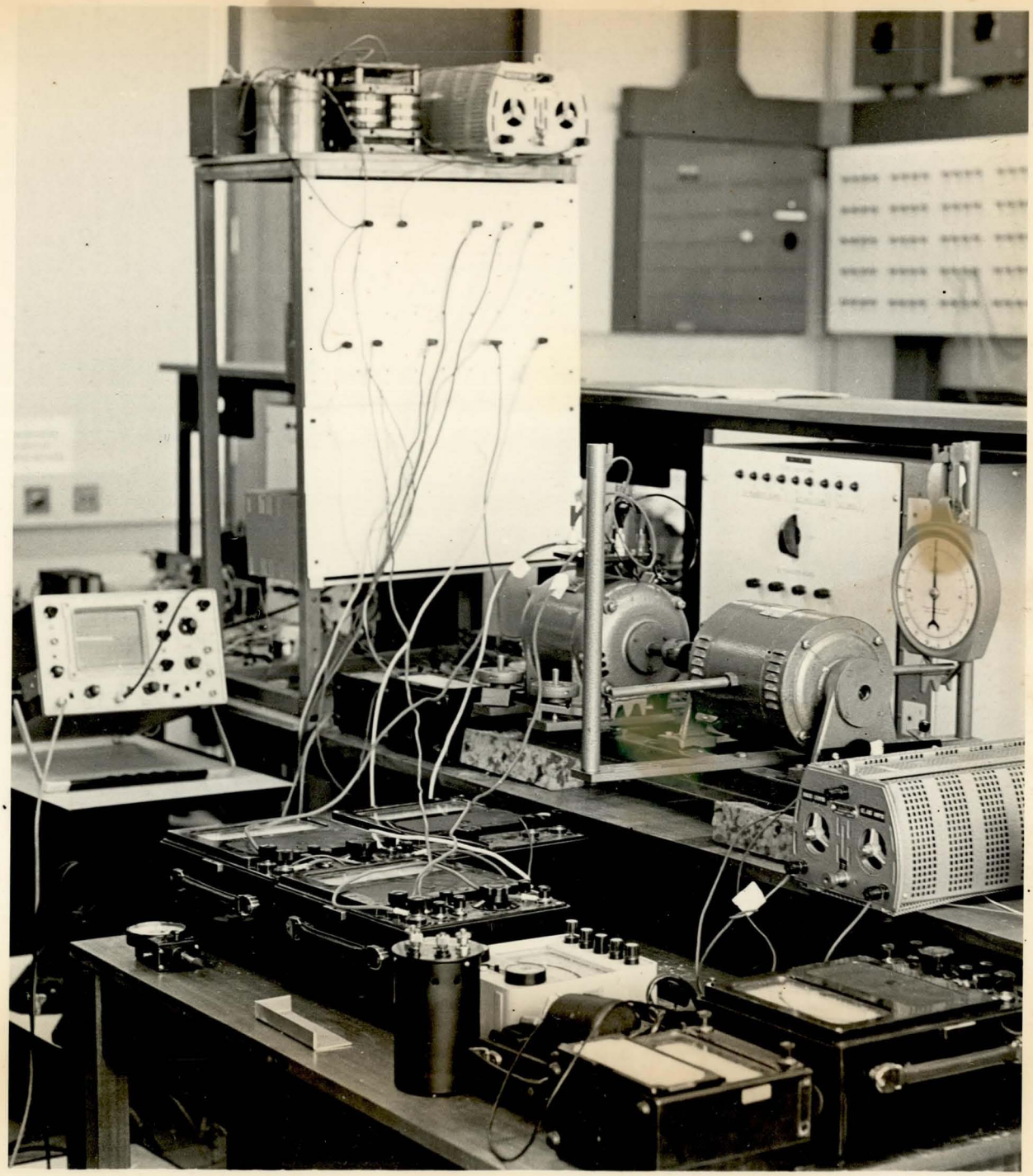


Figure 10.3: THE 3-PHASE INDUCTION MOTOR AND THE D.C. GENERATOR

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APPENDIX 1

CALCULATION OF QUANTIZATION NOISE

1.1 DELTA MODULATION

When the input to a delta modulator is zero, the pattern of the digital output is 10101010. The integrator output is therefore a triangular wave with peaks of $\pm\Delta v/2$, and the mean square difference between this and the input is $(\Delta v)^2/12$. This term represents the total error energy which is contained in a line spectrum of the multiples of f_c. When a sine wave input is applied to the modulator the error is greater, and it has been established by several authors[17-19] that the mean-square error for various sine wave inputs is $(\Delta v)^2/6$.

Because of its random nature and its periodicity in f_c, the spectral distribution of the total error has the form $(\sin x)^2/(x)^2$, and it can be said therefore that the energy contained in the positive frequency spectrum is equal to that which would result if the spectral density at the origin was held constant over a bandwidth from 0 to $f_c/3$. It follows therefore that unfiltered Q-noise energy may be considered as flat throughout the range of the final output filter, so that if the receiver bandwidth is from 0 to B the mean quantisation noise power N_q is,

$$N_q = \frac{(\Delta v)^2}{6}\frac{3B}{f_c}$$

Since

$$\Delta v = \frac{2\pi V f_0}{f_c}$$

$$N_q = \frac{2\pi^2 V^2 f_0^2 B}{f_c^3} \qquad \text{(A1.1)}$$

The mean square value of the overloading sine wave is:

$$E_{max}^2 = \frac{V^2}{2(1+\omega^2T^2)}$$

and

$$\frac{s}{N_q} = \frac{f_c^3}{4\pi^2(1+\omega^2T^2)f_0^2B}$$

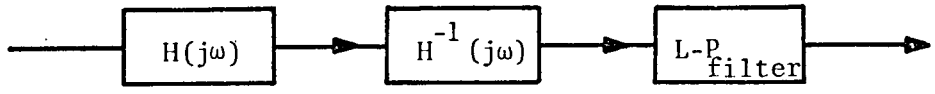
assuming $\omega^2T^2 >> 1$

$$\frac{s}{N_q} = \frac{f_c^3}{4\pi^2.4\pi^2f^2\frac{1}{4\pi^2f_0^2}.f_0^2B} = \frac{f_c^3}{4\pi^2f^2B}$$

$$\frac{s}{N_q} = 0.025\,\frac{f_c^3}{f^2B} \qquad \text{(A1.2)}$$

1.2 DELTA SIGMA MODULATION WITH SINGLE INTEGRATION

Since in a delta sigma modulator, an integrator of transfer function $H(j\omega)$ is placed at the input to the encoder, a complementary inverse process $H^{-1}(j\omega)$ is included in the decoder. Both $H(j\omega)$ and $H^{-1}(j\omega)$ in the decoder may be combined to give a decoder consisting of only a low pass filter.



It was shown in section 1.1 that the error power density at the input to the receiver of the low pass filter is approximately,

$$\frac{(\Delta v)^2}{6} \cdot \frac{3}{f_c}$$

The error power density at the output of the network $H^{-1}(j\omega)$ is therefore,

$$\frac{(\Delta v)^2}{6} \cdot \frac{3}{f_c} \cdot [H^{-1}(j\omega)]^2 = \frac{(\Delta v)^2}{6} \cdot \frac{3}{f_c} \cdot \frac{f^2+f_0^2}{f_0^2}$$

assuming the low-pass filter bandwidth is from 0 to B, the quantization noise power at the output of the low pass filter is,

$$N_q = \int_0^B \frac{(\Delta v)^2}{6} \cdot \frac{3}{f_c} \cdot \frac{f^2+f_0^2}{f_0^2}\, df$$

$$= \frac{(\Delta v)^2}{2f_c f_0^2} \cdot \left(\frac{B^3}{3} + Bf_0^2\right)$$

sunstituting for Δv,

$$N_q = \frac{2\pi^2 V^2}{f_c^3} \left(\frac{B^3}{3} + Bf_0^2\right)$$

and if $B \gg f_0$

$$N_q = \frac{2\pi^2 V^2}{3} \cdot \frac{(B)^3}{(f_c)^3} \qquad \text{(A1.3)}$$

The signal power at the output of the low pass filter is approximately equal to the signal power at the comparator input, or

$$V^2(t) = \frac{E^2}{2(1+\omega^2 T^2)}$$

The signal power of the output of the delta sigma decoder is

$$\frac{E^2}{2(1+\omega^2T^2)} \cdot [H^{-1}(j\omega)]^2$$

$$= \frac{E^2}{2(1+\omega^2T^2)} \cdot (1+\omega^2T^2) = \frac{E^2}{2}$$

which is the mean power at the input of the system. The mean square overloading signal level is:

$$\frac{E_{max}^2}{2} = \frac{V^2}{2}$$

and the mean signal-to-quantisation noise ratio at overload is,

$$\frac{s}{N_q} = \frac{3}{4\pi^2} \frac{(f_c)^3}{(B)^3} \text{ for } f_0 << B \qquad \text{(A1.4)}$$

1.3 DELTA SIGMA MODULATION WITH DOUBLE INTEGRATION

By applying the same arguments as above, the error power spectral density at the input to the receiver low pass filter is,

$$N_q = k^2(\Delta v)^2 \frac{2}{f_c} \quad \text{W/Hz} \quad \text{where } k=0.668$$

and the noise power at the output of the network $H^{-1}(f)$ is,

$$N_q^1 = k^2(\Delta v)^2 \frac{2}{f_c} \cdot |H(f)|^2$$

$$N_q^1 = k^2(\Delta v)^2 \frac{2}{f_c} \cdot \frac{(f^2+f_1^2)(f^2+f_2^2)}{f_1^2 f_2^2}$$

The total quantising noise at the final output (i.e. the output of the low pass filter of bandwidth B) is,

$$N_q = \int_0^B k^2(\Delta v)^2 \frac{2}{f_c f_1^2 f_2^2} \cdot (f^2+f_1^2)(f^2+f_2^2)df$$

$$N_q = \frac{2k^2(\Delta v)^2}{f_c f_1^2 f_2^2} \int_0^B (f^4+f^2f_2^2+f^2f_1^2+f_1^2f_2^2)df$$

By integration,

$$N_q = \frac{2k^2(\Delta v)^2}{f_c f_1^2 f_2^2}\left(\frac{B^5}{5} + \frac{f_2^2 B^3}{3} + \frac{f_1^2 B^3}{3} + f_1^2 f_2^2 B\right)$$

If f_1 is much smaller than B and f_2 is smaller than B

$$N_q = \frac{2k^2(\Delta v)^2 B^5}{f_c f_1^2 f_2^2}\left(\frac{1}{5} + \frac{f_2^2}{3B^2}\right)$$

and on substituting for k and Δv,

$$N_q = \frac{6.144B^3V^2}{f_c^5} \cdot (3B^2+5f_2^2) \qquad \text{(A1.5)}$$

Assuming an input signal $m(t)=E\sin\omega t$ at the input to the comparator, the signal is $E\sin\omega t.H(f)$ and the mean signal power at this point is $\frac{E^2}{2}|H(f)|^2$. The maximum mean signal power (corresponding to the limit of non-overloading) is $\frac{V^2}{2}.|H(f)|^2$

The signal power at the output of the low-pass filter is approximately equal to the signal power at the comparator input. Hence the signal power at the output of the $H^{-1}(f)$ network is (to be consistent with the condition of non-overloading)

$$\frac{V^2}{2}|H(f)|^2.|H^{-1}(f)|^2 = \frac{V^2}{2}$$

which is the maximum mean signal power of the system input. Hence,

$$\frac{S}{N_q} = \frac{V^2/2}{\frac{6.144B^3V^2}{f_c^5}.(3B^2+5f_2^2)}$$

$$\frac{S}{N_q} = \frac{f_c^5}{12.288B^3(3B^2+5f_2^2)} \qquad \text{(A1.6)}$$

APPENDIX II

PROGRAM LISTING

SIMULATION OF Δ-Σ MODULATION

```
JOB A4PLCC,E,AA2079
LUFORTRAN
JOBCORE 50K
VOLUME 9999
DOWN 22
RUN ,,1500
****
DOCUMENT SOURCE
      LIBRARY(ED,SUBGROUPNAGF)
      LIBRARY (ED,SUBGROUPUSUB)
      LIBRARY (ED,SUBGROUPGRAF)
      PROGRAM (DSIG)
      COMPACT
      COMPRESS INTEGER AND LOGICAL
      INPUT 1 = CR0
      OUTPUT 2 = LP0
      TRACE 2
      END
```

```
      MASTER DSIG
      REAL K
      REAL KY
      DIMENSION X(129),Y(129),K(129),AA(128)
      DIMENSION HH(128),BB(128,7),H(128),P(128),U(128),B1(129)
      DIMENSION B2(129),B3(129),Z1(129),Z2(129),Z3(129)
      DIMENSION AY(65),BY(65),CY(65),DY(65),AD(65),BD(65),ILST(14)
      DIMENSION  ZZ(129),KY(256),CLOCK1(256)
      DIMENSION BD1(65),BD2(65),BD3(65),BD4(65)
      DIMENSION E1(35),E2(35),E3(35),E4(35),E5(35)
      DIMENSION CLOCK(129),BD5(65),K1(64)
C  THIS PROGRAMME SIMULATES
C  DELTA SIGMA MODULATION AND
C  ANALYSES THE HARMONICS AND
C  PLOTTES THE VARIOUS WAVEFORMS
      CALL UTPOP
      DO 77 J=1,20
C  READ C WHERE X=C*SINK
C  READ R,RR
C  WHERER  AND  RR ARE THE CHARACTERISTICS
C  OF  THE  LEVEL  DETECTOR
C  WITH  DIFFERENT  VALUES  OF R  AND  RR  NONLINEARITY
C  INTRODUCED  AT  THE  LEVEL  DETECTOR
      READ(1,100) C,R,RR
  100 FORMAT(3F10.2)
      WRITE(2,339) C,R,RR
  339 FORMAT(1H ,///10X,2HC=,F10.5,10X,2HR=,F10.5,10X,3HRR=,F10.5///)
      S=0.9
      PI=3.14159264
C  SIMULATION OF THE 3- PHASE INPUT  WAVEFORMS
C-----------------------------------------------------------------
      DO 20 I=1,129
      M=I-1
      X(I)=C*SIN(PI*(M/64.0))
      Y(I)=C*SIN(PI*(M/64.0)+(2.0*PI)/3.0)
   20 K(I)=C*SIN(PI*(M/64.0)-(2.0*PI)/3.0)
C  BAND LIMITED NOISE INTRODUCED AT THE INPUT
C-----------------------------------------------------------------
      EPS=0.1
      CALL NOISE(X,EPS)
C  INITIAL  VALUES
C     ------------------------------------------------------------
      A1(1)=0.0
      B1(1)=0.0
      B2(1)=0.0
      B3(1)=0.0
      Z1(1)=R
      Z2(1)=R
      Z3(1)=R
```

```
C  SIMULATION  OF  DELTA - SIGMA  MODULATION
C-----------------------------------------------------------------
      A1(I)=X(I)-Z1(I-1)
      A2=Y(I)-Z2(I-1)
      A3=K(I)-Z3(I-1)
C  INTEGRATOR
      B1(I)=(B1(I-1)*S)+A1
      B2(I)=(B2(I-1)*S)+A2
      B3(I)=(B3(I-1)*S)+A3
C  LEVEL  DETECTOR  ACTION
      IF(B1(I)-0.0) 14,14,16
   14 Z1(I)=RR
      GO TO 21
   16 Z1(I)=R
   21 IF(B2(I)-0.0) 22,22,23
   22 Z2(I)=RR
      GO TO 24
   23 Z2(I)=R
   24 IF(B3(I)-0.0) 25,25,26
   25 Z3(I)=RR
      GO TO 17
   26 Z3(I)=R
   17 CONTINUE
C  GRAPH PLOTTING ON THE LINE PRINTER
C-----------------------------------------------------------------
      TIME0=1.0
      DELT=TIME0
      DO 29 I=1,128
      BB(I,1)=B1(I)
      BB(I,2)=X(I)
      BB(I,3)=Z1(I)
      BB(I,4)=Y(I)
      BB(I,5)=1.3*Z2(I)
      BB(I,6)=K(I)
   29 BB(I,7)=1.6*Z3(I)
      I1=1
      I2=128
      J1=1
      J2=7
      IC3=1
      TOP=2.0
      DIP=-2.0
      CALL PLOTH(BB,I1,I2,J1,J2,TIME0,DELT,IC3,DIP,TOP)
```

```
C  GRAPH PLOTTING ON THE OFFLINE PLOTTER
C  INPUT AND OUTPUT
C-----------------------------------------------------------------------
      DO 333 I=1,129
  333 CLOCK(I)=I-1
      XMIN=0.0
      XMAX=128.0
      YMIN=-2.0
      YMAX=2.0
      XINS=5.0
      YINS=3.0
      CALL UTP4A(XMIN,XMAX,YMIN,YMAX,5.0,3.0,4HTIME,1,5HINPUT,1)
      CALL UTP4B(CLOCK,X,128,2)
      CALL HISTOG(Z1,KY,CLOCK1,N)
      CALL UTP4B(CLOCK1,KY,N,2)
C  3-PH INPUT AND 3-PH OUTPUT
C-----------------------------------------------------------------------
      XMIN=0.0
      XMAX=128.0
      YMIN=-1.0
      YMAX=1.0
      XINS=5.0
      YINS=2.0
      CALL UTP4A(XMIN,XMAX,YMIN,YMAX,5.0,2.0,4HTIME,1,9H3PH-INPUT,1)
      CALL UTP4B(CLOCK,X,128,1)
      CALL UTP4B(CLOCK,Y,128,1)
      CALL UTP4B(CLOCK,K,128,1)
      YMIN=-2.0
      YMAX=2.0
      CALL UTP4A(XMIN,XMAX,YMIN,YMAX,5.0,2.0,4HTIME,1,7HOUTPUT1,1)
      CALL HISTOG(Z1,KY,CLOCK1,N)
      CALL UTP4B(CLOCK1,KY,N,2)
      CALL UTP4A(XMIN,XMAX,YMIN,YMAX,5.0,2.0,4HTIME,1,7HOUTPUT2,1)
      CALL HISTOG(Z2,KY,CLOCK1,N)
      CALL UTP4B(CLOCK1,KY,N,2)
      CALL UTP4A(XMIN,XMAX,YMIN,YMAX,5.0,2.0,4HTIME,1,7HOUTPUT3,1)
      CALL HISTOG(Z3,KY,CLOCK1,N)
      CALL UTP4B(CLOCK1,KY,N,2)
```

```
C  INPUT,V-COMPARATOR, V-INTEGRATOR, OUTPUT
C-----------------------------------------------------------------------
      XMIN=0.0
      XMAX=128.0
      YMIN=-2.0
      YMAX=2.0
      XINS=5.0
      YINS=2.0
      CALL UTP4A(XMIN,XMAX,YMIN,YMAX,5.0,2.0,4HTIME,1,5HINPUT,1)
      CALL UTP4B(CLOCK,X,129,2)
      CALL UTP4A(XMIN,XMAX,YMIN,YMAX,5.0,2.0,4HTIME,1,
     117HCOMPARATOR OUTPUT,2)
      CALL UTP4B(CLOCK,A1,129,2)
      CALL UTP4A(XMIN,XMAX,YMIN,YMAX,5.0,2.0,4HTIME,1,
     117HINTEGRATOR OUTPUT,2)
      CALL UTP4B(CLOCK,B1,129,2)
      CALL UTP4A(XMIN,XMAX,YMIN,YMAX,5.0,2.0,4HTIME,1,6HOUTPUT,1)
      CALL HISTOG(Z1,KY,CLOCK1,N)
      CALL UTP4B(CLOCK1,KY,N,2)
```

```
C  CALCULATION  OF  FOURIER  COEFFICIENTS
C     ------------------------------------------------------------
      WRITE(2,112)
  112 FORMAT(1H ,///10X,17HFOURIER  ANALYSIS///)
      WRITE(2,113)
  113 FORMAT(1H ,3HNO.,8X,10HPERCENTAGE,10X,5HPHASE//)
      L=1
      DO 28 I=1,127
      IF(Z1(I)-0.0) 350,351,352
  350 AA(L)=-1.0
      GO TO 28
  351 AA(L)=-1.0
      GO TO 28
  352 AA(L)=1.0
   28 L=L+1
      N=128
      M=30
      CALL FOURY(N,AA,H,U,P,M)
      DO 33 I=2,30
   33 HH(I)=100.*H(I)/H(2)
      WRITE(2,11) (I,HH(I),P(I),I=2,30)
   11 FORMAT(1H ,I3,10X,F10.4,10X,F10.4)
C  CALCULATION  OF  FOURIER  COEFFICIENTS  USING  C06AAF
C     ------------------------------------------------------------
      WRITE(2,112)
      NN=64
      DO 34 I=1,NN
      AY(I)=AA(I)
   34 BY(I)=AA(I+NN)
      N1=NN+1
      N1=14
      CALL C06AAF(AY,BY,N1,.FALSE.,M1,ILST)
      DO 38 I=1,N1
      CY(I)=AY(I)
      DY(I)=BY(I)
      AD(I)=SQRT(CY(I)*CY(I)+DY(I)*DY(I))
   38 CONTINUE
      DO 35 I3=2,N1
      BD1(I3)=ABS(100.0*DY(I3)/DY(2))
      BD2(I3)=100.0*AD(I3)/AD(2)
   35 CONTINUE
      DO 37 I4=2,64,2
      BD3(I4)=ABS(DY(I4))
      BD4(I4)=20.0*ALOG10(BD3(I4))
      BD5(I4)=20.0*ALOG10(AD(I4))
   37 CONTINUE
      WRITE(2,36) (I,CY(I),DY(I),BD1(I),AD(I),BD2(I),
     1BD4(I),BD5(I),I=1,64)
   36 FORMAT(1H ,I2,2X,F10.4,2X,F10.4,2X,F10.4,2X,F10.4,2X,
```

```
     1F10.4,2X,F10.4,2X,F10.4,2X,F10.4)
       WRITE(2,613)
  613 FORMAT(1H1,18HHARMONIC  ANALYSIS)
       WRITE(2,114) C
  114 FORMAT(1H ,2HC=,F4.2)
       WRITE(2,115)
  115 FORMAT(1H ,2HNO,6X,10HPERCENTAGE/)
       DO 41 I=2,64,2
   41 K1(I)=I-1
       WRITE(2,116) (K1(I),BD2(I),BD1(I),I=2,64,2)
  116 FORMAT(1H ,I2,6X,F10.4,6X,F10.4)
       E1(J)=BD5(2)
       E2(J)=BD5(4)
       E3(J)=BD5(6)
       E4(J)=BD5(8)
       E5(J)=C
    77 CONTINUE
C   PLOTTING FUNDAMENTAL,3TH,5TH,7TH COMPONENTS
C-----------------------------------------------------------------------
       XMIN=0.1
       XMAX=1.05
       YMIN=-80.0
       YMAX=10.0
       XINS=5.0
       YINS=4.0
       CALL UTP4A(XMIN,XMAX,YMIN,YMAX,5.0
      1,4.0,1HC,1,16HHARMONICS IN DBS,3)
       N=20
       CALL UTP4B(E5,E1,N,2)
       CALL UTP4B(E5,E2,N,2)
       CALL UTP4B(E5,E3,N,2)
       CALL UTP4B(E5,E4,N,2)
       CALL UTPCL
       STOP
       END
```

```
      SUBROUTINE PLOTH(A,I1,I2,J1,J2,TIMEO,DELT,IC3,DIP,TOP)
C THIS SUBROUTINE PLOTS MAXIMUM OF TEN GRAPHS ON THE SAME PAGE.
C FUNCTIONS PLOTTED ARE STORED COLUMNWISE EACH COLUMN
C EACH COLUMN CONTAINING ONE CURVE
C A CONTAINS THE DATA TO BE PLOTTED
C I1=FIRST ROW IN THE PLOT
C J1=BEGINNING OF COLUMN OF MATRIX OF A
C I2=END OF ROW OF THE MATRIX A
C J2=END OF THE COLUMN OF THE MATRIX OF A
C TIMEO= THE STARTING POINT FOR THE ABSCISSAE
C DELT= THE INCREMENT FOR THE ABSCISSAE
C IF IC3=0 DIP & TOP ARE PRESET TO THEIRVALUES IN THE CALLING PROGRAM
      DIMENSION A(128,7),SCALE(11),PLOT(101)
      DIMENSION H(10)
      DATA H(1),H(2),H(3),H(4),H(5),H(6),H(7),H(8),H(9),H(10),DOT,STAR
     1,BLANK/1H*,1HX,1H+,1HD,1HE,1HF,1HG,1HH,1HI,1HJ,1H.,1H*,1H /
      WRITE (2,17)
   17 FORMAT(1H1///56X,17HGRAPHICAL RESULTS///)
      IC4=1
      IF(IC3.GT.0) GO TO 12
      TOP=-1.0E10
      DO 7 I= I1,I2
      DO 7 J= J1,J2
      IF(TOP.GT.A(I,J)) GO TO 7
      TOP=A(I,J)
7     CONTINUE
      DIP=1.0E20
      DO 8 I=I1,I2
      DO 8 J= J1,J2
      IF(DIP.LT.A(I,J)) GO TO 8
      DIP=A(I,J)
8     CONTINUE
      GO TO 13
   12 DO 11 J=J1,J2
      DO 11 I=I1,I2
      IF(A(I,J).LT.DIP)   A(I,J)=DIP
      IF(A(I,J).GT.TOP)   A(I,J)=TOP
   11 CONTINUE
   13 DEL=0.1*(TOP-DIP)
      FACTOR = 100.0/(TOP-DIP)
      SCALE(1)= DIP
      IDIF=I2-I1
      IF(IDIF-25)14,14,15
   14 ISKIP=50/IDIF-1
      IC4=0
   15 CONTINUE
      DO 1 I=1,10
      K = I+1
      SCALE(K)= SCALE(I)+DEL
```

```
1       CONTINUE
        DO 2  I= 1,101
        PLOT(I)=DOT
2       CONTINUE
        WRITE(2,3)(SCALE(I),I=1,11),(PLOT(I),I=1,101)
3       FORMAT (16X,F9.4,10F10.4/20X,101A1)
        DO 4 I = 2,100
        PLOT(I)=BLANK
4       CONTINUE
        TIME= TIME0
        DO 9  I= I1,I2
        DO 5  J= J1,J2
        K=(A(I,J)-DIP)*FACTOR+1.5
        PLOT(K)=H(J)
5       CONTINUE
        WRITE (2,6) TIME,(PLOT(L),L=1,101)
 6      FORMAT (1X,F11.6,08X,101A1)
        DO 10 M= 2,100
        PLOT(M)=BLANK
10      CONTINUE
        PLOT(1)=DOT
        PLOT(101)=DOT
        TIME=TIME+DELT
        IF(IC4.NE.0)GOTO 9
        DO 9 IS=1,ISKIP
        WRITE (2,16)
   16   FORMAT (20X,'.',99X,'.')
9       CONTINUE
   33   RETURN
        END
```

```
      SUBROUTINE FOURY(N,A,H,U,P,M)
      DIMENSION A(N),U(N),H(N),P(N)
      N1=N/2
      AN=N1
      C1=3.14159265/AN
      I=2*N1
      U(1)=0.
      U(2)=A(I)
      DO 1 L=1,N+1
      K=L-1
      C=2.*COS(C1*FLOAT(K))
      DO 2 J=3,I
      J1=I-J+2
    2 U(J)=U(J-1)*C-U(J-2)+A(J1)
      AK=(0.5*C*U(I)-U(I-1)+A(1))/AN
      IF(K)0,0,6
      H(K+1)=AK/2.
      P(K+1)=0.
      GO TO 1
    6 IF(K-N1)3,0,0
      H(K+1)=AK/2.
      P(K+1)=1.57079633
      GO TO 5
    3 BK=(SIN(C1*FLOAT(K))*U(I))/AN
      H(K+1)=SQRT(AK*AK+BK*BK)
      P(K+1)=ATAN2(AK,BK)
    1 CONTINUE
    5 RETURN
      END
C-----------------------------------------------------------------------
      SUBROUTINE NOISE(X,EPS)
C   THIS SUBROUTINE ADDS BAND LIMITED
C   NOISE TO THE INPUT WAVEFORMS
C   AT INPUT X CONTAINS DATA
C   ON EXIT X CONTAIN OUTPUT
      DIMENSION X(129)
      KR=0.0
      DO 19 I=1,129
      X(I)=X(I)+UTR1(1,1,KR)*EPS
   19 CONTINUE
      RETURN
      END
```

```
      SUBROUTINE HISTOG(ZZ,KY,CLOCK1,N)
C  THIS SUBROUTINE SCALES THE INPUT  DATA  POINTS
C  TO  DRAW  A  HISTOGRAM  AND  CHANGES  THE  DATA
C  TO  SUIT  UTP4B
C  N  IS  THE  NO.  OF  POINTS  TO  BE  JOINED  BY  UTP4B
      REAL KY
      DIMENSION  ZZ(129),KY(256),CLOCK1(256)
      KY(1)=ZZ(1)
      CLOCK1(1)=1.0
      L=2
      N=2
  311 IF(ZZ(L).NE.ZZ(L-1)) GO TO 312
      KY(N)=KY(N-1)
      CLOCK1(N)=CLOCK1(N-1)+1.0
      N=N+1
      L=L+1
      IF(L.GT.128) GO TO 313
      GO TO 311
  312 KY(N)=KY(N-1)
      CLOCK1(N)=CLOCK1(N-1)+1.0
      KY(N+1)=-KY(N)
      CLOCK1(N+1)=CLOCK1(N)
      N=N+2
      L=L+1
      IF(L.GT.128) GO TO 313
      GO TO 311
  313 CONTINUE
      RETURN
      END
      FINISH
****
```

```
DOCUMENT DATA
C  1ST SET OF DATA
C C                R          RR
0.1              1.0        -1.0
.15              1.0        -1.0
0.2              1.0        -1.0
.25              1.0        -1.0
0.3              1.0        -1.0
.35              1.0        -1.0
0.4              1.0        -1.0
.45              1.0        -1.0
0.5              1.0        -1.0
.55              1.0        -1.0
0.6              1.0        -1.0
.65              1.0        -1.0
0.7              1.0        -1.0
.75              1.0        -1.0
0.8              1.0        -1.0
.85              1.0        -1.0
0.9              1.0        -1.0
.95              1.0        -1.0
1.0              1.0        -1.0
1.05             1.0        -1.0
C-----------------------------------------------------------------------
C  2ND SET OF DATA
C C                R          RR
0.1              0.7        -1.3
0.15             0.7        -1.3
0.2              0.7        -1.3
0.25             0.7        -1.3
0.3              0.7        -1.3
0.35             0.7        -1.3
0.4              0.7        -1.3
0.45             0.7        -1.3
0.5              0.7        -1.3
0.55             0.7        -1.3
0.6              0.7        -1.3
0.65             0.7        -1.3
0.7              0.7        -1.3
0.75             0.7        -1.3
0.8              0.7        -1.3
0.85             0.7        -1.3
0.9              0.7        -1.3
0.95             0.7        -1.3
1.0              0.7        -1.3
1.05             0.7        -1.3
****
```

APPENDIX 3

DESIGN EQUATIONS FOR 3-PHASE UNCONTROLLED RECTIFIER

Voltage equations are

$$E_{dc} = 0.955\ E_{max}$$

$$E_{max} = 1.05\ E_{dc}$$

$$E_{r.m.s.} = E_{dc}$$

$$E_{max} = \sqrt{3}\ E_T(max)$$

where:

$E_T(max)$ = maximum phase voltage of the transformer secondary.

Current relationships are

average current/rectifier leg, $I_0 = 0.33\ I_{dc}$ (same for inductive and resistive load)

$I_{r.m.s.}$/rectifier leg = $0.577\ I_{dc}$ (same for inductive and resistive load)

I_{pk}/rectifier leg = $1.05\ I_{dc}$ ($=I_{dc}$ for inductive load)

where I_{dc} is the output direct current.

fundamental ripple frequency = 6×f, where f is the supply frequency

$$\% \text{ ripple} = \frac{\text{r.m.s. fundamental ripple voltage}}{E_{dc}} \times 100 = 4.0$$

crest working voltage = $1.05\ E_{dc}$

For a LC smoothing circuit,

$$\% \text{ ripple} = \frac{1.133}{LC} \quad (L \text{ in Henrys and } C \text{ in } \mu F)$$

$$\text{r.m.s. ripple current} = \frac{E_{dc}}{46\ 500L}$$