BANDWIDTH COMPRESSION OF SONAR DISPLAYS

BY

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To Melrose and Pippa

who made it all worthwhile.

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SUMMARY

A major problem affecting the design of data compression systems is that of employing a buffer of limited size and at the same time prevent uncontrollable loss of data due to overflow. One method of alleviating this problem is to employ an adaptive compression algorithm. With this design approach when overflow is imminent the compression algorithm is degraded which effectively reduces the input rate to the buffer.

A method is proposed here, where by using a recirculating register as the buffer the recirculating data controls the input rate and hence the performance of the system.

The system has been analysed for a Poisson input process, and simulated using synthetic patterns similar to that encountered on sonar displays. The results indicate that this form of storage is quantitatively similar to random-access storage but qualitatively superior due to the random nature of the losses.

An experimental system has been built using dynamic MOS shift registers for the store and a simple run-length coding procedure.

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T_y - duration of fast time-base

T_x - duration of slow time-base

n_y - number of resolution cells along fast time-base

n_x - number of resolution cells along slow time-base

Q - number of probable brightness quanta

m - number of significant changes of brightness

H_{br} - brightness information

H_{pos} - position information

H_{tot} - $H_{br} + H_{pos}$ - total information

N_t - total number of resolvable elements

k - compression factor

C - information capacity of channel in bits/second

w - bandwidth of channel in Hertz

p - mean signal power in channel

n - mean noise power in channel

Chapter 3

$E(\ )$ - expected value of $(\ )$

ρ - traffic intensity = $\frac{\text{mean input rate}}{\text{mean output rate}}$

r - mean number of inputs generated in some time interval

n - queue length

T - service time

$P_i(\ )$ - probability of i words in queue at time $(\ )$

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$k_i(\ )$	-	probability of i Poisson arrivals in time ( )
N	-	buffer capacity
R_N	-	probability of overflow for buffer of capacity N
w	-	word length for recirculating register
t_s	-	bit time for recirculating data
S	-	maximum number of recirculating word spaces
t_d	-	target resolution time
P_C	-	probability of coincidence
P_I	-	probability of occurrence of data in the input data train for recirculating system
P_R	-	probability of occurrence of data in the recirculating data train
P(i)	-	probability of i words in output registers
k(i)	-	probability of i outputs from recirculating store
s	-	number of output registers
R_s	-	probability of overflows of output registers
B	-	probability of occurrence of data in an output word space

INTRODUCTION

Previous analysis has shown that the average information content of radar and sonar displays is much less than the maximum information rate of the system. However, any system which attempts to transmit information directly must provide sufficient bandwidth to accommodate the higher information rate.

For a conventional P.P.I. display there is a fast radial range scan, repeating every pulse repetition period, and a slower rotating bearing scan, synchronised with the antenna rotation. A typical aircraft surveillance radar has a scan period of 9 seconds and a sweep period of 3000 microseconds. If each sweep consists of 490 6-microsecond range bins, then the maximum information rate is of the order of 150KHz.

In the B-scan presentation, range and bearing are presented as orthogonal "X-Y" coordinates. In radar systems the range, or "X" scan, is normally a fast time base, while the bearing or "Y" scan is slower. In systems using within-pulse scanning, such as the electronic sector-scanning sonar[1], the bearing is the faster of the two time bases. For the sonar model, the bearing scan time is of the order of 100 microseconds. The normal resolution requirements suggest a 3 microsecond bearing resolution cell; hence the maximum information rate is of the order of 350KHz.

The accepted methods of transmitting information about target positions at a low information rate follow a general pattern. Firstly, some form of processing is done to remove redundant information. A

queueing buffer is then provided between the processor and the narrow bandwidth link. The buffer accepts information at a random rate, stores this information until it is removed for transmission. Figure (I.1) shows in schematic form the principal components of such a system.

The design of the output buffer is one of the most important tasks to be faced in implementing any bandwidth reduction system. The overflow of the buffer, usually occurring during periods of peak data activity, causes the loss of data samples. These losses are now even more critical since the removal of redundant information has already taken place.

The general method of overflow curtailment is to

(1) monitor the queue length of samples within the buffer, and

(2) use this information to control the redundancy removal algorithm.

Hence, if buffer overflow is imminent, the accuracy requirements can be relaxed thus reducing the input rate to the buffer.

This project is concerned with a remotely positioned sector-scanning sonar system; the video signals from the display are to be transferred over as narrow a bandwidth as possible to enable the sonar pictures to be reproduced on a single or on multiple displays.

A system has been designed[2] using analogue storage for the range and bearing coordinates of each target. This system, although very simple in implementation lacks flexibility due to its analogue nature. A study of fish behaviour shows that fish usually travel in shoals of random size and shape. These shoal distributions do not conform to any random discrete distribution; hence this system would fail in shoals when the overflow situation is most likely to occur.

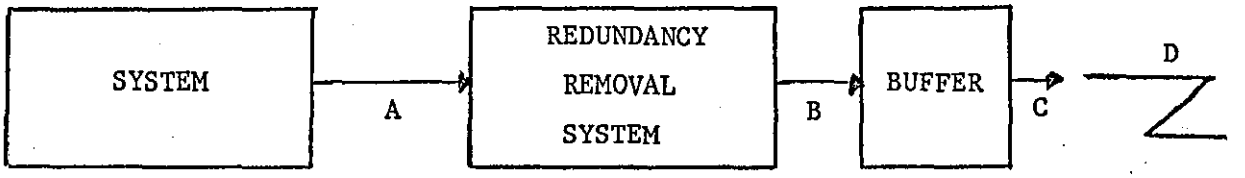
It is proposed to use a digital system in order to minimise this effect. A survey of several storage media was made[3,4] and it was decided to use semiconductor shift registers. This decision was based on the fact that it would fit in well in a clocked system, the size and power requirements are low, also with the improvement in fabrication techniques the prices of integrated circuits have been falling rapidly, while those of the other storage media have remained fairly constant.

In addition, it is proposed to use a serial access store as the buffer. Most bandwidth compression systems to date use a "step-down" type storage device. In these systems information enters the store filling the first vacant position closest to the transmission end. Information is removed at regular intervals from the head of the store, all data in store being shifted down. Hence, with this method parallel-in-parallel out facilities are necessary.

The use of a serial access store would be advantageous since these devices are cheaper than the random access types. However, the main reason for this choice is due to the loss mechanism of such a storage method. Information has to be recirculated between transmitting intervals. Losses will occur when recirculating information and new information seek entry to the store at the same time. A priority scheme built into the system will discard one set of information. These losses could be of some advantage due to the randomness of the coincidence phenomena. It is hoped that these coincidence losses will provide an inherent queue control mechanism. During periods of high data activity the coincidence losses will limit the input rate to the system, but these losses being evenly distributed would produce a more

tolerable effect at the receiving end than with the normal overflow losses.

This project therefore sets out to investigate the performance of this storage mechanism both analytically and practically. Due to the complex nature of the system and the lack of knowledge of the distribution of shoals, a Monte Carlo simulation is done to investigate its performance under near-realistic conditions.



A - Random Data Samples

B - Random Data Samples (Reduced average information rate)

C - Constant Data Rate

D - Transmission Channel

Figure I.1: Block Diagram of a typical Bandwith Compression System.

REFERENCES

1. Welsby V.C. and Dunn J.R.: " A High Resolution Sector Scanning Sonar".
Jnl.Brit.I.R.E., Vol 26, No. 3, September 1963.

2. Barrett C.J.: "Bandwidth Compression by Utilising the Redundancy in Sonar Displays".
M.Sc. Thesis, University of Birmingham, September 1965.

3. Spencer A.J.: "Proposals for Bandwidth Reduction of a Scanning Sonar Video Signal".
Departmental Memo. No. 9, Department of Electronic and Electrical Engineering, Loughborough University of Technology, July 1968.

4. Branson S.J.: "A Method of Removing Fixed Target Echoes from a Scanning Sonar System".
Departmental Memo. No. 42, Department of Electronic and Electrical Engineering, Loughborough University of Technology, May 1970.

CHAPTER 1

REVIEW OF BANDWIDTH COMPRESSION SCHEMES

1.1 Introduction

Data compression techniques have been used in many areas of communications such as voice, video, facsimile and telemetry transmission. These techniques have acquired added significance with the growth in use of digital computers for information processing, control and transmission. Previous schemes which transmitted analogue data are now converting their transmission processes to digital methods. These new schemes however, result in the need for additional bandwidths due to the high bandwidth requirements for digital transmission techniques. For example, a 3KHz voice signal is normally converted to a 64KHz PCM bit stream (8 bit samples at an 8KHz rate) for digital transmission.

Hence, the need for bandwidth reduction in these schemes is obvious. Several attempts have been made to apply these techniques to a number of systems. A summary of some of these schemes is reproduced below.

1.2 Bandwidth Reduction of Television Signals

Cherry and co-workers[1,2,3] have done extensive work on the compression of television signals. They have developed an experimental system and have been able to achieve a bandwidth reduction of 6:1.

In this method use is made of the correlation between successive

picture elements along a scan line; hence a system of run-length coding is used before feeding the data into the buffer. Two sets of data are then transmitted, the brightness data and the run-length data.

The Picturephone ® system[4] developed at the Bell laboratories represents one of the few commercial applications of a bandwidth reduction scheme. This is the video-telephone system whereby visual and aural communication is achieved over a 2-megabit/second channel. In this system use is made of the frame-to-frame correlation of the video signals first observed by Kretzmer[5]. By using a 67,000-bit buffer they have been able to transmit this information at the reduced bandwidth. The direct transmission method would have required a 16MB/second channel, hence a 8:1 reduction was achieved.

1.3 Telemetry Systems

Bandwidth compression techniques have been applied to aerospace systems used in the transmission of telemetry data from outer space. Compression is achieved in the conventional manner, by a redundancy removal processor followed by a queueing buffer.

One process used to decide which data samples to transmit and which were redundant was the "first-order interpolation" method. In general, interpolation methods consider data samples over a predetermined interval which do not exceed a prescribed tolerance level. The interpolator then computes the average value of the set and transmits this value to represent all samples within the set. All samples within the set are therefore within the prescribed peak error tolerance of the transmitted sample. If a sample value is found within the set which exceeds this

limit, the processor considers only values before this sample. Several orders of interpolation are possible, whereby higher orders are given more freedom in the selection of the starting and end points of the straight line. In the zero-order interpolator the transmitted value is simply the average between the most positive and most negative samples within a set. Each straight line starts from the end of the preceding line.

Another processing method used in telemetry systems involves a predictor algorithm. In this method the processor estimates the value of each new data sample based on past performance of the data. If the new value falls within the tolerance range about the previous value, it is rejected as redundant since it is known that the data value can be reconstructed within the specified tolerance. Several variations of this method are also possible; these are discussed in detail by Kortman[6].

After processing, data samples are fed into a buffer. The problem of buffer overflow is avoided by using an adaptive prediction or interpolation technique. Hence the tolerance limits are relaxed during periods of high buffer activity, thus reducing the input rate to the buffer.

In a series of experiments conducted with real time data, compression ratios of up to 20 have been achieved and reported by Medlin[7].

1.4 Radar Systems

With the increased activity at most large airports, the limitations of the human controller have resulted in a reduction in efficiency of

air traffic control. This has led to increased interest in the automation of radar target detection process. Eventually it is hoped that these automation processes will extend to air defence surveillance systems so that track-while-scan, aircraft identification, flight control and collision avoidance functions can be accomplished more efficiently by human operators aided by electronic computers. The peak data rate from the radar video processor can be as high as 1 MB/s hence the need for some form of bandwidth reduction.

Hinckley[8] has reported a system which digitally encodes the coordinates data from a radar, feeds this information into a queueing buffer and transmits the encoded data over a single telephone circuit. This system provides a bandwidth reduction of about 500 but with buffer capacity for 650 words.

In the previous system no analysis of the buffer requirements was conducted hence a large store was provided to minimise data loss due to overflow. A series of simulation runs by Bussard and Wilmot[9] examined the buffer requirements for automatic radar target detection systems. By simulating different aircraft flight patterns such as random targets, targets in formation or groups and targets in radial corridors, they have investigated the behaviour of the buffer under various conditions. The main conclusion of their study was that for the complex target formations larger buffers would be required than for randomly distributed targets.

1.5 Facsimile Systems

Digital coded facsimile systems have been developed employing

bandwidth reduction techniques. Such systems include the transmission of weather maps, newspapers and other typewritten documents.

A typical system consists of a flying-spot scanner which scans the document. A photomultiplier receives a modulated signal which triggers a position encoder.

Redundancy reduction techniques are applicable here since examination of most black-and-white graphics such as drawings and weather maps reveals that the number of black-and-white changes on a single scan line are but a small fraction of the total number of resolvable elements along the line. Run length coding as part of the encoding process followed by a queueing buffer results in bandwidth savings of up to 14:1.

One system reported by Rosenheck[10] is capable of transmitting a typical 8½ by 11-inch document at a resolution of 135 lines per inch in 7 seconds over a 50KB/second group channel. This represents a reduction of 5:1. In his method, use is made of the document as the storage medium. A variable velocity scanner is used which changes its speed according to the amount of information present. This process eliminates the electronic storage requirements entirely.

1.6 Sonar Systems

The need has arisen in the fisheries field for a system capable of transmitting target information from remote sonar systems with a reasonable degree of accuracy. Acoustic telemetry systems suffer from the fact that the maximum data rate possible is of the order of 10 K Bits/second. Direct transmission by other methods would require bandwidths

of the order of 150KHz.

The requirements here are not as stringent as with the previous systems, as the targets being observed would be mainly shoals of fish. Barrett[11] has designed a system whereby analogue signals representing range and bearing are stored, then transmitted at a lower rate. His storage device was a capacitor which was charged to a value proportional to the analogue signal. His system was designed to operate with a 40KHz bandwidth channel. This suggests a bandwidth reduction of about 4:1.

REFERENCES: CHAPTER 1

1. Cherry E.C. and Gouriet G.G.: "Some Possibilities for the Compression of Television Signals by Recoding".
Proc. Institute of Electrical Engineers, Vol 100, Part 3, January 1953.

2. Cherry E.C., Kubba M.H., Pearson D.E. and Barton M.P.: "An Experimental Study of the Possible Bandwidth Compression of Visual Image Signals".
Proceedings of the I.E.E.E., Vol 51, pp 1507-1517, November 1963.

3. Robinson A.H. and Cherry E.C.: "Results of a Prototype Television Bandwidth Compression Scheme"
Proceedings of the I.E.E.E., Vol 55, No 3, pp 356-364, March 1967.

4. Candy J.C., Franke M.A. (Mrs.), Haskell B.G. and Mounts F.W.: "Transmitting Television as Clusters of Frame-to-Frame Differences"
B.S.T.J., 50, No 6 (July-August 1971), pp 1889-1917.

5. Kretzmer E.R.: "Statistics of Television Signals"
B.S.T.J., Vol 23, February 1952.

6. Kortman C.M.: "Redundancy Reduction - A Practical Method of Data Compression"
Proc. of the I.E.E.E., Vol 55, No 3, pp 253-263, March 1967.

7. Medlin J.E.: "The Prevention of Transmission Buffer Overflow in Telemetry Data Compressors"
I.E.E.E. Trans. on Comm. Tech., Vol COM-16, No 1, pp 94-107, February 1968.

8. Hinckley G.L.F.: "An Experimental System for Automatic Radar Target Detection and Digital Coded Plot Extraction and Transmission"
Proc. I.E.E., Part B, Supplement No 19, Vol 107, pp 36-46, March 1960.

9. Bussard D.L. and Wilmot R.D.: "Queueing Requirements in an Automatic Radar Target Detection System Operating with a Narrow Bandwith Link".
I.E.E.E. Trans. on Systems Science and Cybernetics, Vol SSC-6, No 2, pp 81-91, April 1970.

10. Rosenheck B.M.: "FASTFAX, a Second Generation Facsimile System Employing Redundancy Reduction Techniques"
I.E.E.E. Transactions on Communication Technology, Vol COM-18, No 6, pp 772-779, December 1970.

11. Barrett C.J.: "Bandwidth Compression by Utilising the Redundancy in Sonar Displays".
M.Sc. Thesis, University of Birmingham, September 1965.

CHAPTER 2

INFORMATION CONTENT OF SONAR PICTURES

2.1 Introduction

The system under study is the electronic sector scanning sonar system where information is presented on a B-scan display. The bearing scan is the faster of the two time bases. Since the system will be a digital one, range and bearing information will be digitally encoded. One system uses a pulse width of 100 microseconds which corresponds to a range resolution of about 6 inches. Previous work suggests that 32 bearing cells would provide sufficient bearing resolution; hence each bearing coordinate is a 5-bit word. The word length for range coordinates will depend on the maximum range covered. For a range of 40 metres a 9 bit word is sufficient to represent range data.

2.2 Evaluation of information content of sonar pictures

Let the fast time-base be of duration T_y seconds, and the slow (range) sawtooth be of T_x seconds. Also let there be n_y resolution cells along the fast timebase and n_x along the slow timebase.

Now

$$n_x = T_x/T_y \tag{2.1}$$

assuming the flyback times are small. If the signal has Q equally probable brightness quanta and there are m significant changes of brightness, then the total brightness information is given by

$$H_{br} = m \log_2 Q \text{ bits per frame} \tag{2.2}$$

The total information also contains information of the position of these brightness changes. Now the total number of resolvable elements per frame is N_t, where

$$N_t = n_y n_x \tag{2.3}$$

Hence the number of possible independent positions of the m brightness changes is given by

$${}^{N_t-1}C_m = (N_t - 1)!/m!(N_t - m - 1)!$$

The amount of information is given by $\log_2$ of this quantity. It can be shown that this expression reduces to

$$H_{pos} = (N_t-1)\log_2(N_t-1) - m \log_2 m - (N_t-m-1)\log_2(N_t-m-1) \tag{2.4}$$

Hence the total information per frame is

$$H_{tot} = m \log_2 Q + (N_t-1)\log_2(N_t-1) - m \log_2 m - (N_t-m-1)\log_2(N_t-m-1) \tag{2.5}$$

In order to find the maximum information capacity we assume complete independence of picture elements, hence the number of significant brightness changes is the maximum possible, that is N_t-1. Equation 2.5 then reduces to

$$H_{tot} = N_t \log_2 Q \tag{2.6}$$

This indicates that no position information is required since all resolution cells are being described.

From Equation 2.5 it is also possible to obtain an expression for the average information content of the picture. If we consider the extreme case of only one significant brightness transition per frame,

such that m = 1, then

$$H_{tot} = \log_2 Q + (N_t-1)\log_2(N_t-1) - (N_t-2)\log_2(N_t-2) \quad (2.7)$$

For large N, $\log_2(N_t-1)$ and $\log_2(N_t-2)$ may each be taken as $\log_2 N_t$, thus we get

$$H_{tot} = \log_2 Q + \log_2 N_t \quad (2.8)$$

The first term on the right is the information contained in the single change of brightness out of the Q possible brightness levels, whilst the second term is the information of a single position out of N_t possible positions.

To find the total information content we define each of the m positions independently, hence we obtain for the average information content

$$H_{tot} = m(\log_2 Q + \log_2 N_t) \text{ bits per frame} \quad (2.9)$$

Comparing the maximum channel capacities for the two cases we find that by sending information only when occupied positions are found and sending none about the blank areas, a compression k is realisable where

$$k = N_t \log_2(Q+1) / \left(m \log_2(Q+1) \times N_t\right) \quad (2.10)$$

If we are only interested in the presence or absence of targets then there is no need to specify the brightness levels, hence Q = 1 and

$$k = N_t/m \log_2 N_t \quad (2.11)$$

In the system under study it is proposed to use a 9-bit word for range and a 5-bit word for bearing coordinates.

Hence, $N_t = n_x n_y = 16,384.$

On a particular display studied by Barrett[1] an estimated 250 targets per frame were found. Thus

$$k = \frac{16,384}{250 \times \log_2 16,384} \simeq 4.5$$

This suggests that if the channel capacity is equal to the average information rate from the display, then a bandwidth reduction of 4.5 is possible.

It is of interest to evaluate the channel capacity required for direct transmission. Shannon's formula states

$$C = 2W \log (1 + p/n) \qquad (2.12)$$

where C = information capacity of channel in bits/second

W = bandwidth of channel in Hertz

p = mean signal power in channel

n = mean noise power in channel

The bandwidth of the channel should be such that adjacent elements along the fast scan line are resolvable. Hence, for direct transmission of the video signal the minimum bandwidth required is $\frac{1}{2}(n_y/T_y)$ Hz, since from the sampling theorem a bandwidth of $a/2W$ Hz is sufficient to transmit W independent samples per second. If the signal has Q distinctive levels of brightness, a signal-to-noise ratio of Q is required to distinguish between them in the channel. Hence from Equation 2.12

$$C = 2 n_y \log_2(Q+1)/2T_y \qquad (2.13)$$

$$= \frac{n_y}{T_y} \log_2(Q+1) \quad \text{bits per second.}$$

Since there are $1/T_x$ frames per second, the channel capacity is given by

$$C = n_x n_y \log_2(Q+1) \quad \text{bits per frame period}$$

$$= N_t \log_2(Q+1) \quad \text{bits per frame period} \qquad (2.14)$$

This is similar to the expression obtained by considering the information content of the picture. The significance of this is that if all the elements of the display are statistically independent, and all levels equally likely, then the maximum channel capacity is necessary and direct transmission is as efficient as possible.

2.3 Number of targets on typical displays

In an attempt to estimate the average number of targets on a typical display, Barrett[1] found that permanent echoes accounted for a high percentage of the targets detected. In the situation he considered the sector-scanning sonar was being used to observe the behaviour of fish in the River Forth. The system was placed in front of the cooling water intakes at Kincardine Power Station. He found that of the 250 targets per frame, only 100 were due to moving targets. The permanent echoes in this case were due to bottom echoes, the intake piers, and transmission interference. An increase in compression factor would therefore be possible if these permanent echoes were removed from the display. An attempt is being made elsewhere to apply frame subtraction techniques to this problem in order to remove these unwanted echoes[2,3]

However, the situation described cannot be taken as a true reflection of the number of fish likely in any other situation. The

only deterministic criterion that can be applied to fish behaviour is that they usually travel in shoals, with a random number of fish leaving the main shoal occasionally. The permanent echoes found on a display would again depend on the environment. Some echoes, like bottom echoes, reverberation echoes, and transmission interference, are usually present, although not all these will be absolutely permanent.

In a series of sea trials using a sector-scanning sonar, Voglis and Cook[4,5] observed shoals of varying sizes and shapes during search runs. Some shoals displayed a long thin ribbon-like structure while others showed an elliptical shape. Also, in contrast to the compact formations of these two types, there were others showing a distinctly diffuse structure. These in fact occupied a sizeable portion of the display.

In an attempt to arrive at an average number the author also conducted several subsidiary experiments on stills of actual displays. This was done by scanning films of a variety of situations. The number of targets recorded varied from 800 for the thin shoals to 3000 for the extended shoals.

Since no definite statistical model for shoal distributions can be inferred from these investigations, the only alternative is to apply some form of adaptive coding to the system. The selected method could be similar to one of those described in Chapter 1. The system can then be designed to handle a certain target density and the design specifications relaxed during areas of high data activity.

2.4 Possibilities for Run-Length Coding

In Section 2.2, the average information content of the sonar picture was evaluated by defining the position of each of the m targets independently. However, in sonar as in television displays there is a certain amount of element to element correlation along a scan line. It is therefore not necessary to define each position independently; rather it is possible to define runs of target positions. Cherry and co-workers[6] have applied run-length coding to their experimental TV bandwidth compression system. In practice the number of possible run lengths is very large; however, to utilise this to the full capability would create instrumentation problems. In addition, this information has to be buffered before transmission, hence in the case of data loss due to overflow, this may result in the distortion of the output if a long run is lost.

Vieri[7] and others have measured the run-length probability distribution of data from television pictures and have found that these signals have an exponential distribution with negative exponent, so that an upper limit on the maximum permissible run length is possible. In Cherry's system the method of run-coding is modified such that permissable run lengths is restricted to a small subset of the original distribution. Hence all other run lengths are broken up into suitable combinations of these standard runs by insertion of additional redundant samples.

2.4.1 *Probabilistic Model for Run-Length Coding*

Although several workers in the data-compression field have applied

run-length coding to their particular systems[6,7,8] no generalised theoretical approach has been ~~done~~ made. Run-length coding lends itself readily to optimum codes of the Shannon-Fano or Huffman types[9]; however, since the efficiency of these codes is sensitive to the probability distribution of the run-lengths, an empirical approach is usually preferred to the theoretical approach.

Capon[10] has attempted an analysis of run-length coding systems with the aim of predicting more generally the bandwidth reduction possible. He considers only black and white pictures and a binary digital transmission channel. Since the process of scanning reduces a picture from a two-dimensional array of cells to a one-dimensional sequence of cells, a first-order Markoff process representation for pictures is used. His treatment also depends to some extent on an a priori knowledge of the probability distribution of the run-lengths; however, some general guidelines have emerged from his investigation. He has shown among other things that:

1. for pictures which are equivalent to random patterns there is no point in using run-length coding, as there is very little to be gained;
2. for pictures with long white runs (targets) very large savings can be obtained;
3. for pictures which are either completely black or completely white large savings can again be obtained.

Most of these results could be arrived at intuitively, but by determining the several probabilities a quantitative insight is possible.

2.4.2 *Possibilities for Run-Length Coding of Sonar Pictures*

Pictures from a fish detecting sonar display should lend themselves to run-length coding. Since the display will consist mainly of shoals, this represents condition 2 in Capon's results described in Section 2.4.1, that is, long target runs. Hence, instead of encoding each target position independently, one could encode runs of target positions. One simple method of implementation would be to encode the first position and the length of the run.

Once again a knowledge of the probability distribution is necessary to select the optimum code. In the absence of such data a fixed length code can still be used.

In a subsequent chapter the results of simulations involving a simple run-length coding method are given.

REFERENCES: CHAPTER 2

1. Reference 2 - Introduction

2. Reference 4 - Introduction

3. Branson S.J.: "Further details of the Proposed Method of Removing Fixed Target Echoes from a Scanning Sonar System"
Departmental Memo. No 57, Department of Electronic and Electrical Engineering, Loughborough University of Technology, April 1971.

4. Voglis G.M. and Cook J.C.: "Underwater Applications of an Advanced Acoustic Scanning Equipment"
Ultrasonics, pp 1-9, January 1966.

5. Cook J.C.: "Scanning Sonar and the Fishing Industry"
Ultrasonics, pp 139-143, July 1967.

6. Cherry E.C.: Reference 2 - Chapter 1.

7. Deutsch S.: "Some Statistics Concerning Typewritten or Printed Material"
Microwave Res. Inst., Poly. Inst. of Brooklyn, Report No R-526, October 31, 1956.

8. Michel W.S.: "Statistical Encoding for Text and Picture Communication"
Communications and Electronics, Vol 35, pp 35-36, March 1958.

9. Reza F.M.: "An Introduction to Information Theory"
McGraw-Hill Book Company, Chapter 4.

10. Capon J.: "A Probabilistic Model for Run-Length Coding of Pictures"
I.R.E. Transaction on Information Theory, Vol IT5, No 4,
pp 157-163, December 1959.

CHAPTER 3

BUFFER DESIGN FOR BANDWIDTH COMPRESSION SYSTEMS

3.1 Introduction

The design of the output buffer is one of the most important tasks to be faced if an efficient system is to be implemented. After the redundancy removal techniques have been implemented, data from the system will still arrive at a variable rate. The buffer accepts these data samples, stores them to permit transmission at a constant rate. The efficiency of the buffer, as well as the effectiveness of the redundancy removal technique thus determine the amount of compression obtainable.

The main problem in designing this buffer is that of determining the buffer size required to ensure a tolerable loss of data due to overflow. Overflow is even more undesirable in bandwidth reduction systems since redundant samples have already been removed.

One important requirement for proper design is a knowledge of the probability distribution of the input data. This varies from source to source and only empirical data can provide this information for a particular system. A variety of systems have Poisson distributed input sources, hence for ease in comparison this distribution will be used in all analyses. However, where the distribution of the input is unknown or has been shown to be unlike any known distribution, a Monte Carlo simulation has to be done. The approach is described in Chapter 4.

3.2 Elements of Queueing Systems

Since the design of buffers for bandwidth compression systems is similar to that for any queueing system it is worthwhile examining the elements of a queueing system.

The basic system consists of an input source, a queue, and one or more channels or servers.

The input source gives rise to inputs and is characterised by the time distribution with which it gives rise to these inputs. Of the distributed sources the easiest to handle is the Poisson process, which is considered the most random of all discrete processes.

While in the queue the input quantity is usually referred to as a customer. A customer in a traffic queue would be a motor vehicle; in a bandwidth compression buffer, a customer would be a digital word. Queues may be infinite, whereby all customers can be accepted, but suffer a waiting time. Congestion may occur in this situation but no customers are lost. If the queue length is finite, customers arriving to find the queue filled will in most cases leave the system and be lost. This is the overflow situation, and the main reason for this analysis is to examine the parameters at one's disposal which will help to minimise the probability of overflow. Special queues may be found where customers return to test the system occasionally to see if space is available.

The output channels or servers are placed at the head of the queue. The amount of time the customer spends in the channel is called the holding time or the service time. Holding times may be constant or distributed. The server is responsible for implementing the "queue

discipline", which is the order in which customers are served. Usually the "first-come-first-served" discipline is used, but situations occur where priority systems are introduced.

3.3 Queueing aspects of Bandwidth Compression Systems

In most bandwidth compression schemes the elements of the system involve a distributed input source, a finite capacity store, and a constant service mechanism operating on a "first-come-first-served" basis.

The input will be a digital word encoded to represent some position or amplitude information.

The storage device is usually one of the accepted electronic storage devices, that is, magnetic core, semiconductor shift-registers, etc. The storage scheme may be of the step-down type where each bit enters the store in parallel filling the first vacant position closest to the service end. Information is removed at regular intervals from the head of the queue, all words in store being shifted down accordingly.

If a serial access device is used as a buffer, the words in store are recirculated until service is offered. A word is entered into store as soon as a word space becomes available, and removed when possible during a service interval. The queue discipline may be described as pseudo- "first-come-first-served", since the channel will accept the first word that appears when service is offered. However, due to the recirculation of data the first word out may not be the first one in.

In addition, with the recirculating store there may be loss of

data due to a new customer and a recirculating customer seeking entry to the store at the same time. This is the coincidence phenomenon, and a priority system has to be implemented.

The server in bandwidth compression systems is usually a digital clock operating at a frequency determined by the channel capacity. Synchronous transmission is usually applied; that is, data are removed from the buffer at each discrete clock time. Data arriving at the head of the queue during periods between clock times have to wait to begin service at the next clock time, even if the service facility is idle at the time of arrival.

3.4 Input Source Statistics of Bandwidth Compression Systems

The first step in any analysis is to establish a valid statistical description of the input source. Although general formulae can be developed for the design of the system as a whole, only tests on the actual data input can produce any meaningful information concerning the input distribution of any particular system.

For telemetry data compression systems used on space vehicles, buffers have been designed by assuming that the occurrence of the data samples entering the buffer is random and the time intervals between successive events are independent. This would produce either a Poisson or Binomial input distribution. Simulation tests with actual telemetry data indicate that the buffer input statistics agree very closely with the Poisson distribution[1].

In a television bandwidth compression scheme where run-length coding is used[2], it has been shown that successive run lengths along a

television scan line are independent. Buffer design has been carried out by considering the input as Binomially distributed. In addition it was reported that these run coded signals exhibit "short-term" stationarity, that is, the mean input rate undergoes "long-term" variations only.

Bussard and Wilmot[3] have investigated the queueing requirements in an automatic radar target detection system used in air traffic control. Their systems models, which were described in Section 1.4, covered the usual target patterns found in aircraft flights. Their results indicated that the complex target models created queues whose mean and variance were significantly larger than that created by the simplified model with all targets randomly located. Their conclusion therefore was that the assumption of Poisson target arrival rates can cause an appreciable error in modelling radar target detection queueing systems.

Barrett's system[4] for the bandwidth compression of sonar displays was designed on the assumption that the input was Poisson distributed. However, since the targets are usually fish shoals, a situation similar to Bussard and Wilmot's close formation clusters is more likely to exist. The author has simulated a queueing system by generating synthetic inputs typical of the shoaling situation[5]. It was found that losses were greater when using the shoal-like inputs than with the Poisson distributed inputs. The results of this investigation will be discussed fully in Chapter 4.

3.5 Analysis of the Step-Down Buffer

3.5.1 Expected Queue Length

Following a method due to Kendall, it is possible to obtain an expression for the mean queue length without specifying anything about the nature of the input distribution, or the distribution of the holding time. This method is described in detail by Goode and Machol[6] and the analysis is reproduced in Appendix 1.

By examining the expected queue length at an instant of time immediately after a word removal attempt, it can be shown that the expected queue length is

$$E(n) = \rho + \frac{E(r^2) - \rho}{2(1 - \rho)}, \qquad \rho < 1 \tag{3.1}$$

where n represents the number in store, r the number of words clocked into the buffer during T, and ρ the traffic intensity of the system. Equation 3.1 holds for arbitrary input distributions and holding times provided these distributions are independent of n, and that statistical equilibrium exists.

For a Poisson distributed input and constant holding time, Equation 3.1 reduces to

$$E(n) = \frac{\rho(2 - \rho)}{2(1 - \rho)}, \qquad \rho < 1 \tag{3.2}$$

It is obvious from Equations 3.1 and 3.2 that for equilibrium to exist, ρ, the traffic intensity must be less than 1. In other words, the output rate must be greater than the mean input rate. Figure 3.1 shows graphically the variation of E(n) with ρ, and indicates the rapid variation as ρ approaches unity. Hence, to reduce E(n), ρ should be as small as possible. However, since the output clock rate varies inversely

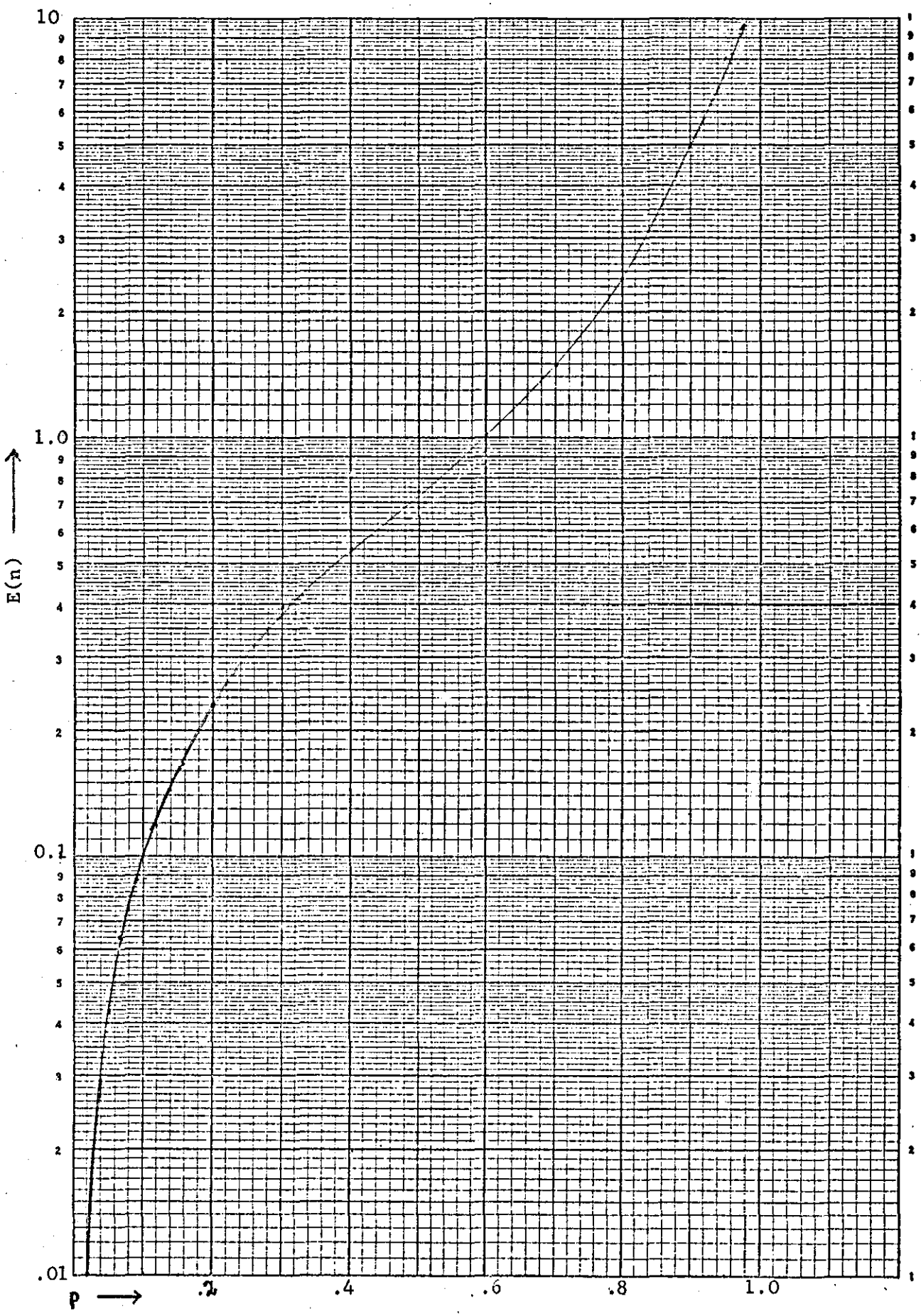


Figure 3.1: Variation of mean queue length with ρ

as ρ, a compromise must be reached since the eventual aim of the system is to use the smallest bandwidth possible.

3.5.2 *Queue length Statistics for Poisson Input and Constant* Output Rate

In this section we consider the buffer behaviour for a Poisson input process with constant removal rate. The problem here is that given a finite capacity buffer and known mean input and output rates a knowledge of the fractional word loss due to overflow is required.

This is a particular case of the M/D/s queueing system, where M indicates a Poisson input, D a deterministic service mechanism and s the number of servers. Prabhu[7] derives expressions for the case of the infinite length buffer with multiple servers. Several workers, including Dor[8], Medlin[1] and Schwarz[9], have investigated the case of the finite length buffer with one server. The essential aspects of the derivations for the single server case are given below.

Let Q(t) be the number of words present in the queue at time t; hence

$$P_n(t) = P_r\{Q(t) = n\}, \quad (n \geq 0) \tag{3.3}$$

Now we can consider Q(t) over consecutive intervals (0,t), (t+T), by examining the state of the queue just before or just after a sampling instant. Both approaches produce similar results since

Probability of n words in queue just before a sampling instant = Probability of n-1 words just after.

If we examine the queue just before each sampling instant then,

$$P_n(t+T) = \sum_{i=o}^{1} P_i(t)\, k_n(T) + \sum_{i=2}^{n+1} P_i(t)\, k_{n+1-i}(T) \qquad (3.4)$$

where $P_n(t+T)$ = Probability of n words in queue just before a sampling instant

$P_i(t)$ = Probability of i words in queue at time t

$k_n(T)$ = Probability of n arrivals during time T.

The first part of the right-hand side of this expression accounts for the combined probability of there being $i \leq 1$ words in the queue at time t and n arrivals during time T. Hence one customer is served and n enter the queue. The second part of the expression accounts for the case where $i \geq 2$ words are in the queue at time t; one will be served leaving i-1, hence n-i+1 words must enter to give the probability P_n.

We shall assume that statistical equilibrium exists, that is,

$$P_n(t) = P_n(t+T) = P_n \qquad (3.5)$$

$$\therefore \quad P_n = (P_o + P_1)k_n + \sum_{i=2}^{n+1} P_i\, k_{n+1-i} \qquad (3.6)$$

$$\text{for } 1 \leq n \leq N$$

Since the buffer is of length N, then clearly the following conditions exist,

$$P_{N+1} = 0 \qquad (3.7)$$

and

$$\sum_{i=0}^{N} P_i = 1 \qquad (3.8)$$

Equations 3.6, 3.7 and 3.8 describe the conditions which govern the buffer behaviour under the constraints mentioned.

3.5.3 Derivation of Probability of Overflow

To find the probability of overflow R_N, we note that the buffer input rate is lower than the rate of word removal attempts by the factor ρ. Hence, for an infinite length buffer with no overflow the probability that on any given removal attempt a word would be removed from the queue would be ρ. For a finite length buffer, however, the probability that a fraction will be lost due to overflow will reduce this probability. Hence, for a finite length buffer,

$$\Pr\{\text{Removing a word}\} = \rho(1 - R_N) \tag{3.9}$$

Thus

$$\Pr\{\text{Not removing a word}\} = 1 - \rho(1 - R_N) \tag{3.10}$$

Now a word will not be removed from the buffer at time $t + T$ if and only if at time t, $n = 0$ or 1, and there are no new entries during the interval T.

Hence,

$$P_o k_o + P_1 k_o = 1 - \rho(1 - R_N), \tag{3.11}$$

But from Equation 3.4

$$P_o(t + T) = P_o(t)k_o + P_1(t)k_o \tag{3.12}$$

Thus
$$P_o = 1 - \rho(1 - R_N) \tag{3.13}$$

or
$$R_N = \frac{P_o + \rho - 1}{\rho} \tag{3.14}$$

To determine P_o for each N use is made of the equations derived in the previous section. Equation 3.6 can be expressed in recursive form as

$$P_{n+1} = \left\{P_n - (P_o + P_1)\, k_n - \sum_{i=2}^{n} P_i\, k_{n-i+1}\right\} \Big/ k_o \tag{3.15}$$

For the Poisson distributed input,

$$k_n = e^{-\rho}\, \rho^n \Big/ n! \tag{3.16}$$

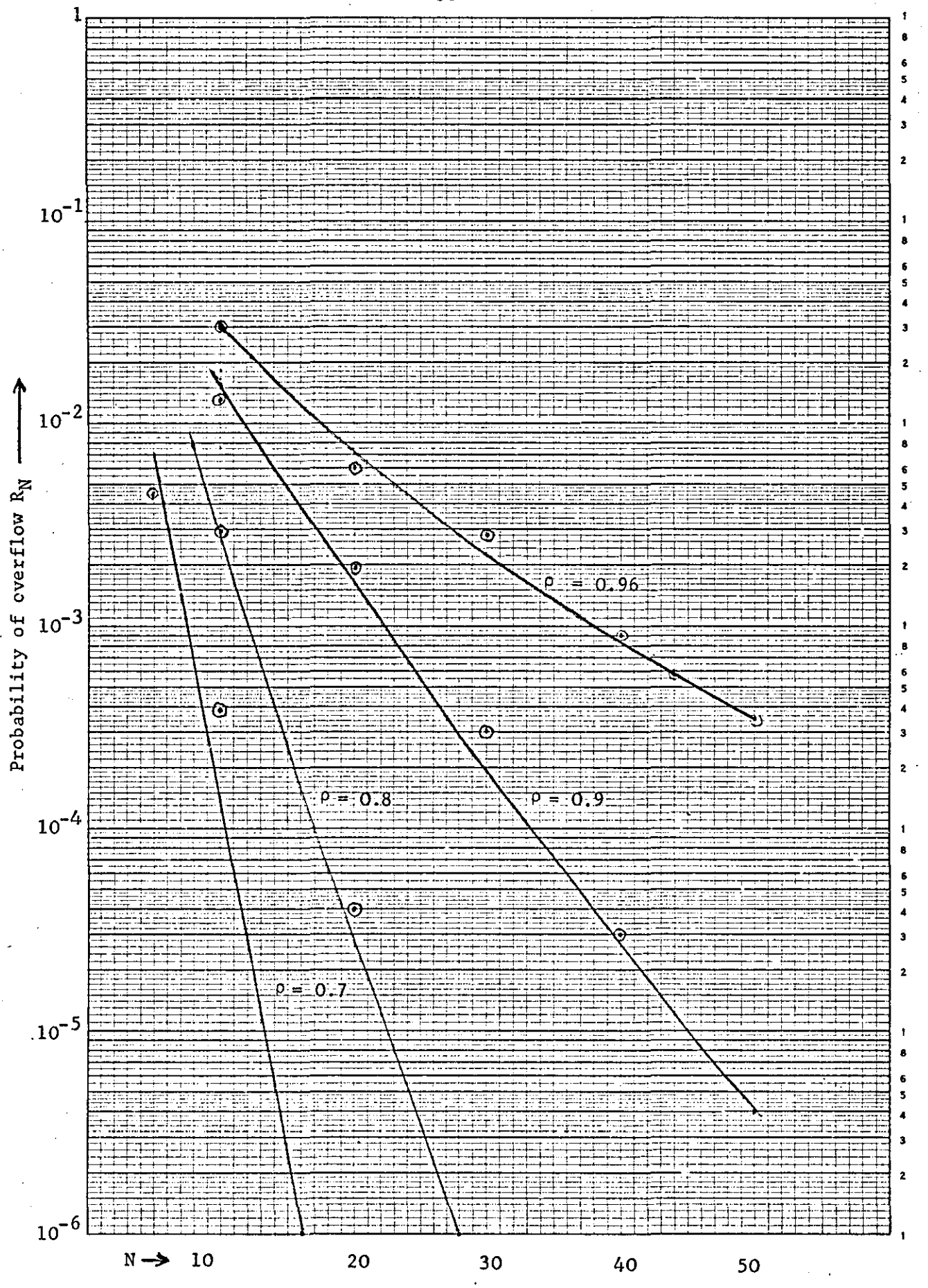


Figure 3.2: Probability of overflow for a fixed length store.

Equations 3.15 and 3.16 can be used to find P_n in terms of P_o by iteration. Equation 3.8 can then be used to find P_o solely in terms of k.

Hence given N, values of R_N can be calculated for various values of ρ. Figure 3.2 shows a plot of R_N against N for several values of ρ.

3.5.4 *Discussion of results*

The parameters at the disposal of the designer are the mean input rate, output rate, and buffer size. The choice of adjustable parameters will depend on the peculiarities of the system under consideration.

For bandwidth compression systems the output rate is usually fixed, its value being determined by the bandwidth of the channel. In addition, varying this parameter would cause difficult synchronising problems at the receiver.

The usual approach is to select a value of R_N which would present a tolerable reproduction at the receiving end. Once this value is chosen there is a choice between selecting the store size for a given value of ρ or vice versa. Assuming the channel capacity is given, and the input rate is known, one chooses N by consulting Figure 3.2 to satisfy the selected value of R_N.

The choice of R_N again depends on the pecularities of the system. For transmission of television pictures, loss of data samples, especially during movement, produce distorted pictures, hence a low value of R_N is necessary. Transmitting information from a sonar display would

not suffer from the same sensitivities, since the loss of an occasional fish would not be very critical. Cherry and co-workers[2] found that a 1% overload probability was sufficient. In both these cases which involve human observers the choice of R_N has to be a subjective one.

On close examination of Figure 3.2, it can be seen that increasing the buffer size indefinitely does not produce a proportional decrease in the overflow probability. As N approaches infinity, the probability of overflow does decrease, however, the mean waiting time increases. Philopyprou and Tzafestas[10] have studied the buffer behaviour in terms of waiting times and have derived an expression for mean waiting time as a function of ρ, R_N and N. They have shown that

$$(T_w/T)_{max} = \left((N - 1)/(\rho - \rho R_N)\right) - 1 \qquad (3.15)$$

where T_w is the mean waiting time.

For example, for $\rho = 0.9$, $(T_w)_{max} = 25T$. The implication here is that for practical purposes there is an optimum value for N for a given value of ρ.

Also, in deriving this expression for R_N, statistical equilibrium was assumed. However, in all these systems data bursts may occur which would temporarily overload the system. Once the buffer size is fixed, with the output rate fixed, the only adjustable parameter is the input rate. The floating aperture redundancy removal technique overcomes this effect by degrading the compression algorithm when overflow seems imminent. One possible method of implementation is to use an up-down counter as buffer load detector; this could be used to trigger a change

in the compression algorithm when the overload situation is being approached.

3.6 The recirculating register as a buffer

3.6.1 Introduction

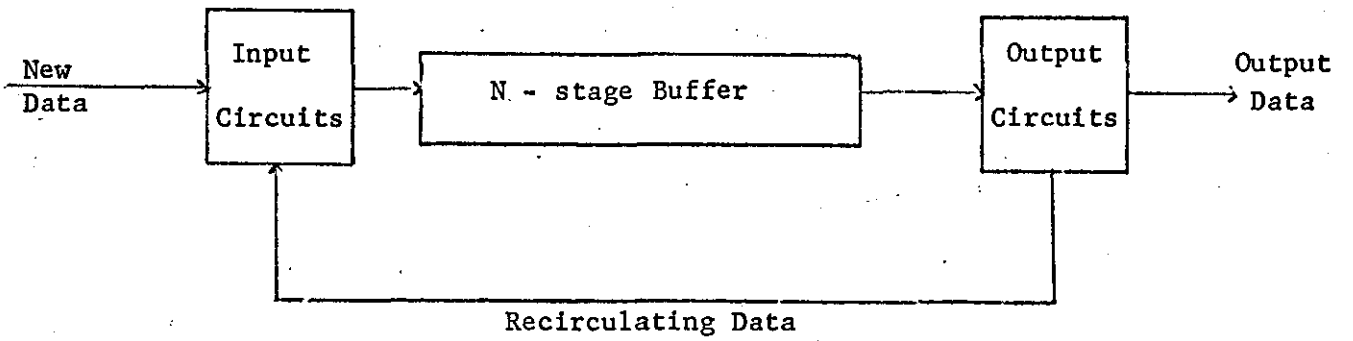


Figure 3.3 The recirculating storage system

Figure 3.3 shows in schematic form the basic elements of the system. The buffer consists of an N-stage register being clocked at a rate of $1/t_s$ Hertz. The Output Circuits contain s parallel registers each capable of receiving one word at the recirculating clock rate. The output circuits also consist of logic circuits which examine the N^{th} storage location at the end of every wt_s seconds. If a word is present and one of the s output registers is vacant, then that word is shifted into the vacant output register at the fast clock rate. The output clock operates in a similar fashion to the clock system used in the step-

down stores. It opens a gate every T seconds and shifts data from the first occupied output register at a rate of 1/wT Hertz if serial transmission is used or 1/T Hertz if parallel transmission is used. When all s registers are filled all words are recirculated until the next service period.

The Input Circuit controls the entry of data to the main register. Data arrive from the source at a maximum rate of $1/t_d$ Hertz. Each word is transferred in parallel to an input buffer which is identical in design to each output register. The Input Circuit examines the recirculating train and the input buffer at the end of every wt_s seconds. If new and recirculating data seek entry to the store at the same time one word will be selected in preference to the other. It is immaterial which word is accepted since the input buffer could be used to hold the recirculating word.

3.6.2 Analysis for a Poisson input and a single output register

The main loss phenomenon in this system is that due to coincidence between the input and recirculating trains. As with the step-down system overflow losses are also possible; however, when this situation exists there will be a word in each of the recirculating word spaces, thus coincidence always occurs. Hence, analytically there will be no difference between the two loss phenomena. However, coincidence under other circumstances should be more random. The effects of these two losses will be demonstrated in the simulation experiments to be discussed in Chapter 4.

The system can be analysed by considering it as three queues operating in series. Data are accepted by the input buffer and are either fed directly into the main register or removed in a distributed manner whenever an empty word space occurs in the recirculating train. The output of the Input Circuit forms the input to the N-stage recirculating register; its output in turn forms the input to the output buffer. The output buffer is in fact a simple step-down store; data being removed at the output clock rate. The overflow of the output buffer determines the amount of data recirculated.

It is convenient to examine the state of the system at the beginning or end of every output interval. During this time a maximum of S words can be shifted out of the main store. Hence there are S word spaces in the recirculating data train. Since the input buffer synchronizes the input data with these word spaces then to evaluate the probability of coincidence we need to consider the distribution of data over the S word spaces.

It is obvious from the nature of the recirculating system that the probability of coincidence will be a function of the statistical behaviour of data in both input and recirculating trains. Since a random input process has been assumed, then the behaviour of data in the input train can be easily analysed. However, the distribution of data in the recirculating train would be of a complex nature due to the feedback in the system. It is felt that there will be some correlation between successive data samples in this train, hence the suggested complexity. Attempts to produce a rigorous solution proved futile; however, since the aim of the investigation was to gain insight into the performance of the system it was decided to use the following approach which should produce an approximate solution.

The first assumption is to consider the probability or coincidence as a function of P_I and P_R; that is

$$P_I = F(P_I, P_R), \tag{3.18}$$

where P_C = Probability of coincidence

P_I = Probability of occurrence of one or more data samples in the input train

and P_R = Probability of occurrence of one or more data samples in the recirculating train.

We further assume that this function is of a product type, hence we write,

$$P_C = KP_IP_R , \tag{3.19}$$

where K is some constant which would depend on the other parameters in the system. If we make the simplifying assumption that K = 1, which can only be justified in the light of agreement finally found between theoretical and simulated results, then we can write,

$$P_C = P_IP_R , \tag{3.20}$$

This equation, although derived by making gross assumptions, produces the expected result for P_I or P_k equal to zero. Also it gives roughly the right kind of behaviour as either P_R or P_I varies.
Thus, if the amount of data in the recirculating train increases, one would expect the probability of coincidence to increase and Equation 3.20 gives a variation of this kind.

In order to calculate P_I, we note that,

P_I = 1 - Probability of occurrence of no data in the input train.

Now $$P_I = \sum_{j=1}^{S} P_j \,, \tag{3.21}$$

where P_j is the probability of finding j words in the input train, and

$$P_j = {}^{S}C_j p_i^j (1 - p_i)^{S-j} \,, \tag{3.22}$$

where p_i = Probability of occurrence of data in an input word space.

Since $$P_I = 1 - P_{(j=o)} \,, \tag{3.23}$$

then $$P_I = 1 - (1 - p_i)^S, \tag{3.24}$$

$$= Sp_i - S(S - 1)p_i^2 + \ldots\ldots \tag{3.25}$$

Since a random input process has been assumed, then p_i can be evaluated using the expression

$$p_i = \frac{\text{mean number of inputs during T}}{\text{maximum number of inputs during T}} \,, \tag{3.26}$$

$$= \lambda T/S \tag{3.27}$$

This expression is valid for T/S small and is applicable here since the recirculating rate will be much higher than the output rate. Substituting for p_i in Equation 3.25, we get,

$$P_I = \lambda T - (S - 1)(\lambda T)^2/2S + \ldots\ldots \tag{3.28}$$

For $\lambda T \ll 1$, we can ignore all but the first term on the right-hand side of Equation 3.28. Since we do not propose to consider cases

for $\lambda T > 1$, we therefore use the approximation,

$$P_I = \lambda T, \quad \lambda T < 1 \tag{3.29}$$

3.6.2.1 Distribution of data in the recirculating train

The distribution of data shifted out of the store will be difficult to analyse due to the problems outlined in the previous section. However, if we assume randomness of data in the recirculating train and use a technique similar to that employed for obtaining P_I we can obtain an expression for P_R.

In order to calculate P_R , we examine the mean number of words shifted out during T. If E(n) represents this mean, then the mean number recirculated would be given by $R_s E(n)$, where R_s is the probability of overflow of the s-stage output buffer. We define a probability p_r which is the probability of finding a word in a recirculating word space. Using Equation 3.26 we can write,

$$P_r = E(n)R_s/S \; ; \tag{3.30}$$

subject to the same restrictions as before.

Hence we arrive at the expression for P_R ;

$$P_R = E(n)R_s \; , \tag{3.31}$$

We can therefore write for P_C ,

$$P_C = \lambda TE(n)R_s \; . \tag{3.32}$$

Hence we will take as the probability of coincidence for an N-stage register, with a single input buffer, s-output registers and a system traffic intensity p, the expression,

$$P_C = pE(n)R_s \; , \tag{3.33}$$

3.6.2.2 Derivation of E(n) and R_s

The values of E(n) will depend on the relationship between the recirculating rate and the store size. Now depending on the recirculating rate, the time T may be less than, equal to, or greater than the major cycle of the store. The major cycle or recirculation time is given by the expression,

$$t_r = wNt_s \tag{3.34}$$

for a w-bit word. If T is greater than t_r, then during the output period all N possible words in store can be shifted out. If T is less than t_r, then only S of the N possible words in store can be shifted out. We therefore have to treat these two cases separately.

3.6.2.3 Case 1: $S \geq N$

This means that the ratio S:N is such that the data in store may be recirculated several times during the output interval. Now S may or may not be an integral multiple of N, hence we can write

$$S = (j - 1 + z)\, N \tag{3.35}$$

where $j = 1, 2, 3, \ldots\ldots$, and z can take on values from 0 to 1. If S is an integral multiple of N then $z = 1$. In any case we examine the system every T/j seconds; hence, after the first interval we can write

$$n_1 = r/j + (1 - P_I)\, n_o R_s \tag{3.36}$$

where n_1 represents the number in store at the end of the first interval, r new words are generated during T, hence r/j are fed into store, n_o words were in store at the end of the previous interval hence $n_o R_s$

words are recirculated. Only $(1 - P_I)$ of these can be accepted, hence the expression for n_1. We can continue this procedure over successive intervals; however, if we assume that statistical equilibrium exists then we can write

$$E(n_2) = E(n_1) = E(n_o) = E(n_j) \tag{3.37}$$

If we return to Equation 3.36 and take the expected value of both sides of the equation then we can write

$$E(n_j) = E(r)/j + (1 - P_I)E(n_j)R_s \tag{3.38}$$

But from Equation 3.33 we can write

$$E(n_j)R_s = P_C/jp \tag{3.39}$$

Hence Equation 3.38 becomes

$$E(n_j) = p/j + (1 - P_I)P_C/jp \tag{3.40}$$

$$= p/j + (1 - p)P_C/jp \tag{3.41}$$

since $P_I = p$

$$E(n_j) = \frac{p^2 + (1 - p)P_C}{jp} \tag{3.42}$$

Now Equation 3.42 gives the mean number shifted out after one of $j + z - 1$ possible intervals. Hence to find the total number shifted out during the time T, we write

$$E(n) = \left(\frac{j + z - 1}{j}\right) \frac{p^2 + (1 - p)P_C}{p} \tag{3.43}$$

Hence if $z = 1$, and $S = jN$ and

$$E(n) = \frac{p^2 + (1 - p)P_C}{p} \tag{3.44}$$

3.6.2.4 Case 2: $S < N$

This means that only S of the N possible words in store can be shifted out during time T. A similar treatment can be undertaken by expressing N in terms of S by the expression

$$N = (j + z - 1)S \tag{3.45}$$

where j and z have the same values as before.

If we examine the system after every T seconds, then we can write for n_1,

$$n_1 = r + (1 - P_I)n_o R_s + gn_o + (z - 1)n_o \tag{3.46}$$

where n_1 = number in store at time t + T

r = number of new words generated in time T

n_o = number of words in S word spaces at time t.

The extra factors gn_o and $(z - 1)n_o$ account for those words which suffer shifts within the store but are not shifted out. The factor g is given by the expression

$$g = j - 1 \tag{3.47}$$

Figure 3.4 shows diagrammatically the word arrangement for this case.

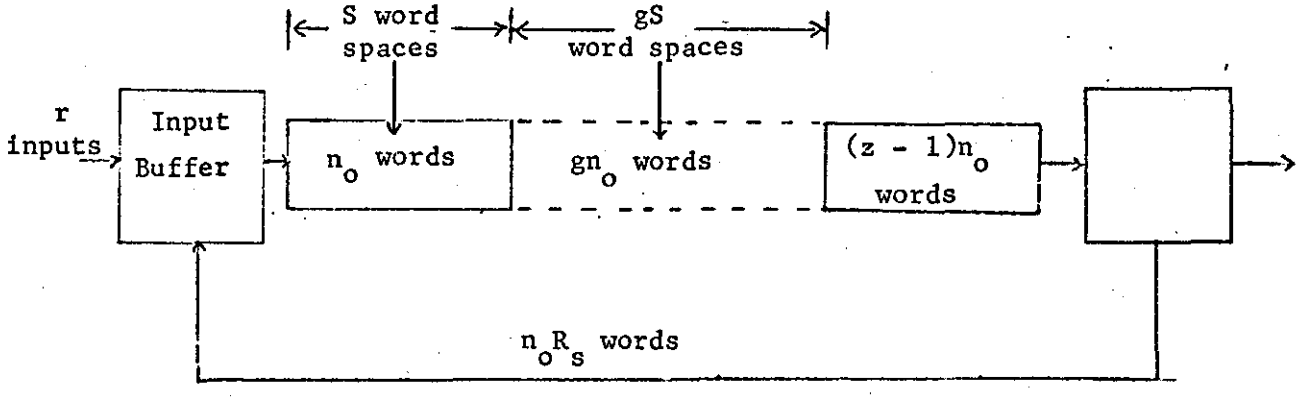


Figure 3.4: Distribution of data in store for $S < N$ $(z \neq 1)$

If we again assume that equilibrium exists then by taking the expected value of both sides of Equation 3.46 we can write

$$E(n_j) = E(r) + (1 - P_I)E(n_j')R_s + gE(n_j') + (z - 1)E(n_j'), \quad (3.48)$$

where $E(n_j)$ = mean number in store after any shift,

and $E(n_j')$ = mean number in any S word spaces.

Now the number shifted into the first S word spaces represents the mean value of n_j' when equilibrium exists. Hence we can write,

$$E(n_j') = E(r) + (1 - P_I)E(n_j')R_s \quad (3.49)$$

and from Equation 3.48 we obtain

$$E(n_j) = (g + z)(E(r) + (1-P_I)E(n_j')R_s) \ , \quad (3.50)$$

$$= (g + z)\ (p + (1 - p)P_C/p) \ , \quad (3.51)$$

since $E(n_j')R_s = P_C/p$, $E(r) = p$ and $P_I = p$.

Also since $g = j - 1$, Equation 3.51 becomes

$$E(n_j) = (j + z - 1)\frac{(p^2 + (1 - p)P_C)}{p} \quad (3.52)$$

This expression is for the mean number in store after each T second interval. To find the mean number shifted out of store, we take a fraction $1/j$ of this. Therefore we can now write for E(n),

$$E(n) = \frac{(j + z - 1)}{j}\frac{(p^2 + (1 - p)P_C)}{p} \quad (3.53)$$

This equation is identical to Equation 3.47

3.6.2.5 Derivation of probability of overflow

In order to calculate the probability of overflow, use is made of some of the expressions derived in Section 3.5.3. Equation 3.13 gives as the probability of not removing a word the expression,

$$1 - p(1 - R_N).$$

In this situation the probability of not removing a word from the output buffer is,

$$1 - E(n)\ (1 - R_s) \tag{3.54}$$

since E(n) represents the traffic intensity of the output buffer. Again this condition exists only if the store is empty just before service begins. Hence

$$P(0) = 1 - E(n)\ (1 - R_s) \tag{3.55}$$

$$\text{or } R_s = \frac{P(0) + E(n) - 1}{E(n)} \tag{3.56}$$

We can therefore write the complete expression for P_C as,

$$P_C = pE(n)R_s$$

$$= p\{P(0) + E(n) - 1\} \tag{3.57}$$

Equation 3.57 gives the probability of coincidence for s output registers. To find the value for a particular case we need to find that particular value of P(0).

3.6.2.6 Single output register

From Section 3.5.3 we make use of Equations 3.7 and 3.8 and write,

$$P(s + 1) = 0 \tag{3.58}$$

and

$$\sum_{i=o}^{s} P(i) = 1 \tag{3.59}$$

If the output buffer consists of one register then s = 1 and Equation 3.59 becomes

$$P(0) + P(1) = 1 \tag{3.60}$$

Also if we examine this register at the beginning of every output interval then we can write for P(0),

$$P(0) = P(0)k(0) + P(1)k(0) \tag{3.61}$$

where k(n) gives the probability of n arrivals during the previous interval. Substituting for P(1) in Equation 3.61, we get

$$\begin{aligned} P(0) &= P(0)k(0) + k(0)(1 - P(0)) \\ &= k(0) \end{aligned} \tag{3.62}$$

Hence, for a single output register P(0) is simply the probability that no words entered during the previous interval.

Having assumed that the occurrence of data from the main store represents independent events, then the distribution of data follows a Binomial distribution. This is due to the synchronous nature of the system. Hence

$$k(i) = {}^{S}C_{i} B^{i} (1 - B)^{S-i} \tag{3.63}$$

where B = probability of occurrence of data in a word space. The

probability of occurrence of data in a word space can be evaluated by using the relationship,

$$B = \frac{\text{Fraction of time during which data occur}}{\text{Total time}}$$

$$= \frac{E(n).w.t_s}{T}$$

$$= E(n)/S \qquad (3.64)$$

since $S = T/wt_s$.

$$\text{Hence } k(0) = (1 - E(n)/S)^S , \qquad (3.65)$$

$$\text{or} \quad k(0) = 1 - E(n) + \frac{S(S-1)}{2S^2} E(n)^2 - \ldots\ldots \qquad (3.66)$$

For large values of S this expression would be difficult to simplify; however, by making approximations a fair estimate can be obtained. Thus Equation 3.57 becomes,

$$P_C = \rho \left\{1 - E(n) + \frac{S-1}{2S} E(n)^2 + E(n) - 1\right\} \qquad (3.67)$$

$$= \rho\left(\frac{S-1}{2S}\right). E(n)^2 \qquad (3.68)$$

3.6.2.7. Results for a single output register

Using the approximate relationship of Equation 3.68, values for P_C are computed for various values of ρ, S and N. Figure 3.5 shows a plot of P_C against N for several values of ρ and a fixed value of S.

The first point of interest is the "beat-effect" which occurs between S and N. When S = jN and N = jS the value of P_C increases above neighbouring values. This is due to Equations 3.44 and 3.53 being identical for z = 1. The physical explanation for this

phenomenon could be due to the fact that at these points the maximum number of words are shifted out of store. This therefore increases the probability of coincidence between the two data trains. Figure 3.6 shows a plot of E(n) against ρ, and Figure 3.7 a plot of P_C against S for a fixed value of N and for $\rho = 0.5$.

Due to the unique nature of this queueing system and due to the simplifying assumptions made, a direct comparison between this system and the step-down storage system is not feasible at this stage. However, it is apparent that even for large values of S and parameters away from the "beat-point", the losses in this system are much higher than for the previoius system. For example, for $\rho = 0.5$ and a store size of 10, the step-down system has a value of R_N of about 3×10^{-6}, while a low value of P_C is of the order of 3×10^{-1}. There is also a marked difference in the sensitivities of the systems to changes in traffic intensity. For the recirculating system a change in ρ from 0.5 to 0.9 results in a tenfold increase in P_C, while the corresponding change in the step-down system produces an increase in R_N of 10^4. This apparent insensitivity of the recirculating store tends to support the original assumption that this storage system would be self-adaptive. This suggests that should there be a data burst from the input source the average losses would not deviate extensively from the design values.

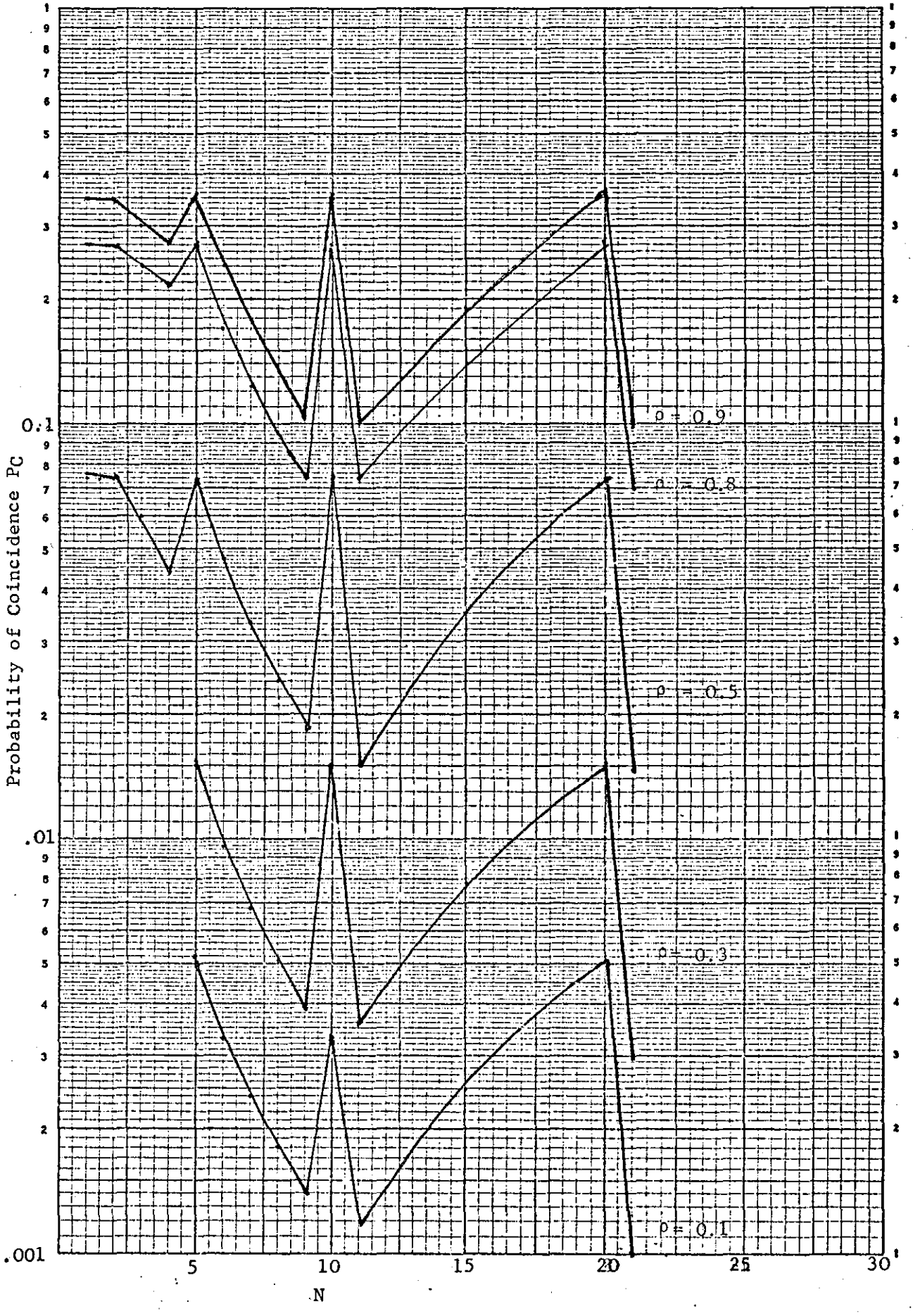


Figure 3.5: Fractional loss for a single register recirculating store with Poisson input.

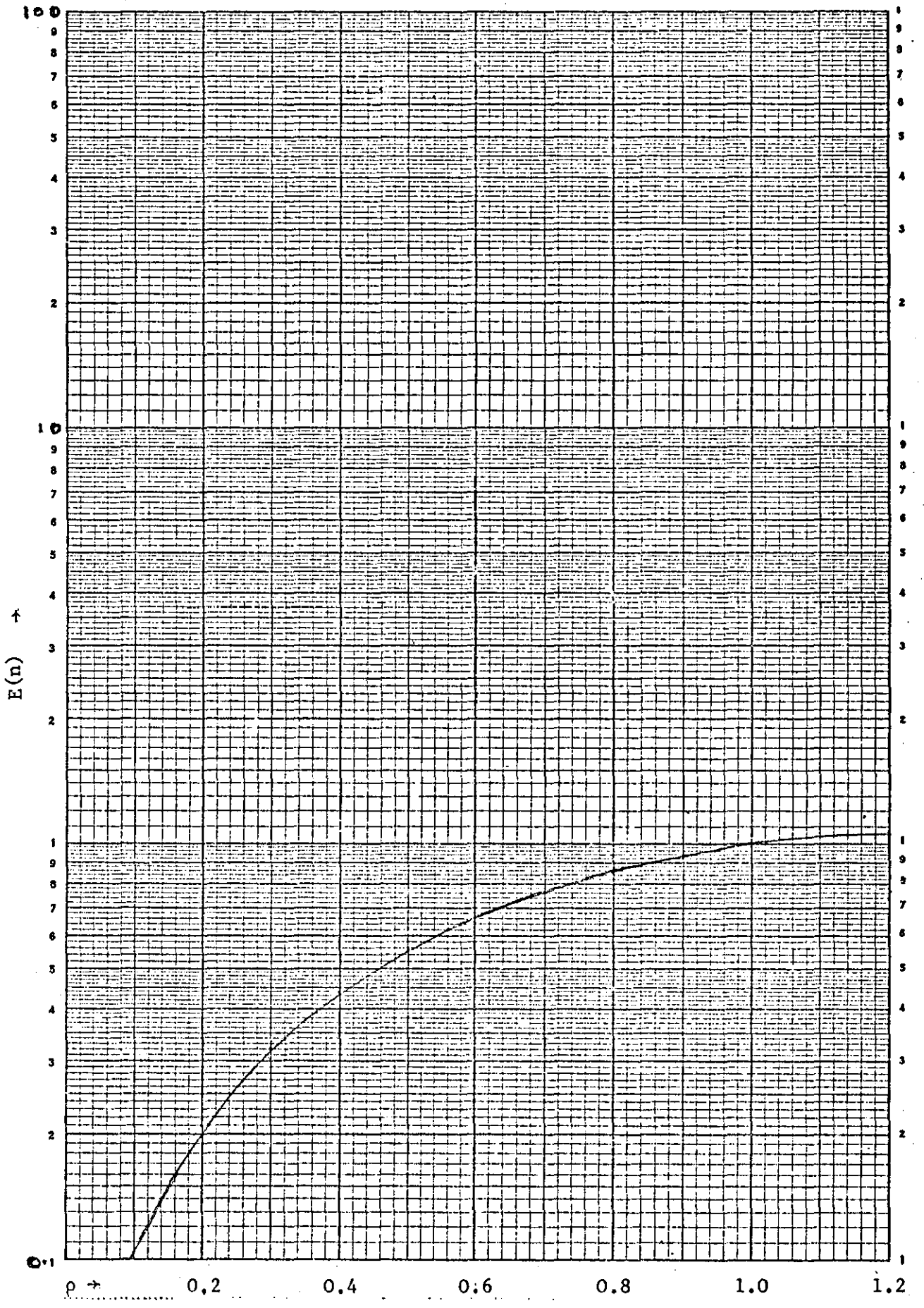


Figure 3.6: E(n) vs ρ for recirculation store

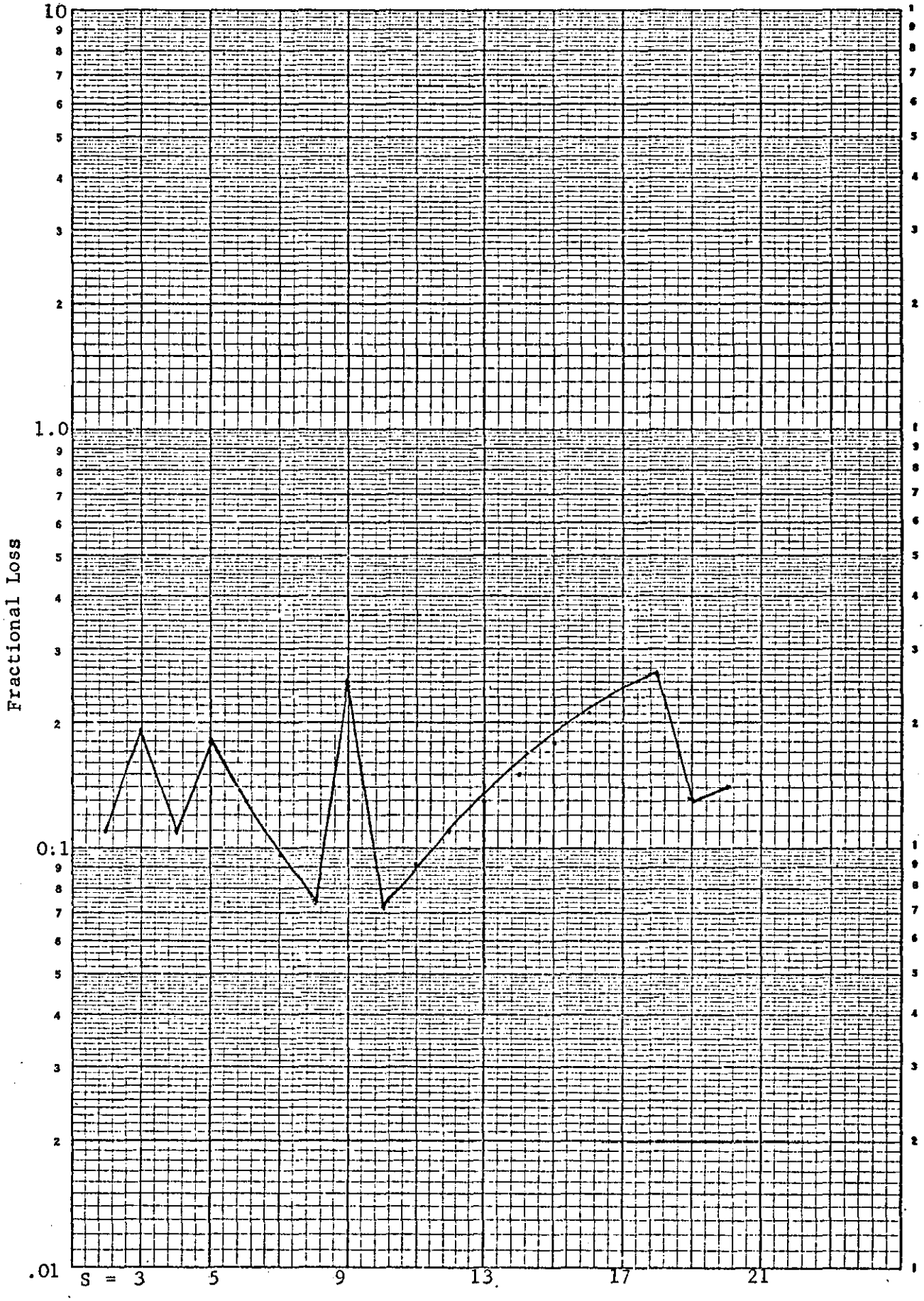


Figure 3.7: Variation of fractional loss with recirculating rate
($\rho = 0.8$, $N = 9$)

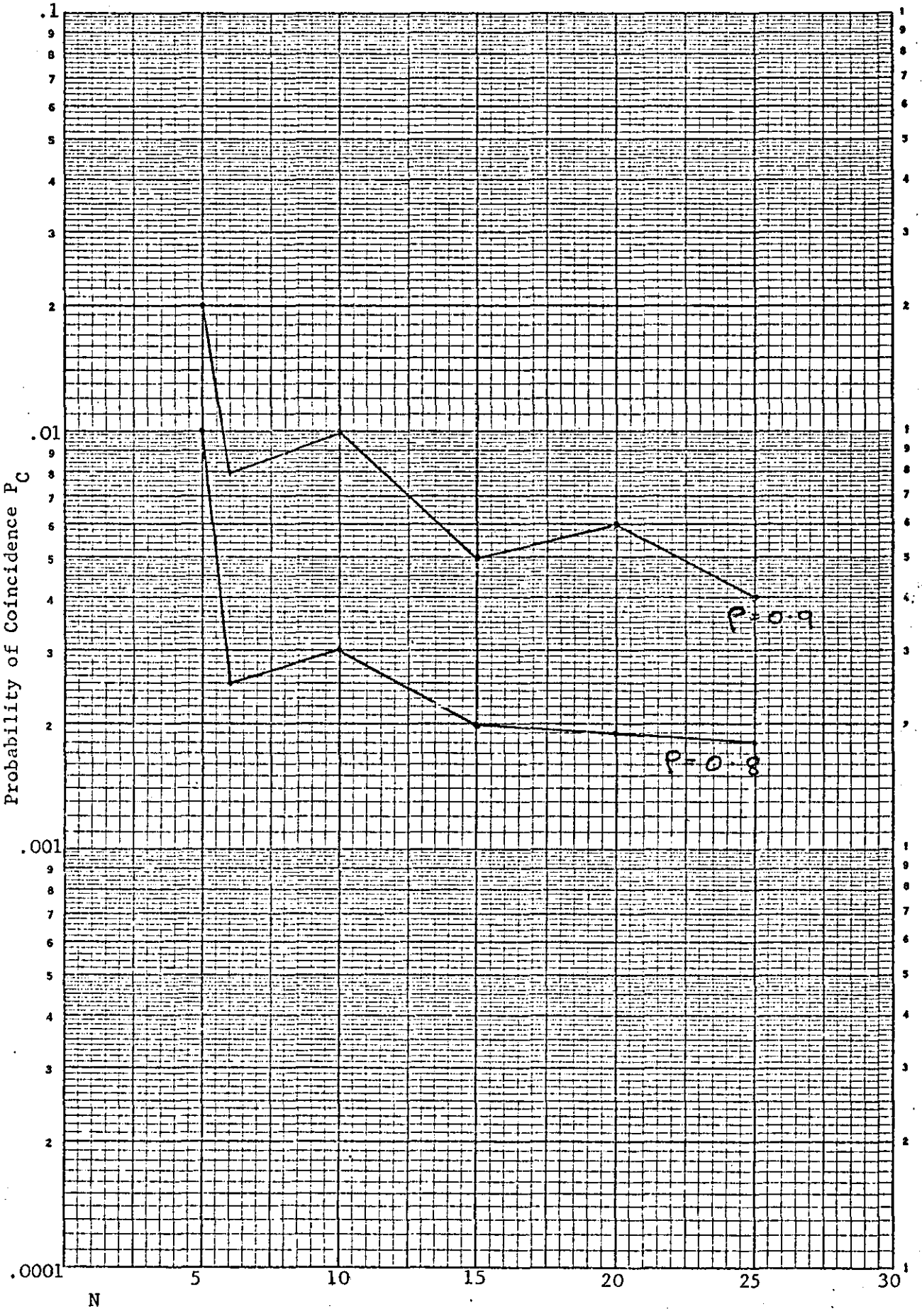


Figure 3.8: Variation of fractional loss for 2 Registers with Poisson input.

3.6.2.8 Coincidence losses with two output registers

In order to evaluate P_C for two output registers we need to calculate P(0) for s = 2. Equation 3.59 then becomes

$$P(0) + P(1) + P(2) = 1 \tag{3.69}$$

Also if we put n = 1 in Equation 3.6, we get

$$P(1) = \{P(0) + P(1)\, k(1) + P(2)k(0)\} \tag{3.70}$$

Along with Equation 3.61 which states

$$P(0) = P(0)k(0) + P(1)k(0)$$

we can obtain an expression for P(0). Hence we can write

$$P(0) = \frac{k(0)^2}{1-k(1)} \tag{3.71}$$

where k(1) = probability of one input to the output buffer during T.

$$\text{Now } k(1) = {}^{S}C_1 \frac{E(n)}{S} \left\{ 1 - \frac{E(n)}{S} \right\}^{S-1} \tag{3.72}$$

$$= E(n) \left\{ 1 - \frac{E(n)}{S} \right\}^{S-1} \tag{3.73}$$

P_C then becomes,

$$P_C = P\left\{ \frac{k(0)^2}{1-k(1)} + E(n) - 1 \right\} \tag{3.74}$$

By substituting for k(0) and k(1) and making similar approximations, estimates of P_C can be obtained.

Figure 3.8 shows a plot of P_C against N for several values of p and for S fixed. The "beat-effect" is again present, however, there is now a greater dependence on store size as there is a gradual decrease

in P_C as N is increased. There is now a favourable comparison between this system and the step-down system. For $p = 0.9$ and $N = 10$, P_C is about 10^{-2} while R_N is also approximately 10^{-2}. However, R_N is again more sensitive to variations in N and p.

3.6.3 Discussion of Results

The preceding analysis suggests that this type of storage is at least as good as the parallel entry type. Owing to the assumption of independence of events at the output of the recirculating store the results presented can only be used to gain an insight into the performance of the system.

It seems obvious that further improvement is possible as the number of output registers is increased. From the trend of the decrease a maximum of three registers would be sufficient for our purposes. The calculations then become laborious, hence no value of P_C for $s = 3$ have been computed.

The "beat-effect" which has been uncovered appears to be inherent in the system. However, the effect is less noticeable for $s = 2$. The cyclic nature of the system could be the main contributor to this effect, hence at the beat points the system would effectively be in the same state at the end of every output period. The effect of increasing the store size or recirculating rate is therefore negated. By increasing the number of output registers the cycle would be disturbed thus resulting in a decrease in the "beat-effect".

Also, this analysis does not distinguish between coincidence and overflow losses. The simulation experiments to be discussed in Chapter 4 examine this aspect of the system as well as simulating the three output register system.

REFERENCES: CHAPTER 3

1. Medlin J.: "Buffer Length requirements for a Telemetry Data Compression System".
National Telemetering Conference Report, pp 1-9, 1962.

2. Cherry E.C., Kubba M.H., Pearson D.E. and Barton M.P.: "An Experimental Study of the Possible Bandwidth Compression of Visual Image Signals".
Proceedings of the I.E.E.E., Vol 51, pp 1507-1517, November 1963.

3. Bussard D.L. and Wilmot R.D.: "Queueing Requirements in an Automatic Radar Target Detection System Operating with a Narrow Bandwidth Link.
I.E.E.E. Trans. on Systems Science and Cybernetics, Vol SSC-6, No 2, pp 81-91, April 1970.

4. Barrett C.J.: "Bandwidth Compression by Utilising the Redundancy in Sonar Displays".
M.Sc. Thesis, University of Birmingham, September 1965.

5. Davies R.A.: "Simulation of a Bandwidth Compression Queueing System using a Recirculating Store".
Departmental Memo No. 51, Department of Electronic and Electrical Engineering, Loughborough University of Technology, February, 1971.

6. Goode H.H. and Machol R.E.: "Systems Engineering".
McGraw-Hill Book Company.

7. Prabhu N.U.: "Queues and Inventories".
New York, Wiley, 1965.

8. Dor N.M.: "Guide to the Length of Buffer Storage required for Random (Poisson) Input and Constant Output Rates".
I.E.E.E. Transactions on Electronic Computers, Vol 16, pp 683-684, October 1967.

9. Schwarz G.R.: "Buffer Design for Data Compression Systems".
I.E.E.E. Transactions on Communication Technology, Vol COM-16, No.4, pp 606-615, August 1968.

10. Philokyprou G., and Tzafestas S.: "Buffer-Size and Waiting-Time Calculations for Random Arrivals and Periodically Regular Service".
Electronics Letters, Vol. 6, No. 18, pp 588-590, September 1970.

11. Stein S. and Johansen D.: "A Statistical Description of Coincidences among Random Pulse Trains".
Proceedings of the I.R.E., 1958.

CHAPTER 4

SIMULATIONS

4.1 Introduction

The analysis undertaken in Chapter 3 suggests that a recirculating store with multiple output registers and a single input register would produce results comparable to the random access store. The analysis, although general in form, becomes laborious as the number of output buffers is increased. No recursive relationship could be found between succeeding values hence approximate results were produced.

However, by generating Poisson distributed numbers it is possible to simulate the entire system on a digital computer; by suitable programming the parameters of the system can be easily changed. Simulation runs would also be able to distinguish between overflow and coincidence losses.

In addition, a Poisson distributed data source has been used throughout the analysis. However, the nature of the target distributions encountered on fish detecting sonar displays suggests a more complex distribution. It is doubtful whether these distributions would conform to any of the known random distributions hence it was decided to generate on the computer synthetic displays resembling the real situation. A more realistic appraisal can then be made, also a better comparison between the two storage systems.

Finally, in Chapter 2 it was suggested that due to the normal

shoal formations of fish behaviour, the information from the display would lend itself readily to some form of run-length coding. It is proposed therefore to test the effectiveness of some simple run-length coding schemes. The codes proposed are fixed length binary codes with the maximum run-length being chosen after examining the simulation results. It is appreciated that more efficient coding would be possible with the use of variable length codes. However, due to the lack of sufficient knowledge of the information source, and since the eventual aim of the project is to produce an experimental model it was decided to test the system by using the simpler approach.

4.2 Monte Carlo Simulations

The simulation models to be developed will be based on the Monte Carlo approach[1,2,3]. This branch of experimental mathematics is concerned with experiments whose behaviour is controlled by random numbers. Problems handled by Monte Carlo methods are of two types called probabilistic or deterministic according to whether or not they are directly concerned with the behaviour and outcome of random processes. In the case of a probabilistic problem the simplest Monte Carlo approach is to observe the behaviour of random numbers; these numbers are chosen in such a way that they directly simulate the physical processes of the original problem. The desired solution can then be inferred from the results of the simulations. The application of Monte Carlo methods to deterministic problems involves those problems which can be formulated in theoretical language but cannot be solved by theoretical means. Being deterministic, these problems

have no direct association with random processes, but when the theory has exposed its underlying structure, it may be recognised that the expressions derived also describe some apparently unrelated random process. Hence Monte Carlo simulation methods can be used to solve such problems.

Queueing systems fall within the first category. The source and service mechanisms in general follow some random process; hence the appropriate random numbers are used to control these two aspects of the system. For our purposes the situation is simple as our holding times are non-distributed. With the recirculating store the randomness of the coincidence phenomenon is self-generating and no externally generated numbers are necessary.

It should be appreciated that simulation models can only result in inferences and exact solutions to problems are not possible. This constitutes one disadvantage of simulating low probability events, since it is the nature of probability that very large numbers of simulation runs must be made if any confidence is to be put in the resulting small probabilities. The number of runs required to produce a result within a specified tolerance may be estimated by applying the accepted confidence-limit techniques (4, Chapter 23), (3, Chapter 11). For example, it is shown in (4) that if a certain event has probability of the order of 0.001, and we wish to determine this probability with a high confidence that the result is not in error by more than ±10%, then approximately one million runs are required. With the high cost of computer time this would be an uneconomic course of action.

Hence, in this chapter, the models developed are intended to provide a framework on which an intuitive approach can be developed concerning the basic relationship between the variables.

4.3 Generation of Random Numbers

Monte Carlo simulations require sequences of random numbers drawn from a distribution that in general is not uniform. Methods for directly generating random numbers with a particular discrete distribution are not usually available. Methods do however exist for generating random numbers with a uniform distribution. Almost all methods used for generating non-uniform distributions are based on the principle of transforming a uniformly distributed sequence of random numbers into the required sequence.

4.3.1 *Continuous Uniformly Distributed Random Numbers*

By a continuous uniform distribution we mean that the probability of a variable x falling in any interval within a certain range of values is proportional to the ratio of the interval size to the maximum range. Hence for equal intervals throughout the range the probabilities are equal.

Generation of uniformly distributed random numbers by computer is a well-documented technique[5]. The random numbers used in this simulation were generated by the University's ICL 1904A computer. The random number generator is in the form of a FUNCTION, (FUNCTION UTR1(I,J,K)) and uses the linear feedback shift register technique.

Approximately 8×10^6 numbers are generated before the sequence repeats. By setting the arguments of the FUNCTION, the random numbers can have a uniform probability distribution in the range 0 to 1.0.

4.3.2 *Generation of Poisson Distributed Random Numbers*

Poisson distributed numbers may be generated through a process of analytic inversion. In this method use is made of the relationship between the Poisson and Exponential distributions. It can be shown that if the intervals between events are exponentially distributed, then the number of events in a fixed period of time has a Poisson distribution.

Hence, in order to generate Poisson distributed numbers by the inversion method, we need to first of all generate exponentially distributed random variables.

4.3.2.1 *Generation of Exponentially Distributed Random Variables*

The exponential distribution can be generated from the uniform distribution by an inversion technique. Hence, if we require a variable x with probability density function f(x) and cumulative density function F(x), the transformation

$$r = F(x) \qquad (4.1)$$

is performed, where r is a uniformly distributed random variable such that $0 < r < 1$, and F(x) is the cumulative density function of the variate x and is defined by

$F_X(x)$ = Probability that the value X is less than or equal to x

= $Pr\{X \leq x\}$.

Now the density and cumulative density functions of exponential random variables with parameter λ are given by

$$f(x) = \exp(-\lambda x) \tag{4.2}$$

and

$$F(x) = \int_0^x \lambda \exp(-\lambda t)\,dt \tag{4.3}$$

$$= 1 - \exp(-\lambda x)$$

Hence $$\exp(-\lambda x) = 1 - F(x) \tag{4.4}$$

Now applying the transformation $r = F(x)$ we get

$$\exp(-\lambda x) = 1 - r \tag{4.5}$$

or

$$x = -\frac{1}{\lambda}\ell n(1 - r) \tag{4.6}$$

Hence to generate exponentially distributed random variables we generate a uniformly distributed random number r, between 0 and 1 and solve Equation 4.6 for x. In Equation 4.6, 1-r may be replaced by r since both are identically distributed.

4.3.2.2 *The Poisson Process Generator*

As stated in Section 4.3.2, the relationship between Poisson and Exponential random variables leads to a simple method of generating Poisson distributed numbers.

If n events occurred in time t, then the sum of the times between the n events must be less than or equal to t. Let x_i be the time between the $(i - 1)^{st}$ and the i^{th} events, $(x_o = 0)$; then

$$\sum_{i=1}^{n} x_i \leq t \tag{4.7}$$

It is known that for the Poisson process x_i is exponentially distributed with mean $1/\lambda$ for all i; hence to generate the value of n with mean λ successive values of x_i are generated until the sum of the successive values is just greater than t, that is, until

$$\sum_{i=1}^{k} x_i > t \tag{4.8}$$

Hence k-1 event occurred in time t, but the k^{th} event did not. The Poisson number n is therefore k-1.

4.3.2.3 *Poisson Generator for Queue Simulation*

The value of t for bandwidth compression queueing systems is T the output period. We therefore require the mean number of events during this time which is λT. But this is also the traffic intensity of the system since

$$\rho = \lambda T .$$

Hence, if we put $\lambda = 1$, then $T = \rho$ and Equation 4.8 becomes

$$\sum_{i=1}^{k} x_i > \rho \tag{4.9}$$

The flowchart for implementing this process is shown in Figure A.1, Appendix 2; programming was done using FORTRAN IV. The program was

designed such that values of ρ from 0.1 to 0.9 could be generated. Table 1 shows a comparison of the theoretical and simulated values for three values of ρ. The results indicate reasonable correspondence for only 1000 runs.

4.4 Generation of Synthetic Test Pattern

This pattern is intended to simulate the systems' response to a "shoal-like" input distribution. Also, since the system under study involves the human observer as part of the receiver, subjective decision making takes palce. The use of numbers to estimate data loss, although instructive would not be readily related to the actual situation.

For a sector scanning sonar with a B-scan display the relevant parameters indicate a frame rate of 5 to 10 frames per second. Integration from frame to frame due to subjective effects could easily conceal slight imperfections. In order to gain an insight into the distribution of the losses it was decided to produce the Test Pattern in a display fashion.

The Test Pattern was formed by first generating Poisson distributed numbers with a particular value of ρ. In this case $\rho = 0.96$ was used. It was decided to use 5000 runs throughout the simulations. This figure was a compromise between a long run which results in better accuracy, and a reasonable run due to the maximum computer time available. Two 120 × 186 elements array (120 columns and 186 rows) were used to hold the displays, one for the output display. Each run is allocated 5 elements along a row; when a Poisson number

TABLE 1

Comparison of Theoretical and Simulated Probabilities

Number	*Frequency*	*Simulated Probability*	*Theoretical Probability*
	$\rho = 0.1$		
0	919	0.919	0.905
1	79	0.079	0.091
2	2	0.002	0.004
	1000	1.000	1.000
	$\rho = 0.2$		
0	825	0.825	0.819
1	160	0.160	0.164
2	15	0.015	0.016
	1000	1.000	1.000
	$\rho = 0.6$		
0	564	0.564	0.549
1	313	0.313	0.329
2	100	0.100	0.099
3	21	0.021	0.020
4	2	0.002	0.003
	1000	1.000	1.000

n is generated, n asterisks (*) are placed along the line. If the number is greater than 5, the excess is carried over into the next run's space allocation. To indicate the shoal patterns, pre-selected blocks were filled in with targets. A check of the number added was made and approximately the same number of Poisson numbers were subtracted such that the total numbers on the display was the same as with Poisson numbers only. The aim is to compare the performance of the systems using Poisson inputs of a particular traffic intensity and the synthetic input of equal load factor. The load factor (L) of the system is defined as

$$L = \frac{\text{total number of inputs for } \ell \text{ runs}}{\ell}$$

According to this presentation, 24 output periods are represented along a scan line. This situation, although not pictorially realistic, does not affect the simulation process as the buffer views the input process as a sequential operation with one line continuing into the other. In addition, this presentation has the advantage of allowing one to examine the nature of the loss phenomena in the systems.

The input display was held in a subroutine DISPLAY; the flowchart for generating this process is shown in Figure A.2, Appendix 2.

4.5 Simulation of a system with a single-channel step-down store

4.5.1 *Program Structure*

This follows the conventional simulation pattern for this type of storage. The system is simulated for several values of store size. A count is made of the number of inputs generated and the number removed. An independent count is made of the overflow losses.

4.5.1.1 *Simulation using Poisson distributed numbers*

These runs are conducted to compare the results from the simulation model with the analytical results quoted in Chapter 3.

After 20,000 runs for each value of ρ and store size, results were obtained only for high values of ρ and small store sizes. This was due to the low probability of overflow for other values. Figure 4.1 shows graphically a comparison between the theoretical and simulated results. Figure A.3, Appendix 2, shows the flow-chart used for this simulation.

4.5.1.2 *Simulation using Test Pattern*

The response of this system to the Test Pattern was investigated for store sizes from 10 to 30 in steps of 5. Since each input on the input display has a unique position an encoding/decoding procedure was included in the program.

Each position is encoded in decimal form by using its row/column number; hence the first point on the display is (1,1) and is

- - - - - - - - - Simulated

_____ Theoretical

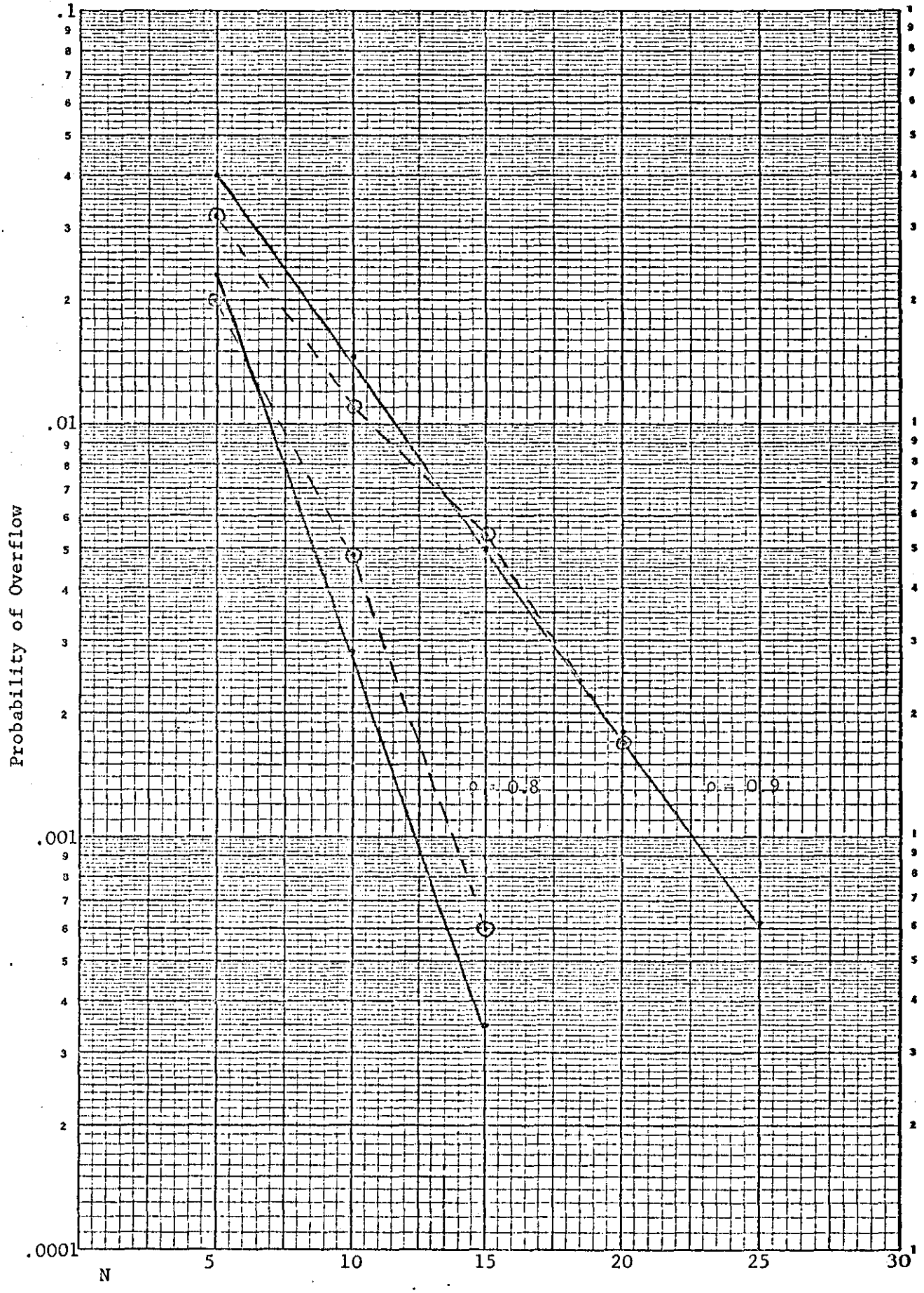


Figure 4.1: Comparison of simulated and theoretical values for overflow losses.

encoded as IN = 1001, and for the last position (186,120) IN = 186120. This number IN is then entered into the basic program. To decode, the inverse process is done and the corresponding element of the output display receives the symbol. Again a check is made of the overflow losses.

The flow-chart for simulating this system is shown in Figure A.4 Appendix 2. Figure 4.2 shows a graphical comparison of data losses between this run and the equivalent run using pure Poisson numbers. It is obvious from these results that losses are greater with the Test Pattern; for N = 10 and $\rho = 0.96$, R_N, the probability of overflow, is approximately 0.025, while for a load factor of 0.96, $R_N = 0.3$. Also, increasing the store size has only a slight effect on the losses. Figure 4.3 shows the computer print-out of the input Test Pattern and the output displays for two values of store size. The occurrence of overflow is obvious and the "one-in-one-out" situation is seen clearly especially within the data clusters.

4.6 Simulation of systems using a recirculating store

4.6.1 *Program Structure*

These systems involve an extra variable, the recirculating rate of the store. Each run, which is equivalent to an output period, is subdivided into subsidiary runs corresponding to the recirculating rate. The factor $\$_R$ which was introduced in Chapter 3 determines the number of shifts the stores undergo during each output period. The programs therefore simulate varying values of traffic intensity ρ, store

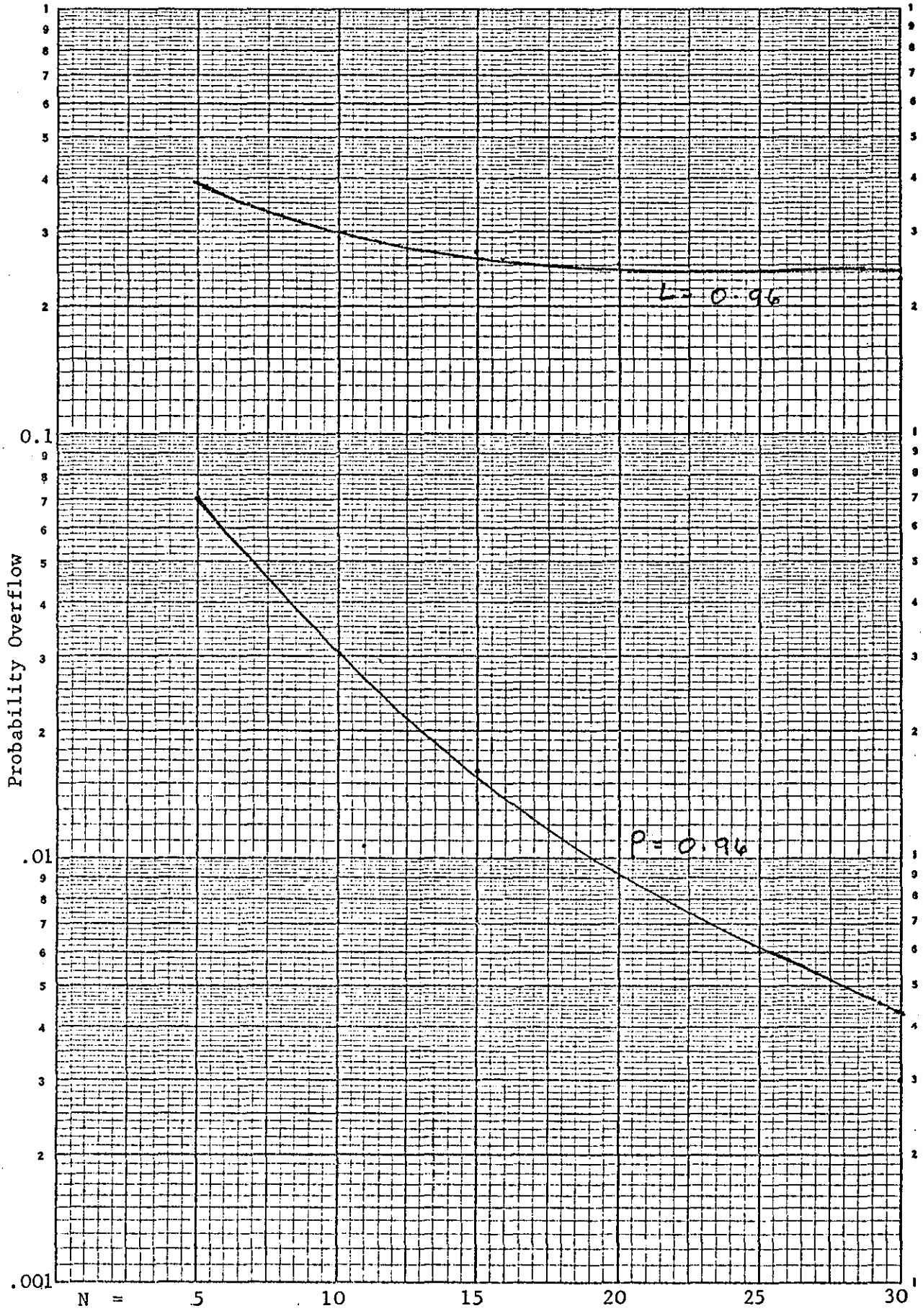


Figure 4.2: Comparison of overflow losses for Poisson and Test Pattern inputs.

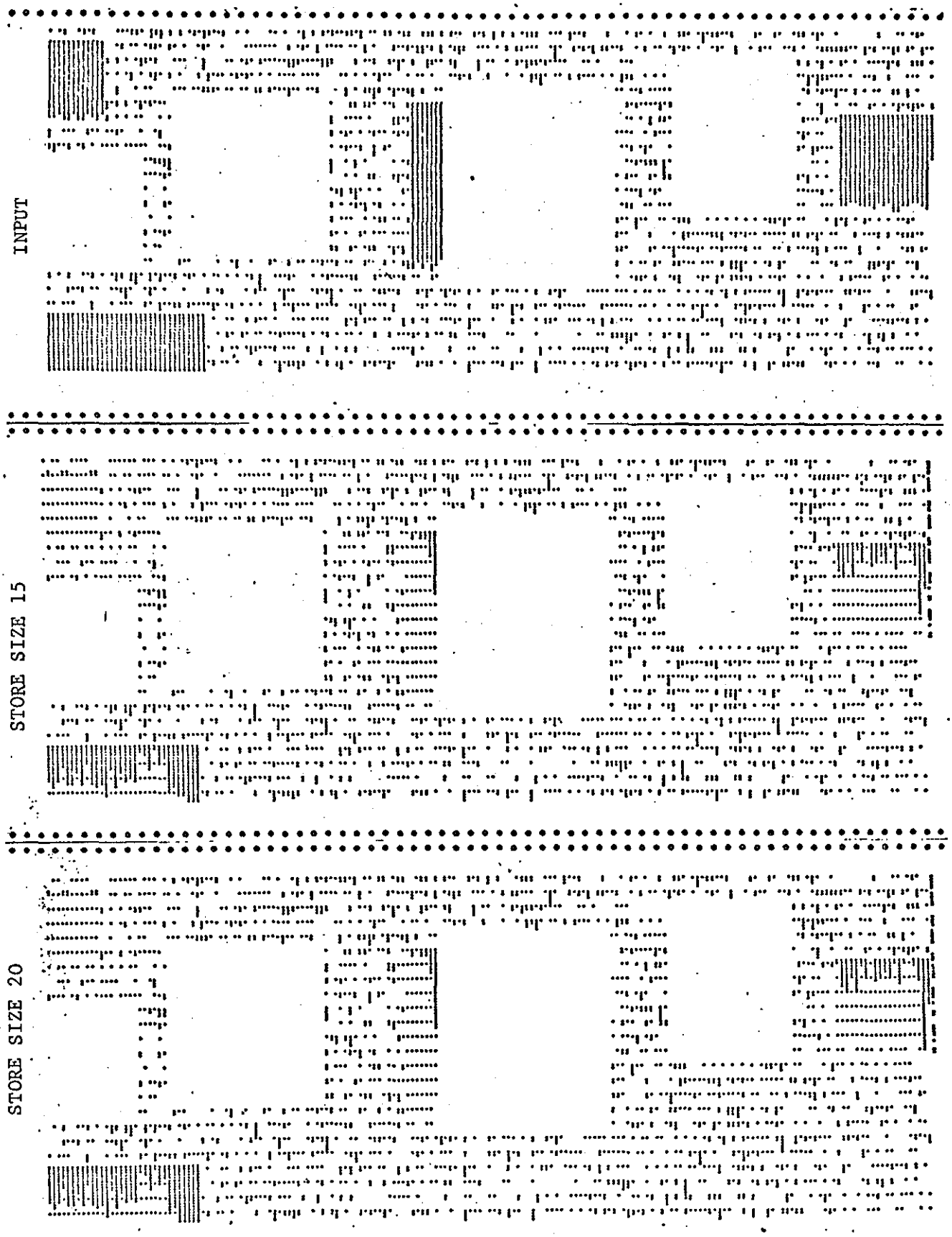


Figure 4.3 : Computer print-out of input and output patterns using step-down store.

size N, recirculation rate $\mathcal{L}_a$ as well as the number of registers. For high probability losses 5000 runs were done, but 20,000 runs were done for some low probability values.

4.6.2 *Single output register with Poisson input*

This system was analysed in some detail in Chapter 3. A check is made of the losses in the system in order to compare those due to overflow with those due to coincidence.

The flowchart for this system is shown in Figure A.5, Appendix 2.

Table 2 shows the nature of the losses with 5000 runs, for two values of ρ and varying store sizes. Figure 4.4 shows graphically a comparison between these values and the analytical values.

The main observations to be made are:

(1) There is reasonable correspondence between the theoretical and simulated values for total data loss for higher values of ρ.

(2) The "beat-effect" uncovered in the analysis again appears in all simulation runs.

(3) As expected, overflow is predominant for the lower values of store size. There is a gradual decrease in overflow losses as the store size is increased.

TABLE 2

Data losses for recirculating store with Poisson input - single output register $S_e = 10$

Store size	Number In	Number Out	Fractional Losses: Coincidence	Overflow	Total
	$\rho = 0.3$				
5	1484	1301	-	0.12	0.120
10	1510	1322	-	0.09	0.091
15	1480	1418	0.035	0.007	0.042
20	1497	1337	0.106	-	0.106
25	1475	1420	0.032	-	0.032
	$\rho = 0.9$				
5	4429	2880	-	0.346	0.346
10	4495	2991	-	0.320	0.320
15	4506	3468	0.229	-	0.229
20	4364	2960	0.126	0.194	0.320
25	4442	3462	0.220	-	0.220

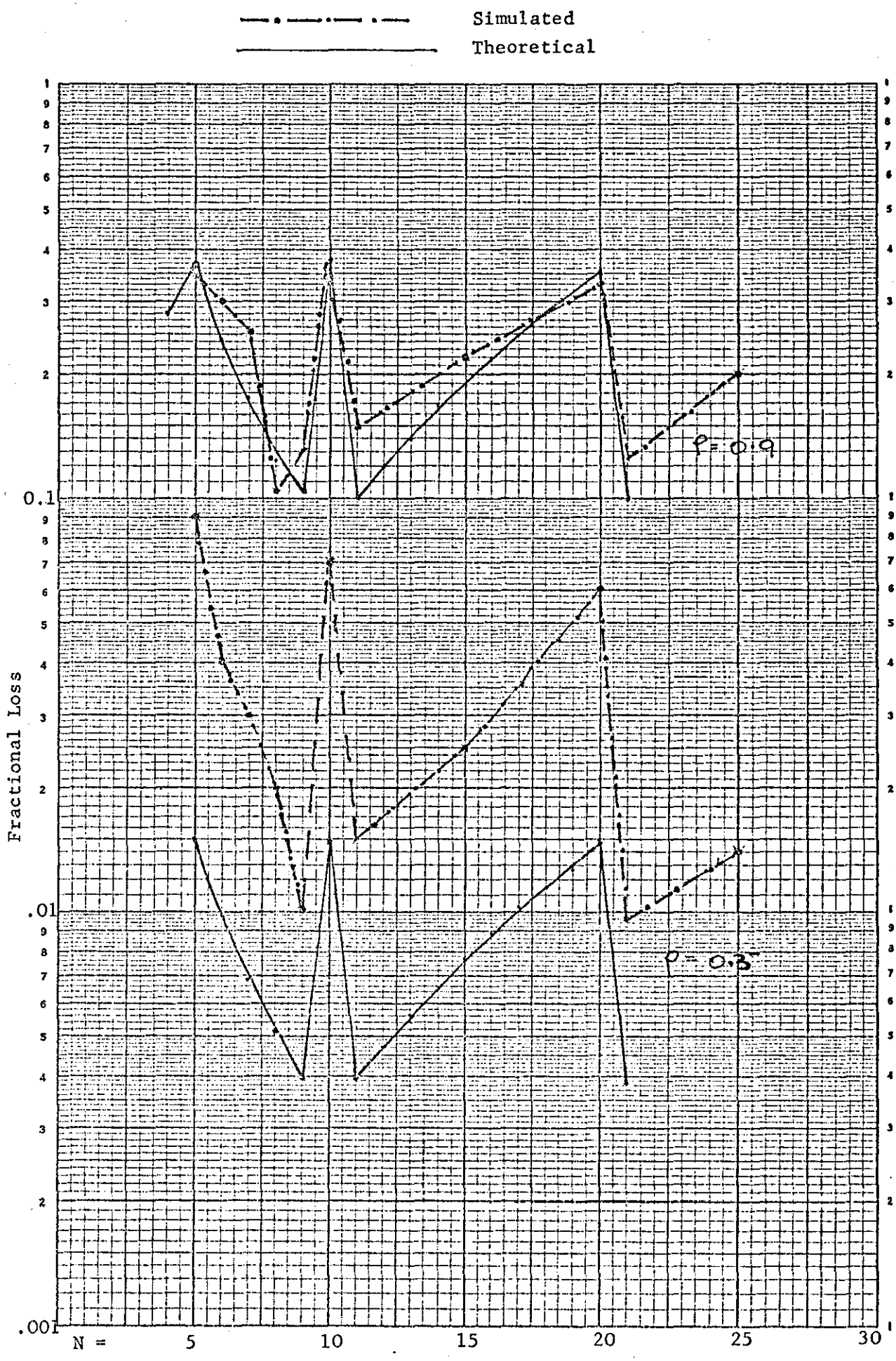


Figure 4.4: Comparison of simulated and theoretical values for Fractional loss using single register.

4.6.3 *Multiple Output Registers with Poisson Input*

The programming changes necessary only involve the recirculation and output loops of the single channel simulation.

The flow-charts of Figures A.6 and A.7, Appendix 2, show the additional programming necessary for this simulation. Simulations are done for 2 and 3 output registers. It should be noted that the effective store size is increased with the addition of the extra registers. Hence, with 2 output registers, there is an extra storage location which will have to be considered when summing overflow losses.

Figure 4.4a shows graphically a comparison of the losses for 1, 2 and 3 output registers for $\rho = 0.9$. As expected, increasing the number of registers results in a decrease in data loss. Due to the low probability of the losses, results were obtained for $\rho = 0.9$ and 0.8 only in both cases. The "beat-effect" is present but its effect appears to be diminishing as the number of output registers is increased. Figure 4.5 shows the variation of losses as the recirculation rate is varied. The system is more sensitive to the recirculation rate but again the insensitivity to increase in buffer size is apparent. With 3 output registers the system has now surpassed the random access system. For example, for $\rho = 0.9$, store size 15, and 3 output registers P_C is 0.0013, while the corresponding R_N is 0.004.

4.6.4 *Multiple Output Registers with Synthetic Input*

Simulations are done with 2 and 3 output registers and varying store sizes and recirculating rates. The encoding/decoding procedure

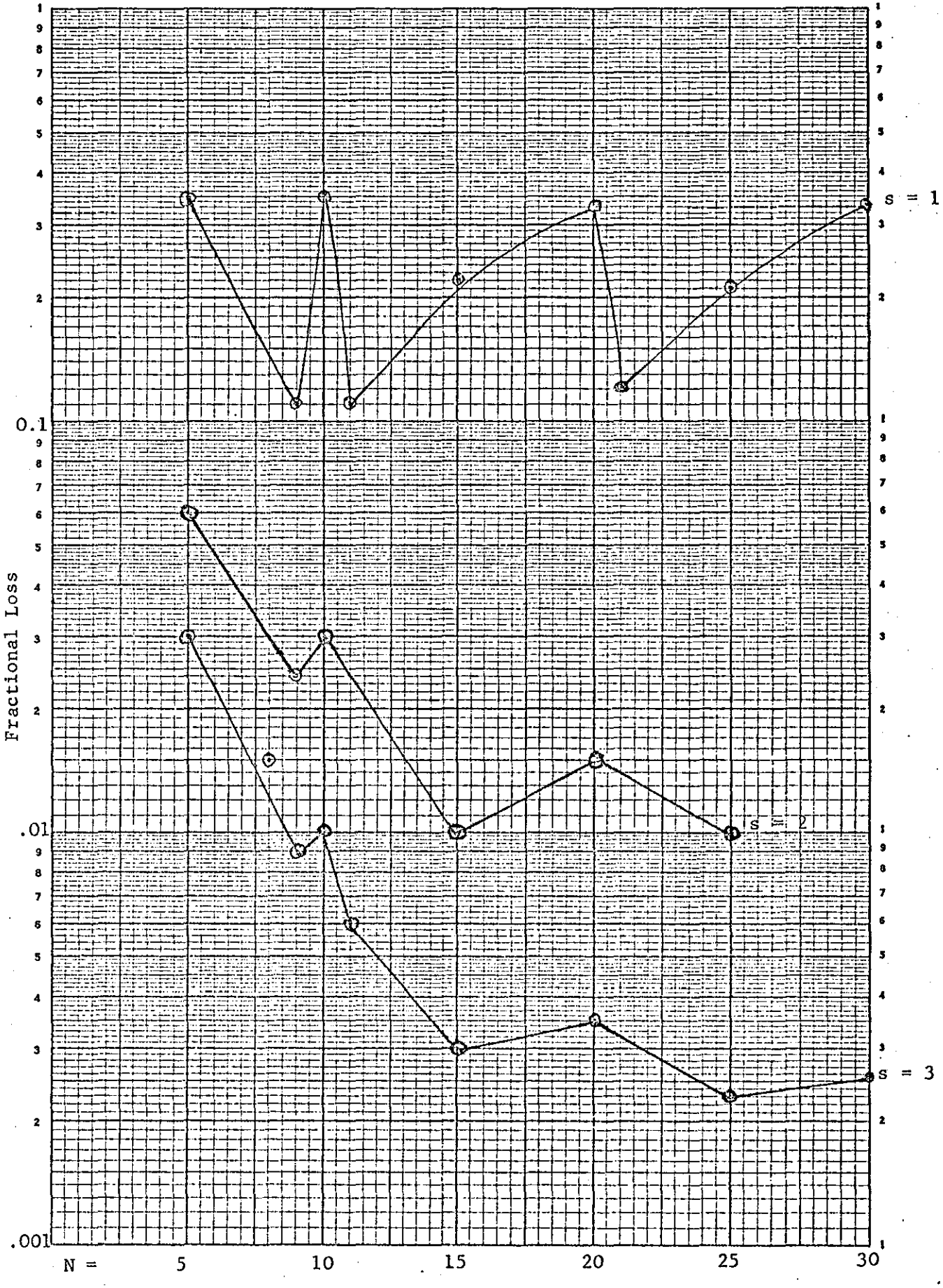


Figure 4.4a: Comparison of losses for 1, 2 and 3 registers with Poisson Input ($\rho = 0.9$)

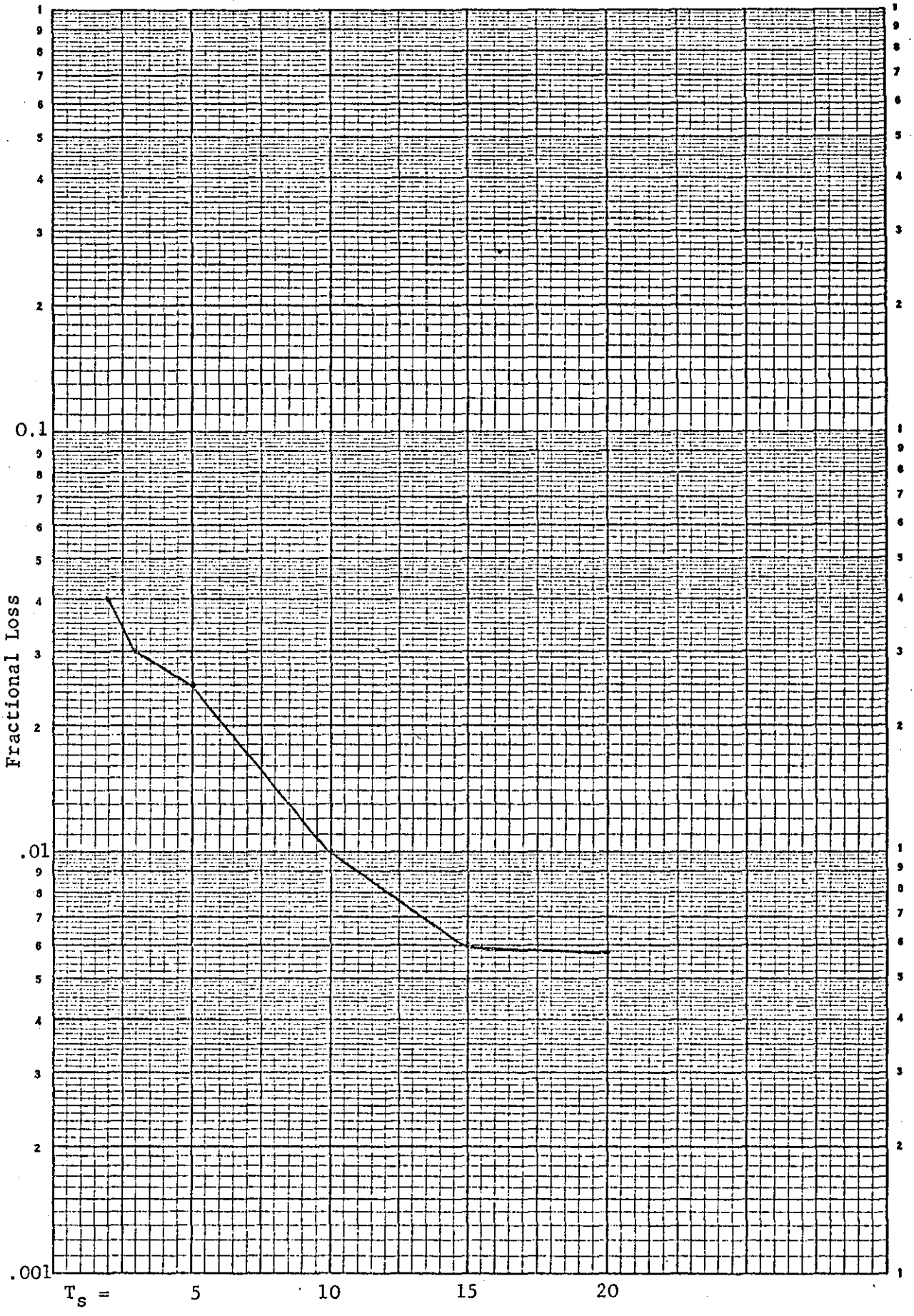


Figure 4.5: Variation of Fractional loss with S_a for 3 output registers ($P = 0.9$, $N = 10$).

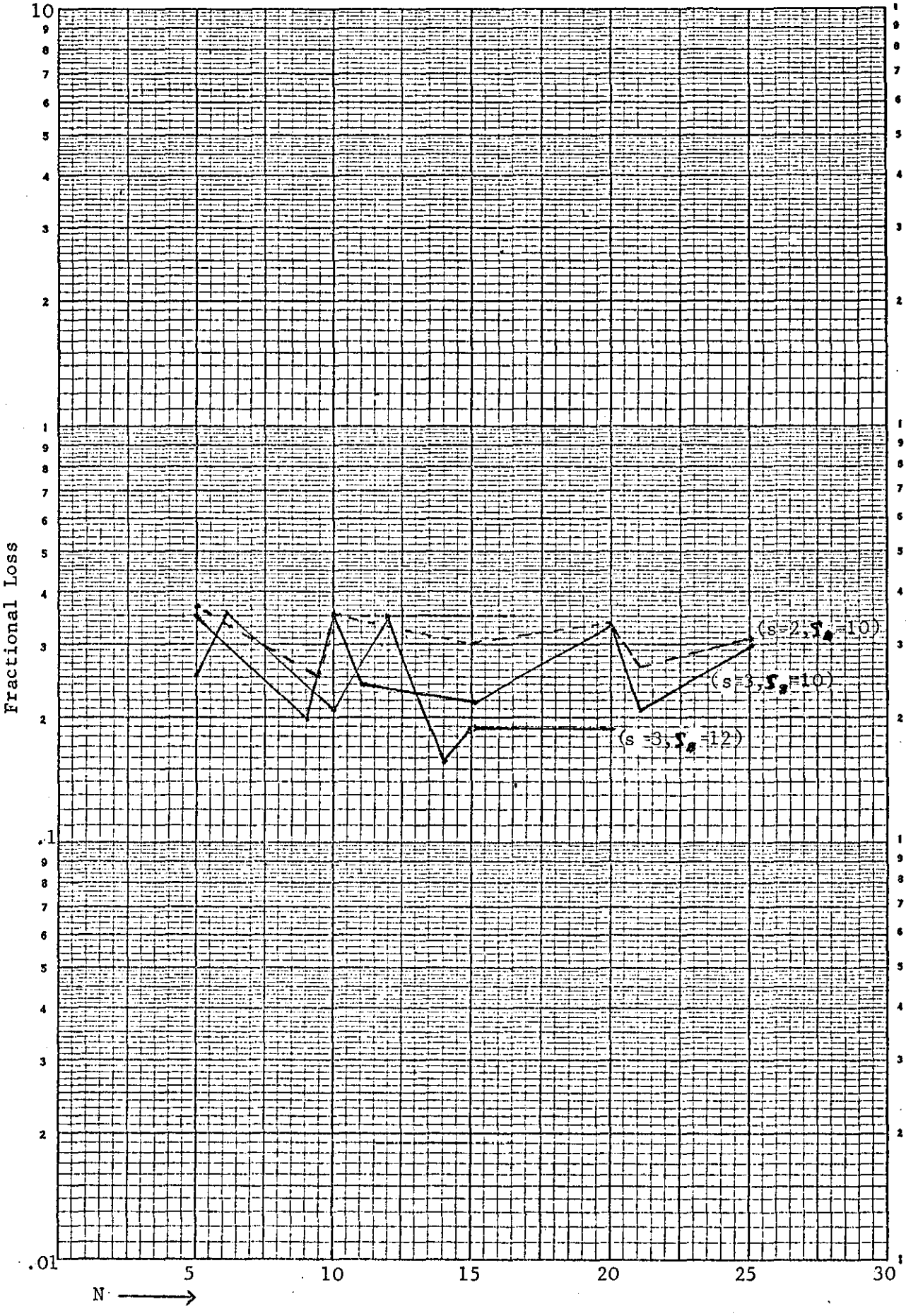


Figure 4.6: Losses for Multiple Registers with Test Pattern.

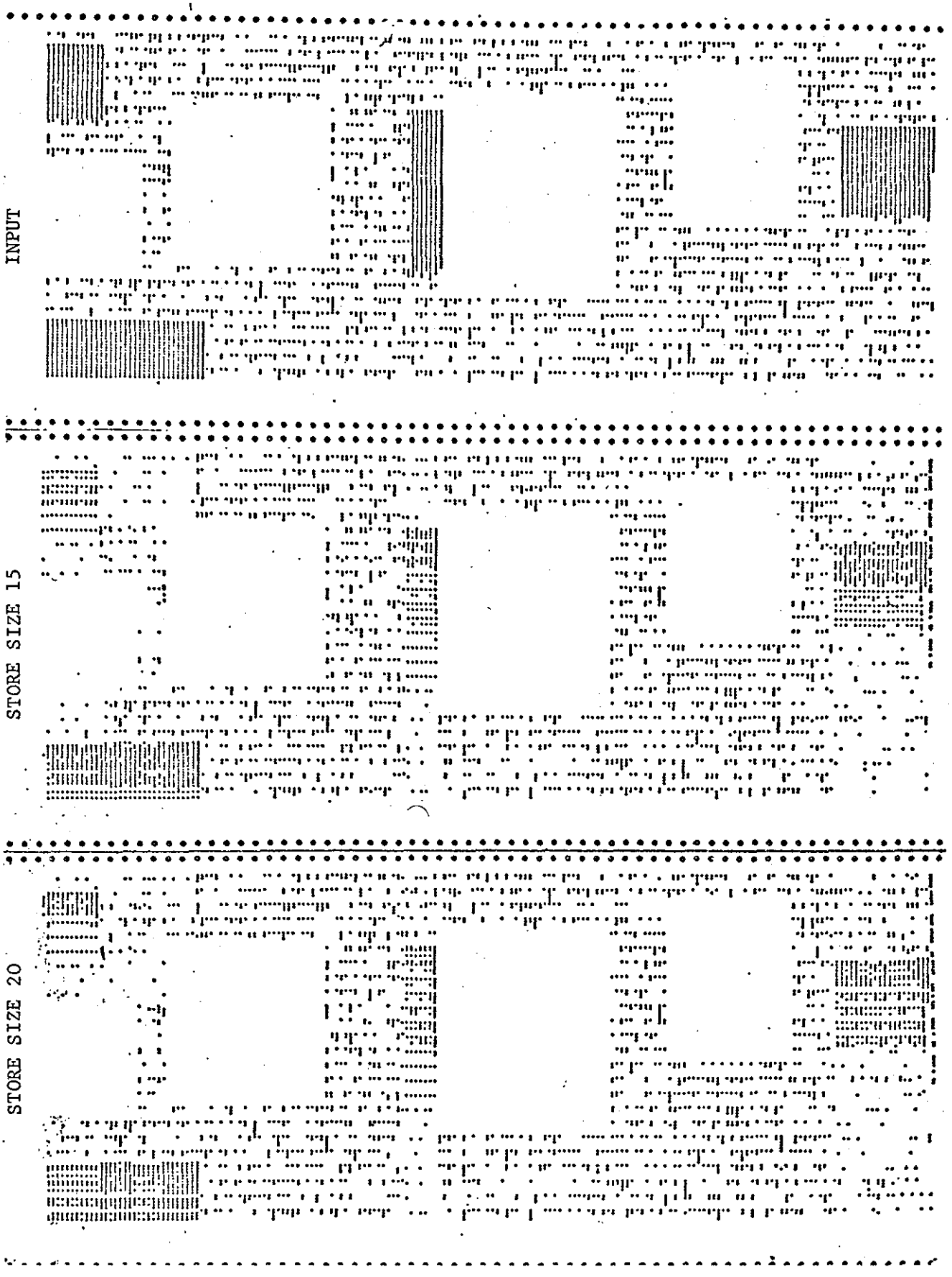


Figure 4.7: Computer print-out of input and output patterns using recirculating store - $\mathfrak{T}_{\beta}$ = 14.

is as outlined in Section 4.5.1.2 and the recirculating system is as before.

Figure 4.6 shows graphically the variation of P_C for various store sizes and recirculating rates. Figure 4.7 shows the computer print-outs of the input pattern and the outputs for two values of store size.

The main observations are:

(1) The losses are again comparable with those obtained when using the random access store. The results suggest a slight improvement with the recirculating system but with only 5000 runs little emphasis can be placed on such small variations.

(2) The nature of coincidence losses can now be observed by examining the output patterns. The effect of these losses is to distribute the losses over the whole display. On the other hand, when overflow losses occur especially in some clusters, there is the distinct "one-in-one-out" effect which the observer is better able to detect.

(3) The "beat-effect" again is noticeable.

(4) The effect of increasing the number of input registers is negligible.

4.6.5 *Comments on Simulation Results*

Due to the restriction on the number of runs, high accuracy had to be sacrificed in some cases. However, for the higher values of traffic intensity, the confidence limit calculations suggest that the results should be within acceptable limits. For example, for $p = 0.9$ the results should not be more than 5% in error; however,

for $\rho = 0.1$ they could be anything up to 50% in error. The comparison graphs of Figure 4.4 suggest close correspondence between the larger values of ρ; however, on account of the assumptions made in arriving at the theoretical curves, little emphasis can be placed on these magnitudes. However, the location of the beat-points are similar and hence the theory would appear to be reasonably acceptable, particularly for high values of ρ.

4.7 Simulation of simple Run-Length Coding Methods

The Test Patterns used in the previous simulations would not be suitable for these simulations since, in order to accommodate the required number of runs, the range cells were compressed. In the real situation there are 32 bearing cells on each bearing scan line and the coding method usually operates on a line by line basis. For a digital system it would be convenient to consider maximum runs of 2, 4, 8 or 16 cells.

4.7.1 *Preparation of Test Pattern*

The input patterns are held in 32 × 120 element arrays (32 bearing and 120 range cells). The target patterns were chosen to resemble likely situations. Two patterns were produced consisting of 305 and 662 occupied cells. These numbers were selected in order to test the coding methods over a wide range of input rates.

These patterns were prepared by Branson and the program structure is described fully elsewhere[6].

Figures 4.8 and 4.9 show the computer prints of the two input patterns.

4.7.2 *System Parameters*

In the sector-scanning sonar system proposed a minimum pulse width of 100 micro-seconds is envisaged. Hence 120 range cells would simulate a range of 20 metres. Considering the display with 305 targets per frame the mean input rate can be calculated.

Now from queueing theory fundamentals it has been shown that in order to maintain equilibrium ρ should be less than 1. For the recirculating system the analysis also suggests that a value of ρ less than one maintains better equilibrium. Also, in order to use as small a bandwidth as possible, the system designer aims for a high value of ρ.

For $\rho = 0.9$ targets have to be removed from the buffer at a rate of 340 per frame. This is equivalent to removing 1 target every 11 bearing cells, or an output clock rate of about 30 KHz. If the same removal rate is used on the 660 targets pattern, then this would be equivalent to a traffic intensity of about 1.8.

4.7.3 *Coding Methods*

Each cell on the display has a unique position and for the purposes of this simulation the encoding/decoding method outlined in Section 4.5.1.2 is used. The maximum run-lengths simulated are 4 and 8 cells. Two coding methods are simulated.

In Method 1, each range cell is subdivided into 4 or 8 runs

depending on the maximum run-length used. The number of targets within the run is counted and this number is attached to the coordinate of the last target position in the run. Hence, in binary form, each word is now 16 or 17 bits, depending on the maximum run length. This method has one drawback in that there is no indication of the distribution of targets within the run, hence a slight distortion is to be expected. However, it is hoped this effect will not be noticeable.

In Method 2 a maximum run is also selected; however, if a break in the run is encountered before the maximum is reached, the run counter stops and the run-length and last target position are encoded. This method overcomes the distortion effect of the previous method but should result in an increase in the number of runs required to encode the same number of targets.

The decoder separates the run length number from the coordinate position and simply fills in successive cells until the end of the run count.

4.7.4 *Program Structure*

The program structure is similar to those used in Section 4.5. Bearing is represented columnwise on the displays. The Test Patterns are held in SUBROUTINES and the main program reads the displays columnwise. The output period is synchronised to the bearing cells with one target being removed every k bearing cells. The value of k depends on the output rate desired. In the simulations k varied from 9 to 16 which simulates high traffic intensities. The output patterns are again displayed on computer print-outs.

The following simulations are done:

(1) Examination of the distribution of runs on the two displays for
   (a) an unlimited maximum run length,
   (b) maximum run lengths of 4 and 8 runs with coding methods 1 and 2.

(2) Comparison of the two coding methods and comparison of both coding methods with the previous un-coded method.

The flowcharts for the coding/decoding processes are shown in Figures A8, A9 and A10, Appendix 2.

Three output registers are used in all simulations.

4.7.5 *Discussion of Results*

Table 3 shows the distribution of run-lengths obtained with the two coding methods as well as for an unlimited run. The figures suggest that for these patterns a maximum of 6 to 8 runs would be adequate. There is very little difference in the number of runs for either coding method but the decrease in runs as the maximum run length is increased is noticeable. It is of interest to note that although the shapes and sizes of the targets were arbitrarily chosen, the proportions of runs remain approximately the same on both Test Patterns.

Table 4 compares the performance of the several coding methods on the 305 targets input pattern for a store size of 14 words, 3 output registers and a recirculating rate factor of 5. The first column indicates the intervals at which targets are removed. Table 5 shows the corresponding figures for the 660 targets display.

The figures indicate the vast improvement obtained with run-length coding. When using the higher input rate the fractional data loss is of the order of 50%. This figure is reduced considerably when run-length coding is used. There is very little difference quantitatively between the two coding methods; however, with an 8 run maximum better results are always obtained.

Figures 4.10 to 4.15 show the computer prints of various situations. Those for code method 1 (Figures 4.14 and 4.15) demonstrate the distortion effect mentioned before. It is interesting to note that even for the non-coded method the shapes of most of the patterns have been retained. Also, the fractional data loss for this case is of the same percentage as those encountered in the previous simulation runs.

TABLE 3

Run-Length Distribution

Run Length	305 TARGETS					662 TARGETS				
	MAXIMUM RUN-LENGTH					*MAXIMUM RUN-LENGTH*				
	Unlimited	*8*		*4*		*Unlimited*	*8*		*4*	
		Code 1	*Code 2*	*Code 1*	*Code 2*		*Code 1*	*Code 2*	*Code 1*	*Code 2*
1	44	48	48	67	54	122	77	127	150	135
2	12	12	24	42	25	20	55	23	83	40
3	13	15	7	17	15	37	28	41	41	45
4	11	11	7	26	40	23	26	23	56	78
5	6	6	10			8	13	8		
6	11	11	11			17	21	17		
7	0	0	3			3	7	4		
8	0	6	3			0	6	13		
9	4					5				
10	0					3				
11	2					4				
12	0					0				
13	0					1				
Total runs =	103	109	113	152	134	248	233	256	330	298

TABLE 4

Comparison of Coding Methods

305 Targets

Output Intervals	*No Code*	*Numbers Out*			
		Code 1		*Code 2*	
		8 run max	*4 run max*	*8 run max*	*4 run max*
9	270	305	305	305	305
10	250	305	305	305	305
11	240	305	305	305	305
12	225	305	305	305	297
13	201	305	303	305	289
14	192	305	297	305	279
15	183	305	280	305	270
16	176	305	270	305	260

TABLE 5

662 Targets

9	397	662	649	662	646
10	384	662	630	662	627
11	340	662	620	662	620
12	320	662	601	662	587
13	295	657	581	662	581
14	274	657	535	653	520
15	256	640	501	648	500
16	240	635	475	628	480

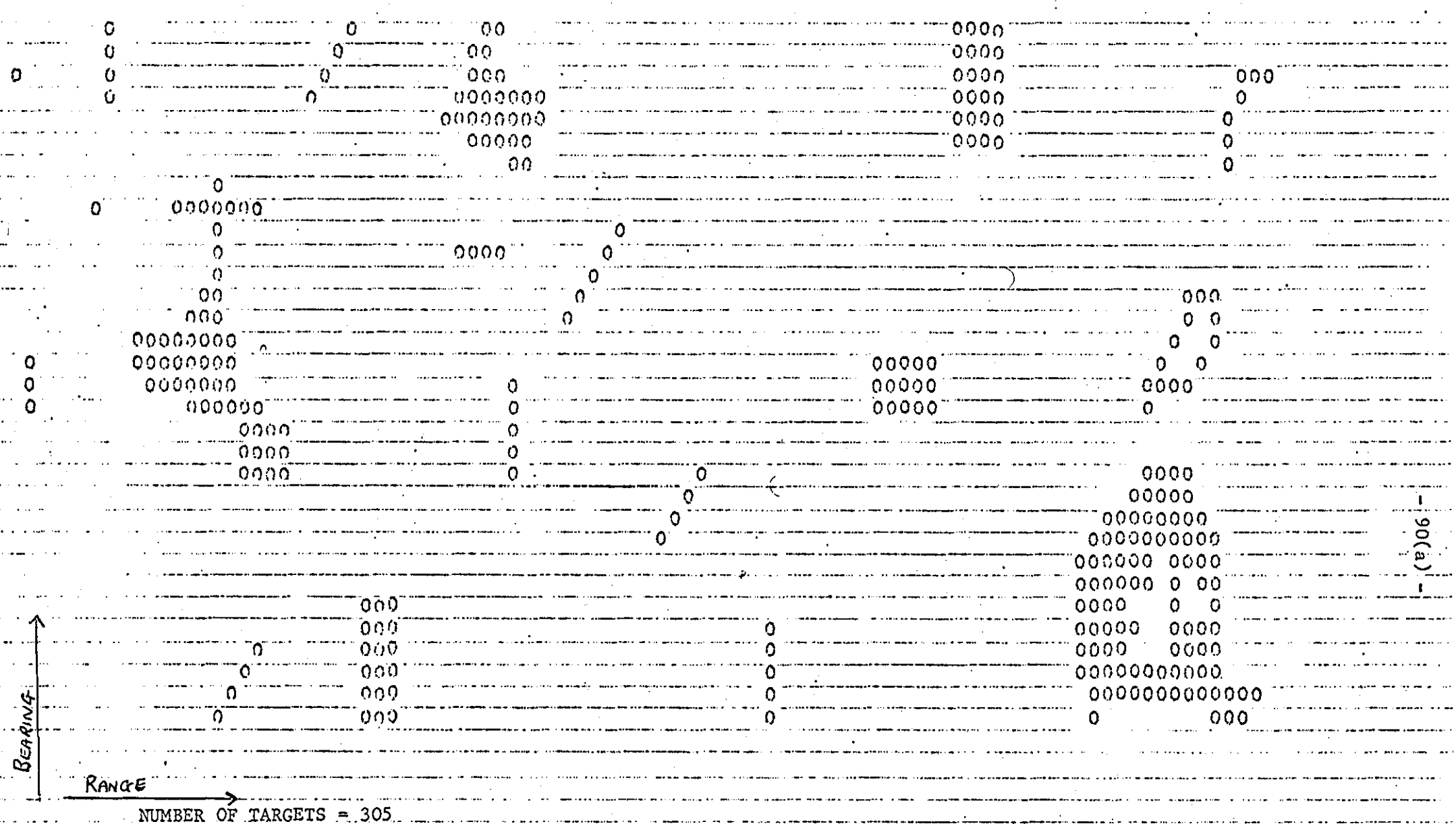
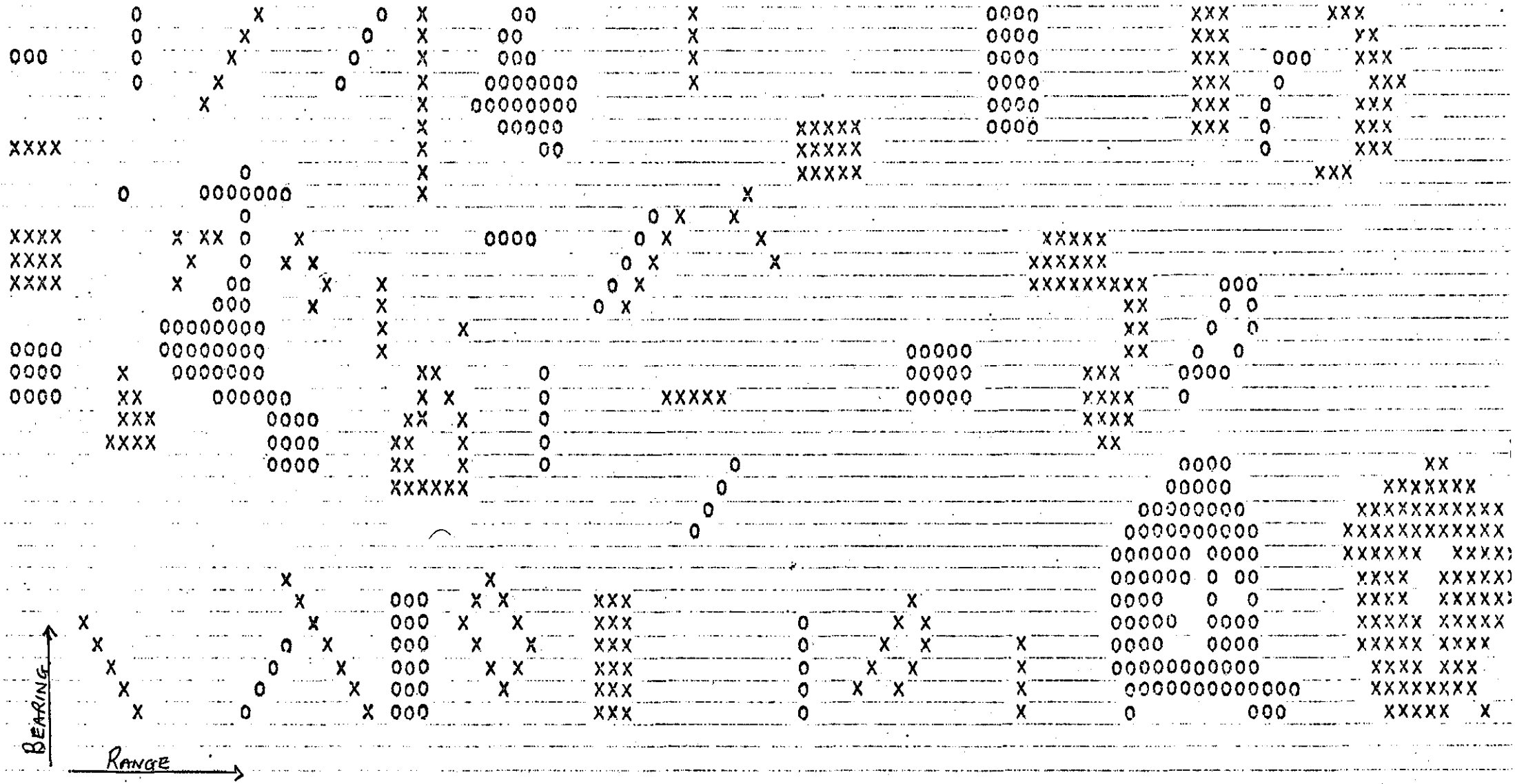


Figure 4.8: Simulated Input Pattern



NUMBER OF TARGETS = 660

Figure 4.9: Simulated Input Pattern - 660 Case

Figure 4.10: Output Display for "305" Pattern

(No Run Length Coding, Output Period Interval - 11)

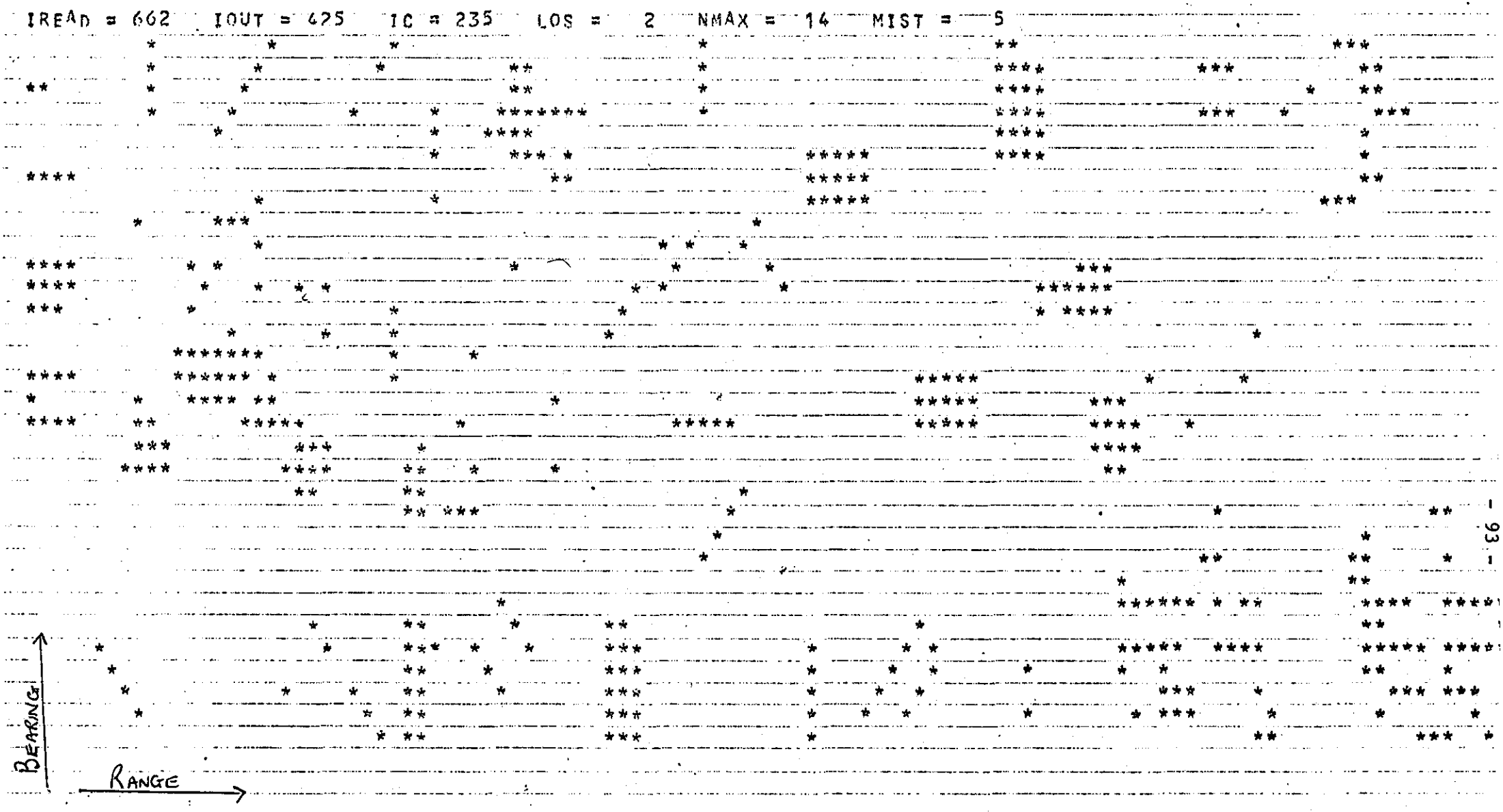


Figure 4.11: Output Display for "660" Pattern

(No Run Length Coding, Output Interval - 9)

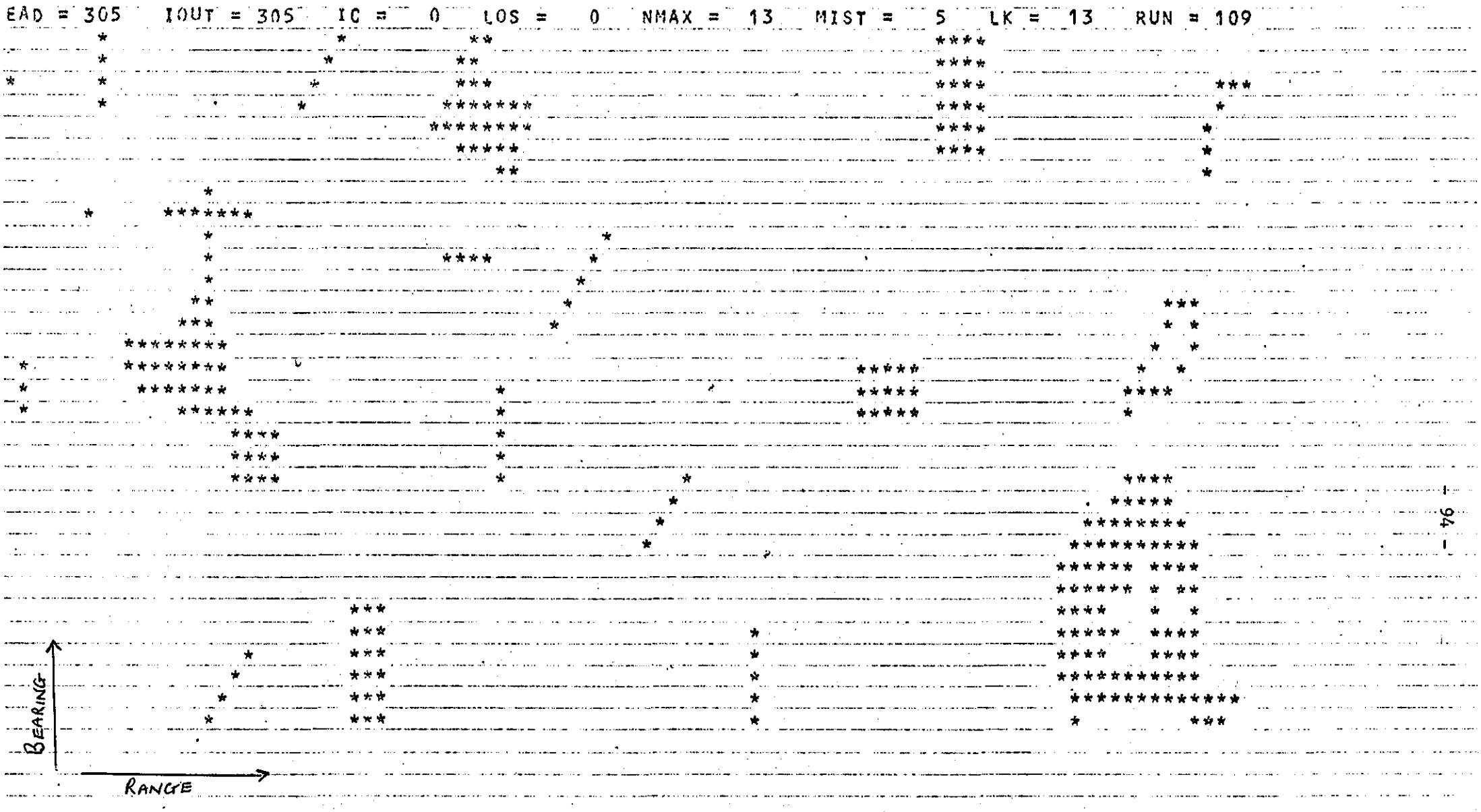


Figure 4.12: Output Display for "305" Targets Pattern

(Run Length Code 2 - Maximum Run of 8 Targets Output Interval = 13)

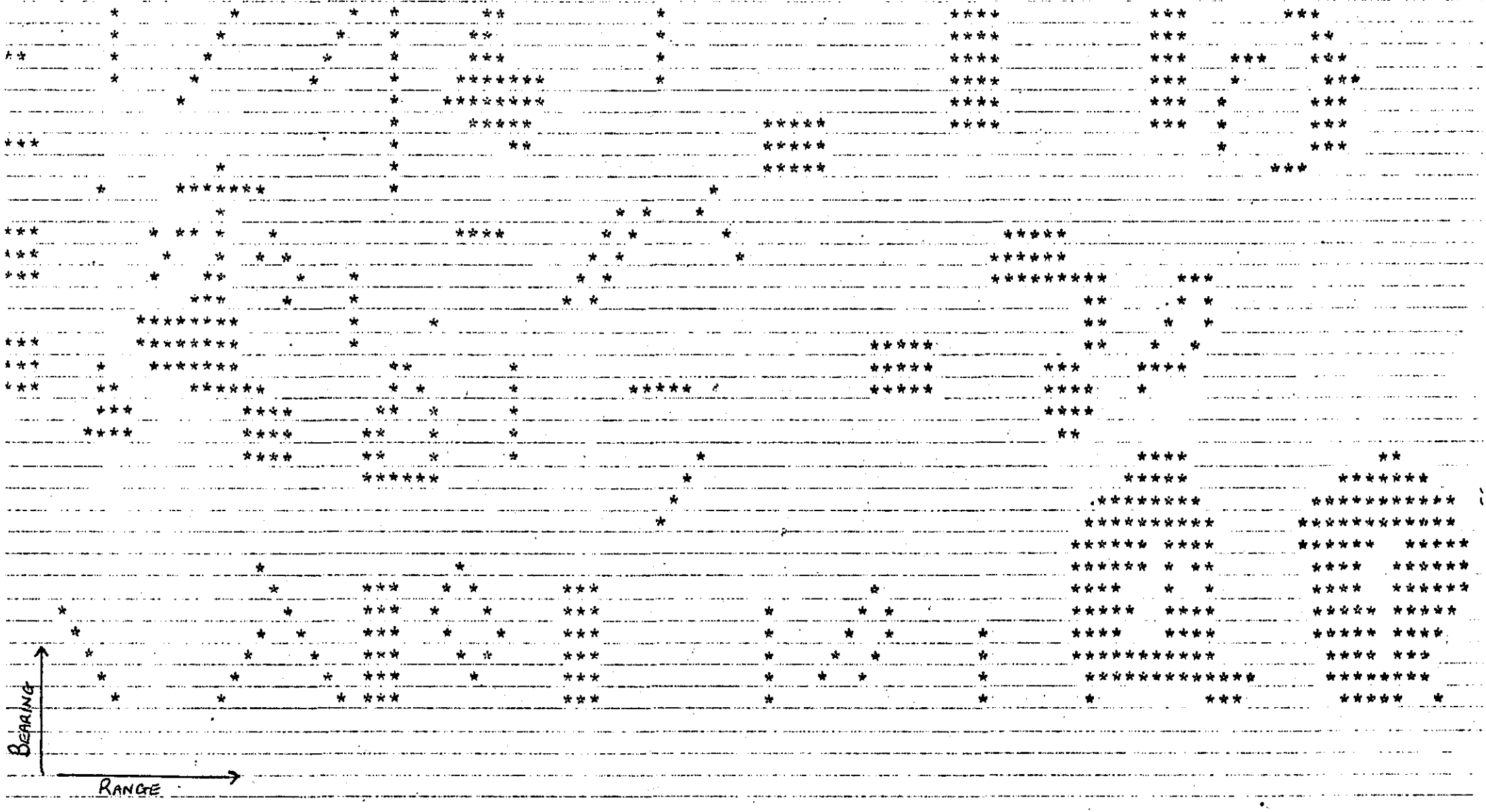


Figure 4.13: Output Display for "660" Targets Pattern

(Run Length Code 2 - Maximum Run of 8 Targets, Output Interval - 13)

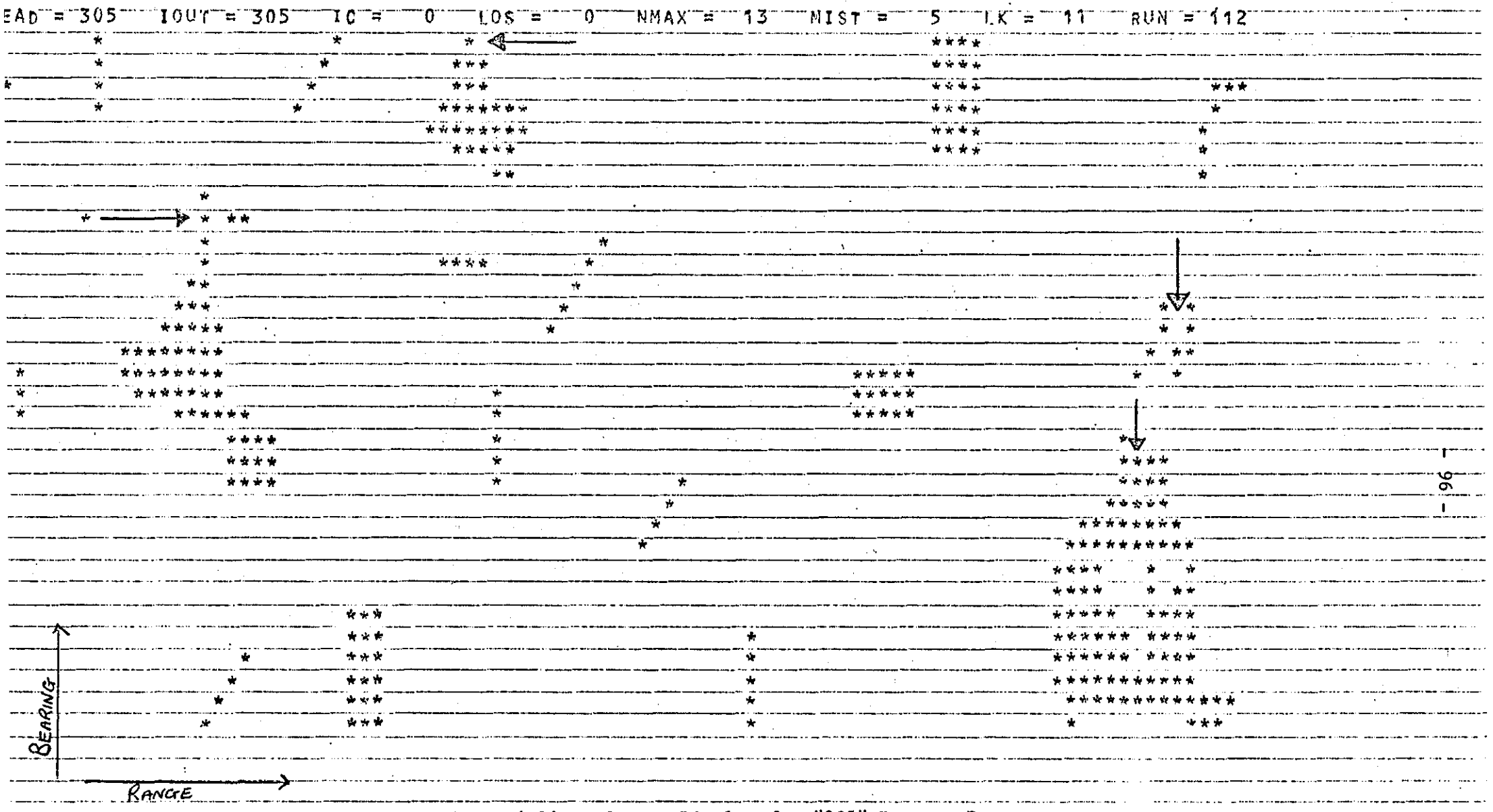


Figure 4.14: Output Display for "305" Targets Pattern

(Run Length Code 1 - Maximum Run of 8 Targets - Output Interval = 11)

Note distortion at sections indicated by arrows.

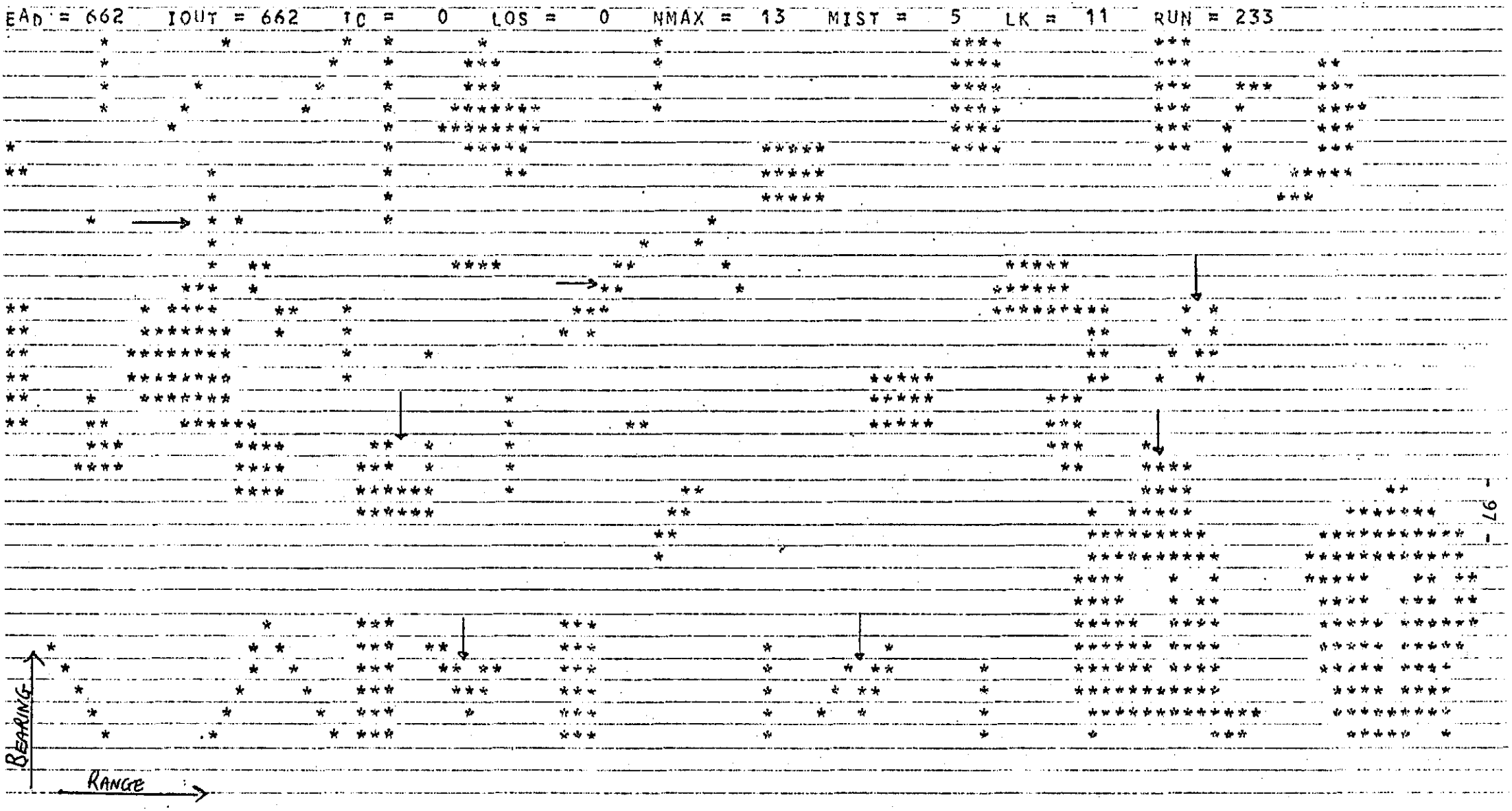


Figure 4.15: Output Display for "660" Targets Pattern.

(Run Length Code 1 = Maximum Run of 4 Targets, Output Interval = 11)

Note distortion at sections indicated by arrows

REFERENCES: CHAPTER 4

1. Hammersley J.M. and Handscomb D.C.: Monte Carlo Methods, Methuen 1964.

2. Schneider A.: The Monte Carlo Method, London, Pergamon Press 1966.

3. Schmidt J.N. and Taylor R.E.: Simulation and Analysis of Industrial Systems, Illinois, Irwin Series, 1970.

4. Goode H.H. and Machol R.E.: System Engineering, New York, McGraw-Hill, 1957.

5. Tocher K.D.: The Art of Simulation, London, English Universities Press Ltd., 1963.

6. Branson S.J.: Reference 3, Chapter 2.

CHAPTER 5

DESIGN AND CONSTRUCTION OF THE EXPERIMENTAL SYSTEM

5.1 Introduction

The results of the simulation runs suggest that for suitably chosen system parameters the recirculating storage system could produce compression ratios comparable with those of the random access store. The purpose of the experimental system is to test the practicality of the method in terms of hardware utilization.

Figure 5.1 shows in schematic form the main features of the proposed system. In an operational system the design would have to consider transmission through a communication channel. This would involve the design of modulation and demodulation systems. However, this project has concerned itself with processing the signal before modulation and after demodulation of the R.F carrier. The choice of the transmission media will depend eventually on the location of the system, but since these details are standard for such systems no thorough research was conducted into this aspect of the system. In any calculations to establish bandwidth requirements a typical value for Signal-to-Noise ratio will be assumed.

The Target Simulator (Figure 5.2) provides the system with video signals representing targets, and range and bearing pulses for line and frame synchronization of the B-scan display.

The Input Circuitry includes a Display Clock a Target Detector and Time Quantizer and the Encoding Circuits. The Target Detector clips the video signal and the Time Quantizer synchronizes the clipped signal to the Display Clock. The encoder is also synchronized to the display clock as well as to the range and bearing pulses. When the Target Detector produces a pulse, the encoder contains a 14-bit word which indicates the position of this target. This information may be transferred in parallel directly to the Input Buffer to await acceptance by the store. Alternatively, if the Run Length Coder is used, transfer may be delayed until the end of a run; then a 17-bit word indicating the length of the run and the co-ordinate of the last position of the run is transferred to the Input Buffer. A manual switch is included in the design to include the Run-Length Coder when required.

The Input Decision Circuit examines the recirculating data train for empty word spaces. It controls the transfer of data from the encoders to the Input Buffer and from the Input Buffer to the Main Store. If a new word arrives from the encoder while the previous word is still in the Input Buffer, the Input Decision Circuit causes the new word to be discarded.

The Main Store unit consists of the recirculating store and clocks. The store is built from Metal Oxide Semiconductor Shift Registers, hence clock drivers are necessary to provide the level translation to MOS levels. The Main Clock, which recirculates data also shifts information from the Input Buffer to the store and from the store into the Output Buffers.

The Output Circuits consist of the Output Decision Circuits, the Output Buffers, the Output Clock, the Transfer Circuits and the Decoder.

The Output Decision Circuit examines the last position of the Main Store and the Output Buffers, after every word shift. If a word is present and a register is empty, this word is transferred serially at the recirculating clock rate to the vacant register. If all registers are filled then all words are diverted to the Input Decision Circuit.

The Output Buffers are simply three sets of registers capable of receiving one word at the recirculating clock rate.

The Output Clock is obtained from the Main Clock by division. Several stages of division are taken to test the system's performance over a range of output rates.

The Transfer Circuits examine the Output Buffers at the end of every output period. Data are transferred from the first occupied register located to the Decoder.

The Decoder separates run-length information from co-ordinate information and provides the Digital-to-Analog converters with a 9-bit and 5-bit word indicating range and bearing. The Decoder is used only if the Run Length Coder is used and is engaged automatically by the run-length code. If no run coding is done the single co-ordinate word is transferred directly to the D-to-A converters.

The Digital-to-Analog converters produce analog signals proportional to co-ordinate positions; these are applied to the "X" and "Y" plates of a cathode ray tube. Bright-up pulses are applied to the "Z"

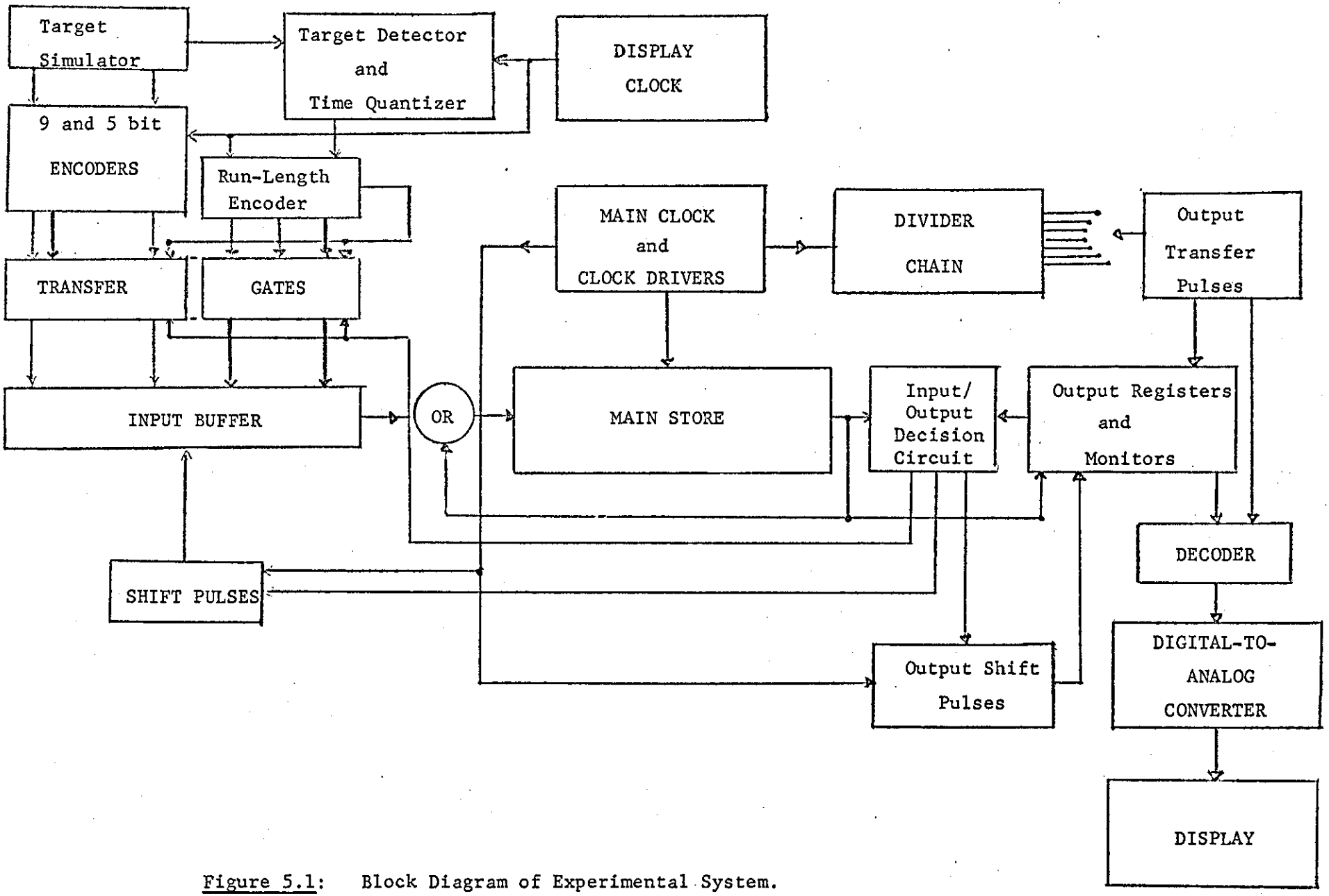


Figure 5.1: Block Diagram of Experimental System.

modulation terminal to prevent the transition of the spot from one co-ordinate to the next from being visible on the screen.

Since M.O.S. shift registers are used for the Main Store and RTL and TTL logic circuits are used elsewhere, interface circuits between the two sets of devices are provided.

A detailed description of the complete system is given in the following sections.

5.2 The Target Simulator

In the absence of signals from a sonar system it was decided to incorporate into the system a target simulator.

Figure 5.2 shows in schematic form the main features of this system. This method uses the flying spot scanning technique and is similar to one designed and built before in this department (1). This system is capable of producing real time signals by scanning a moving film taken from a sonar display. However, this would require complicated mechanical designs as the film is only moved during the flyback period at the end of the scanning frame. These refinements have been achieved in television scanning systems; however, for the purposes of this project, only the static system is used.

The cathode ray tube used had a P 15 phosphor which has a decay time of about 2 microseconds. The bearing resolution time is of the order of 3 microseconds hence the phosphor resolution requirements are just satisfied. Ideally a larger separation would be preferred in

order to accommodate the capacative effects of the coaxial cable used to conduct the video signal. However the P 15 phosphor produced reasonable signals hence this system was accepted. An alternative scheme using a vidicon system is being investigated elsewhere (2). This system overcomes the resolution problems of the flying-spot scanning system.

The Raster Generator consist of two sawtooth generators whose sweep times are designed to simulate the required range and bearing times. The range sawtooth is made variable such that different range scans can be simulated. The bearing sweep is a constant 100 microsecond sweep. The circuit for the sawtooth generators is described Appendix 3. The slow sawtooth is applied to the "Y" deflection plates and the fast sawtooth to the "X" plates of the raster generating oscilloscope.

The pulses produced during the flyback of the sweep waveforms are used as the range and bearing pulses.

The raster is projected on to the film by a system of lenses, and the modulated light is received by a photomultiplier. The photomultiplier tube used is an RCA 931A tube.

The video signal from the photo tube is first fed into a head amplifier which serves as the input stage of the video amplifier. This head amplifier is simply a field effect transistor circuit in the common drain mode. This amplifier, which has unity gain serves as an impedance matching transformer for the output of the photomultiplier and the input of the video amplifier stage.

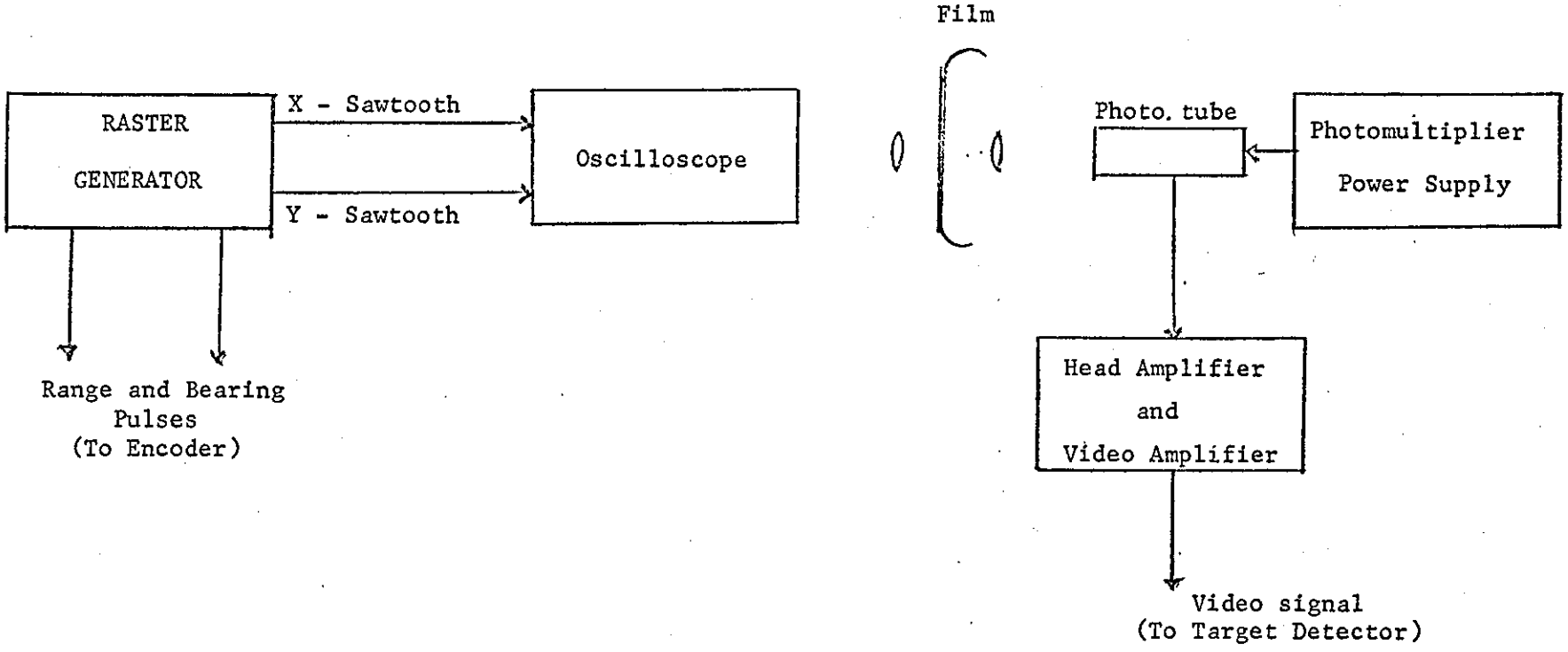


Figure 5.2: Block Diagram of Target Simulator.

The video amplifier is designed to have a gain of 20 with a bandwidth of 1 MHz. Since the target resolution is of the order of 3 microsecond, the video amplifier should have a bandwidth of at least 330 KHz, hence this requirement is easily accommodated. The output of the video amplifier will be fed to a threshold detector; with the signal from the photomultiplier of the order of 300 millivolts, this gain produces an output voltage of sufficient magnitude to trigger the threshold detector. The design of the video and head amplifiers is discussed in Appendix 3.

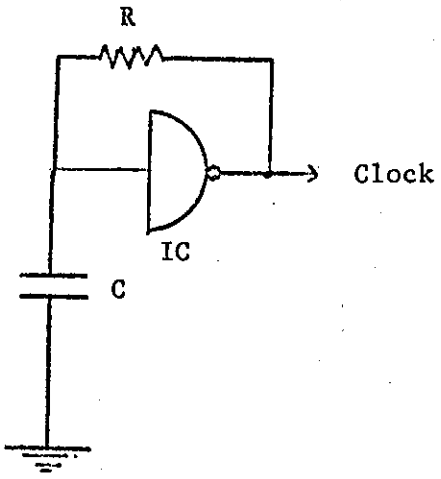
5.3 The Target Detector

The target detector is required to produce a pulse whenever the video signal exceeds a predetermined level. This level has to be determined by examining the video signal from knowntarget patterns. A potentiometer is included in the design which allows adjustment of this switching level. The design of the threshold detector is discussed in Appendix 3. Since these pulses are required to switch R.T.L. and T.T.L. logic circuits, the design of the threshold detector also includes provision for translating these pulses to the required level.

5.4 The Display Clock

This clock is required to synchronize the video pulses to the rest of the system. It is also used to digitize the bearing time into 32 resolution cells.

The clock is built around a TTL Schmitt trigger and is designed to operate at 330 KHz. The circuit used is shown in Figure 5.3. The mark-space ratio of the clock is adjusted so that the clock pulse is "ON" for 0.5 microsecond.



R = 330 ohms

C - Chosen according to frequency required

IC - SN 7413 (Dual Schmitt-Trigger)

Figure 5.3: The Schmitt-Trigger used as a multivibrator.

5.5 Blanking and Quantization Circuits

5.5.1 Blanking Circuit

No provisions are made for suppressing the range and bearing sweeps during their fly-back periods. This of course produces unwanted signal. This was intentional since with a digital system it is just as easy to use the flyback pulses to inhibit the unwanted pulses.

The logic requirements are therefore to reject all video pulses if range or bearing flyback pulses are present. Hence,

$$TD = VP \cdot \overline{RP} \cdot \overline{BP}$$

where TD = Target Detected Pulse

VP = Video Pulse

RP = Range Pulse

BP = Bearing Pulse

Figure 5.4A shows the implementation of this circuit using TTL gates, and Figure 5.4B shows the resulting waveform diagram.

5.5.2 Quantization Circuit

Target pulses from the threshold detector are produced whenever the video signal exceeds the preset level. The position of these pulses on the bearing scan line must be related to one of the thirty-two co-ordinate cells on the scan line. The clock discussed in Section 5.4 is synchronized to the co-ordinates digitizer; hence, if each target pulse is synchronized to a clock pulse, then it is automatically synchronized to a co-ordinate.

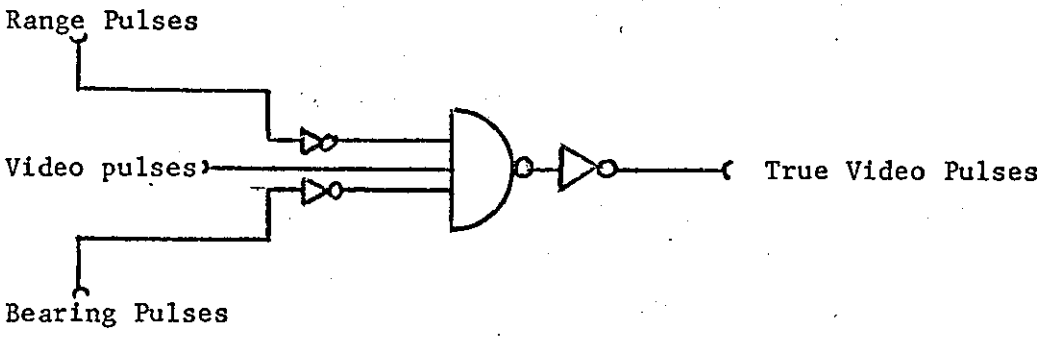


Figure 5.4A: Flyback blanking circuit.

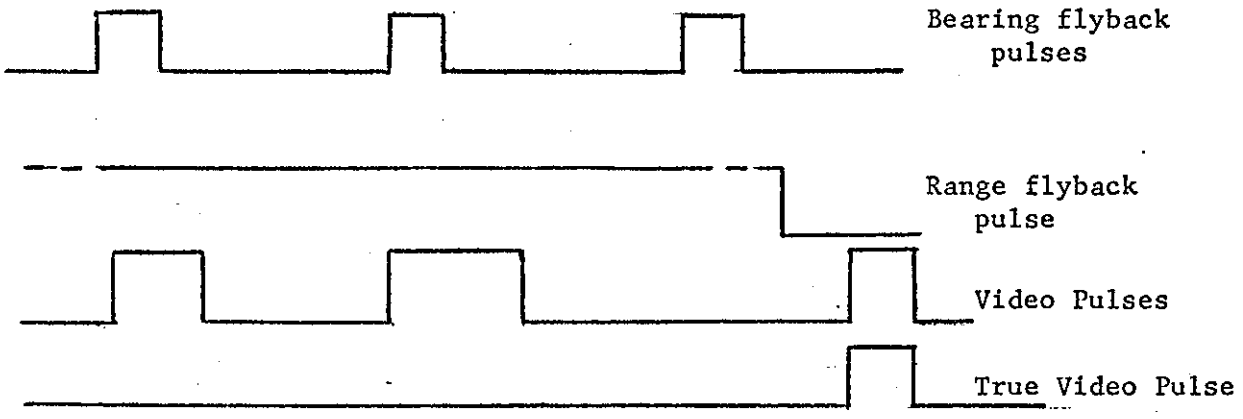


Figure 5.4B: Waveform diagram for flyback blanking.

Figure 5.5A shows the method used to time quantize these target pulses. The Target Detected pulse (TD) is fed to a monostable with a time constant of 3 microseconds. This pulse is fed to the J input and its inverse to the K input of a J-K Master Slave Flip Flop. This Flip-Flop is triggered by the display clock; hence its output is the time quantized version of TD. Figure 5.5B shows the waveforms representing this action. It should be noted that all pulses of length $\geq$ 3 microseconds will be time quantized without the monostable. However, it is possible for pulses of length less than 3 microseconds to be ignored with this monostable. If two pulses are less than 3 microseconds apart then the second pulse is ignored since the bearing resolution is set at 3 microseconds.

It is appreciated that this method of target detection and time quantization is prone to noise pulses common to all sonar systems. However, it is assumed that the signal processing of the signal would have been done within the sonar receiver itself. In addition, it is proposed that the final system will include a moving-target indicator which provides signals for the compression system. This fixed-target removal system is being considered elsewhere and it is intended that this system will contain more complicated noise-combatting circuitry.

5.6 Co-ordinates Encoder

The sector scanning sonar system, on whose specification this model is being designed, has a minimum pulse width of 100 microseconds with a 32-element receiving array. The co-ordinates encoder is therefore required to digitize this 100 microsecond interval into 32 (2^5) equal

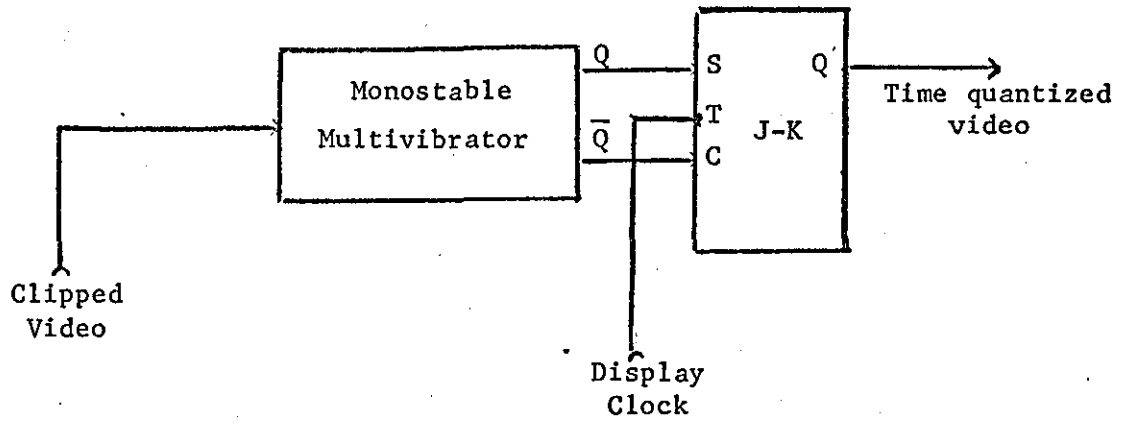
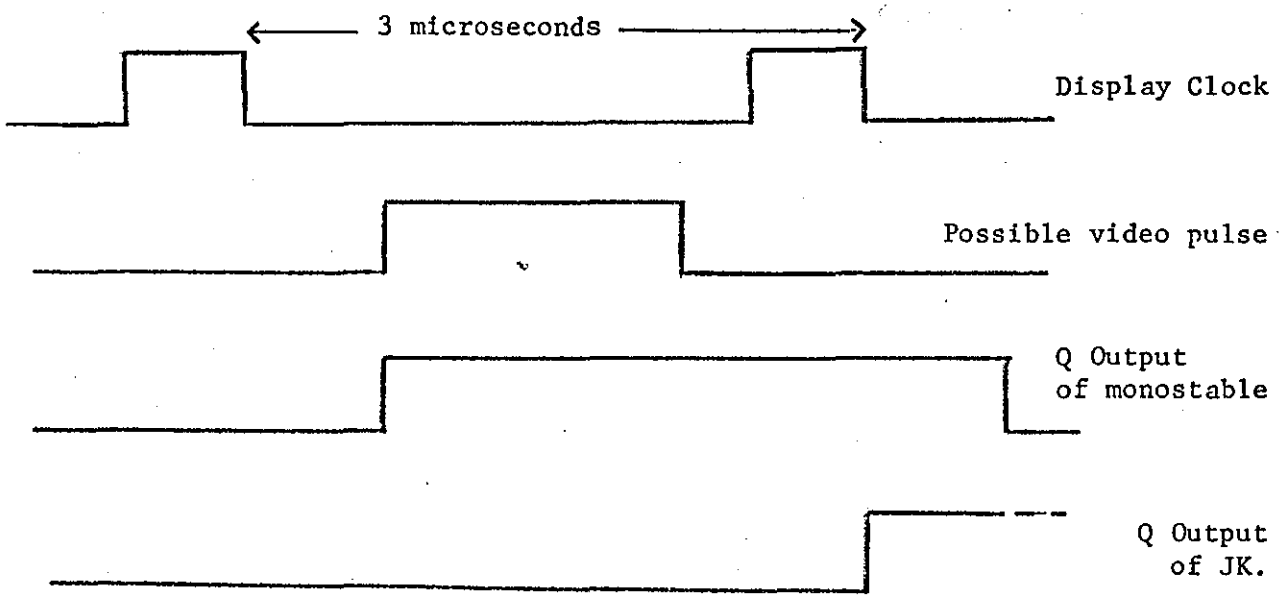


Figure 5.5A: Time Quantization Circuit.



Monostable multivibrator - SN74121

J - K Flip-Flop - SN7472

Figure 5.5B: Waveform diagram for Time Quantization process.

intervals. The range intervals are automatically produced by the bearing scan pulses. This system is designed to simulate 512 (2^9) range resolution cells.

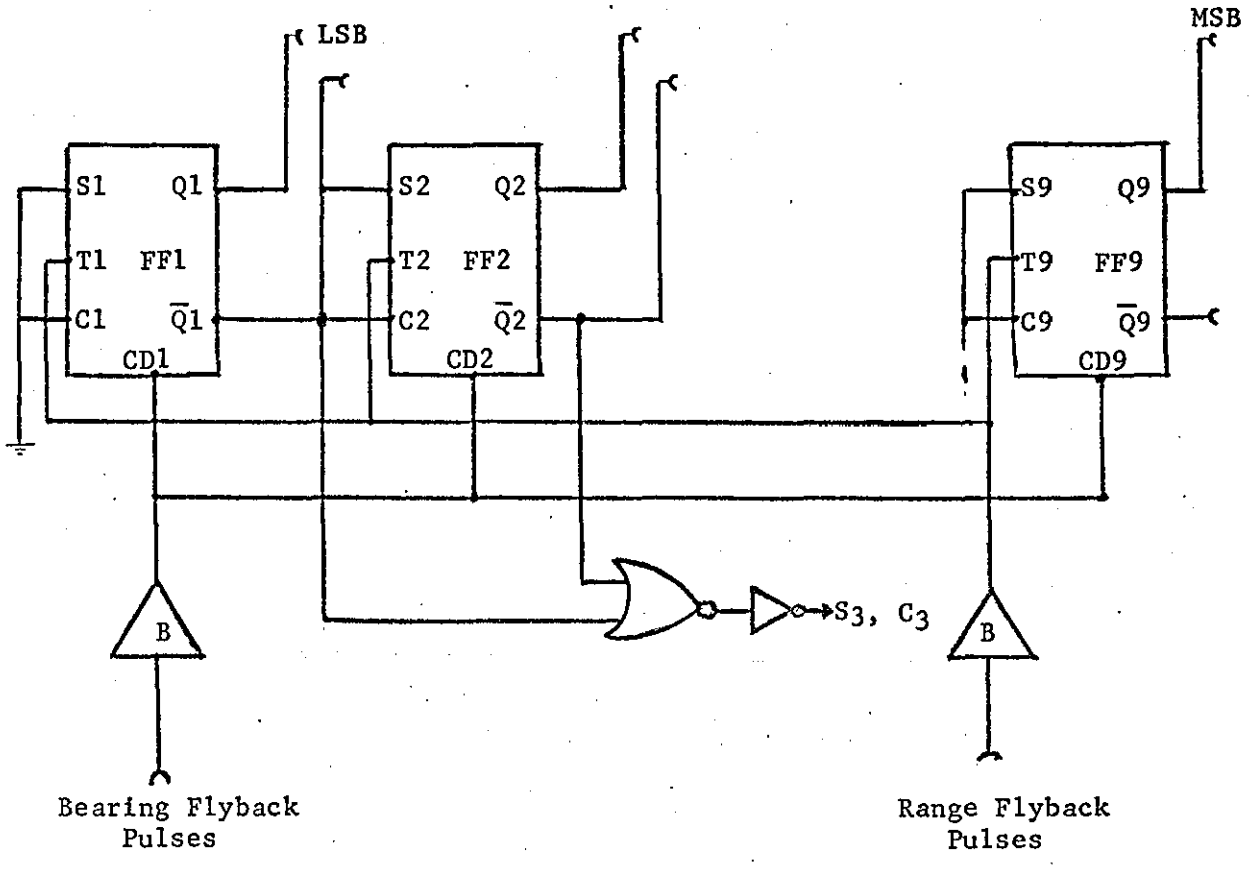
The range encoder is simply a 9-stage binary counter triggered by the bearing scan flyback pulses and cleared by the range flyback pulses, Figure 5.6A.

The bearing digitizer is built around a 5-stage binary counter. If the simulator is accurately designed such that the bearing sweep time is exactly 32 clock pulses in duration, then triggering the 5-bit counter with the display clock would provide accurate encoding. However, in order to obtain accurate synchronization it is necessary to ensure that counting begins at the start of the bearing sweep. The count should cease after the 31st count when the counter is in the all one's state; also counting should be inhibited during the range sweep flyback times.

Figure 5.6B shows the circuit used to implement these requirements. The counter is cleared by each active bearing pulse; this ensures that the counter is in the all zero's state at the start of the sweep. Clocking then begins on the next clock pulse. When the counter is in the all one's state the monitor signal M inhibits further counting. The clock is therefore gated with a control pulse formed by performing the function,

Control Pulse = $\overline{RP}.\ \overline{BP}.\ \overline{M}$, where M = 1 when the counter is in the 1 1 1 1 1 state.

Figure 5.6C shows the waveform diagramsof the process.



$S1, C1 = 0$

$S_n, C_n = \overline{Q_{n-1} \quad S_{n-1}}$

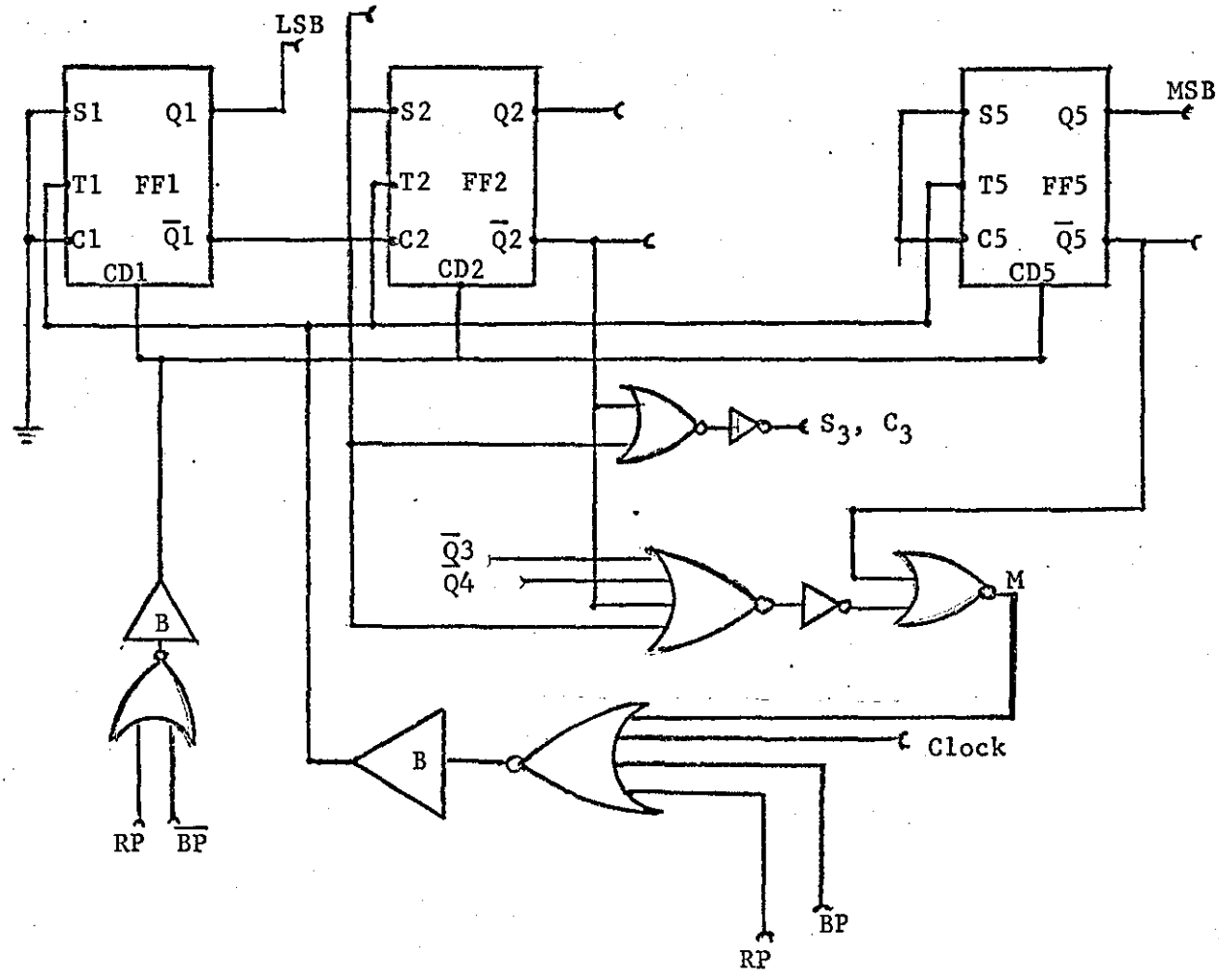
All Flip-Flops - MC 726P

All Buffers - 4 - Input OR (Buffer) MC788P

2 - Input NOR - MC724P

Inverters - MC789P

Figure 5.6A: Schematic diagram of Range Counter.



4 - Input NOR - MC725P

Other Devices as before

Figure 5.6B: The Bearing Digitizer.

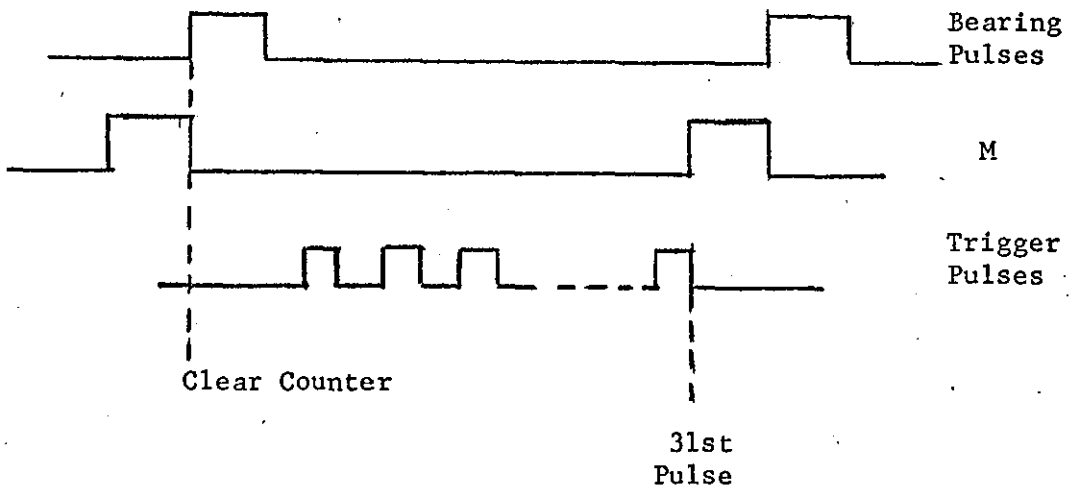


Figure 5.6C: Waveform diagrams for Bearing Digitizer.

The Q and $\overline{Q}$ outputs of all fourteen Flip-Flops are taken to external pins to be used for setting the Flip-Flops of the Input Buffer.

5.7 Run Length Encoder

The purpose of the Run Length Encoder (RLE) is to restrict the transfer of information to the Input Buffer until either there is a break in the run of targets, or the target run has reached a predetermined maximum value. In either case, the RLE transfers a word indicating the length of the run and the co-ordinate of the last point in the run. The maximum run-length selected for this system is a run of 8; hence each word is now a 17-bit word. The system also contains a manual control which can inhibit the RLE's operation. The word length is still 17-bits, but entry is attempted at every Target Detected signal, and the run-length word is always 000.

Figure 5.7A shows in schematic form the principle of operation of the RLE circuit. If the code switch is in the ON position the Run Length Decision (RLD) circuit examines the Target Detected pulses and controls the clocking of the Run Length Counter (RLC). It also examines the state of the counter; when a count of eight is recorded or a break in the target run is detected the RLD circuit produces a Transfer Pulse (TP), which is used to control the transfer of the 3-bit word from the RLC and the 14-bit word from the co-ordinates encoder. If the code switch is in the OFF position the RLD circuit keeps the RLC in the 000 state and allows all TD pulses to become Transfer Pulses.

5.7.1 The Run Length Decision Circuit

The performance of this circuit can best be examined by referring to the waveform diagram in Figure 5.7B.

Waveform TD represents a run of targets on a scan line which contains examples of possible run distributions. Waveform TDD represents a delayed version of TD, the delay time being one clock pulse. From the waveform diagram it is seen that by the coding algorithm selected, transfer is possible at points A, B and C. Hence, TP is formed by the logic function

$$TP = TDD.\ \overline{TD} + F,$$

where F = 1 when the RLC is in the 111 state. Now to ensure that the counter is ready for the next run it is cleared by a pulse formed by the function,

$$J = TD.\ \overline{TDD};$$

there is no need to perform the clear operation after a run of eight. The above operation means that before every run, the counter is always in the 000 state; hence for a single target run there is no need to clock the counter, for two targets in a run one clock pulse is needed, and so on. Hence, the function $K = \overline{J}.\ TD.\ TDD$, produces the clock waveform for the run counter.

5.7.2 Code - No Code Circuit

This circuit is controlled by a manual switch (S) which is in either logical state. When S = 0, the coding operation is inhibited; hence all co-ordinates are transferable and the run count is always 000. When S = 1 coding occurs as described above.

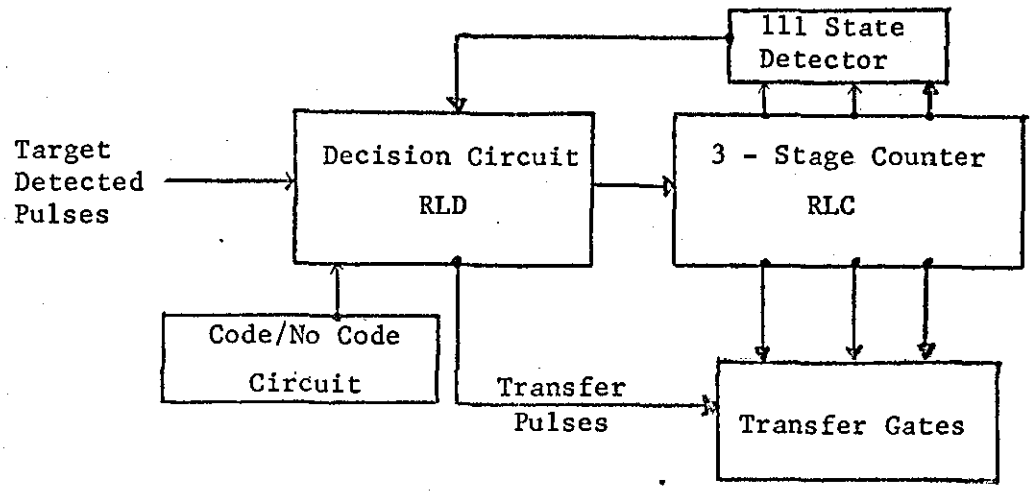


Figure 5.7A: Block Diagram of Run Length Encoder.

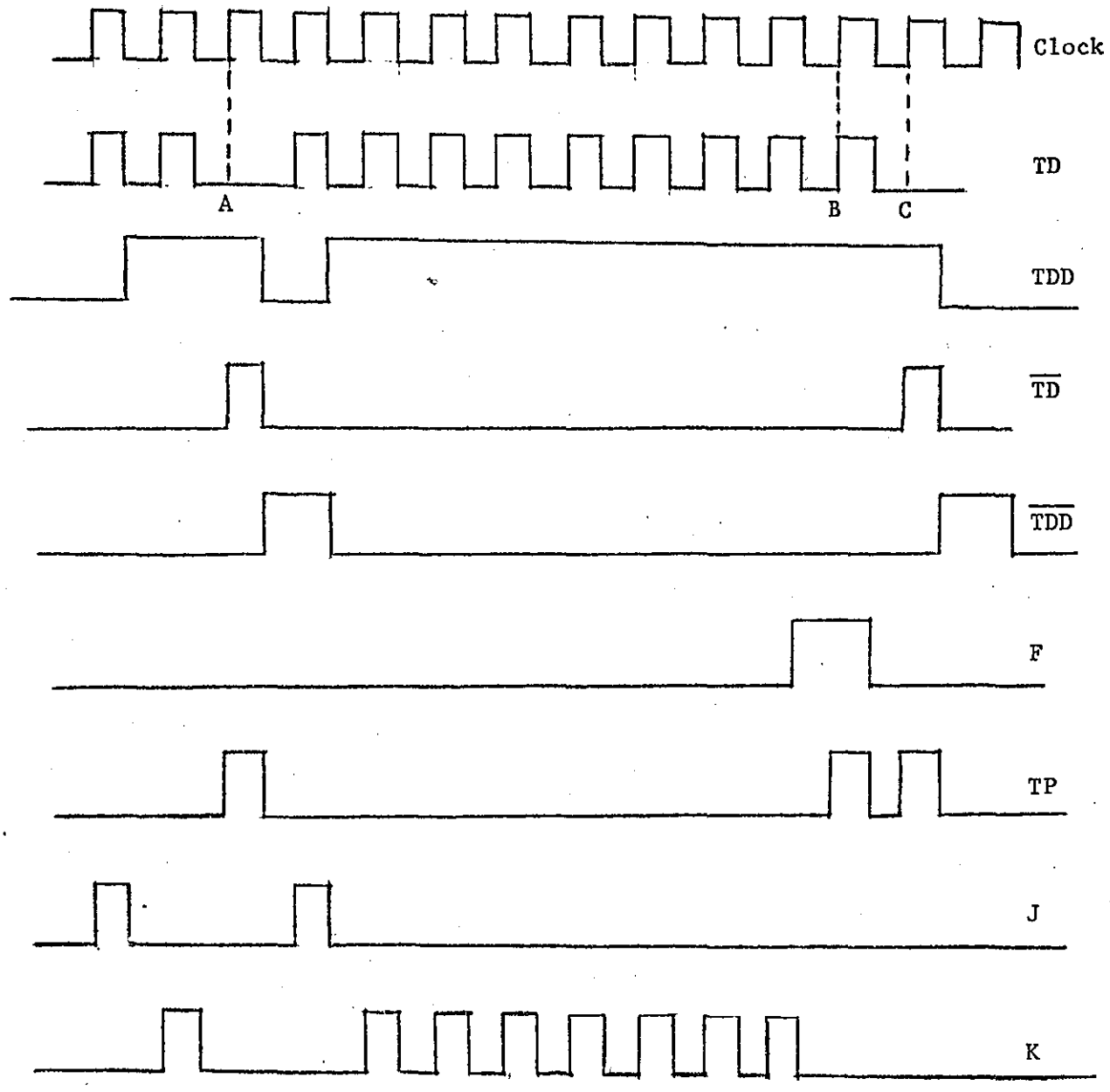
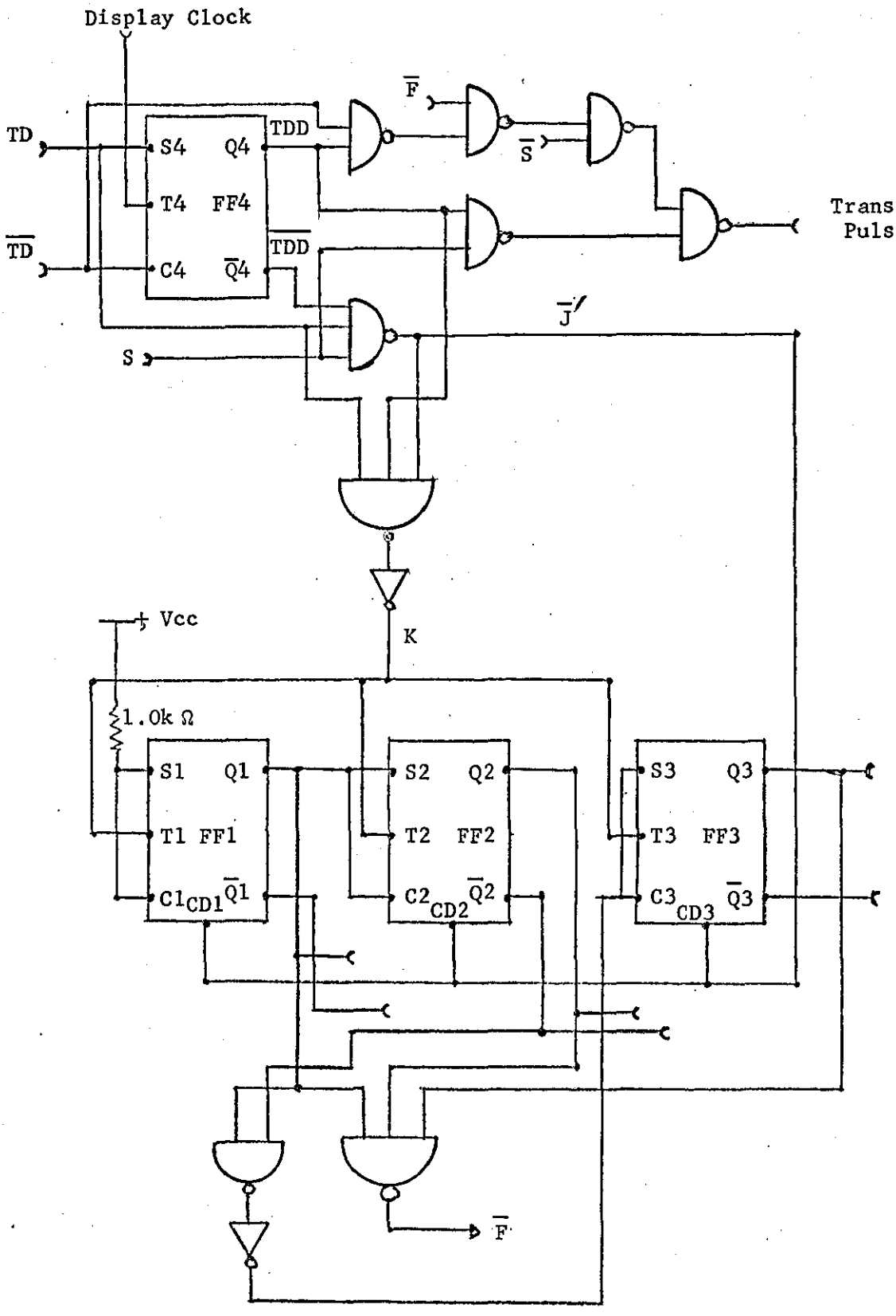


Figure 5.7B: Waveform Diagram showing the operation of the Run Length Decision Circuit



FF1, FF2, FF3, FF4 - TTL Master-Slave Flip-Flop SN7472

3 - Input NAND Gates - SN 7410
2 - Input NAND Gates - SN7400
Inverters - SN7404

Figure 5.7C: Implementation of Run Length Encoder.

Hence two sets of pulses are modified when S = 0, that is the clear pulse and the Transfer Pulse. The clear pulse now becomes J', where

$$J' = S.J,$$

and the Transfer Pulse becomes TP', where

$$TP' = \overline{S}.\ TD + S.TP.$$

5.7.3 Circuit Implementation

Figure 5.7C shows the circuit implementation of the RLE using TTL gates and Flip-Flops. The RLC is a simple 3-stage binary counter. The Q and $\overline{Q}$ outputs of the 3 counter stages are taken to external pins for setting and clearing the Run Length registers in the Input Buffer.

5.8 The Recirculating Store

5.8.1 Store Organization

The store was built from 2 dual 64 bits MOS dynamic shift registers (MM510). Hence, each chip consists of 128 Flip-Flops. Figure 5.8A shows the connection diagram of the device. With the recirculate control line at a logic "0" state the device functions as an accumulator. A logic "1" state at this line allows external information to enter the register serially. The manufacturer's data sheet is included in Appendix 4.

The maximum frequency of operation of this device is given as 4MHz, with a power consumption of 0.8 mw/bit/MHz. Now it has been decided to employ a 20-bit word, with 14 bits for co-ordinate information,

3 bits for run length information and 3 extra bits for synchronization purposes. Hence, at the maximum clock rate the word time for a 20-bit word would be 5 microseconds. Since the target resolution time is 3 microseconds it would not be possible to shift in one target before the next target arrived.

Figure 5.8B shows in schematic form the organization of the store which overcomes the difficulties mentioned above. Each 64 bit register is used as a single recirculating register accepting 5 bits of the 20-bit word. In addition, in order to obtain a 13-word store a single bipolar Flip-Flop is attached to each register. The breakdown of the data word is as follows:-

Register 1 - 5 bits of range data

Register 2 - 4 bits of range data + 1 Flag bit

Register 3 - 5 bits of bearing data

Register 4 - 3 bits of run length data + 2 extra bits.

The word time at the maximum clock rate is now 1.25 microseconds.

5.8.2 Interface Units

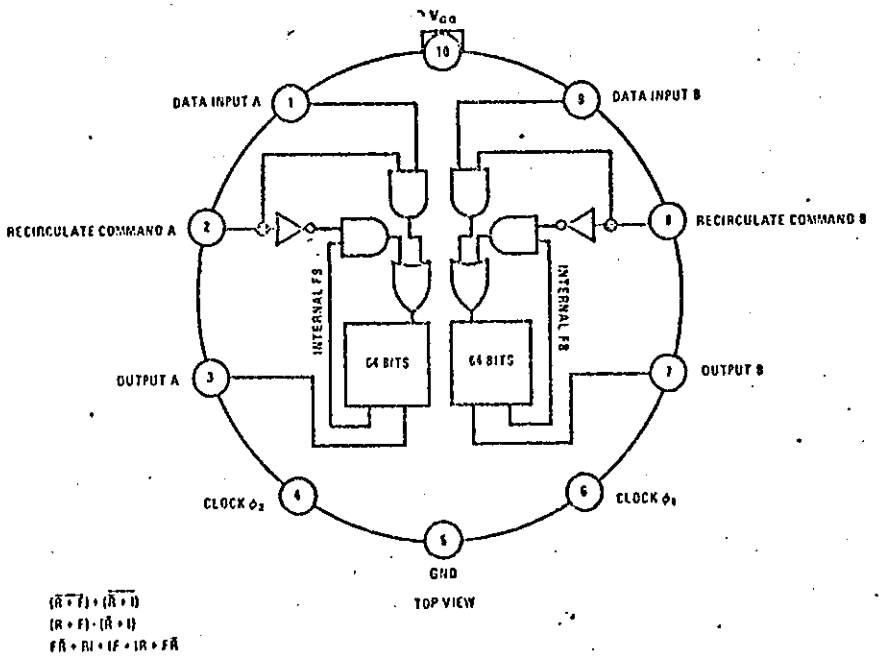
The logic levels for this MOS device are,

Logic "1", -7.0V Minimum, -18V Typical

Logic "0", -2.5V Maximum.

Hence, interface units are required to translate these levels to bipolar levels and vice-versa. Figure 5.8C shows the interface units used.

connection diagram



absolute maximum ratings

Drain Voltage ($+V_{GG}$)		+0.5V to −25V
Clock Inputs (V_{ϕ_1}, V_{ϕ_2})		+0.5 to −25V
Data Inputs		+0.5V to −25V
Power Dissipation (Note 1)		500 mW
Operating Temperature	MM410	−55°C to +125°C
	MM510	−25°C to +70°C
Storage Temperature		−65°C to +150°C

Figure 5.8A: Connection Diagram for MOS Shift Register used in Main Store.

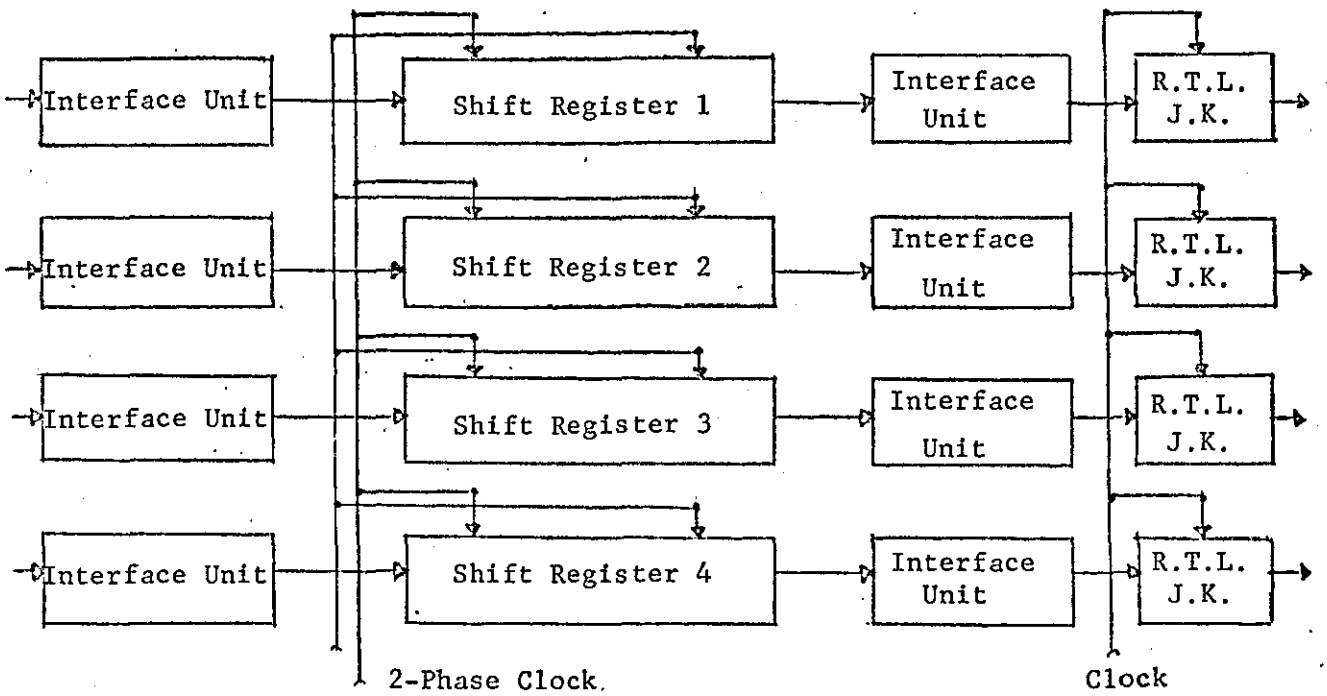
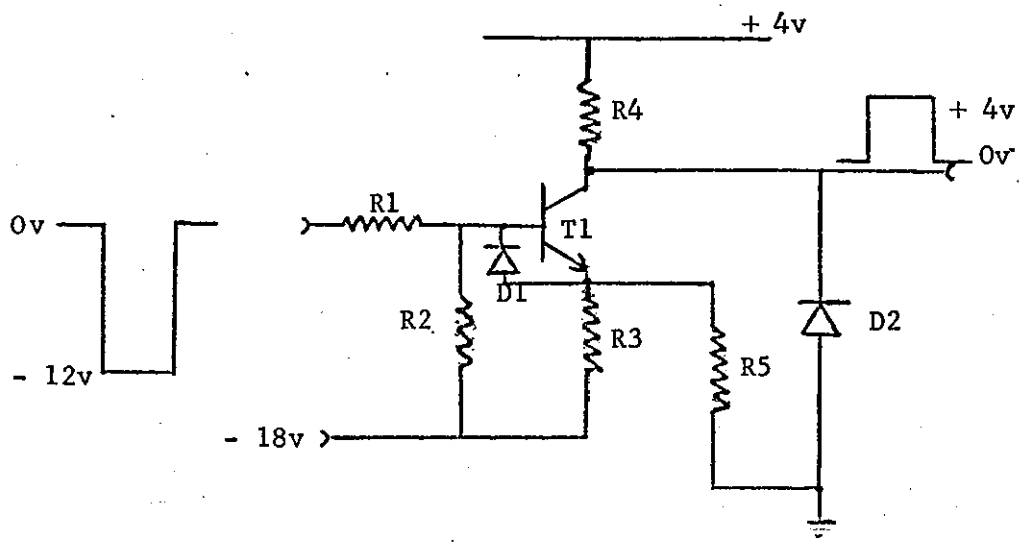
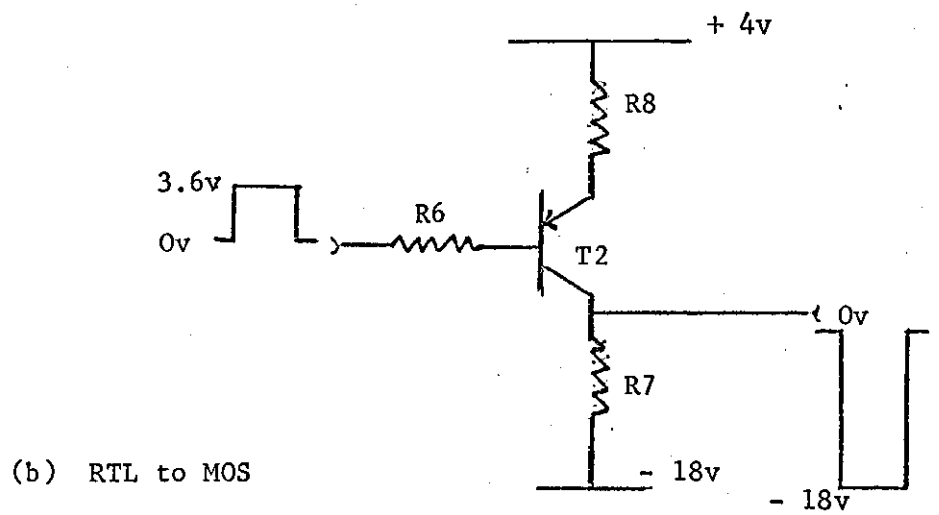


Figure 5.8B: Organization of Main Store Unit.



(a) MOS to RTL



(b) RTL to MOS

T1 - ZTX 302
R1 = 10kΩ
R2 = 22kΩ
R3 = 820Ω
R4 = 2.2kΩ

T2 - 2N.1132; D1, D2, - 1S44
R5 = 1kΩ
R6 = 470Ω
R7 = 1.5kΩ
R8 = 330Ω

Figure 5.8C: Circuit diagrams of interface circuits.

5.8.3 Clock Drivers

In all MOS applications, it is necessary to employ clock drivers capable of driving the high capacitive clock inputs. In addition since the shift registers are of the dynamic types a two-phase clock is needed.

The clock input capacitance of the MM510 is of the order of 40pF at a clock frequency of 1 MHz. An integrated circuit clock driver is used to provide both the level translation from standard logic levels to MOS levels, as well as sufficient current and voltage drive capability for clocking the shift registers.

Figure 5.8D shows the circuit diagram of the device (NH 0007), and Figure 5.8E shows the scheme used to generate the required two phase clock. Figure 5.8F shows the waveforms diagrams of the clock generating process.

5.9 The Input Buffer

The Input Buffer consists of 4 - 5 stage shift registers. The purpose of these registers is to accept data from the encoders in parallel. The registers retain this datauntil a shift command is received; the shift register clock then shifts the data serially into the four recirculating registers. The Transfer Pulse (TP) controls the transfer of data in conjunction with a control pulse from the Input Decision circuit. This control pulse inhibits TP if data are being shifted out or if old data are still in the buffer.

Figure 5.9 shows the schematic diagram of one shift register with its loading gates.

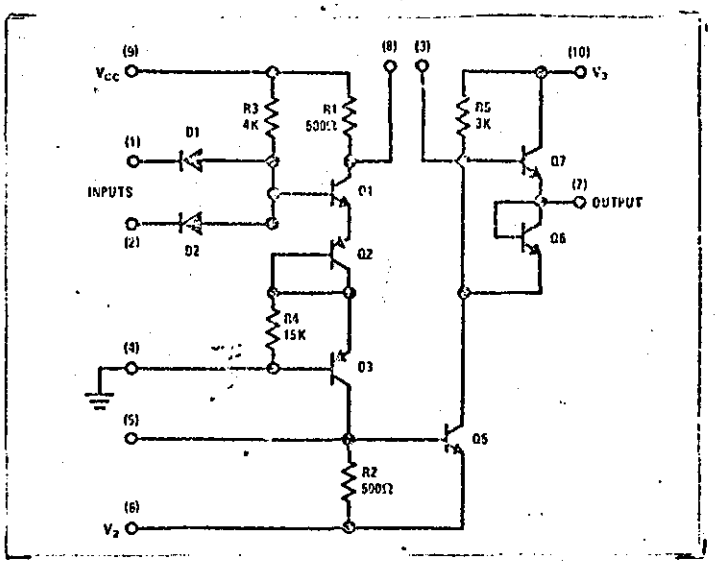


Figure 5.8D: Circuit Diagram of Clock Driver NH 0007.

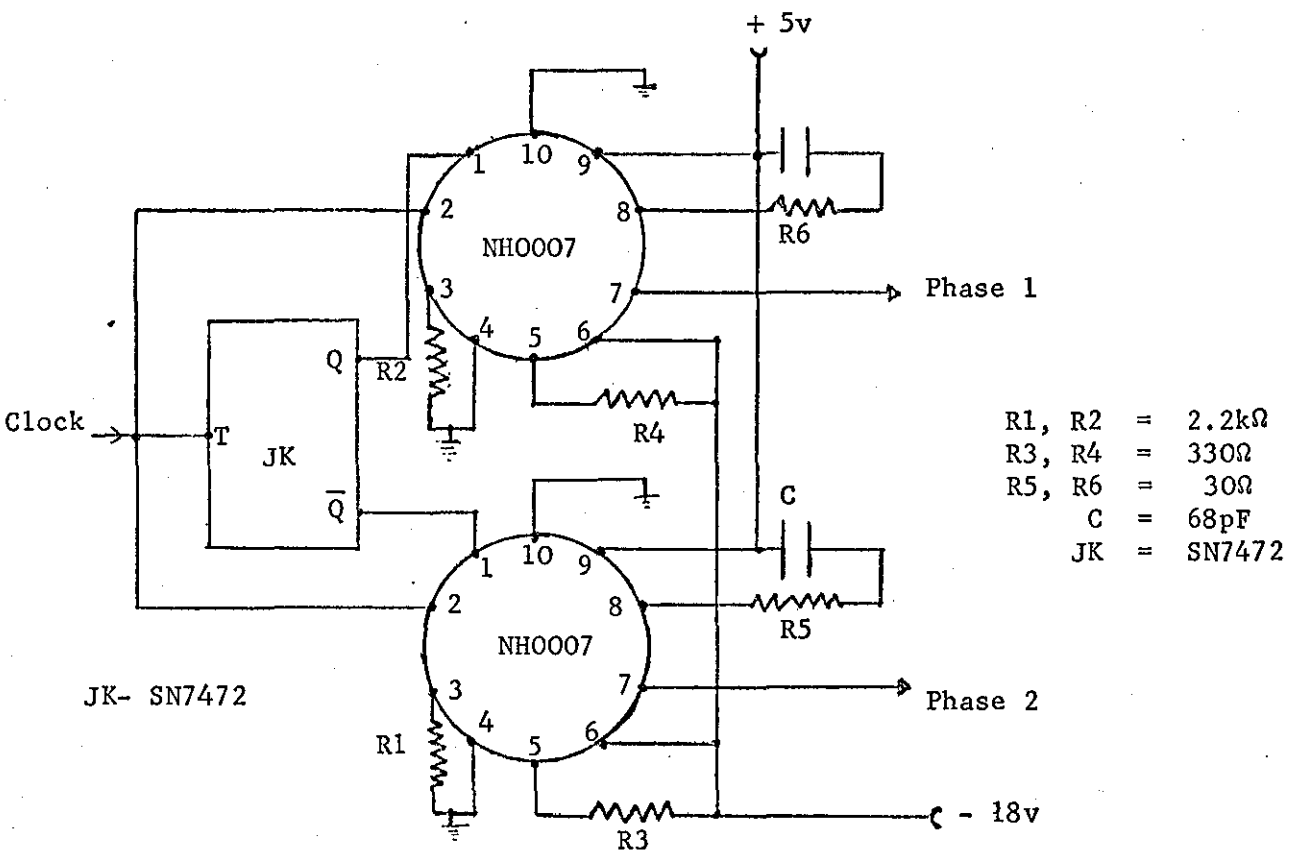


Figure 5.8E: Two Phase clock system.

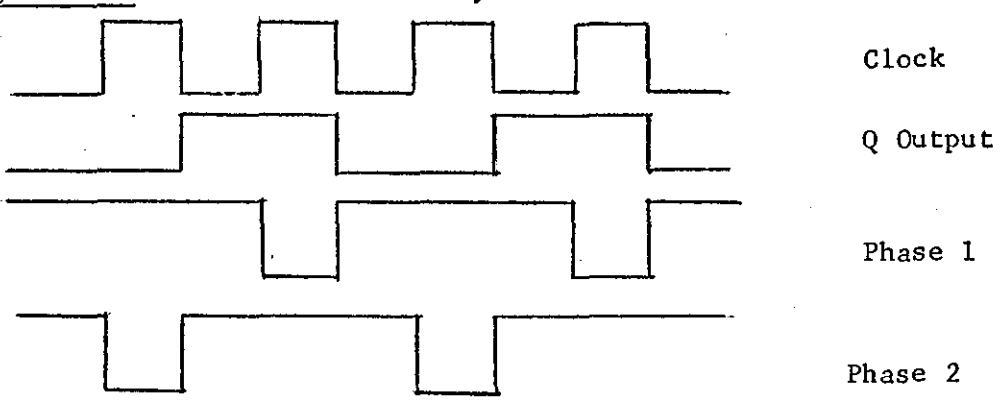


Figure 5.8F: Waveform Diagrams

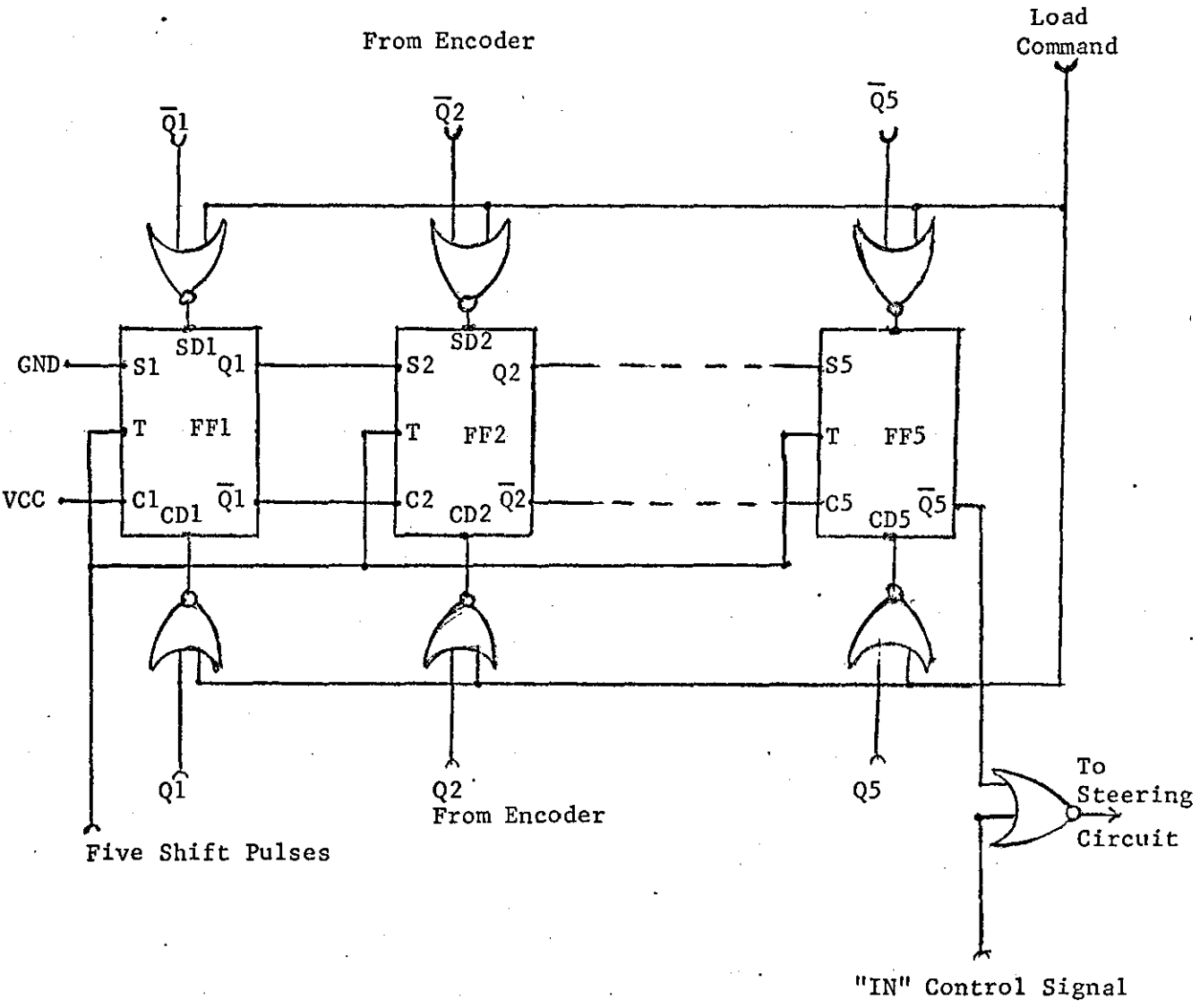


Figure 5.9: Circuit Diagram of Input Register.

5.10 Main System Clocks

5.10.1 Main Clock

The main clock should operate at twice the recirculating clock frequency. It was decided to clock the registers at 3 MHz, hence the main clock is designed to operate at 6 MHz.

This multivibrator is built around two RTL inverters in the conventional manner.

5.10.2 Shift Clock

This clock is responsible for shifting data from the input buffer to the store and from the store into the output buffers. It is obtained from the main clock by a single dividing stage.

5.10.3 Synchronizing Clock

Since the word length is 5-bits there is a requirement for a synchronizing pulse to indicate the beginning and end of a word space. This is obtained by dividing the shift clock by five.

The complete clock system is shown in schematic form in Figure 5.10A and the resulting waveforms are shown in Figure 5.10B.

5.11 Input and Output Decision Circuits

5.11.1 Control Signals

The purpose of these circuits is to control the transfer of data in and out of the store. The Input Decision circuit contains the priority

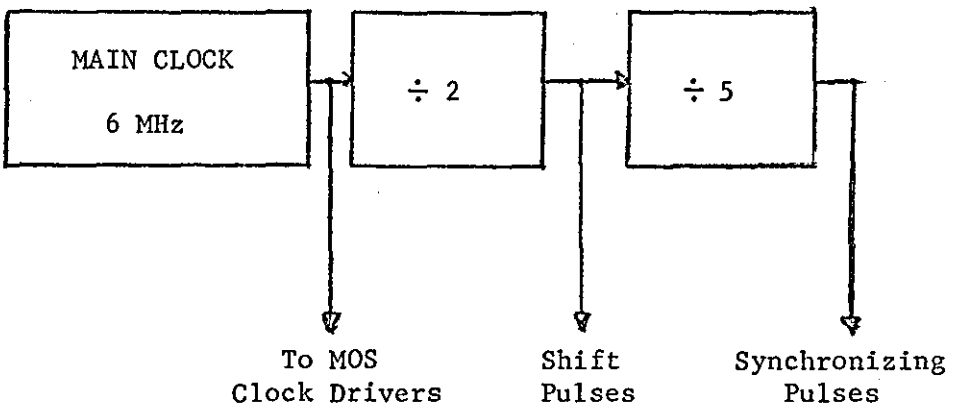


Figure 5.10A: Block Diagram of Main Clock System.

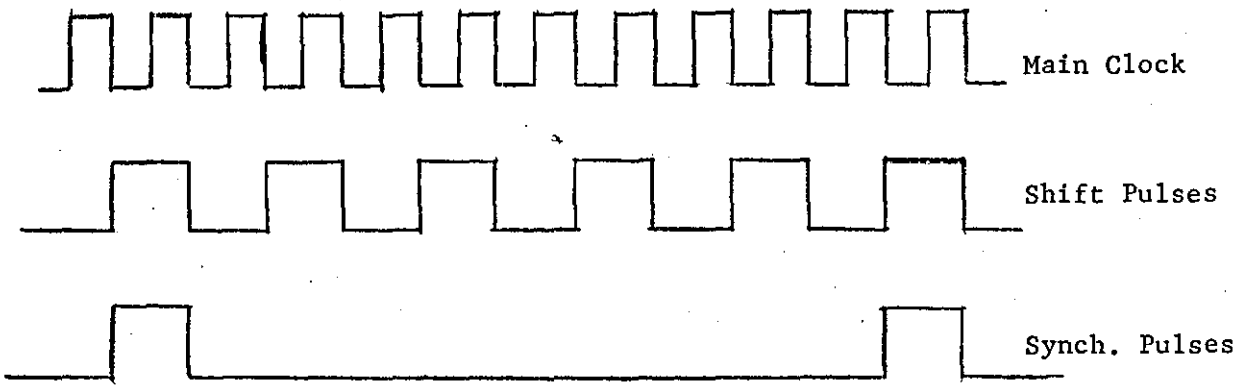


Figure 5.10B: Waveform Diagram of Clock System.

system which determines which target is to be discarded in the event of coincidence.

The circuits examine the output registers, the last position in the main store and the input registers. If there is a vacant output register and an occupied word space then that word is shifted out and any word in the input register is shifted in. Each word contains a Flag bit which is the fifth bit of the second range register. Hence examining this position at the synchronizing intervals will indicate the presence of a word.

If all registers are filled, then that word is recirculated and any word in the input register is held until the next word space.

If a new target arrives while the old target is still in the input registers or is being shifted out, then the new target is discarded.

By examining the TRUTH-TABLE of the system the requirements of this circuit can be clearly seen. The symbols used have the following meanings:-

FLAG - Single bit at the end of every word
FL = 1 implies word follows,

SYNC - Synchronizing pulse indicating the beginning of a word space,
SYNC = 1 implies beginning of word space,

MONITOR - Signal which indicates whether an output register is empty,
MO = 1 implies a vacant output register,

MARKER - Monitor which indicates whether the Input Buffer is occupied,
MA = 1 implies an occupied input register,

ACTIONS - OUT = 1 allows data to be shifted out of store

IN = 1 allows data to be shifted from Input Buffer into store

REC = 1 allows data to be put back into store

TRANS = 1 allows new data to be put into the Input Buffer.

TRUTH TABLE

SYNC	FLAG	MONITOR	MARKER	OUT	IN	REC	TRANS
0	X	X	0	-	-	-	1
0	X	X	1	-	-	-	0
1	0	0	0	X	0	X	1
1	0	0	1	X	1	0	0
1	0	1	0	X	0	X	1
1	0	1	1	X	1	0	0
1	1	0	0	0	0	1	1
1	1	0	1	0	0	1	0
1	1	1	0	1	0	0	1
1	1	1	1	1	1	0	0

By using a Karnaugh Map the minimized expressions become,

$$OUT = FL.\ SYNC.\ MO$$

$$IN = SYNC.\ MA\ (MO.FL + \overline{FL})$$

$$= SYNC.\ MA\ (OUT + \overline{FL})$$

$$REC = SYNC.\ FL.\ \overline{MO}$$

$$TRANS = \overline{IN} + \overline{SYNC.}\ \overline{MA}$$

The control signals OUT, IN and REC must be maintained for five or multiples of five shift pulses. To achieve this the control pulses are used to set individual Flip-Flops. The bistable is cleared by the next synchronizing pulse if the control conditions no longer exist. Hence the following pulses clear the bistables,

$$INC = \overline{IN}.\ SYNC$$

$$OUTC = \overline{OUT}.\ SYNC$$

$$RECC = \overline{REC}.\ SYNC$$

TRANS is obtained from the $\overline{Q}$ output of the IN Flip-Flop. Figure 5.11A shows the waveforms for a typical situation, and Figure 5.11B the circuit implementation.

5.11.2 Steering Circuits

These circuits, one for each register use the control signals derived above to steer the data from the store along the required path.

Figure 5.11C shows the circuit implementation.

5.12 The Output Buffer

These registers accept data from the main store at the recirculating clock rate. In this system three output registers are used, hence the complete bank of registers consists of 12 - 5 stage shift registers.

5.12.1 The Monitors

The state monitors inform the Input-Output Decision circuits when an output register is vacant. Each monitor detects the all zero states; the pulse MO is obtained by the function

$$MO = M1 + M2 + M3\ ,$$

where M1 = 1 when the first register is empty. The monitor circuits consider all 20 Flip-Flops as one register.

Figure 5.12 shows the implementation of one monitor using standard RTL gates.

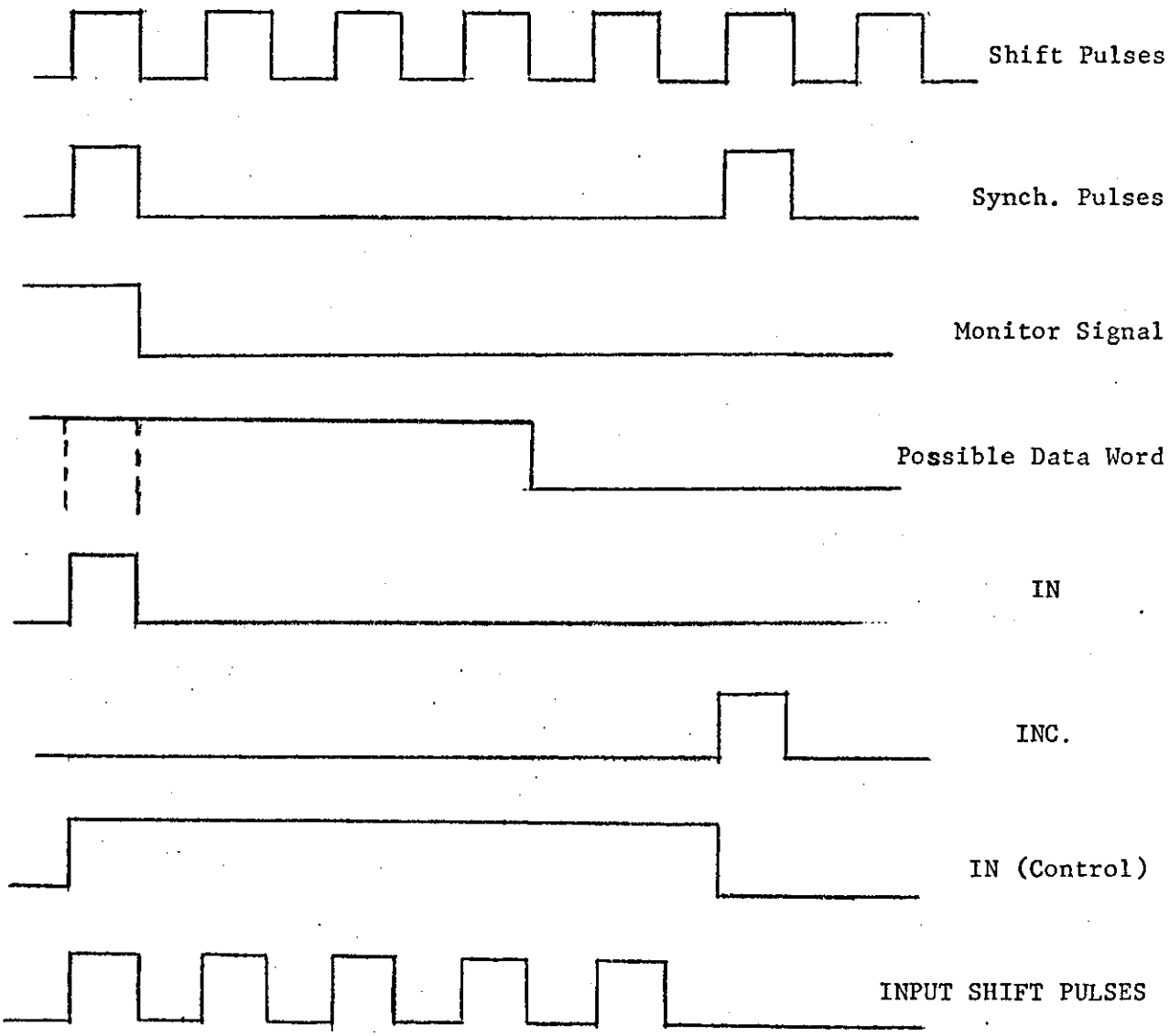


Figure 5.11A: Waveform Diagram for Input-Output Decision Circuits.

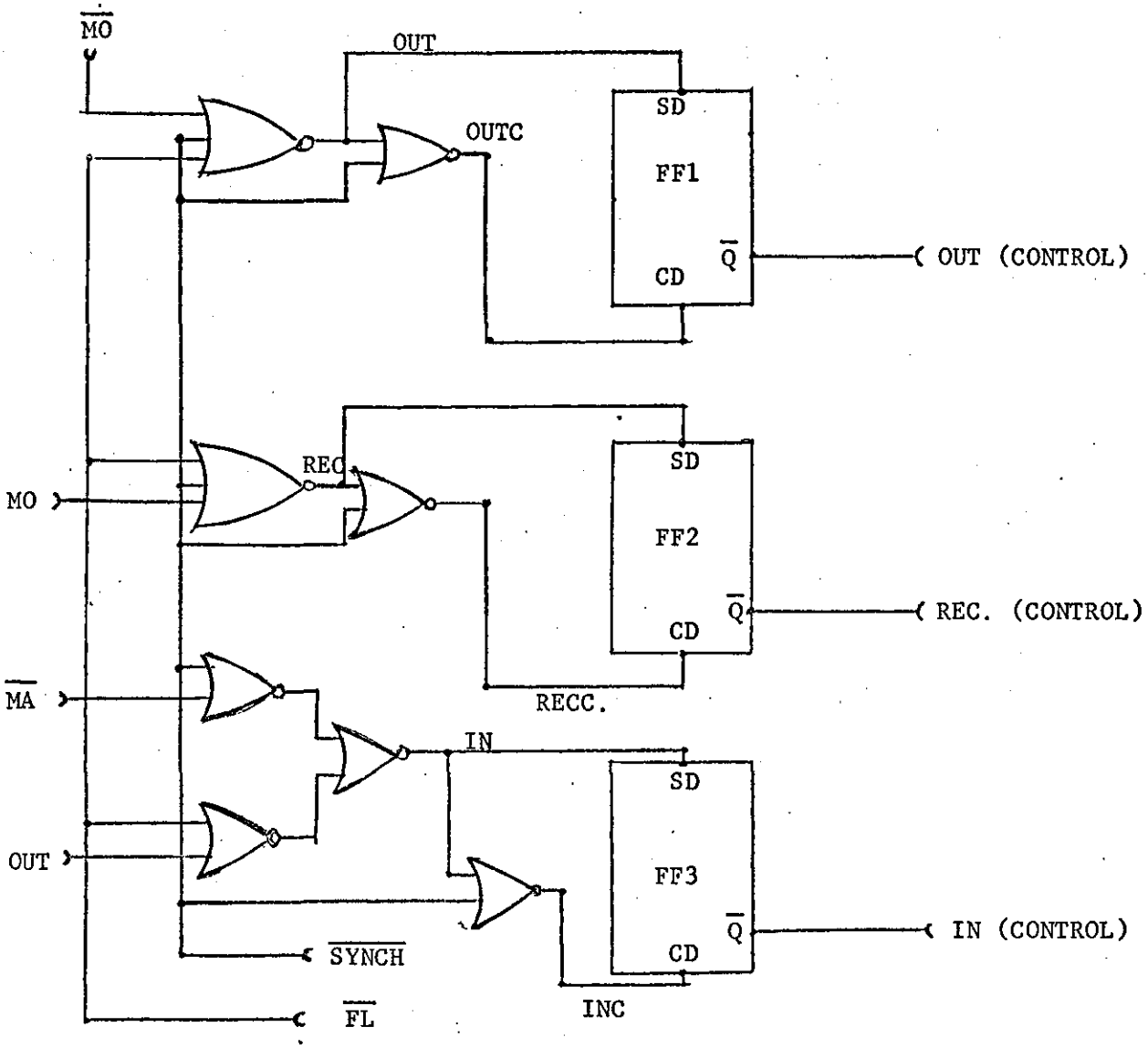


Figure 5.11B: Implementation of Input-Output Control Circuits.

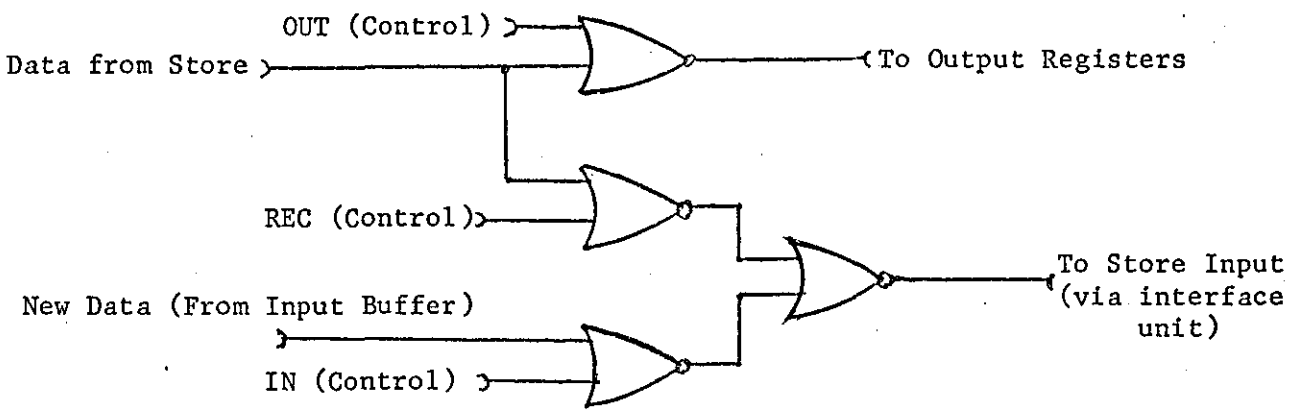


Figure 5.11C: Steering Circuit.

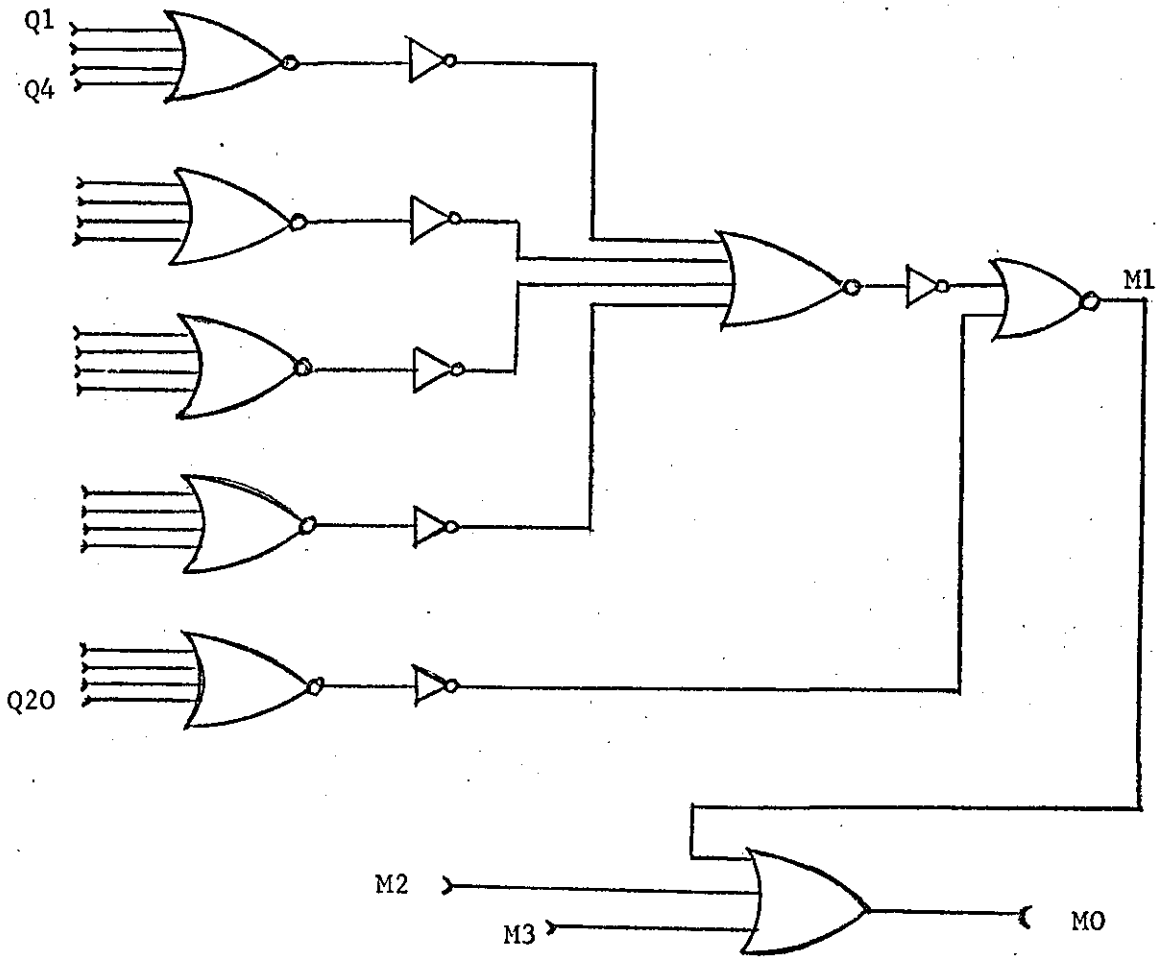


Figure 5.12: Circuit Implementation of State Monitor.

5.13 The Output Shift Circuit

5.13.1 Principle of Operation

This circuit examines all three output registers and decides which register will receive the data being shifted out. When the vacant register is selected, 5 shift pulses are produced which are applied to the selected register only. Hence although the information reaches all the output registers only one register receives the clock.

5.13.2 Logic Design

Each buffer is given a priority state and the shift action is determined in part by the priority state of the buffer. Here Register 1 is the highest priority buffer and Register 3 the low priority buffer. The TRUTH-TABLE of the operation is shown overleaf. The symbols used have the following meanings;

FLAG = Single bit at the end of every word
FL = 1 indicates presence of data.

M1 = 1 indicates that Register 1 is empty

M2 = 1 indicates that Register 2 is empty

M3 = 1 indicates that Register 3 is empty

The symbols in the ACTION column indicate which register will receive the data.

TRUTH TABLE

FLAG	M1	M2	M3	ACTION
0	X	X	X	-
1	1	1	1	CLOCK 1
1	1	1	0	CLOCK 1
1	1	0	1	CLOCK 1
1	1	0	0	CLOCK 1
1	0	1	1	CLOCK 2
1	0	1	0	CLOCK 2
1	0	0	1	CLOCK 3

From the Truth Table it is seen that the following control signals would initiate the required shift action.

CLOCK 1 = FL. M1

CLOCK 2 = FL. M2. $\overline{M1}$

CLOCK 3 = FL. M3. $\overline{M2}$. $\overline{M1}$

Now these control pulses must be maintained for five shift pulses. Figure 5.13A shows the method used for obtaining these shift pulses and Figure 5.13B shows the resulting waveforms. It should be noted that these shift pulses are a delayed version of the input shift pulses. This modification is introduced to ensure synchronism between the two sets of shift pulses. During circuit tests it was found that due to propagation delays through the RTL and interface circuits the signals CLOCK 1, 2 and 3 were not coincident with the synchronization pulse. The data are therefore subjected to a further one bit delay to restore synchronism with the output shift pulses. Figure 5.13B shows the waveforms of the complete process.

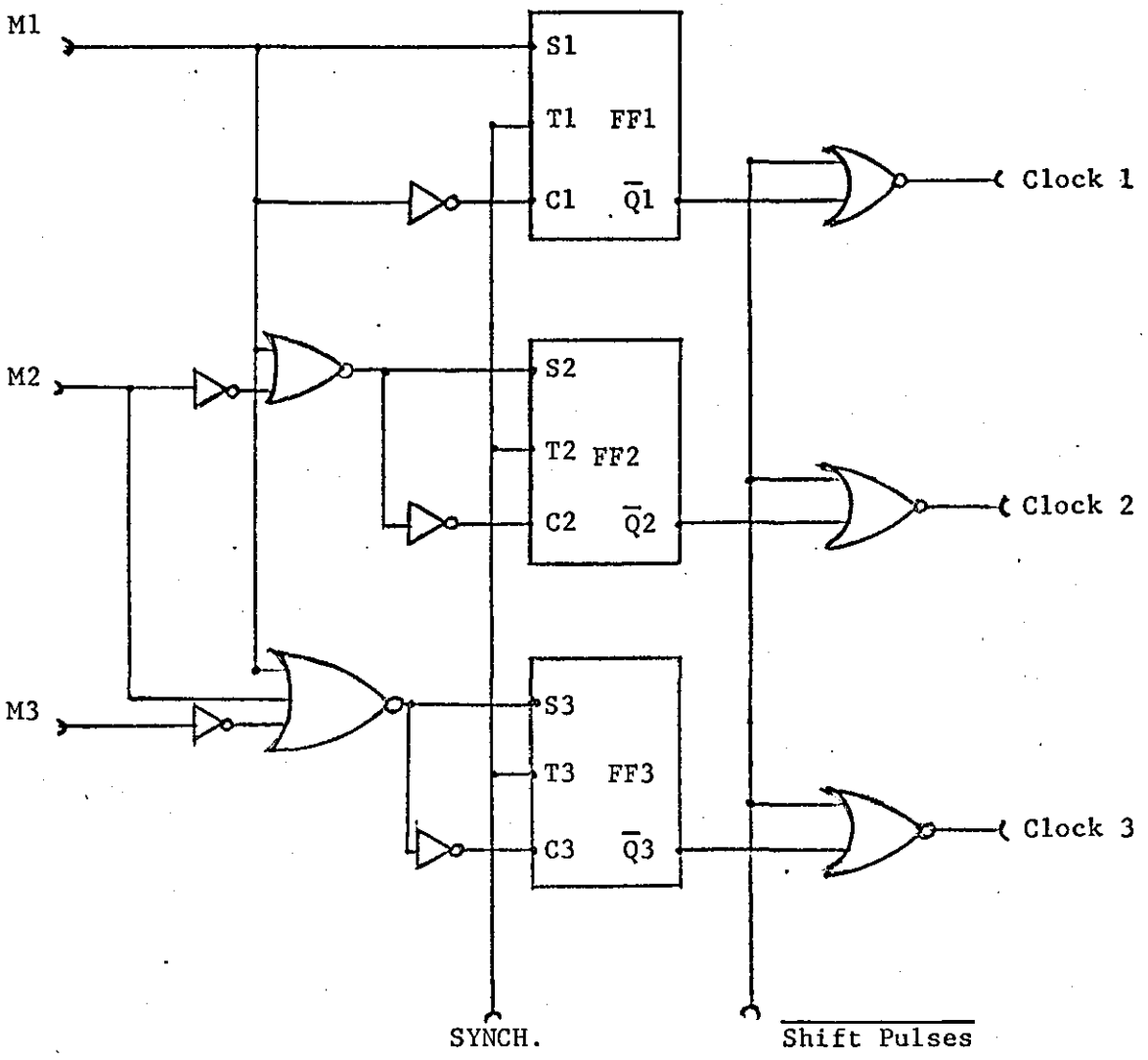


Figure 13A: Implementation of Output Shift Pulses Generator.

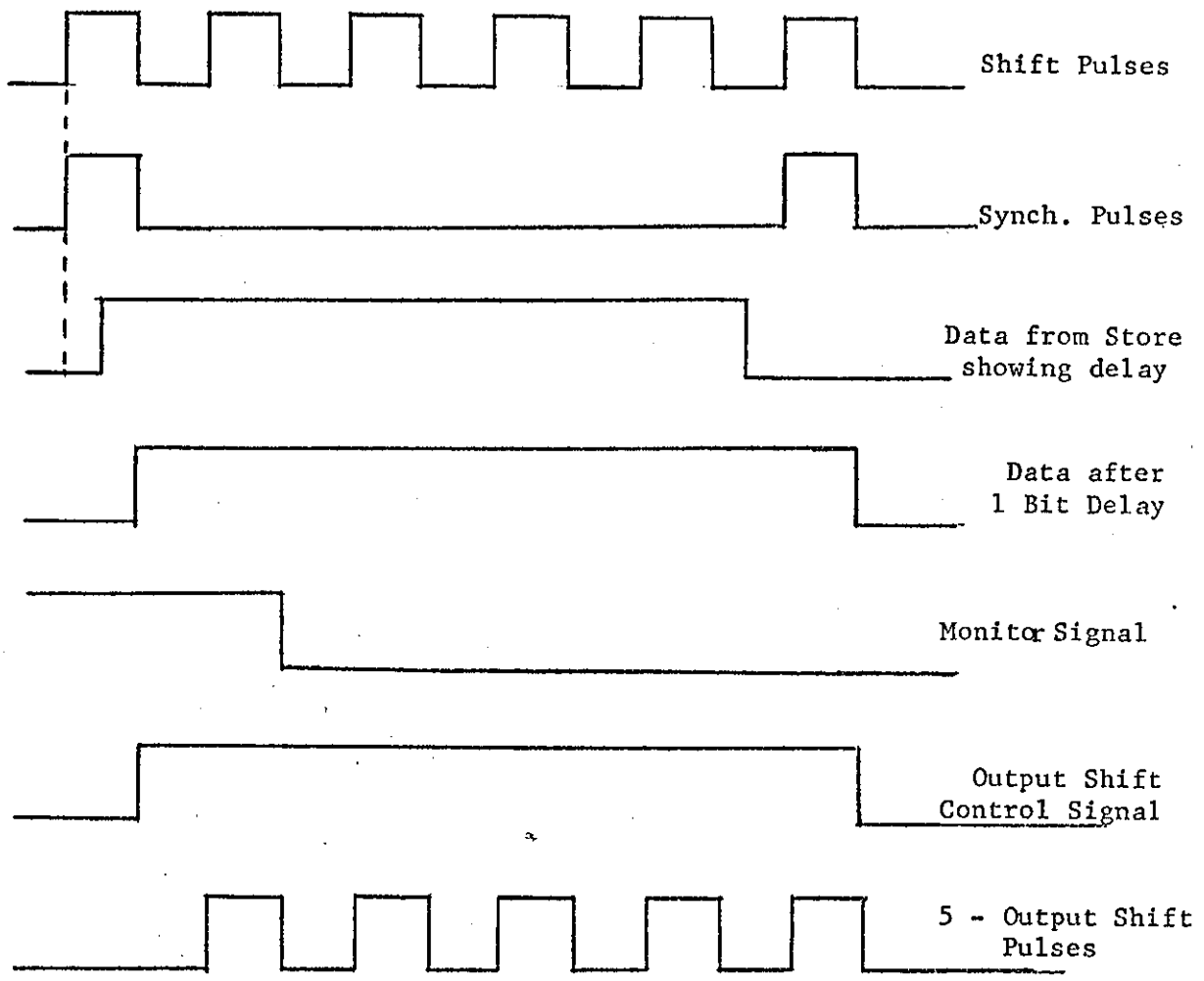


Figure 5.13B: Waveforms showing the production of the 5 - Output Shift Pulses.

5.14 The Output Clock

The Output Clock controls the transfer of data from the output registers to the transmission channel. In this system the channel is assumed, hence transfer is made directly to the decoding circuit in parallel.

The output clock is obtained by dividing down the main clock. Several stages of division are done to test the systems performance over a range of output rates.

The circuits are of the conventional form and are built from TTL JK Master Slave Flip-Flops (SN 7473).

5.15 Output Transfer Circuit

5.15.1 Principle of Operation

This circuit controls the transfer of data from the output registers to the decoder. The same priority system is used as with the Output Shift circuit. Hence, Register 1 is first examined. If this register is filled then the next output clock pulse will transfer the 17-bit word to the Decoder. In order to simulate the entire output interval the data are kept in the buffer until just before the next service interval. In the operational system the data would most likely be shifted out serially into a single channel. The output registers would therefore be cleared automatically at the end of the last shift pulse. In this system a pulse is generated at this time to clear that channel only.

If Register 1 is empty control is passed to Register 2 and a similar process occurs.

5.15.2 Logic Design

5.15.2.1 Transfer Pulses

The output registers accept the 20 bits in the original encoded pattern. Hence the Flag bit is always the last bit in the second range register. The presence of the Flag in this Flip-Flop therefore signifies the occupancy of the entire register. Since the Flag bit is the last bit to be received in its train of five bits then there can be no false indication.

The Truth Table of the process shows the action taken under the various conditions. The symbols have the following meanings:-

FL1 = 1 indicates the presence of the flag in Register 1 and so on.

OC = 1 indicates the presence of the output clock pulse.

Action T1 indicates that the transfer pulse is applied to Register 1.

TRUTH TABLE

OC	FL1	FL2	FL3	ACTION
0	X	X	X	-
1	0	0	0	-
1	0	0	1	T3
1	0	1	0	T2
1	0	1	1	T2
1	1	0	0	T1
1	1	0	1	T1
1	1	1	0	T1
1	1	1	1	T1

The following control pulses will satisfy the system requirements.

$$T1 = OC.\ FL1$$
$$T2 = OC.\ FL2.\ \overline{FL1}$$
$$T3 = OC.\ FL3.\ \overline{FL2}.\ \overline{FL1}$$

Figure 5.14A shows the implementation of this circuit using RTL gates. Seventeen such circuits are needed for each bit of data.

5.15.2.2 Clear Pulses

In order to clear the output registers at sometime just after the negative going edge of the twentieth output shift pulse, a pulse must be produced just before the pulse OC. In addition, this pulse should clear only the register just emptied.

Figure 5.14B shows the waveforms illustrating this process. The clear pulses are obtained from the pulses T1, T2 and T3. This ensures that only the register just transferred is cleared. The relevant pulse is delayed by one output clock period. By gating the resulting waveform with a pulse A^1 obtained from the output clock the clear pulse is obtained. Since data are shifted in at the recirculating clock rate, the clear line is activated for a maximum of one recirculating clock pulse only.

Figure 5.14C shows the circuit implementation using RTL gates and Flip-Flops.

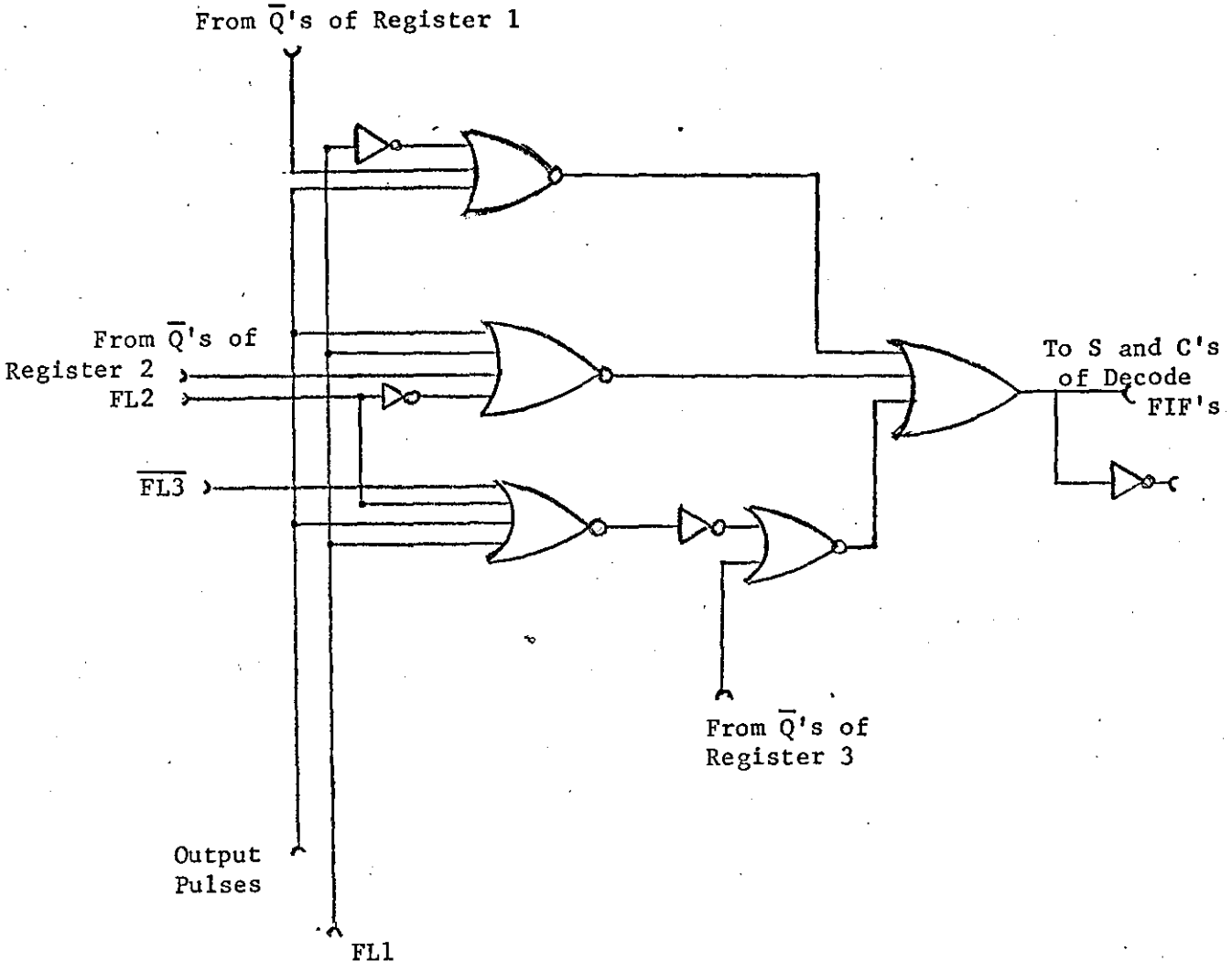


Figure 5.14A: Circuit implementation of Output Transfer Circuit.

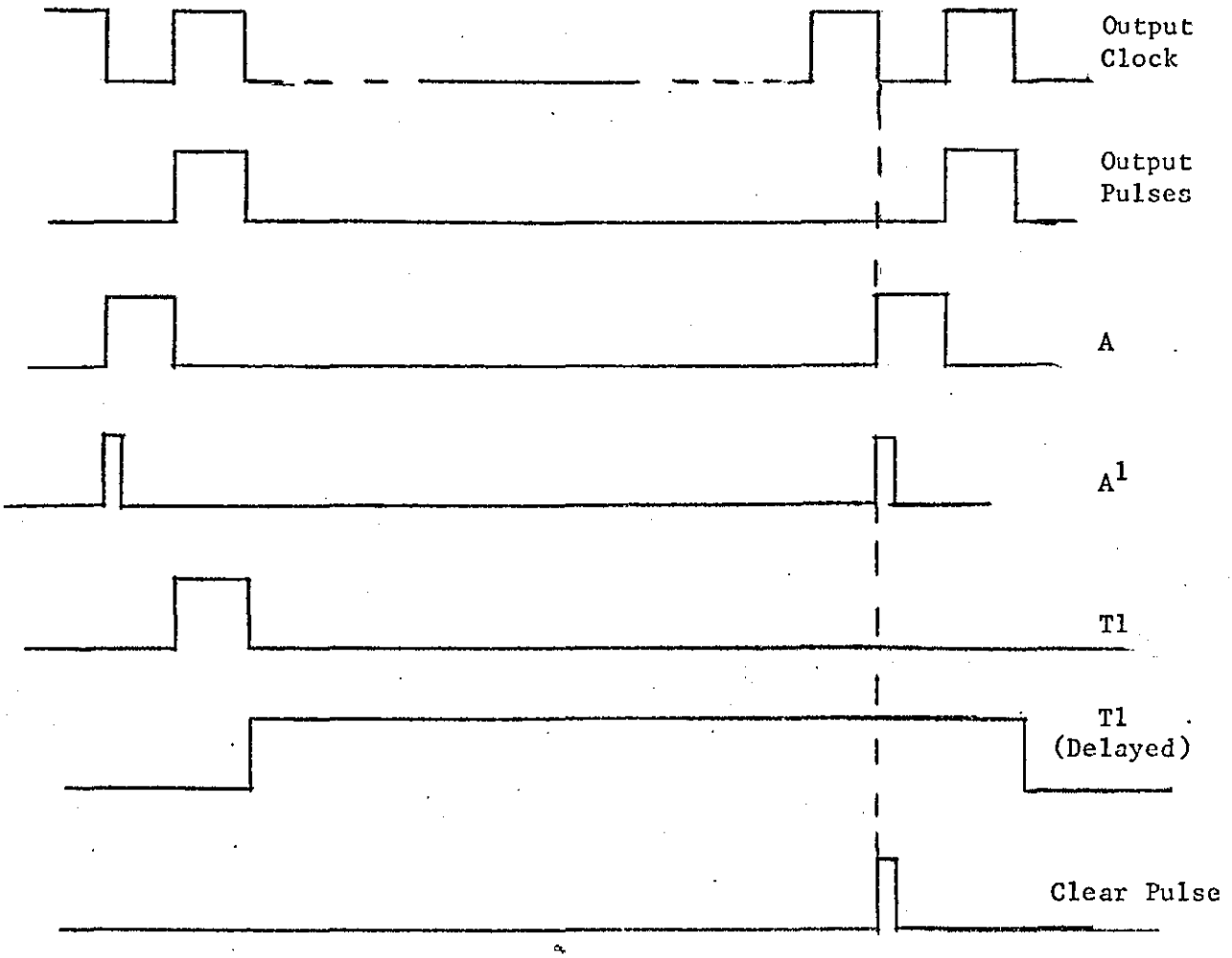


Figure 5.14B: Waveform diagram showing production of clear pulses.

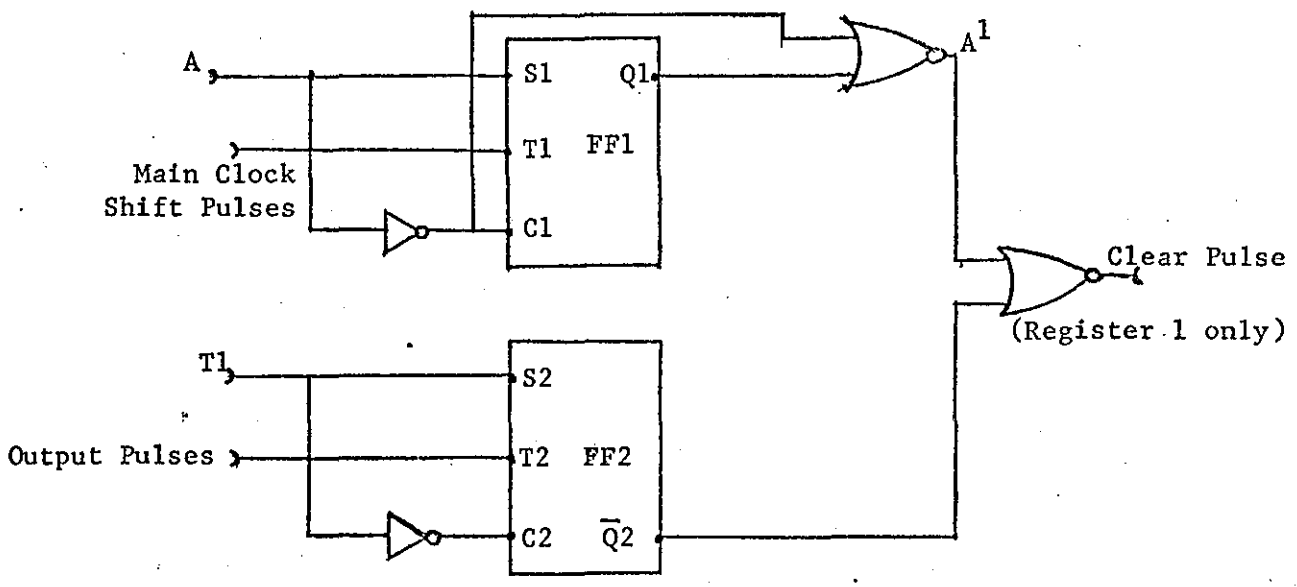


Figure 5.14C: Circuit implementation of Clear Pulse process.

5.15.2.3 Manual Clear

When the system is first switched on the bistables in the output registers can be in any state. Since the operation of the automatic removal system depends on the presence of the flag bit in the expected position a manual starting pulse is needed. To ensure proper operation a manual "push-to-make" switch is included to clear all the output buffers. This can also be used to restart the system in the event of momentary failures. The manual signal is "0 Red" with automatic clear signal.

5.16 The Decoder

5.16.1 Principle of Operation

The decoder accepts a 17-bit word from one of the output register. The three bits representing the run length are separated from the co-ordinates information. This co-ordinate represents the last position in a run and is first stored in a 14-stage down-counter. If the run length word is 000, indicating a single run, then this coordinate is transferred directly to the Digital-to-Analog Converter (D-to-A) and no further decoding is necessary. If the run length word is 001 indicating two targets in the run, then the first co-ordinate is displayed and one shift pulse is produced which clocks the co-ordinate down counter. Hence for a run of n targets n-1 shift pulses are produced. These pulses are obtained from the output clock and the number of pulses produced is determined by the Run Length Decoder (RLD) circuit.

Figure 5.15A shows in schematic form the main elements of the Decoder.

5.16.2 Decoder Shift Pulses

Since the maximum number of runs per output period is eight, the output period is divided into eight equal intervals. The main output clock is designed to shift a 20-bit word during the output period. Hence, to produce 8 shift pulses within the output period necessitates dividing the main output clock by $2\frac{1}{2}$.

This division process is achieved by manipulating the outputs of a divide-by-ten counter used in producing the output pulses. This device, (the SN7490 divide-by-ten counter) produces the waveforms shown in Figure 5.15B at its output pins. By forming the functions

$$X = \overline{A}.\ B.\ \overline{Clock},$$

and

$$Y = C.\ Clock,$$

the divide by $2\frac{1}{2}$ waveform is obtained by the expression $Z = X + Y$ as shown in Figure 5.15B.

5.16.3 The Run Length Decoder

This section of the circuit controls the clocking of the co-ordinates down-counter and hence the number of targets displayed. The three bits of information are stored in a 3-stage register. At the moment of transfer a 3-stage binary counter is cleared. The comparison circuit consists of three EXCLUSIVE - OR gates plus additional gates which combine to give a control signal whenever the contents of both the run length store and 3-stage counter are similar. Hence, if the target run is of length one, at the moment of transfer the comparison would be complete and the control pulse would be produced. This pulse is used

to inhibit the shift pulses, hence the requirement is satisfied in that for a run of n only n-1 shift pulses are produced.

Figure 5.15C shows the waveform diagram for a run of three targets and Figure 5.15D shows the circuit implementation using TTL devices.

5.16.4 The Co-ordinate Counter

This counter is a 14-stage down-counter whose Preset and Clear inputs are connected to the corresponding outputs of the output registers. A down counter is necessary since this co-ordinate is the last position of a run. The Q outputs of the counter are taken directly to the D-to-A converter as shown in Figure 5.15E.

5.17 The Digital-to-Analog Converter

This D-to-A converter transforms the co-ordinate data to analog voltages which are used to deflect the spot of a cathode ray tube. The only constraint on its design is that it should be able to do eight conversions within the output period. It is anticipated that this system will be operable with an output period of about 50 microseconds. This would mean an available conversion time of about 6 microseconds. This figure is well above the conversion time of even low accuracy converters.

Figure 5.16 shows the converter for the Most Significant Bit (MSB) of bearing data and the two MSB's of range data.

The design approach is discussed in Appendix 5.

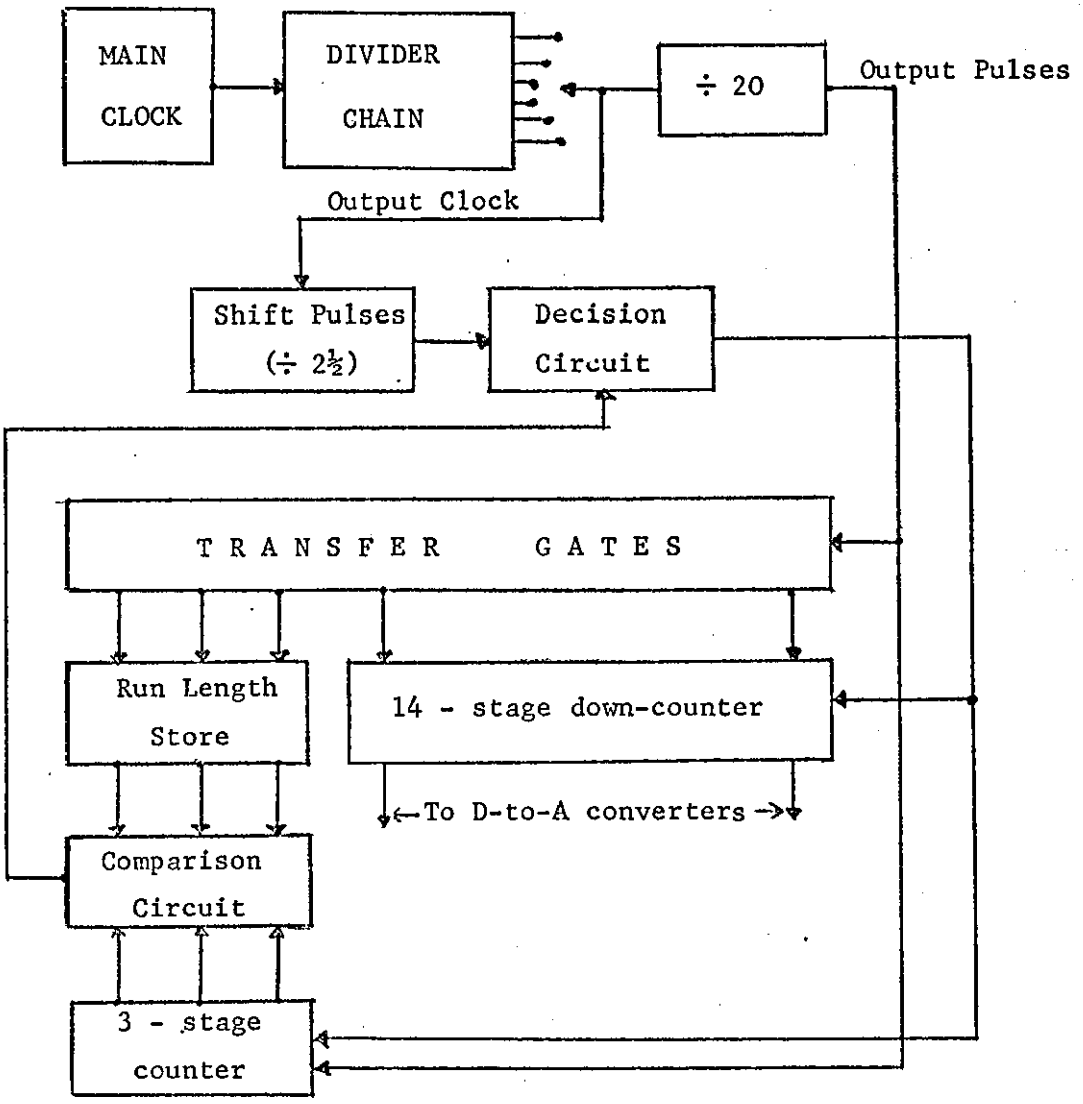


Figure 5.15A: Block Diagram of Output Decoder.

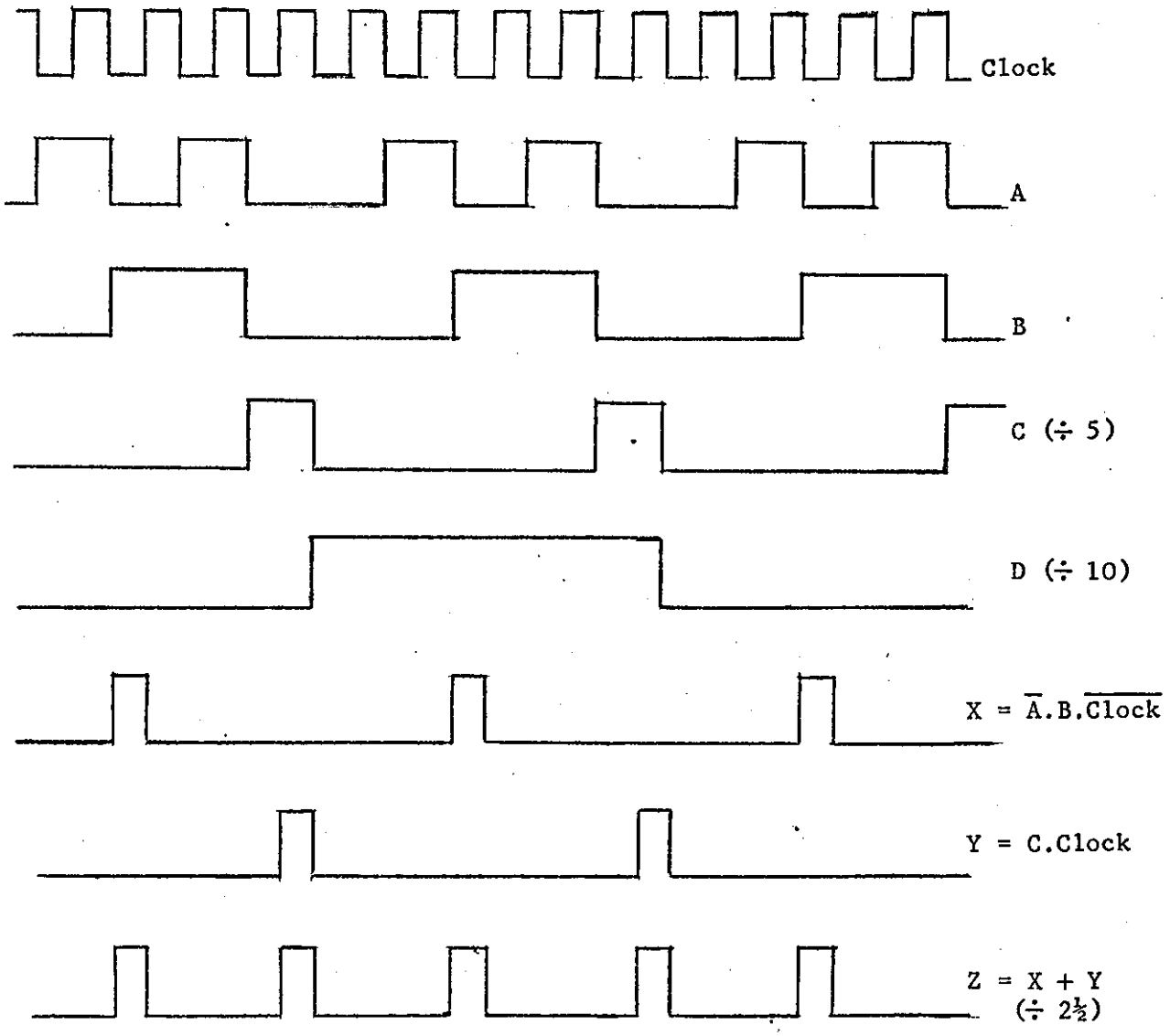


Figure 5.15B: Waveform Diagrams for performing the Divide-by-2½ operation.

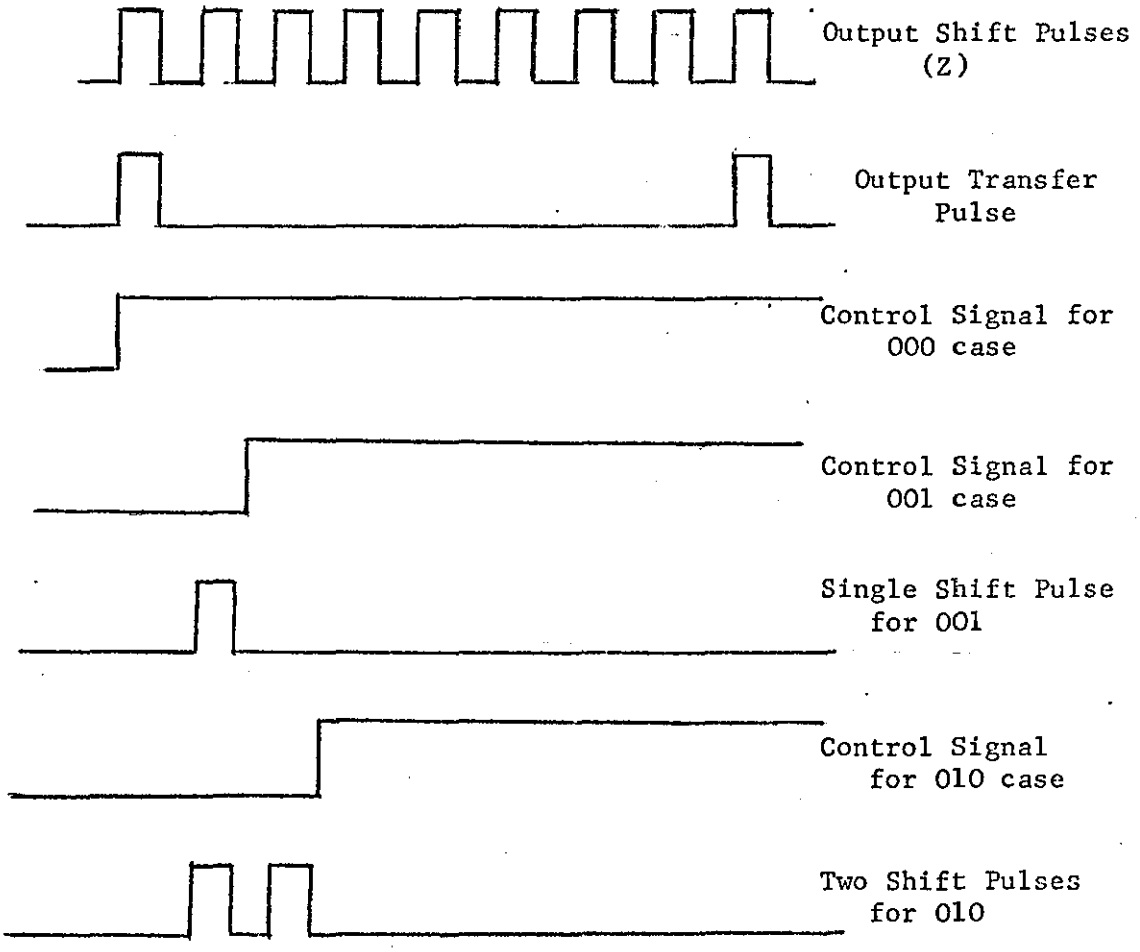
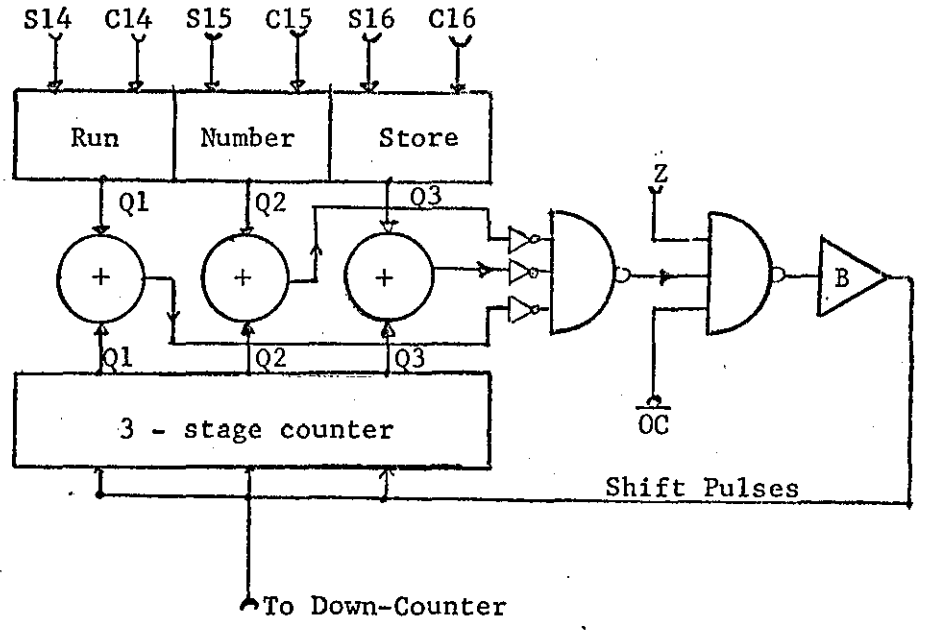


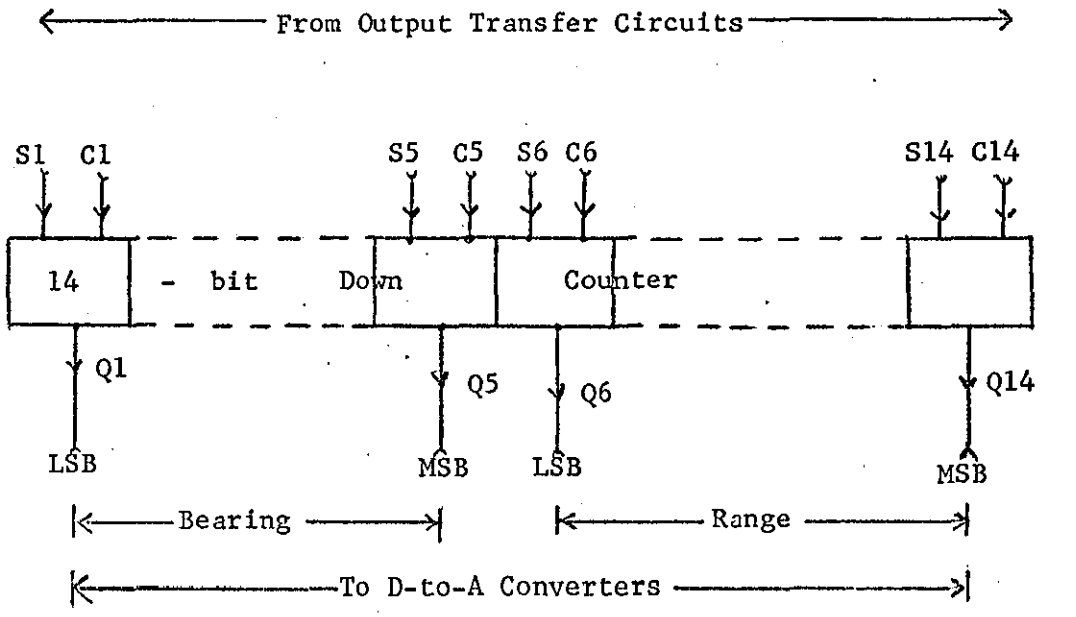
Figure 5.15C: Waveform diagram showing operation of Decoder Circuit.



Exclusive - OR gates - SN 7486
3 - input NAND - SN 7410
Buffer - SN 7440

Figure 5.15D: Circuit implementation of Decoder.

Figure 5.15E: Block Diagram showing organization of 14-bit Down-Counter



Flip-Flops used in Down-Counter -SN7476

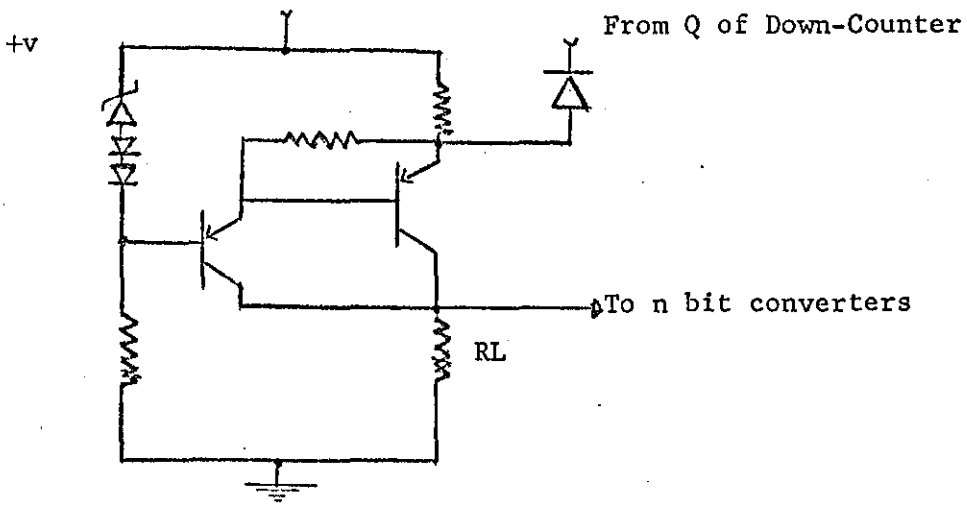


Figure 5.16: Circuit diagram of single bit converter of Digital-to-Analog converter.

5.18 The Display

The specifications of the Display are fairly standard. A Solatron oscilloscope fitted with a long persistence tube was used throughout all experiments.

5.19 Auxillary Circuits

5.19.1 Output Registers Selector

In order to investigate the effect of varying the number of output registers a manual switch is included in the system. This switch selects the number of registers used during experiments.

Figure 5.17A shows the circuit used.

5.19.2 Bright-up Pulses

These pulses are required to modulate the spot on the cathode ray tube such that the transitions to and from co-ordinates are not visible.

The bright-up pulse for each position is obtained just after the D-to-A converter has settled. An appropriate time is just after the counter shift pulses have been applied; in the case of the single target just after the output transfer pulse is applied. Figure 5.17B shows the waveforms diagrams for this process and Figure 5.17C the circuit implementation.

5.19.3 Target Count - In

These pulse are required to indicate the number of targets originating from the source. They are taken from the Target Detected circuit and gated with display clocks for counting purposes.

5.19.4 Target Count - Out

Since a bright-up pulse is generated for every D-to-A operation these pulses provide a convenient count of the number of targets displayed.

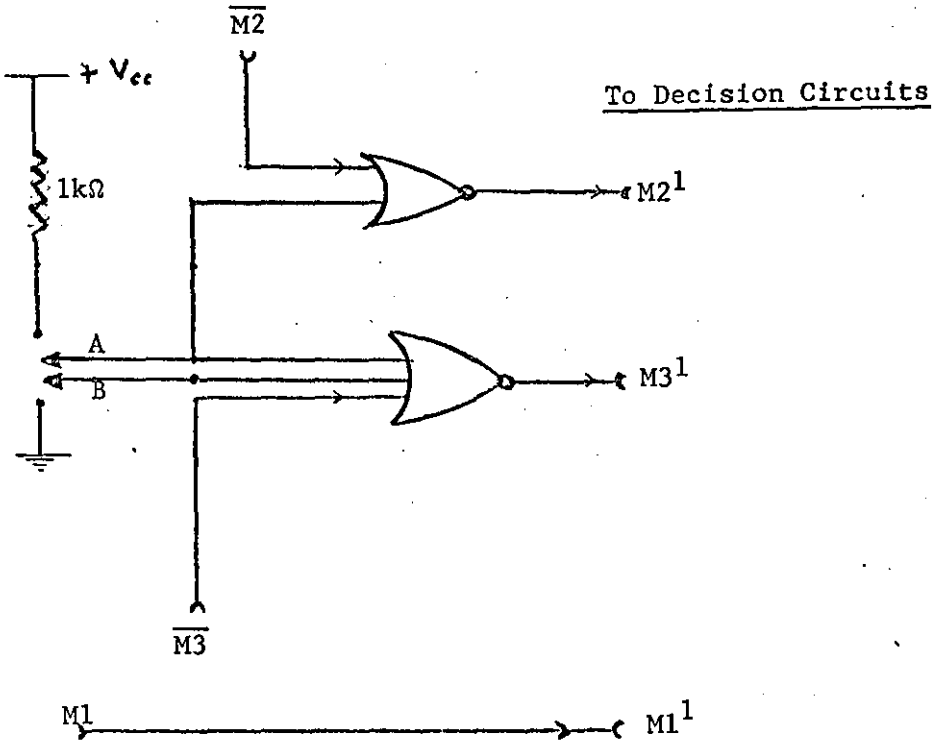


Figure 5.17A: Circuit Implementation of Output Registers Selector.

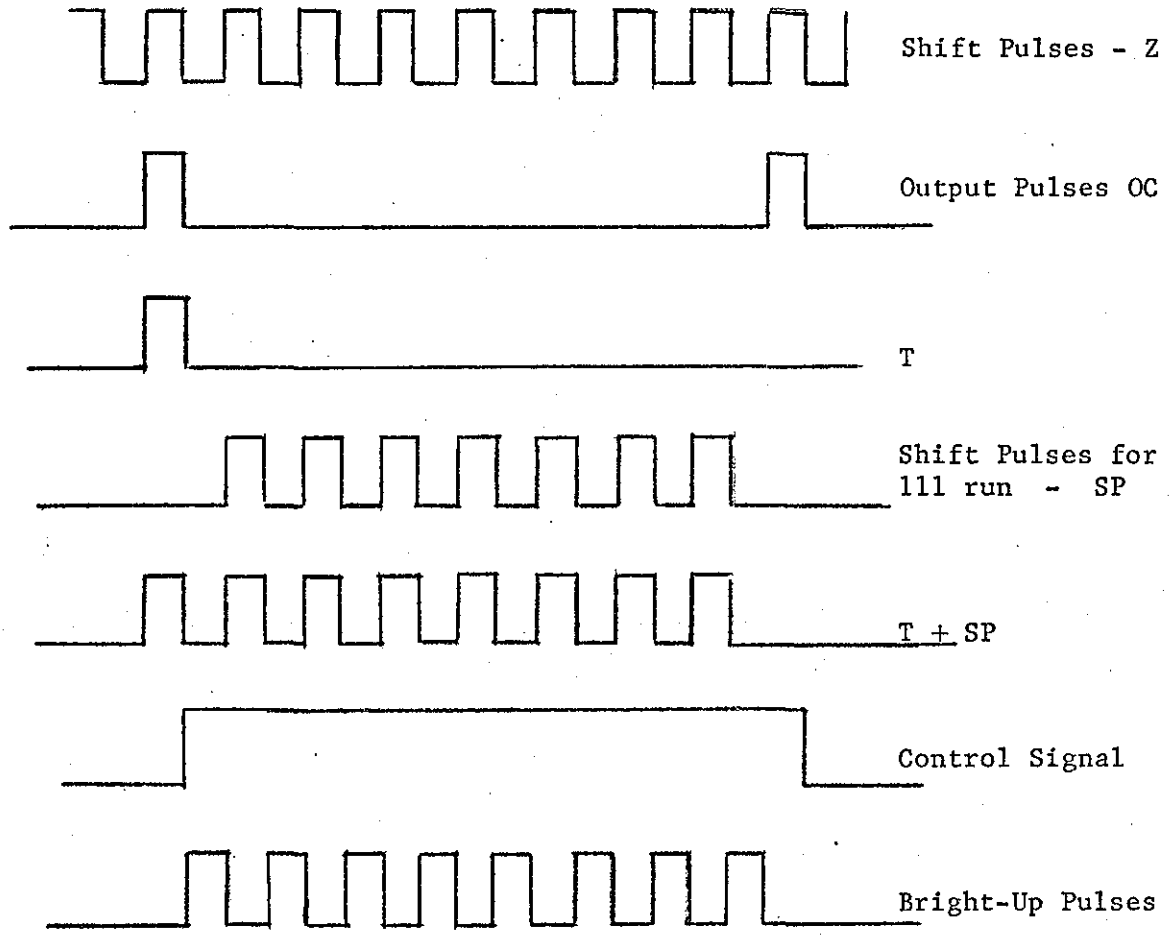


Figure 5.17B: Waveform diagram for Bright-Up Pulse generation.

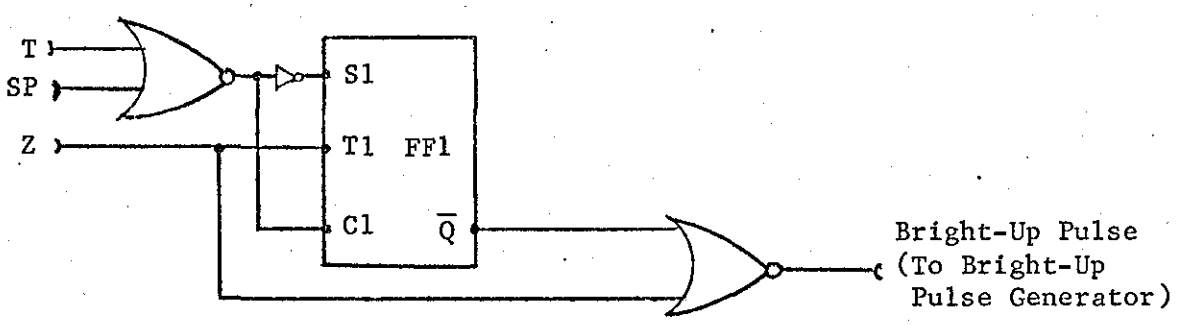


Figure 5.17C: Bright-Up pulse circuit.

REFERENCES: CHAPTER 5

1. Parker P.: "A High Resolution Sonar Target Simulator".
B.Sc. Project Report, Loughborough University of Technology, June 1968.

2. Culshaw R.M.: "A Target Simulator for a High Resolution Sonar Display".
B.Sc. Project Report, Loughborough University of Technology, April 1972.

CHAPTER 6

SYSTEM PERFORMANCE

6.1 Introduction

The performance of the complete system was investigated with the video signals provided by the simulator. The success of such a system depends eventually on the response of the human observer; however, a quantitative appraisal is necessary for the purposes of comparison.

The experiments conducted tested the system's performance when simple shapes are scanned, then tests on more complex shoal-like shapes were processed. For all tests the number of output registers, the output rates and the coding methods were varied.

Photographs of selected patterns are also included in this report.

6.2 Output Clock Frequencies

The output clock rate will be determined mainly by the channel capacity available. The method of transmission is immaterial as far as this system is concerned since the signal from the D-to-A converters could be filtered and transmitted as analog signals. Alternatively the signal could be transmitted by digital means.

This system has been tested with clock rates from 8KHz to 550 KHz, which is equivalent to target removal rates of 20 to about 5000 targets per frame. With most frames having in the region of 1200 targets, the lower removal rate produces a very high traffic intensity. The higher

rate produces a traffic intensity of about 0.2. In most designs a value very close to 1 is preferred, hence a target removal rate of the order of 1500 per frame should be catered for.

This aspect of the system has been left open until the method of transmission is selected.

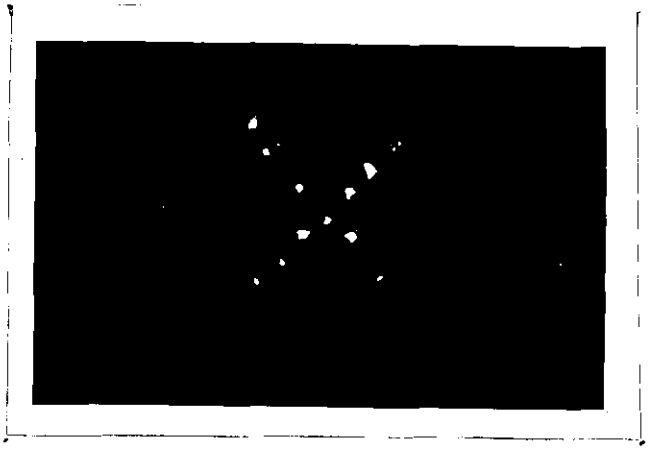
6.3 Preliminary Tests - Simple Shapes

The system was first tested by simulating the "all ones" situation, that is the occurrence of a target in every cell. This served as a convenient means of checking the key sections of the system. This test produced signals which covered the entire display. The tests confirmed the proper operation of the system.

Simple shapes processed included a "T" and an "X". The displays produced by scanning the figure "X" are reproduced in Figures 6.1 to 6.4. These displays represent both run-length coded and non-coded operations.

The photographs were recorded with a Polaroid Land Camera operating at f8 for 1/60th of a second. The pictures recorded do not represent accurately the observations made as the limitations of the camera does not allow it to record the integrating effect due to visual perception and phosphor persistence. In fact the displays produced recognizable shapes even at the lowest output rate.

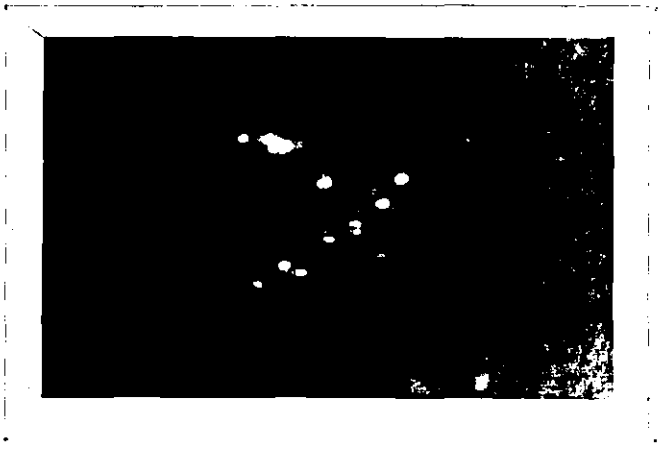
The main observation is that the run length coding procedure has little effect on the display. This is to be expected since the target distribution is such that the non-coded method is just as effective.



Original

Output Period 2.3 milliseconds

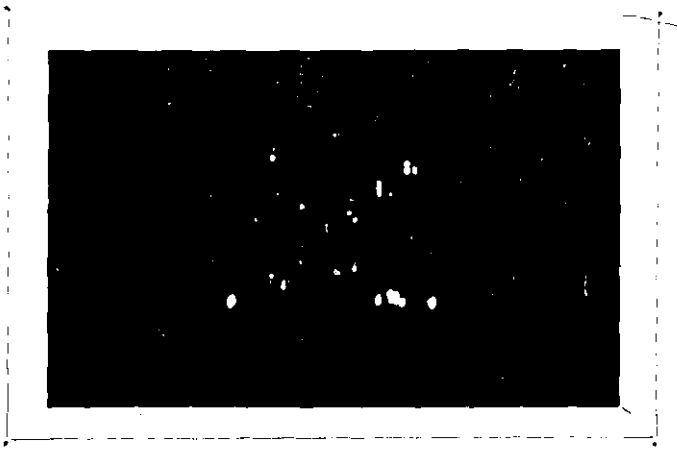
No Run Length Coding



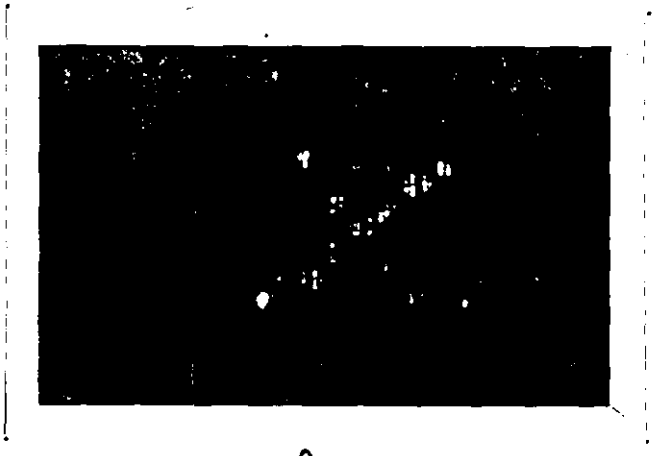
Output Period 1.15 milliseconds

No Run Length Coding

Figure 6.1: Records of Output Display with Pattern "X" as input.

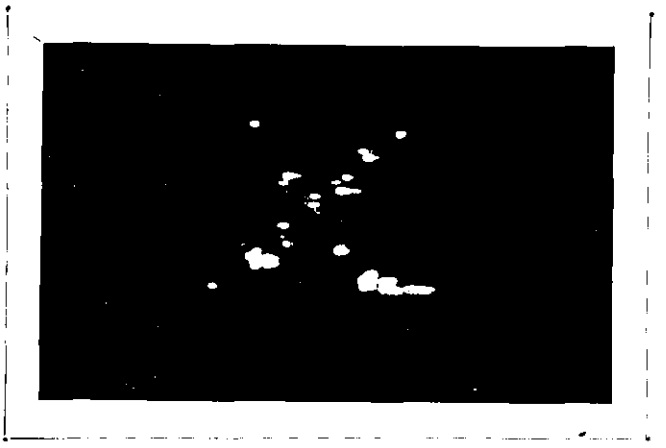


Output Period 5·80 μs



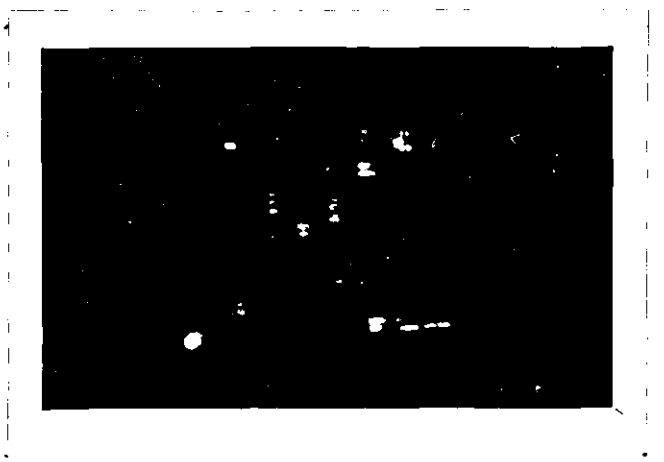
Output Period 145 μs

Figure 6·2 "X" Outputs - No Run Length Coding



Output Period 2.3 milliseconds

Output Period 1.15 milliseconds



Output Period 580 microseconds

Figure 6.3: "X" Outputs - with Run Length Coding.

Output Period 145 microseconds

Figure 6.4: "X" Output - with Run Length Coding.

6.4 Complex Shapes

Several experiments were conducted on more complex shapes. The effect of the run-length coder was more apparent in these experiments. Figures 6.5 to 6.8, show photographs of a typical pattern processed. Again the photographic recording technique underates the true performance of the system especially at the lower output rates. However, even though the loss of data was apparent to observers a fairly accurate estimate of the shapes could be made without any prior knowledge of the original pattern.

Only a section of the original pattern is displayed due to the resolution restrictions of the simulator lens system. However, by adjusting the position of the film,different sections could be scanned and the entire shape estimated.

6.5 Data Losses in Experimental System

By counting the number of targets generated during each frame interval and counting the number of target displayed in the same interval a quantitative estimate of data losses was made.

Table 3 shows the figures obtained when processing a pattern occupying 630 target cells. The output clock was obtained by a series of division stages from the main shift register clock.

The numbers indicated in the table represent the total number of targets counted. These figures were averages taken of several readings for each value.

TABLE 3

NUMBER OF TARGETS DISPLAYED

	1 Register		2 Registers		3 Registers	
Output Period	C	NC	C	NC	C	NC
2.3ms	60	28	75	32	85	32
1.15ms	120	52	135	58	145	60
580.00μs	150	75	165	80	180	170
290.00μs	280	140	300	150	320	140
145.00μs	430	220	450	240	460	240
72.50μs	540	350	570	370	580	380
36.25μs	580	400	600	440	620	420

C = Run Length coding applied

NC = No Run Length coding

The main observations to be made are:-

1. The effectiveness of the run length coding method is obvious for all values.

2. These figures indicate only a slight improvement in performance as the number of output registers is increased. The slight improvement in using 3 registers over that while using 2 confirms the results of the simulation tests with the synthetic inputs. Further tests conducted with more concentrated inputs showed a greater deviation between the single and double register case but still only a marginal improvement when the third register is introduced. In one test with a 2000 targets pattern, the average output figures for the non-coded case were 1100, 1350, 1370 respectively.

3. The fractional data loss is very high for the lower output rates. However, only the last two output rates need to be considered as these values provide the only realistic traffic intensities from which comparisons can be made. For an output period of 72.5 microseconds the target removal rate is approximately 640 targets per frame and for 36.25 microseconds, 1280 targets per frame. The respective traffic intensities are approximately 1 and 0.5. The fractional data losses are 0.38 and 0.30; the equivalent figures from the simulations are 0.48 and 0.22. Subsequent tests with other input distributions produced figures of the same order of magnitude. With run length coding the fractional data losses are 0.08 and 0.16, however, the tests indicated that the observers could not distinguish between these two situations.

6.6 Conclusion

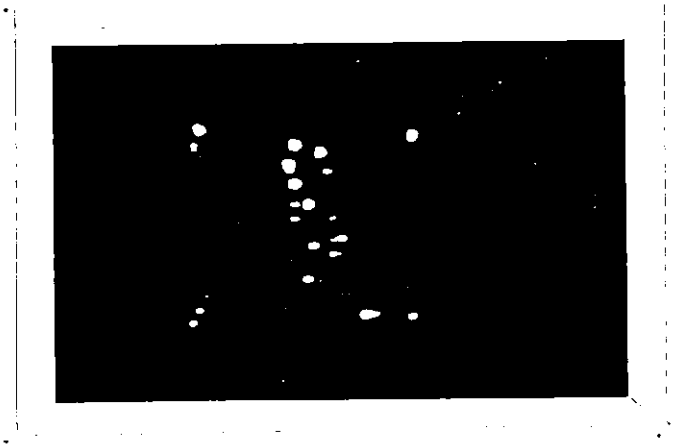
6.6.1 Performance of Recirculating Store

All phases of the project have confirmed the original assumption that this method of storage would produce an acceptable display even for high data losses. The analysis demonstrated the relative insensitivity of the buffer to data bursts; hence even though the losses are comparatively high, the variations are small for varying traffic intensities. Both the simulated and experimental displays demonstrate the effects of coincidence losses whereby a recognizable displays is evident even for high losses.

Hence it is suggested that this storage approach provides a cheap and effective bandwidth compression buffer for low priority systems

Original Pattern Processed

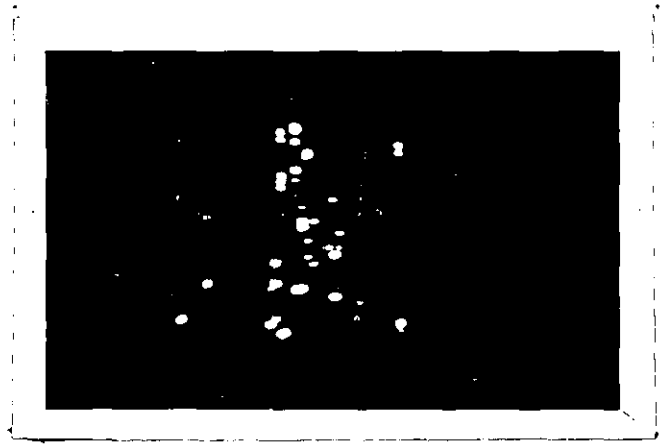
Note:- Only the lower section of the circular inset is reproduced in the output patterns.



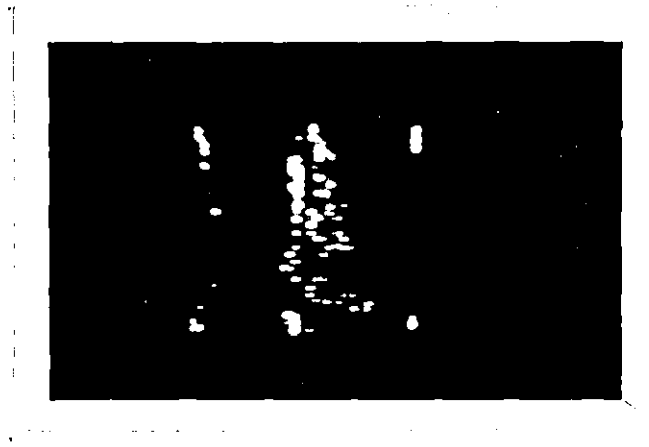
Output Period 2.3 milliseconds

No Run Length Coding

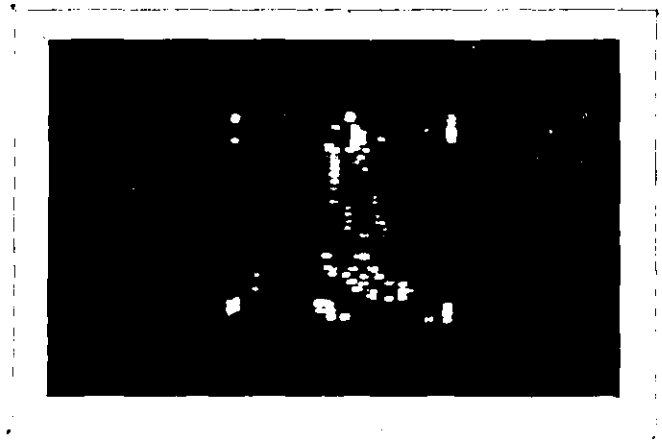
Figure 6.5: Reproduction of Shoal Patterns.



Output Period 1.15 milliseconds

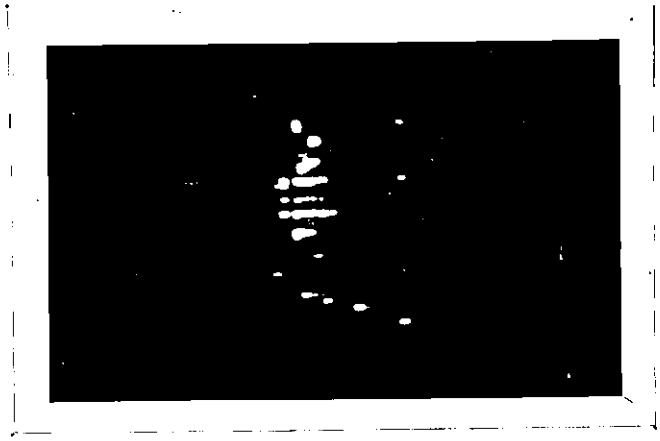


Output Period 580 microseconds

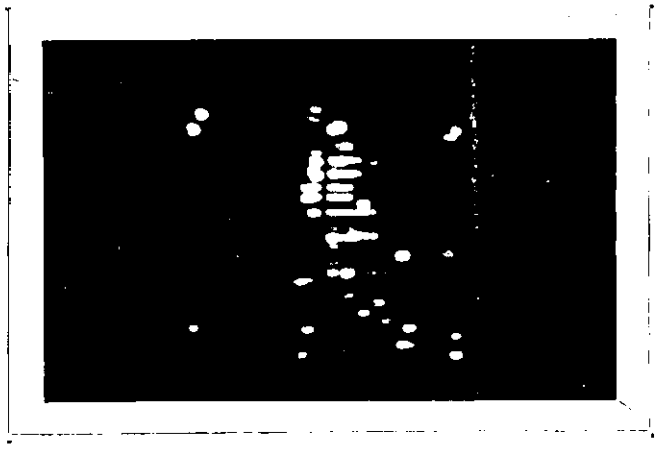


Output Period 145 microseconds

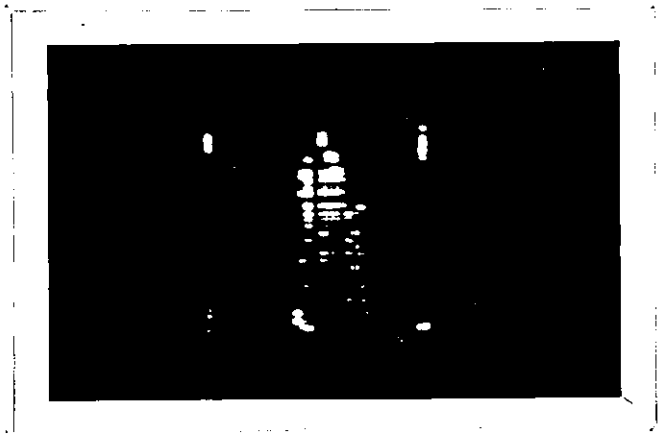
Figure 6.6: Shoal Outputs - No Run Length Coding.



Output Period 2.3 milliseconds

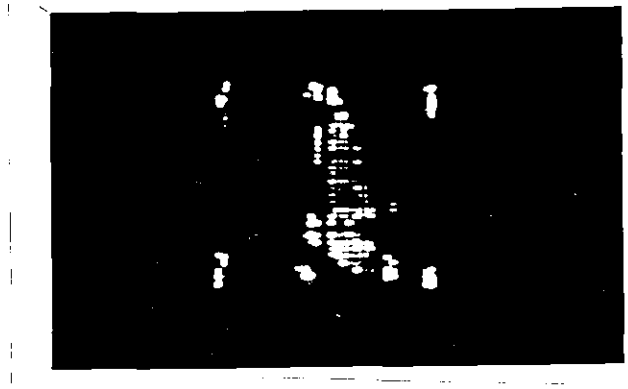


Output Period 1.15 milliseconds

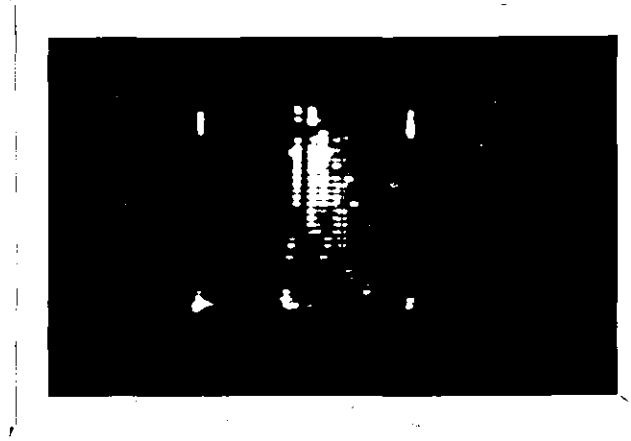


Output Period 580 microseconds

Figure 6.7: Shoal Outputs - with Run Length Coding.



Output Period 145 microseconds



Output Period 72.5 microseconds

Figure 6.8: Shoal Outputs - with Run Length Coding.

such as ours. In addition, the results with the Poisson distributed inputs suggests that the recirculating store could be used effectively as a stand-by store for a main store; the main store would in effect be a bank of output registers. The theory suggests that the size of the main store could then be reduced considerably.

Since the "beat-effect" diminishes as the number of output registers is increased, high recirculation rates can be used which yield even bettter performances. At present this rate is restricted by the maximum clocking rate of MOS shift registers. However, fabrication techniques will no doubt increase this figure considerably. In addition, Large Scale Integration techniques are being extended to bipolar devices which would provide an even more convenient storage system. This would eliminate the need for interface units, dual power supplies and clock drivers.

6.6.2 Coding Methods

The system responds favourably to the simple run-length coding used. As mentioned before, the recommended coding scheme for information sources of this type is one of the optimum code types. These coding schemes allot significance to the probability distribution of elements within the source. Hence in this situation the more frequent runs would be given shorter code lengths. This results in more efficient coding; effectively matching the source to the channel. It is felt that target distributions on sonar displays follow some distinct run-length pattern similar in some respects to the situation encountered in television systems. Further research into this aspect of the system could produce the information necessary to utilize the above coding schemes.

6.6.3 Output Registers

Both simulations and tests on the experimental system suggest that two output registers would be sufficient for the purposes of this system. The apparent sensitivity to the number of registers in the case of Poisson distributed inputs can be explained as follows.

Since the input data is randomly distributed, then the recirculating data is to some extent randomly distributed. Hence, in order to ensure that a word is removed at every output interval the extra channels are needed. In the case of the non-Poissonian input the targets are more compactly distributed hence there is a higher probability that there will be a word in the last store position at the beginning of every output interval. The extra registers are therefore not as essential.

6.6.4 Estimate of Cost

At the time of writing, the average cost of a 256 bit dynamic MOS shift register is in the region of £9.00; the price of the equivalent Random Access device being twice as much. The price of a 5 bit TTL parallel-in-parllel-out shift register which would be needed for the input and output buffers is about £1.80. The implications here are that by using the recirculating method, the cost of storage is now comparable with that of the encoding and decoding circuitry.

These additional circuits are on the whole similar irrespective of the storage method used; hence an estimate of the cost differential of the two methods can be made by comparing the costs of the storage devices.

6.6.5 Communications Channel Requirements

From the experimental results it would seem that a target removal rate of 1000 targets per frame would reproduce recognizable shapes at the output, irrespective of target concentration. This is equivalent to an output period of about 50 microseconds.

Assuming a 20-bit word, an estimate of the channel requirements can be derived. If a single channel is used, then the 20 bits must be shifted out serially in 50 microseconds. This gives a channel capacity of about 400 K Bits per second. This figure takes us well into the region of current wideband telephone links. The equivalent figure for direct transmission would be in the region of 6 M Bits per second. This represents a compression ratio of about 15:1. The figures quoted produced good reproduction on all patterns scanned hence if a lower grade display is tolerable then a lower output rate can be used. In addition, when frame subtraction methodsare applied then even lower output rates could be used.

APPENDIX 1

Expected Queue Length of a Buffer

The following derivation of the expected queue length of a buffer has been produced by Kendall. This is reproduced from Goode and Machol (1, pp336-339).

Consider the instant when a word is to be clocked out of the buffer. If the buffer content immediately after the removal attempt (which may be zero) is n_o then after the next removal attempt (time T later), the buffer content n_1, can be expressed as,

$$n_1 = n_o + r_1 - 1 + d \qquad \ldots\ldots \text{A.1.1}$$

where r_1 is the number of words clocked in the buffer during T, and

$$d = 1, \qquad n_o = 0$$
$$= 0, \qquad n_o \neq 0$$

The quantity d is a number that takes on only the values 0 and 1 and has an expected value lying between these two. We note that $n_o d = 0$ and that $d^2 = d$.

Taking expected value first relative to r_1 and then relative to T, Equation A.1.1 reduces to,

$$E(n_1) = E(n_o) + E(d) + \lambda T - 1 \qquad \ldots\ldots \text{A.1.2}$$

If we assume that stationarity exists then

$$E(n_1) = E(n_o) = E(n), \text{ hence}$$

$$E(d) = 1 - \lambda T \qquad \ldots\ldots \text{A.1.3}$$
$$= 1 - \rho \ ,$$

since ρ the traffic intensity is equal to λT.

Squaring both sides of Equation A.1.1 and taking means we obtain

$$E(n_1^2) = E(n_o^2) + E\left[(r_1 - 1)^2\right] + E(d) + 2E\left[n_o(r_1 - 1)\right] + 2E\left[d(r_1 - 1)\right] \quad \ldots\ldots \text{A.1.4}$$

since $d^2 = d$, and $2n_o d = 0$

Again $E(n_1^2) = E(n_o^2) = E(n^2)$ hence,

$$0 = E(r_1^2) - 2E(r_1) + 1 + E(d) + 2E(n) \cdot E(r_1) - 1 + 2E(d) \cdot E(r_1) - 1 \quad \ldots\ldots \text{A.1.5}$$

Substitution $E(r_1) = \rho$ and

$E(d) = 1 - \rho$, we get

$$E(n) = \frac{E(r^2) - 2\rho^2 + \rho}{2(1 - \rho)}$$

$$= \rho + \frac{E(r^2) - \rho}{2(1 - \rho)} \quad \ldots\ldots \text{A.1.6}$$

Poisson Input Distribution and Constant Holding Time

For a Poisson distributed input

$$p(r_1) = \frac{e^{-\lambda T_1}(\lambda T_1)^{r_1}}{r_1!} \quad \ldots\ldots \text{A.1.7}$$

where r_1 is the number of inputs during the holding time T_1. The mean and variance of this distribution is λT_1.

Now $\sigma r_1^2 = E(r_1^2) - E(r_1)^2$, $\ldots\ldots$ A.1.8

hence $E(r_1^2) = \sigma r_1^2 + E(r_1)^2$ $\ldots\ldots$ A.1.9

$= \lambda T_1 + (\lambda T_1)^2$ $\ldots\ldots$ A.1.10

Taking the expected value of r_1 over all T_1's we obtain

$$E(r^2) = \lambda E(T) + \lambda^2 E(T^2) \quad \ldots\ldots \text{A.1.11}$$

But $E(T^2) = \sigma_T^2 + E(T)^2$, and

$$E(T) = T$$

Hence
$$E(r^2) = \lambda T + \lambda^2(\sigma_T^2 + T^2) \quad \ldots\ldots \text{A.1.12}$$

$$= \rho + \lambda^2\sigma_T^2 + \rho^2 \quad .$$

Substituting this expression for $E(r^2)$ in Equation A.1.6 we get,

$$E(n) = \rho + \frac{\rho^2 + \lambda^2\sigma^2}{2(1 - \rho)} \quad \ldots\ldots \text{A.1.13}$$

For a constant output rate, the variance of the holding time is zero, hence,

$$E(n) = \frac{\rho(2 - \rho)}{2(1 - \rho)} \quad \ldots\ldots \text{A.1.14}$$

This expression is evaluated for several values of ρ and is shown graphically in Figure 3.1.

APPENDIX 2

FLOWCHARTS FOR COMPUTER PROGRAMS USED FOR SIMULATIONS

Programming Language - FORTRAN IV

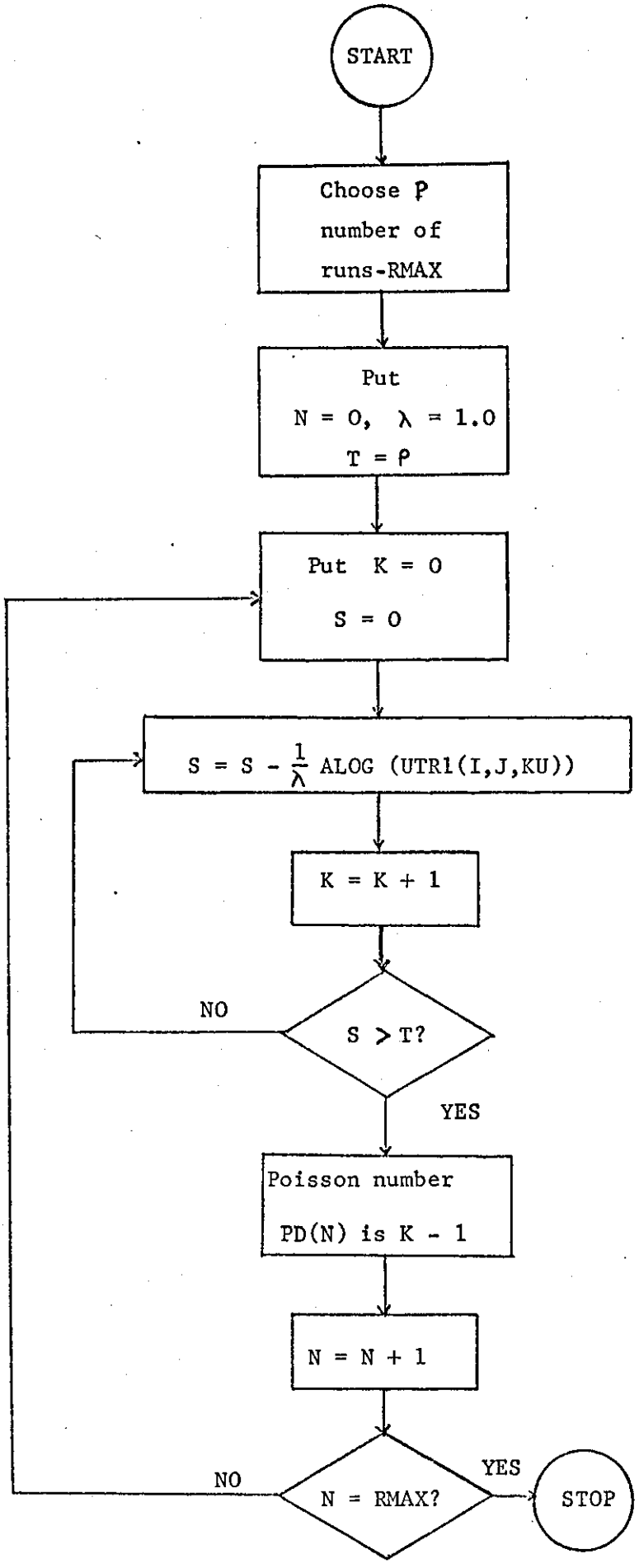


Figure A.1: Poisson generator.

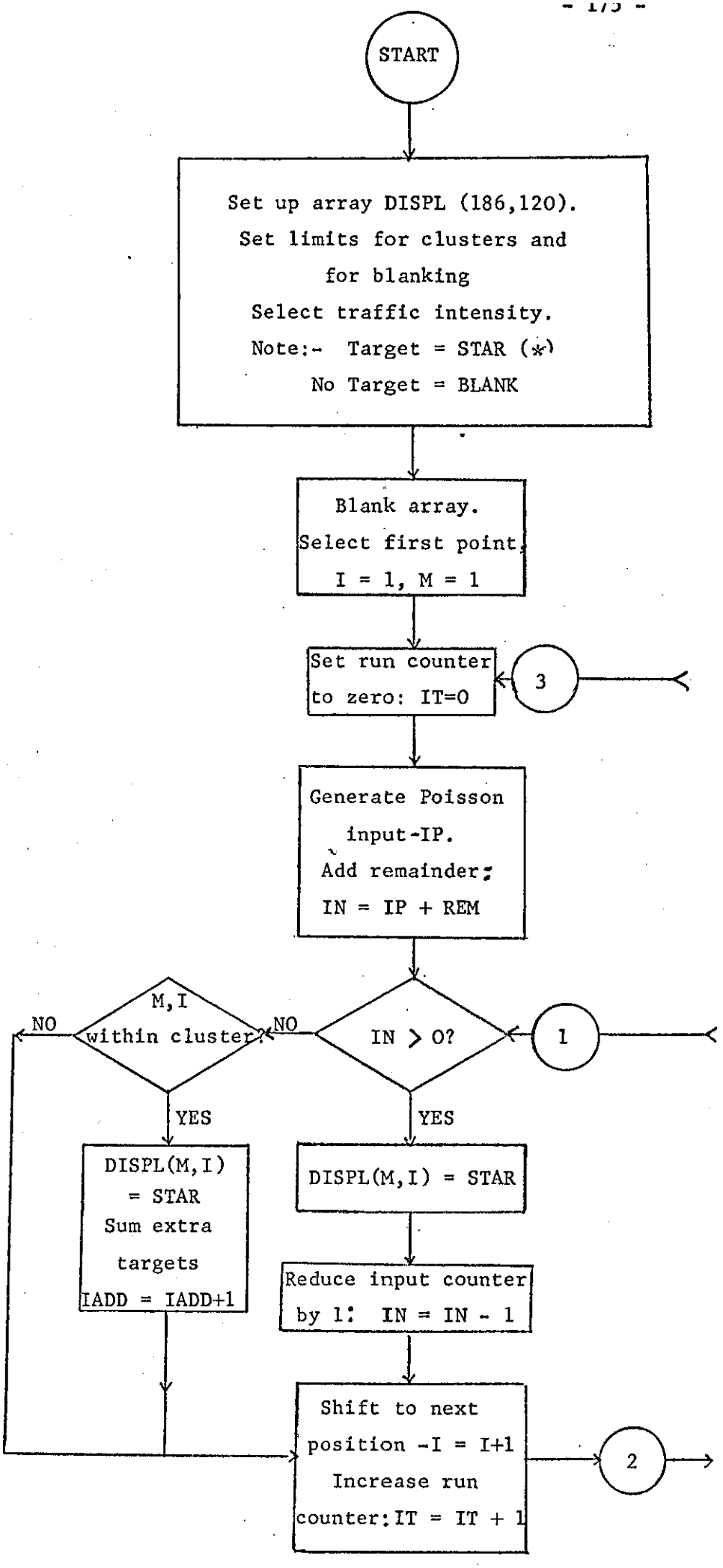


Figure: A.2(1): Generation of Test Pattern.

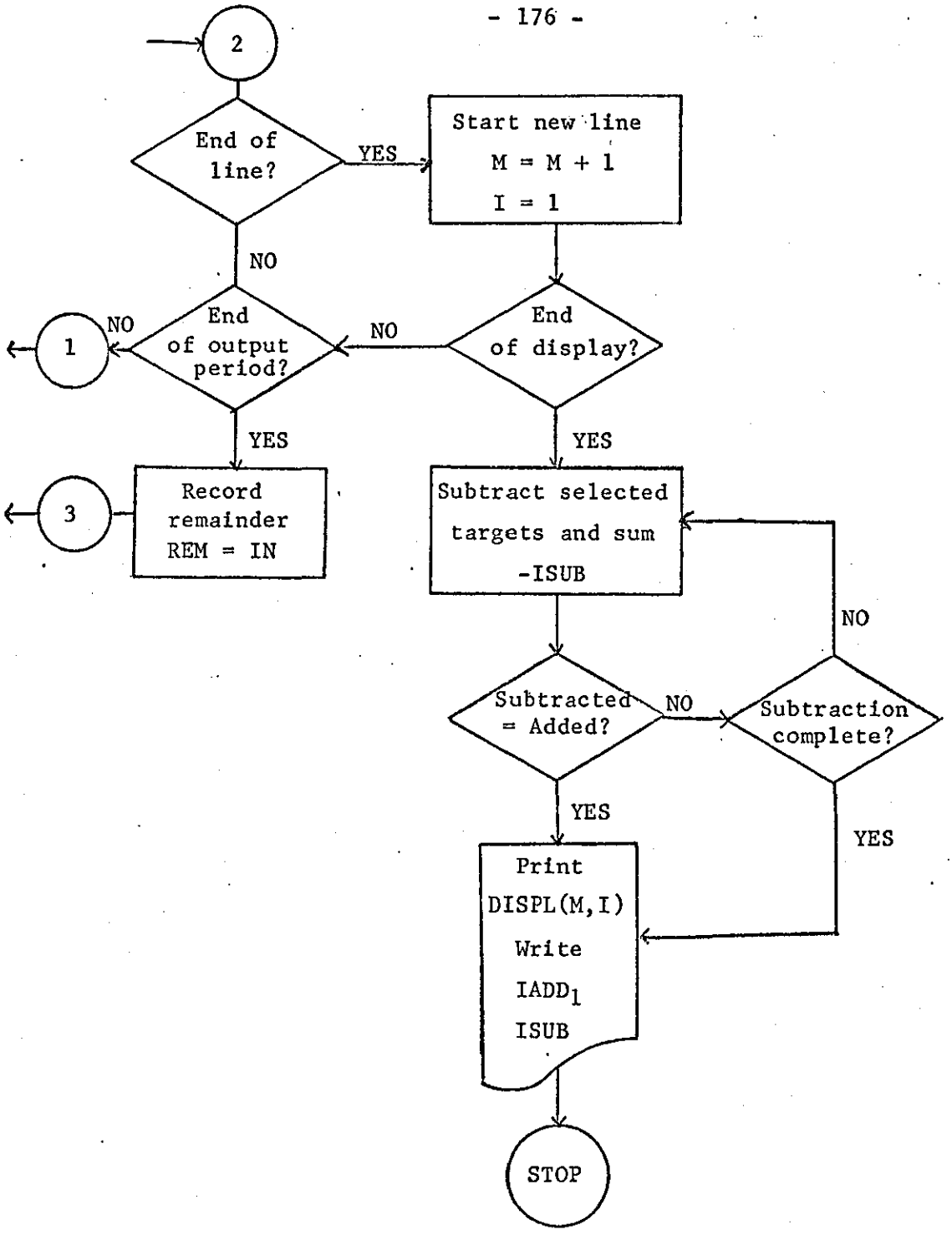

2
End of line?
YES
Start new line
M = M + 1
I = 1
NO
End of output period?
NO
1
NO
End of display?
YES
YES
3
Record remainder
REM = IN
Subtract selected targets and sum
-ISUB
NO
Subtracted = Added?
NO
Subtraction complete?
YES
YES
Print
DISPL(M,I)
Write
IADD1
ISUB
STOP

Figure A.2(2):

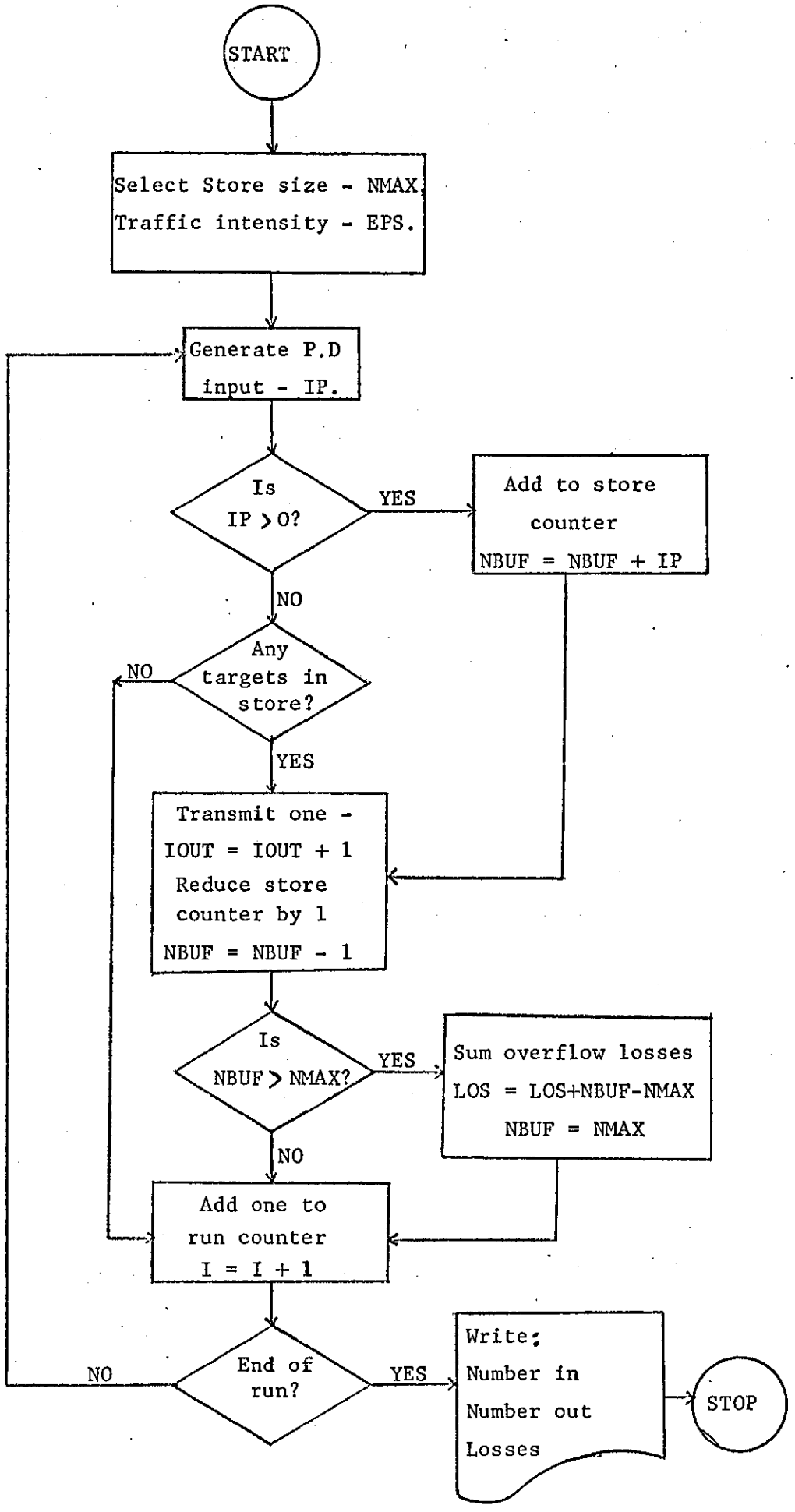


Figure A.3: Simulation of step-down store with Poisson input.

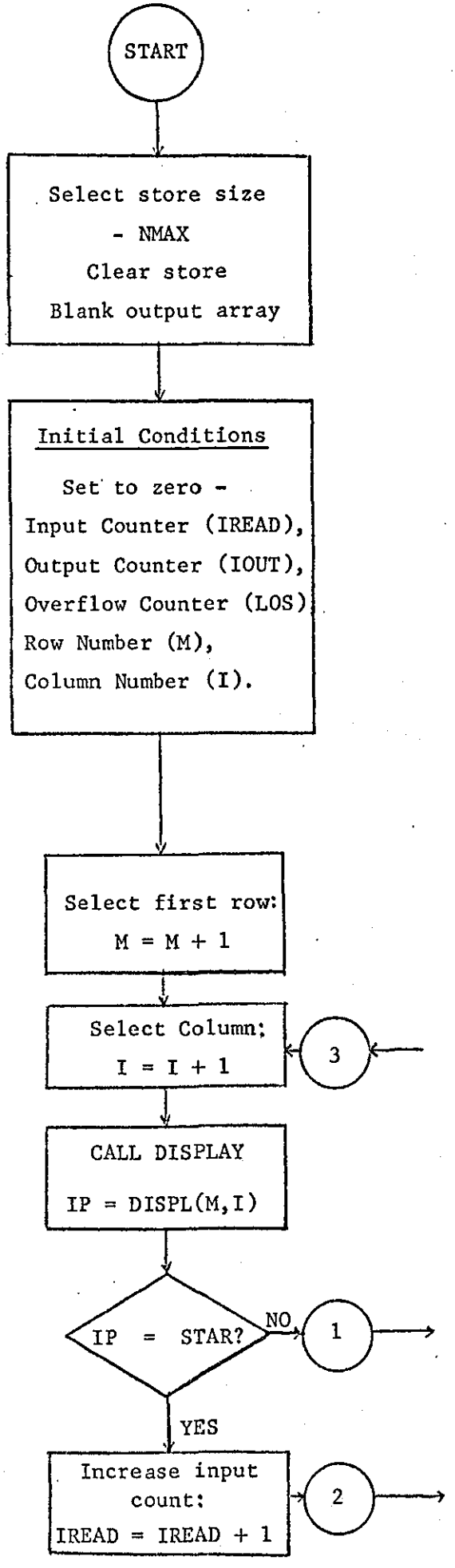


Figure A.4(1): Simulation of a step-down store with Test Pattern as input.

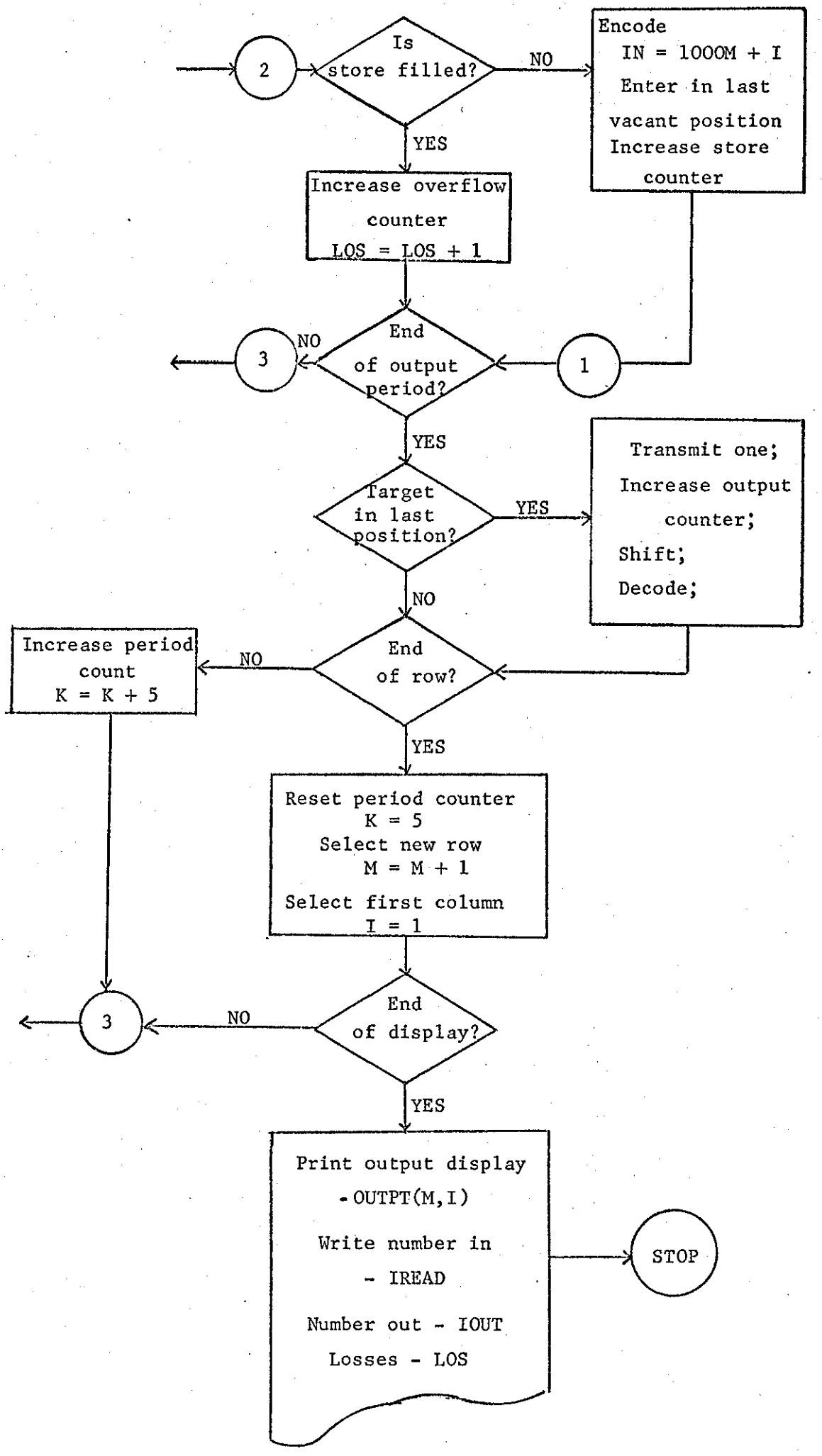

2
Is store filled?
NO
Encode
IN = 1000M + I
Enter in last vacant position
Increase store counter
YES
Increase overflow counter
LOS = LOS + 1
3
NO
End of output period?
1
YES
Target in last position?
YES
Transmit one;
Increase output counter;
Shift;
Decode;
NO
Increase period count
K = K + 5
NO
End of row?
YES
Reset period counter
K = 5
Select new row
M = M + 1
Select first column
I = 1
3
NO
End of display?
YES
Print output display
- OUTPT(M,I)
Write number in
- IREAD
Number out - IOUT
Losses - LOS
STOP

Figure A.4(2):

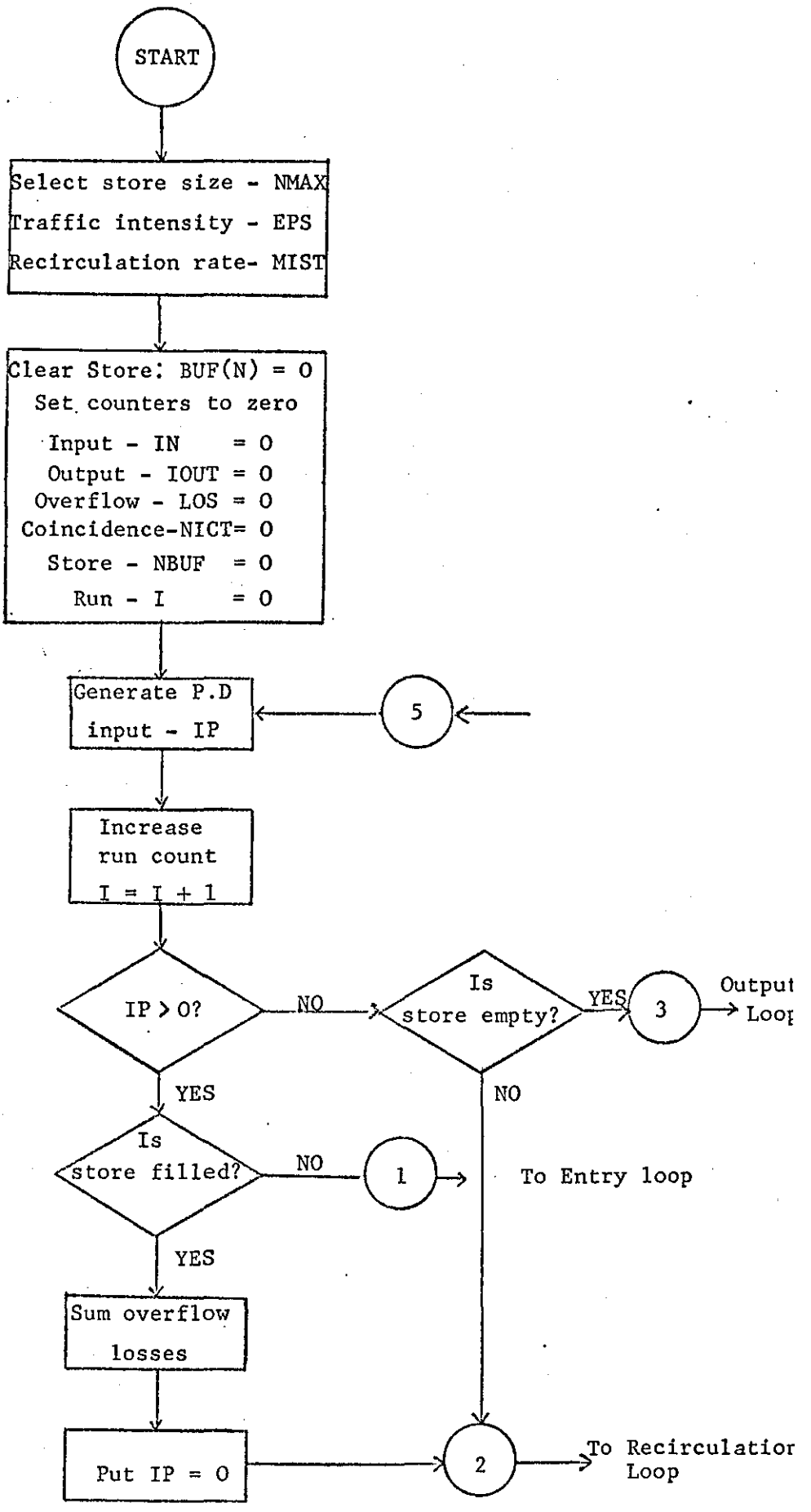


Figure A.5(1): Simulation of a single channel recirculating store with Poisson input.

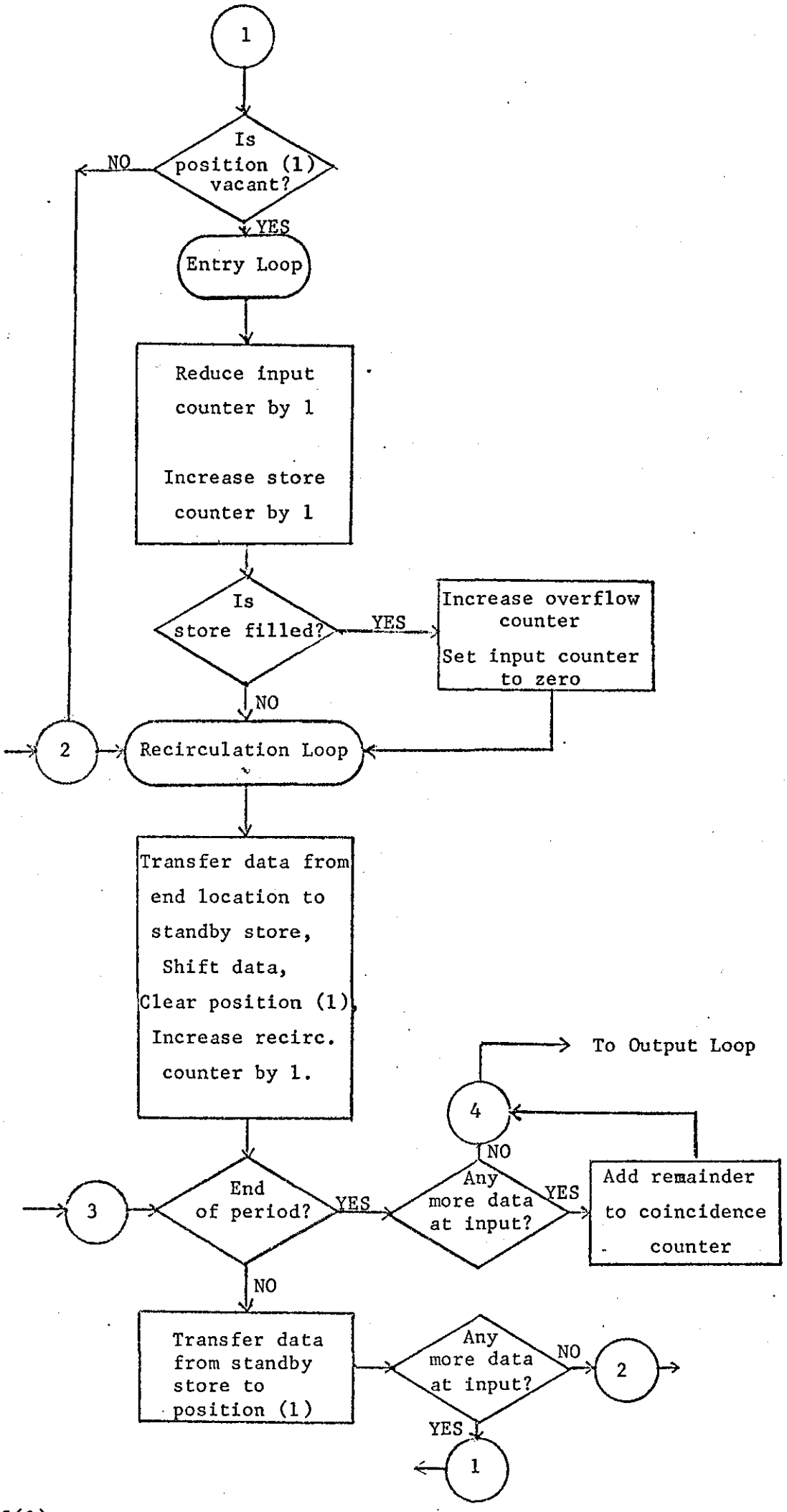

1
Is position (1) vacant?
NO
YES
Entry Loop
Reduce input counter by 1
Increase store counter by 1
Is store filled?
YES
Increase overflow counter
Set input counter to zero
NO
2
Recirculation Loop
Transfer data from end location to standby store,
Shift data,
Clear position (1),
Increase recirc. counter by 1.
To Output Loop
4
NO
3
End of period?
YES
Any more data at input?
YES
Add remainder to coincidence counter
NO
Transfer data from standby store to position (1)
Any more data at input?
NO
2
YES
1

Figure A.5(2):

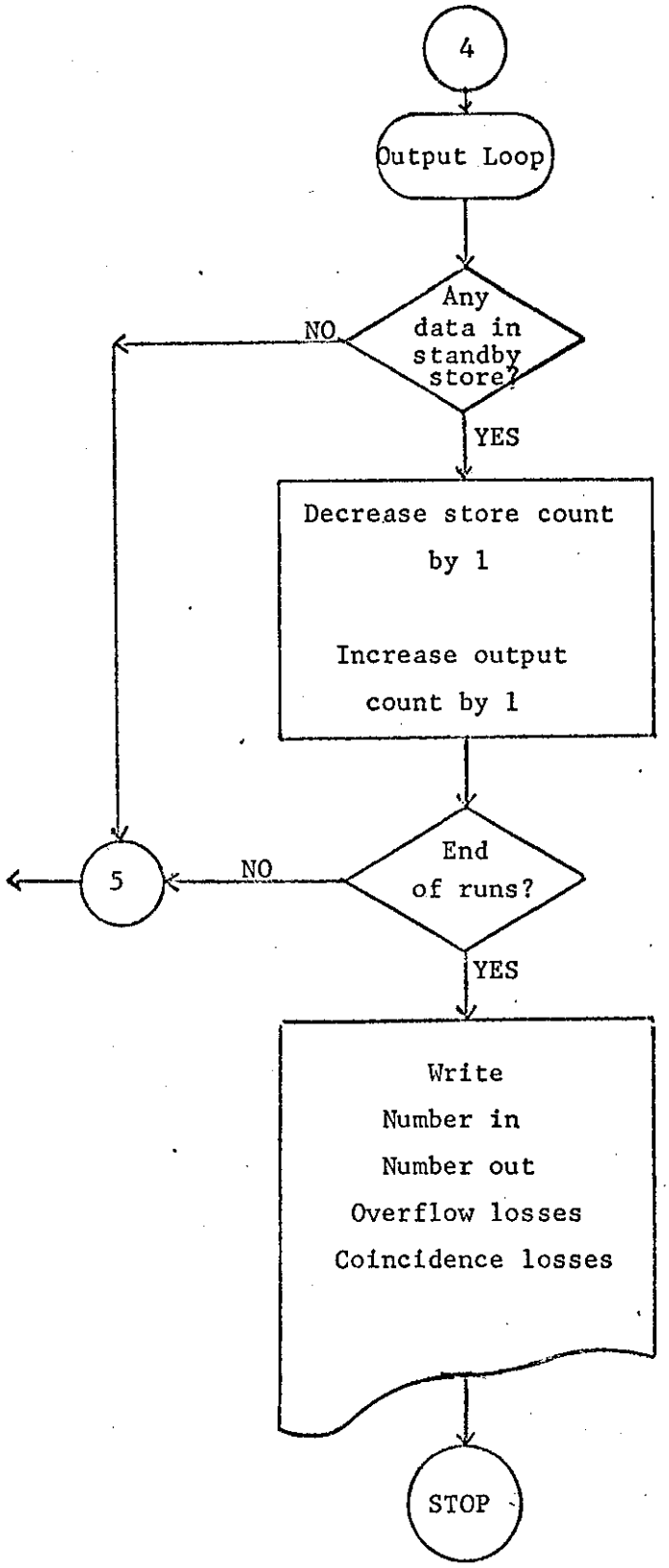

4
Output Loop
Any data in standby store?
NO
YES
Decrease store count by 1
Increase output count by 1
End of runs?
NO
5
YES
Write
Number in
Number out
Overflow losses
Coincidence losses
STOP

Figure A.5(3):

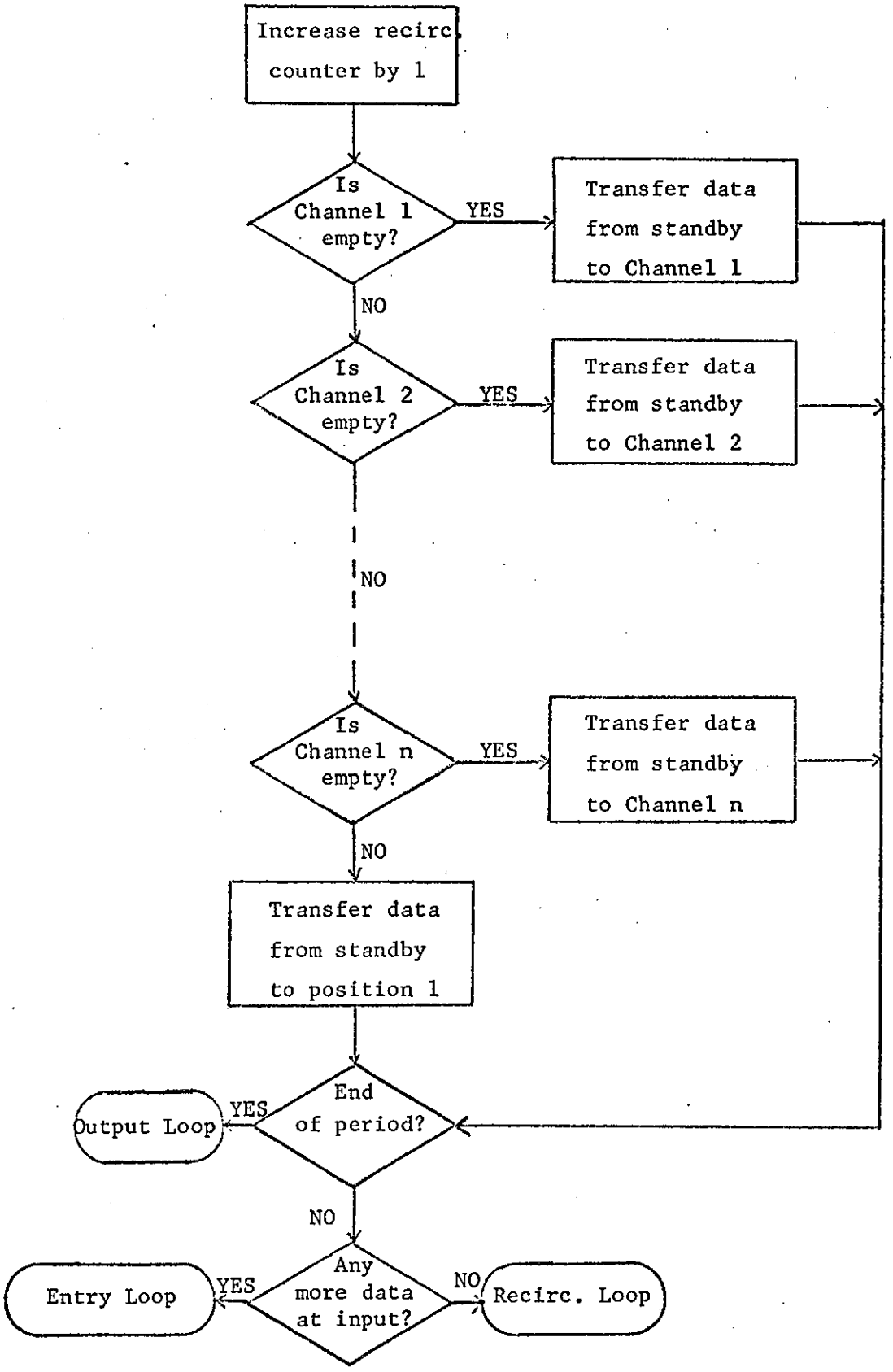


Figure A.6: Modifications to recirculation loop for multiple channels.

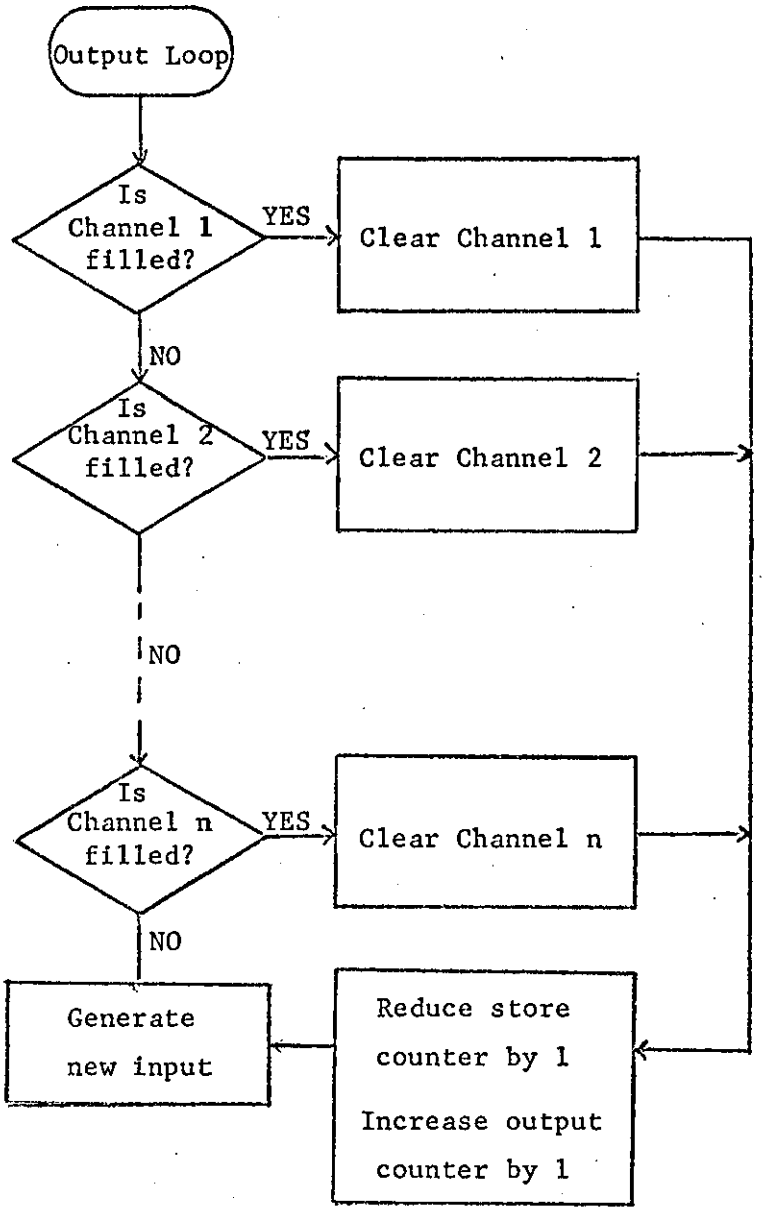


Figure A.7: Modifications to output loop for Multiple Channels.

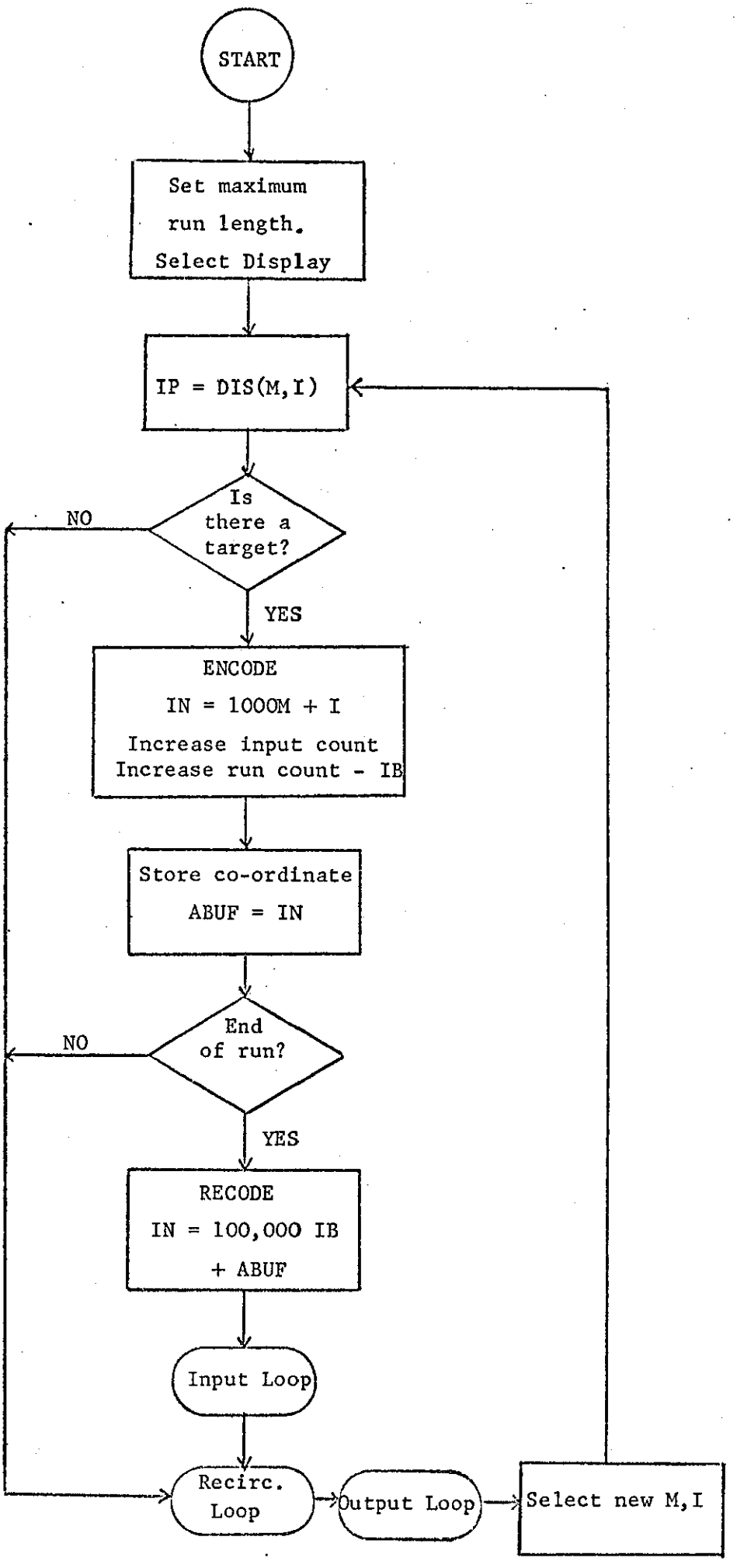


Figure A.8: Run Length Coding using Method 1.

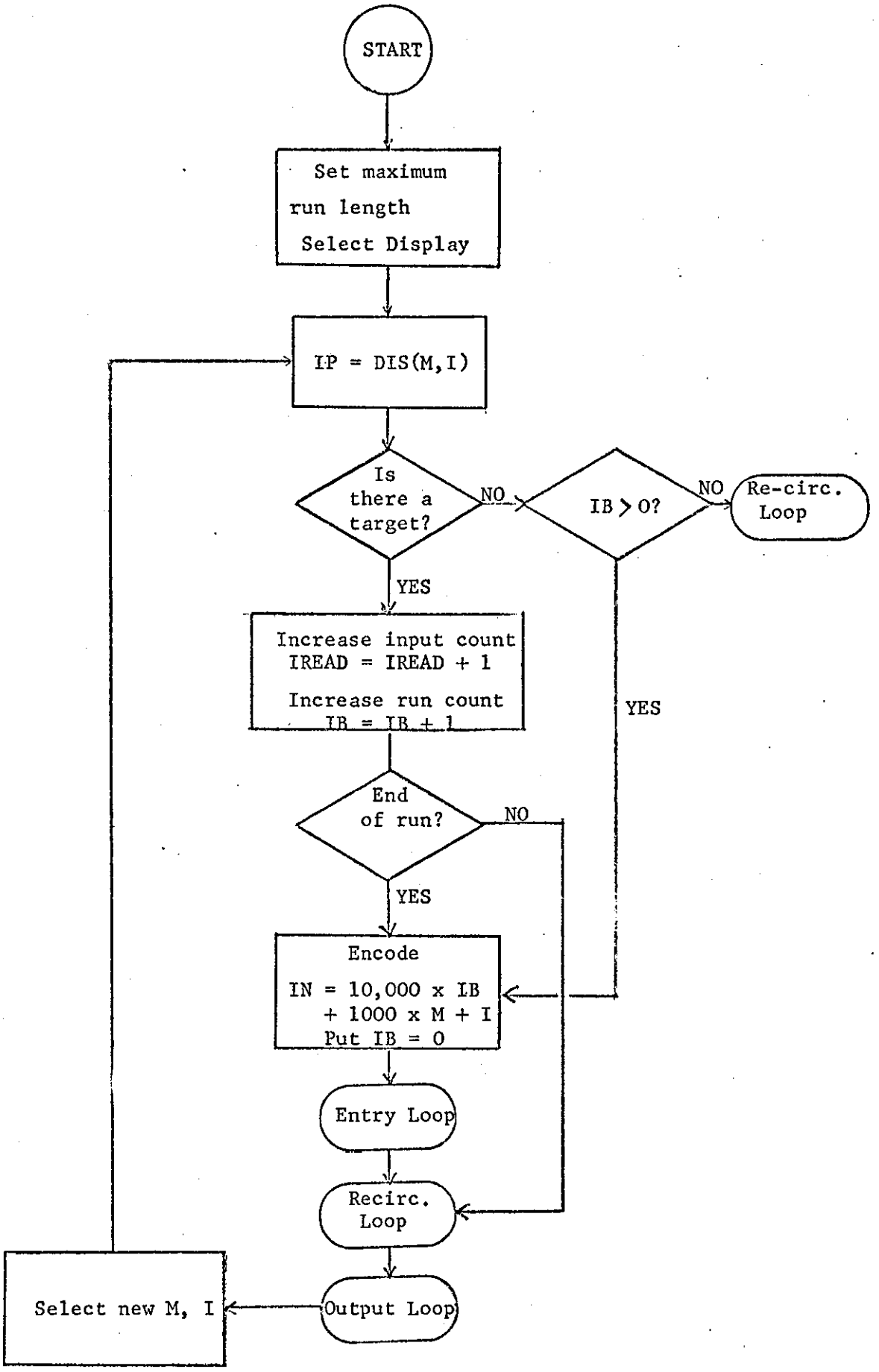


Figure A.9: Run Length Coding using Method 2.

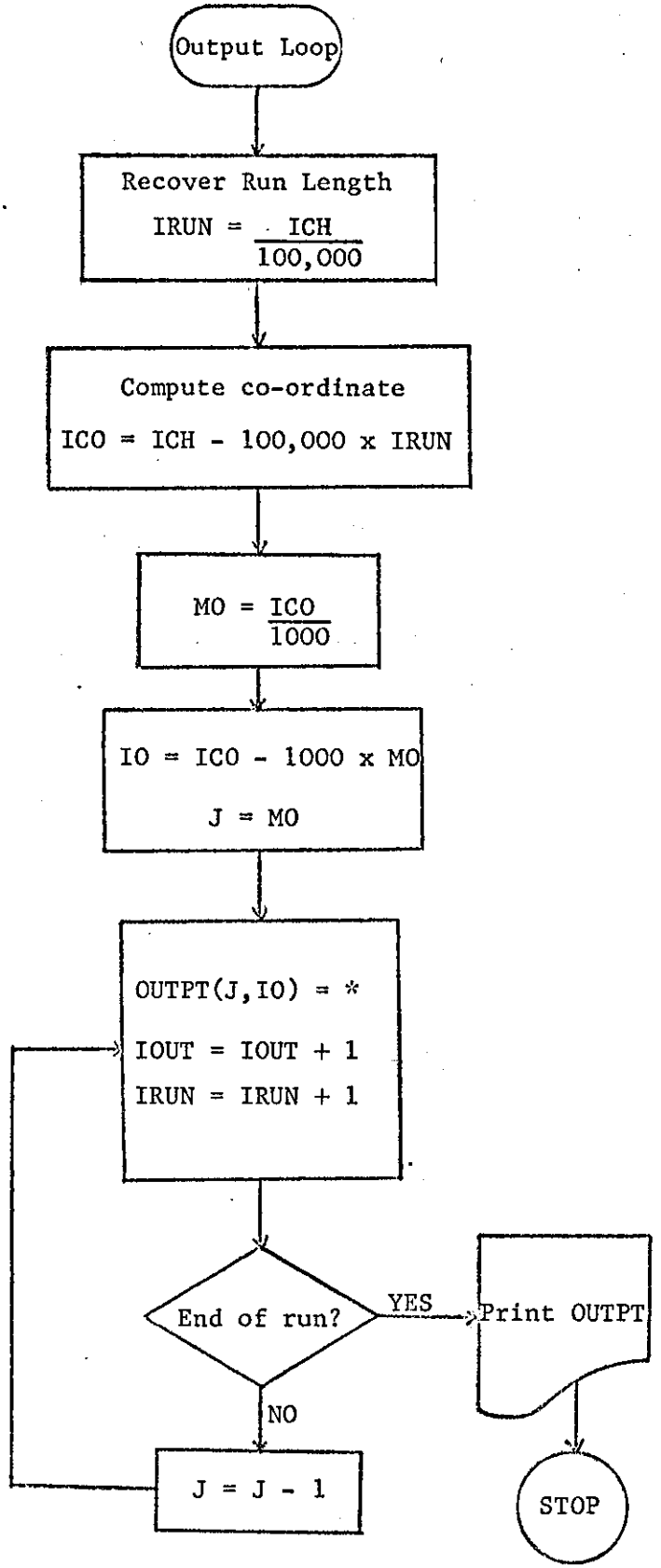


Figure A.10: Decoding process for run-coded inputs.

APPENDIX 3

THE TARGET SIMULATOR

A.3.1 System Requirements

This system is required to simulate the conditions likely to occur on the display of an electronic sector scanning sonar system with a B-scan display. The main features of the system have been described in Section 5.2 and a block diagram of the system is shown in Figure 5.2.

In theory this method should, by scanning a moving film taken of an actual display, reproduce the real situation. However, due to the mechanical problems mentioned in Section 5.2, it was decided to construct the static system only.

The system should be able to simulate various maximum ranges with a fixed bearing scan time of about 100 microseconds. It should be able to resolve two targets along the bearing scan line separated in time by about 3 microseconds. The video signal should be of sufficient magnitude to trigger a threshold detector circuit. In order to synchronize the target pulses to the bandwidth compression system the simulator should produce end of line and end of frame pulses.

A.3.2 Sweep Generators

The time-base circuits are built around a constant-current transistor whose current flows into a capacitor of known value. Figure A.11 shows the basic circuit used. Transistor T_1 whose base voltage is held constant forms the constant current source. Transistors T_3 and T_4

are connected as a regenerative switching pair and form the shut-off circuit. The base voltage of T_3 should be less than the base voltage of T_1 as its magnitude determines the shut-off point. With the emitter of T_3 reversed biased, the collector current from T_1 produces a ramp by the charging of the capacitor. When the ramp voltage becomes sufficiently positive to forward bias the emitter of T_3, the collector current of T_3 turns on T_4. The capacitor discharges to approximately 1V, T_3 and T_4 stop conducting and the action repeats. T_2 is included to provide an extra low conductance path during the discharge.

A.3.2.1 Calculation of Capacitor Values

A3.2.1.1 Range Simulation

The sweep time of the slow time base should accommodate the time taken for an ultrasonic pulse to travel the maximum range and back. Now, the velocity of sound in sea water is approximately 1540 metres/second.

Consider a maximum range of 2.5 metres, then,

$$\text{the Scan Time} = \frac{2 \times 2.5}{1540} \text{ seconds} \qquad \ldots\ldots \quad \text{A.3.1}$$

For a charging current of 10 mA and a voltage sweep of 6v, then the capacitor value is given by the expression,

$$C = i\,T/V$$

$$= \frac{10 \times 10^{-3} \times 2 \times 2.5 \times 10^{6}}{6 \times 1540} \text{ micro Farads}$$

$$\simeq 5 \text{ micro Farads}$$

i = charging current

T = sweep time

V = ramp voltage

This capacitor value simulates one range only; other range values are simulated by switching in other capacitor values. For each capacitor value, various ranges can be simulated by varying the charging current using a variable resistor in the emitter lead.

A3.2.1.2 Bearing Simulation

The bearing sweep time is held fixed at approximately 100 micro-seconds. The design approach is similar to that used for the range capacitors.

The design was also extended to produce varying fast sweep times. This was needed for subsidiary experiments to investigate the resolution properties of cathode ray tube phosphors.

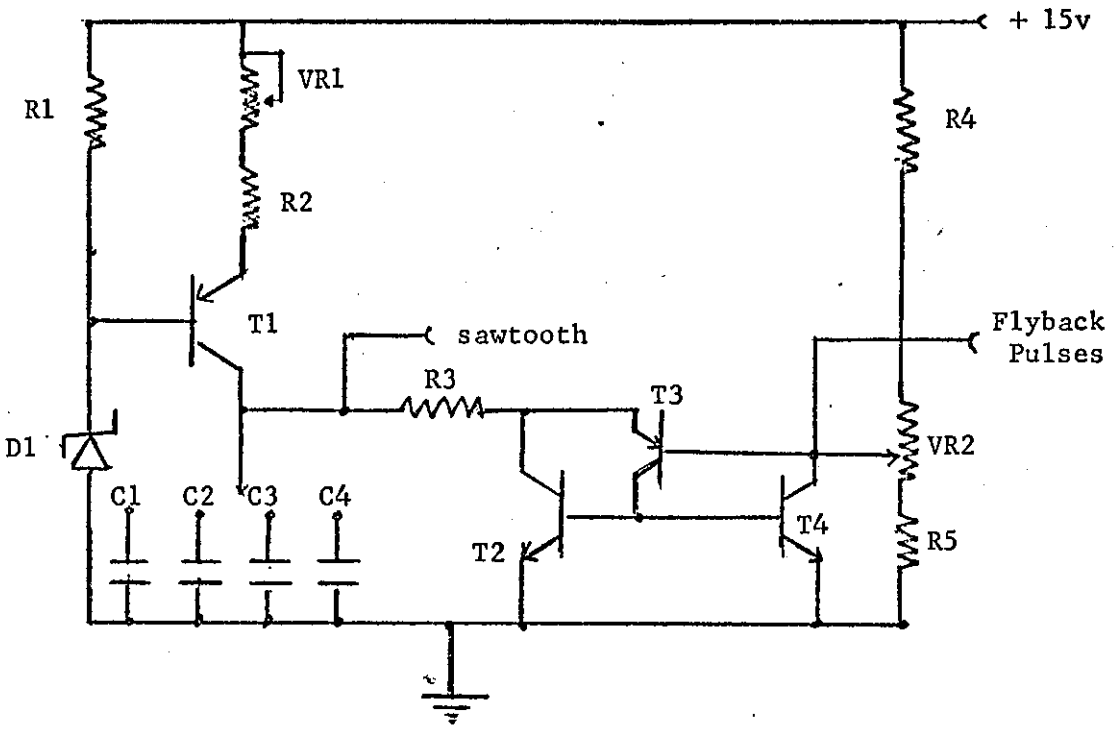
A3.2.1.3 Synchronizing Pulses

These are taken from the bases of transistor T_3 (range) and T_3 (bearing). The pulse height, which is the same as the sweep voltage has to be clipped before being fed to standard logic gates.

A3.3 Phosphor Resolution

The high resolution requirements of the system demand in turn high resolution characteristics from the cathode ray tube phosphor.

The medium persistence phosphor supplied with a standard oscilloscope was found to be unsuitable due to the phosphor decay time. Initial experiments using medium persistence P7 and 11 phosphors demonstrated the effect of the long decay time. When a narrow slit was scanned



T1, T3	- ZTX 502		
T2, T4	- ZTX 302		
C1 ...	- Capacitors calculated as described in text		
R1 - 2.2kΩ	R4	- 220Ω	
R2 1.0kΩ	R5	- 220Ω	
R3 10Ω	VR2	- 1kΩ potentiometer	
VR1, 10kΩ pot.	D1	- 10v Zener	

Figure A.11: Circuit diagram for Range and Bearing Sawtooth Generators.

with the 100 microsecond sawtooth a decay time of the order of 2 milliseconds was measured. When these tubes were replaced with a short persistence P15 phosphor a decay time of about 3.5 microseconds was recorded. The manufacturer's figures quote an average build-up time of about 0.035 microseconds and an approximate decay time of 2.5 microseconds. These figures would make this phosphor just sufficient for the required resolution. The build-up and decay times quoted are between the 10% and 90% levels.

A.3.4 Head Amplifier for Video Signal

The purpose of this amplifier is to match the high impedance of the photomultiplier tube to the comparatively low impedance of the video amplifier.

The Field Effect Transistor used was a 2N524 N-Channel device and was connected in the common drain mode as shown in Figure A.12. The amplifier is mounted close to the photomultiplier output and its output connected to the video amplifier by a short length of coaxial cable.

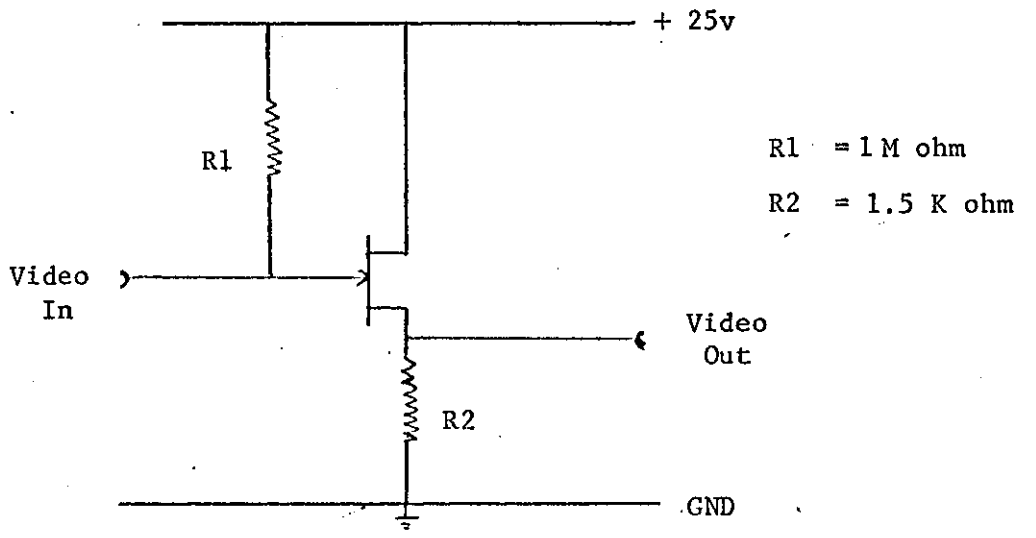


Figure A.12: Head amplifier for video signal.

A3.5 The video amplifier

The signal from the photomultiplier varied in amplitude from 0.2V to 0.5V. In addition, the signal was negative going as the photomultiplier anode was biased at 0V.

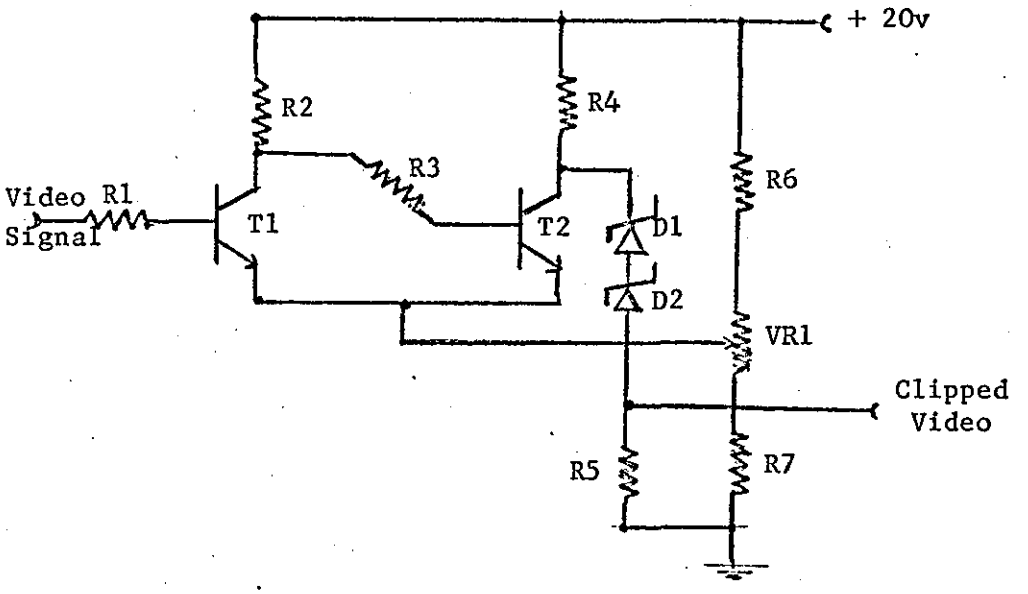
The requirements of this amplifier are therefore to provide a bandwidth of about 1 MHz, a gain of about 20 and inversion of the signal.

A single stage common emitter amplifier satisfies these conditions hence this method of design is used.

A3.6 The threshold detector

This circuit is required to produce a pulse whenever the video signal exceeds a preset level. The design is a modification of a method outlined in (2). The circuit used is shown in Figure A13; the modification introduced involves the emitter resistor. In this circuit this resistor is made variable; this effectively varies the switching level.

The pulse produced is clipped for processing by standard logic circuits.



T1, T2	-	2N697	
D1	-	ZB 11	
D2	-	ZB 3	
R1 - 2.2KΩ		R5 - 1kΩ	
R2 - 3.3kΩ		R6 - 3.3kΩ	
R3 - 2.2kΩ		R7 - 1kΩ	
R4 - 3.3kΩ		VR1 - 1kΩ	potentiometer

Figure A.13: Circuit Diagram of Threshold Detector.

APPENDIX 4

DATA SHEET FOR MOS DEVICES USED FOR MAIN STORE

electrical drive characteristics (Note 2)

PARAMETER	CONDITION	MIN	TYP	MAX	UNITS
Clock Pulse Width					
ϕ_1 Clock, ϕ_1 pw		0.100		10	μs
ϕ_2 Clock, ϕ_2 pw		0.100		10	μs
Clock Pulse Risetime, $t_{r\phi}$	4 MHz Operation			0.01	μs
Clock Pulse Falltime, $t_{f\phi}$	4 MHz Operation			0.01	μs
Clock Delay, ϕ_d		0.01			μs
Clock Input Level					
Logic "0"			-0.5	-1.5	V
Logic "1"	4 MHz Operation	-17	-18	-20	V
Logic "1"	Less than 2 MHz	-14.5	-16	-18	V
Data Pulse Width, t_{dw}		0.115			μs
Data Input Voltage Levels					
Logic "0"				-2.5	V
Logic "1"		-7.0			V
Data Setup Time, t_{ds}		0.01			μs

electrical performance characteristics (Note 2)

PARAMETER	CONDITION	MIN	TYP	MAX	UNITS
Clock Repetition Rate	Fan-out of "one"	0.01		4.0	MHz
Data Output Voltage Levels					
Logic "0"	Input (dc)			-1.5	V
Logic "1"	Input (dc)	-8.0			V
Data Input Capacitance	f = 1 MHz at 25°C				
	0V Bias		2.5	3.5	pF
	-10V Bias		2.0	2.5	pF
Clock Input Capacitance	f = 1 MHz at 25°C				
	0V Bias		45	55	pF
	-20V Bias		30	40	pF
Output Impedance					
Logic "0"			2.0		KΩ
Logic "1"			2.0		KΩ
Breakdown Voltage	1.0 μA Test Current T_A = 25°C				
On Pin 1	GND all pins except pin 1	-28			V
On Pin 2	GND all pins except pin 2	-28			V
On Pin 4	GND all pins except pin 4	-28			V
On Pin 6	GND all pins except pin 6	-28			V
On Pin 8	GND all pins except pin 8	-28			V
On Pin 9	GND all pins except pin 9	-28			V
Leakage Current	T_A = 25°C				
Pin 1	GND all pins except pin 1 Bias pin 1 at -25V			0.5	μA
Pin 2	GND all pins except pin 2 Bias pin 2 at -25V			0.5	μA
Pin 4	GND all pins except pin 4 Bias pin 4 at -25V.			0.5	μA
Pin 6	GND all pins except pin 6 Bias pin 6 at -25V			0.5	μA
Pin 8	GND all pins except pin 8 Bias pin 8 at -25V			0.5	μA
Pin 9	GND all pins except pin 9 Bias pin 9 at -25V			0.5	μA

Note 1: For operation at elevated temperatures, the device must be derated based on curves which will be incorporated in the final data sheet.

Note 2: These specifications apply over the indicated operating temperature ranges for $-20 \leq V_{GG} \leq -17V$ at 4 MHz and $-18 \leq V_{GG} \leq -14.5V$ at 2.5 MHz or less. The output is measured with a load of less than 4 pF in parallel with 10 MΩ to ground unless otherwise specified.

National Semiconductor Corporation
2975 San Ysidro Way, Santa Clara, California 95051
(408) 245-4320/TWX (910) 339-9240

APPENDIX 5

THE DIGITAL-TO-ANALOG CONVERTERS

A.5.1 System Requirements

Two converters are required, one for decoding the 5 bits of bearing data and one to decode the 9 bits of range data. The system need not be of high accuracy hence a medium accuracy design would be sufficient.

Since in this system the decoder outputs are to be fed directly to the "X" and "Y" inputs of an oscilloscope the final summing amplifier is ignored; the amplifiers of the oscilloscope being of sufficient gain and bandwidth.

The speed of decoding will vary with the output rate used. However, the maximum output rate envisaged would be of the order of 50 KHz. If run-length coding is used then a maximum of 8 conversions must be done in 20 microseconds.

A.5.2 Circuit Design

The circuit used follows a design outlined in (3). This circuit, shown in Figure A.14 achieves conversion by the weighted current technique; with n current sources for n bits. The value of the current for each bit depends on the significance of the bit in the digital word, and is determined by the resistor R3.

Diode D-4 is the decoder switch; when a digital "1" is applied to this diode, current from the current source flows into the summing

resistor. If the input is at OV, then D-4 is forward biased and the current is zero except for leakage currents. Diodes D1 and D2 are temperature compensating diodes and D3 holds the base of T1 at a fixed voltage. Two transistors are used for the M.S.B. and N.M.S.B. of each decoder; for the less significant bits, only one transistor is used since the output current and hence the error capability decreases as the significance of the bit decreases.

An expression derived in (3) shows that the decoding speed is given by,

$$T_D = 4.6 \cdot RO \cdot C_1 \qquad \ldots\ldots \quad A.8.1$$

where RO = network output resistance

C_1 = capacitive load driven by decoder output.

Hence a typical value of T_D for this circuit would be,

$$T_D = 4.6 \times (10 \text{ Kohm}) \times (40\text{pF})$$

$$\simeq 2 \text{ microseconds}$$

This derivation assumes that the input resistance is much greater than the network output resistance. Typical values for the "Y" input of a standard oscilloscope is 1 M ohm and 33pF hence this assumption is permissible.

The tolerance of resistor R_3 determines the accuracy of the analog voltage hence low tolerance resistors are normally used. A simple estimate of the error introduced by resistor tolerance can be obtained by considering the errors induced by each bit decoder.

Hence for the M.S.B.

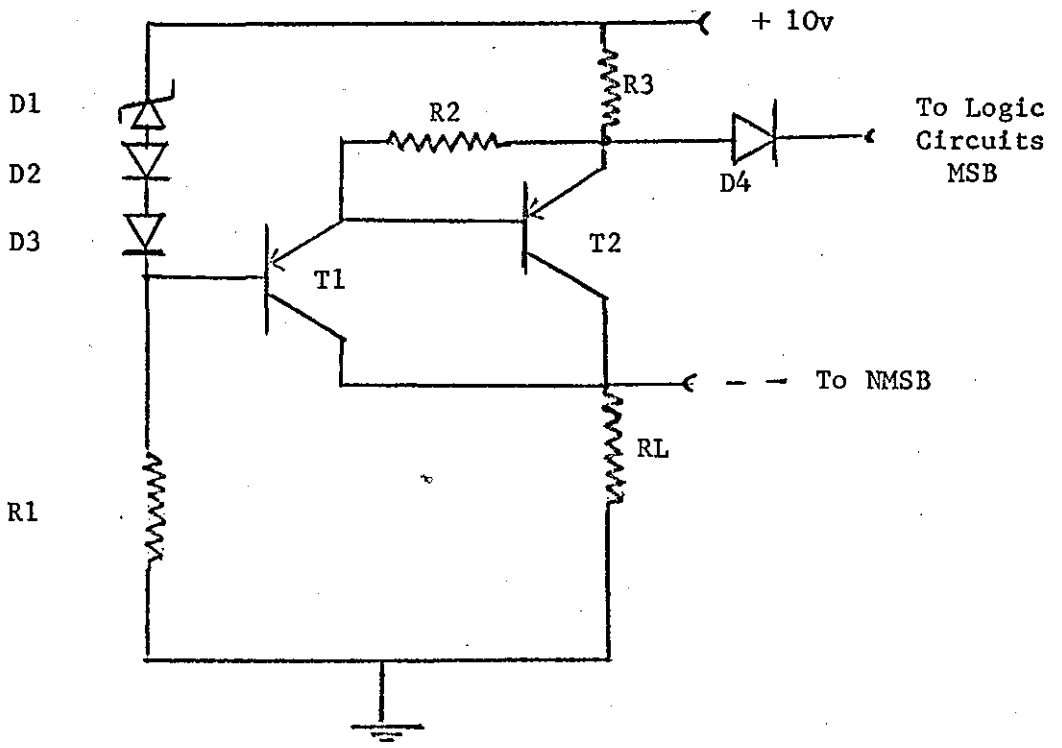
$$E1 = \frac{1}{2^2} \varepsilon_1 ,$$

for Bit 2, $$E2 = \frac{2^2 + 1}{2^5} \varepsilon_2$$

for Bit n, $$En = \frac{2^{2(n-1)} + .. 2^4 + 2^2 + 1}{2^{3n} - 1} \varepsilon_n ,$$

Where ε_n = actual percentage error of the nth bit resistor. These results are taken from (3, Chapter 6).

The resistors used in this design were 1% wire wound resistors.



T1, T2 - 2N1132
D1 - ZF7
R3 - calculated according to bit significance MSB = 10K Ω (1%)
D2, D3, D4 - 1S44
R1 - 1K Ω
R2 - 2.2K
RL - 1K Ω

Figure A.14: Transistor weighted - current D/A decoder.

APPENDIX 6

CONSTRUCTIONAL DETAILS

These notes are added for the convenience of anyone who proposes to use the experimental system in the future.

The system is contained in two Vero-racks clamped together to form one unit. The integrated circuits are mounted on 0.1 x 0.1 in. double sided Veroboards with other circuits on the single-sided type. For reasons of economy three types of integrated circuits are used in the design; the MOS devices used in the main store and RTL and TTL devices used in the computing circuits. The following power supply rails are therefore provided;

- 18v for MOS devices,
+ 25v for Target simulator and D-to-A converter,
+ 3.6v for RTL devices, and
+ 5.0v for TTL devices.

The power supply lines are easily located; however, on the IC boards these are connected as follows;

Pin 1 - + Vcc

Pin 40 or 32 - Ground.

An attempt was made to build the system according to the design approach, hence each board consists of an operational unit. For convenience, Board 1 is considered the left-hand board in the lower rack.

Board 1:- consists of the range and bearing digitizers. The main pin connections are as follows;

Pin 6	-	Display Clock	- Input
7	-	Range Pulses	- Input
11	-	Bearing Pulses	- Input
Pins 12 - 25	-	$\overline{Q}$'s of counters	- Output
26 - 39	-	Q's of counters	- Output

Board 2:- consists of Run Length Encoding circuits and Code/No-Code circuits.

Pin 12	-	Target Detected Pulses	- Input
15	-	Inverse of above	- Input
19	-	Display Clock	- Input
Pins 26 - 28	-	$\overline{Q}$'s of counter	- Output
30	-	Transfer Pulse	- Output
33 - 35	-	Q's of counter	- Output
39	-	Code/No-Code Switch	- Input

Board 3:- consists of a section of the Input Buffer. This section contains the register for 9 bits of range data and 5 bits of bearing data.

Pin 5	-	Shift Control Signal	- Input
6	-	Q5 of First Range Register	- Output
7	-	Target Detected Pulses	- Input
8	-	Q5 of Bearing Register	- Output
9	-	Q4 of Second Range Register	- Output
10	-	Q4 of Second Range Register	- Output
11	-	Shift Pulses	- Input
Pins 12 - 25	-	$\overline{Q}$'s (1-14) of Encoder	- Input
26 - 39	-	Q's (1-14) of Encoder	- Input

Board 4:- consists of the Input-Output Decision Circuits, and Output Registers Shift circuits.

Pin	2	- Marker Bit	- Input
	3	- Recirculation Control	- Output
	4	- Data containing flag	- Input
	11	- Output Shift Pulses for Register 1	- Output
	12	- Output Shift Pulses for Register 2	- Output
	13	- Output Shift Pulses for Register 3	- Output
	14	- Output Register 1 Monitor Signal	- Input
	15	- Output Register 2 Monitor Signal	- Input
	16	- Output Register 3 Monitor Signal	- Input
	23	- Output Control Signal	- Output
	26	- Input Control Signal	- Output
	30	- Synchronizing Pulses	- Input
	39	- Shift Clock	- Input

Board 5:- consists of the Main Store with Clock Drivers and Interface Units.

Pin	5	- Data from Store (D)	- Output
	8	- Data from Store (A)	- Output
	13	- Data from Store (B)	- Output
	15	- Data from Store (C)	- Output
	17	- Data from Steering Circuit (A)	- Input
	19	- Data from Steering Circuit (D)	- Input
	21	- Data from Steering Circuit (B)	- Input
	23	- Data from Steering Circuit (C)	- Input
	25	- Main Clock	- Input
	31	- + 5v	- Input
37 -	38	- - 18v	- Input

Board 6:- consists of the Steering Circuits and the extra Flip-Flops for each Main Store register.

Pin 2	-	Data to Output Register A	- Output
3	-	Recirculation Control Signal	- Input
4	-	Data containing Flag	- Output
5	-	Data to Output Register B	- Output
6	-	Data to Output Register C	- Output
7	-	Data to Output Register D	- Output
12	-	Shift Clock	- Input
19	-	New Data (C)	- Input
22	-	New Data (B)	- Input
23	-	Output Control Signal	- Input
24	-	New Data (D)	- Input
25	-	New Data (A)	- Input
26	-	Data to Main Store Register (A)	- Output
27	-	Data to Main Store Register (D)	- Output
28	-	Data to Main Store Register (B)	- Output
29	-	Data to Main Store Register (C)	- Output
31	-	Data from Main Store Register (C)	- Input
32	-	Data from Main Store Register (B)	- Input
36	-	Data from Main Store Register (A)	- Input
38	-	Data from Main Store Register (D)	- Input

Board 7:- consists of the remaining section of the Input Buffer.

Pin 7	-	$\overline{Q}_1$ output of Run Counter	- Input
8	-	$\overline{Q}_2$ output of Run Counter	- Input
9	-	Q_4 output of Second Range Register	- Input
10	-	$\overline{Q}_4$ output of Second Range Register	- Input
11	-	Shift Clock	- Input
19	-	Q_5 output of Flag F.F.	- Output
21	-	Q_5 output of Run Length Register	- Output
25	-	Marker Bit	- Output
31	-	Transfer Pulses	- Input
33	-	Q_1 output of Run Counter	- Input
35	-	Q_2 output of Run Counter	- Input
37	-	Q_3 output of Run Counter	- Input

Board 8:- consists of the Main Clocks and synchonizing pulses generator.

Pin 11	-	Shift Pulses	- Output
16	-	Synchronizing Pulses	- Output
23	-	Shift-In Control Signal	- Input
37	-	6 MHz Clock	- Output

Board 9:- consists of the Video amplifier, Threshold detector and Time Quantization circuits.

Pin 1	-	+ 25v	- Input
13	-	Display Clock	- Output
16	-	Range Pulses	- Input
17	-	Bearing Pulses	- Input
18	-	Targets in Count Pulses	- Output
25	-	+ 5v	- Input
27	-	Target Detected Pulses	- Output
29	-	Inverse of 27	- Output
31	-	Video In	- Input

Board 10:- consists of the Bright-Up Pulses Generators and the Flyback Pulses clipping circuits.

Pin 1	-	+3.6v	- Input
10	-	Bearing Flyback Pulses	- Input
13	-	Clipped Bearing Flyback Pulses	- Output
14	-	Ground	- Input
15	-	Clipped Range Flyback Pulses	- Output
18	-	Range Flyback Pulses	- Input
23	-	+ 25v	- Input
24	-	Blanking Pulses for Raster	- Output
25	-	Bright-Up pulses for Display	- Input
28	-	Bright-Up pulses for Display	- Output
31, 32	-	Ground	

Board 11:- consists of Sawtooth Generators.

Pin 1	-	+ 25v	- Input
4	-	To 10K ohm potentiometer (X)	- Output
6	-	To 10K ohm potentiometer (Y)	- Output
7	-	To 10K ohm potentiometer (Y)	- Output
10	-	- 18v	- Input
13	-	To common of Capacitors wave change switch for Y - Time base	- Output
14	-	Ground	- Input
15	-	To 10K ohm potentiometer (X)	- Output
16	-	Bearing (X) sweep	- Output
18	-	Bearing Flyback pulses	- Output
19 - 22	-	To Capacitors wave change switch for X - time base	- Output
23 - 26	-	To Capacitors wave change switch for Y - time base	- Output
28	-	Range Flyback pulses	- Output
29	-	Range (Y) sweep	- Output

Board 12:- (Upper Rack - Right Hand Board), consists of Output Register 1 with its monitor circuit.

Pin 3	-	Shift Pulses	- Input
6 - 14	-	$\overline{Q}$'s of Register 1 (1 - 9)	- Output
15	-	Clear Pulses	- Input
16 - 24	-	$\overline{Q}$'s of Register 1 (10 - 18)	- Output
25	-	Monitor Signal	- Output
26 - 27	-	$\overline{Q}$'s of Register 1 (19 - 20)	- Output
31	-	Data Word (C)	- Input
32	-	Data Word (A)	- Input
34	-	Data Word (B)	- Input
38	-	Data Word (D)	- Input

Board 13:- consists of the Transfer Circuit for Register 1

Pin 3	-	Output Pulses	- Input
5 - 10	-	$\overline{Q}$'s from Output Register 1	- Input
17 - 23	-	$\overline{Q}$'s from Output Register 1	- Input
27 - 34	-	$\overline{Q}$'s from Output Register 1	- Input

Due to lack of sufficient pin connections, the board was modified to allow connections to be made at the back of the rack. The following numbers relate to the Rear Pin connections.

Pins 9 - 28	-	Output Data to D-to-A Drivers	- Output

Board 14:- consists of Output Register 2 with monitor circuit.

Pin connections similar to Board 12.

Board 15:- consists of the Transfer circuit for Register 2.

Pins 2 - 21	-	$\overline{Q}$'s of Register 2	- Input
30	-	Output Pulse	- Input
38	-	Flag bit from Register 1	- Input

Rear connections

Pins 9 - 28	-	Output Data to D-to-A Drivers	- Output

Board 16:- consists of Output Register 3 and monitor circuit

Pin connections similar to Boards 12 and 14.

Board 17:- consists of Transfer circuit for Register 3.

Pin 2	-	Output Pulse	- Input
5	-	Flag bit from Register 2	- Input
6	-	Flag bit from Register 1	- Input
7 - 27	-	$\overline{Q}$'s from Register 3.	- Input

Rear connections

Pins 6 - 25	-	Outputs to D-to-A drivers	- Output

Board 18:- consists of circuits for driving the set and clear Inputs of the Down-Counter and Run-Length Store.

Rear connections

Pins 2 - 4 - Outputs (1) from Transfer Circuits
(These outputs are from equivalent positions of the three Registers)

Pins 5 - 7	-	Outputs (2) from Transfer Circuits	- Input
8 - 10	-	Outputs (3) from Transfer Circuits	- Input
11 - 13	-	Outputs (4) from Transfer Circuits	- Input
14 - 16	-	Outputs (5) from Transfer Circuits	- Input
17 - 19	-	Outputs (6) from Transfer Circuits	- Input
20 - 22	-	Outputs (7) from Transfer Circuits	- Input
23 - 25	-	Outputs (8) from Transfer Circuits	- Input
26 - 28	-	Outputs (9) from Transfer Circuits	- Input
29 - 31	-	Outputs (10) from Transfer Circuits	- Input
32	-	To Clear FF3 of Down Counter	- Output
33	-	To Clear FF4 of Down Counter	- Output
34	-	To Clear FF5 of Down Counter	- Output
35	-	To Clear FF8 of Down Counter	- Output
36	-	To Clear FF9 of Down Counter	- Output
37	-	To Clear FF13 of Down Counter	- Output
38	-	To Clear FF14 of Down Counter	- Output

Front Connections

Pin 15	-	To Set FF14 of Down Counter
19	-	To Set FF5 of Down Counter
23	-	To Set FF4 of Down Counter
25	-	To Set FF9 of Down Counter
27	-	To Set FF13 of Down Counter
31	-	To Set FF3 of Down Counter
33	-	To Set FF8 of Down Counter

Board 19:- Similar circuits as on Board 18 for driving the remaining elements of the Decoder Circuit.

Rear Connections

Pins 2 - 4	-	Outputs (11) from Transfer Circuits - Input
5 - 7	-	" (12) " " "
8 - 10	-	" (13) " " "
11 - 13	-	" (14) " " "
14 - 16	-	" (15) " " "
17 - 19	-	" (16) " " "
20 - 22	-	" (17) " " "
23 - 25	-	" (18) " " "
26 - 28	-	" (19) " " "
29 - 31	-	" (20) " " "
32	-	To Clear FF11 of Down Counter
33	-	" " FF6 " " "
34	-	" " FF7 " " "
35	-	" " FF10 " " "
36	-	" " FF11 " " "
37	-	" " FF12 " " "
38	-	" " FF1 " " "
39	-	" " FF2 " " "

Front Connections

Pin 15	-	To Set FF12 of Down Counter
16	-	To Set FF3 of Run Length Store
19	-	To Set FF2 of Down Counter
21	-	" " FF7 " " "
23	-	" " FF11 " " "
24	-	To Set FF2 of Run Length Store
27	-	To Set FF1 of Down Counter
29	-	" " FF6 " " "
31	-	" " FF10 " " "
32	-	To Set FF1 of Run Length Store

Board 20:- consists of automatic and manual clear circuits, output register selector and bright-up pulse circuits.

Pin 2	-	Register 2 Monitor signal	- Input
5	-	÷ 10 Output from "Output Clock" board	- Input
6	-	÷ 20 Output from "Output Clock" board	- Input
8	-	T_1 - Transfer Pulse to Register 1	- Input
10	-	Bright-up pulses	- Output
12	-	Output Pulses	- Input
14	-	Register 2 Monitor signal - from selector	- Output
15	-	Register 1 Clear pulses	- Output
19	-	Register 3 Clear pulses	- Output
24	-	Register 3 Monitor signal - from selector	- Output
25	-	Register 2 Clear pulses	- Output
27	-	Selector switch	- Input
28	-	Register 3 Monitor signal	- Input
31	-	T_2 - Transfer Pulse to Register 2	- Input
33	-	T_3 - Transfer Pulse to Register 3	- Input
35	-	Fast Clock	- Input
36	-	Manual Clear Switch	- Input
38	-	Selector Switch	- Input

Board 21:- consists of output clocks and part of the run-length decoder circuit.

Pin 5	-	Fast Clock	- Output
6	-	÷ 10 Output from counter	- Output
7	-	÷ 20 Output	- Output
13	-	Output Pulse	- Output
14	-	Shift Pulses for Down Counter	- Output
17	-	Q_1 of run-length counter	- Input
18	-	Q_1 of run-length store	- Input
20	-	Output Clock 2	
21	-	Q_2 of run-length counter	- Input
23	-	Common terminal of output clock switch	- Output
24	-	Output Clock 1	
26	-	Output Clock 3	

Board 21 cont.....

27	-	Output Clock 4	
28	-	Output Clock 5	
30	-	Q_3 of run-length counter	- Input
31	-	Output Clock 6	
35	-	P_2 of run-length store	- Input
36	-	P_3 of run-length store	- Input
39	-	Fast Clock	- Input

Board 22:- consists of the 14-stage Down-Counter, 3-stage run length counter, and one stage of the run length store. Rear and Front connections are used.

Rear Connections

Pin 4	-	Clear Signal for F/F1 of Down-Counter
6	-	" " " F/F10 " " "
7	-	" " " F/F9 " " "
9	-	" " " F/F2 " " "
16	-	" " " F/F11 " " "
17	-	" " " F/F12 " " "
24	-	" " " F/F14 " " "
25	-	" " " F/F13 " " "
27	-	" " " F/F7 " " "
28	-	" " " F/F8 " " "
31	-	" " " F/F3 " " "
33	-	" " " F/F5 " " "
34	-	" " " F/F6 " " "
36	-	" " " F/F4 " " "

Front Connections

Pins 3 - 13	-	Q_1 - Q_{11} of Down Counter	- Output
14	-	Clock for Counters	- Input
15 - 17	-	Q_{12} - Q_{14} od Down Counter	- Output
19	-	Q_1 of run length store	- Output
22 - 35	-	Clear signals for Down Counter	- Input
36	-	P_1 of run length store	- Input
37 - 39	-	Q outputs of run-length counter	- Output

Board 23

5-bit Digital-to-Analog Converter

Pin 14	-	Bit 3 to D-to-A	- Input
15	-	NSMB to D-to-A	- Input
16	-	MSB to D-to-A	- Input
23	-	+ 25v	
24	-	Bit 2 to D-to-A	- Input
25	-	L.S.B. to D-to-A	- Input
31	-	Analog Signal	- Output

Board 24

9-bit Digital-to-Analog Converter

Pin 1	-	+ 25v	
11	-	Bit 4 to D-to-A	- Input
14	-	Bit 2 to D-to-A	- Input
15	-	Bit 5 to D-to-A	- Input
18	-	Bit 3 to D-to-A	- Input
20	-	Bit 7 to D-to-A	- Input
21	-	L.S.B. to D-to-A	- Input
23	-	MSB to D-to-A	- Input
24	-	NMSB to D-to-A	- Input
25	-	Bit 6 to D-to-A	- Input
30	-	Analog Signal	- Output

Decoupling

On all boards containing digital integrated circuits, supply decoupling is performed by using a 47 micro-farad tantalum and several 0.1 micro-farad ceramic capacitors. The number of 0.1 uF capacitors is determined by the number of I.C's per board; on the average one capacitor per 6 circuits is used.

Control Panel

The control panels for both racks are shown in Figure A.15. The functions of the controls are as follows;

Upper Panel

Display Outputs: X, Y and Z are fed to the equivalent inputs of the display oscilloscope.

Manual Clear: Push-to-make switch which clears all the output registers.

Output Registers Selector: Wave-change switch which includes either 1, 2 or 3 registers in the system.

Output Clock selector: Wave-change switch which selects the output clock rate. The main shift clock is divided by 2, 3, 4, 6, 8 and 12 with the highest frequency on position 1 of the switch.

Targets Out (Count): BNC socket for connecting to a counter. These pulses are produced by the bright-up pulses generator and indicate the number of targets displayed.

Lower Panel

Voltage sockets: values as shown.

Code/No-Code Switch: Miniature two-way switch which enables or inhibits the run-length coding operation. On the panel UP signifies CODE.

Video In: BNC socket for receiving video signal from photomultiplier.

Targets In (Count): BNC socket suitable for connecting to a counter. These pulses are produced by the Target Detector Circuit.

Range Pulses: BNC socket; these are the flyback pulses from the range sweep generator and are used as time markers when counting the number of targets fed in and shifted out.

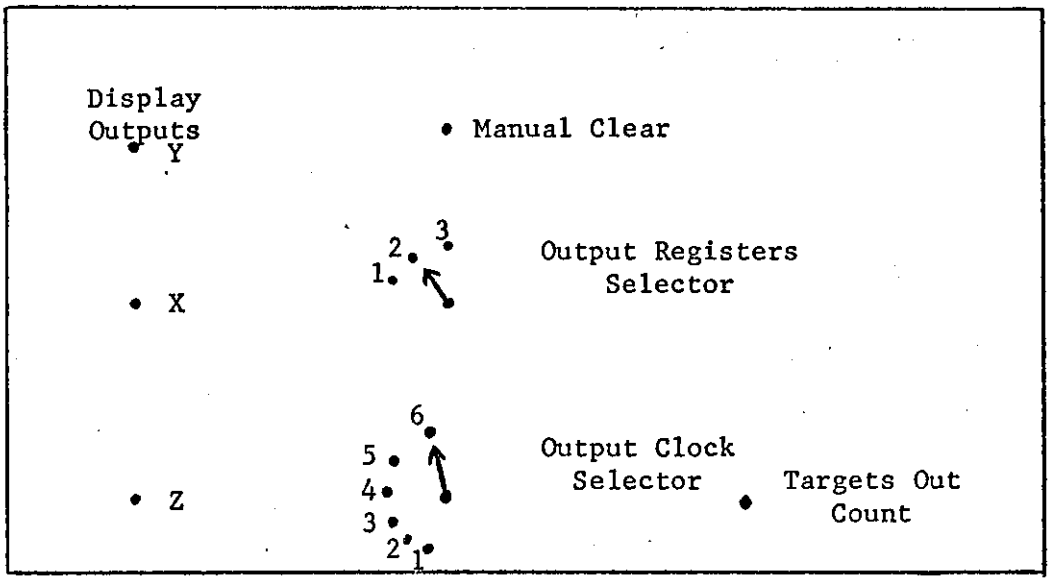
Range Sweep: BNC socket; from the range sawtooth generator to the Y input of the Raster Generating oscilloscope.

Bearing Sweep: as above.

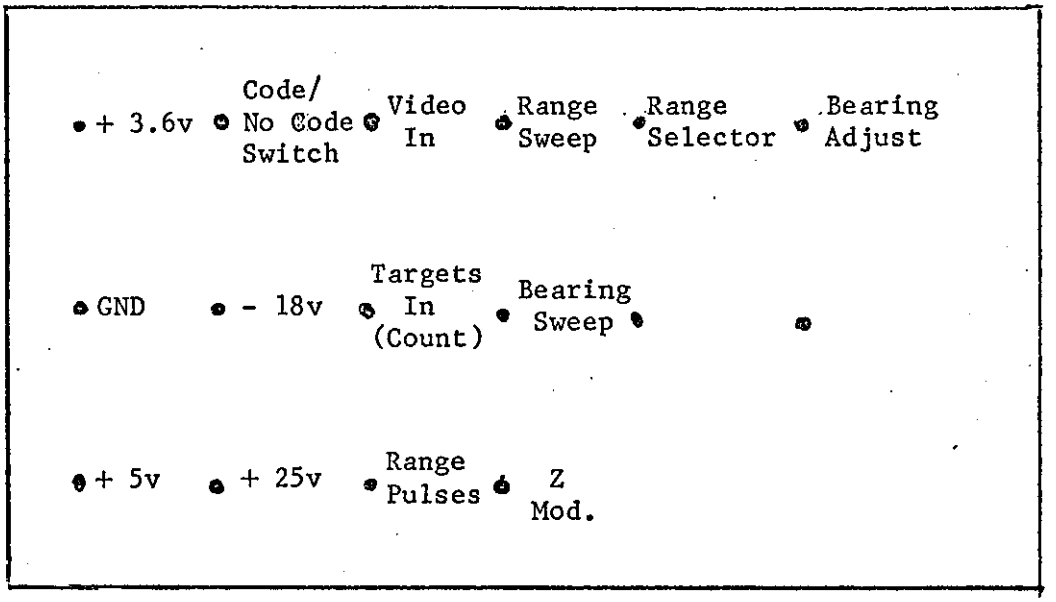
Range Selector: a wave change switch, which includes a selected capacitor in the sawtooth circuit, and a variable resistor which provides fine tuning.

Bearing Adjuster: as above.

Z. Mod: BNC socket; flyback blanking pulses for Raster Generator oscilloscope. This signal is not used normally as the digital blanking is sufficient. However, if direct reproduction of the scanned pattern is required then this signal is taken to the Z terminal of the oscilloscope.



Control Panel for Upper Rack



Control Panel for Lower Rack

Figure A.15: Schematic Diagram of Control Panels.

REFERENCES: APPENDICES

1. Goode H.H. and Machol R.E.: "Systems Engineering", McGraw-Hill, 1957.

2. Ferranti: "E - Line Transistor Applications 1971.

3. Hoeschele D.F.: "Analog-to-Digital/Digital-to-Analog Conversion Techniques, New, York, John Wiley & Sons Inc. 1968.

ADDITIONAL REFERENCES

Other articles were consulted during the research into this project. Fortunately a bibliography on all aspects of Data Compression systems has been compiled. This document (4) contains references to nearly all the relevant publications since Kretzmer's work in 1952.

4. Wilkins L.C. and Wintz P.A.: "Bibliography on Data Compression, Picture Properties and Picture Coding". I.E.E.E. Trans. on Information Theory, VOL IT-17, No.2, pp. 180-197, March 1971.

In addition the following references on queueing theory are useful for background information.

5. Kendall D.G.: "Some Problems on the Theory of Queues". J. Royal Statistical Society, Vol. 13, No. 2, pp 151-185, 1955.

6. Chu W.W.: "Buffer Behaviour for Poisson Arrivals and Multiple Synchronous Constant Outputs".
IEEE Trans. on Computers, Vol. C-19, No. 6, pp 530-534, June 1970.

7. Lindley D.V.: "The Theory of Queues with a Single Server".
Proc. Cambridge Philosophical Society, Vol. 48, No. 2, pp 277-289, April 1952.