An Investigation into the Effect of Dry Bake on the Solderability Degradation of Electrodeposited Tin Finishes

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Abstract—The solderability of component termination finishes degrades upon storage due to the combined effects of surface contamination, oxidation, corrosion and/or intermetallic compound (IMC) formation at the interface between substrate and finishes. Such solderability degradation impinges on the shelf-life of the electronics components and hence demands an indepth understanding to ensure high reliability Pb-free soldering. This paper is concerned with the effect of the 155°C dry bake precondition on the accelerated ageing of bright Sn electrodeposited termination finishes over Cu substrates. Two coating thicknesses, 2.5 µm and 9 µm, were studied as-received and dry baked for 4 hr and 16 hr as per industrial standards and analysed with respect to their solderability, microstructural and compositional characteristics. It was found that, with increasing dry bake time, both the thickness variations experienced continued solderability degradation, with only the 2.5 µm thick coatings failed after 16 hr of dry heat. Such a loss of solderability was primarily contributed to the exposing of Sn-Cu IMCs. The thickness safety margin (i.e. maximum IMC thickness) for the dry bake condition (16 hr) of the given bright Sn samples was identified to be around 2.5 µm, which could provide a guidance for any future industrial initiative to further reduce coating thickness. Besides, the dry bake conditions have proven to be a consistent and reliable precondition approach for the Sn-based metal finishes.

Keywords—Solderability; Preconditioning; Dry bake; Wetting Balance; Termination finishes.

I. INTRODUCTION

The solderability of electronics components and its degradation during storage pose a serious issue in the challenge of defect-free soldering of electronic assemblies. This is especially true in a transition era towards Pb-free technology, where the prevailing Sn-Ag-Cu (SAC) alloy solders exhibit inferior wetting abilities and entails narrower process windows (cf. conventional Sn-Pb solders) to merit adequate wetting. Furthermore, the predominant use of miniaturised surface mount (SMT) components exacerbates the issue due to greater difficulty of inspection, rework and repair of solder joints, as well as the need to use milder fluxes because of cleaning difficulties. These factors require the manufacturers to take a

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responsible approach towards ensuring the integrity of the products, whilst making effective trade-offs to minimise materials and process costs [1].

Solderability is defined as the total suitability of a termination surface for industrial soldering, which can be further divided into three aspects: wettability, thermal demand and resistance to soldering heat [1]. The solderability degradation of Sn-based metal finishes have been attributed, primarily to interfacial Sn-Cu IMC growth and secondarily to surface oxidation [2]. However, open literature concerned with the solderability degradation and precondition of Sn-based termination finishes is immensely scarce and outdated, normally dating back to pre-1990s [3-5]. The present study constitutes one part of a cooperative attempt between Loughborough University (UK) and Huawei (China) to understand the subject from a contemporary materials science viewpoint, with specific focuses on the implications and suitability of various accelerated ageing preconditions for the solderability degradation simulation of termination finishes.

Since the publication of J-STD-002/003 standards in the early 1990s, steam conditioning, as a precondition method recommended for the accelerated, simulative ageing of component/PCB terminations, has led to the greatest amount of controversy [3]. OEMs tended to adopt it as per the standards, whilst component/PCB suppliers criticised it to be too severe to represent the entire shelf lifetime of Sn-based coatings. Even though the updated versions of industrial standards such as EIA/IPC/JEDEC J-STD-002D (2013) still recommend steam precondition, there has been a general interest to replace it with other conditioning methods. Such a need was largely attributed to the findings that steam ageing tends to give results too erratic and difficult to correlate to actual natural ageing [6]. Instead, dry bake at 155°C has been recommended. The present study explores the efficacy of the dry bake precondition in the accelerated ageing of commercial bright Sn electrodeposits. Two coating thicknesses have been evaluated, i.e. 2.5 µm and 9 um, with the smaller thickness selected to promote rapid loss of solderability, as well as to identify the thickness safety margin of the dry bake preconditions for the given electroplated Sn finishes. The solderability of the as-received and dry-baked

samples has been evaluated using wetting balance in the solder bath mode. The morphological and compositional information of the samples have been acquired from both the surface and cross-sectional views.

II. EXPERIMENTAL PROCEDURES

A. Specimen Preparation

The bright Sn deposited test coupons employed in this study were electroplated under galvanostatic conditions using a proprietary process, on Cu sheet substrates following a configuration (20 mm \times 5 mm \times 0.2 mm) illustrated in Fig. 1. The test pieces were separately stored in sealed transparent polyethylene (PE) bags and received for analysis 18 days after electrodeposition. The coating thickness was monitored using an X-ray fluorescence (XRF) spectroscopy (Orbis PC Micro-XRF Elemental Analyzer, EDAX, USA) equipped with an X-ray source of monochromatic Rh K α radiation (30 µm aperture, 30 Kv, 1,000 µA) and a 25 µm Al filter. This was corroborated from cross-sectioned observations explained in the next.



Fig. 1 Schematic diagram illustrating the electroplated test coupons used in this study

B. Preconditioning

Dry bake conditioning was conducted at 155° C with bare testpieces positioned in a fanned oven in ambient atmosphere, for periods of 4 hr and 16 hr as per the industrial standards. No specific pretreatment or post-treatment was conducted.

C. Wettability test

Wettability test was performed using a Robotic Process Systems Six-Sigma wetting balance tester. Prior to analysis, the equipment was calibrated with respect to load cell reading, flux surface position, blot paper surface position and solder bath surface position. The wetting balance tests utilised an optimised condition, with solder bath of SAC305 alloy operating at 245°C, a ROL0 flux (Alpha rosin flux 800), immersion depth of 7 mm, immersion/emersion speed of 25 mm/s. a dwell time of 5 s and no pre-heat. At least 10 testpieces were assessed of each condition for data accuracy were and representativeness. Test pieces analysed straightforward without any pretreating action. Wetting curves were obtained, from which readings of zero cross time (ZCT) and maximum wetting force (F_{max}) were extracted.

D. Metallographic study /FIB/SEM

The cross-sectioned samples were prepared for SEM/EDX analysis complementarily using either standard metallographic approach or focused ion beam (FIB) The milling. metallographic method involved mounting in a two-part Struers SpeciFix-20 epoxy resin and grinding using SiC paper down to p1200 grit size. Following grinding, polishing was conducted using 6 µm and 1 µm diamond paste, culminating at a final chemical etching step in 2 v/v % hydrochloride solution for 15 - 20 s. Since the Sn deposits appeared to be removed more rapidly than Cu during polishing, small scratches on the Cu surface were tolerated to ensure a well-polished state of the Sn with minimal surface relief. Prior to SEM analysis, the samples were sputtered with gold on a 90 s exposure time to ensure electrical conduction. Alternatively, FIB milling was carried out using a dual beam (FEI Nova 600 NanoLab) instrument, fitted with a liquid gallium ion source and operating at 30 kV accelerating voltage. 'Pt strap' deposition was carried out in situ, via ion beam assisted chemical vapour deposition, to protect the sampling area surface from Ga+ implantation damage. FIB milling involved coarse milling at a 3 nA beam current, followed by smooth milling at 1 nA then at 300 pA. It is necessary to compensate for the convergence angle of the focused ion beam by tilting the sample small angles from the optic axis (i.e. $+1.5^{\circ}$). SEM analysis was conducted using either a Leo 1530VP field emission gun SEM or in the dual beam mode stated above. The morphological and compositional details of the samples were acquired from both surface and cross-sectional views.

III. RESULTS

A. Effect of Dry Heat on Solderability

Fig. 2 shows representative wetting force-time curves of 2.5 µm and 9 µm thick bright Sn electrodeposits after having subject to varied periods of dry bake condition at 155°C. Two subtracted solderability indices, zero cross time (ZCT) and maximum wetting force (F_{max}) , were presented in Fig. 3, which give information about the speed and the degree of wetting respectively. ZCT refers to the measured wetting force returning to zero, whilst Fmax denotes the maximum wetting force achieved on the time-force curve. For the as-received state (i.e. 18 days after electrodeposition), the 2.5 μm and 9 μm thick testpieces demonstrated similar wetting curves, with comparable and minimally variable ZCT as 0.96 s and F_{max} as 0.42 mN/mm, indicative of excellent rate and degree of wetting. Upon the application of dry bake condition for 4 hr, the 2.5 μ m group saw a slight extension of the average ZCT up to 1.05 s and a drop of F_{max} to 0.36 mN/mm. Albeit not severe, such a toll on the solderability degradation is largely attributable to the surface oxidation artificially promoted by dry heat, which slows down the solder spreading (meniscus rise) and reduces the degree of reactive wetting. The overall solderability for such a condition is still deemed as satisfactory. With a further increase of dry bake time to 16 hr, the wetting curves of the 2.5 µm samples exhibited only the initial trench corresponding to the buoyant force upon immersion of the testpiece, but failed to show any significant meniscus rise (i.e. positive wicking). Also, the variations of the wetting curves became more pronounced compared with those less artificially aged. These data imply no

wetting, owing to the penetration of Sn-Cu IMC growth to the Sn coating surface. This aspect will be further elaborated on in the next from a metallographic viewpoint. For the 9 μ m thickness samples, with increasing dry heat time from 0 hr through 4 hr to 16 hr, the average ZCT saw a steady increase from 0.96 s to 1.04 s, and further to 1.69 s, whilst the average Fmax was decreased from 0.42 mN/mm to 0.35 mN/mm and further to 0.23 mN/mm. The survival of the 9 μ m thickness samples from the solderability test after 16 hr of dry heat points to the possibility that the IMC growth had not been reaching the coating surface. Therefore, the degradation of solderability of these samples is thought to be due largely to the artificial surface oxidation.

B. Effect of Dry Heat on Deposit Surface Morphology

Fig. 4 shows the representative surface morphology of 2.5 um thick and 9 um thick bright Sn electrodeposits after having subjected to various periods of dry heat condition at 155°C. For both thickness variations, the as-received deposit surface morphology was generally smooth and levelled, indicative of the efficacy of brightening agents on Sn electrocrystallisation. With a dry heat ageing time of 4 hr, the 2.5 µm thick deposit surface saw the advent of discrete-distributed, irregular-shaped and coarse features with an in-plane dimension of a few micronmetre. EDX point analyses conducted on several individual features confirmed that these were Cu₆Sn₅ IMCs, which point to the locations where Sn-Cu IMCs had been growing at faster speeds, penetrating the pretinned surface and exposing themselves. At this stage the coating appearance retained bright and metallic grey, without any appreciable change by visual assessment compared to that of the asreceived counterparts. With the dry heat ageing time increased from 4 hr to 16 hr, the 2.5 µm thick deposit surface became



Fig. 3. Bar charts showing the a) zero-cross time (ZCT) and b) maximum wetting force for 2.5 μm and 9 μm thick pure Sn electrodeposits as a function of dry bake ageing time.



Fig. 2. Representative wetting curves of bright Sn electrodeposits: 2.5 μ m (a-c) and 9 μ m (d-f) thickness a) & d) as-received, b) & e) dry bake for 4 hr and c) & f) dry bake for 16 hr.

matte and yellow-whitish hued by visual assessment. The corresponding surface morphology was universally faceted and wedge-shaped. EDX point analyses indicated that most of the Sn electrodeposited layer had been transformed into Sn-Cu IMC layers. For the 9 µm thick Sn deposits, with increasing dry heat time from 0 hr (i.e. as-received) to 4 hr and further to 8 hr, there was not evident change either from visual assessment or from micron-scale electron microscopic observations. The 'exposing' of the Sn-Cu IMCs is thought to be the major cause of coating wettability degradation. This will be further corroborated by cross-sectional observations presented in the next section. For industrial practice, a clear point emerging from the morphological studies is that the coating appearance of Sn-based finishes could serve as an effective indicator for the loss of solderability where the exposing of IMCs is the dominant degradation mechanism.

C. Effect of Dry Heat on Interfacial IMC Evolution

The cross-sectional images of 2.5 µm and 9 µm thick pure Sn electrodeposits over Cu substrate as a function of dry heat ageing time are shown in Fig. 5. The 'as received', 2.5 µm thick Sn coatings exhibited a columnar grain morphology. An uneven and wedge-shaped IMC layer had formed at the coating-substrate interface, with an average thickness of ca. 200 nm and the thickest region at ca. 500 nm after 18 days of electrodeposition. This was accompanied by the presence of discrete IMC particles with an average size of tens of nanometers, distributed alongside the columnar grain boundary spanning the coating thickness. Kirkendall voiding was observed upon IMC formation. EDX point analyses suggested the IMCs were largely Cu₆Sn₅. With an increase in the dry bake time through 4 hr to 16 hr, the IMC layer saw increases in the average thickness to 1.8 µm and further to 2.3 µm, indicative of the nearly all consumption of the Sn coating. It is

also noteworthy for the dry baked samples that the IMC layers contained duplex layers, with the lower uniform layer EDX assigned as Cu₃Sn and the upper uneven layer as Cu₆Sn₅. It remains questionable in terms of whether the IMC growth had progressed to completion., to which in-depth microstructural and compositional investigations are ongoing in the attempt to provide answers. For the 9 μ m thickness samples, the as received state showed IMCs with sizes comparable to that of the 2.5 μ m thickness to 1.9 μ m and further to 2.4 μ m. Such a growth kinetics of IMC layer was also in line with that of the 2.5 μ m group. This implies that the coating thickness did not seem to play a significant role in the IMC growth.

IV. DISCUSSION

It can be drawn from the present study that, the exposing of interfacial IMC formation gives rise to complete solderability loss of Sn metal finishes, whilst surface oxidation also plays a role that is less significant but steady throughout the whole process. The exposing of IMCs can be easily observed either from visual assessment or from macroscopic microscopy. However, a systematic gauge repeatability & reproducibility (Gauge R & R) study shall always be adopted with a precondition that is able to demonstrate consistent data. It can be drawn that the dry bake condition appeared to give inerratic and reproducible results, which represents a clear advantage over conventional steam conditioning [6].

The industrial standards recommended dry bake precondition at 155° C for 4 hr (J-STD-002D and IEC 60068-2-20/69) and for 16 hr (IEC 60068-2-20/69) to simulate natural



Fig. 4. Secondary electron images illustrating the representative surface morphology of bright Sn electrodeposits: 2.5 μ m (a-c) and 9 μ m (d-f) thickness a) & d) as-received, b) & e) dry bake for 4 hr and c) & f) dry bake for 16 hr, with insets of magnified images.



Figure 5. Secondary electron images illustrating the representative cross-sectional morphology of bright Sn electrodeposits: 2.5 μ m (a-c) and 9 μ m (d-f) thickness a) & d) as-received, b) & e) dry bake for 4 hr and c) & f) dry bake for 16 hr, with insets of magnified images.

ageing. It needs to be reiterated that a precondition shall neither be too relaxed to lose the discriminating capabilities against inferior samples, nor be too severe to screen out those satisfactory ones. It can be appreciated from the present study that thin coatings (e.g. down to 2.5 µm thickness) appeared to hardly survive the 16 hour trials due to reaction of the Sn coatings into Sn-Cu IMC structures. It has been suggested [2] that, albeit being readily wet on its own, the Sn-Cu IMC surface tends to form tenacious oxide which practically renders common fluxes (such as rosin-based ROL0 or ROL1) ineffective. It is therefore necessary to recommend an adequate coating thickness to accommodate interfacial IMC growth within the designed coating shelf-life. This also stands valid as thinner coatings are more susceptible to Sn whisker formation, which represents another dimension of Pb-free reliability issues [7]. Besides, it was found for the present Sn metal finish system that, the maximum IMC thickness after 16 hours of dry bake condition at 155°C was ca. 2.4 µm. Therefore, theoretically a coating thickness appreciably beyond such a value may survive the 16 hr dry heat precondition. Such a knowledge may contribute to the initiative of thickness reduction for minimising material usage and process time of electrodeposition. Long term nature ageing study is being conducted at Loughborough University, which will provide an insight into the question as to what extent the dry bake conditions would simulate the actual natural ageing.

V. CONCLUSIONS

This paper investigated the effect of the dry bake preconditions on the accelerated ageing of bright Sn electrodeposited termination finishes over Cu substrates. Two coating thicknesses, 2.5 μ m and 9 μ m, were studied as-received and dry baked at 155°C for 4 hr and 16 hr. It was found, with

increasing dry bake time, both the thickness variations experienced continued solderability degradation, with only the 2.5 µm thick coatings failed after 16 hr of dry heat. Such a loss of solderability was thought to relate to the exposing of Sn-Cu IMCs, the growth of which had nearly consumed the entire Sn coatings. The thickness safety margin for the dry bake condition (16 hr) of the given bright Sn samples was identified to be around 2.4-2.5 µm. This assumption was made based on the finding that the maximum IMC thickness for the 9 µm thick coatings after 16 hours of dry bake was around 2.4-2.5 µm. In any attempt to minimise Sn coating thickness, it is, however, recommended to allow for a certain thickness in addition to the safety margin for reducing the risks of preferential IMC growths at locations, and in the meanwhile for minimising Sn whisker formation propensity. Besides, the aforementioned dry bake conditions have proven to be a consistent and reliable precondition approach for the electrodeposited Sn-based metal finishes.

REFERENCES

- L. Colin, "Quantitative solderability measurement of electronics components, parts 1-6", BCR Information, Applied Metrology, Commission of the European Communities, 1991.
- [2] H. L. Reynolds & J. W. Morris, "The role of Cu-Sn intermetallics in wettability degradation", Journal of Electronic Materials, 24 (10), 1995, p. 1429-1434.
- [3] G. C. Wilson, "A review of accelerated ageing of printed boards with respect to solderability", Circuit World, 25, 1978, p. 287.
- [4] K. M. Line, E H. Friend and D. Schoenthaler "Accelerated aging temperature evaluation." Presentation to Joining Processes Committee. IPC Meeting, Hollywood, FL, April 1989.
- [5] D. Schoenthaler, 'The New J-STDs', Circuits Assembly, 4, 1993, p. 26-26.

- [6] D. Hillman, D. Romm, T. Krueger and B. Russell, "Replacing Steam Preconditioning, An EIA/IPC Designed Experiment: Confirmation Trial", 2010.
- [7] J. Wang, M. A. Ashworth & G. D. Wilcox, "An investigation into the role of lead as a suppressant for tin whisker growth in electronics", IEEE Transactions on Components, Packaging and Manufacturing Technology, 4(4), 2014, p. 727-740.