Process sensitivities and interface optimisation of CdTe solar cells deposited by close-space sublimation

by

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Contents

Abstract

In a world where the need of clean and sustainable energy production has become a necessity, photovoltaic (PV) solar cells can provide a clean and cost-effective alternative to conventional fossil fuel energy sources. Recent technological advancements in PV technologies have improved their financial viability, making the PV industry the leading energy market at the moment in new installations. Thin film solar cells can potentially further reduce manufacturing costs through less material requirements and simpler deposition methods.

CdTe solar cells are currently the most commercially successful thin film technology which have secured approximately half of the thin film market share. However, CdTe solar cells have only achieved 70% of their theoretical maximum efficiency, making this a promising area of research in the quest for improving the financial viability of this technology. This thesis aims to investigate possible ways of improving the performance of CdTe solar cells through interface optimisation.

Firstly, for the purpose of this thesis, a homemade closed spaced sublimation system (CSS) was designed and implemented for cadmium telluride deposition. Using CSS, a repeatable baseline process was realised, in order to further investigate the interface optimisation through comparative studies. The process presented in the first working chapter was the first baseline process for CdTe solar cells, achieved in Centre for Renewable Energy Systems Technology (CREST). Device optimisation included introduction of O_2 in Ar during CdTe deposition by CSS and it was found that O_2 when introduced during sublimation, acts as a nucleation aid leading to a reduction of pinhole formation. It also increased homogeneity providing better process control of sublimation procedure through CdTe grain size reduction. Additionally, $CdCl_2$ activation treatment optimisation showed that the electrical performance is interlinked with the amount of evaporated $CdCl_2$ used during the activation process of the

device. Interface optimisation was divided into three parts: absorber/emitter, window/emitter and absorber/back contact interface.

For the absorber/emitter interface, the effect of adding chlorine during the CdS chemical bath deposition followed by the effect of the cooling cycle during the $CdCl_2$ activation treatment were investigated. Cl was found to act as a doping mechanism for CdS thin films and enhance the V_{OC} and the FF through reduced interface recombination. The study on the effect of cooling cycle showed that the cooling cycle has a big impact on the formation of self-compensating defects which can lead to recombination of carriers either in CdTe or in CdS. Photoluminescence (PL) imaging was also found to be a useful tool which can provide qualitative information about the uniformity and the effectiveness of the $CdCl_2$ treatment on CdS/CdTe devices.

For the window/emitter interface, the experiments revolved around the effect of reducing the CdS thickness, the effects of adding a high resistive transparent layer (HRT) in the CdS/CdTe structure and their possible utilisation as alternative emitters for CdTe devices. Surprisingly, it was shown that reducing the thickness of the CdS in the baseline CdS/CdTe structure, does not improve the current density. The use of SnO_2 as an HRT buffer allowed the reduction of CdS film thicknesses without the formation of weak localised diodes. Through the investigation of SnO_2 and ZnO used as buffer layers, it was illustrated that even though substitution of the CdS buffer with an HRT increases the current density, not all HRT's can be used effectively as emitters. ZnO buffer layer proved to be a more suitable candidate for CdS buffer substitution.

The interface optimisation of the absorber/back-contact focused on the role of Cu on the performance, controllability and stability of non-etched CdTe solar cells and the implementation of a new baseline process, based on substrate configuration of CdS/CdTe devices. Introduction of Cu at the back contact without etching, was found to induce a moderately doped surface which creates a tunnelling junction without affecting the Schottky barrier height. This proved that etching CdTe devices is not necessary to cause performance improvements. However, Cu was found to induce a significant degradation even though devices were kept in the dark. Using a substrate baseline process the effects of a Cu-

free absorber/back were investigated. MoO_x was found to be a promising candidate as a back-contact buffer layer. Careful adjustment of the O_2 concentration showed a transition from metallic to semi-metallic properties, affecting the resistivity, carrier concentration and optical properties of MoO_x films, properties which were found to affect device performance.

Further investigations are proposed as potential routes for efficiency improvements, specifically on CdS doping with group III elements, and optimisation conditions of ZnO and MoO_x buffer layers.

Key words: CdTe solar cells, close-space sublimation, interface optimisation, emitter/absorber interface, window/absorber interface, absorber/back-contact interface, Cl doping, ZnO buffer, Cu doping, MoO_x buffer.

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Chapter 1. Photovoltaic Technology

1.1 Introduction

We live in an era which humanity has enjoyed unprecedented levels of medical, technological and economic achievements. However, these came at a great cost. In 2017, the world's energy demand reached 13,511 Mtoe which is the equivalent of 157,132 TWh [1]. This staggering energy supply is generated heavily by fossil fuels (*Fig. 1.1),* which emit high concentrations of CO_2 and other greenhouse gasses. This has led to an abnormal increase of earth's average temperatures which can have devastating environmental effects [2]. As the word strives to sustain its thirst for continuous growth, we are in the process of destroying our planet.

In 2019 the latest IPCC report suggested that if humanity wants to achieve the 1.5℃ temperature increase target and avoid global environmental catastrophe, anthropogenic CO_2 emission must be reduced by 45% by 2030 [3]. Fossil fuels as an energy source is no longer an option if we want to avoid the pending environmental and social-economic disaster.

Assuming that humanity will not reduce its immense consumption of energy, there is a necessity for energy generation with zero CO_2 emissions. Renewable energy sources such as wind, hydropower and solar energies can provide the only viable option at the moment for a sustainable future and aid in the quest of healing the planet. Solar energy in particular has the largest potential, given the amount of energy supplied from the Sun. The Earth receives on average approximately 5,000 times more energy (833.6×10^6 TWh [4]) per year than the global energy demand and this makes the utilization of this vast amount of 'clean' energy an obligation.

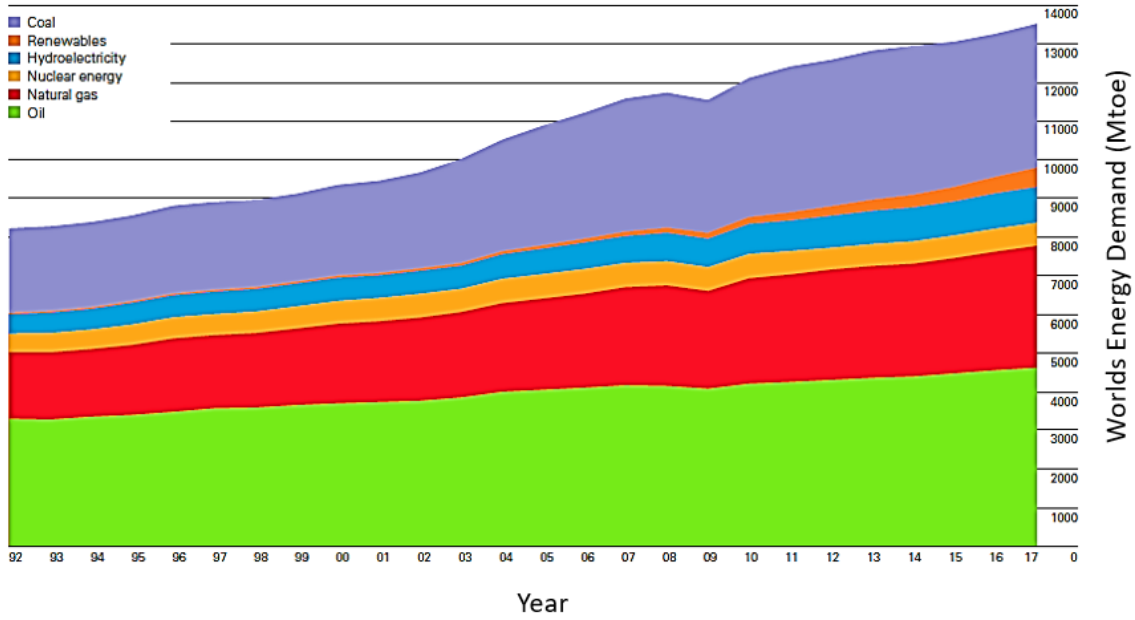

Fig. 1.1: Energy supply from different energy sources [2].

1.2 Overview of Photovoltaic Market

In 1839 a young French physicist was experimenting in his father's laboratory with silver coated platinum electrodes. Edmund Bequerel observed that once the electrodes were illuminated an electric current was generated. This effect was named the photovoltaic effect and since then it has ignited the spark which led to today's photovoltaic (PV) research and industry [5].

Over the last two decades, the PV market has seen an incredible expansion, with global installed PV capacity in 2017 reaching over 404 GW from just 9.2 GW in 2007 (*Fig. 1.2*) [6]. Recent technology improvements and installed system cost reductions have improved the viability of solar PV by reducing the levelized cost of electricity (LCOE) from ~ 0.36 to 0.10 $/kWh (73%) between 2010 and 2017 [7]. This, along with the introduction of supporting policies has made the PV industry the leading energy market at the moment with new installations exceeding 95 GW in 2017, more than coal, natural gas and nuclear power combined [8]. In 2018 utility scale PV LCOE, finally became cheaper than conventional sources reaching ≥ $40/MWh [9]. This makes the PV industry an environmentally and financially sensible direction to follow for a cleaner future.

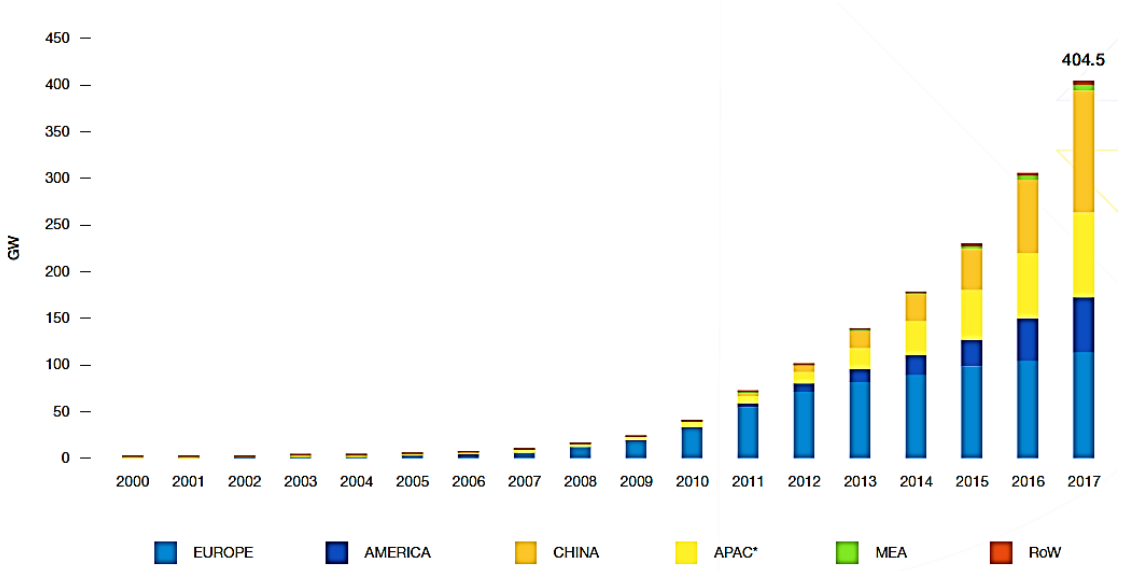

Fig. 1.2: Total global PV capacity from 2000 to 2017 [6].

1.3 Solar cell operation

1.3.1 Semiconductors

Solar cells convert sunlight directly to electricity by absorbing photons in one or more semiconductor materials. This conversion is based on the photovoltaic effect with an efficiency that depends significantly on the material of the semiconductor that the solar cell utilises. The theoretical maximum efficiency of a single junction solar cell when taking into account the available solar spectrum and radiative recombination is around 33% [5]. This theoretical maximum efficiency is calculated for a semiconductor with an optimum bandgap (Eg) of around 1.4 eV for AM 1.5G spectrum (*Fig. 1.3*).

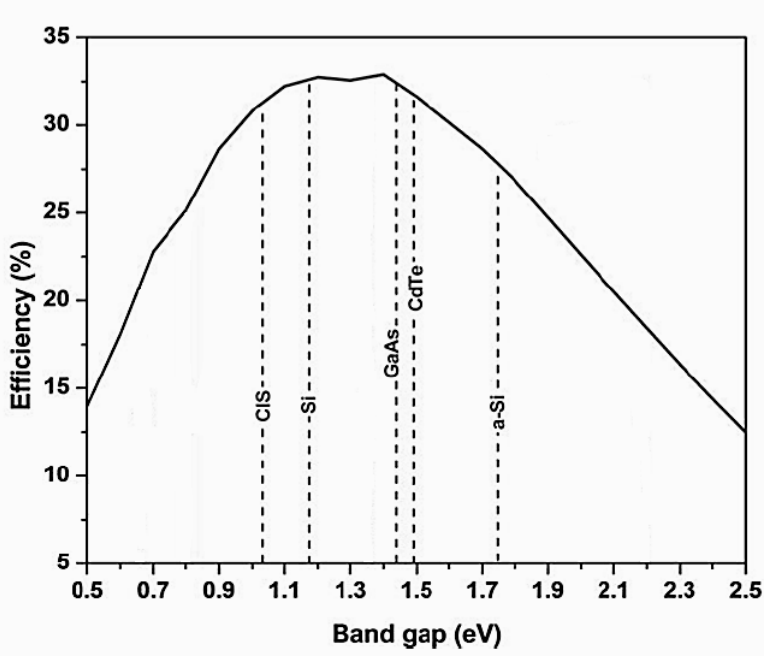

Fig. 1.3: Efficiency vs Bandgap at AM 1.5 spectrum.

Semiconductors are materials which have an electrical conductivity between a metal and an insulator, and generally exhibit an Eg between 0.5 to 3.0 eV. Free electrons are excited in a semiconducting material from penetrating photons, when the available photon energy $E = hv$ (where h is the Planck's constant and v is the photon frequency), is larger than the Eg of the material. This process promotes an electron from the valence band (VB) to the conduction band (CB) leaving a corresponding hole in the valence band (*Fig. 1.4.a*)

For direct bandgap materials, the above statement is true, however in indirect bandgap materials this process is not sufficient (*Fig. 1.4.b*). Excited electrons in this case require momentum to cross from the valence band to the conduction band which photons do not possess. The required momentum in these materials is supplied by a phonon (lattice vibration) which must occur at the same time as the photon strikes the semiconductor. For this reason, indirect bandgap semiconductor materials (such as cSi) exhibit lower optical absorption compared to direct bad gap materials such as CdTe and $Cu(InGa)Se_2$.

In either case a successful separation of the generated electron-hole pair before recombination (electron relaxes to its original state) leads to a potential difference which can be utilized to perform useful work.

The requirements for a solar cell to achieve its maximum theoretical efficiency are stated below:

- All of incident photons with energy of E > Eg are absorbed
- Each photon absorbed generates one electron - hole pair
- All the generated hole-pairs do not recombine except radiatively
- All excited charges are completely separated by the p-n junction's electric field
- Charge is transported to an external circuit without any losses

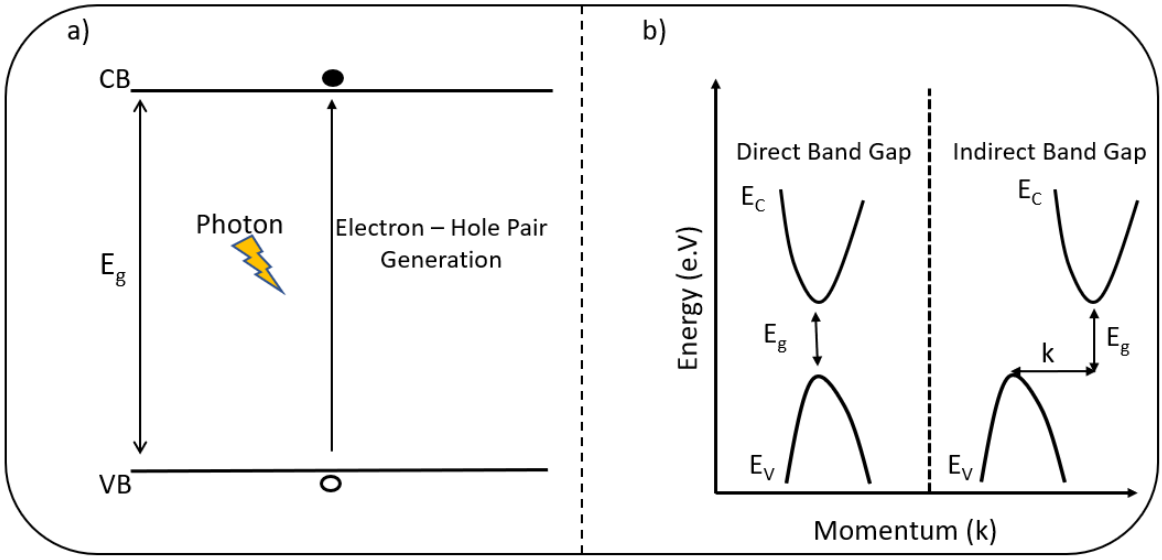

Fig. 1.4: a) Generation of electron – hole pairs during the photovoltaic effect

b) Direct and indirect bandgap semiconductor diagram

1.3.2 The P-N Junction

To increase the probability of a successful charge separation two semiconducting materials with different doping levels are interconnected. These interconnected partners can be made from either the same, or different semiconducting materials. In the first case this configuration is called a

homojunction, while in the later is called a heterojunction. The most conventional photovoltaic device (c-Si) utilizes the principle of a P-N homojunction. However, the basic principles outlined below are true for every configuration.

In a P-N junction one of the semiconductors is doped n-type (able to provide electrons easily - donor) and its partner is doped p-type (able to provide holes - acceptor) [10]. When these materials are brought into intimate contact, diffusion of electrons and holes into the opposite side creates a region depleted of free carriers and a field is established. This region is called the depletion region (*Fig. 1.5)*. In an ideal scenario, it is highly desirable in order to minimize recombination for generation of electron – hole pairs to occur in this region [11].

Fig. 1.6 shows the energy band diagram of a c-Si solar cell before and after the intimate contact between the two differently doped semiconductors is made. On an n-type semiconductor, the Fermi level (E_F) lies closer to the conduction band while on the p-type material, $E_{F\,is}$ closer to the valence band. Upon contact and charge exchange, the device reaches an equilibrium and the E_F between the two semiconductors align forming a junction. The difference between the two work functions of n-type and p-type is defined as the built-in bias (V_{bi}) of the device, and as seen from *eq. 1.1* is a function of the donor and acceptor densities of the two semiconductors.

(*eq. 1.1*)

$$V_{bi} = \frac{k_B T}{q} \ln\left(\frac{N_d N_a}{n_i^2}\right)$$

Where N_d and N_a are the donor and acceptor densities of n-type and p-type materials respectively, and N_i is the intrinsic carrier density of the material.

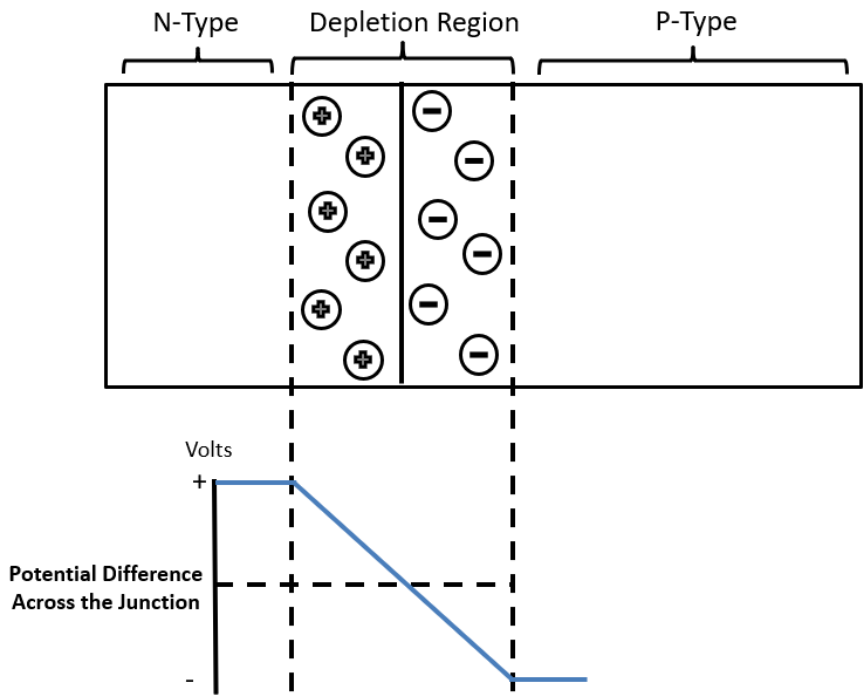

Fig. 1.5: Diagrammatic representation of a P-N junction and respective potential.

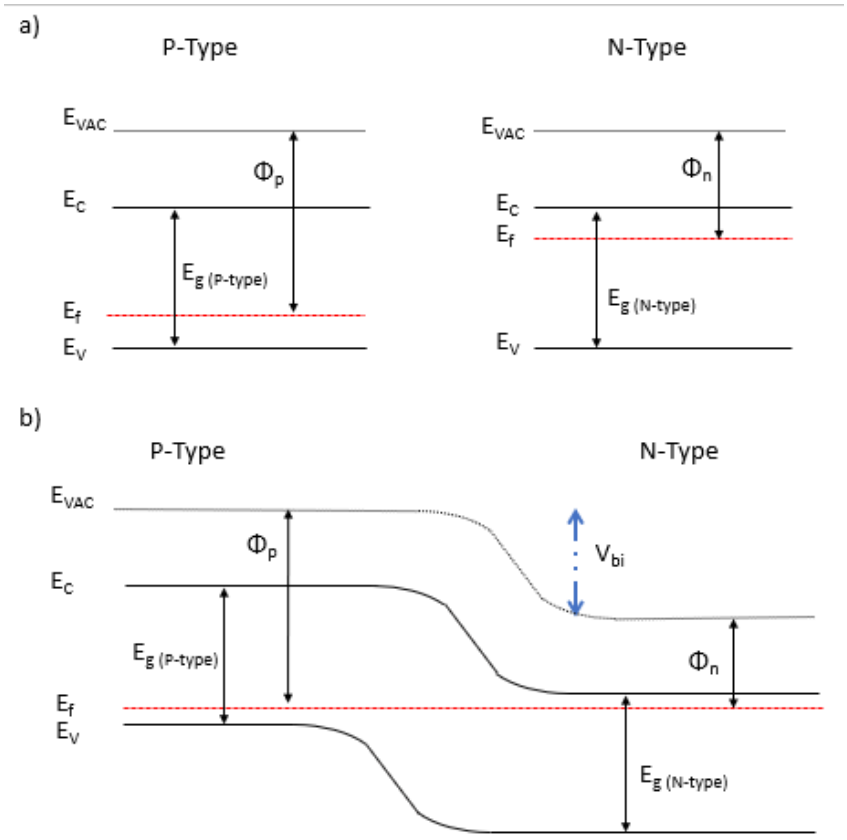

Fig. 1.6: a) Energy band diagrams of p-type and n-type c-Si semiconductors prior to contact and b) Energy band diagrams of p-type and n-type cSi semiconductors after contact

1.3.3 J-V Characteristic Curve

Fig. 1.7.a shows the equivalent circuit diagram, where an ideal cell is represented by a current source in parallel with a rectifying diode. The Shockley solar cell *eq. 1.2* describes the corresponding J-V curve of an ideal solar cell which is illustrated in *Fig. 1.7.b*. Here, the approximated total current density (J) is defined as the sum of the photocurrent (J_L) and the dark saturation Current (J_o).

(*eq. 1.2*)

$$J = J_L - J_o\left(e^{\frac{qV}{K_B T}} - 1\right)$$

Where J is the total current density in mA/cm^2, K_B is the Boltzmann constant, T is the temperature in Kelvin and V is the voltage at the terminals of the solar cell.

The power conversion efficiency (PCE) in a solar cell can be described by the equation below:

(*eq. 1.3*)

$$n = \frac{V_{OC}\, J_{SC}\, FF}{P_{in}}$$

Where V_{OC}, J_{SC}, FF, P_{in} are the open circuit voltage, short circuit current density, fill factor and the incident light power density respectively.

Fill factor describes the 'squareness' of the J-V curve and is defined as the ratio:

(*eq. 1.4*)

$$FF = \frac{J_m V_m}{J_{SC} V_{OC}}$$

Where J_m and V_m represent the maximum power, which is generated from a solar cell on a J-V curve.

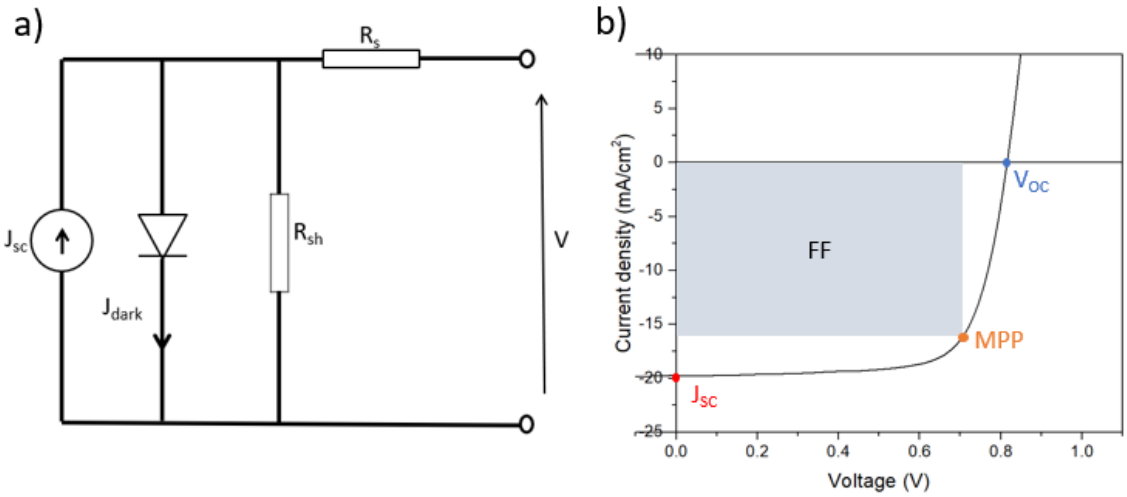

Fig. 1.7: a) The equivalent circuit diagram of a solar cell and b) J-V characteristic curve of an ideal solar cell.

1.4 Thin film technology

Crystalline silicon until now has dominated the PV market. In 2017 crystalline silicon-based photovoltaics (c-Si) accounted for 95% of global production [12]. However, in recent years, thin film photovoltaics have attracted the attention of the worldwide market. Technological advancements in thin film module efficiencies, combined with silicon ingots complex and large manufacturing processing energy requirement have led to thin film technologies becoming a viable alternative.

Because of their material properties such as direct bandgap, higher absorption coefficient and a wide range of deposition processes, thin films can potentially further reduce manufacturing costs. The main advantages of thin film technology are summarized below.

- High absorption coefficients (~ 10^5 cm^{-1}) → Close to 100% absorption possible with only 1-2 µm thickness.
- Hetero-junction structures → Possibility of junction partner choice and tunable junction properties can provide performance improvements through interface engineering.

- Lower temperature coefficients → Can provide higher suitability in adverse environments, diffuse light conditions and hot temperatures [13].

- Flexible substrates → Can be deposited on flexible substrates which unlocks new potential applications for the PV market.

- Simple volume production → Deposition of layers with simple methods and possibility of roll-to-roll manufacturing can further reduce manufacturing costs.

Thin film materials up to date used in PV, include cadmium telluride (CdTe), copper-indium-gallium-selenide (CIGS) and amorphous silicon (a-Si). At the moment, CdTe heterojunction thin film devices are one of the most encouraging commercially available thin film technologies that can potentially compete with crystalline silicon. CdTe based photovoltaics have secured approximately half of thin film market share [12], with First Solar Inc in 2018 reaching more than 20 GW worldwide [14].

1.5 Polycrystalline CdS/CdTe solar cells

1.5.1 Device structure

Currently the efficiency record for these devices is 22.1%, reported by First Solar in 2016 [15]. This only accounts for 70% of the theoretical maximum and makes CdTe a promising area of research in order to achieve higher efficiencies.

CdTe devices can be manufactured either in the substrate or superstrate configuration (*Fig. 1.8*) with the latter being established for commercial use. A CdTe solar cell consists of a glass substrate, a transparent conductive oxide (TCO) which acts as the front contact, an n-type buffer layer (typically CdS), the p-type CdTe absorber layer and a back contact comprising of a hole transport layer and a metal. In the superstrate configuration the incident photons first pass through the glass substrate, the TCO and the buffer layer and finally reach the CdTe absorber. Any photons with energy higher than 1.5 eV (bandgap of

CdTe) are absorbed and electrons from the valence band are excited to the conduction band, resulting in the generation of electron hole pairs. Generated electron-hole pairs are separated by the built-in electric field of the junction, ideally before recombination occurs. When charges are separated, electrons flow and collected by the front contact and holes by the back contact. An external load is then connected to the contacts to complete the circuit in order for useful work to be carried out.

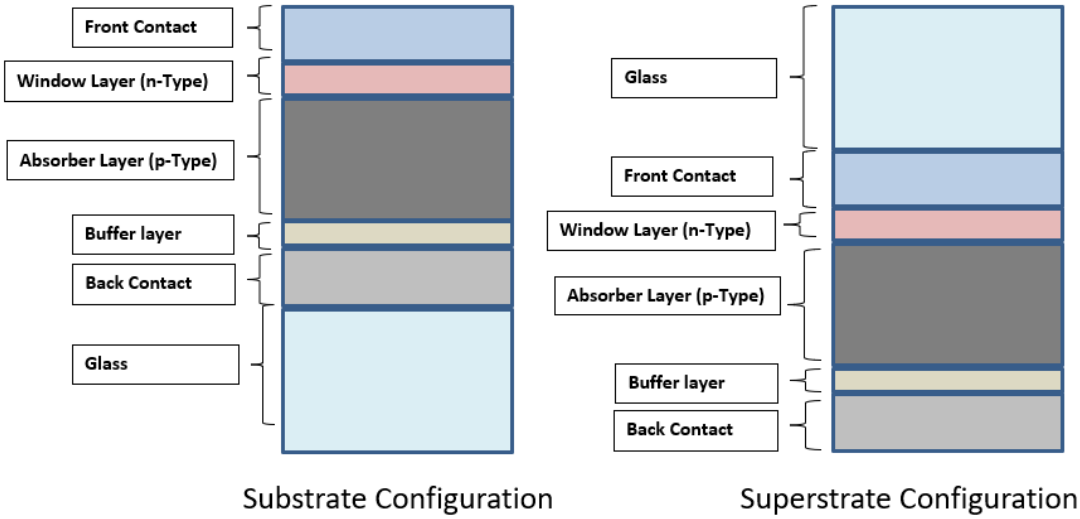

Fig. 1.8: A schematic diagram of substrate and superstrate configuration for CdS/CdTe heterojunction devices.

1.5.1.a Glass substrate

In the superstrate configuration, the glass substrate plays a vital role since the photons need to travel through the substrate to reach the absorber, and subsequent layers can be deposited at high temperatures. The substrate needs to provide high transmission and be able to withstand thermal cycling during device fabrication and operation. Most commonly, the glass substrate is made of soda-lime or borosilicate glass due to their resistance to high temperatures and their relatively low cost, however soda-lime glass can contribute to a current density loss of ~ 1 mA/cm^2 due to FeO_x if a low iron concentration is not specified [16]. An antireflective coating can be applied to the glass surface to minimise losses due to glass absorption which can lower the performance of the overall device.

For the substrate configuration, the substrate does not play as much of a significant role, however it still needs to be able to withstand thermal cycling and provide reasonable surface roughness to minimise adhesion problems [17].

1.5.1.b Front contact

Transparent conductive oxides (TCO's) are used as front contacts in thin film solar cell technology. A TCO is a highly doped large bandgap semiconductor (E_g > 3.0 eV) which needs to combine enough electrical conductivity for efficient charge transport and high transparency in the wavelength range of 300 to 850 nm. This is to allow incoming photons to reach the absorber layer for generation of electron-hole pairs [18]. TCO's must be able to withstand subsequent exposure to high temperatures and chemical processes without their opto-electrical properties being affected. TCO's can be deposited by various methods such as sputtering, spray deposition and chemical vapour deposition. Common options in the market include fluorine doped SnO_2 (FTO), aluminium doped ZnO (AZO) and tin doped indium oxide (ITO).

A subsequent deposition of a highly resistive and transparent layer (HRT) can be applied to permit the thickness of the CdS layer to be decreased for maximisation of the photocurrent in the device. This prevents absorption of photons by the CdS by enabling the reduction of the CdS thickness without affecting the voltage and the fill factor of the device due to formation of localised shunt paths.

1.5.1.c CdS buffer layer

The CdS layer is one of the most widely used materials as a buffer layer in thin film solar cells which acts as the n-type partner in a p-n heterojunction structure. CdS has been successfully incorporated into various PV thin film technologies such as CIGS, copper tin zinc sulphide (CZTS) and CdTe [19][20][21]. CdS can be deposited by various methods including sputtering, high vacuum evaporation (HVE) and chemical bath (CBD) with the later providing lowest optical absorption and good coverage properties on TCOs.

Depending on the deposition method, CdS exhibits a metastable zinc blende (cubic) with (002) preferred orientation or a stable Wurtzite (hexagonal) structure with orientation along (111). CdS is a II-IV group wide bandgap

semiconductor of 2.4 eV which absorbs light below a wavelength of 510 nm and allows large portions of the visible spectrum to be transmitted into the absorber [22].

1.5.1.d CdTe layer

CdTe is an II-IV group semiconductor with a direct optical bandgap of 1.5 eV, which is close to optimum for solar cells applications. Because of the nearly ideal bandgap and a high absorption coefficient (> 5x 10^4 cm^{-1}), CdTe can absorb > 99% of the available spectrum in about 2 µm [10].

As deposited CdTe crystallizes in the zinc blende (cubic) structure with a preferred orientation of (111) and is the only II-IV group semiconductor that can be easily doped n-type or p-type.

CdTe is the only possible compound in the Cd-Te system, since both Cd and Te exhibit much higher vapour pressures. This allows, polycrystalline CdTe stoichiometric growth at high deposition rates with several low-cost fabrication methods including RF sputtering, electrodeposition and close space sublimation (CSS), with the latter providing the state-of-the-art efficiencies. This is further discussed in *Chapter 2* (*2.1.4*).

Typical thicknesses of the CdTe layer is between 2 µm and 10 µm with grain size varying between 0.5 to 8 µm depending on the deposition technique. The polycrystalline nature of CdTe affects the device performance due to grain boundaries inclusion of trap states. To overcome this, CdTe needs to be appropriately passivated usually with a $CdCl_2$ annealing treatment [23].

1.5.1.e $CdCl_2$ treatment

As previously mentioned in section *1.5.1.d* it is important to passivate CdTe grain boundaries with a subsequent $CdCl_2$ treatment. $CdCl_2$ is usually deposited by vacuum evaporation or CBD in a saturated solution followed by annealing in an oxygen containing environment.

It is now widely accepted that a $CdCl_2$ treatment is necessary for high performing devices due to the structural and electrical beneficial impact on CdS/CdTe heterojunction devices.

In low temperature deposited CdTe (typically deposited using sputtering), the $CdCl_2$ treatment leads to recrystallization and grain growth, while it reduces stacking faults along the grain boundaries. Furthermore, the treatment leads to interdiffusion between CdS and CdTe, reducing the lattice mismatch [24][25].

In high temperature deposited CdTe devices (using methods such as CSS), no structural alterations are observed, but due to chlorine segregation along the grain boundaries, the minority carrier lifetime in CdTe and p-type conductivity are enhanced (by formation of chlorine acceptor centres). However aggressive $CdCl_2$ annealing treatment can cause migration of sulphur from CdS in the CdTe layer resulting in excessive consumption of the CdS layer. This can lead to a weaker diode limiting the built-in potential of the junction [26]. A more detailed discussion about the effects of $CdCl_2$ is included in section *1.6.2*.

1.5.1.f Back contact

The application of a back contact is the last element that completes a CdS/CdTe heterojunction device. Usually it is composed of a buffer layer to limit the back-contact barrier and a low resistive, high work function metal. The back contact can be deposited by various methods, such as sputtering, screen printing and high vacuum evaporation (HVE). Typical back contacts for CdTe solar cells include Cu/Au, HgTe:Cu/Ag and ZnTe:Cu/Ni. This is further analysed in section *1.6.4*.

1.6 CdTe device structure interfaces

As discussed earlier, CdTe heterojunction devices depend on different materials integrating with each other, each performing a specific role. In the simplest structure of these devices (front contact/buffer/absorber/back contact) which was outlined in the previous section, there are at least four different materials that interact with each other forming various interfaces. These, due to the different material structures and/or lattice constants can add considerable complexity during the device formation.

The combination of these dissimilar materials leads to the formation of high interface states (*Fig. 1.9)* and thus, increasing interface recombination between the two materials. This can be further promoted by poor band alignment between the energy levels (valence band and conduction band offsets) and can inhibit carrier transport between the different semiconductors leading to loss of either voltage or photocurrent [27].

In this section important aspects of interface engineering for CdTe are presented which can aid into the understanding of the complex nature of CdTe solar cells.

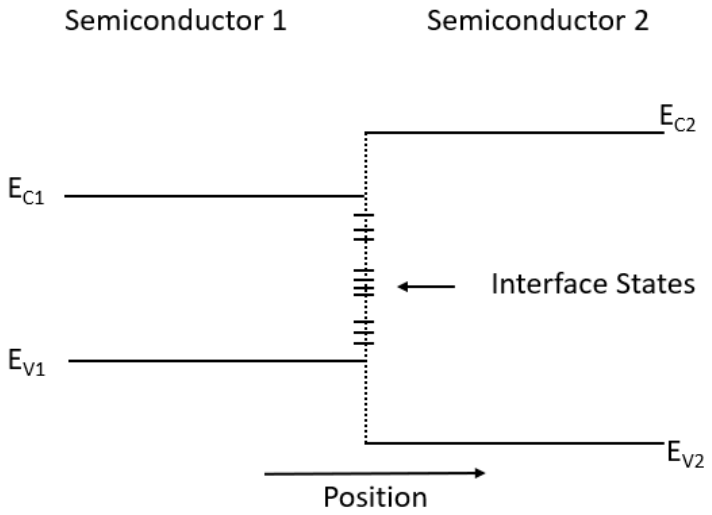

Fig. 1.9: Interface states diagram at a heterojunction interface.

1.6.1 CdTe device energy band diagram

Band diagrams can provide useful comprehension in a device structure since they can define the carrier transport, carrier recombination and the Fermi level position across a thin film heterojunction device.

Now let us consider the energy band diagram of a conventional CdS/CdTe heterojunction structure (*Fig. 1.10*). Here the back contact is not shown for simplicity. For details about the absorber/back contact interface refer to section *1.6.4*.

First note the CdTe/CdS (IF_1) interface. In this example there is a positive band offset for the conduction band (ΔE_C). This is referred to as a 'spike' where charge

carriers traveling from the CdTe (small gap) to the CdS (large gap) must spend kinetic energy in order to overcome this energy barrier.

Now note the CdS/TCO interface (IF_2), here there is a negative band offset, this is referred to as a 'cliff. In this case charge carriers gain kinetic energy traveling from the CdS (small gap) to the TCO (large gap) semiconductors.

The conduction and valence band offsets in a device are governed by the band gap, the doping density and the material used. As the E_F must be flat between contacted materials, the doping will determine the E_F position in each material and thus affecting the band bending when the materials are brought into intimate contact.

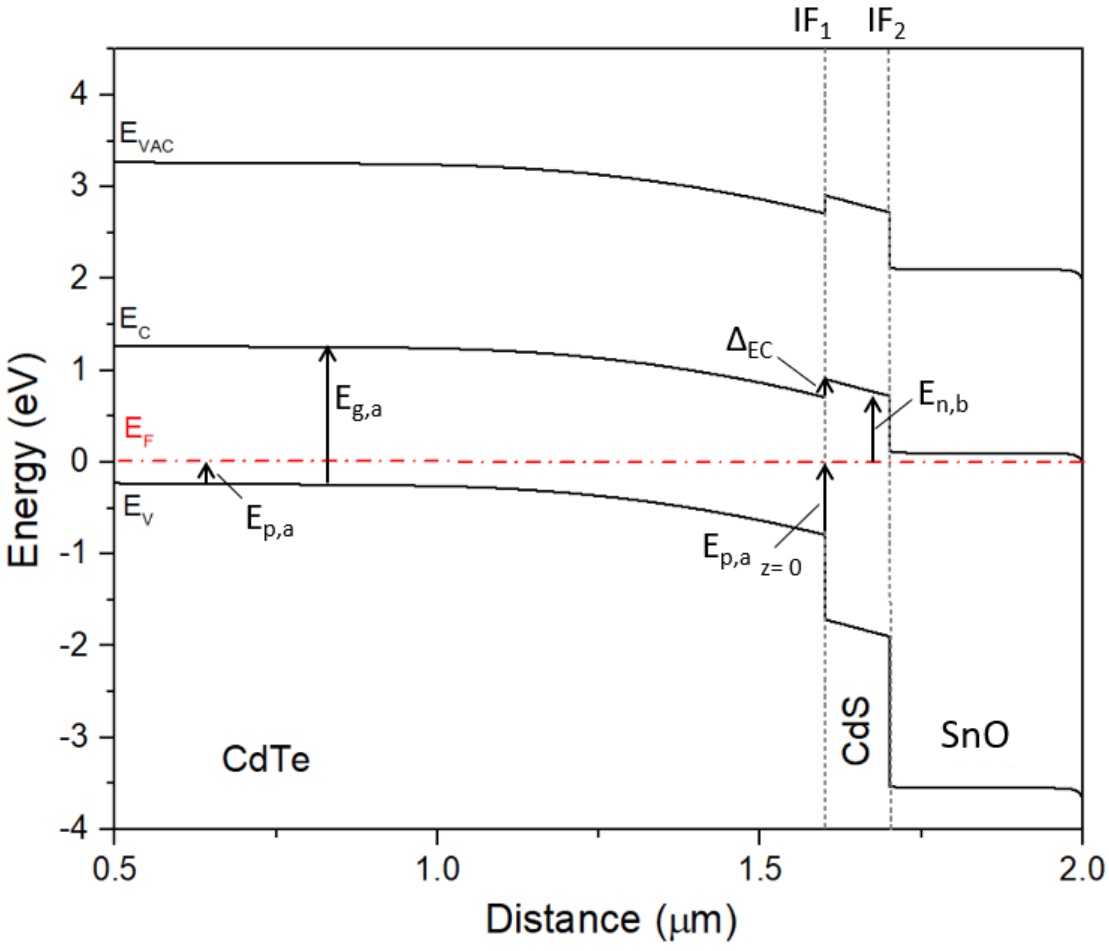

Fig. 1.10: Example of a CdS/CdTe device band diagram simulated by SCAPS. Here the back contact is omitted for simplicity.

To understand the effect of doping and the effect of the E_F position in a heterojunction interface, let us assume that a complete device is only composed from just the CdTe/CdS interface (IF_1) for simplicity.

The E_F position with respect to the band edge in an absorber (a) and in a buffer (b) can be defined as $E_{p,a}$ and $E_{n,b}$, where these values are taken in the bulk of the absorber and the buffer, away from the interface [28], in the region with zero band bending.

The built-in voltage, V_{bi} ,of the CdS/CdTe interface is given by

(*eq. 1.5*)

$$qV_{bi} = E_{g,a} - E_{p,a} - E_{n,b} + \Delta_{EC}$$

Where $E_{g,a}$ and Δ_{EC} are the absorber bandgap and absorber/buffer conduction band offset respectively.

The energy $E_{p,a_{Z=0}}$, where z=0 is the position at the interface, is defined as the amount of absorber inversion at the absorber/buffer interface. An absorber inversion occurs when the absorber majority carriers (holes) in the bulk become minority carriers at the interface. $E_{p,a_{Z=0}}$ is given by the equation:

(*eq. 1.6*)

$$E_{p,a_{Z=0}} = \frac{E_{p,a} + q(V_{bi} - V)\, N_{D,b}}{\varepsilon_a\, N_{A,a} + \varepsilon_b N_{D,b}}$$

Where ε_a and ε_b are the permittivity of the absorber and buffer layer, $N_{A,a}$ and $N_{D,b}$ are the acceptor and donor densities of the absorber and buffer respectively, and V_{bi} is the built-in potential of the junction.

From *eq. 1.6*, it is apparent that the degree of absorber inversion ($E_{p,a_{Z=0}}$) depends on the doping densities of semiconductors ($N_{A,a}$ and $N_{D,b}$) where $E_{p,a_{Z=0}}$ increases when $N_{D,b} > N_{A,a}$. Additionally, *eq. 1.5* also shows that a larger Δ_{EC} will also induce a greater absorber inversion ($E_{p,a_{Z=0}}$), by increasing V_{bi} [28].

1.6.2 Emitter/Absorber Interface

A key aspect of the emitter/absorber junction formation in heterojunction devices is to minimise interface recombination. In a traditional CdS/CdTe solar cell there is ~ 10.8% of a lattice mismatch between heterojunction partners [28]. This aspect combined with the impurities present during device fabrication are likely to form a large number of defect states at the interface. These can be electrically active and can act as recombination centers for electron-hole pairs [27]. Defect states present at the interface are easily accessible from either the emitter or the absorber. Consequently, the device can exhibit reduced photocurrent, and more importantly a significant reduction in open circuit voltage due to large diode saturation current.

Empirically, in CdS/CdTe devices the $CdCl_2$ treatment has been shown to be a crucial process for high performing devices. Some aspects of the $CdCl_2$ treatment have been already discussed. In summary the $CdCl_2$ treatment has been demonstrated to be responsible for grain boundary coalition, recrystallisation and grain reorientation. It has been also associated with increase in p-type conductivity and passivation of bulk interface states increasing minority carrier lifetime and enhance the charge separation, increasing hole depletion near the grain boundaries and improve carrier collection [29][30].

For interface recombination, the most important characteristic of the $CdCl_2$ treatment is the reduction of the lattice mismatch between CdS and CdTe. During this crucial annealing step, sulphur from CdS diffuses into the CdTe, forming $CdTe_{1-x}S_x$; while Te diffuses in CdS as $CdS_{1-y}Te_y$. This interdiffusion process and the formation of these ternary compounds, can increase the V_{OC} through reduction of active recombination centers at the interface and increase the current density of the device due to consumption of CdS [16][31].

However, CdTe has only reached ~ 70% of its V_{OC} potential, and minimising emitter/absorber interface recombination can provide future performance improvements.

At the interface, the charge balance between emitter/absorber can affect the absorber inversion due to the presence of charged interface states. However, a

negative charge (acceptor states) can decrease the inversion. As demonstrated from *eq. 1.6* this depends on the window doping.

A high emitter doping $N_{D,b} \gg N_{A,a}$ translates to a high buffer positive charge. A highly doped buffer can screen more negative charged defects and at the same time balance the absorbers negative charge. This makes the heterojunction less sensitive to interface states.

Fig. 1.11.a shows the effect of emitter doping on the band alignment and carrier distribution across a CdS/CdTe solar cell. In this example, the first emitter is lightly doped ($N_{D,b} = 10^{15}$ cm^{-3}), while the second emitter is moderately doped ($N_{D,b} = 10^{17}$ cm^{-3}). The negative conduction band offset (cliff) between absorber and emitter remains the same at ΔE_C = - 0.1 eV. Here, the value of $E_{p,a_{Z=0}}$ increases from 0.9 to 1.3 eV when the emitter doping increases.

Similarly, *Fig. 1.11.b* shows the difference between a negative and a positive conduction band offset at the emitter/absorber interface while the emitter doping remains the same at $N_{D,b} = 10^{17}$cm^{-3}. The value of $E_{p,a_{Z=0}}$ increases from 1.3 eV to 1.4 eV, in accordance with eq. 1.5.

In both examples, the carrier distribution at the interface changes. The absorber depth where the charge equalises (*Fig. 1.11*) bottom graphs) shifts further away from the interface when the absorber inversion increases ($E_{p,a_{Z=0}}$) and as a consequence the interface recombination is reduced because of the limited availability of holes at the interface, for electrons to recombine with [32]. This reduces the diode current and the V_{OC} is improved.

A positive ΔE_C (spike) must be limited to ΔE_C = + 0.4 eV [28]. If the barrier is too large, it will impede electron flow from the absorber to the emitter and lead to a J_{SC} reduction [32].

The concepts discussed here are not specifically related to CdS/CdTe devices and reside in all heterojunction devices. Interface recombination strongly depends on the carrier concentration of each layer and the band alignment between heterojunction partners. Through appropriate management, interface recombination can be minimised, enhancing the performance of thin film solar cells. This will be discussed in *Chapter 4*.

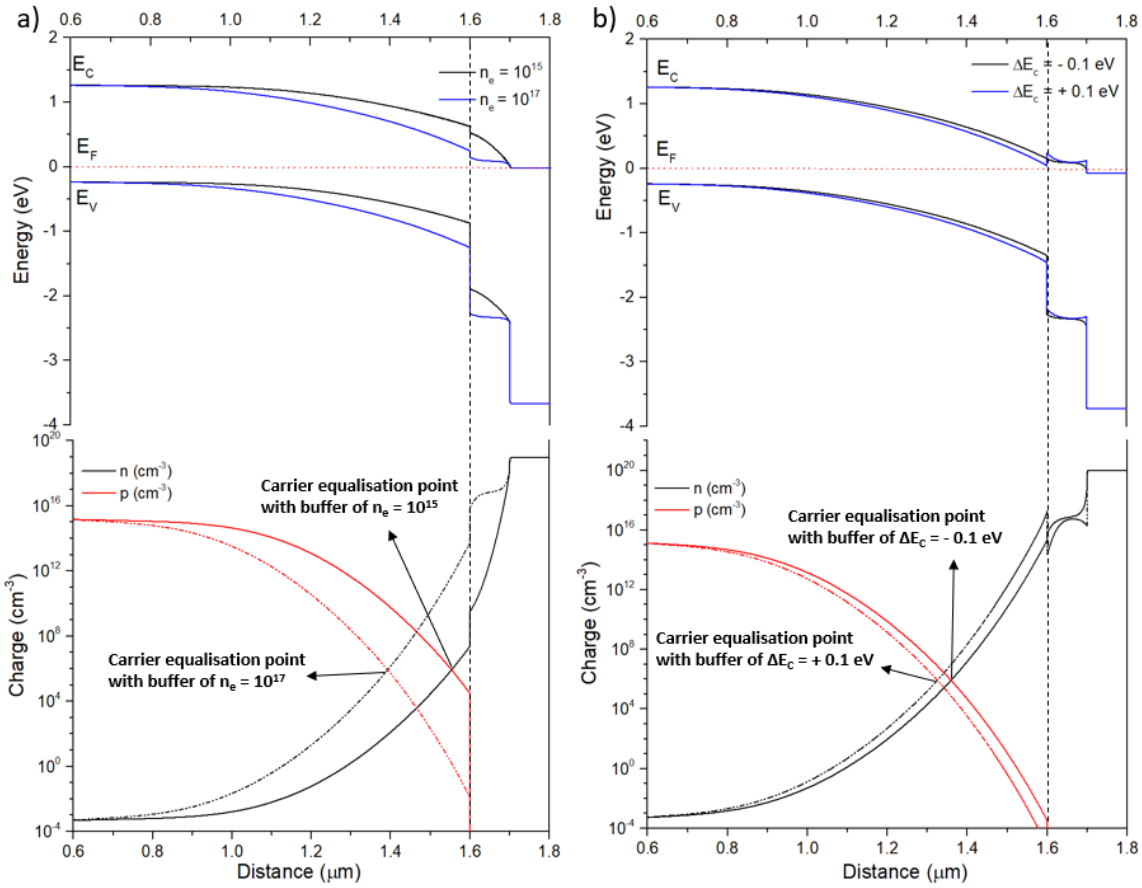

Fig. 1.11: Simulations with SCAPS 1D of band diagrams (top) and carrier distributions (bottom) of a) Comparison of differently doped emitters with a negative conduction band offset of ΔE_C = - 0.1 eV and b) Comparison equally doped emitters with positive and negative conduction band offsets of ΔE_C = - 0.1 and ΔE_C = +0.1 respectively.

1.6.3 Window/Emitter Interface

As already shown, traditionally CdTe devices employ CdS as their heterojunction partner to form a p-n junction, and through this device structure, efficiencies of > 16 % have been achieved [16][33][34]. However, CdS buffer can contribute to current loss at wavelengths below ~ 510 nm due to absorption of photogenerated carriers inside the buffer layer [10][35]. Carriers generated inside the CdS cannot be collected due to small lifetimes and strong interface recombination that arise from the lattice mismatch between CdS and CdTe [28].

One way to mitigate this effect is to apply a reduction of the CdS thickness in the solar cell structure to allow a larger fraction of light to reach the absorber. This however, has a deleterious effect on the V_{OC} and FF for CdS thickness below ~ 100 nm [36][37]. Reduction of CdS can lead to incomplete coverage of the TCO

and increased pinhole density. This can lead to a local shunt path for the current to be formed between the absorber and the TCO.

This effect can also be considered a high recombination site if we take into account a localised unfavourable band structure between the absorber/TCO interface. At this point the size of $E_{p,a_{Z=0}}$ will be very small (as seen in section 1.6.2). To mitigate this effect usually an HRT layer is deposited on top of the TCO to allow the thickness of the CdS to be reduced. This layer acts as a localised barrier between TCO and absorber. However, it has been argued by Kephart et al [38] that this mechanism alone cannot explain the role of an HRT. It was demonstrated that even with a homogeneous coverage of the TCO by a thin CdS, voltage and fill factor still showed considerable degradation. In that report, the effects of interdiffusion between CdS and CdTe were not investigated. During the $CdCl_2$ annealing localised total consumption of CdS from CdTe could lead to the formation of localised shunt paths which could support the initial theory. In the same report (Kephart et al [38]) it was also demonstrated that the HRT's has a positive effect on the window/emitter band alignment and thus minimising interface recombination at the window/emitter interface.

Additionally, wider bandgap materials such as MgZnO have recently been proven to be effective as buffer layers for CdTe devices and prominent candidates for replacing CdS. These materials allow a larger fraction of the solar spectrum to reach the CdTe absorber, and thus increases the photocurrent of CdTe devices [32][38][39].

The role of thinning down the CdS layer and the introduction of HRT's and their implications on the window/emitter interface have not been fully understood and more research needs to be undertaken in this subject. This is explored in *Chapter 5* of this thesis.

1.6.4 Absorber/Back Contact Interface

According to the classical Anderson model [40] when two semiconducting materials are brought into intimate contact the vacuum levels of the two semiconductors on either side of the heterojunction should be aligned at the same energy. Similarly, when a metal and a semiconductor are brought together their respective fermi levels line up, causing a band bending equal to the difference of the metal-semiconductor work functions. Depending on the semiconductor-metal work function relationship either a rectifying or a non-rectifying behaviour at the semiconductor-metal junction can be formed. A non-rectifying behaviour is called an ohmic contact while a rectifying behaviour is called a schottky diode.

In a p-type semiconductor the formation of an ohmic contact (*Fig. 1.12.a*) is developed by the use of a metal which has a higher work function than the semiconductor (in this case p -type CdTe) [22]. This prevents the formation of a Schottky barrier (*Fig. 1.12.b*), which acts as a reversed biased diode to the CdS/CdTe junction, increasing the back-contact resistance. This hole transport barrier when formed at the CdTe/metal interface reduces the carrier collection at the back contact and naturally limits the device performance [41][42].

The work function (Φ) is defined as the minimum energy needed to remove an electron from the Fermi level in a solid to the nearest vacuum level. It is denoted as $\Phi = E_{VAC} - E_F$.

Since the fermi level position inside a p-type semiconductor resides close to the valence band, an approximation for the quantity of Φ can be often referred as $\Phi = E_g + x$, where E_g and χ are the semiconductor's bandgap and electron affinity respectively.

The summation of CdTe bandgap and electron affinity yields a work function of ~ 5.7-5.9 eV and since there are no metals with higher work function, the formation of a Schottky barrier is inevitable (*Fig. 1.12.b*) [41].

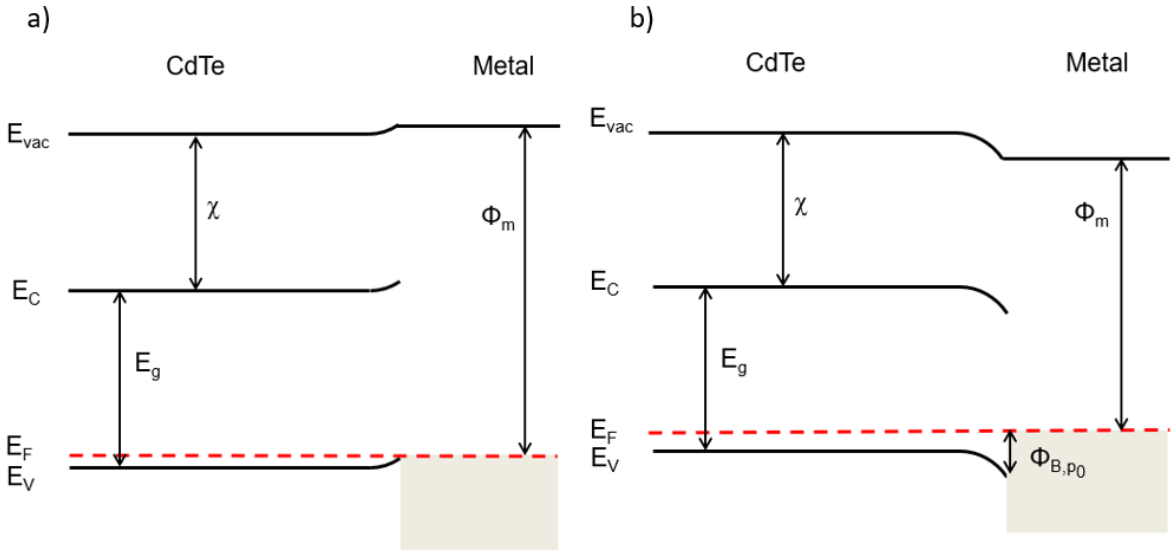

Fig. 1.12: a) Band diagram of an ohmic contact formation and b) Schottky barrier formation at the semiconductor/metal interface

Now let us consider a semiconductor/metal junction without surface states. The schottky barrier height in an ideal a p-type semiconductor/metal interface Φ_{B,p_0} is given as:

(*eq. 1.7*)

$$q\Phi_{B,p_0} = E_g - (q\Phi_m - qx)$$

where, E_g and x are the semiconductor's bandgap and electron affinity respectively and Φ_m is the work function of the metal.

Upon contact between semiconductor and metal, a depletion region is formed similar to a one-sided abrupt junction. This is essentially a second diode opposite the main diode of the solar cell.

Under forward bias the voltage in the device will be distributed across the main and back contact junction as $V = V_m + V_b$ where V_m and V_b are the main junction and back contact field voltages.

Equating the current density flow between the two junctions gives:

(*eq. 1.8)*

$$J = J_{m0}\left(e^{\frac{qV_m}{AkT}} - 1\right) = J_{b0}\left(1 - e^{\frac{qV_b}{kT}}\right)$$

where, A is the effective Richardson constant and J_{m0} and J_{b0} are the main and back contact junction reverse saturation currents respectively.

When $J_{m0}\left(e^{\frac{qV_m}{AkT}}\right) - 1 \ll J_{b0}$ the main voltage drop occurs at the main junction, and the diode current is not blocked by the back-contact barrier. However, the moment the diode current approaches J_{b0} the applied voltage drops at the back-contact barrier, saturating current. This appears as a distortion in the forward bias of device's J-V curve as a 'roll-over' (*Fig. 1.13*)

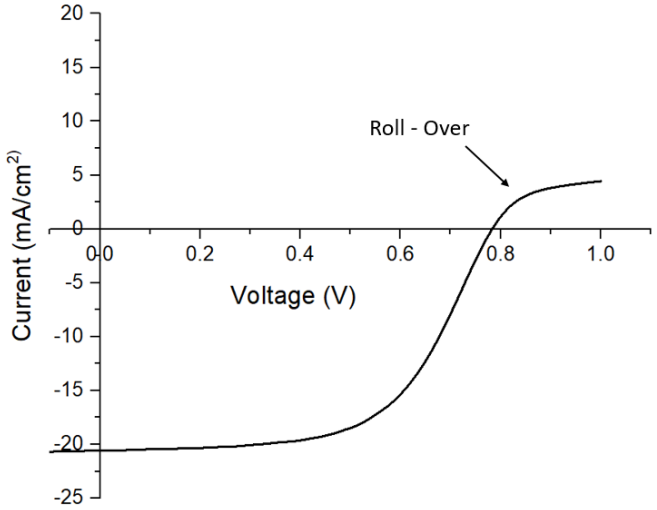

Fig. 1.13: Example of 'Roll-over' distortion a J-V characteristics curve.

The back-contact opposing diode does not only depend on the semiconductor/metal barrier height but also by the depletion width of the back-contact junction (*Fig. 1.14*). The width of the depletion region can be defined as (*eq. 1.9*)

$$W_a = \sqrt{\frac{2\varepsilon_a}{N_A}(V_b - V - \frac{kT}{q})}$$

where, ε_a is the dielectric permittivity of the semiconductor, N_A is the semiconductor acceptor doping density near the surface, V_b is the built-in potential of the back-contact field and V is the external applied voltage on the solar cell.

Note that the depletion width strongly depends on the absorber's doping density. A highly p-type doped semiconductor will yield a narrow depletion width (W_a) allowing tunnelling of carriers through the back-contact barrier.

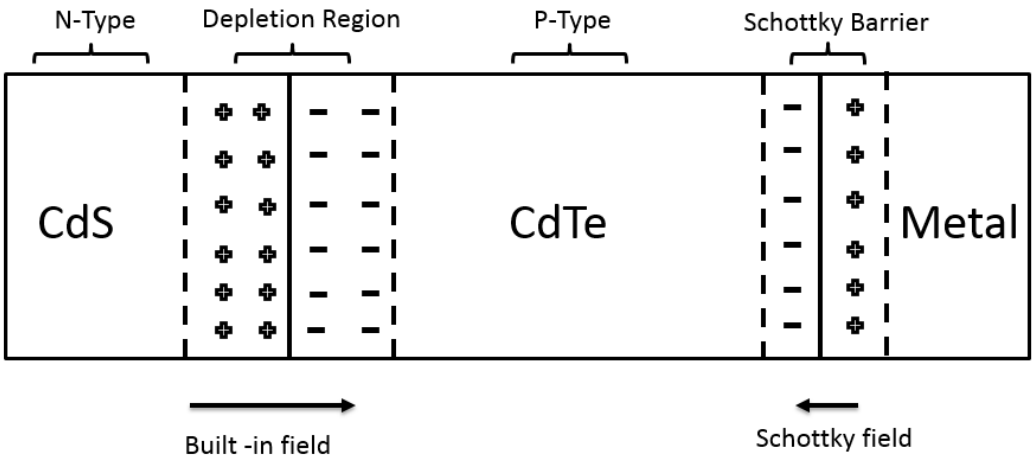

Fig. 1.14: Diagrammatic representation of the opposing P-N and Schottky junctions.

Traditionally, in CdTe devices the approach employed to create a low resistance contact is narrowing the depletion width of the back-contact barrier with the utilisation of Cu.

First, to avoid fermi level pining a selective surface modification step is performed. A common method is based on making a Te-rich layer on the surface of the CdTe. Te is a p-type semiconductor with a bandgap of E_g =0.33 eV. In order to create a Te rich layer, CdTe is submerged either in Br-methanol or HNO_3-H_3PO_4 (NP) acid solutions which removes Cd, before the application of the back electrode [43].

Solution based etching has proved to have various disadvantages including non-compatibility with vacuum processing which increases the cost of production, controlling the etching process is very difficult and can result in

over-etched films where shunt resistance decreases dramatically causing shunt paths degrading device performance [43][44].

Cu is alloyed which bonds with tellurium and forms Cu_2Te, a highly p-type material with a bandgap of 1.04 eV [45]. This increase in p-type conductivity and the fact that Cu forms a shallow acceptor in CdTe, forces a narrowing of the back-contact's junction depletion width and creates a quasi-ohmic contact and eliminates the 'roll-over' from the J-V curve [46].

However, weak Cu-Te bonds and the high bulk diffusion coefficient of Cu in CdTe (3×10^{12} cm ^{2}/s), result in migration of Cu away from the back contact when CdTe devices are subjected in thermal and electrical stresses [10].

Cu migration is aided by the $CdCl_2$ treatment, as Cu_{Cd} can complex with Cl_S in CdS and increase the solubility of Cu and Cl. Accumulation of Cu together with significant amounts of Cl can increase photoconductivity in CdS [47]. Excess Cu accumulation in CdS can create deep acceptor states and thus act as recombination centres decreasing the effective donor concentration [48].

To address the stability issues arising from Cu inclusion in CdTe devices, intermediate semiconducting materials without Cu have been recently explored as back contact buffer layers. These include Sb_2Te [49], ZnTe [50] and various transitional metal oxides such as MoOx [51]. Up to date however, Cu-free back contacts have not managed to compete with Cu back contact structures.

Back contacting CdTe devices yields a difficult and complex interface optimisation problem that significantly affects the performance and stability of CdTe devices. This will be explored in *Chapter 6*.

1.7 Scope of the Thesis

At the moment, CdTe thin film PV is one of the most promising commercially available thin film technologies which can potentially compete with crystalline silicon. To achieve this there are significant performance and stability issues that need to be addressed to further improve the viability of this technology. In heterojunction devices interfaces present a complex and difficult problem, and the physical mechanisms associated with each interface are not entirely understood. The research presented in this thesis focuses on the interface optimisation at each layer of thin film CdTe solar cells through comparative studies.

Chapter 2 describes the design and implementation of a bespoke close-space sublimation system that is necessary for the fabrication high efficiency CdTe solar cells.

Chapter 3 focuses on the development of a repeatable baseline process based on a simple superstrate cell configuration and identifies important process sensitivities for CdTe solar cells.

Chapter 4 is divided in two parts. The first part concentrates on improving the emitter/absorber interface focusing on the emitter doping with chlorine compounds such as $CdCl_2$ and highlighting the importance of emitter doping on device performance. In the second part of this chapter a crucial aspect of the annealing $CdCl_2$ passivation process is identified. Results highlight the effect on the performance of air activated CdS/CdTe solar cells during the $CdCl_2$ passivation cooling cycle which has not been discussed in literature.

Chapter 5 concentrates on the window/emitter interface optimisation and photocurrent losses arising from the utilisation of the CdS buffer. This chapter is divided in three parts. The first part investigates the effect of thinning down the CdS buffer layer and the role of CdS thickness on CdS/CdTe interdiffusion process. In the second part of this chapter the role of HRT is explored in respect with device performance. The last part of this chapter identifies the importance of HRT's on interface band alignment, device performance and investigates the complete elimination of the CdS buffer to enhance the photocurrent of CdTe devices.

Finally, Chapter 6 concentrates on the absorber/back contact interface and is divided in two parts. The first part investigates the role of Cu in absorber/back contact interface of non-etched CdS/CdTe devices and focuses on the performance, controllability and the stability of the process. The second part of this chapter describes the implementation of a new baseline process based on substrate configuration CdS/CdTe devices and focuses on the development of a Cu-free back contact based on TMO's and specifically MoO_x.

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Chapter 2. Fabrication and characterisation procedures of CdS/CdTe solar cells

2.1 Thin film and device fabrication

Fabrication of CdTe solar cells involves the deposition and characterisation of multiple thin films, often with different procedures for each layer. The first part of this chapter outlines the fabrication methods and equipment used for each layer, necessary to achieve a complete device. This work is dedicated to interface optimisation of CdTe devices which involves the combination of optical, structural and electrical measurements of individual thin films and complete devices. The characterisation techniques used in this work are presented in the second part of this chapter.

2.1.1 CdS deposition

CdS/CdTe heterojunction device performance is greatly affected by the microstructural and electrical properties of each layer. In a given superstrate structure, the TCO/CdS interface is the first interface to be formed in a typical cell design.

CdS can be deposited by various deposition techniques such as: sputtering [1], chemical bath deposition [2], close space sublimation [3], electrodeposition [4] and chemical vapour transport deposition [5]. Depending on the deposition technique used, CdS will attain different structural properties such as grain size and grain orientation, which will strongly affect the morphology of the subsequent CdTe deposition [6]. However, the choice of the deposition method used in each research lab/group often depends on the availability and compatibility of resources available.

There is an agreement in literature that generally, carriers generated inside the CdS buffer layer do not contribute to a photocurrent due to recombination [7][8][9]. Therefore, it is highly desirable for the buffer to be as thin as possible in the multi-stuck structure [7]. However, a non-uniform coverage of the TCO

by the CdS can result in the formation of localised shunt paths and weak diodes limiting the performance of the device dramatically [10].

2.1.2 CdS by chemical bath deposition (CBD)

Chemical bath deposition is a low cost, non–vacuum deposition method which has, to date provided (alongside with CVD [11]), the highest efficiencies for CdTe solar cells [12][13]. Its simplicity, repeatability and scalability make CBD a commercially viable solution for buffer layer deposition [14], as well a convenient method for thin film deposition within a research lab.

CBD involves a controlled chemical reaction in an aqueous solution containing various precursors, at a low film growth rate. Since the reaction takes place at a low temperature (< 90°C) it is compatible with a wide range of substrates without the risk of oxidation or decomposition [15].

CdS thin film fabrication usually takes place in an alkaline solution (basic ammonium) containing a Cd salt and thiourea [14]. The process can be described through ion by ion condensation, where Cd^{2+} and S^{2-} exist over the solubility limit [16].

Choi et al. [17] described the process involving cadmium acetate as:

$$(NH_2)_2CS + 2OH^- \rightarrow S^{2-} + CN_2H_2 + 2H_2O \quad (2.1)$$

$$Cd(NH_3)_4{}^{2+} \rightarrow Cd^{2+} + 4NH_3 \quad (2.2)$$

$$Cd^{2+} + S^{2-} \rightarrow CdS \quad (2.3)$$

During this process, Cd^{2+} ions combine with ammonia forming $Cd(NH_3)_4{}^{2+}$complexes which adhere to the surface of the substrate. Hydrolysis of thiourea releases S^{2-} ions which are attracted onto the substrate, and through ion by ion exchange between $Cd(NH_3)_4{}^{2+}$and S^{2-} a uniform CdS thin film is deposited [16][17].

However, as the reaction progresses, colloidal CdS particle adsorption results in thick powdery films affecting the uniformity and quality of the resulting CdS,

particularly their optical properties, due to an increase in opacity. This latter step is called 'colloid by colloid' and has been described by Kaur et al [15]. Therefore, for uniform high quality CdS films, the reaction must be interrupted before it progresses to 'colloid by colloid'.

The CdS CBD can take place using simple equipment consisting of a hotplate, a beaker and a magnetic stirrer, but precise control of the process conditions such as reaction temperature, precursor concentration and maintaining a constant pH are required. However, Ortega- Borges and Lincot [16], suggested that precise control of the process can be very difficult due to ionic exchange and colloid by colloid reactions happening at the same time. In contrast, Choi et al. [17] has argued that the utilisation of an ultrasonic probe can provide uniform films supressing the formation of bad quality film due to colloidal reactions, and thus forming compact and transparent CdS thin films in shorter time and at lower reaction temperatures.

Fig. 2.1 shows the CdS deposition set up used in this thesis. The beaker is placed in a water jacket to ensure constant reaction temperature. The bath is agitated using an ultrasonic probe (Microson XL 2000 Ultrasonic liquid processor) at an output power of 4 W (RMS) [18]. More details about the CdS deposition process and CBD precursors can be found in *Chapter 3* section 3.2.3.a.

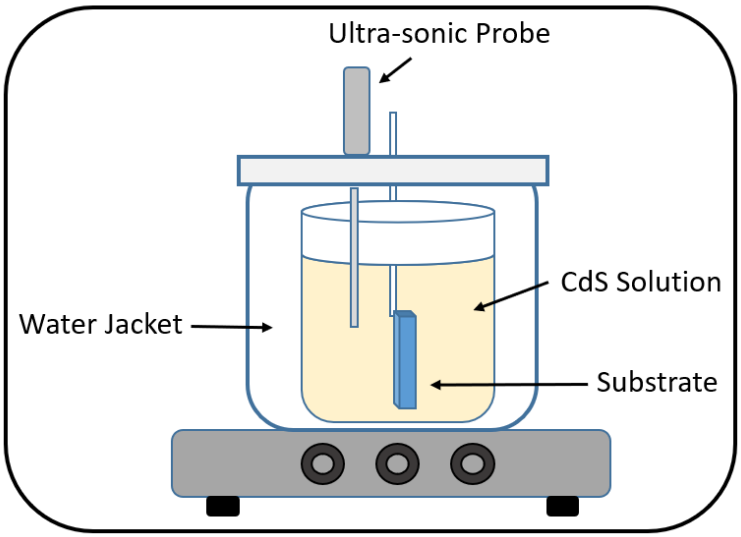

Fig. 2.1: CdS chemical bath deposition (CBD) diagram.

2.1.3 CdTe deposition

CdTe thin films can be deposited by numerous methods which grow robust and reproducible CdTe thin films. Some of the deposition methods available for CdTe are outlined in *Fig.2.2*. CdTe deposition methods can be divided into three main categories:

a) Condensation/reaction of vapours which include: sputtering [19], vapour transport deposition (VTD) [20] and close space sublimation (CSS) [9].

b) Reaction of precursors which include: metal-organic chemical vapour deposition (MOCVD) [21], screen –print deposition and spray deposition [22].

c) Electrodeposition [23].

However, out of all the available deposition techniques, only a handful to date have provided commercially viable devices with the main two being CSS and VTD [24][22]. In this thesis, CdTe deposition was carried out with CSS where a bespoke system has been designed and built for the purpose of this research. More details about the system can be found in *section 2.1.4.a*.

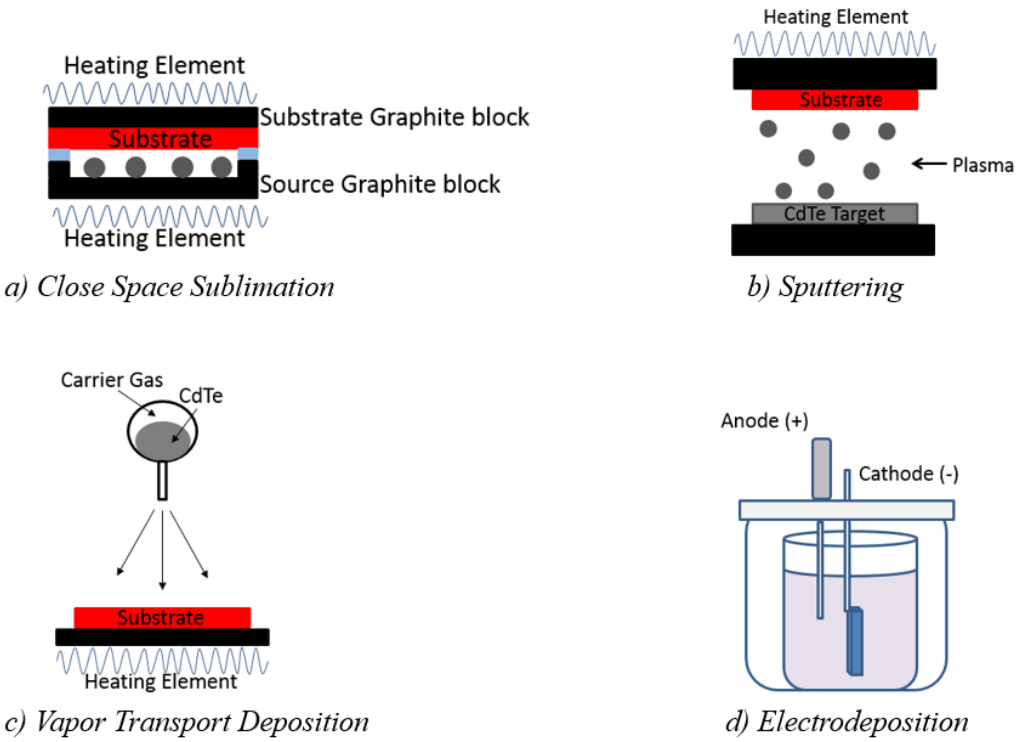

Fig. 2.2: Examples of methods used for depositing CdTe thin films.

2.1.4 Close space sublimation (CSS)

CSS is one of the techniques that to date has provided the highest laboratory efficiencies of CdS/CdTe devices. Sublimation refers to the direct transition of chemical compounds from the solid phase to gas without passing through the liquid phase. CdTe is an ideal compound to be sublimated due to its physical properties. CdTe is the only compound possible in the Cd –Te phase diagram (*Fig. 2.3*) and the vapour pressures of Cd and Te_2 are substantially higher than CdTe [7]. This results in single phase solid films possible over a large range of substrate temperatures [22]. CdTe dissociates, liberating equal amounts of Cd and Te and condenses stoichiometrically at a temperature of around 400° C [25]. B. Langry et al. [26] described this reversible reaction process as:

$$CdTe(s) \rightleftarrows Cd(g) + 0.5Te_2(g) \quad (4)$$

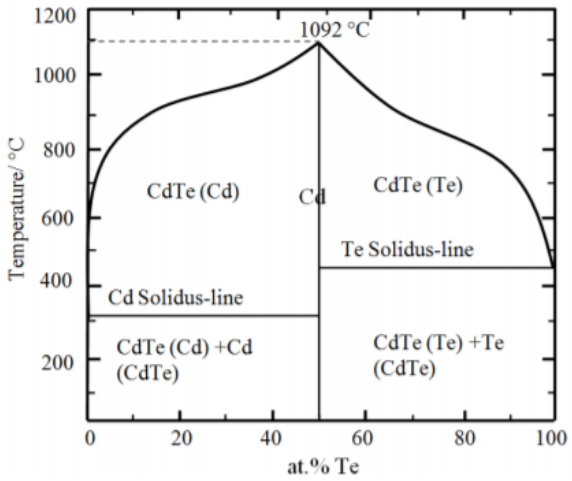

Fig. 2.3: CdTe phase diagram [27].

There are two growth mechanisms that can describe CdTe sublimation process depending on the deposition process and parameters utilised; diffusion limited transport and free sublimation [28]. Per the diffusion limited transport model, Cd and Te_2 atoms collide with inert gas atoms present in the chamber during migration to the substrate before condensing. In this case, the growth rate is assumed to be inversely proportional to the gas pressure and proportional to $e^{-E_a/kT_{so}}$ where E_a, k and T_{so} are activation energy, Boltzman's constant and source temperature respectively. In the free sublimation scenario, the deposition rate is independent from gas pressure since Cd and Te_2 atoms diffuse directly to the substrate without any interaction with the chamber gases, but still proportional to $e^{-E_a/kT_{so}}$[29]. Due to re-sublimation of Cd and Te_2 species from the substrate at temperatures above 400°C, in CSS the pressure is limited to ≥ 1 Torr. Consequently, the sublimation procedure becomes diffusion limited and the substrate and source need to be to in close proximity in order to maximise deposition rates.

In practice, solid CdTe (powder, granulate or film [3][1][30]) is placed in a graphite crucible (source) at a distance of around 2 to 20 mm below a substrate holder in an evacuated chamber. The source and substrate are heated at temperatures of 600° to 700°C and 400° to 600°C respectively in the presence of an inert gas (Ar, N_2 or He [25]). Due to the substrate being held above the source in the CSS system, the maximum substrate temperature is limited by the softening point of the glass used as substrate. The deposition rate strongly

depends on: temperature of the source (T_{so}) and substrate (T_{sub}), separation between source and substrate (usually provided by thermally insulating spacers), pressure during the deposition process and presence of any other gasses (usually oxygen) [31]. Deposition rates in CSS are typically in the range of µm/min and the minimum film thickness required to give a void free film has been found in literature to be ~ 2 - 4 µm, due to the large CdTe grain size [7]. With CSS it is possible to vary grain orientation, grain size and film uniformity through optimisation of T_{sub}, deposition pressure and gas mixture during the sublimation process [22][3].

2.1.5 CSS system design and implementation

Deposition of CdTe thin films was carried out in a bespoke built CSS system, illustrated in *Fig. 2.4. a*. The system consists of a horizontal quartz tube supported by a stainless-steel reactor. Source material (CdTe powder 99.999 % Alfa Aesar) was placed on a Corning Eagle XG glass support or into a 40 x 40 mm graphite boat for sublimation onto a substrate. A silicon carbide (SiC) coated graphite block was used as a heat susceptor to heat up the source. SiC was selected to prevent conversion of oxygen into CO and CO_2 during the CdTe sublimation process [30]. The substrate was placed on a second SiC coated graphite block and kept in close proximity to the source material. Both susceptors are supported by a quartz holder (*Fig. 2.4.b*) and quartz spacers were used to provide thermal separation between the source and substrate. Thermocouples were inserted inside the graphite blocks to control the temperature. Heating of the susceptors was provided by seven 1-kW IR lamps (USHIO) in a two-set configuration in an enclosed heating zone. Three lamps were used for heating the substrate graphite block and four lamps provided the heating for the source graphite block. All lamps are placed in reflectors to concentrate the light on to the susceptors. Independent temperature control for the two-set configuration was provided by two PID controllers (Eurotherm 2416), each communicating with a power controller (OMEGA SCR 19P-24-80-S9). The designed encapsulated heating zone was placed on a rail where it can be pushed away from the reactor. This provides faster cooling cycles, reducing

the overall time for each deposition. The system was fitted with three gas inlets (Ar, N_2 and O_2) through mass flow controllers for each gas. Evacuation of the deposition chamber is achieved through an Edwards RV8 mechanical pump. Pressure was manually adjusted with the use of a butterfly valve, and through the mass flow controller of the injected gas. A quartz insert is positioned immediately inside the horizontal quartz tube to protect it from material condensation. Using this configuration, the system can be easily cleaned from excess material condensing on the walls of the system without the need of dismantling the main reactor.

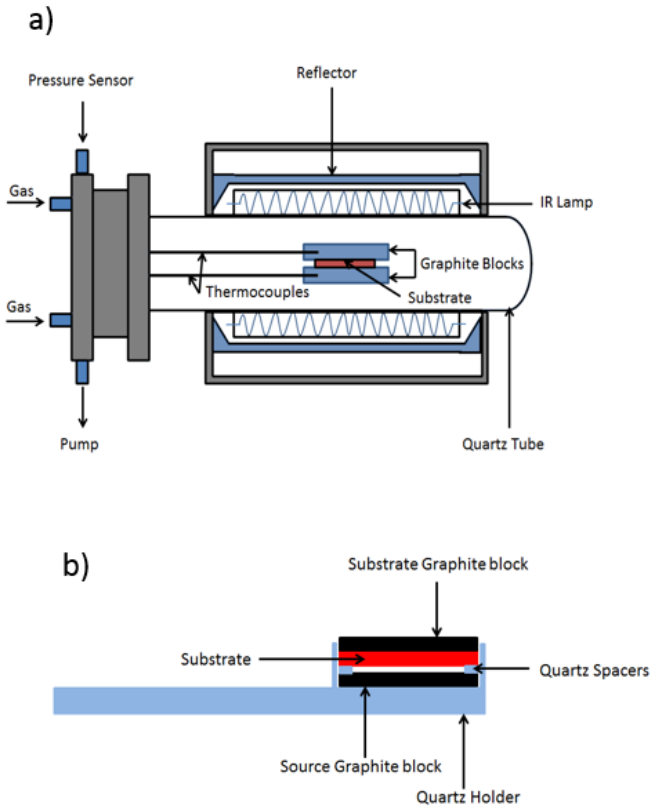

Fig. 2.4: a) Schematic diagram of bespoke CSS system designed and implemented for the purpose of this research. b) Substrate configuration diagram.

In *Fig. 2.5* the temperature profile of the home-made system is shown, where the substrate and source were heated up to 600° C and 700° C respectively. This procedure was necessary to identify the power distribution difference inside the heating element. The results obtained here were used to establish a clear reference procedure for subsequent depositions (*see section 2.1.4.b*). Initially,

both substrate and source were heated to 600° C to measure the time it takes for the system to reach the intended temperature (400 s). Then the source was heated to 700° C to measure the time delay for the source to reach its final temperature (100 s).

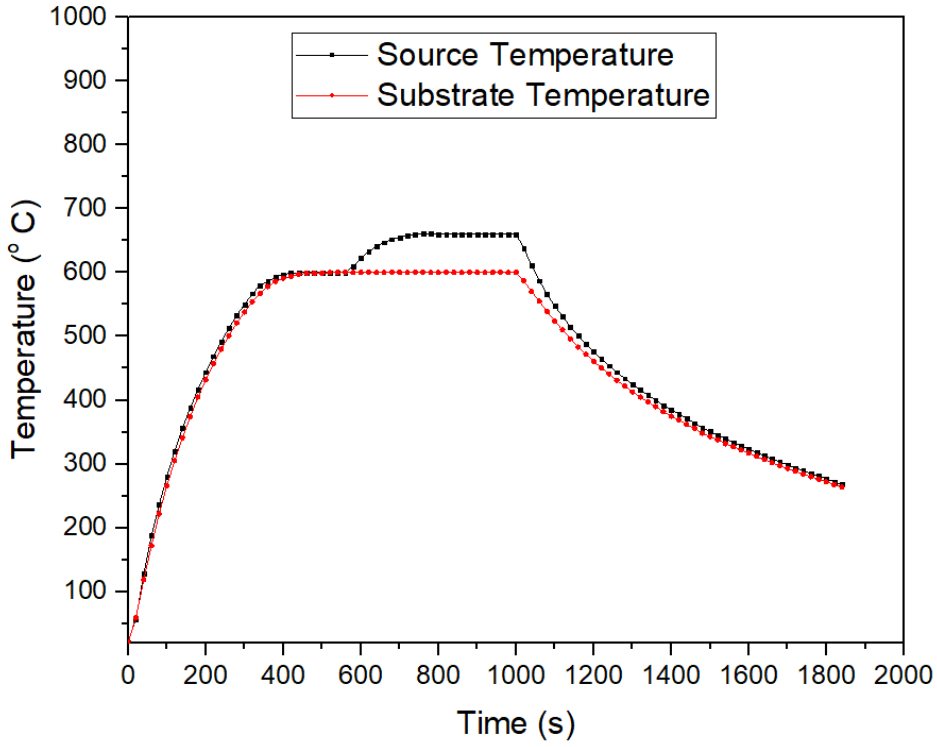

Fig. 2.5: Temperature Profile of bespoke CSS System.

2.1.5.a CSS process and system sensitivities

While the fabricated system performed as designed and provided the means to complete this research project, like any other laboratory equipment, it has its constraints. In this section, the most important limitations are presented so the reader can have a complete representation of what the system can and can't do. Note that these limitations apply to every system with similar design and this section provides information about how to effectively address some of these issues for better process control.

Sublimation Control

Since this type of system does not include a shutter to initiate or stop the sublimation occurring, a baseline procedure is required to control each deposition. The deposition procedure is outlined as follows:

I. The chamber is evacuated to a base pressure of 10 mTorr. Subsequently gases are introduced at a sublimation pressure of 1 Torr.
II. T_{Sub} and T_{Source} are set to 300°C and power is applied to the heating element. Both T_{Sub} and T_{Source} are left at 300°C for 5 minutes to clear any residual water vapour or solvent.
III. T_{Sub} is then set to the target temperature of 515°C. When T_{Sub} has reached 450°C, T_{Source} is set to 630°C. This is to allow both T_{Sub} and T_{Source} to reach their targeted temperatures at the same time due to the power distribution of the lamps inside the heating element, identified from the system's temperature profile.
IV. When both T_{Sub} and T_{Source} are at their targeted temperatures, the deposition is considered to have started, and a timer is begun.
V. To rapidly stop sublimation occurring at the end of the deposition the chamber is flooded with N_2, raising the pressure to 300 Torr in 5 seconds, and the heating zone is removed from the main reactor.

T_{Sub} and T_{Source} thermal insulation

One of the most important parameters in CdTe sublimation is the ability to control the temperature difference between the substrate and the source. However, in CSS because the sublimation is diffusion limited, the source must be kept in close proximity to the substrate to achieve an acceptable thin film growth rate. This limits the temperature difference between the source and the substrate. In the designed system, the maximum temperature difference that could be sustained without the source heating the substrate was found to be 120°C at a 2 mm distance. It was possible to extend the temperature difference (to 150°C) by increasing the separation of the source and substrate, however, this greatly affected the deposition rate. Consequently, the 120°C temperature difference was the maximum used in this work.

2.1.6 The $CdCl_2$ annealing treatment

As mentioned in section 1.6.2, the $CdCl_2$ treatment is an essential step in the fabrication of CdTe solar cells. The $CdCl_2$ treatment can take place in situ or after the CdTe deposition and can be carried out using a solution process (e.g. $CdCl_2$:CH_3OH), in a gas phase (e.g. Cl_2 vapour), or in the solid phase ($CdCl_2$) by evaporation or close space sublimation [7]. In all the deposition processes, $CdCl_2$ requires elevated temperatures ($T_{Sub} \leq 350°C$) for a successful CdTe 'activation' [32]. In situ deposition processes (e.g. co-sublimation of CdTe and $CdCl_2$) are considered to be industrially suited because no residual $CdCl_2$ remains. This makes the disposal of toxic $CdCl_2$ residues easier and more cost effective [33]. However, in situ treatments require constant and precise control of the CdTe deposition and Cl_2 flux, making the process very difficult. In contrast, $CdCl_2$ processes after CdTe deposition provide more process flexibility and require simpler equipment (a simple $CdCl_2$ evaporation and subsequent annealing on a hot plate is enough). However, precise control of the activation temperature and time is critical. Additionally, $CdCl_2$ treatments are usually optimised specifically to individual CdTe recipes, so deposition and annealing parameters are very difficult to duplicate/interchange between research/industrial laboratories [22].

For this thesis, $CdCl_2$ (99.999 % LTS Research laboratories Inc.) has been deposited by high vacuum evaporation using a quartz crucible placed in a tungsten basket. The subsequent annealing step was carried out in a closed titanium hot plate (Harry Gestigkeit) fitted with a 5-step temperature programmable controller (RR 5-3T). For improved control of the $CdCl_2$ annealing process the sample was placed on a graphite block to provide uniform heat transfer from the hotplate to the substrate (*Fig. 2.6).* The full optimisation details are discussed extensively in section *3.3.4* of *Chapter 3*.

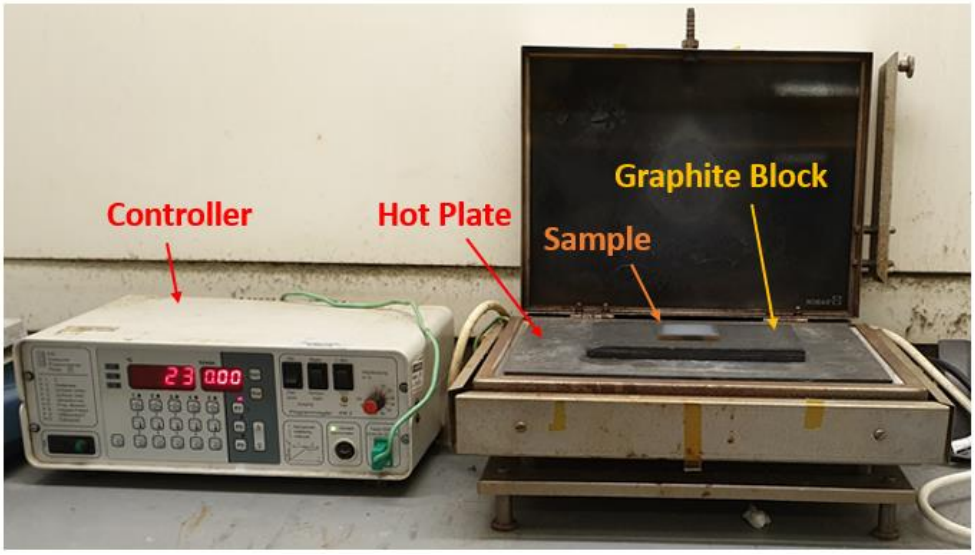

Fig. 2.6: $CdCl_2$ annealing equipment apparatus.

2.1.7 Back contact deposition

Back contacts for CdTe devices have been traditionally deposited by various deposition techniques such as sputtering, high vacuum evaporation, screen printing, CSS and VTD. Due to the formation of a Schottky barrier (details in section 1.6.4), contacting CdTe usually consists of a bi-layered film. First, CdTe receives a surface modification process (primary contact) to form a tellurium rich surface (p^+) and subsequently a secondary contact is deposited to act as the current transport layer [34].

To date, the best performing CdTe solar cells include a Cu-based primary contact in the cell structure. The benefits and deleterious effects of Cu in these devices have been extensively discussed in *section 1.6.4*. In summary, Cu primarily is responsible for p-type doping in CdTe, increasing the hole concentration by approximately one order of magnitude when diffused into the device. Cu can be introduced in the multi stack by numerous methods, but most commonly, Cu is added by alloying HgTe:Cu paste, by sputtering of ZnTe:Cu layer or by high vacuum evaporation of a thin Cu layer. The secondary contact is usually formed by the deposition of a metal (Au, Ni, Mo or Ag) [35]. Diffusion of Cu in the stack can take place by in situ annealing during the deposition of the back contact or by annealing after the Cu deposition.

For this thesis, Cu (99.99 % Kurt Lesker) has been deposited by high vacuum evaporation from a tungsten boat. The amount of evaporated Cu was precisely controlled using a quartz microbalance (Inficon STM-2 Rate/Thickness Monitor) and a shutter placed directly above the boat. Th secondary contact was achieved by gold (99.99 %, Testbourne) deposition in the same system without breaking the vacuum using a second boat as the source. Diffusion of Cu inside the stack was achieved by annealing in an oven. All contacts were deposited through a stainless-steel mask consisting of 5 x 5 cells with an area 0.25 cm^2 for each cell.

2.2 Thin film and device characterisation

2.2.1 Electrical device characterisation

2.2.1.a Current density – voltage curve (J-V)

The J-V curve is the primary output characteristic used when analysing a solar cell. The curve can be considered a graphical representation of the operation of a solar cell and is defined by four device performance indicators: open circuit voltage (V_{OC}), short circuit current density (J_{SC}), fill factor (FF) and efficiency (η). In a J-V curve the V_{OC} represents the x-axis intercept and is voltage obtained under open circuit conditions (i.e there is no load connected), J_{SC} represents the y-axis intercept and is the current density seen under short circuit conditions, and the FF describes the 'squareness' of the J-V curve [36]. The efficiency is the product of all the described parameters, divided by the incident light power. By analysing the parameters and shape of the J-V curve it is possible to acquire information about the parasitic resistances, maximum power point and any abnormalities in a solar cell's electrical performance. The J-V curve is produced by measuring the current as a function of an input voltage, using a source measurement unit under illumination from a solar simulator.

For this thesis, superstrate CdTe solar cells have been measured in a bespoke built solar simulator (*Fig. 2.7*), where the devices rest on a stage with the glass side down. Contacting the cell can be easily done from above without the need for the substrate to be suspended. In this configuration, the light source (1000

W Newport Xenon lamp), illuminates the individual cells through a 2-cm diameter aperture on the stage where the substrate rests. The light source was directed on the substrate using a 45° reflector, 2 multi-lens arrays and a convex lens to provide even distribution on the illuminated area. Before every measurement, the optic arrays where adjusted using a reference diode. Unfortunately, in this configuration temperature control of the substrate was not possible, however, measurements were taken as fast as possible to ensure limited voltage degradation due to increased temperature.

Substrate CdTe solar cells were measured using a commercial simulator (Abet technologies 10500) fitted with a 100 W xenon lamp. Substrate devices were placed on a temperature-controlled stage, fitted with a reference diode for measurement calibration. All measurements were taken at 25°C.

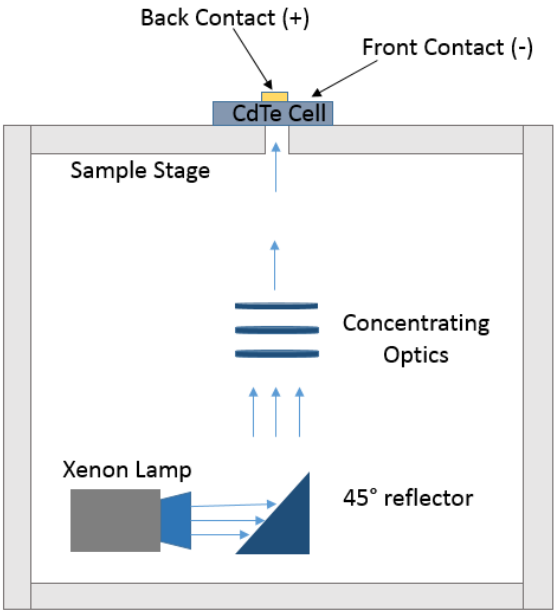

Fig. 2.7: Schematic diagram of home-made solar simulator.

2.2.1.b External quantum efficiency (EQE)

Quantum efficiency is defined as the number of carriers collected by a solar cell per photon of incident radiation of a given energy. QE can be expressed as External Quantum Efficiency (EQE) and Internal Quantum Efficiency (IQE). The difference between EQE and IQE is that in EQE measurements optical

losses (such as transmission and reflection) from the substrate and window layer are included where in IQE these are not taken into consideration. In this respect EQE is a quantum efficiency characterisation across of the whole device structure while IQE only refers to the quantum efficiency across the p-n junction [37]. In this thesis, only EQE measurements were considered.

In practice, EQE is obtained by measuring the photocurrent spectrum of a solar cell (spectral response) and comparing this with the photocurrent spectrum of a calibrated reference diode. The short circuit current density (J_{SC}) of the device is linked to EQE using the equation below and can be calculated by integrating the EQE curve across the entire spectrum [38].

$$J_{SC} = q \int \Phi(\lambda)\, EQE(\lambda) d\lambda \quad (2.5)$$

where q and $\Phi(\lambda)$ are electron charge and incident photon flux respectively.

EQE measurements were carried out using a commercial system (Bentham PVE300) fitted with a combination of a 75 W Xenon lamp and a 100 W quartz halogen lamp to cover the whole spectrum. The reference diode used for the system calibration was a Si photodiode. Superstrate samples were mounted in a home-made designed holder, and all of the measurements were taken in a range between 300 – 1100 nm.

2.2.1.c Capacitance -voltage (C-V)

Capacitance measurements are suited for probing bulk and interface properties of the absorber layer of solar cells. C-V is a widely used electrical characterisation technique, which can be used to identify parameters such as doping concentration, build in potential and depletion width of the p-n junction [7]. The capacitance-voltage (C-V) profiles usually show a U-shaped form commonly reported in literature and minima of the curve corresponds to the carrier concentration [39].

The capacitance-voltage (C-V) profiles were obtained with a Keysight E4990 impedance analyser at a frequency of 100 kHz. All measurements were taken under dark conditions with voltage biases between 1 and -1 V at room

temperature. Prior to capacitance measurements, the samples were kept in the dark for one hour to ensure a relaxed state.

2.2.1.d Hall Effect

For this thesis, resistivity, carrier concentration and hall mobility were measured using the Van der Pauw Hall Effect method using a Ecopia HMS-3000 Hall Measurement System. For a successful measurement, this method dictates that each corner of a 0.5 cm^2 square sample must be electrically contacted, and a series of current-voltage measurements are conducted.

For resistivity measurements, a predetermined current is applied between 2 adjacent contacts and the voltage drop is measured across the two opposite contacts. The process is replicated for all four configurations, the polarity is then reversed, and measurements are repeated. Sheet resistance (R_{sheet}) is calculated using the Van de Pauw equation and resistivity can be calculated by multiplication with the films thickness.

Carrier concentration can be measured by applying a current between a set of diagonal contacts in a perpendicular magnetic field. Voltage is then measured on the opposite diagonal contacts. The applied magnetic force pushes electrons to accumulate on one side of the film (Lorentz force) creating a Hall voltage (V_H). The carrier concentration can be calculated using the equation below:

(2.6)

$$V_H = \frac{IB}{qN_s d}$$

where N_s is the sheet carrier concentration, d is the film thickness, B is the magnetic field and I is the applied current. The bulk carrier concentration N_b can be calculated by dividing with the film thickness d.

The Hall mobility can be calculated using eq. 2.7 below:

(2.7)

$$\mu = \frac{1}{qN_s R_{sheet}}$$

2.2.2 Optical and structural device characterisation

2.2.2.a Scanning Electron Microscopy (SEM) and Transmission Electron Microscopy (TEM)

With scanning electron microscopy (SEM) it is possible to acquire in depth analysis of the surface and cross section of thin films through utilisation of a focus beam of electrons. In summary, a beam of electrons is focused through electromagnetic lenses on an area of the sample utilising an electron gun. Atoms inside the sample interact with electrons emitted (absorbed, scattered or transmitted). Through this process, detailed imaging of the sample is possible due to different electron scattering in an investigated area.

Transmission electron microscopy (TEM) uses high accelerated voltages on ultrathin (~ 200 nm) samples to penetrate the investigated sample area. The imaging of the investigated sample is possible through the detection of the transmitted electron beam trough the specimen instead of the scattered electrons. Compared with SEM, TEM can produce significantly higher resolution images in higher magnification.

For this thesis, cross section and planar SEM measurements were carried in a LEO 1530 VP, Field Emission Gun (FEG)- SEM. This instrument provides high spatial resolution (~ 2 nm) with low accelerating voltages (5 kV) through utilisation of in lens detectors. Chemical analysis of the samples was carried out in the same system with Energy Dispersive X-ray analysis. Prior to SEM analysis samples were scribed and cut with a diamond cutter and coated with gold-palladium via sputtering to avoid charging.

TEM analysis was carried out by Tecnai F20 operating at 200 kV, fitted with an EDX detector (Oxford instruments X-max N80 TLE SDD) for chemical analysis and production of elemental maps. Prior to TEM analysis samples were prepared by Focus Ion Beam (FIB) milling utilising a FEI NOVA 600 Nanolab dual beam. A standard in situ lift off method was used to prepare cross-sectional samples through the coating into the glass substrate. A platinum (Pt) over-layer was deposited to define the surface of the samples and homogenise the final

thinning of the samples. An example of a typical TEM image for a CdS/CdTe device sample is illustrated in *Fig. 2.8*.

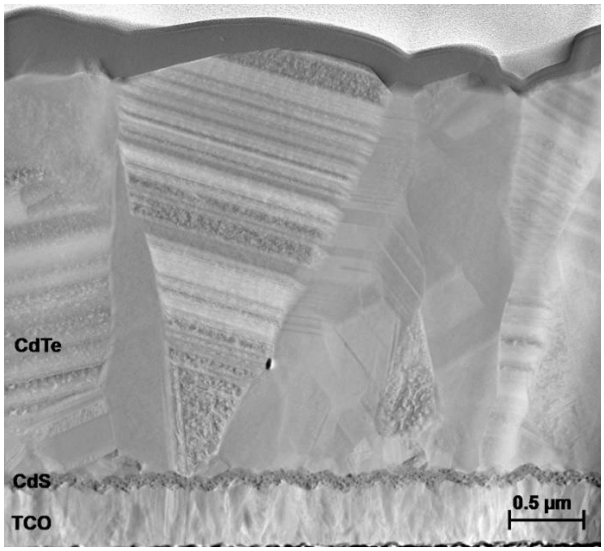

Fig. 2.8: TEM of a CdS/CdTe solar cell.

2.2.2.b Spectrophotometer

The generated photocurrent of a CdTe solar cell is directly related to the optical properties of each layer that constitute the heterojunction device. Through spectrophotometric analysis of the individual layers, it is possible to optimise the optical properties (transmission, reflection and absorption) of each layer to effectively improve the device performance.

The optical properties of TCO, CdS and CdTe thin films were carried out using a Cary 5000 (Agilent Technologies, USA) spectrophotometer. Transmission measurements were acquired through an integrating sphere in 1 nm step resolution in the range of 200 to 1800 nm unless stated otherwise.

Prior to thin film optical measurements, a baseline correction was performed for system calibration. For transmission measurements (e.g. *Fig. 2.9*) samples were mounted on the entrance port of the integrating sphere with the glass side of the substrate facing the beam. Measurements included direct and diffuse transmission. This set up was found to best simulate a superstrate solar cell in realistic conditions where the light passes through the glass first and then reaches the actual solar cell. The advantage of this set up is that any changes due to refractive indices of the glass are included in the measurements. During

transmission measurements, the reflectance port was covered with a reference reflectance disk (PTFE).

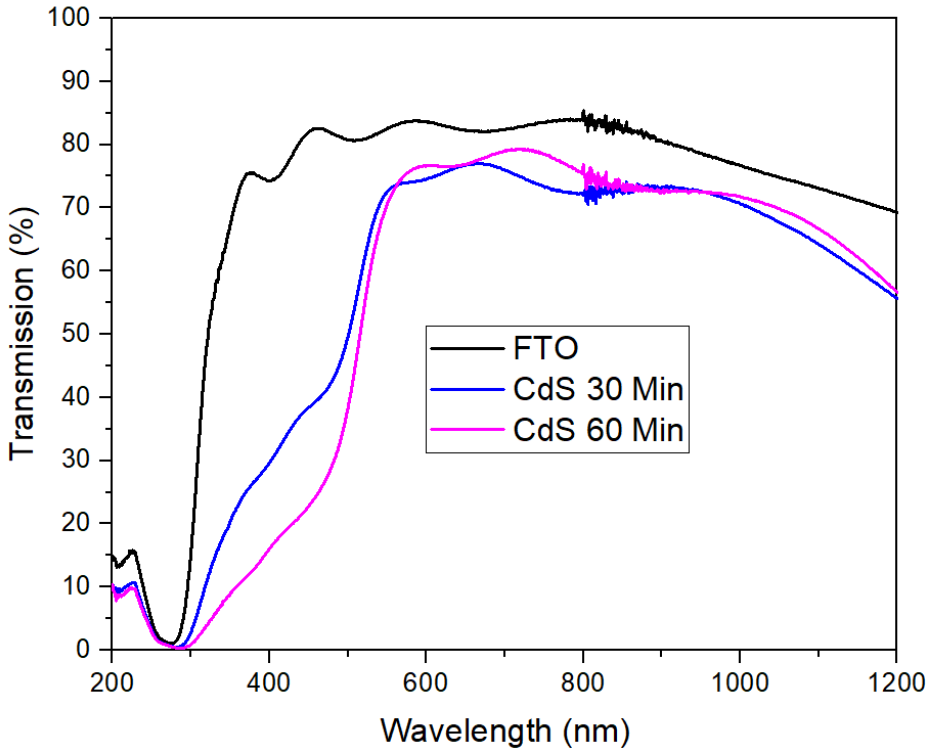

Fig. 2.9: Example of transmission curves of various thin films.

2.2.2.c X-Ray Diffraction (XRD)

X-Ray Diffraction (XRD) uses Bragg's law ($n\lambda = d\ Sin\theta$) to determine the preferred orientation of crystalline thin films, where λ is the incident wavelength, d is the atomic layer spacing in crystal lattice and θ is the diffraction angle. In practice a monochromatic beam of incident X-rays is focused on a sample at different consecutive angles. Diffracted beams are collected in a detector and specific angle intensities are recorded. This results in specific diffractograms from different crystallographic planes of the material and identification of the predominant crystal plane is possible.

In this thesis, samples were measured using a Bruker D2 Phaser bench -top XRD system. The system is equipped with a 1.52 nm Cu anode for generating the X-rays. The 2-theta (2θ) range used for the measurements was from 20° to 90°, with a step size of 0.02° and 0.1 s dwell time. This set up was used to be

able to capture and identify the full CdS and CdTe diffraction spectrum. Results were compared to powder diffraction files from the International Centre for Diffraction Data (ICDD).

2.2.2.d Photoluminescence Analysis

Spectrally resolved photoluminescence (PL) characterisation uses the principle of radiative recombination emission of photons in a semiconductor material. Using this method, it is possible to determine the material's bandgap. Additionally, it is possible to collect information about impurities and defects present inside the material and the overall device's interfaces. In practice a sample is excited by a light source with an energy larger than the materials bandgap. During the measurement, the light source has a fixed wavelength and power. Generated electron-hole pairs recombine radiatively emitting photons. Collection optics direct the emitted photons into a monochromator and subsequently are detected by a photodetector resulting in PL intensity – wavelength [38].

Spatially-resolved photoluminescence (PL imaging), differs from PL spectra in that the whole area of the sample is exited from a light source and the emission detection is carried out a camera. The resulting information acquired from this technique can be spatially resolved images with qualitative and quantitative information about efficiency limiting impure regions [40].

Time-Resolved Photoluminescence (TRPL) uses a similar principle to PL spectra; however, excitation of the sample is through a pulsed light source instead of a steady state. TRPL measures the luminescence decay from radiative recombination as a function of time providing information about minority carrier lifetime and material impurities and defects [41].

In this thesis, PL spectra and TRPL measurements have been carried out in a bespoke combined measurement system. For PL Spectra, samples were excited using a 640-nm 2.5 MHz pulsed laser unless stated otherwise. The system is fitted with a InGaAs photodiode with a wavelength range of 500 to 1700 nm for PL emission detection. The scanning range was from 700 nm to 1000 nm to cover the whole spectrum for CdTe. TRPL measurements have been

carried out using a photomultiplier tube (PMT) (230-920nm range) for emission detection.

PL imaging was carried out using a home-made system. A 405 nm LED was utilised as the excitation source, with a Si CCD camera fitted with a 720 nm long-pass filter. Exposure time for all the measured samples was kept to 10 seconds. All measurements were taken at room temperature, with the sample positioned with the glass side of the substrate facing the camera. A more detailed analysis of PL imaging is provided in *section 4.3.1.*

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Chapter 3. Sensitivities of a reliable baseline process for CdTe solar cells

3.1 Introduction

Prior to this work, it is important to note that there was no capability of depositing CdTe by CSS at CREST. The primary deposition method for CdTe within this lab was pulsed DC magnetron sputtering, however this proved to be an extremely difficult method of depositing CdTe suitable for solar cell applications. The maximum efficiency was ~5%, and it was difficult to optimise specific interfaces, due to the devices having low performance, and poor repeatability. It was therefore necessary to develop a CSS system which was able to provide a much more robust process. With this in mind, this chapter highlights the process sensitivities seen in producing a repeatable and reliable baseline process, allowing the investigation of interface effects through comparative studies. For this purpose, a simple structure of a CdTe solar cell was used, to achieve an acceptable device performance in a relatively short period. The proposed structure is illustrated in *Fig. 3.1*.

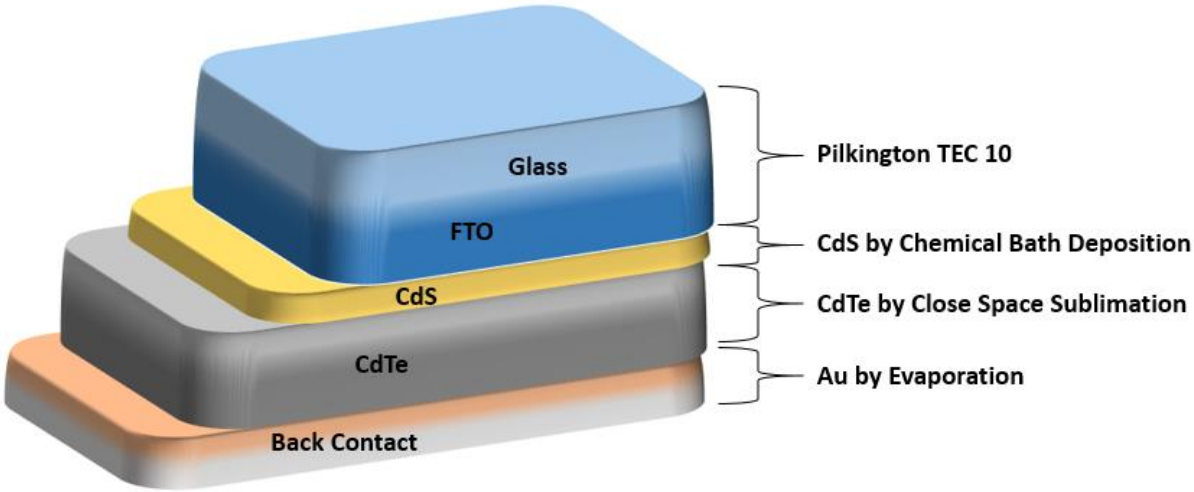

Fig. 3.1: Baseline Process Proposed Structure

The sequence of the baseline optimisation was divided in two processes which consist of:

a) Thin film optimisation

b) Device optimisation.

A flow chart with more detail about the optimisation process is illustrated in *Fig. 3.2.*

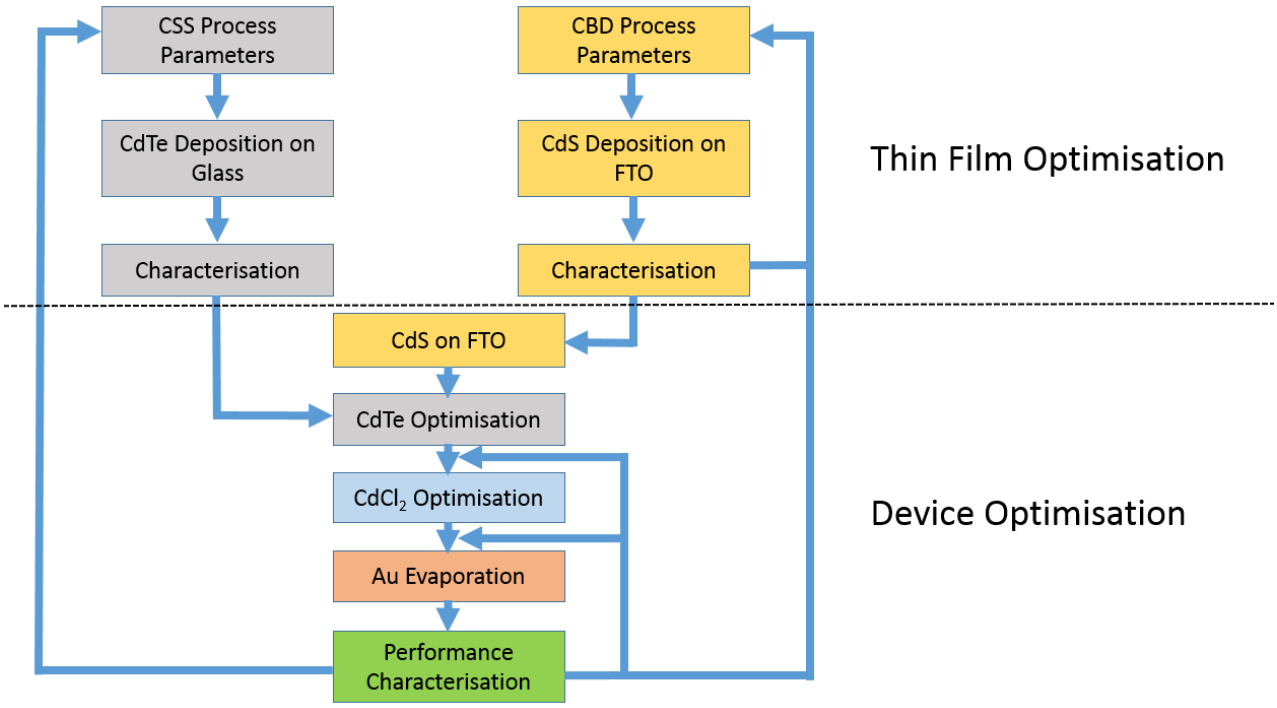

Fig. 3.2: Flow chart of baseline process optimisation

3.2 Thin film optimisation

3.2.1 CdTe deposition by CSS

The first step to form a repeatable baseline process was the optimisation of the CdTe layer. In this section the effects of substrate and source temperatures, deposition time and CdTe powder preparation using CSS were investigated.

As explained in *Chapter 2* (*2.1.4*) CSS consists of sublimating CdTe from a source material on to a substrate by having a temperature difference between the two. For CdTe, the source material can be in the form of a powder, beads or a sintered film [1][2]. Sublimating from a source plate (sintered film) has the

advantage of preventing spitting of CdTe particles when the substrate directly faces the source during deposition. This minimises the surface roughness of the film and attains good uniformity once deposited on the substrate [2]. Additionally, this process can act as a purification step resulting in higher purity CdTe thin films when compared with the source material [2]. In this work, a CdTe source plate was fabricated by sublimating a very thick CdTe layer (~ 300 µm) on a substrate from pressed CdTe powder, which can be later used as the main source for films deposited for solar cell fabrication [3]. The source plate must be able to withstand multiple thermal cycles (temperatures up to 700° C). Consequently, borosilicate glass (Eagle XG Corning) or quartz must be used for source plate fabrication.

3.2.2 Source plate deposition and characterisation

Initially, 5.5 mm x 5.5 Eagle XG glass substrates were ultrasonically cleaned in a DI water solution containing 10% IPA and 10% acetone, for 1.5 hours at 60°C. CdTe powder (Alfa Aesar, 99.999%) was then placed on the substrates, and then subsequently sublimated on to another borosilicate substrate.

Source plate optimisation was carried out by varying substrate and source temperatures, working gas partial pressure, substrate to source distance, deposition time and CdTe powder preparation. Deposition parameters of different source plates are summarised in *Table 3.1* below. Characterisation of CdTe source plates was performed using SEM, XRD and EDX.

Table 3.1: Summary of source plate's deposition parameters.

Substrate temperature range (°C)	560 – 600
Source temperature range (°C)	680 – 700
Separation (mm)	2
Partial pressure (Torr)	0.4 - 0.7
Powder preparation	Spread or Compacted

3.2.2.a Investigation of powder preparation

Two source plates using identical deposition parameters were created to investigate the effect of CdTe powder preparation on the CSS process. In both cases, substrate and source temperatures, N_2 partial pressure and separation were kept constant at 560°C, 680°C, 400 mTorr and 2 mm respectively for a 30-minute deposition. Equal amounts of CdTe powder (0.8 g) were spread on glass substrate or compacted using a soda lime glass as a presser.

Results showed that void free CdTe films can be produced with an average grain size of 12 µm for both pressed and unpressed powder. However, compacting the source material prior to deposition has a positive effect on deposition rate (deposition rate increased from 1.2 µm/min to 3.2 µm/min) resulting in thicker source plate films. EDX characterisation showed a stoichiometric composition on both source plates. Further increase of substrate and source temperatures to 600°C and 700°C respectively resulted in higher deposition rates (5.25 µm/min) and much larger grains as expected [4]. However, source plates exhibited poor uniformity with the presence of voids visible as illustrated in *Fig. 3.3*.

Voids on CSS films at high temperatures (>450°C) can be formed either by re-sublimation of CdTe vapour from the substrate during the cooling cycle [1] [5], or by interruption of the process before completion of island growth into a continuous film [6]. To rapidly stop the sublimation process, the chamber was flooded with N_2 increasing the process pressure from 400mTorr to >300 Torr. At the same time, the heating zone was removed, and the temperature rapidly decreased from 700°C to 550°C in 35 seconds. At 550°C, the vapour pressure of CdTe is ~ 4.5 Torr, and so sublimation should halt once the ambient pressure is greater than 4.5 Torr. Due to this rapid change in pressure and temperature to a process condition where CdTe cannot sublimate, the presence of voids in the final film must be related to insufficient CdTe powder, which resulted in interruption of island growth and grain coalescence.

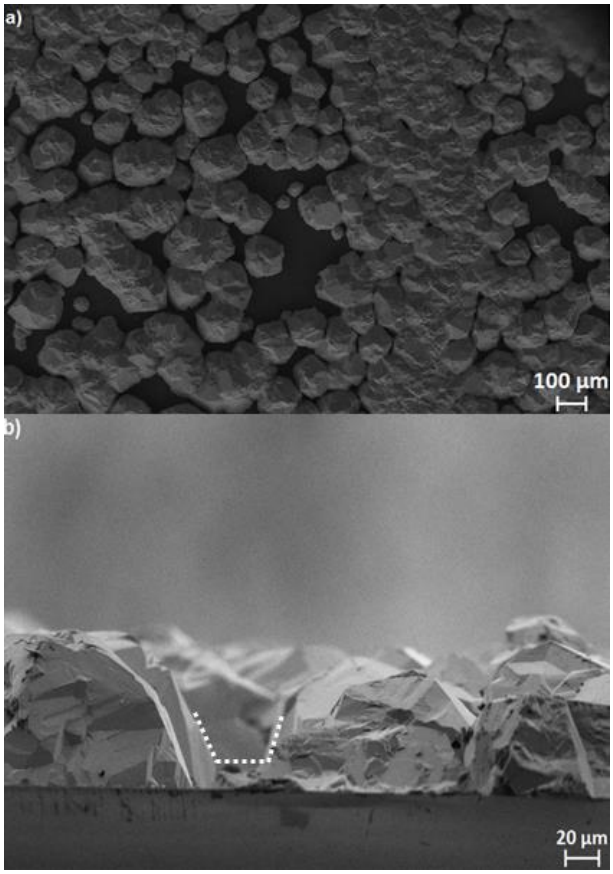

Fig. 3.3: a) SEM planar view of void formation on the CSS fabricated source plate and b) SEM cross section of voids (white dotted line).

3.2.2.b Graphite crucible and effect of source plate adhesion

The source plate must be able to withstand multiple thermal cycles without detachment of the CdTe film. Initial results showed that adhesion of CdTe on the source plate presented a problem, where after the source plate deposition, CdTe was delaminating from the substrate.

Eagle XG glass has a thermal expansion coefficient of 3.17 $x10^{-6}$/°C and a softening point of 978°C, whereas quartz (fused silica) exhibits a smaller thermal expansion (~ 0.55 x 10^{-6} /°C) and higher softening point of 1683°C [7]. Empirically, it was found that with using quartz substrates, the CdTe source plate could withstand multiple thermal cycles with the CdTe layer showing better adhesion properties, which is most likely related to the difference in the expansion coefficients between the substrates.

To further improve adhesion, quartz substrates received a 1 minute etch in 1:5 HF to DI water after standard cleaning. This process increased the surface roughness of the substrate aiding the adhesion of CdTe [8]. Additionally, the use of a SiC coated graphite crucible improves the quality of the CdTe source plate. It was found using a crucible improved the uniformity and thickness of the deposited films because it was possible to use significantly more CdTe powder in the course (5g in this case, opposed 0.8g previously). This enabled longer deposition times where a continuous CdTe film at higher temperatures could be formed. Additionally, a bespoke "presser" was used to compress the CdTe powder within the crucible. Compressing the CdTe powder was found to reduce CdTe 'spitting' during sublimation of the source plate, decreasing the roughness. To further compact the powder, the crucible was loaded inside the CSS and annealed at 300 Torr for 30 minutes at 550°C. Due to the high pressures used, and lack of temperature gradient between the source and substrate, sublimation is supressed, and the CdTe powder becomes a solid compact film.

3.2.2.c Optimised source plate deposition

The prepared crucible with the compacted CdTe powder and quartz substrate were placed in the vacuum chamber and separated using quartz spacers (2 mm). To fabricate the optimised source plate Ar was used instead of N_2. Empirically it was found that using Ar reduces stress during source plate fabrication and the source plate can withstand several more deposition cycles compared to using N_2. This improved the CdTe throughput from each source plate. During this process, the pressure was kept at 450 mTorr with 20 sccm of Ar. The substrate and crucible were then subjected to a 5 minute anneal at 300° C to remove any residual water present on the substrate. The source and substrate temperatures were rapidly increased, to 680°C and 560°C, and the deposition time was fixed to 1 hour, which results in 300 - 350 µm thick source plates. To end the sublimation, the chamber was flooded with N_2 raising the pressure to 300 Torr in 5 seconds. The optimised steps involved to complete the source plate are summarised below.

1. 5 g of CdTe powder is placed in a SiC coated crucible. The powder is compressed using a home-made presser.

2. The crucible is loaded in the CSS and annealed at a pressure of 350 Torr. T_{Sub} and T_{Source} are kept at the same temperature (550^{o} C) to supress sublimation.

3. The quartz source plate is loaded in the chamber with the crucible to initiate the source plate deposition. The substrate and crucible are subjected to a 5 minute anneal at 300° C to remove any residual water present on the substrate. T_{Sub}, T_{Source}, pressure and separation are kept at 560 ^{o} C, 680 ^{o} C, 450 mTorr and 2 mm respectively during deposition. Source plate deposition duration is 1 hour. This results in ~300 - 350 µm thick CdTe layer.

3.2.2.d CdTe thin film deposition and characterisation

CdTe thin films for use in solar cells were then deposited using the same CSS system. Ar was introduced in the chamber at a deposition pressure of 700 mTorr. The source and substrate were ramped to 300 °C for a 5-minutes to remove any residual water present in the chamber, and then the source and substrate temperatures were increased to their target temperatures. For the entire length of this experiment the substrate temperature was kept constant at 515°C while the source temperature and deposition time were varied from 610°C to 630°C and 1 to 5 minutes respectively to investigate the effects on CdTe grain growth. Spacing between the source plate and substrate was kept constant at 2 mm.

Fig. 3.4 (left) shows SEM results for CdTe films grown at three different source plate temperatures while pressure, substrate temperature and deposition time remain constant (515 °C, 700 mTorr, and 5 minutes respectively). It was found that the growth rate strongly depends on the source temperature. At a source temperature of 610°C, (*Fig 3.4.a*) films exhibit poor area coverage with voids present between grains. Island formation and island coalition are clearly visible. The average island size is around 35 µm. Increasing

the source temperature to 625°C (*Fig. 3.4.b*) island size increased to an average of 41 µm while island coalition density in the film also increased, however, full substrate coverage still does not occur. Further increase of source temperature to 630°C, (*Fig. 3.4.c*) resulted in a 30 µm thick void free film, with an average grain size of 26 µm. XRD characterisation (*Fig. 3.5*) showed a zinc blende CdTe structure highly oriented along the (111) direction in agreement with literature [9]. EDX showed close to stoichiometric sublimation with equal atomic percentage of Cd and Te (50.31% Cd and 49.69 % Te)

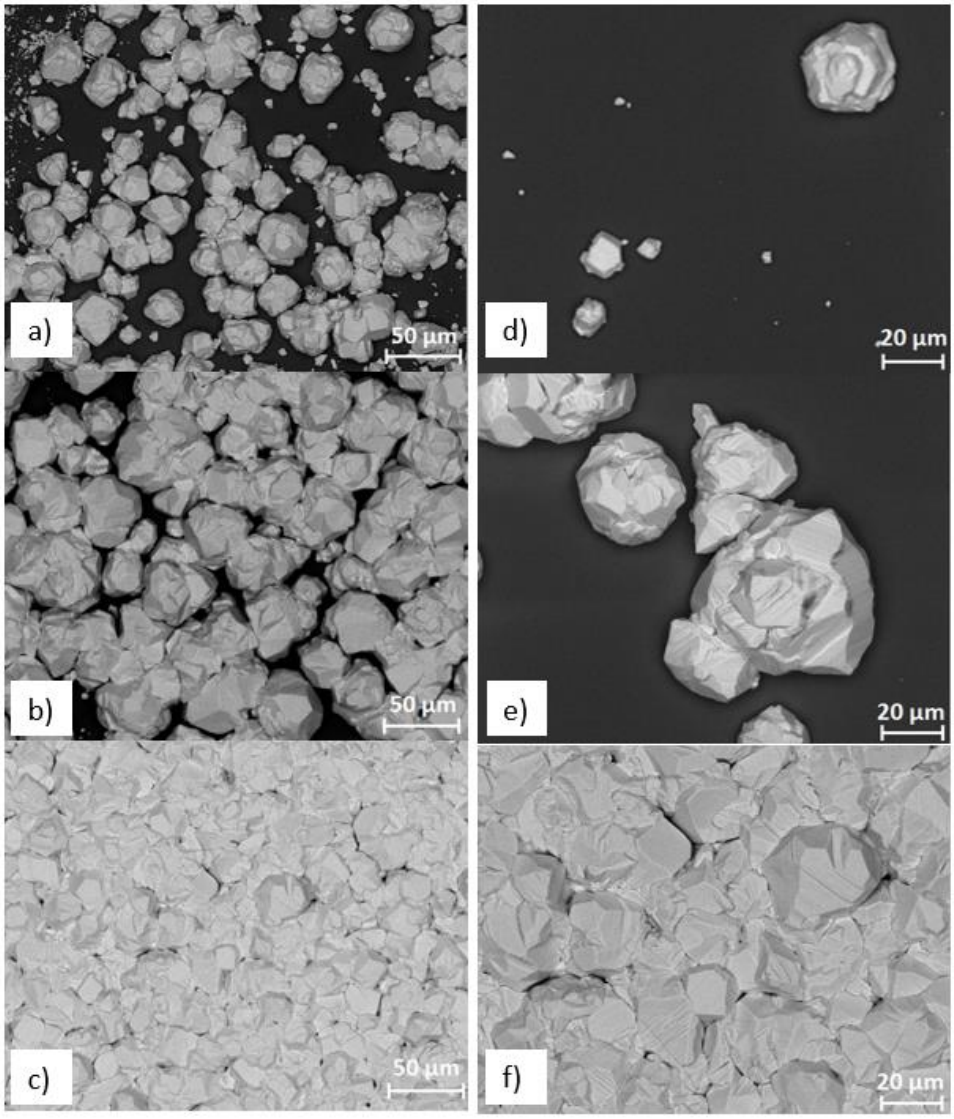

Fig. 3.4: (Left): SEM of CSS CdTe films deposited a) 610°C, b) 625°C and c) 630° for 5 minutes and (Right): SEM of CSS CdTe Films deposited at a) 1 minute, b) 2.5 minutes and c) 5 minutes at 630°C.

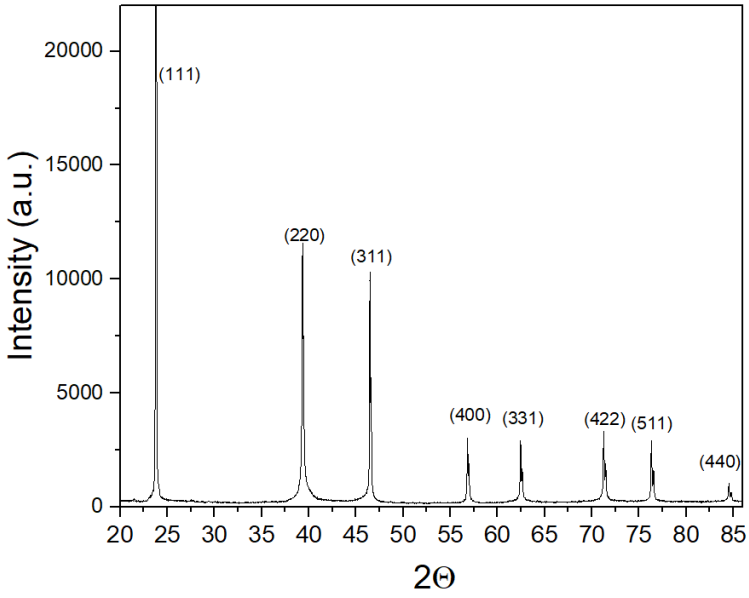

Fig. 3.5: X-Ray Diffraction of CSS CdTe deposited film at Tsub, Tsou and separation of 515℃, 630℃ and 2 mm respectively.

The same deposition parameters which provided the 30 µm film were used to investigate the effect of deposition time on the growth rate. *Fig. 3.4 (right)* shows SEM surface images for films grown for 1, 2.5 and 5 minutes. The substrate and source temperature were kept constant at 515°C and 630°C respectively.

After 1 minute, there was little CdTe growth, with very poor surface coverage over the substrate. *Fig. 3.4.d* shows this, with an average grain size of around 25 µm. According to the Volmer-Weber growth model [6], this corresponds to the initial stages of the film growth where the formation of individual islands occurs [6]. By increasing the time to 2.5 minutes, the thin film surface coverage increases, however there is still a significant void fraction observed. It is clear in *Fig. 3.4.e* that the individual islands are starting to coalesce, and the formation of a single larger island can be seen. At this stage, individual island growth has reached a maximum size of around 40 µm, where individual islands are coalescing and forming larger grains. At the same time, secondary island formation continues in accordance to Volmer-Weber growth model [6] illustrated at in *Fig. 3.6.* An increased deposition time to 5 minutes results in the formation a 30 µm thick void free CdTe film (*Fig 3.4.f*).

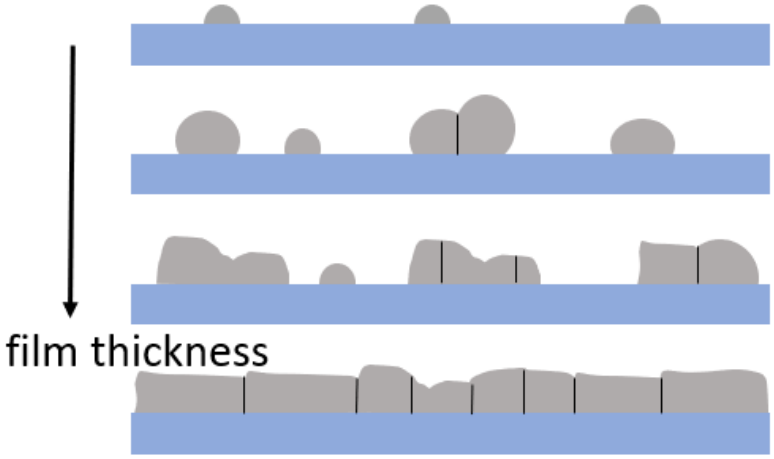

Fig. 3.6: Volmer – Weber growth model [10].

3.2.3 CdS thin films by chemical bath deposition

One of the most important requirements of the CdS layer for achieving a high performing device, is uniform coverage of the buffer layer. This lowers the risk of pinhole formation, avoiding shunts that limit the device performance [11]. To establish the baseline, thick CdS films (~ 100 nm) were initially used, and then the CdS was gradually reduced in thickness to improve the performance of the device. The effects of CdS thickness on device performance are explored in *Chapter 5*

3.2.3.a CdS thin film deposition

Prior CdS deposition the (50x50) mm^2 substrates (Pilkington TEC 10, FTO) were subjected to the same cleaning process as section *3.2.1.a* and the reaction vessel was preheated to 70°C. Substrates are placed two at a time in a Teflon holder and the precursors outlined in *Table 2* are added one at a time in 200 ml of DI water. An ultrasonic probe is used to agitate the solution. The deposition time required to deposit a 100-150 nm CdS film is 1-hour. After the deposition, the substrates are rinsed with DI water and dried with compressed air.

After the CdS deposition, the excess CdS layer on the back of the substrate is removed using HCl, rinsed with DI water and dried with compressed air.

Table 2. 3.2: Precursors for CdS by CBD.

Chemical	Volume (ml)	Molarity (M)	Function
Cadmium acetate ($Cd(CH_3COO)_2$)	20	0.01 M	Cadmium source
Ammonium hydroxide (NH_4OH)	35	25 M	Complexing agent
Thiourea ($CS(NH_3)_2$)	20	0.1 M	Sulphur source

3.2.3.b CdS thin film characterisation

Optical properties and bandgap characterisation

Transmission and bandgap (Eg) measurements were carried out using a spectrophotometer. The optical bandgap (E_g), was determined by an extrapolation by linear fit of $(\alpha h\nu)^2$ vs energy curve.

In *Fig. 3.7* the optical transmittance (T%) is shown for the deposited CdS thin film on a TEC 10 substrate in comparison with a bare TEC 10 substrate.

As expected, the optical transmission reduces in the range between 300 nm to 520 nm due to CdS absorption. As mentioned in *Chapter 1,* carriers generated inside the CdS recombine possibly due to low carrier lifetimes (~ 0.1 ns) or high interface recombination, there CdS represents a region of a photocurrent loss [1][12]. The thickness of the 1 hour deposited CdS film was ~100 nm (*Fig. 3.8*). This was in agreement with CBD CdS used for highly efficient devices (range varies between 60 – 100 nm) [12] [13]. However, the objective was to achieve a uniform coverage on the substrate without pinholes. SEM analysis of the film (*Fig. 3.9*) show a uniform CdS layer with an average grain size of ~120 nm, which is in agreement with literature [14].

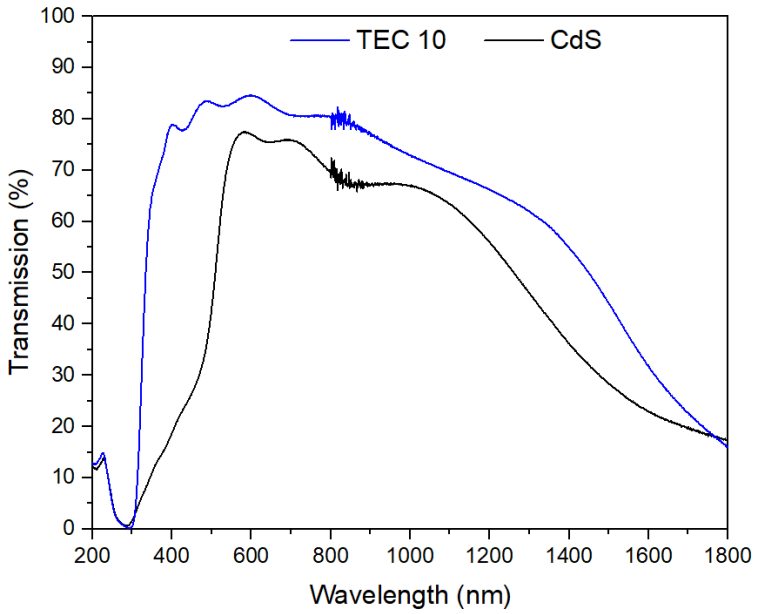

Fig. 3.7: Transmission curves of a bare TEC 10 substrate and CdS coated TEC 10 substrate, the figure shows the optical loss exhibited from the CdS deposited thin film

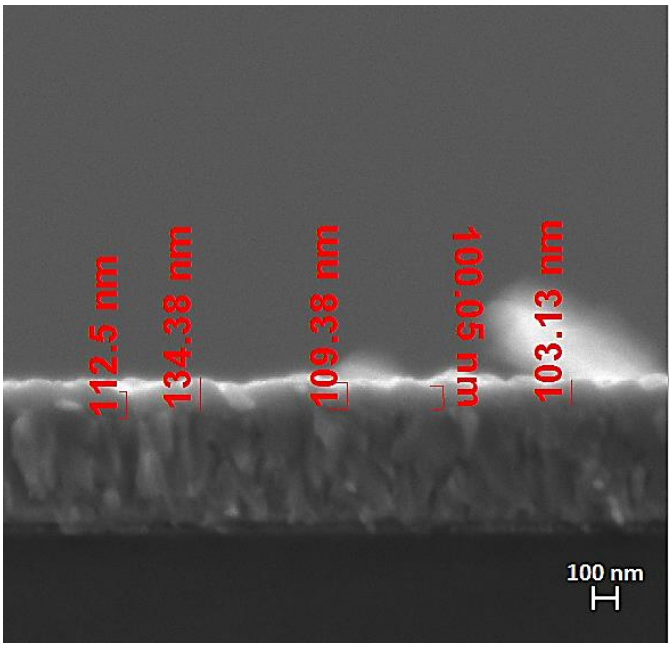

Fig. 3.8: SEM cross section of 1 hour CBD CdS film showing the thin film thickness.

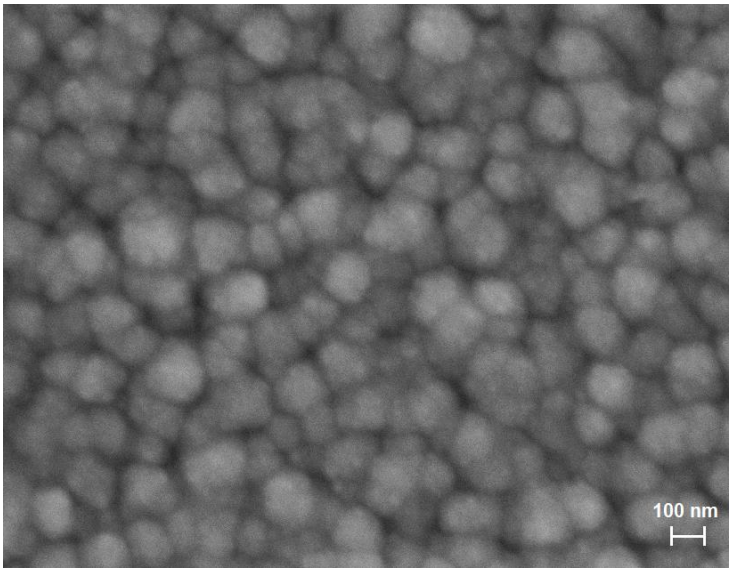

Fig. 3.9: SEM planar view of 1 hour CBD deposited CdS film.

In *Fig. 3.10* the Tauc plot of the as deposited CdS thin film is displayed. The extrapolation of the linear slope to the x-axis shows the direct transition of electrons between the valence band and conduction band (Eg) [14]. Here the bandgap of CdS was found to be 2.38 eV which is in agreement with literature when comparing similar thicknesses [15].

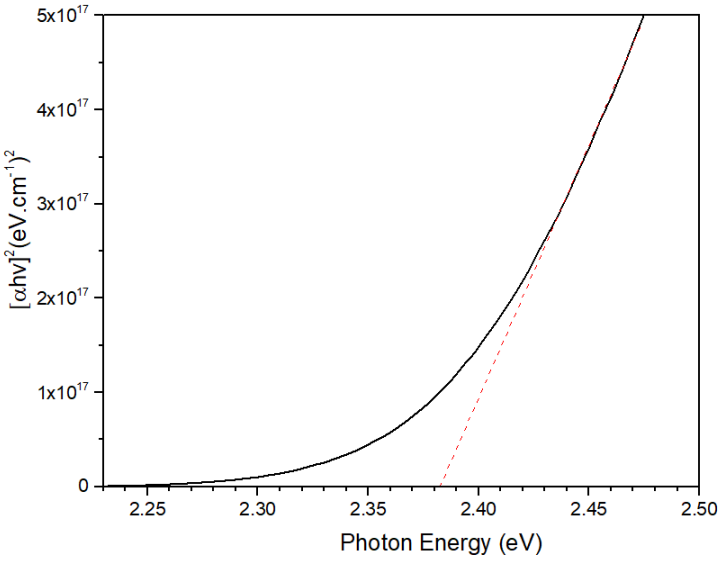

Fig. 3.10: Calculated bandgap (Eg) of 1 hour CBD deposited CdS film, the bandgap was found to be 1.38 eV.

3.3 CdS/CdTe device optimisation

Device optimisation was carried out by using the deposition parameters of individual layers discussed in the previous section and combining them into a complete device. Necessary modifications to the proposed structure were carried out through characterisation and by assessing the device performance according to *Fig. 3.2.*

3.3.1 As deposited device

In *Fig. 3.11* a TEM image of an as deposited device (before receiving a $CdCl_2$ annealing treatment) is shown. It was found that deposition of CdTe thin films on CdS substrates provided additional controllability of the sublimation process. Uniform CdTe films could be achieved at shorter deposition times due to the CdS increased surface roughness when compared to glass substrates. The deposition time was decreased to 3 minutes to limit the total thickness of the resulting films in order to reflect a more suitable process for PV applications. As deposited CdTe devices were found to exhibit a uniform layer with thickness of ~2.7 µm with an average grain size of ~1.5 µm and a columnar grain structure. Since the device shown in *Fig. 3.11* has not been $CdCl_2$ treated, the CdTe grains exhibits a high stacking fault density which can limit the device performance [16]. The CdS layer has a uniform thickness of ~ 100 nm along the CdS/CdTe interface. However, it can be observed that the CdS layer exhibits high porosity regions. This effect could have been caused because the deposition had progressed into the 'colloid by colloid' reaction as discussed previously in section 2.1.2 [17].

Fig. 3.12 show the J-V curve of a representative as-deposited device. The device exhibits low performance with efficiency, $V_{OC,}$ J_{SC} and FF of 0.07 %, 220 mV, 1.16 mA/cm^2 and 30 % respectively. This is in agreement with the literature where $CdCl_2$ untreated devices exhibit low performance due to the high stacking fault density seen in CdTe, and high interface defect density resulting in increased bulk and interface recombination. The first arises from poor

passivation of the grain boundaries while the latter occurs due to lattice mismatch between CdS and CdTe [18][19][20].

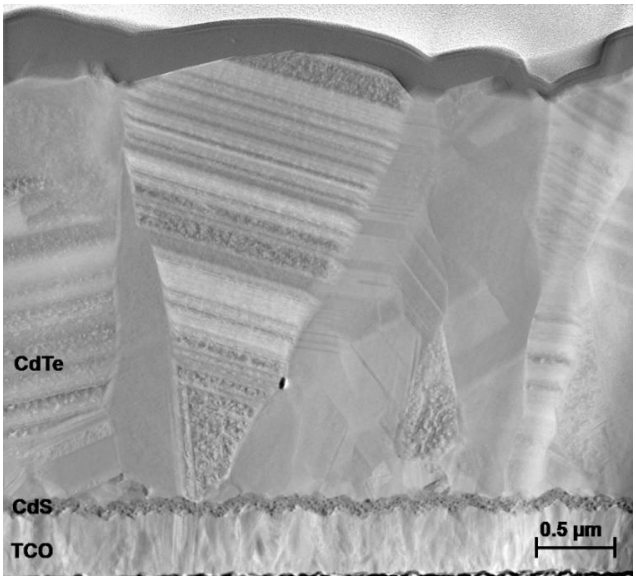

Fig. 3.11: TEM of as deposited CdS/CdTe device

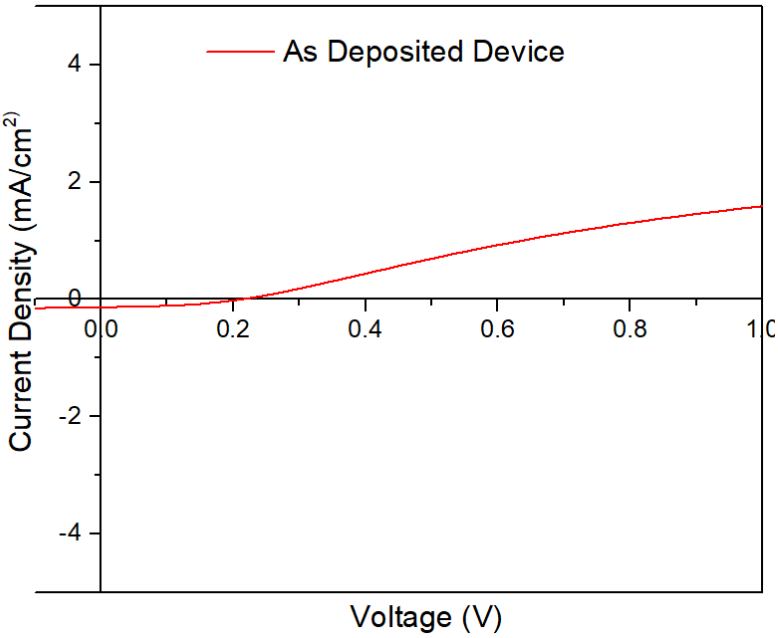

Fig. 3.12: J-V curve of as-deposited CdTe device which has not received a CdCl2 activation treatment. This device exhibits poor device efficiency (0.07%).

3.3.2 Effect of oxygen during CSS

This set of experiments were designed to optimise the CdTe layer on CdS thin films to improve the device performance. One possible way to enhance device performance is to add O_2 during CdTe deposition. Generally, O_2 is believed to act as a nucleation aid during CdTe sublimation providing better controllability of the sublimation procedure [1]. However, the amount of O_2 during CdTe deposition, which can be beneficial to a device, varies due to different deposition parameters and processes and exact adaptation from literature is impossible. The focus of this section was the investigation of the effects of oxygen inclusion during CdTe deposition on CdS films to further improve the performance of the baseline process.

Initially, CdS deposition was carried out as per the baseline process previously discussed. CdTe deposition was carried out by varying the O_2 concentration inside the CSS chamber by volume, where CdTe films with 0 %, 5 %, 10 % and 15 % oxygen concentration in Ar were deposited. The substrate and source temperatures were set to 515° C and 630° C respectively and the chamber pressure was kept always at 1 Torr for the entire length of this experiment. Upon introduction of O_2 the minimum achievable pressure by the system was ~ 850 mTorr depending on the oxygen concentration in comparison with 700 mTorr with only Ar. To keep the process conditions the same, pressure had to be raised to 1 Torr. Additionally, empirically it was found that raising the pressure to 1 Torr provided more controllability over the sublimation process with a slightly reduced deposition rate. The deposition time with varying O_2 content was adjusted accordingly to remain within the range of 2 - 4 µm in accordance with the baseline process. The film process parameters are summarised in *Table 3.3.* $CdCl_2$ was carried out using thermal evaporation of 0.5 g of $CdCl_2$ and subsequently annealed on a hot plate using two-step ramping conditions of 50°C/min up to 370°C and 5°C / min to the dwell temperature of 425°C, which was held for 1 minute. Back-contact deposition was carried out by thermal evaporation of ~ 84 nm of Au.

Characterisation of the devices was carried out using J-V, and EQE measurements.

Table 3.3: CSS process parameters

CSS deposition parameters	
Substrate temperature (°C)	515
Source temperature (°C)	630
Separation (mm)	2
Deposition pressure (Torr)	1
Oxygen concentration in Argon (%)	0-10

For high efficiency devices, it is necessary to have a uniform CdTe layer. A non-uniform CdTe layer with high pinhole density can exhibit shunting between the back contact and CdS reducing the overall performance of the device. Additionally, high pinhole density can introduce defects during the formation of the p-n junction which can act as recombination centers [21]. Devices were optically tested under AM1.5G illumination to identify pinhole density. Devices without any O_2 during CdTe deposition exhibited high pinhole formation density (*Fig. 3.13. a*), leading to poor coverage of the CdS layer by CdTe. In contrast, devices deposited in a O_2 containing environment showed uniform coverage of the CdS layer without any pinholes (*Fig. 3.13.b*). TEM analysis performed on the samples (*Fig. 3.14. a and b*) showed a reduction in the average grain size between devices with O_2 (~1.3 µm) and devices without O_2 (~ 1.8 µm).

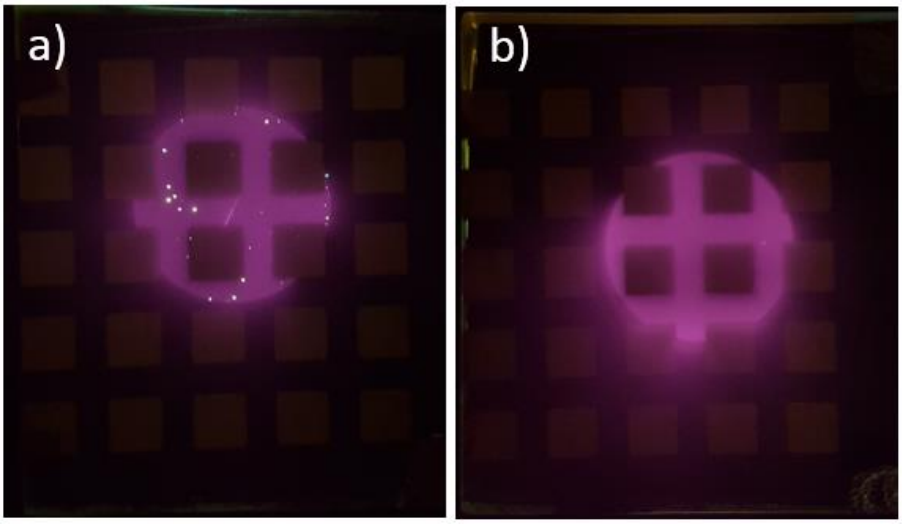

Fig. 3.13: Devices under AM 1.5G illumination a) No oxgen during CSS, b) 5% oxygen during CSS

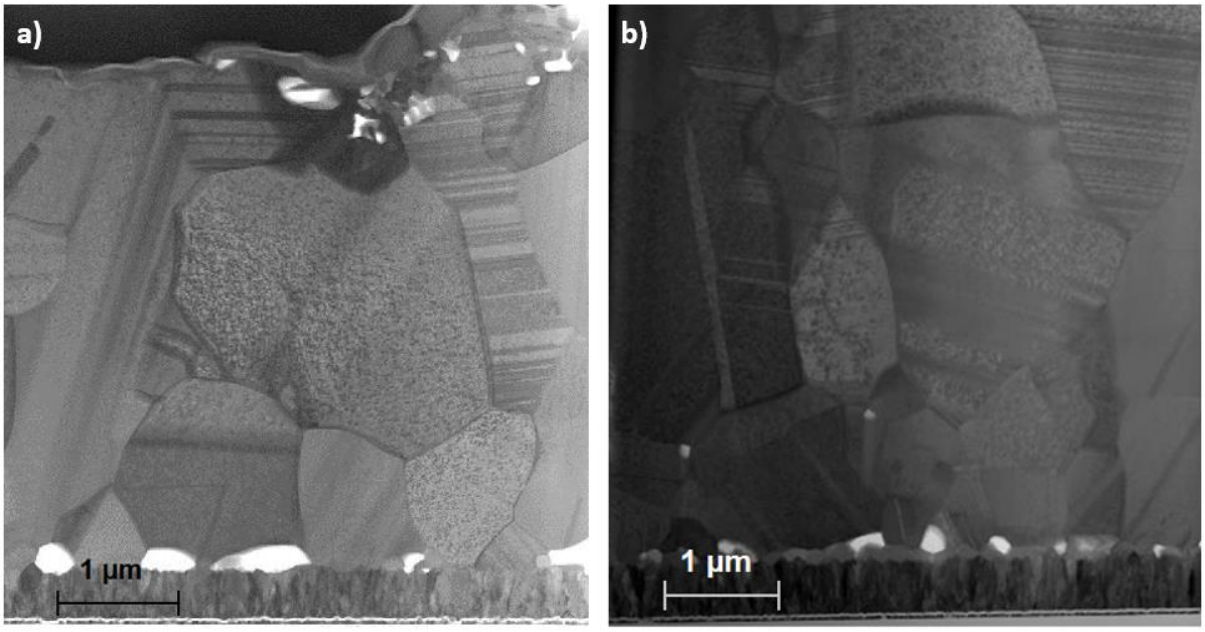

Fig. 3.14: a) TEM of device with No oxgen during the CSS process, b) TEM of device with 5% oxygen during the CSS process.

The results show that O_2 introduction during the CdTe deposition acts as a nucleation aid, which agree with previously reported literature [1][3]. O_2 was found to reduce the grain size of the sublimated CdTe films. This effect promotes the reduction of pinhole density and increases the homogeneity of the absorber (CdTe) on the emitter (CdS)

During CdS/CdTe interface formation, sulphur within CdS diffuses into CdTe forming sulphur rich ($CdTe_yS_{1-y}$) and tellurium rich (CdS_xTe_{1-x}) ternary compounds. These layers contribute to the reduction of recombination centers formed by the lattice mismatch (~10%) between CdS and CdTe [13]. However, during this interdiffusion process sulphur consumption results in CdS thickness reduction, where this can have deleterious effects for the device. CdS can be either consumed during CdTe deposition in CSS (due to high deposition temperatures > 450°C), or during the necessary $CdCl_2$ activation treatment (due to increase of the diffusion coefficient of sulphur) [1].

TEM analysis performed on the samples showed total consumption of the CdS layer in the device without any O_2 present during CdTe deposition (*Fig. 3.15.a*) while the device with 5% O_2 presented only partial consumption of the CdS layer (*Fig. 3.15.b*).

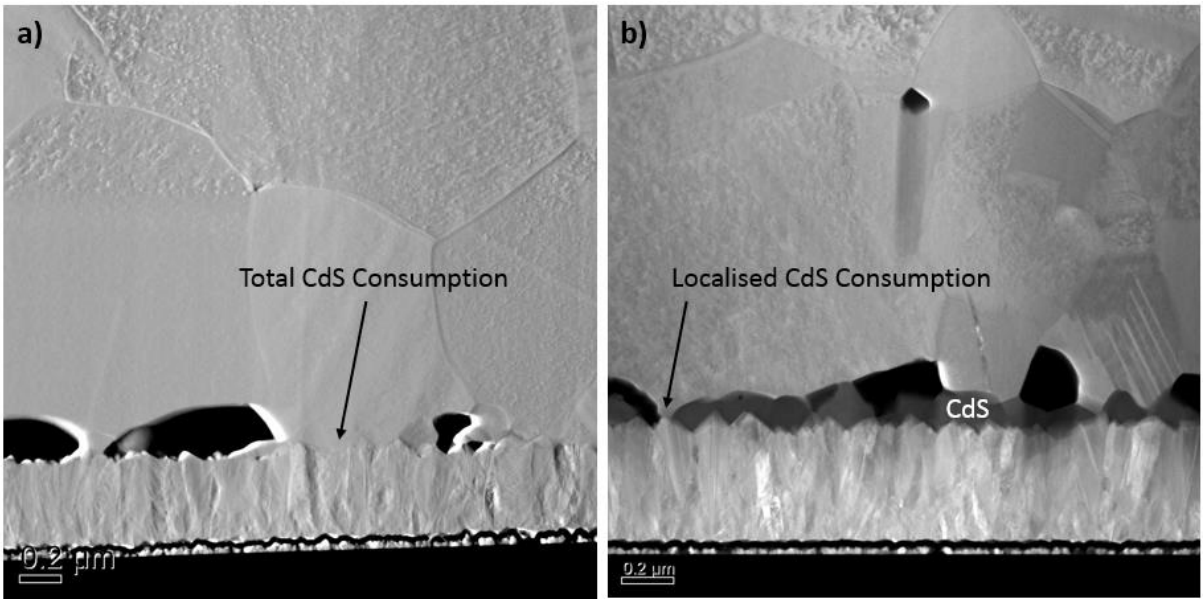

Fig. 3.15: a) TEM of device with no oxgen during CSS showing total CdS consumption, b) TEM of device with 6 % oxygen during CSS showing localised CdS Consumption

Considering that both devices received the same $CdCl_2$ activation treatment it can be concluded that the presence of O_2 during CdTe deposition leads to a reduction of sulphur diffusion through grain boundaries and prevents total consumption of the CdS layer [22]. This effect is beneficial for CdTe devices as

it prevents the formation of localised shunting between the TCO and the CdTe layers which can reduce the device performance.

In *Fig 3.16* the J-V curves of the best cells from each sample with 0 %, 5 %, 10 % and 15 % O_2 during CdTe deposition are shown with their associated performance indicators summarised in *Table 3.4.* From these results the trend observed is that introduction of O_2 during CdTe deposition has a beneficial impact on FF and V_{OC} of the device. The device without any O_2 incorporation exhibits 7 % efficiency with V_{OC} and FF of 664 mV, and 56.3 % respectively. Introduction of 5 % oxygen increased the V_{OC} by 40 mV and the FF by 2.4 %. Further increase of the oxygen content to 10 % and 15 % results in a FF increase of 58.6 % and 61.9 % respectively while the V_{OC} remains relatively constant in a range between 680 mV and 700 mV. The current density from the J-V curves for all the investigated devices varied in the range of 19.95 ± 0.65 mA/cm^2. The current density variation can be attributed to an expected device by device distribution and the measurement uncertainty in the solar simulator, therefore O_2 incorporation could not be associated with any current density variation effects.

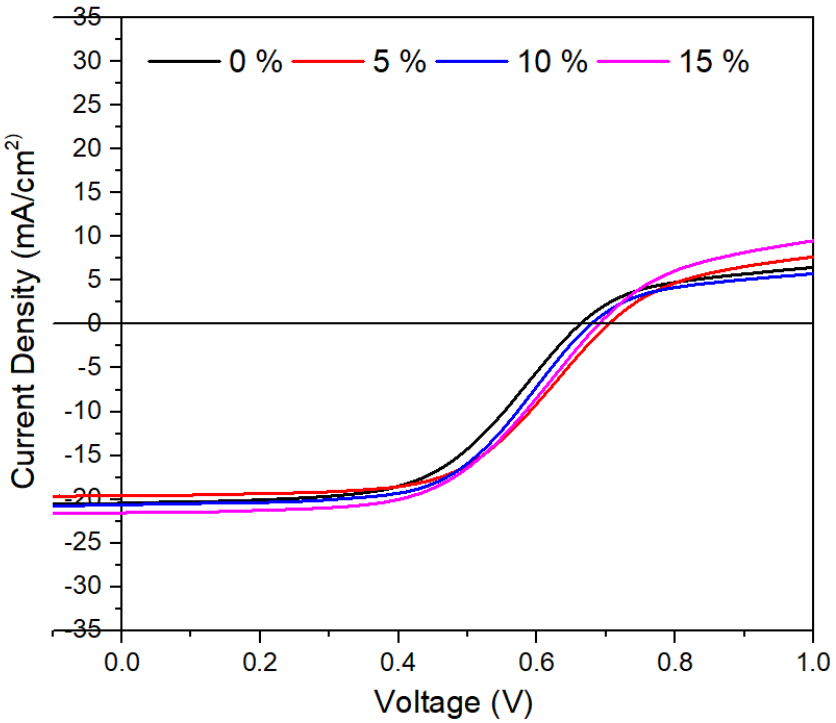

Fig. 3.16: J-V curves of devices with different amount of O_2 during CSS

Table 3.4: Performance indicators of devices with different amount of O_2 during CSS

Sample	Voc (mV)	Jsc (mA/cm²)	FF	Efficiency (%)
0 %	664	20.4	56.3	7.00
5 %	704	19.6	58.7	8.10
10%	679	20.6	58.6	8.22
15 %	702	19.3	61.9	8.40

The bandgap of the investigated devices (*Fig. 3.17*) was calculated by extrapolation of the linear slope to x-axis intercept of the curve of $[E \times \ln(1 - EQE)^2]$ vs energy. It is evident by the difference of the bandgap between samples with and without O_2 (bandgap shifts from ~1.46 eV to ~1.47 eV between non-oxygenated samples and oxygenated samples) that introduction of O_2 during CdTe deposition limits the intermixing between CdS and CdTe due to sulphur diffusion suppression. This has the effect of reducing the formation of CdS_xTe_{1-x} which is responsible for shifting the bandgap to longer wavelengths in the EQE. These results are in agreement with the reported literature where it was found that O_2 when present during CdTe deposition, forms Cd-O bonds by occupying the tellurium vacancies (V_{Te}) along the grain boundaries. These Cd-O bonds along the grain boundaries, when present, before the subsequent $CdCl_2$ treatment can limit the sulphur diffusion due to low concentration of V_{Te} [22].

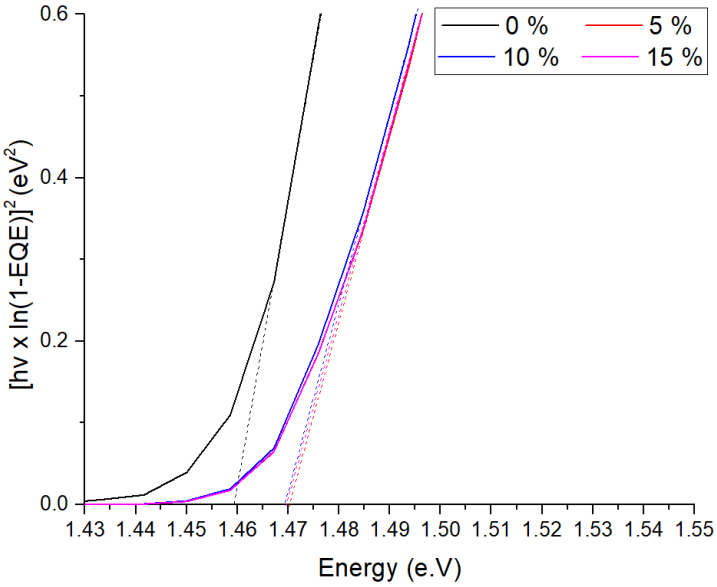

Fig. 3.17: $[E \times ln(1 - EQE)^2]$ *vs energy plots of devices with different* O_2 *- concentrationsduring CSS*

In *Fig 3.18* box plots of the samples with different concentration of O_2 is shown for a) V_{OC}, b) J_{SC}, c) FF and d) efficiency. Comparing the investigated samples, it is evident that O_2 plays a significant role in device performance by increasing all the device parameters and importantly has a significant improvement on the uniformity of the samples. With introduction of O_2, the sublimation procedure becomes more controllable by reducing the CdTe grain size, deposition rate and, most importantly, limits the interdiffusion between CdS and CdTe during the $CdCl_2$ activation treatment. The combination of these effects improves the p-n junction stability by limiting the formation of shunting and localised weak diodes due to pinhole formation and uncontrolled sulphur consumption from the CdS layer.

Comparing just the oxygenated samples, the variation between the electrical characteristics are minor. However, by careful examination, even though a trend can be observed where increase in oxygen leads to better performance for a single device, there is a slight voltage uniformity decrease when comparing across the whole sample, especially for the V_{OC} with increasing concentration level. This can suggest that by introducing large amounts of O_2 during the CSS process it is possible that secondary phases (such as CdO and $CdTeO_3$) can form

which can introduce defects during junction formation and affect the uniformity [21].

In conclusion, in this section the effects of O_2 concentration during CSS of CdTe have been investigated. O_2 incorporation was proven to be beneficial for the performance of CdTe solar cells. When introduced during CdTe sublimation, O_2 was found to act as a nucleation aid leading to a reduction of pinhole formation. Additionally, O_2 provides better process control of the sublimation procedure through CdTe grain reduction which increases homogeneity of CdTe thin films. Finally, O_2 was found to lead in a reduction of sulphur diffusion through grain boundaries preventing total consumption of the CdS layer, which leads to extreme shunting of the device limiting the performance.

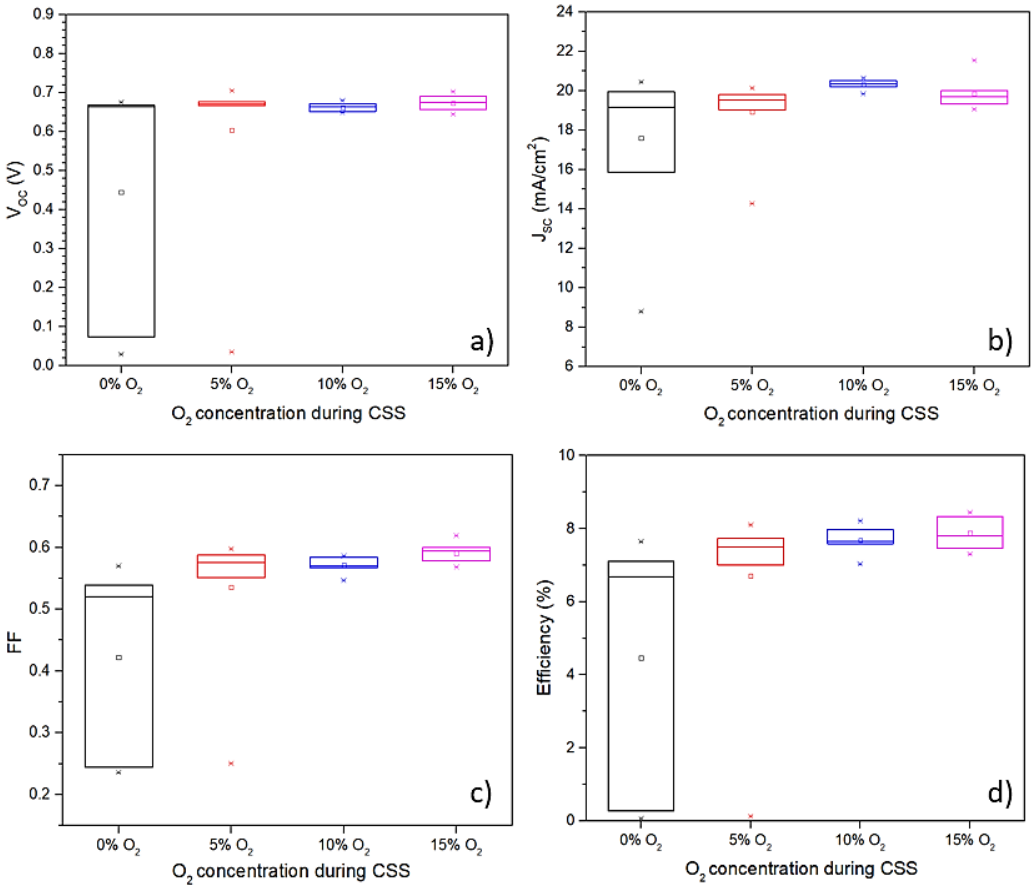

Fig. 3.18: Boxplots of a) V_{OC}, b) J_{SC}, c) FF and d) PCE of samples with different amount of O_2 during CSS.

3.3.3 Cadmium chloride annealing treatment optimisation

As shown in *section 3.3.1*, a CdS/CdTe device which has not received a $CdCl_2$ activation treatment exhibits poor performance with efficiencies of ~ 0.07%. The $CdCl_2$ treatment is an essential step for high efficiency CdTe solar cells, which significantly changes the structural and electrical properties of the film. Briefly, during $CdCl_2$ activation, CdTe films undergo a change in surface morphology, with coalescence of grain boundaries, recrystallization and grain reorientation. Furthermore, during the annealing treatment there is a reduction in optical losses due to junction formation, where S diffuses into the CdTe, forming $CdTe_{1-x}S_x$; while Te diffuses in CdS as $CdS_{1-y}Te_y$ [13]. These ternary compounds shift the bandgap of the device increasing the absorption in longer wavelengths. The $CdCl_2$ activation treatment has been also associated with an increase in p-type conductivity, passivation of interface defects, reduction of planar defect density and change in concentration and distribution of trapping states.

However, the process window for successful implementation for device performance is small. Under-treatment can result in limited device current, while an over-treatment can result in excessive consumption of the CdS layer limiting the device V_{oc} due to shunt paths [23] and possibly leading to blistering and delamination [24].

Electrical performances and material characterisation are generally carried out to assess the effect of $CdCl_2$ treatment. Photoluminescence (PL) imaging is an advanced characterisation technique that can assist device optimisation, allowing each processing stage to be analysed.

In this section, the optimisation of the $CdCl_2$ treatment using PL imaging is investigated. The amount of $CdCl_2$ evaporated on CdTe surfaces was varied. $CdCl_2$ was evaporated from a crucible in the range of 0 - 0.8 grams to evaluate the effect and the homogeneity of the treatment. The performance of the CdTe devices were measured and related to the amount of $CdCl_2$ used. The pixel intensity and distribution on the PL images were also related to the electrical performances.

For this set of experiments CdS was deposited by ultrasonically assisted chemical bath deposition where an ultrasonic probe was used to agitate the bath as presented in *section 3.2.3*. The deposition was carried out for 1 hour in a 70° C preheated bath, resulting in ~100 nm thick CdS films. The CdTe deposition was carried using CSS and the pressure, T_{sub} and T_{Sou} were 1 Torr, 515°C and 630°C respectively. Deposition was carried out using 6% of O_2 in Ar, for 3 minutes.

The $CdCl_2$ treatment was carried out using thermal evaporation at various $CdCl_2$ concentrations. A quartz crucible was filled with 0.2, 0.4, 0.5, 0.6 and 0.8g of $CdCl_2$, which was evaporated at ~$3x10^{-7}$ Torr, until the crucible was empty. The samples were subsequently annealed on a hot plate at a dwell temperature of 425°C, which was held for 1 minute. Devices were completed by depositing ~80 nm of gold using thermal evaporation, as the back contact.

PL imaging was carried out using a home-made system (*Fig. 3.19*). A 405 nm LED was used as the excitation source, with detection of the emitted light using a Si CCD camera fitted with a 720 nm long-pass filter. Exposure time for all of the measured samples was kept to 10 seconds. All measurements were taken at room temperature, with the sample positioned with the glass side of the substrate facing the camera.

During the $CdCl_2$ activation treatment of a complete CdS/CdTe stack, Cl (either in the form of Cl or $CdCl_2$) diffuses through the CdTe layer and eventually reaches the CdS layer. In the CdS layer, diffused Cl is responsible for the formation of sub bandgap V_S-Cl_S and V_{Cd} - Cl_S complexes [25]. These complexes can be detected by PL imaging and the intensity of the PL emission can be used as a qualitative indication of the effectiveness of the $CdCl_2$ treatment. In *Fig. 3.20* a comparison of the PL emission detected for an untreated CdS film and a $CdCl_2$ treated CdS film, both on FTO is shown. 0.2 g of $CdCl_2$ were evaporated on the CdS film and annealed. When a sample is $CdCl_2$ treated, the image appears brighter with higher pixel intensity due to the presence of chlorine in the CdS layer, while an untreated sample exhibits low pixel intensity and the image appears dark. For reference, an untreated CdS

film has an average of 1,000 counts while a treated CdS film has an average pixel intensity of 58,000 counts (*Fig. 3.20)*. A more detailed discussion about PL imaging can be found in *Chapter 4*.

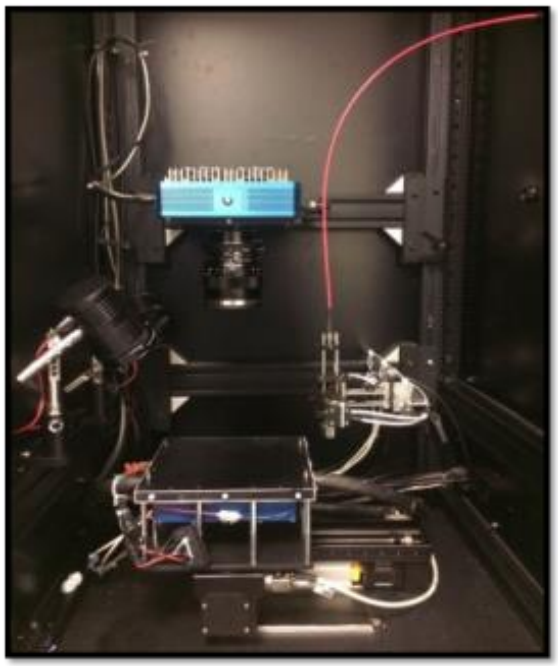

Fig. 3.19: Bespoke PL imaging system used for this work with excitation wavelength of 405 nm and a 720 nm long-pass filter.

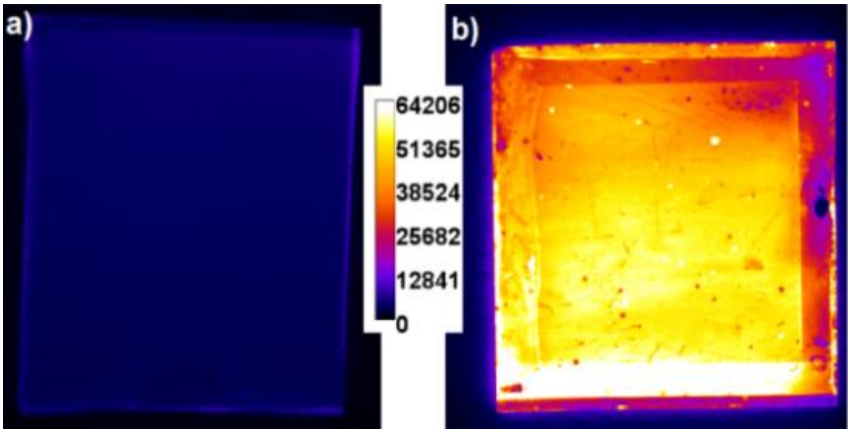

Fig. 3.20: PL image of a) an as-deposited CdS layer and b) $CdCl_2$ treated CdS layer.

Fig. 3.21 shows the J-V curve and the associated PL image of an as deposited device where no $CdCl_2$ treatment has been performed. The performance of this

device is extremely poor, with an average V_{OC} of 370mV and an average J_{SC} of 0.3 mA/cm^2 and FF of 0.48. The average measurements were calculated using 10 cells across each device. PL image analysis also confirmed that the post deposition annealing step performed without the presence of chlorine, had no effect on the device. In fact, low signal intensity was detected with an estimated average of ~1,000 counts. This indicates no presence of Cl in the CdS layer.

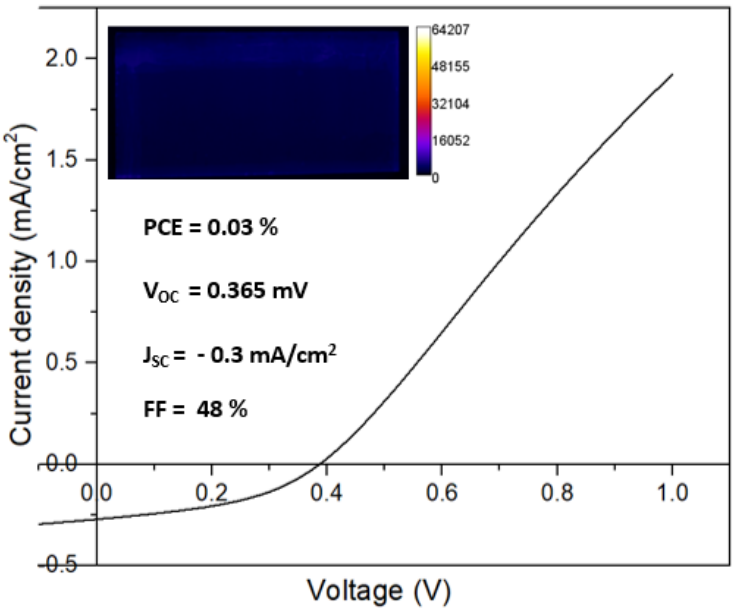

Fig. 3.21: J-V Curve and PL image of an as-deposited CdTe device.

In *Fig. 3.22* the J-V curve and the associated PL image of CdS/CdTe thin film with 0.2 g of evaporated $CdCl_2$ is shown. The average efficiency increased from ~0.03% (when no $CdCl_2$ was added) to 7.2 %, with a V_{OC}, J_{SC} and FF of 727mV, 18.7mA/cm^2 and 0.48, respectively. PL imaging analysis showed an average of ~13,700 counts contrary to the ~1,000 counts detected previously on the samples annealed with no $CdCl_2$. This is because the formation of sub- bandgap complexes due to the diffusion of Cl through the CdTe layer into the CdS layer. 0.4 g results in higher performance devices, with an average efficiency of 7.9 % and a PL intensity ~ 22,240. The optimum device performance was achieved when CdS/CdTe thin films were treated with 0.5 g of evaporated $CdCl_2$ with the device showing the highest average efficiency (8.40%) with a V_{OC}, J_{SC}, and FF of 762 mV, 18.77 mA/cm^2 and 0.59 respectively. *Fig. 3.23* shows the J-V curve

with the associated PL image, with an average emission of 23,300 counts. Further increase in the amount of $CdCl_2$ used in the deposition proved to have a deleterious effect on the performance of the devices. With 0.6 g of evaporated $CdCl_2$, the average V_{OC} significantly decreased to 662 mV while the J_{SC} remained at approximately the same value (18.74 mA/cm^2) and the FF decreased to 0.54. To conclude the study, 0.8 g of $CdCl_2$ was deposited on the CdTe, to identify an over-treated $CdCl_2$ treatment. The performance of this sample was very similar to 0.6 g, with average V_{OC}, J_{SC}, and FF of 661 mV, 18.5 mA/cm^2, and 0.51 respectively. The drop in V_{OC} can be an indication of excessive consumption of sulphur from CdS due to the intermixing between the CdS and CdTe layers during the activation process.

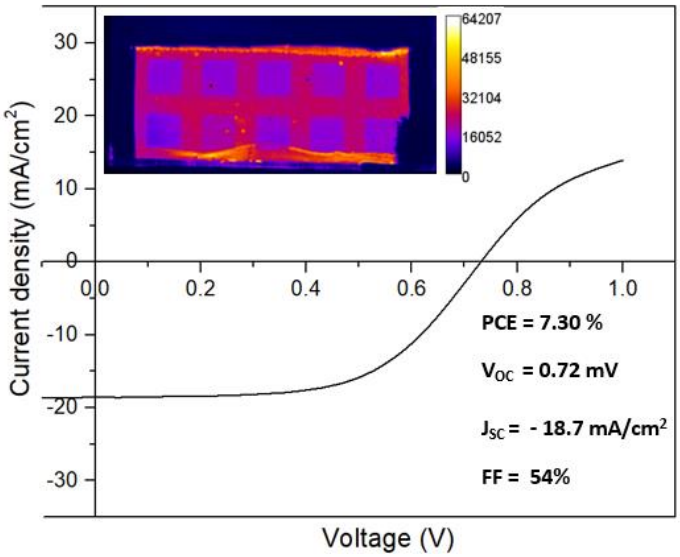

Fig. 3.22: J-V Curve and PL image of a CdTe device with 0.2 g of evaporated $CdCl_2$

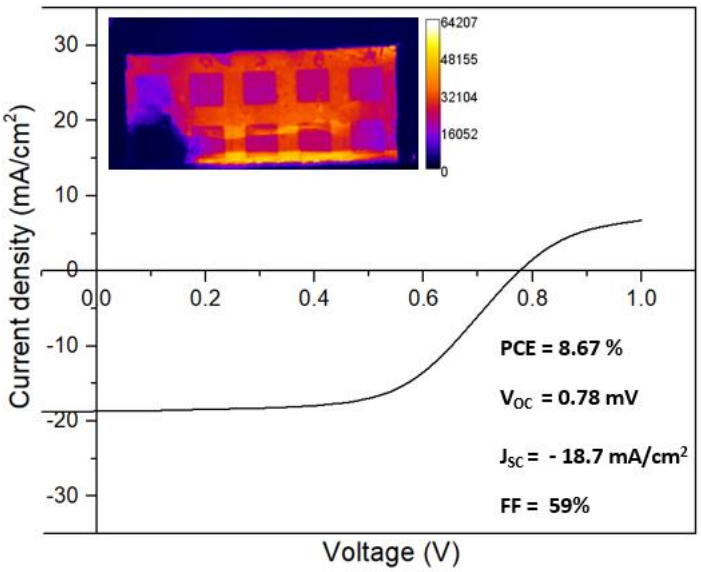

Fig. 3.23: J-V Curve and PL image of a CdTe device with 0.5 g of evaporated $CdCl_2$.

Fig.3.24 shows the clear trend of efficiency with increasing amount of evaporated $CdCl_2$. The figure shows a curvilinear trend where the ascending part represents the progressive increasing amount of the $CdCl_2$ used (starting from 0 g), reaching the highest efficiency at 0.5 g. The descending part of the curve corresponds to the further increase of $CdCl_2$ used, where a harmful effect has been observed on the performances of the CdTe devices. A similar trend was observed in the PL imaging analysis (*Fig. 3.25*) where the optimum performance corresponded to the highest intensity detected. PL imaging was found to be a useful tool which can provide qualitative information about the uniformity and the effectiveness of the $CdCl_2$ treatment on CdS/CdTe devices and is used extensively in Chapter 4.

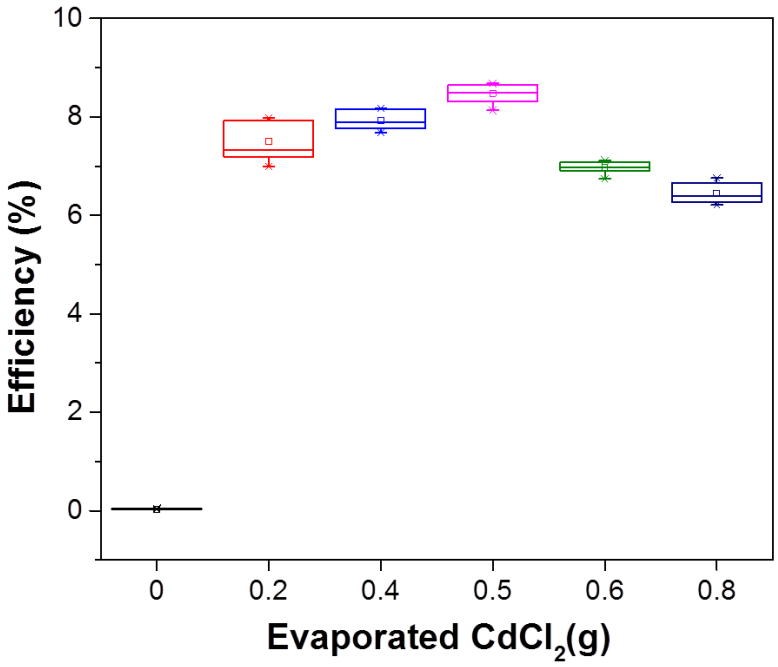

Fig. 3.24: The efficiency trend versus the amount of evaporated $CdCl_2$.

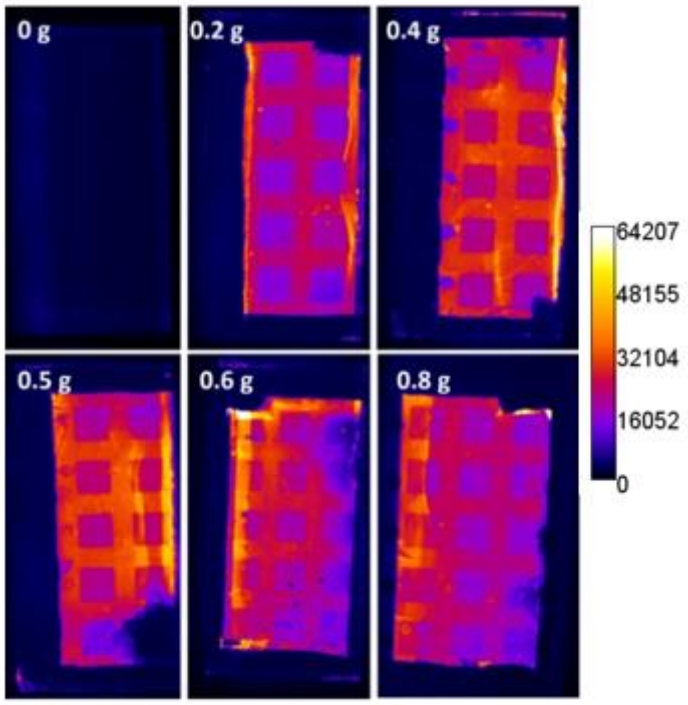

Fig. 3.25: PL images of CdTe devices treated with different amount of evaporated $CdCl_2$

3.4 Concluding remarks

A repeatable baseline process has been realised through individual layer optimisation that can enable further investigation of interface optimisation through comparative studies. The process presented in this chapter was the first baseline process for CdTe solar cells achieved in CREST which was enabled through the design and implementation of a bespoke CSS system (*2.1.4*)

CdTe thin films grown on Eagle XG glass substrates showed a zinc – blend crystal structure highly oriented along the (111) direction, with stoichiometric sublimation of Cd and Te. CdTe deposition followed the Volmer-Weber growth model which includes island formation, island growth and island coalition.

CdTe source preparation showed that compacting and baking the CdTe powder (sintering) as well as etching the source plate's quartz substrate prior to source plate fabrication results in higher sublimation rates and better adhesion of the CdTe for subsequent thin film depositions.

Optimised CdS thin films deposited by chemical bath deposition on TEC 10 substrates have a bandgap of 2.38 eV with a thickness of ~100 nm (for 1-hour deposition).

Device optimisation included introduction of O_2 in Ar during CdTe deposition by CSS, improving the device performance. O_2 was found to lead to a reduction of sulphur diffusion through grain boundaries preventing total consumption of the CdS layer, which leads to extreme shunting of the device. Additionally, it was shown that O_2, when introduced during sublimation, acts as a nucleation aid leading to a reduction of pinhole formation and increased homogeneity providing better process control of the sublimation procedure through CdTe grain size reduction.

$CdCl_2$ activation treatment optimisation showed that the electrical performance is interlinked with the amount of evaporated $CdCl_2$ used during the activation process of the device. A trend was identified in $CdCl_2$ treated devices where the electrical output improved with increasing quantity of evaporated $CdCl_2$ up to an optimal point. However, further increase of evaporated $CdCl_2$ caused a reduction in performance, particularly of the V_{OC}. This is believed to be linked with excessive consumption of the CdS layer leading

to a weaker p-n junction. Furthermore, PL imaging was found to be a useful tool which can provide qualitative information about the uniformity and the effectiveness of the $CdCl_2$ treatment on CdS/CdTe devices. It would be interesting to investigate the role of CdS doping and its effects on interface optimisation and device performance, as well as developing a comprehensive understanding of effects identified with PL imaging.

3.5 References

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Chapter 4. Interface optimisation part A: The emitter/absorber interface

4.1 Introduction

CdTe solar cells depend on various materials, each performing a specific role. During the fabrication process, there are at least four different materials which are used, and consequently, interfaces between these materials are formed. These interfaces can act as recombination centers due to the development of large interface states, which can ultimately limit the device performance.

One of the biggest challenges of CdTe solar cells, as discussed in *Chapter 1* (*1.6.2*), is high interface recombination at the emitter/absorber interface. The lattice mismatch between CdTe and CdS, and the introduction of impurities during junction formation create interface defects inside the junction [1]. These have the potential to act as recombination centers between generated electron-hole pairs and can significantly reduce the V_{OC} and FF of devices.

This chapter aims to identify and investigate possible optimisation processes that could potentially minimise interface recombination. These processes can provide a path to improvement in the performance of CdTe solar cells. The first part of this chapter explores an approach of increasing the doping density of the emitter (CdS) with chlorine compounds during chemical bath deposition. By doping the emitter, the inversion of the absorber can be increased, and interface recombination supressed leading to higher V_{OC} and FF.

The second part identifies and investigates the role of the cooling cycle during the $CdCl_2$ passivation treatment on the performance of CdS/CdTe air activated devices. It was observed that temperature during the $CdCl_2$ activation treatment cooling cycle was linked with the performance and in particular the V_{OC} of devices and could be attributed to interface recombination effects.

4.2 CdTe devices with chlorine doped CBD CdS

One possible way to mitigate interface recombination in any heterojunction device is to cause a large absorber inversion near the interface through band alignment engineering [2][3]. For an absorber to be inverted, the E_F should be close to the conduction band, so the minority carriers collected in the absorber become majority carriers at the CdS/CdTe interface [4]. This effect suppresses interface recombination by a lack of holes recombining with electrons from CdS [5]. As seen from SCAPS 1D simulations in section *1.6.2,* a high emitter doping translates to a high positive charge making the heterojunction less sensitive to interface states.

During CdS/CdTe interface formation, interdiffusion between CdS and CdTe causes the formation of CdS_xTe_{1-x} ternary compound. This interdiffusion process contributes to the reduction of the lattice mismatch between the two semiconductors [6]. This normally occurs during the post-annealing step in the presence of $CdCl_2$, where chlorine (Cl) atoms reach the CdS/CdTe interface via diffusion along the grain boundaries. These can act as donors in the CdS layer, improving the n-type conductivity by shifting the E_F of the CdS closer to the conduction band. Consequently, the V_{OC} of the device improves [7].

Since chlorine causes an improvement in the doping density of the CdS, this work explores the use of Cl containing compounds in the growth of CdS to improve device performance. Cl can act as an n-type dopant when added to the CdS lattice by reducing the amount of compensating cadmium vacancies (V_{Cd}), which can form acceptor centers [8].

$CdCl_2$, when introduced during CdS deposition, creates a neutral complex defect of $(V_{Cd}2Cl_S)^0$ [9]. This complex thermally dissociates to:

$$(V_{Cd}2Cl_S)^0 \leftrightarrow (V_{Cd}Cl_S)^- + Cl_S{}^+$$

During the subsequent CdTe deposition inside the CSS, CdS is subjected to an annealing process. Consequently, $CdCl_2$ evaporates from the CdS crystal structure leaving behind a V_{Cd} and 2 V_S (sulphur vacancies) [8]. Since V_{Cd} is acting as an acceptor and V_S acts as a donor, donors and acceptor centers

neutralise leaving behind a single V_S. This is beneficial for the emitter since V_S can attract residual Cl during the $CdCl_2$ activation treatment forming Cl_S, increasing the carrier concentration.

In this section, the optical, structural and electrical effects of adding $CdCl_2$ during the CdS chemical bath deposition were investigated and associated with device performance.

4.2.1 Methodology

CdS doping with chlorine was carried out by varying the amount of $CdCl_2$ (99.99 % Sigma-Aldrich) inside the bath to act as a dopant after all the other precursors were added according to *section 3.3.2.a*. The concentration of $CdCl_2$ was varied by adding 0.009 g (0.179 mM), 0.36 g (7.14 mM) and 0.65 g (12.89 mM). Because it was not possible to further increase the $CdCl_2$ concentration inside the bath due to precipitation of precursors, which led to non-uniform CdS layers, a CdS thin film without any $CdCl_2$ during CBD was also fabricated which subsequently received a wet $CdCl_2$ treatment. This was done in an effort to overtreat the sample with a high Cl dose. The sample was submerged in a $CdCl_2$ saturated solution of 54.54 mM and received a 425° C anneal for 1 minute to diffuse the dopant from the surface into the film. Deposition for all the CdS films was carried out for 1 hour which resulted in similar thicknesses of ~ 100 nm. CdS deposition parameters of investigated films are summarised in *Table 4.1*. CdTe deposition was carried according to deposition parameters found in *section 3.3.2.a,* T_{Sub}, T_{Source} and separation were kept at 515℃, 630℃ and 2 mm respectively at 1 Torr in a 6% O_2/Ar gas mixture. A final $CdCl_2$ treatment on the entire CdS/CdTe stack was carried out using thermal evaporation of 0.5 g of $CdCl_2$ and subsequently annealed on a hot plate at 425°C for 1 minute. Devices were completed by depositing ~ 84 nm of gold using thermal evaporation, as the back contact and their performance was assessed.

Table 4.1: Summary of deposition parameters of CdS samples with $CdCl_2$ during fabrication

Sample name	*$CdCl_2$ amount in CBD (g)*	*Molarity (mM)*
A	0	-
B	0.009	0.179
C	0.36	7.14
D	0.65	12.89
E	saturated solution	54.54

4.2.2 Results

Effect of Cl in CBD on optical and structural properties of CdS thin films

In *Fig. 4.1.a.* a comparison of the optical transmittance between CdS thin film with different amounts of $CdCl_2$ inside the bath is presented. The investigated samples show very similar transmission curves with minor differences. However, in the range of ~ 320 to 550 nm, the CdS without any $CdCl_2$ inside the bath (sample A), shows higher transmission. Samples with chlorine inside the CdS CBD show less absorption in the range between ~ 620 and ~1000 nm.

In *Fig. 4.1.b*. the Tauc plot of the CdS thin films with and without $CdCl_2$ inside the bath is presented, where $(\alpha h\nu)^2$ is shown as a function of the energy. The CdS without $CdCl_2$ in CBD exhibits a bandgap of 2.38 eV. In comparison, the CdS samples B and C with 0.179 mM and 7.14 mM of $CdCl_2$ during CBD respectively, show a gradual reduction in the bandgap. Sample D (12.89 mM) showed similar E_g with samples B and C thus it was omitted from these figures for simplicity. The reduction of the bandgap with increasing Cl amount during CBD for CdS as deposited films was also observed by Maticius et al [8] and can be attributed to incorporation of hydroxy chloride groups in the CdS lattice. Sample E (54.54 mM) which was annealed to diffuse the $CdCl_2$ exhibits a wider bandgap (2.44 eV) and a sharp absorption edge. This can be attributed to a decrease in defect concentration due to the annealing process in the presence of $CdCl_2$ [10].

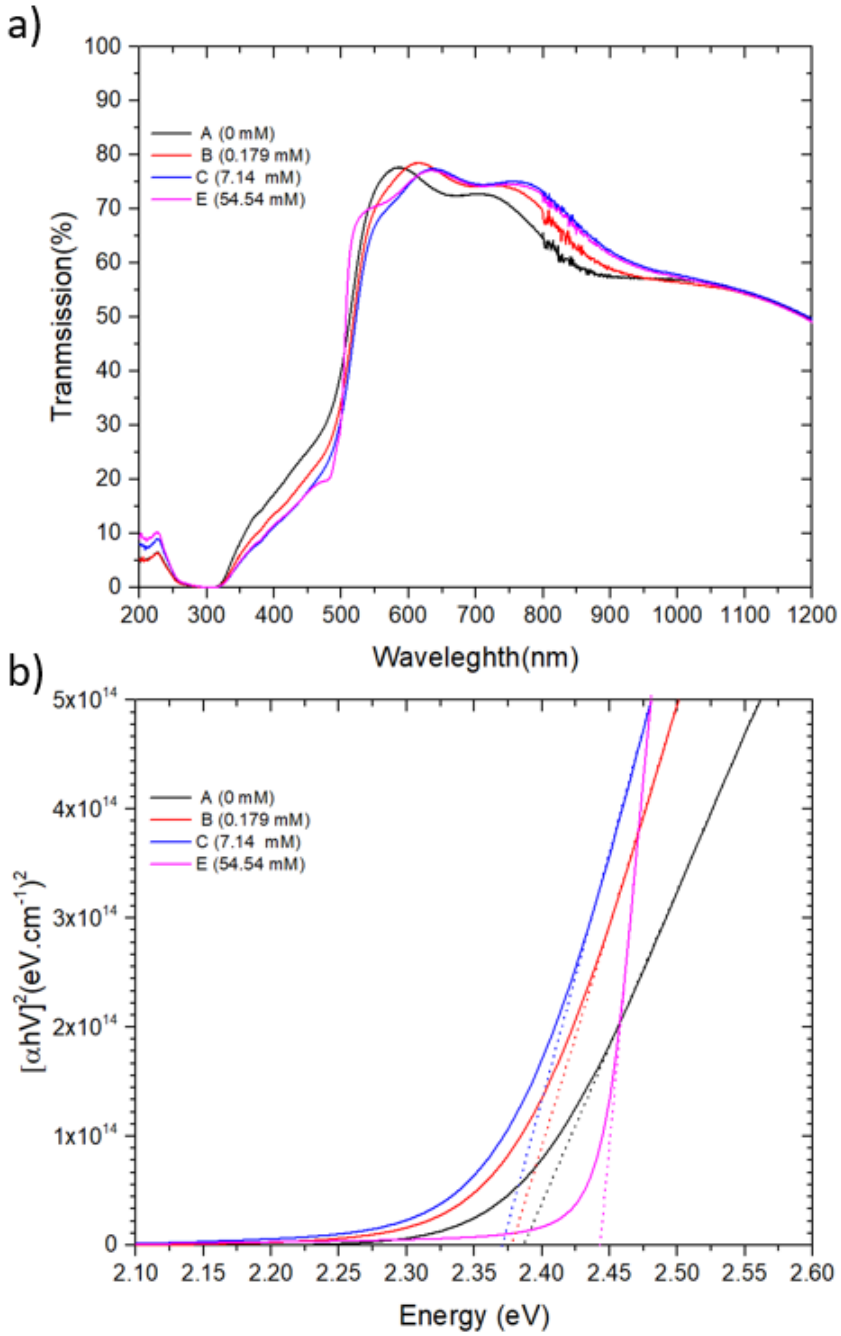

Fig. 4.1: CdS thin films (A, B and C) with 0 mM, 0.179 mM and 7.14 mM of added $CdCl_2$ during CBD, sample E (54.54 mM) was submerged in a $CdCl_2$ saturated solution and subsequently annealed. a) Transmission curves and b) Tauc plot of extrapolated bandgap.

XRD analysis was performed on CdS samples deposited on FTO (TEC 10) because of non-uniform growth on bare glass substrates (*Fig. 4.2*). In *Fig. 4.3* the XRD patterns for the TEC 10 substrate, CdS with 0 mM of $CdCl_2$ during CBD, CdS with 0.179 mM and 54.54 mM of Cl during CBD are illustrated. Unfortunately, the XRD analysis could not show any conclusive results when

comparing the TEC 10, 0 mM and 0.179 mM samples due to smaller thickness of the CdS layers (~ 100 nm) when compared to the TEC 10 substrate and the coincidence between TEC 10 and CdS peaks. However, the sample which has received a $CdCl_2$ annealing treatment with 54.54 mM of $CdCl_2$ showed diffraction patterns at 2θ = 24,3º, 26,4º, 27,8º, 36,64º, 43,7º, and 51,6º where indexed as (1 0 0), (0 0 2), (1 0 1), (1 0 2), (1 1 0) and (2 0 0) planes respectively according to JCPDS Card no. 65-3414. The XRD analysis showed that the diffraction peaks correspond to a hexagonal crystal structure with a preferred orientation along the (002) plane. No peaks were detected in any of the as deposited samples which suggest that Cl incorporation does not affect the crystal structure of the deposited CdS thin films.

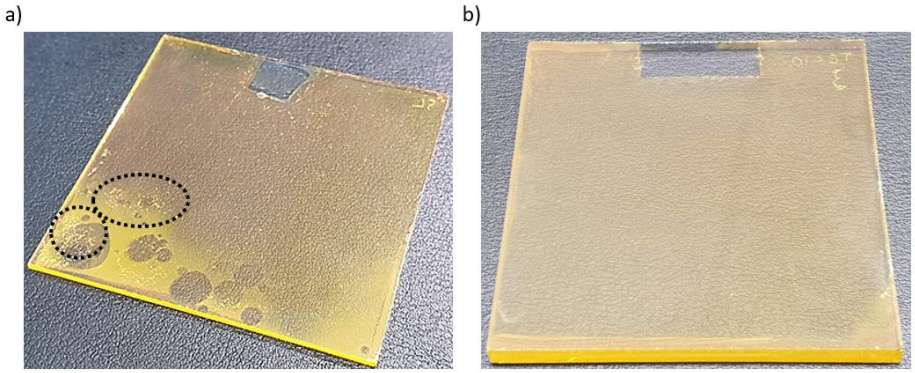

Fig. 4.2: CdS CBD thin film deposition on a) Soda lime glass substrate illustrating the non-uniformity of the CdS thin film, and b) FTO (TEC 10) substrate showing a uniform CdS deposition.

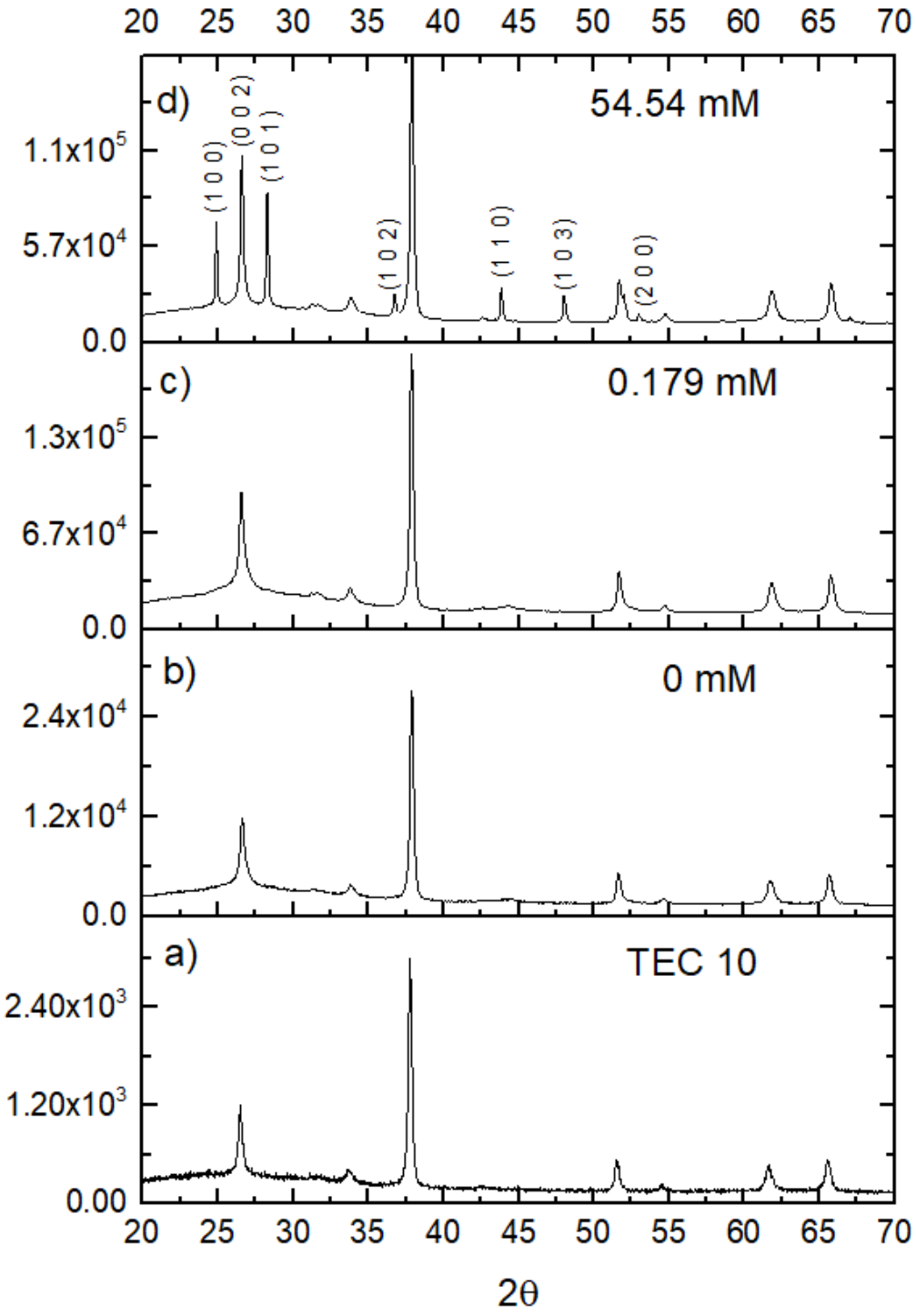

Fig. 4.3: XRD Pattern of a) TEC 10, b) CdS without $CdCl_2$ during CBD and c) CdS with 0.179 mM of $CdCl_2$ (B) during CBD and d) CdS submereged in a $CdCl_2$ saturated solution with 54.54 mM of $CdCl_2$ and subsequently annealed.

Device performance

In *Fig. 4.4* the boxplots of the investigated samples for V_{OC}, J_{SC}, FF and efficiency are shown. Investigated samples showed an average V_{OC} of 760 mV, 790 mV, 800 mV, 810 mV and 730 mV for 0 mM, 0.179 mM, 7.14 mM, 12.89 mM and 54.54 mM respectively. The V_{OC} gradually increased with larger $CdCl_2$ concentration up to 12.89 mM. Sample E (54.54 mM) showed a sharp decrease in average V_{OC} of ~80 mV. However, this sample is not directly comparable due to the different fabrication procedure used (this sample was submerged in a $CdCl_2$ saturated solution and subsequently annealed to diffuse Cl inside the CdS layer).

All investigated samples showed comparable J_{SC} with the average J_{SC} gradually increasing from ~19 mA/cm^2 to ~ 20 mA/cm^2 from 0 mM to 54.54 mM. Sample D (12.89 mM) showed a reduction in average J_{SC} of ~ 0.5 mA/cm^2. This behaviour does not coincide with previous results and further research could be conducted in this direction.

The FF showed a similar trend with open circuit voltage where the average FF gradually increased from 63.5% (0 mM) to 70.7% (12.89 mM) with larger $CdCl_2$ concentration during the CdS CBD. Sample E (54.54 mM) showed an FF reduction of ~ 20%.

Investigated samples showed an average efficiency of 9.3%, 9.7%, 10.4%, 10.1% and 7.6% for 0 mM, 0.179 mM, 7.14 mM, 12.89 mM and 54.54 mM respectively. Average efficiency increased with larger $CdCl_2$ concentration up to 7.14 mM. Sample D (12.89 mM) showed a slight decrease in average efficiency of ~ 0.3% which was attributed to the decrease in J_{SC} mentioned previously

Adding $CdCl_2$ during CdS chemical bath deposition had a positive effect on the V_{OC} and FF of CdS/CdTe devices. Optically, these films show a slight decrease in bandgap which is not translated into a performance loss. Sample E with 54.54 mM showed a dramatic decrease in efficiency (~ 7.3 %). Performing a $CdCl_2$ activation treatment on CdS films prior to CdTe deposition proved to be harmful for the performance of subsequent devices. The over-annealing process could promote the formation of compensating cadmium vacancies (V_{Cd}) which

act as recombination centers, reducing the FF and the V_{OC} of these devices [10]. Additionally, over-annealing could promote the formation of surface oxides, introducing defects inside the junction and reduce the overall performance.

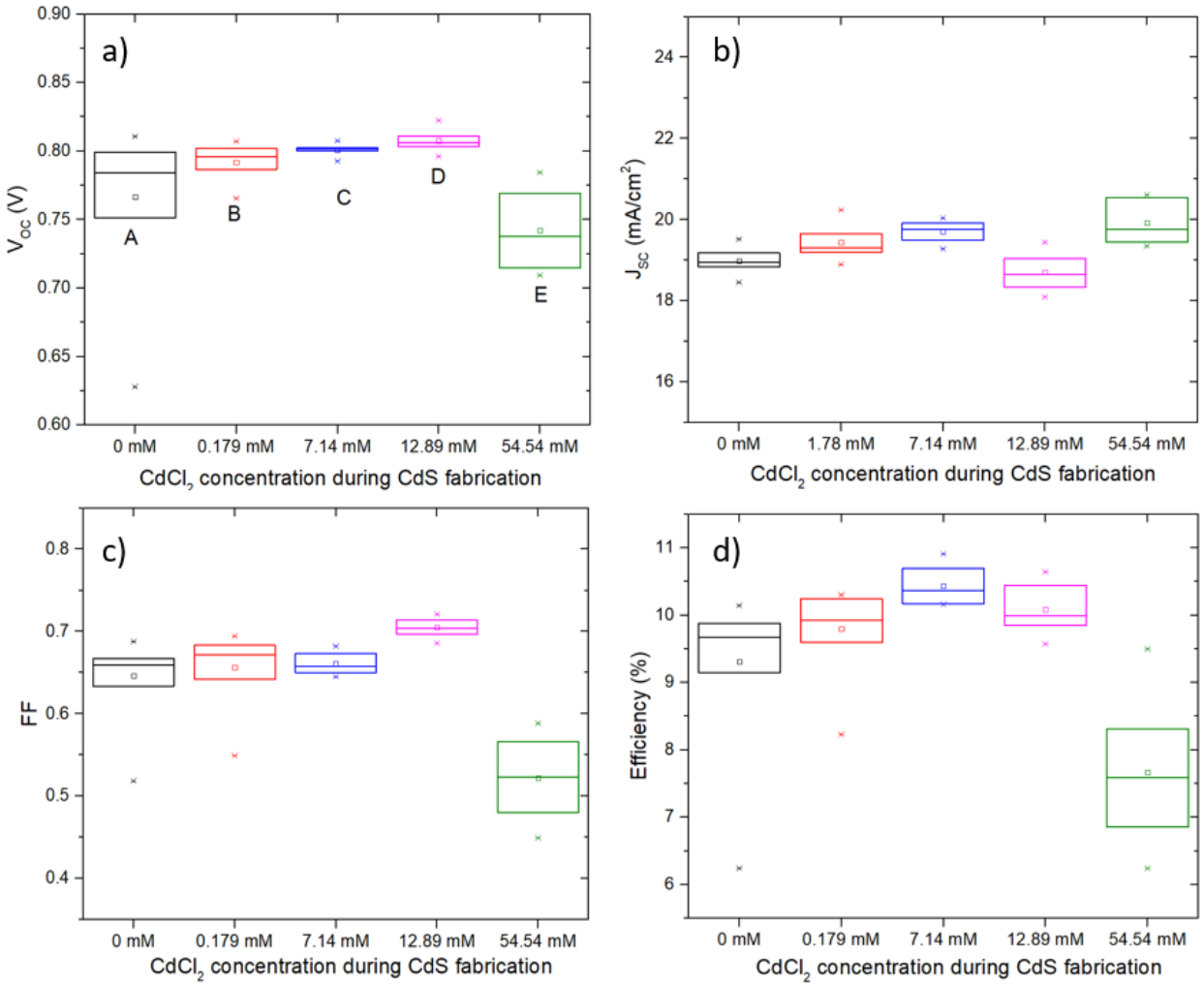

Fig. 4.4: Boxplots of CdS/CdTe devices with different amounts of $CdCl_2$ concentrations during CdS fabrication for a) V_{OC}, b) J_{SC}, c) FF and d) Efficiency. Capital letters A to E represent the CdS deposition parameters according to Table 4.1.

4.2.3 Discussion

During this work, it was not possible to measure the carrier concentrations of CdS thin films using the Hall-effect method because of the high resistivity of the film. Also, Hall measurements require films deposited on insulating

substrates, and in this case, it was difficult to grow CdS on substrates other than FTO coated glass. Doped CdS measurement values are also very sparse in the literature and not easily comparable due to different deposition and doping methods. In an effort to verify the hypothesis of CdS doping with Cl during CBD, SCAPS 1D simulation software was used to vary the emitter carrier concentration and evaluate the effects on V_{OC} and FF. SCAPS is a PV simulation software which can be used to model simplified structures and generate performance information. It is not able to model 2D or 3D behaviour of real devices, however it often used as a useful approximation to understand device behaviour in thin film solar cells [11].

To simulate these effects accurately, a model of the baseline process (0 mM) was constructed and shown in *Fig. 4.5*. The simulation parameters are illustrated in *Table 4.1*. Most of the parameters for this simulation were taken from commonly used values for CdS/CdTe solar cells [11][12]. After the baseline was modelled, the CdS (emitter) carrier concentration was varied from 5 x 10^{15} to 1 x 10^{17} cm^{-3}.

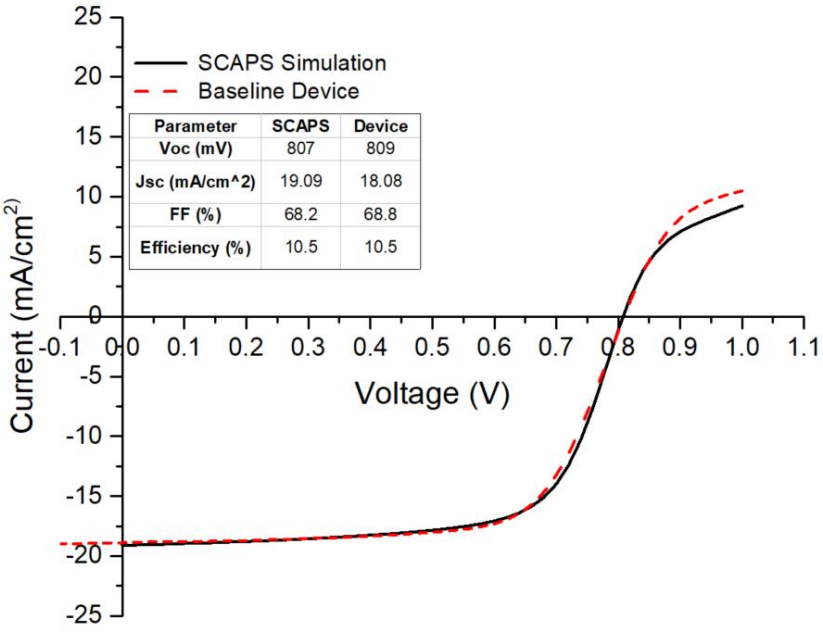

Fig. 4.5: J-V comparison and performance parameters between modelled and baseline device.

Table 4.2: SCAPS 1D model parameters.

Parameter	*Symbol*	*FTO*	*CdS*	*CdTe*
Thickness	x (nm)	400	100	3000
Bandgap	E_g (eV)	3.6	2.4	1.5
Electron Affinity	X (eV)	4.8	4.5	4.4
Dielectric Permittivity	$\varepsilon/\varepsilon_o$	9.0	10	9.4
CB effective density of states	N_c (cm^{-3})	2.2×10^{18}	2.2×10^{18}	8×10^{17}
VB effective density of states	N_V (cm^{-3})	1.8×10^{19}	1.8×10^{19}	1.8×10^{19}
Electron thermal velocity	μ_e (cm^2/Vs)	9	100	320
Hole thermal velocity	μ_h (cm^2/Vs)	25	25	40
Lifetime	T_n, T_p (ns)	0.1	0.1	2
Shallow uniform density	n or p (cm^{-3})	1×10^{20}	5×10^{16}	3×10^{14}
		Defect States		
Total defect density	N_t (cm^{-3})	D: 10^{15}	A:10^{15}	D:10^{13}
Defect energy level	E_t (eV)	midgap	midgap	midgap
Electron capture cross-section	σ_e (cm^2)	1×10^{-12}	1×10^{-13}	2×10^{11}
Hole capture cross-section	σ_h (cm^2)	1×10^{-15}	1×10^{-13}	2×10^{11}
		Interface States		
		CdS/CdTe		
Total defect density	N_t (cm^{-3})	3×10^{13}		
Defect energy level	E_t (eV)	0.4 (above highest E_V)		
Electron capture cross-section	σ_e (cm^2)	9×10^{-15}		
Hole capture cross-section	σ_h (cm^2)	9×10^{-15}		
		Back Contact		
Electron thermionic mission	S_e (cm/s)	10^7		
Hole thermionic mission	S_h (cm/s)	10^7		
Metal work Function	Φ (eV)	5.4		

Fig. 4.6.a shows the simulated results obtained from SCAPS for V_{OC} and FF values as a function of the emitter doping density. V_{OC} is presented with black square points with its corresponding y-axis on the left and the FF with blue triangular points with its corresponding y-axis on the right. The results show that as the emitter doping density increases, there is a steep increase in the V_{OC} up to around ~ 3 x 10^{16} cm^{-3} (voltage increased from ~ 0.6 to ~ 0.8 V). At higher doping densities (> 3 x 10^{16} cm^{-3}) the voltage gradually increases but the increase is very small. Similarly, the FF has a steep increase between 0 and 3 x 10^{16} cm^{-3}. FF improvement at doping densities >3 x 10^{16} cm^{-3} is much more pronounced compared to the V_{OC} improvement. A high emitter doping translates to a high positive charge making the heterojunction less sensitive to interface states [5]. This improves both the V_{OC} and the FF of the device. The V_{OC} however remains relatively unaffected at higher doping densities while the FF continues to improve.

In *Fig. 4.6.b* the average experimental values obtained from the investigated samples for V_{OC} and FF values as a function of $CdCl_2$ concentration during CdS fabrication are illustrated. In this analysis the 54.54 mM device was omitted because of the different fabrication procedures followed during CdS $CdCl_2$ doping and difference in morphology and performance. Only devices where $CdCl_2$ was added during the CdS chemical bath deposition were considered. The results show a similar trend for both the V_{OC} and the FF as observed previously from the simulated analysis. There is a steep increase in voltage from 0 mM of added $CdCl_2$ to 0.179 mM. Further increase of $CdCl_2$ concentrations results in minor V_{OC} improvements (only a few mV). The FF however continuous to improve with increasing $CdCl_2$ concentrations.

These results suggest that addition of Cl compounds during CdS chemical bath deposition can act as a doping mechanism for CdS thin films and enhance the V_{OC} and the FF through reduced interface recombination. This is achieved by reducing the amount of V_{Cd} which usually forms acceptor centers, contributing to self-compensation of carriers inside the CdS. By introducing un-compensating donors such as Cl in the CdS lattice, the E_F shifts towards the conduction band inducing a larger absorber inversion at CdS/CdTe interface

thus minimising interface recombination. Furthermore, addition of $CdCl_2$ during CBD does not change the structural properties of as deposited CdS thin films which remain amorphous.

However, diffusion of $CdCl_2$ inside CdS through post-deposition annealing was found to induce recrystallisation of thin films to a hexagonal crystal structure with a preferred orientation along the (002) plane. The poor performance of these devices could suggest that the over-annealing process could promote the formation of compensating cadmium vacancies (V_{Cd}), or/and promote the formation of surface oxides introducing defects inside the junction, thus increasing interface recombination.

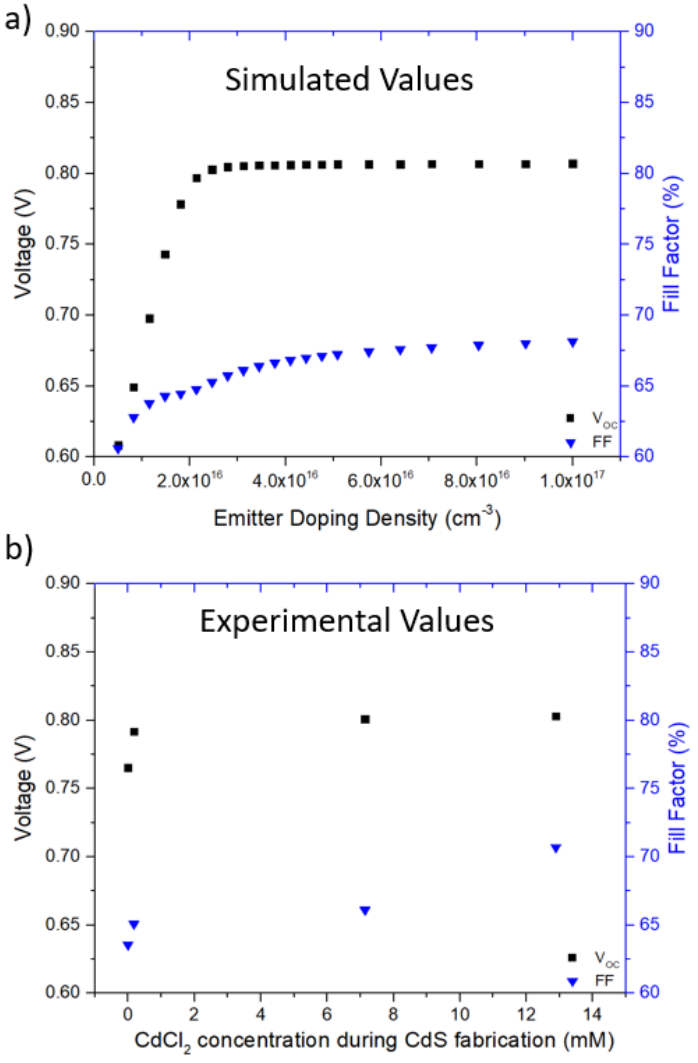

Fig. 4.6: a) Simulated results obtained from SCAPS 1D for V_{OC} and FF values as a function of the emitter doping density and b) the average experimental values obtained from the investigated samples for V_{OC} and FF values as a function of $CdCl_2$ concentration during CdS fabrication (V_{OC} is represented with black squares and FF with blue triangles).

4.3 Effect of cooling cycle during the $CdCl_2$ passivation treatment of CdTe solar cells

As presented in *Chapter 1 and 2*, $CdCl_2$ activation treatment is an essential step for high efficiency CdS/CdTe solar cells. The effectiveness of the $CdCl_2$ activation treatment depends on many factors, nevertheless for cells treated in air this is mainly attributed to precise control of the activation temperature and time [13][14]. In this section the effects of the cooling down temperature during the $CdCl_2$ activation treatment are investigated.

As mentioned in *Chapter 3*, it was important to have a stable and repeatable baseline process, to be able to achieve interface optimisation through comparable studies. *Fig. 4.7* shows the J-V characteristics of two identical samples following the same optimised baseline deposition process presented in *Chapter 3*. Between these months, reproducibility of the baseline process with similar performance was difficult for no apparent reason (nothing has changed in either equipment, materials or deposition parameters of the reference baseline process). This large variation between two identical samples presented a significant obstacle for the continuation of this research. Through a process of elimination, it was suspected that the loss of performance was due to removing the CdTe sample from the hotplate at lower temperatures due to safety concerns (the sample could crack due to thermal mismatch at higher temperatures. The notion that led to this decision was that elevated temperatures are needed (typically ≥ 350 °C) for $CdCl_2$ diffusion through the sample [15][16][17][18]. Based on this, the assumption was that the activation process stops around 350 ℃ during the cooling cycle of the hot plate and removing the sample at lower temperatures should not have any effect on the performance of the device. However, it became clear that this assumption was not valid due to the differing results seen, specifically the V_{OC} showed a remarkable decrease and could be related to interface effects and should be investigated. Therefore, this work aims to identify how the cooling temperature of air activated $CdCl_2$ devices plays a significant role in achieving high performance CdS/CdTe devices and should be considered during the optimisation stages of the fabrication process.

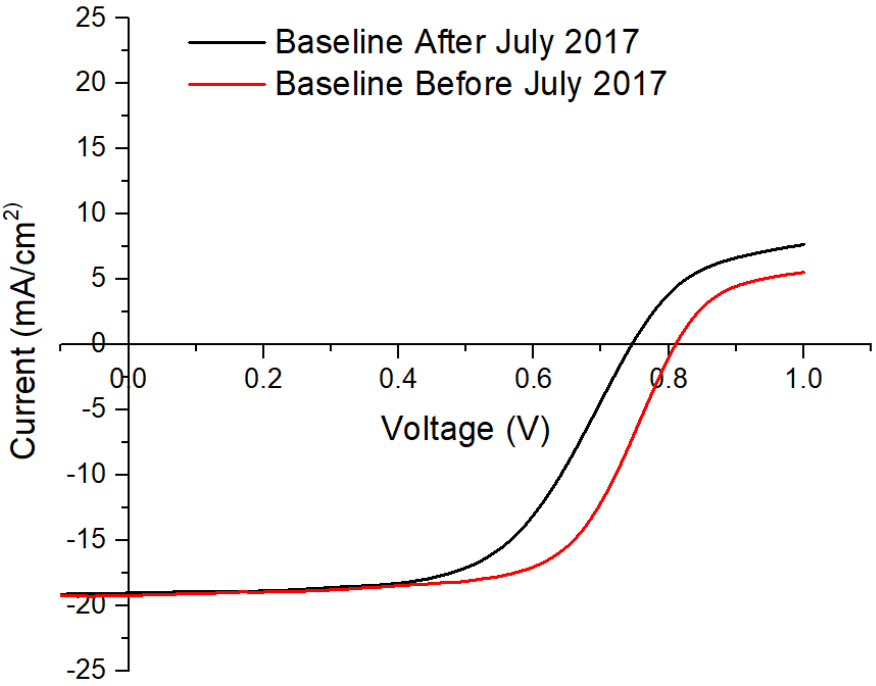

Fig. 4.7: J-V comparison between identical devices before and after July 2017

For this investigation, identical samples were prepared using the baseline process. Each sample however, was removed from the hot plate at a different temperature during the cooling stage of the $CdCl_2$ activation treatment.

CdS was deposited by an ultrasonically assisted chemical bath deposition where an ultrasonic probe was used to agitate the bath as per section *3.2.3.a.* The deposition was carried out for 1 hour in a 70° C preheated bath, resulting in ~100 nm thick CdS films. CdTe deposition was carried according to deposition parameters found in section *3.3.2.a* using CSS. T_{Sub}, T_{Source} and separation were kept at 515°C, 630°C and 2 mm respectively at 1 Torr in a 6% O_2/Ar gas mixture. $CdCl_2$ treatment was carried out using thermal evaporation of 0.5 g of $CdCl_2$ and subsequently annealed on a hot plate at 425°C for 1 minute. Then the hot plate was left to cool down to the required temperature before removing the sample. The cooling down range investigated was from 400°C to 150°C in 50°C steps. After each sample was removed from the hot plate it was placed on a tin foil 'boat' (in air) for 5 minutes to avoid cracking the glass substrate and subsequently received a DI rinse to remove excess $CdCl_2$ from the surface of the

sample. The back-contact deposition was carried out by thermal evaporation. Contact formation was carried out with evaporation of 84 nm of Au.

4.3.1 Results and Discussion

Device Performance

In *Fig. 4.8* the box plots of the investigated samples for V_{OC}, J_{SC}, FF and efficiency as a function of hot plate cool down temperature are shown. Efficiency (*Fig. 4.8.d*) shows a curvilinear trend where the ascending part represents the progressive decrease of the hotplate's cooling down temperature (starting from 400℃), reaching the highest efficiency at 300 ℃ of 10.3 %. The descending part of the curve corresponds to further decrease in the cooling temperature where a detrimental effect is observed on the performance of the devices.

Analysis of each of the performance indicators, showed that the performance decrease is due to the V_{OC} and the FF of these devices, which could suggest interface effects as seen in the previous section (*4.2.3*). While J_{SC} remains unaffected from changes in the cooling down temperature (*Fig. 4.8.a and Fig. 4.8.c*), V_{OC} and FF show the similar curvilinear trend as efficiency. V_{OC} increased from an average of ~ 720 mV to the optimum average of ~ 800 mV when the cooling temperature was decreased from 400 ℃ to 300℃. Further decrease in the hotplate's cooling down temperature to 150℃ caused the V_{OC} to gradually decrease back to an average of ~ 720 mV. Similarly, the FF from an average of ~ 0.55 at 400℃ increased to an average of ~ 0.65 at 300℃ cooling temperature. However, even though the FF shows a gradual decrease after the optimum performance at 300℃, it is worth mentioning that the rate of decline is less pronounced when compared with the V_{OC}. At 150℃, the average FF exhibited is still considerably higher (~ 0.63) than the starting average FF at 400℃ (~ 0.55).

Based on these results, it can be concluded that the performance of air activated $CdCl_2$ solar cells is not affected only by the dwell temperature and time as previously mentioned, but also by the temperature during the cooling cycle of the process A more thorough investigation is presented in the section to identify the possible factors that affect this process.

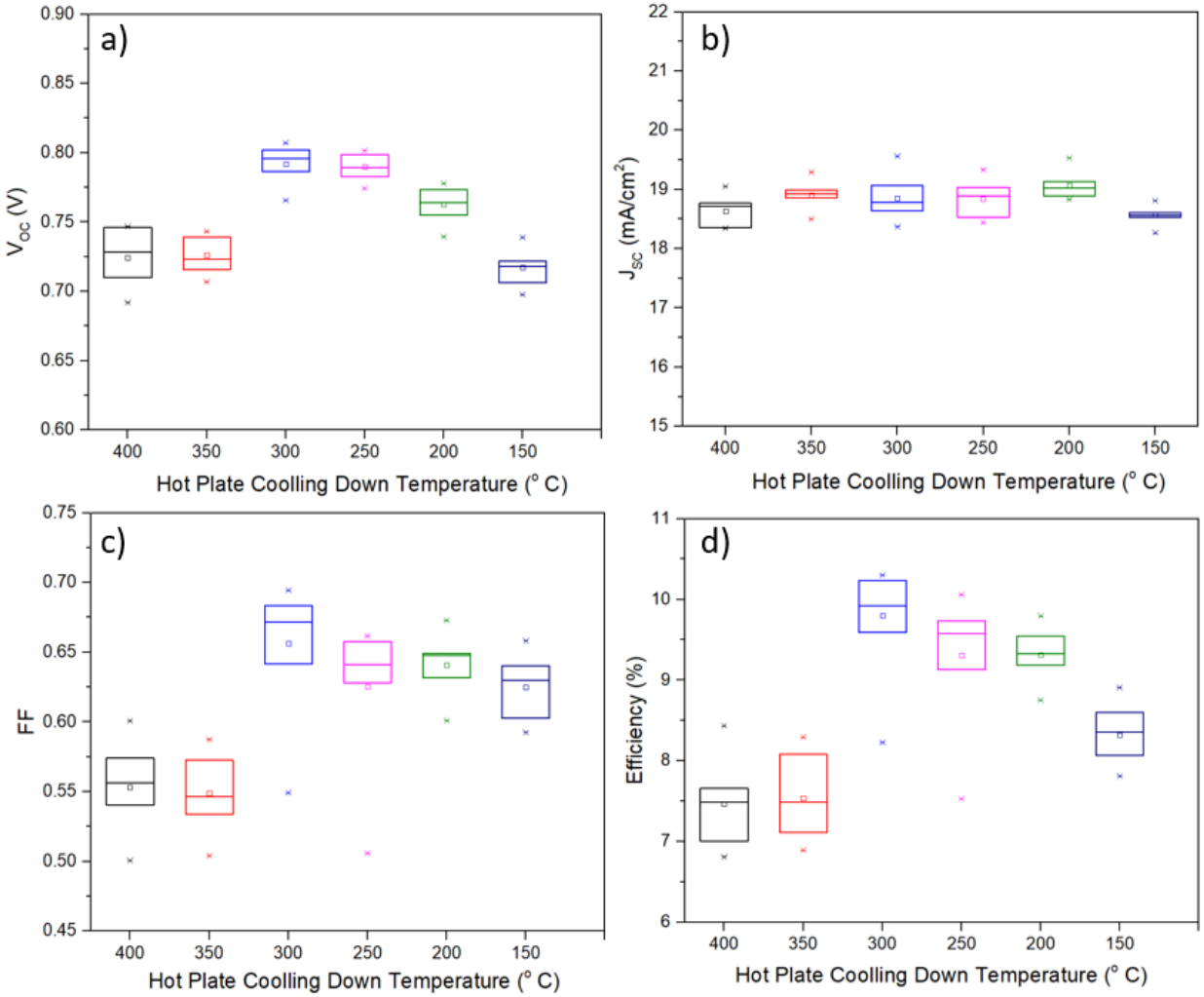

Fig. 4.8: Boxplots of CdS/CdTe devices at removed at different temperature during the $CdCl_2$ passivation treatment cooling cycle.

In *Fig. 4.9* the J-V curves of the best device on each of the investigated samples are illustrated. In *Table. 4.2* a detailed summary for all the performance indicators of these devices can be found. All devices exhibit comparable current densities (18.97 ± 0.36 mA/cm^2) with a variation inside the measurement uncertainty (±1 mA/cm^2) of the solar simulator used for these measurements. Consequently, it can be safely assumed that current density remains unaffected by temperature variations during the cooling cycle of the $CdCl_2$ passivation treatment. V_{OC} and FF on the other hand show large variations according to fluctuations in hot plate cooling temperature with a curvilinear trend.

The sample removed from the hot plate at 400 ℃ shows a V_{OC} of 746 mV and FF of 0.60. Performance remains relatively unaffected when leaving the hot plate to cool down to 350 ℃, with similar results as the sample removed at 400℃. However, at 300℃ hot plate cooling temperature, a spike in both V_{OC} and FF is observed exhibiting an increase to 804 mV and 0.69 respectively. This was the optimum performance achieved through this study. At 250℃, the V_{OC} reduces to 786 mV and FF to 0.67 reducing the overall performance of the device from 10.3 % to 10.0%. Further decreasing the cooling temperature of the hot plate to 150℃ resulted in a gradual decrease of the V_{OC} to 722 mV which is lower than the V_{OC} achieved by removing the sample at 400℃. However, FF does not show the same behaviour as V_{OC} as it exhibits a slower rate of decline than V_{OC}. Consequently, the overall performance of the device removed at 150℃ is higher than the device removed at 400 ℃.

Another observation, hot plate cooling temperature does not only affect the V_{OC} and the FF of the investigated devices but has a pronounced effect on the shape of their J-V curves in forward bias. Generally, it is observed that longer annealing exposure results in a decrease of the roll-over effect present due to the formation of a Schottky barrier at the back contact. This suggests that longer exposure of CdTe' s surface to $CdCl_2$ at moderately elevated temperatures can result in the formation of a tunnelling junction due to moderately doping the CdTe back surface. However, this is out of the scope of this study and further research is needed to draw any significant conclusions.

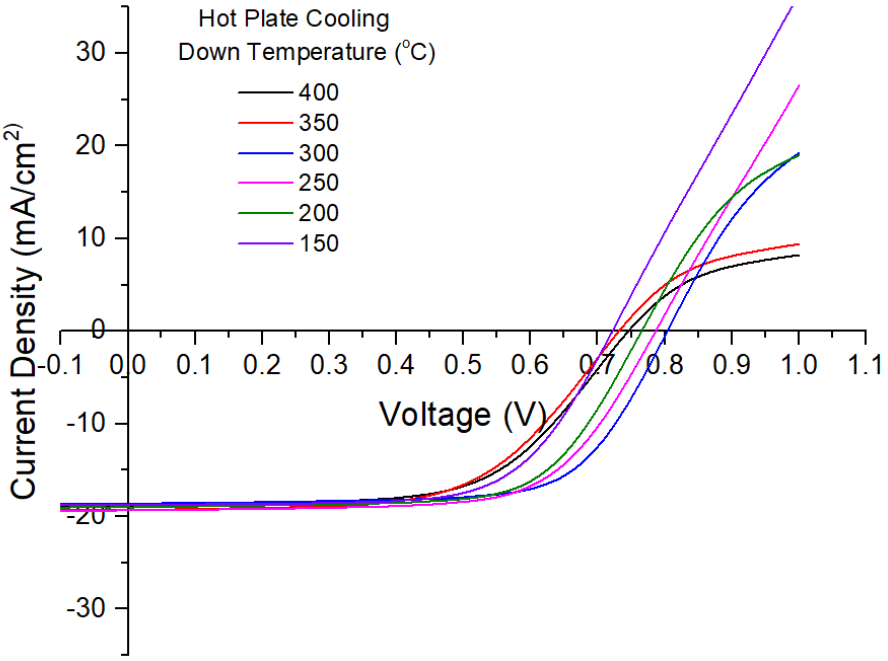

Fig. 4.9: J-V curves of CdS/CdTe devices removed at different temperatures during the $CdCl_2$ passivation treatment cooling cycle.

Table 4.3: Performance parameters of CdS/CdTe best devices removed at different temperature during the $CdCl_2$ passivation treatment cooling cycle

Hotplate Cooling Temperature (℃)	**Voc (mV)**	**Jsc (mA/cm^2)**	**FF**	**Efficiency (%)**
400	746	18.8	0.60	8.4
350	732	19.3	0.59	8.3
300	804	18.6	0.69	10.3
250	786	19.3	0.66	10.0
200	766	19.0	0.67	9.8
150	722	18.7	0.65	8.9

As mentioned in Chapter 1, interface recombination strongly depends on the emitter and absorber doping levels. *Fig. 4.10.a* shows the doping profiles of the investigated devices as a function of the depletion width (W_{CV}) acquired from C-

V measurements. All samples exhibit the same U-shaped carrier profile which is common in CdTe devices and is in accordance with literature [19][20]. The net acceptor densities were determined from the bottom of the U-shaped curve at zero bias. It is generally agreed that for CdTe devices, it is most reliable to extract the doping density at zero bias due to limited response from deep level trap states [20].

In *Fig. 4.10.b* the calculated carrier concentration values are shown as a function of hotplate cooling down temperature. By applying a linear fit, it is possible to identify a trend. In this case there is an observable decrease in net acceptor density inside the absorber as devices are extracted from the hot plate at lower temperatures. This suggests that performance degradation can arise from lower net acceptor densities due to $CdCl_2$ over-treatment. $CdCl_2$ activation treatment is responsible for the formation of a shallow acceptor complex with V_{Cd}, which leads to an increase in doping densities in CdTe devices [21]. However, excess Cl can lead to the formation of Cl_{Te} compensating donors [22]. This effect could explain the decrease in the net acceptor densities which can be directly translated into a V_{OC} loss, as presented previously.

The interpretation of these results proposes that diffusion of Cl does not stop as previously speculated at ~350℃ during the cooling stages of air activated CdTe devices. During the $CdCl_2$ activation it is possible that Cl diffusion continues at much lower temperatures (as low as 150℃). This leads to CdTe forming self-compensating Cl_{Te} reducing the effective net acceptor densities and the V_{OC} decreases.

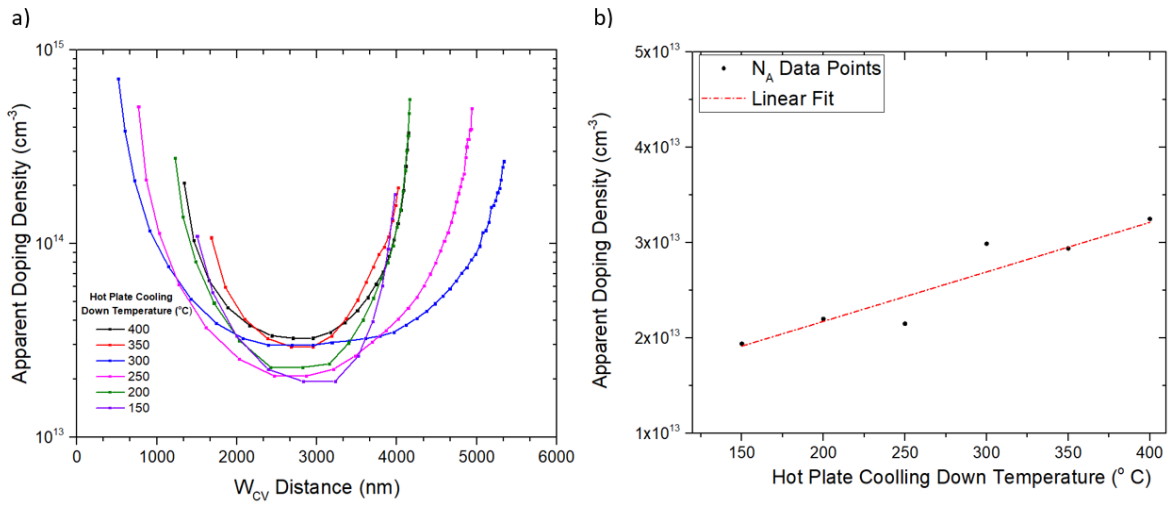

Fig. 4.10: CdS/CdTe devices removed at different temperature during the $CdCl_2$ passivation treatment cooling cycle a) Doping profiles as a function of the depletion width (W_{CV}) and b) Carrier concentration with a linear fit as a function of hotplate cooling temperature.

Fig. 4.11.a shows the spectral response of devices removed from the hot plate at cooling temperatures of 400°C, 300°C, and 150°C for clarity. These devices were selected because they represent the significant points of the curvilinear trend observed of varying performances. All devices exhibit similar spectral response, however the device removed at 400 °C shows marginally lower spectral response in the range between 575 and 625 nm and in the range between 800 and 825 nm. These losses can be attributed to CdS/CdTe incomplete intermixing and enhanced recombination losses respectively.

Fig. 4.11.b shows the bandgap of the investigated devices. The bandgap was calculated by extrapolation of the linear slope to x-axis intercept of the curve of $[E \times \mathrm{Ln}(1 - \mathrm{EQE})^2]$ Vs Energy. All devices exhibit a bandgap in the range of 1.47 to 1.48 eV which is expected for this device structure [17]. Due to the formation of CdS_xTe_{1-x} from interdiffusion of CdS and CdTe during the $CdCl_2$ activation treatment, the bandgap is shifted to longer wavelengths [23]. Devices removed from the hot plate at 400 °C and 300 °C had comparable bandgaps of 1.48 eV, whilst the device removed at 150°C exhibits a reduction in bandgap to 1.47 eV. This suggests enhanced interdiffusion between CdS and CdTe due to excessive exposure to $CdCl_2$ annealing treatment, which results to a more pronounced bandgap shift to longer wavelengths. This indicates that devices which have

been exposed to a longer hotplate cooling cycle show more intermixing between CdS and CdTe.

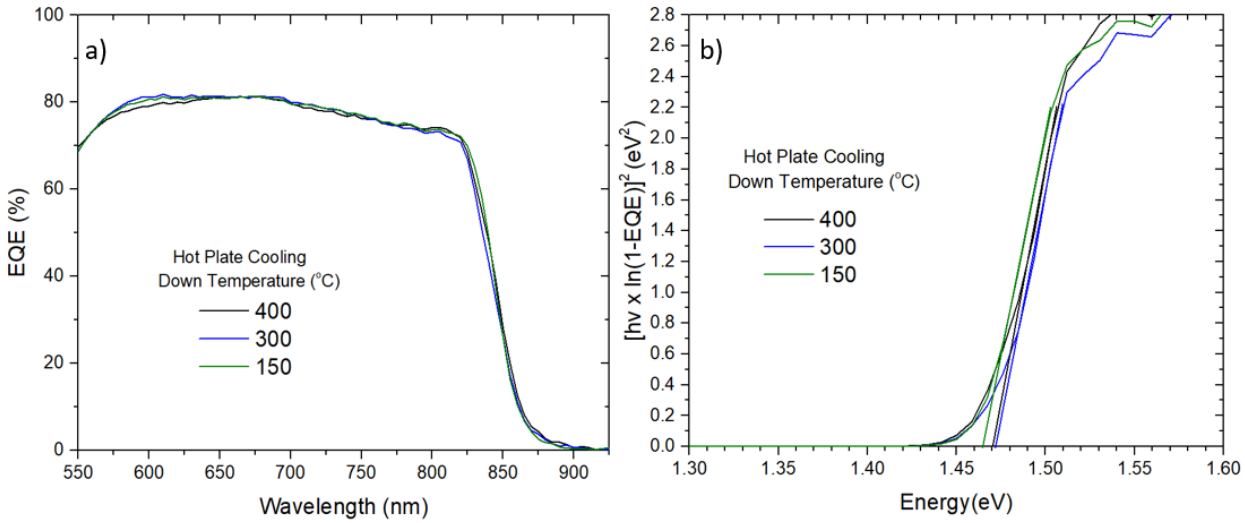

Fig. 4.11: CdS/CdTe devices removed at different temperature during the $CdCl_2$ passivation treatment cooling cycle a) EQE and b) extrapolated bandgap

Due to the small E_g shift from EQE measurements to rule out experimental drift, spectrally-resolved photoluminescence (PL spectra) was carried out with two different excitation sources to verify these values. All measurements were carried out from the glass side of the devices. *Fig. 4.12.a* shows the PL spectra of the investigated samples excited with a 640 nm laser and *Fig. 4.12.b* with a 532 nm. In each case there are two distinctive peaks that can be observed. There is a strong peak at ~ 1.46 eV which is attributed to CdS_xTe_{1-x}, and a shoulder at ~1.5 eV attributed to CdTe [24]. Fitting the peaks revealed comparable results, where the 400℃ and 300℃ devices showed CdS_xTe_{1-x} associated peaks at 1.465 eV and 1.463 eV respectively while the 150℃ device showed a shift to 1.457 eV. This shift could suggest a slight change in composition of the CdS_xTe_{1-x} alloy [25]. For all the measured devices the CdTe peak remained unaffected at 1.50 eV. However, the CdTe shoulder observed at 1.5 eV becomes progressively less noticeable with decreasing hot plate cooling temperature. This is due to a reduction in radiative emission coming from CdTe as more CdSxTe1-x alloy is created with decreasing temperature which becomes the predominant radiative

emission. This effect further supports that there is enhanced interdiffusion between CdS and CdTe with decreasing hotplate cooling temperature.

The interpretation of these results further supports the proposition that the interdiffusion process does not stop as previously speculated at ~ 350℃ during the cooling stages of air activated CdTe devices. During the $CdCl_2$ activation it is possible that the $CdCl_2$ activation process continues at lower temperatures (as low as 150℃) which leads to enhanced interdiffusion between CdS and CdTe. The consumption of CdS during this process can explain the reduction in FF observed at lower cooling down temperatures. This reduction in combination with the reduction in V_{OC} showed earlier, can explain the degraded performance of devices removed at lower cooling down temperatures.

However, while the proposed mechanisms can explain the decrease in performance after the optimum achievable performance at 300℃, they fail to explain the curvilinear nature of performances obtained between 400℃ and 300℃. The 400℃ and 350℃ performances are lower that the optimum performance achieved at 300℃, but these devices exhibit higher doping densities and similar interdiffusion properties with the optimum cooling down temperature. Further analysis of devices process at temperatures between 400 and 300 using PL imaging is shown in the next section to investigate this behaviour.

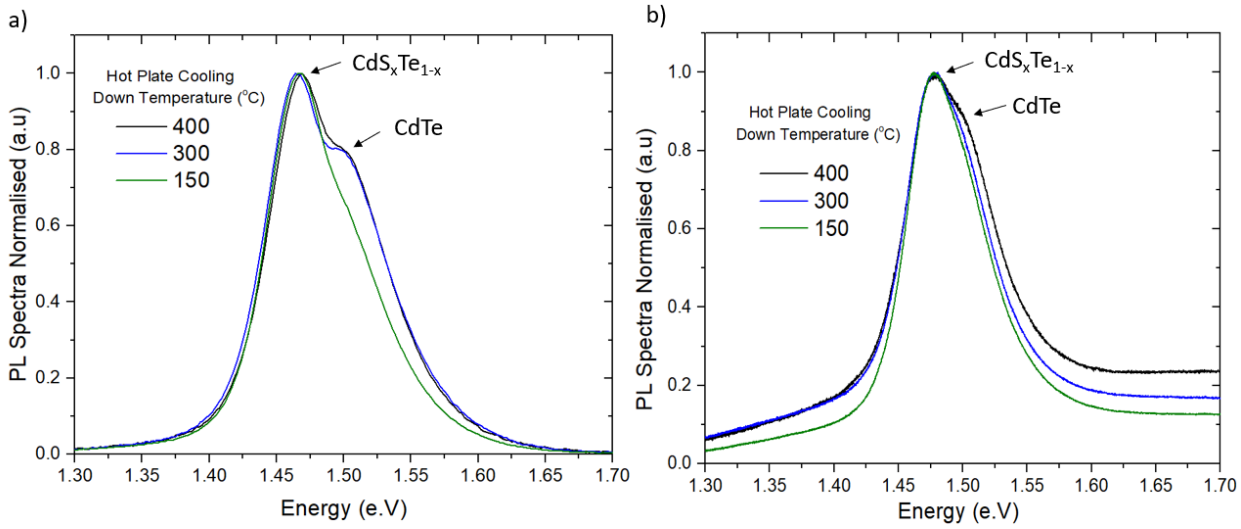

Fig. 4.12: PL Spectra of CdS/CdTe devices removed at different temperature during the $CdCl_2$ passivation treatment cooling cycle with a) Excitation source of 640 nm and b) Excitation source of 532 nm.

Photoluminescence image analysis

PL imaging was carried out using the system shown in *Fig. 4.13*. A 405nm LED was used as the excitation source, with a Si CCD camera fitted with a 720 nm long-pass filter used to detect the PL signal. The exposure time for all the measured samples was kept at 10 seconds. All measurements were taken at room temperature and with the sample positioned with the glass facing the camera.

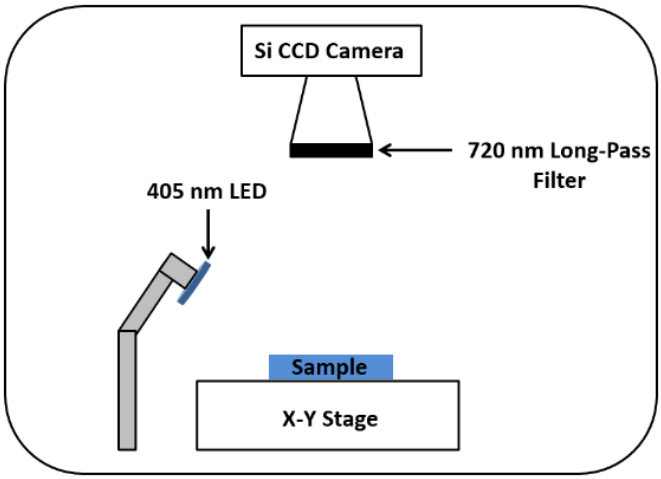

Fig. 4.13: Schematic diagram of PL imaging system

As seen in chapter 3 (*3.3.3*), During the $CdCl_2$ activation treatment, the emission present in the PL imaging, is likely from chlorine containing defects as both sulphur (V_s-Cl_s) and cadmium vacancies (V_{Cd}-Cl_s) in the CdS. This creates a broad PL emission in the range of 1.6-1.8 eV [26] [10]. Chlorine is responsible for the formation of sub bandgap V_s-Cl_s and V_{Cd} - Cl_s complexes in the CdS.

To verify that the signal detected from PL imaging is in fact emitted from chlorine containing defects as both sulphur (V_s-Cl_s) and cadmium vacancies (V_{Cd}-Cl_s) in the CdS, PL spectra was carried out using a 535 nm laser as an excitation source. All samples were excited through the glass at room temperature to be directly comparable with PL imaging.

Fig. 4.14 shows the PL intensity vs energy for a) bare FTO, b) an as deposited CdS film, c) a CdS film that have received a standard $CdCl_2$ annealing

treatment, d) an as deposited CdTe film and e) CdTe film that has received a standard $CdCl_2$ treatment.

It is evident that the broad peak at ~ 1.6 eV is only present in the CdS film which has been subjected to a $CdCl_2$ treatment, while the rest of the investigated samples do not show the same response. The only other sample that shows a significant peak at 1.5 eV (E_g of CdTe) is the CdTe film which has undergone a standard $CdCl_2$ treatment it this was to be expected according to literature [24]. Therefore, it can be safely assumed that the emission detected from PL imaging corresponds to the broad peak at ~1.6 eV detected by PL spectra and arises from the presence of chlorine inside the CdS layer.

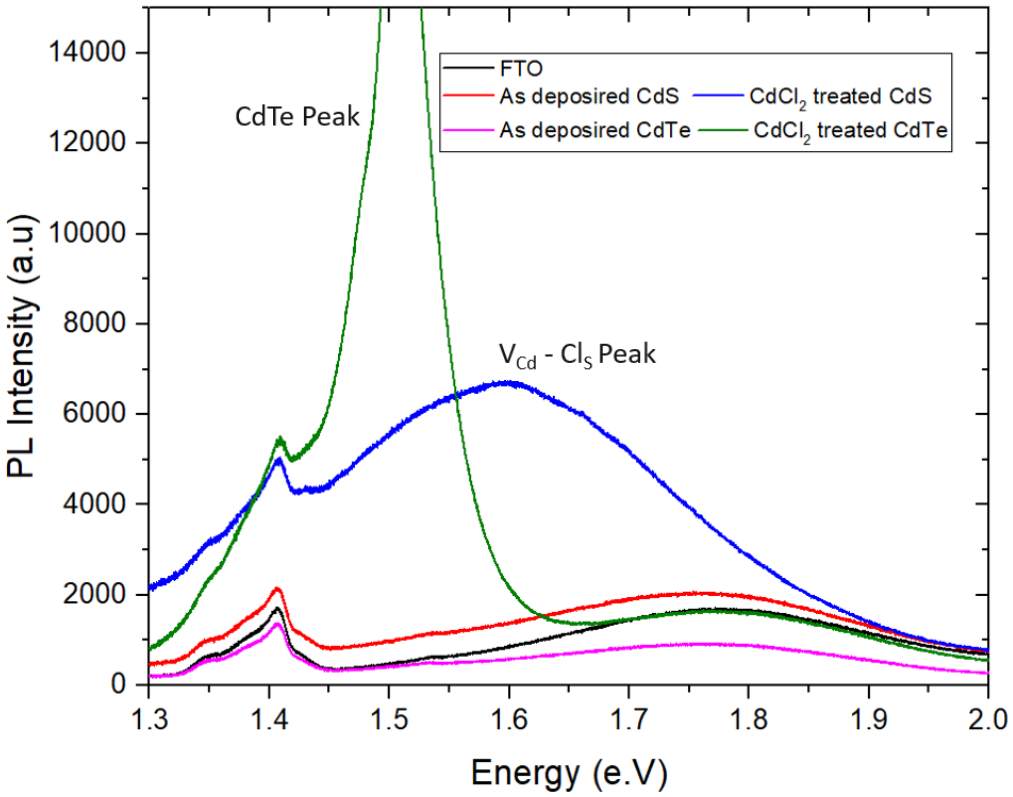

Fig. 4.14: PL spectra analysis of bare FTO substrate, as deposited CdS thin film, $CdCl_2$ treated CdS thin film, as deposited CdTe thin film and $CdCl_2$ treated CdTe thin film

Fig. 4.15.a shows the PL image from CdS/CdTe samples removed from the hot plate at different temperatures during the cooling cycle of the $CdCl_2$ passivation treatment. The average Pl intensity (pixel counts) was calculated by using *ImageJ* image processing software. The figure shows a progressive increase of intensity up to a temperature of ~250℃ where intensity differences

cannot be detected by naked eye. The sample at 400℃ during the $CdCl_2$ annealing treatment cooling cycle showed an average PL intensity ~ 11,976 counts. It is worth mentioning that in this sample it is evident that Cl detected inside the CdS is not uniform. The sides appear brighter than the middle of the sample. Uniformity issues emerge from the fact that there is a thickness variation during CdTe deposition between the sides and the middle of any given sample. Because of this, Cl during the $CdCl_2$ activation treatment diffuses faster from the sides into the CdS and can be detected by PL imaging from the Cl associated complexes.

When the cooling cycle temperature was decreased to 350℃, the average PL intensity counts increased to 24,950. Further decrease of the hot plate cooling temperature resulted in an increase in average intensity counts to 34,189. The maximum intensity counts (36,178) were detected at 250℃ cooling temperature. Further decrease in cooling temperature resulted in a slight decrease in pixel intensity counts to 33,854 and 35,837 for 200℃ and 150℃ respectively.

Fig. 4.15.b shows the average pixel intensity counts as a function of hot plate cooling temperature. By applying an exponential fit to the data points, it was possible to identify a relationship where the average pixel intensity counts increase up to ~250℃, where it then reaches a saturation point of ~35,000 intensity pixel counts.

As previously discussed in *section 4.2,* during the $CdCl_2$ annealing treatment Cl atoms reach the CdS through diffusion along the CdTe grain boundaries. Cl introduction inside the CdS creates the neutral complex of $(V_{Cd}2Cl_S)^0$. This complex can thermally dissociate into the formation of $(V_{Cd}Cl_S)^- + Cl_S^+$ [8][9]. These complexes produce emission at ~1.6 to 1.8 eV and can be used as a qualitative measure of Cl inside the CdS. Through this mechanism, a beneficial situation arises where available V_{Cd} (acceptor centers) are reduced and the doping density of the CdS increases, which can lead to an increase in V_{OC} [8][9].

These results indicate that at higher cooling temperatures, not enough Cl is able to reach the CdS layer. This can lead to a reduced V_{OC} due to the presence of high number of V_{Cd} acceptor centers inside the CdS. This agrees with the electrical characterization seen previously where devices removed at higher

cooling temperatures (400℃ and 350℃) exhibited lower V_{OC}. This mechanism can explain the curvilinear trend identified between 400℃ and 300℃, where while net acceptor densities measured inside the CdTe in these samples appear higher that other devices their performance is limited.

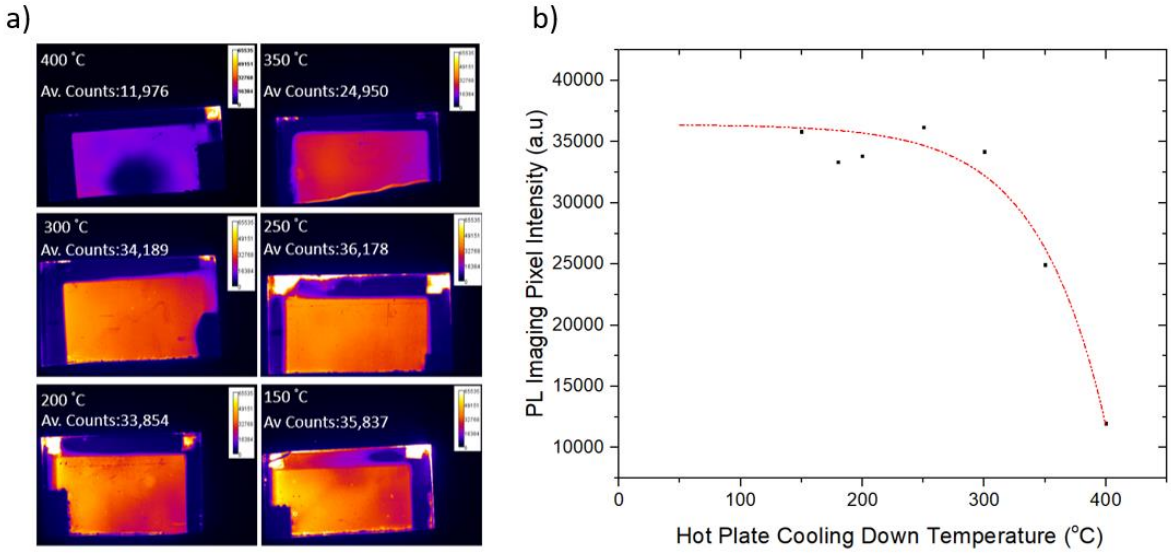

Fig. 4.15: CdS/CdTe devices removed at different temperatures during the $CdCl_2$ passivation treatment cooling cycle a) PL imaging of investigated devices and b) average PL imaging pixel intensity as a function of hot plate cooling temperature with an exponential fit.

Discussion

In this study the optimum temperature range during the cooling cycle of the activation treatment was identified to be between 300℃ and 250℃. Anything above and below this temperature range led to devices with decreased performance. Two mechanisms have been identified which can explain the curvilinear nature of device performances obtained by varying the cooling temperature of the hot plate.

Using PL imaging, it was possible to identify that at high cooling temperatures, not enough Cl is able to reach the CdS layer. This leads to a reduction in V_{OC} due to the presence of high number of V_{Cd} acceptor centers inside the CdS layer. Through this, it was shown that PL imaging is a useful non-contact technique which can qualitatively identify the presence of Cl inside the CdS layer due to formation of $(V_{Cd}Cl_S)^{-} + Cl_S^{+}$ complexes.

From optical and electrical characterisation, it was shown that interdiffusion during the cooling stages of the $CdCl_2$ activation process continues down to temperatures of ~150℃ which leads to excessive consumption of the CdS layer and reduction in the FF. However, the most significant performance degradation mechanism identified for devices removed at lower temperatures than the proposed temperature range, was a reduction of the V_{OC}. This effect was attributed to a decrease in the net acceptor densities. This is probably caused due to excess Cl inside CdTe which leads to the formation of Cl_{Te} compensating donors.

4.4 Concluding remarks

In this chapter two crucial optimisation processes were proposed for CdS/CdTe heterojunction devices that can reduce interface recombination and enhance device performance.

In the first part of this chapter, the effect of adding chlorine during the CdS chemical bath deposition was investigated. It was concluded that addition of Cl compounds such as $CdCl_2$ during CdS chemical bath deposition can act as a doping mechanism for CdS thin films and enhance the V_{OC} and the FF through reduced interface recombination. This is achieved by reducing the amount of available V_{Cd} which usually forms acceptor centers, contributing to self-compensation of carriers inside the CdS. By introducing un-compensating donors such as chlorine in the CdS lattice, the E_F shifts towards the conduction band inducing a larger absorber inversion at CdS/CdTe interface. The optimum $ClCl_2$ concentration during the CdS chemical bath deposition was found to be 7.29 mM which provided an average performance of 10.4%. Optical characterisation showed a slight reduction in the CdS bandgap with increasing $CdCl_2$ concentrations at non-annealed samples. Structural characterisation showed that chlorine does not affect the crystal structure of as deposited CdS thin films. These results were verified through modelling of the baseline process with SCAPS 1D, where similar trends for the V_{OC} and FF were observed with increasing emitter carrier concentration. Since it is possible to dope the CdS with Cl compounds due to S substitution during CBD, group III elements could be used as dopants to substitute the Cd sites during CdS deposition. Preliminary results at CREST, and research from other authors [27][28], showed that Ga and other metallic ions such as Al could potentially be used as effective dopants in CdS thin films.

In the second part of this chapter, the effect of the cooling cycle during the $CdCl_2$ activation treatment was investigated. It was concluded that the cooling cycle strongly affects the formation of self-compensating defects which can lead to recombination of carriers either in CdTe or in CdS. The optimum temperature range during the cooling cycle of the activation treatment was between 300℃ and 250℃. The best performance was 10.3% at 300℃ cooling temperature. Two

mechanisms were proposed to explain the curvilinear nature of device performances obtained by varying the cooling temperature of the hot plate. Through PL imaging it was possible to identify that at high cooling down temperatures, not enough Cl is able to reach the CdS layer. This leads to a reduction in V_{OC} and it can be attributed to the presence of high number of V_{Cd} acceptor centers inside the CdS layer. In this study PL imaging was demonstrated to be a useful non-contact technique which can qualitatively identify the presence of Cl inside the CdS layer due to formation of $(V_{Cd}Cl_S)^-$ + Cl_S^+ complexes. C-V measurements showed that at lower cooling temperatures there is a decrease in the net acceptor densities which cause the degradation of the V_{OC}. This is attributed to excess Cl inside CdTe which leads to the formation of Cl_{Te} compensating donors.

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Chapter 5. Interface optimisation Part B: The window/emitter interface

5.1 Introduction

As already mentioned in Chapter 1 (*1.6.3*), traditionally, CdTe devices employ CdS as their heterojunction partner to form a p-n junction. Through this device structure, it is possible to achieve efficiencies exceeding 16% [1][2][3]. However, the CdS buffer can contribute to current loss at wavelengths below ~ 510 nm due to parasitic absorption of photogenerated carriers [4][5]. Carriers generated inside the CdS cannot be collected due to small lifetimes and strong interface recombination that arise from the lattice mismatch between CdS and CdTe [6].

So far in this thesis any performance improvements achieved in CdS/CdTe devices can be mainly attributed to an increase in V_{OC} and FF whilst J_{SC} remained relatively low (average ~ 20 mA/cm^2) constituting a significant performance limitation. The aim of this chapter is to investigate the effects of the window/emitter interface and minimise photocurrent losses arising from the CdS buffer layer. The first part of this chapter concentrates on the effects of reducing the CdS thickness and the role of the CdS thickness on the CdS/CdTe interdiffusion process. In the second part, the role of high resistive transparent layers (HRT's) is explored and compared with the baseline process. The final part of this chapter identifies the importance of HRT's on interface band alignment and device performance and investigates the complete elimination of the CdS buffer to enhance the photocurrent of CdTe devices.

5.2 Methodology

For all the experiments performed in this chapter, CdTe deposition was carried according to deposition parameters found in *Section 3.3.2.a.* T_{Sub}, T_{Source} and separation were kept at 515°C, 630°C and 2 mm respectively at 1 Torr in a

6% O_2/Ar gas mixture. $CdCl_2$ treatment was carried out using thermal evaporation of 0.5 g of $CdCl_2$ and subsequently annealed on a hot plate at 425°C for 1 minute. Devices were completed by depositing ~ 84 nm of gold using thermal evaporation, as the back contact and their performance was assessed.

Specific details for buffer and window layers in each section of this chapter are outlined in their respective section.

5.3 Effect of CdS thickness on CdTe solar cells

In this section, the effects of reducing the CdS thickness on the CdS/CdTe interface are investigated. Optimisation of the CdS buffer layer is crucial to absorber/emitter interface engineering. The CdS buffer can contribute to current loss at wavelengths below ~ 510 nm due to absorption of photogenerated carriers inside this layer [6]. One way to mitigate this effect is to apply a reduction of the CdS thickness in the solar cell structure. However, this can lead to incomplete coverage of the TCO, having deleterious effects for the device performance. Specifically, the formation of pinholes during CdS deposition can lead to shunt paths or reduction of the V_{OC} due to the formation of localised weak diodes [2]. Recently, it has been argued that even with a thin uniform CdS layer (< 90 nm), there is a considerable FF and V_{OC} degradation [7][8]. Additionally, it has been established that during the $CdCl_2$ annealing, CdS diffuses into the CdTe, forming $CdTe_{1-x}S_x$; while Te diffuses in CdS as $CdS_{1-y}Te_y$ [9][10]. It is possible that interdiffusion can lead to total consumption of CdS from CdTe which can cause the formation of localised shunt paths even if a CdS layer is initially uniform. Nevertheless, the effects of the CdS thickness during CdS/CdTe interdiffusion are not yet completely understood and are further investigated in this section.

5.3.1 Results and Discussion

For this set of experiments, CdS was varied by reducing the CBD deposition time by 15-minute intervals, starting from the baseline process which was comprised of a 1-hour CdS long deposition. The final measured thicknesses of

the CdS deposited samples for 1 hour, 45 minutes and 30 minutes were ~100 nm, ~70 nm and ~50 nm respectively.

In *Fig 5.1* the J-V curves of the best devices from each of the investigated samples with different CdS thickness are presented. As expected, it is observed that reduction of the CdS thickness affects device performance. The device with 1 hour (~ 100 nm) deposited CdS exhibits the best device performance with V_{OC} of 803 mV, J_{SC} of 18.6 mA/cm^2, FF of 0.68 and efficiency of 10.3%. Decreasing the CdS deposition time to 45 min (~ 70 nm), the V_{OC} decreased to 746 mV, FF to 0.61 and efficiency to 8.6%. J_{SC} remained relatively constant at 19.0 mA/cm^2. Further decrease of the CdS thickness to ~ 50 nm (30 min) resulted in the V_{OC}, FF and efficiency to drop to 584 mV, 0.45 and 5.13 % respectively, while current density again remained relatively stable at 19.3 mA/cm^2.

Reducing the CdS thickness did not have the intended outcome of increasing the current density of the device, and it remained relatively unaffected by the thickness reduction of the buffer layer, whereas V_{OC} and FF were found to decrease.

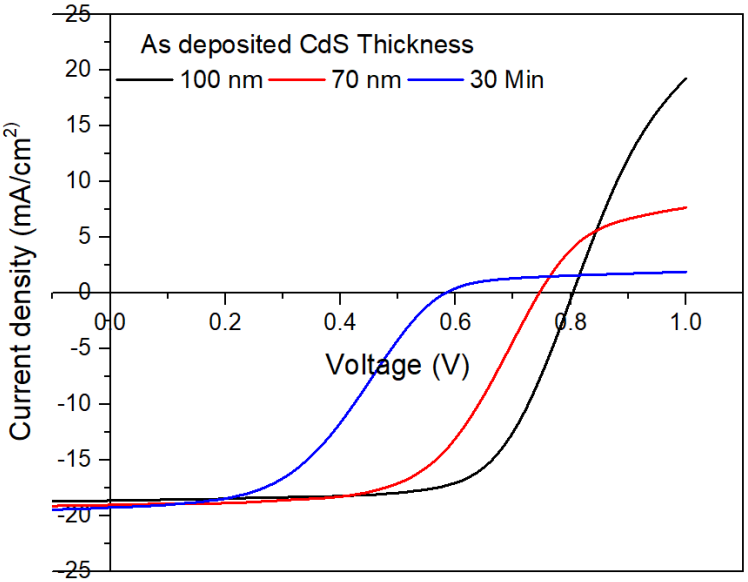

Fig. 5.1: J -V Curves of best devices on each sample with different CdS thickness.

In *Fig. 5.2.a,* the EQE of all three devices is presented. The range between ~ 300 nm and ~ 510 nm in the EQE curve is associated with the optical contribution of the CdS layer. The trend observed in this range is as expected, where by reducing the thickness of the CdS layer, photogenerated carrier losses

inside this range are reduced. This effect should have been translated in a J_{SC} increase. However, it can be observed that while the 50 nm thick CdS device spectrally outperforms in the range associated with the buffer layer, significant spectral losses arise between ~ 510 nm and ~ 900 nm. These can be attributed to enhanced intermixing losses due to increased consumption of the CdS layer from the CdTe (~ 510 nm to ~ 600 nm), resulting in absorption of carriers in CdS_xTe_{1-x}. Comparing the 70 nm and 100 nm CdS devices, it can be observed that the 70 nm thick CdS device exhibits better EQE performance up until ~ 850 nm, whereas the 100 nm CdS thick device's EQE is shifted to longer wavelength. A bandgap analysis (*Fig. 5.2.b*) by plotting $[E \times \ln(1 - EQE)^2]$ Vs Energy, showed a noticeable change of the CdTe bandgap with varying CdS thickness from 50 nm and 75 nm to 100 nm (bandgap shifts from ~ 1.48 eV to 1.47 eV). This shift can be explained by the formation of CdS_xTe_{1-x} which is responsible for shifting the CdTe bandgap in longer wavelengths in the EQE. It was found that, when reducing the CdS thickness there is a decrease of CdS_xTe_{1-x} formation during CdS/CdTe intermixing caused by the lack of sulphur. Consequently, the CdTe bandgap of the devices with thinner CdS buffer layers becomes wider and thus decreases carrier collection.

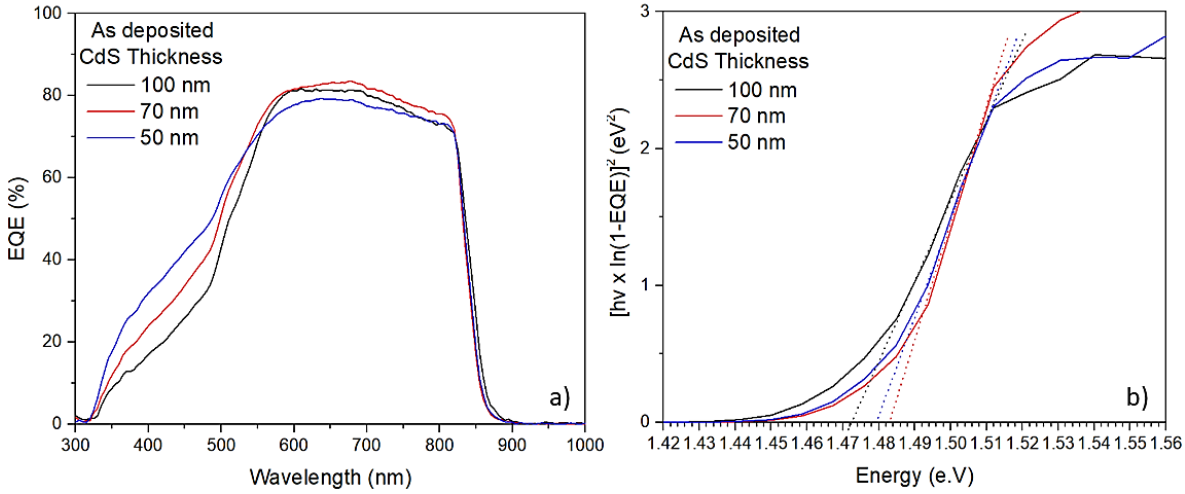

Fig. 5.2: a) EQE responce of best devices on each sample with different CdS thickness and b) Extrapolated bandgap of best devices on each sample with different CdS thickness.

Fig. 5.3 shows the cross-section SEM images of the completed devices with different thickness of the CdS emitter layer. In the 100 nm deposited CdS

device, there is a uniform continuous CdS layer across the CdTe interface and no visible contact between CdTe and the TCO could be identified. The device with the 70 nm deposited CdS no longer exhibits a uniform CdS layer and some localised contact between CdTe and TCO is clearly visible (marked with black arrows). Further reduction in CdS thickness (50 nm) resulted in almost total consumption of the CdS layer with multiple contact points between TCO and CdTe across the interface.

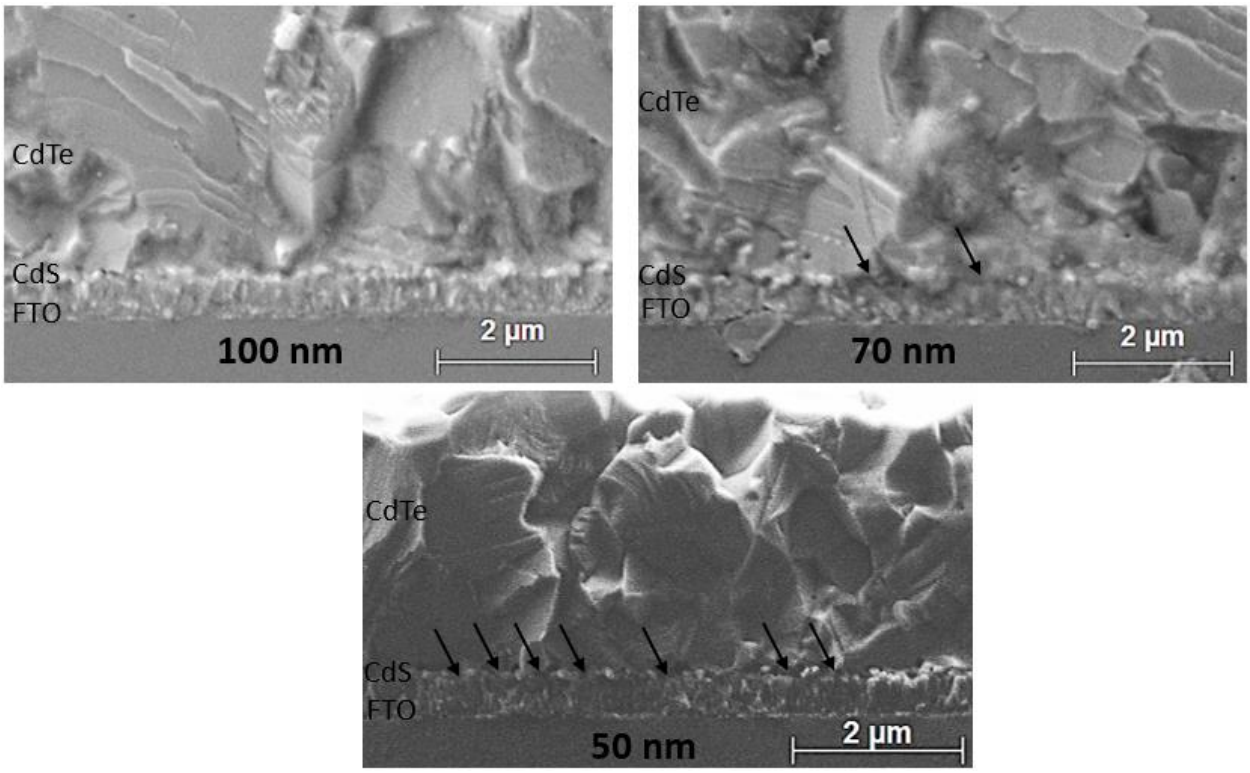

Fig. 5.3: SEM cross-section images of devices with different CdS thickness. The figure shows that reduction of CdS results in the formation of localised contact between CdTe and the TCO.

Discussion

From the EQE and SEM cross section results obtained, the electrical performance of these devices with respect to V_{OC}, FF and J_{SC} can now be explained. Even though reducing the CdS thickness can contribute in minimisation of carrier collection losses inside the CdS buffer layer, losses that arise from improper CdS/CdTe intermixing can mitigate this improvement. This effect results in a small/negligible current density increase in the electrical

performance of the device. However, the V_{OC} and the FF dramatically decrease due to the formation of localised weak diodes and shunt paths from incomplete coverage of the TCO, attributed to consumption of the CdS layer by CdTe. This is caused by the CdS initial limited thickness.

In Fig. 5.4 boxplots of the investigated samples for all the electrical performance indicators are illustrated. These results confirm the analysis previously discussed where CdS thickness reduction decreases the V_{OC} and FF while J_{SC} remains relatively unaffected. Similar detrimental effects on the FF and V_{OC} as a result of reducing the CdS buffer on CdTe devices have been also reported by McCandles and Hegedus [11].

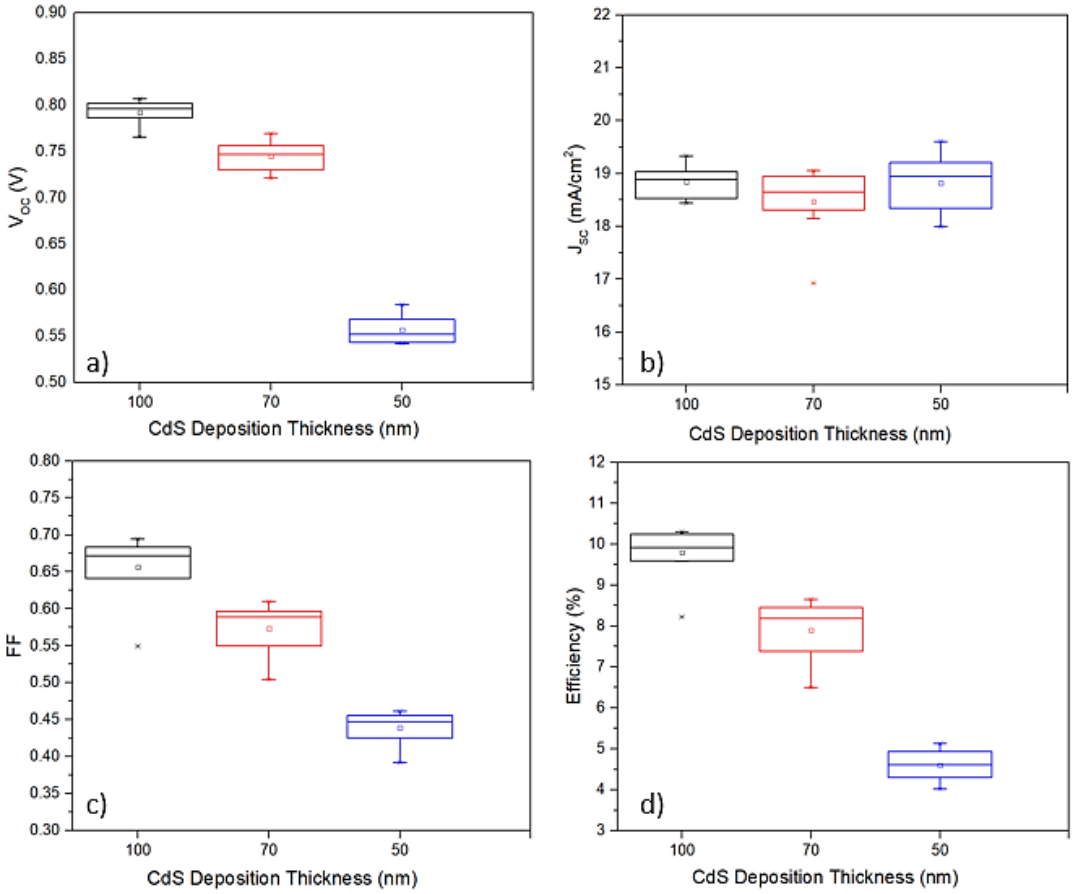

Fig. 5.4: Boxplots of a) V_{OC} and b) J_{SC}, c) FF and d) Efficiency of samples with different thickness of CdS

5.4 Effect of adding a high resistivity transparent layer (HRT)

One way to mitigate the absorption of carriers by the CdS, is to reduce the thickness of the buffer layer. However, to achieve this without the performance limitations identified in section 5.2, a high resistivity transparent layer (HRT) can be utilised between the window layer (FTO) and the buffer layer (CdS). The benefit of adding an HRT layer is generally believed to be the minimisation of the V_{OC} degradation by preventing the formation of localised shunt paths. This allows the CdS to be as thin as possible, hence improving the current density of the device [12].

In this section, the performance effects of adding an HRT layer are investigated on CdS/CdTe solar cells.

For this set of experiments CdS buffer layers were deposited on NSG TEC TM C12D (TEC 12D) glass substrates which include a SnO_2 HRT layer on top of the TCO (SnO_2:F). For comparison, CdS films were also deposited on a standard TEC TM C10 (TEC 10) as per baseline process which does not include the HRT layer.

CdS variation was carried by reducing the deposition time of the CdS thin films during CBD in 15-minute intervals. The final measured thicknesses of the CdS deposited samples for 1 hour, 45 minutes and 30 minutes were ~100 nm, ~70 nm and ~50 nm respectively, for substrates with and without the HRT layer present.

5.4.1 Results and discussion

In *Fig. 5.5* boxplots for all performance indicators between samples with and without an HRT are shown for every CdS thickness variation. Samples without the HRT buffer are represented with a dotted line while samples including the HRT buffer are represented with straight lines.

A comparison of the V_{OC} between the investigated devices is shown in *Fig. 5.5.a*. Initially, for the thickest CdS, which is ~ 100 nm (60-minute deposition), the V_{OC} of the samples with and without the HRT buffer are almost identical

(average of ~ 760 mV). This was expected, since the CdS thickness is adequate to sustain a uniform layer without the formation of micro-shunts and the effect of the HRT buffer appears to be negligible [13]. A reduction of the CdS buffer to 70 nm (45-minute deposition) caused a minor reduction in the voltage of the sample without the HRT buffer. However, there was a substantial increase to an average of ~810mV in the sample with the HRT. This was found to be the optimum thickness for CdS/CdTe devices with an HRT buffer. Further reduction in CdS to ~ 50 nm (30-minute deposition) resulted in extensive deterioration of the V_{OC} in the sample without the HRT to an average of ~ 0.55 mV, while the sample with the HRT showed a reduction of ~ 2 mV.

A comparison of the current densities (*Fig. 5.5.b*) across the investigated samples showed that reducing the CdS on devices without an HRT layer had no effect for reasons which were already explained in section 4.2.1. Investigated samples which included the HRT show an increase in J_{SC} with decreasing CdS thickness as expected [8]. This is also illustrated on the EQE of the samples (Fig. 5.6.b). There is a gradual reduction in spectral losses in the range of 300 to 550 nm with decreasing CdS thickness. This minimises the absorption of photogenerated carriers inside the CdS resulting in higher current densities. However, it is worth mentioning that all the samples which included the HRT showed considerably higher current densities than devices without the HRT at all investigated CdS thicknesses. This effect was attributed to substrate differences. The TEC 10 substrate which the baseline process was optimised on, utilises a 4 mm glass substrate. TEC 12D on the other hand utilises a 3mm glass substrate with lower iron content inside the glass. This affects the transmission properties of the substrate. *Fig. 5.7* shows a comparison of the transmission response between the two substrates with and without the CdS buffer layer which illustrates this effect.

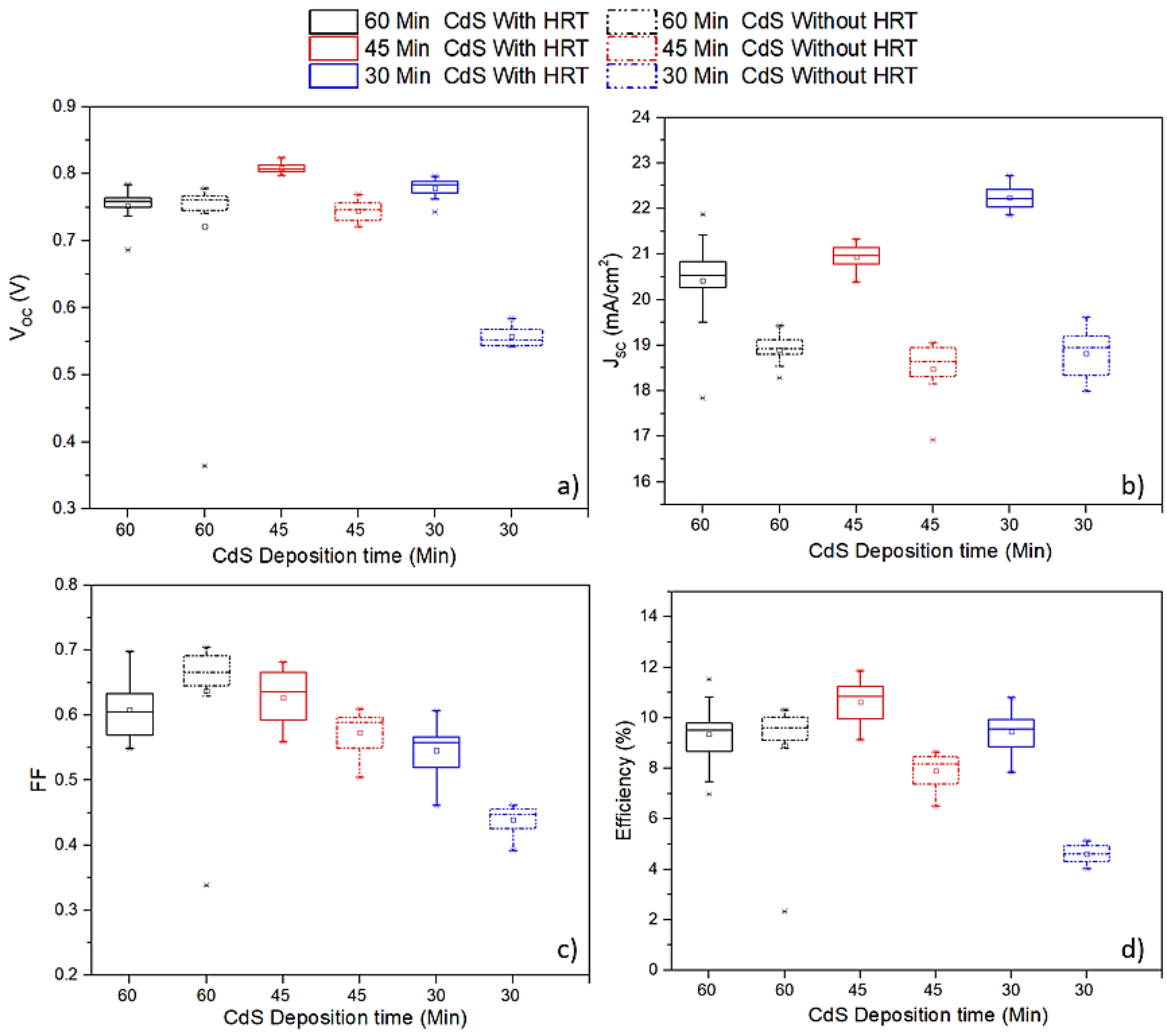

Fig. 5.5: Boxplots of a) V_{OC}, b) J_{SC}, c) FF and d) efficiency of samples with different thickness of CdS with and without an HRT.

Fig. 5.5.c shows a comparison between the FF of the investigated samples. Both samples with and without an HRT show a gradual reduction in FF with decreasing CdS thickness. However, it is observed that degradation in the FF is more pronounced in samples without the HRT layer. Samples investigated without the HRT buffer layer showed a FF reduction of ~24% from thickest to thinnest CdS deposited layer, while devices with the SnO_2 HRT layer exhibited a reduction of ~ 9%. The HRT aids in the prevention of localised weak diodes forming due to insufficient CdS thickness.

In *Fig. 5.5.d* the comparison between the efficiencies of the investigated samples is illustrated. Devices without the SnO_2 HRT layer exhibited a gradual deterioration of performance with decreasing CdS thickness from ~10.8% to

~5.13% (when comparing the best devices on each sample). This is attributed to a deterioration of the V_{OC} and the FF due to the formation of localised shunting to non-uniform coverage of the absorber from the CdS buffer layer. Devices with the SnO_2 HRT exhibited greater performance uniformity with decreasing CdS thickness. Generally, it was found that for these devices there is an inverse relationship between the FF and the J_{SC}. While it is possible to increase the J_{SC}, the reduction in the FF compensates any performance improvements and the samples appear to exhibit similar efficiencies. However, it was possible to achieve efficiencies exceeding 10% at all CdS investigated thicknesses. The optimum device performance was found to be at a CdS thickness of ~ 75 nm (45-minute deposition). This effect is also demonstrated in the J-V characteristics curve of the best devices from each sample (*Fig. 5.6.a*)

In summary, the utilisation of SnO_2 as an HRT buffer allowed the reduction of CdS thin film thicknesses without the formation of weak localised diodes which can limit the V_{OC} and FF of CdS/CdTe devices. Devices with efficiencies of ~ 12% were achieved through increase in current densities. However, even with the thickness reduction achieved, the CdS buffer still presents a significant loss of photogenerated carriers limiting the device performance. Thus, in the following section alternative buffer layers for CdTe solar cells are investigated.

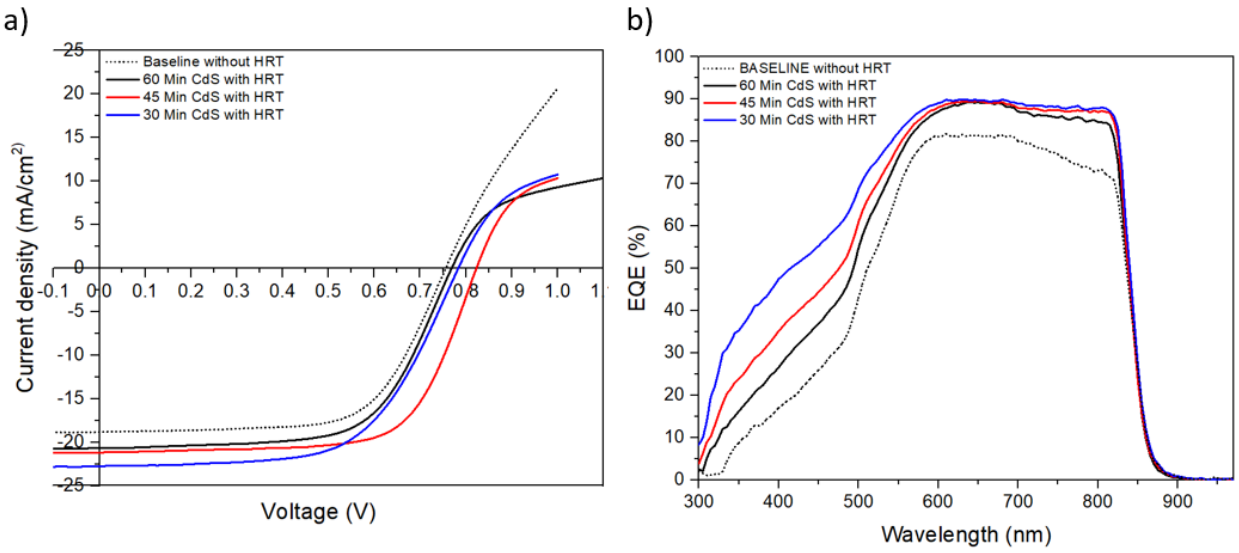

Fig. 5.6: a) J-V curves of best devices with HRT with different CdS thickness and b) Spectral response of best devices with HRT with different CdS thickness. Straight lines represent devices with the HRT and the dotted line represent the baseline process.

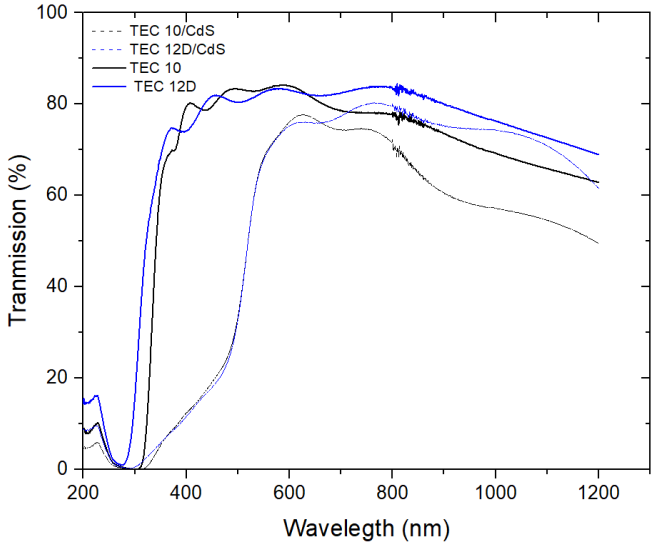

Fig. 5.7: Transmission curves comparison between TEC10 and TEC 12D substrates with and without the CdS layer.

5.5 CdTe devices without the CdS buffer layer

Currently the CdS buffer layer constitutes one of the biggest loss in photocurrent due to absorption of photogenerated carriers at wavelengths below ~ 510 nm. In the previous section it was possible to limit this effect by the addition of a high transparent resistive layer (HRT), which allowed the reduction of the CdS buffer, and thus achieving higher performing devices. While this structure proved to be beneficial for the performance and lessen the deleterious effects arising from CdS absorption, it fails to eradicate the problem.

Wider bandgap materials such as ZnMgO have recently been proven to be effective as buffer layers for CdTe devices and prominent candidates for replacing CdS. These materials allow a larger fraction of the solar spectrum to reach the CdTe absorber, and thus increasing the photocurrent of the device [14][15].

In this section HRT layers are explored as replacements of the standard CdS buffer layer for CdTe devices.

5.5.1 Results and discussion

For this set of experiments, prior to deposition of thin films, substrates were cleaned as previously described in Chapter 3. ZnO and SnO_2 films were deposited on NSG TEC TM C10X (TEC 10X) glass substrates using an Orion 8 HV magnetron sputtering system (AJA international, USA) equipped with an AJA 600 series RF power supply. The purity for both SnO and ZnO targets was 99.99%. ZnO films were deposited in 1% O_2 to Ar environment while SnO films in a 22% O_2 to Ar environment. The pressure and rotation for all deposited films was kept at 1 mTorr and 10 rpm respectively. Deposition time was kept at 15 minutes for all deposited films which resulted in ~ 150 nm thick films. For comparison, CdTe films were also deposited on a (SnO:F) TEC TM C10X which does not include an HRT layer and on NSG TEC TM C12D (TEC 12D) glass substrates which include a SnO_2 HRT layer on top of the TCO. Additionally, a CdTe film was deposited on a CdS film as per baseline process

In *Fig. 5.8* boxplots summarising the performance of the investigated samples are shown. The comparison shows the various alternative thin film layers used as buffers (Samples A to D) contrary to the standard baseline structure. The structure of the investigated samples is as follows, with the acting buffer layer of each structure underlined.

- Baseline: FTO/***CdS***/CdTe/Au
- Sample A: ***FTO***/CdTe/Au
- Sample B: FTO/***SnO_2*** (TEC 12D)/CdTe/Au
- Sample C: FTO/***SnO_2*** (RF sputtered)/CdTe/Au
- Sample D: FTO/***ZnO*** (RF sputtered)/CdTe/Au

Fig. 5.8.a shows the V_{OC} of the investigated samples. The baseline process exhibits the highest V_{OC} with an average of ~800 mV. Sample A showed the lowest V_{OC} of an average of 300 mV. This low V_{OC} behaviour was previously observed [16] for devices with FTO/CdTe junction. Introduction of the SnO_2 layer on top of the FTO (samples B and C) had a positive effect on the V_{OC} when compared to sample A. Sample B exhibited an average V_{OC} increase of ~ 350 mV, while sample C exhibited an increase of ~ 100 mV. However, there is a discrepancy between V_{OC} performance of sample A and B which both included a SnO_2 buffer layer but from different sources. Sample D (ZnO buffer) exhibited an average V_{OC} of 750 mV, the closest V_{OC} achieved when compared with the baseline process.

In *Fig. 5.8.b* the J_{SC} of the investigated samples is illustrated. As expected, all samples without the CdS buffer layer exhibit higher current density than the baseline structure which showed an average current density of ~ 20.5 mA/cm^2. Sample A exhibited an average increase in current density of ~ 12%. Introducing a SnO_2 layer (samples B and C) resulted in a further ~2% increase in current density. Sample D (ZnO buffer) exhibited the average highest current density (~ 25 mA/cm^2) which is a total of 21% increase when compared to the baseline process which includes the CdS buffer layer.

The FF of the investigated samples with different buffer layers is showed in *Fig. 5.8.c*. FF are considerably lower for all the investigated samples with alternative buffer layers. The baseline process exhibited an average FF of ~ 65%, while sample A had an average FF of 50%. Samples inclusive of a SnO_2 buffers (B and C) showed an average increase in FF of ~ 2 % and ~5%. Sample D (ZnO buffer) exhibited an average FF of 55%.

The efficiency of the investigated samples is displayed in Fig. 5.8.d. The average efficiency of the baseline process was found to be ~ 10.5%. Sample A (no buffer layer) exhibited a poor efficiency of ~ 3.5%. The most influential contributor towards low efficiency was determined to be the low V_{OC}. Sample B which included a SnO_2 buffer (supplied by NSG) showed an average efficiency of ~8%, while sample C (RF sputtered SnO) showed an average efficiency of ~ 6%. Sample D (ZnO) buffer layer exhibited the best overall performance with an average efficiency of ~ 11% leading to ZnO buffer layers being the best candidate of replacing CdS buffer for CdTe devices.

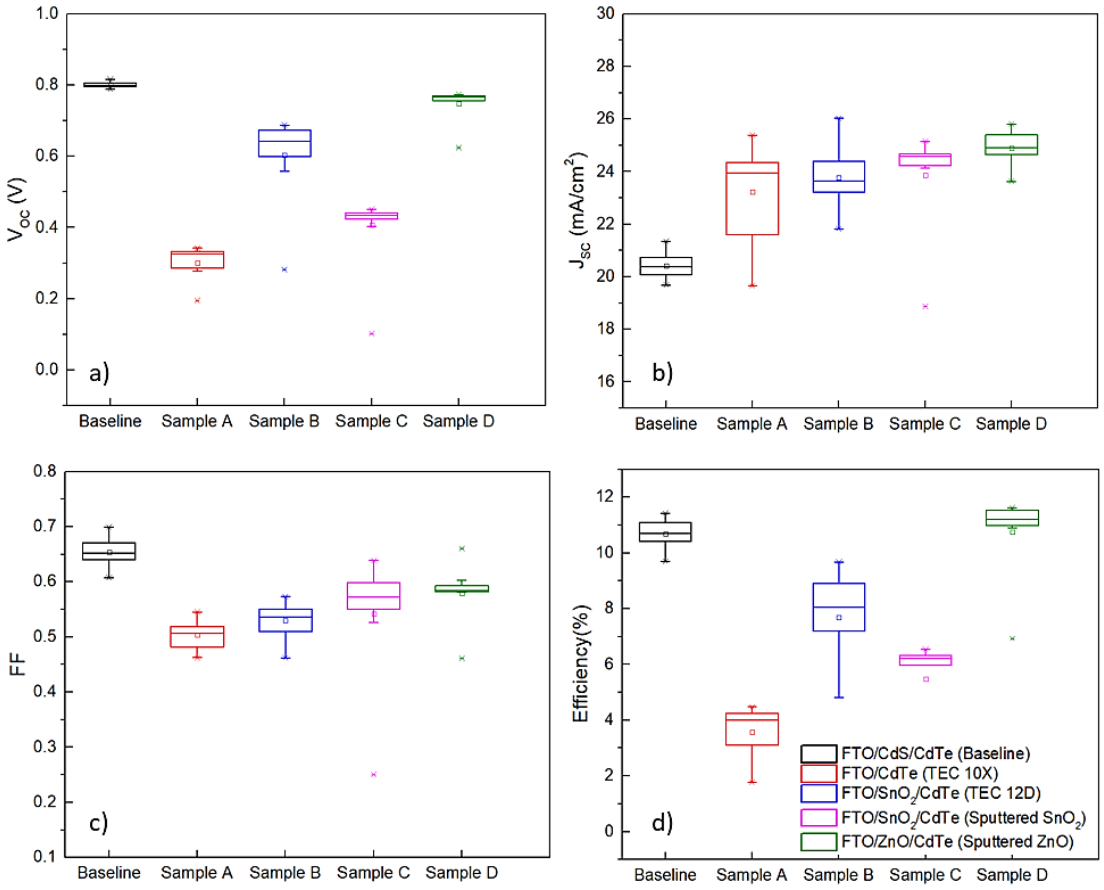

Fig. 5.8: Boxplots of a) V_{OC}, b) J_{SC}, c) FF and d) efficiency of samples with different buffer layers acting as the emitter in the device structure.

Fig. 5.9.a shows the J-V curves of the best devices on each of the investigated samples with the different buffer layers and *Table. 5.1* shows their respective parameters. Analysis of the results shows that device A (no buffer) and device C (SnO_2 sputtered buffer), exhibit low V_{OC} (< 400 mV) which is attributed to excessive shunting (shunt resistance < 500 Ω). Device B (SnO_2 buffer TEC 12D) exhibits a performance improvement; however, the V_{OC} is still limited to 687 mV due to a relatively low shunt resistance of ~ 820 Ω. The only device which is comparable to the baseline process is device D which included the ZnO buffer layer. The V_{OC} is ~ 40 mV lower which could indicate the formation of a poorest junction, however, the J_{SC} is 25% higher which compensates the V_{OC} and FF loss. This effect can be also illustrated in *Fig. 5.9.b* from the EQE of these cells. All devices exhibit superior EQE in the range between 350 and 600 nm when compared with the baseline process. This use of an HRT as a buffer layer in CdTe devices eliminates the absorption of photogenerated carriers inside the CdS, resulting in considerably J_{SC}. Specifically, in the case of device D (ZnO buffer), it is evident that there is substantial spectral loss in the range of 300 to 350 nm when compared with SnO_2 buffer layers which is attributed to the lower bandgap of ZnO. However, this is not translated in a current density loss. In that range, the available spectrum is too low to influence a drastic shift in J_{SC}. Because of this effect, device D has comparable J_{SC} with devices that do not exhibit the same spectral loss in that range. This is illustrated in *Fig.5.10* where a comparison between the spectral irradiance of the baseline, SnO:F/SnO_2 and SnO:F/ZnO at AM 1.5G is shown.

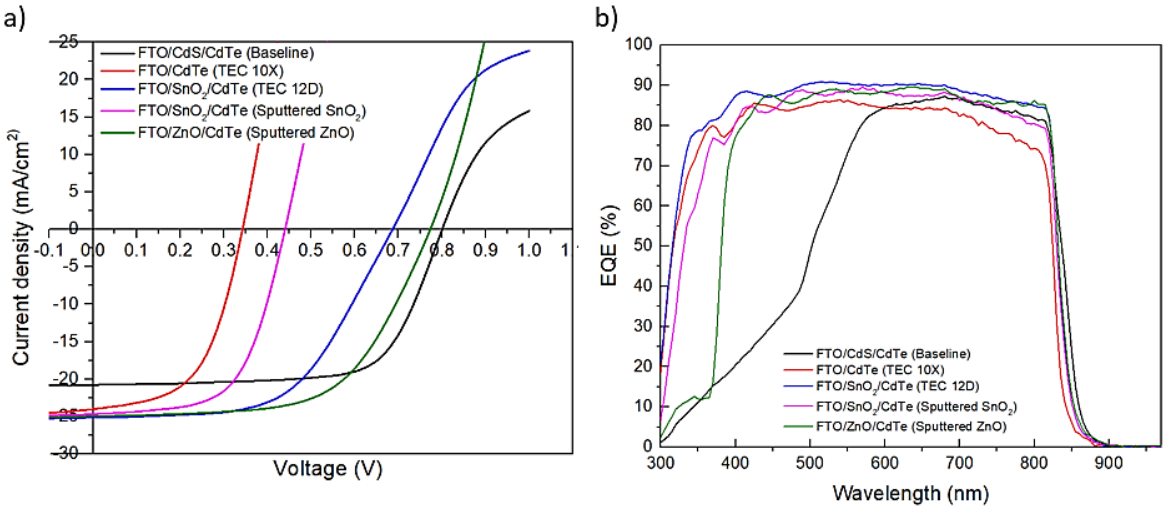

Fig. 5.9: a) J-V curves and b) EQE of best devices with different buffer layers acting as the emitter

Table 5.1: Performance parameters of devices with different buffer layers acting as the emitter in the CdTe device structure

	Baseline	*Device A*	*Device B*	*Sample C*	*Device D*
V_{OC} *(mV)*	816	342	687	440	773
J_{SC} *(mA/cm²)*	20.1	24	25.1	24.7	24.9
FF	69.6	54.5	60.3	56	60.3
Efficiency (%)	11.4	4.5	9.7	6.6	11.6
R_{Sh} *(Ω)*	2136	274	818	368	1089
R_S *(Ω)*	32	13	32	14	30

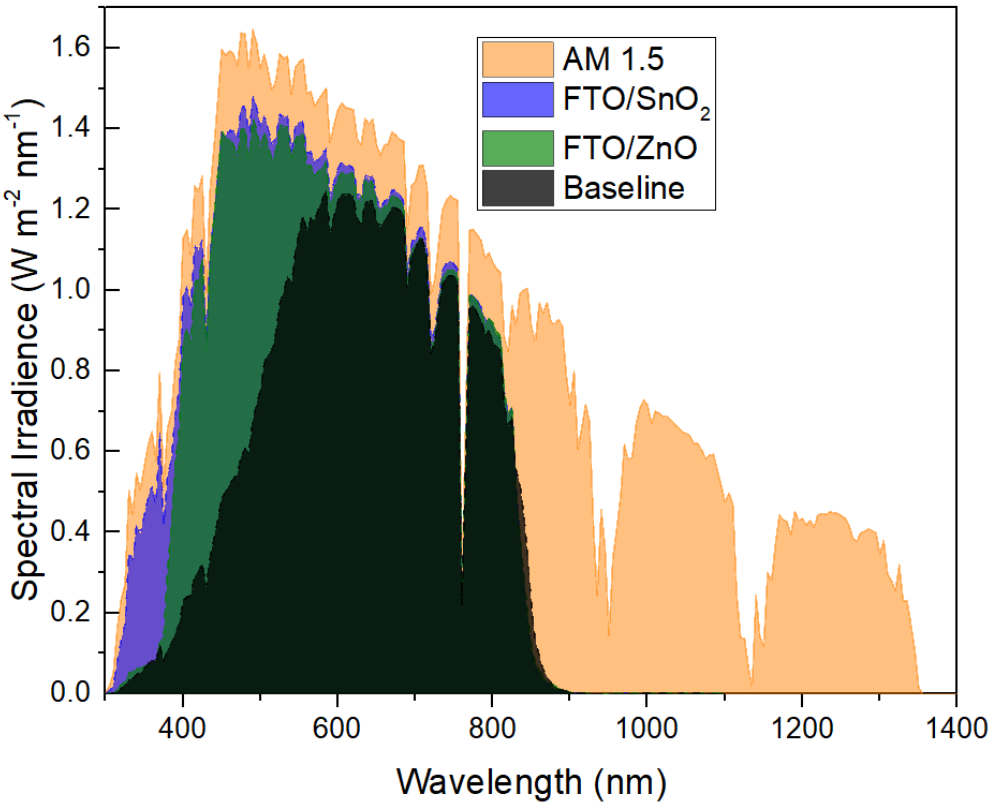

Fig. 5.10: Comparison between the spectral irradiance of the baseline structure, the SnO:F/SnO structure and the SnO:F/ZnO structure at AM 1.5 spectrum.

Discussion

It has been shown that it is possible to achieve high performing devices without the presence of a CdS buffer, however not all HRT's are suitable replacements as buffer layers. Devices directly deposited on SnO:F or SnO_2 buffer layers exhibited poor performances mainly due to low V_{OC} , FF and low shunt resistances. This is an indication of a weak diode formation between CdTe and the SnO_2 HRT buffer layers. Nevertheless, shunting cannot justifiably be the only reason of poor performance since devices with reasonable shunt resistance are possible but still exhibit lower V_{OC} than devices with either CdS or ZnO buffer layers. Song et al. and Kephart et al. [14][12] suggested that band alignment between the emitter and absorber is of key importance for high efficiency CdTe devices. As seen in *Chapter 1* (*1.6.1*), the band alignment is determined by the offsets of valence and conduction bands at the interface of the heterojunction.

In summary, to minimise interface recombination at the emitter/absorber interface, band alignment engineering demands that the minority carriers in the absorber become majority carriers at the emitter/absorber interface. This situation is referred to as absorber inversion [6][15]. A flat or slightly positive conduction band offset (CBO) which is referred to as "spike" is highly desirable. In this configuration, holes are limited at the interface (since the absorber is inverted) and thus cross recombination between electrons from the emitter is limited. A negative CBO (cliff) on the other hand would lead to reduced built in potential due to high interface recombination from high hole density provided at the interface from the absorber and electrons from the emitter [14][6][15]. This is shown in *Fig. 5.11*.

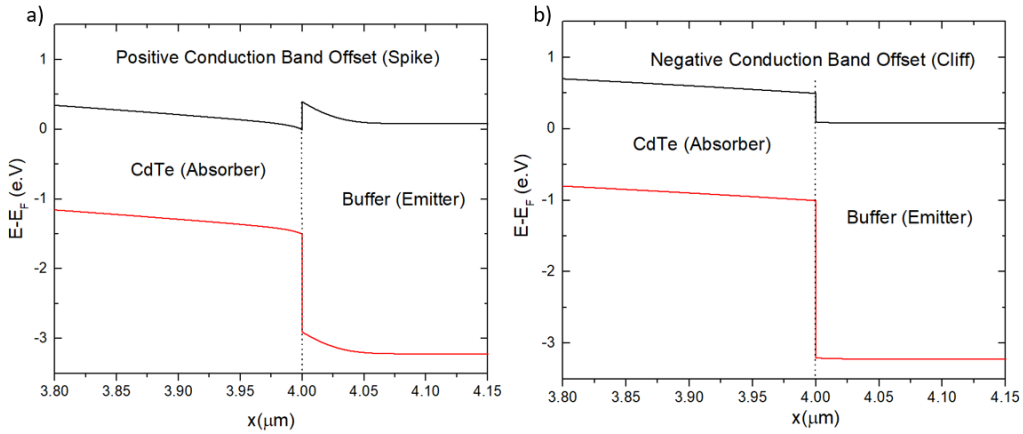

Fig. 5.11: Buffer/CdTe band diagram a) positive conduction band offeset (spike) and b) negative conduction band offset (cliff).

The varying performance behaviour that has been observed with SnO_2 based buffer layers could arise from the fact that one was deposited at room temperature, whilst the other was done by CVD at very high temperature. There could be significant changes in the growth and evolution of the sputtered sample during the CSS which could affect junction formation and consequently the performance.

Band alignment engineering could also explain this behaviour. It has been reported that it is possible for SnO_2 to exhibit a wide work function variation of more than 1 eV [17]. This can affect the emitter/absorber CBO and could explain the disparity in performances between devices with SnO_2 based buffer layers. To investigate this hypothesis, the effects of electron affinity variation on the

band alignment between SnO_2, and ZnO buffer layers and CdTe were investigated with SCAPS 1D simulation software. The parameters used in this simulation have been taken from commonly used values and are summarised in *Table 5.2* [18].

Fig. 5.12.a and Fig. 5.12.b (top graphs) show the change in the CBO between two identical SnO_2 layers with different electron affinities. Here the CBO has changed from ΔE_C = - 0.2 eV to ΔE_C = - 0.4 eV to simulate a moderate variation in the SnO_2 work function. The absorber depth where the charge equalises (Fig. 5.12.a and Fig. 5.12.b bottom graphs) shifts closer to the interface when the absorber inversion decreases (the quantity of $E_{p,a_{Z=0}}$ decreased from 1.1 eV to 0.9 eV) which can be translated to a loss in V_{OC} and FF due to enhanced interface recombination. This could explain the varying performance observed between similar devices with different SnO_2 buffer layers [14]. SnO_2 based layers used in HRT/CdTe junction produce a V_{OC} between the FTO/CdTe and CdS/CdTe structures due to the unfavourable band alignment (cliff) between SnO_2 and CdTe [12].

Simulated results showed that ZnO based HRT can provide a good alternative as buffer layers for CdTe devices. ZnO exhibits a nearly flat conduction bad offset with CdTe (Fig. 5.12.c). This induces a large absorber inversion at the interface (the value $E_{p,a_{Z=0}}$ increased to 1.45 eV) causing the carrier equalisation point to shift further away from the interface, and thus minimising interface recombination [19][12]. This can explain the experimental results where the ZnO/CdTe structure was able to retain most of the voltage compared to CdS/CdTe and improve the current density due to less absorption of photogenerated carriers.

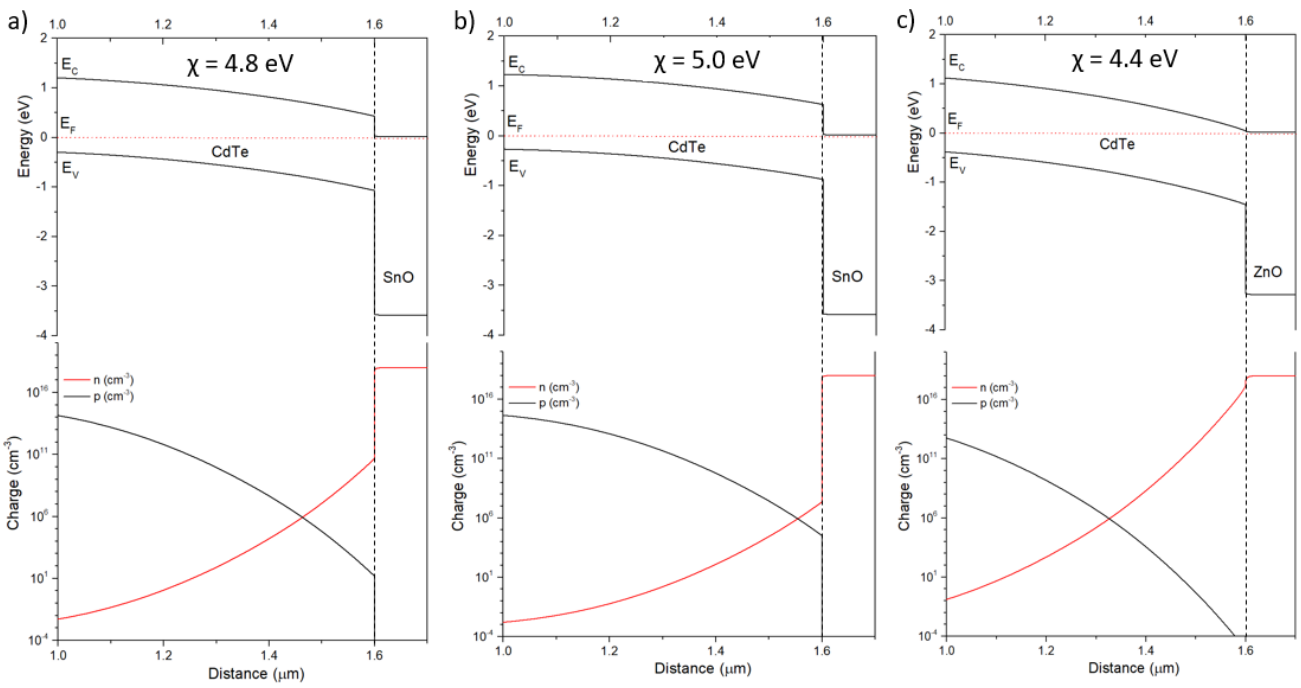

Fig. 5.12: Simulations with SCAPS 1D of buffer/CdTe band diagrams (top) and carrier distributions (bottom) of a) SnO_2 buffer with a negative conduction band offset of ΔE_C = - 0.2 eV, b) SnO_2 buffer with a negative conduction band offset of ΔE_C = - 0.4 eV and c) ZnO buffer with a flat conduction band offset of ΔE_C = 0 respectively.

Table 5.2: SCAPS 1D model parameters for different SnO and ZnO buffer layers used as a device emitter.

Parameter	*Symbol*	*SnO*	*ZnO*	*CdTe*
Thickness	x (nm)	150	150	3000
Bandgap	E_g (eV)	3.6	3.3	1.5
Electron Affinity	X (eV)	4.8 – 5.0	4.4	4.4
Dielectric Permittivity	$\varepsilon/\varepsilon_o$	9.0	8.5	9.4
CB effective density of states	N_c (cm^{-3})	2.2×10^{18}	2.2×10^{18}	8×10^{17}
VB effective density of states	N_V (cm^{-3})	1.8×10^{19}	1.8×10^{19}	1.8×10^{19}
Electron thermal velocity	μ_e (cm^2/Vs)	10	10	320
Hole thermal velocity	μ_h (cm^2/Vs)	25	25	40
Lifetime	T_n, T_p (ns)	0.1	0.1	2
Shallow uniform density	n or p (cm^{-3})	1×10^{18}	1×10^{18}	3×10^{14}
		Defect States		
Total defect density	N_t (cm^{-3})	D: 10^{15}	D:10^{15}	D:10^{13}
Defect energy level	E_t (eV)	midgap	midgap	midgap
Electron capture cross-section	σ_e (cm2)	1×10^{-12}	1×10^{-12}	2×10^{11}
Hole capture cross-section	σ_h (cm^2)	1×10^{-15}	1×10^{-15}	2×10^{11}

5.6 Concluding remarks

In this Chapter, various optimisation processes on the window/emitter interface were investigated. Specifically, in an effort to improve the J_{SC} of devices, experiments focussed on the effects of reducing the CdS thickness, the effects of adding a high resistive transparent layer (HRT) in the CdS/CdTe structure and their possible utilisation as alternative emitters for CdTe devices.

In conclusion, reducing the thickness of the CdS in the baseline CdS/CdTe structure, does not improve the current density as the original hypothesis suggested. In addition, thinning down the emitter, rapidly decreased the V_{OC} and the FF of the devices investigated. The detrimental effects observed in device performance were attributed to CdS/CdTe intermixing losses and to the formation of localised weak diodes and shunt paths from incomplete coverage of the TCO. To maintain a high V_{OC} and FF, the optimum CdS thickness was found to be ~ 100 nm. Devices with reduced CdS thicknesses showed partial or total consumption of the emitter (CdS) by the absorber (CdTe) resulting in lower performance.

The use of SnO_2 as an HRT buffer allowed the reduction of CdS film thicknesses without the formation of weak localised diodes which proved to limit the V_{OC} and FF of CdS/CdTe devices. Devices with efficiencies of ~ 12% were achieved through increase in V_{OC} and J_{SC} by reducing the absorption of photogenerated carriers inside the CdS buffer layer and preventing the formation of shunt paths. However, the CdS buffer still presented a significant loss of photogenerated carriers through absorption, limiting the device performance. Thus, replacing CdS buffer with a suitable candidate may offer a significant improvement to the $J_{SC.}$

Substitution of the CdS buffer with an HRT increased the current density. However, not all HRT's are suitable candidates as an alternative buffer layer. SnO_2 based buffer layers showed a variable performance uniformity which was attributed to electron affinity fluctuations between SnO_2 samples. SCAPS 1D band diagram simulations showed that SnO_2 based HRT's can suffer from an unfavourable band alignment (cliff) with CdTe, resulting in low voltages due to increased interface recombination. ZnO buffer layers proved to be a more

suitable candidate for CdS buffer substitution. Due to the formation of a zero-conduction band offset (flat) with CdTe, ZnO/CdTe devices can retain most of the V_{OC} compared to CdS/CdTe and improve the current densities due to less absorption of photogenerated carriers leading to performance improvements.

ZnO buffer layers have been extensively used as HRT's in both CIGS and CdTe devices [19][20][21][22], however the use of ZnO as a CdS replacement is very sparse. Some of the techniques employed to optimise the ZnO as an HRT layer in literature could also be used to further optimise the ZnO as a buffer layer. Specifically, tuning some of its characteristics during deposition, could benefit band alignment with CdTe and it is in the authors opinion that this could provide further performance improvements for CdTe solar cells.

5.7 References

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Chapter 6. Interface optimisation part C: The absorber/back contact interface

6.1 Introduction

As discussed in Chapter 1 (*1.6.4*), in CdTe devices, the absorber/back contact interface yields a very difficult problem, ohmic contact formation. So far in this thesis the absorber (CdTe) was contacted with ~ 84 nm of gold by evaporation without the surface of the absorber receiving any modification, treatment or any intentional doping. This had an impact on the fabricated device performance limiting their true potential due to the formation of a Schottky barrier.

Traditionally, CdTe solar cells receive a surface modification step, such as etching, to create a Te rich surface by removing Cd. Subsequently, a thin layer of Cu is alloyed to induce the formation of $Cu_{2-x}Te$, to either lower the back-contact barrier and/or create a tunnelling junction. This is achieved through the reduction of the barrier's depletion width by moderately doping the back contact's surface [1]. However, while Cu was found to be beneficial for the initial performance of the devices, if not managed properly, it can have detrimental effects [2]. Stability issues arise from the high bulk diffusion of Cu in CdTe (3 x 10^{-12} cm/s at 300 K) and weak Cu-Te bonds. Cu under forward bias stress, can migrate from the back contact and accumulate in CdS, forming a compensating doping complex which limits the device performance [3].

This chapter concentrates on the absorber/ back contact interface optimisation and is divided in two parts. The first part investigates the role of Cu on the performance, controllability and stability of non-etched CdTe solar cells. The second part of this chapter describes the implementation of a new baseline process, based on substrate configuration of CdS/CdTe devices and also focuses on the development of a Cu-free back contact based on transitional metal oxides (TMO's) and specifically MoO_x. In substrate configuration the CdS is deposited after the CdTe, enabling the dissociation between the high temperature $CdCl_2$ activation treatment and junction formation. This can

provide better control over the p-n junction formation but most importantly, it allows the investigation of the absorber/back contact interface separately without any contribution from other interfaces. However, because the deposition order is reversed, traditional processes employed in superstrate configuration such as etching are not applicable in this structure. This makes the realisation of an ohmic contact in substrate CdTe devices more difficult and the effects of the back contact are more pronounced and easily identifiable.

6.2 Copper doping of non-etched CdS/CdTe devices

In this section, the effects of adding Cu at the back contact without performing a surface modification step on performance and degradation of CdTe solar cells are investigated. As mentioned earlier it has been reported that stability issues arise from the high bulk diffusion of Cu in CdTe (3×10^{-12} cm/s at 300 K) and weak Cu-Te bonds [2]. Not etching the CdTe surface prior to back contact deposition could limit the formation of $Cu_{2-x}Te$ and possibly limit the degradation, since fewer weak Cu-Te bonds will be formed. However, since Cu_{Cd} has been shown to act as an acceptor in CdTe [3], intrinsic V_{Cd} inside the CdTe could be enough to cause moderate surface doping and induce a tunnelling junction and/or lower the back-contact barrier without the need of a surface modification step.

Identical samples received different amounts of evaporated Cu (0, 10, 20, 50 and 100 Å) to act as the primary contact by thermal evaporation. Secondary contact formation was carried out with subsequent evaporation of ~ 84 nm of Au without breaking the vacuum. To diffuse the dopant (Cu) inside CdTe, samples which received a primary contact were subjected to a post-deposition anneal at 200°C for 20 minutes in air. To identify the long-term effects of Cu on non-etched solar cells, devices with different amount of evaporated Cu where left under darkness for 150 days and their performance was reassessed.

6.2.1 Initial performance of Cu-doped CdTe solar cells

In *Fig. 6.1.a* the J-V curves of the best cells of each of the investigated samples are illustrated. The baseline device without intentional Cu doping used in this study exhibits a device efficiency of 10.3% with a V_{OC} of 766 mV, FF of 69.2% and J_{SC} of 19.4 mA/cm^2. Additionally, the cell exhibits a 'roll-over' in the forward bias of the curve which, as discussed before, is an indication of a Schottky barrier formation at the back contact [4].

Adding 10 Å of evaporated Cu increased the efficiency to 11.4%, by mainly increasing the V_{OC} and FF to 818 mV and 70.6% respectively. When the Cu amount increased to 20Å, the FF remained unaffected (70.6 %) while the V_{OC} increased to 825 mV. Further Cu increase to 50Å at the back contact resulted in a slight decrease in V_{OC} (820 mV), but in a FF increase to 72.9%. For both devices with 20Å and 50Å evaporated Cu, efficiency remained the same at 11.4%. Further increase in Cu amount to 100 Å resulted in a lower V_{OC} (815 mV) however, FF increased to 73.2% with the efficiency increasing to 11.8 %, which was the maximum performance achieved in this study. All the devices with any amount of Cu exhibit similar electrical performance with efficiency variation of ± 0.5 %. This variation is attributed to the current density distribution of ± 1 mA/cm^2 which falls within the measurement uncertainty of the solar simulator used.

Table 6.1 summarises the performance of the investigated devices along with other typical electrical parameters. It seems that there is not a significant correlation between the amount of added Cu at the back contact (in the range investigated) and efficiency, however, only that there is a significant difference between samples with and without Cu. This observation is also in agreement with literature for etched devices [5]. It is worth mentioning that while the device with 100 Å exhibits the highest device performance due to a better R_S, it had the largest ideality factor (n) and dark saturation current (J_0), suggesting that larger amounts of Cu could affect the quality of the junction. Additionally, none of the devices with Cu at the back contact exhibit a 'roll-over' in the forward bias. This is indicative of the formation of an ohmic contact caused by doping the back surface of the absorber, or by lowering the back- contact barrier. This

effect is also suggested by the increase in V_{OC} and FF of the Cu containing devices, when compared with the baseline process.

In CdTe absorbers with moderate thickness (~ 3 µm), such as in this case, the depletion width of the two opposing diodes (main diode and back contact diode) overlap. When the forward current approaches the reverse saturation current of the back-contact diode (J_{b0}) the current saturates in the forward bias ('roll-over') and the voltage drops at the back-contact diode limiting the device performance [6]. However, most likely, upon introduction of Cu the back surface of the absorber is moderately doped, creating a tunnelling junction at the back by decreasing the Schottky diode depletion width. This allows the majority carriers to tunnel through the barrier and transported effectively to the back electrode. This results in a V_{OC} and FF increase [7][3].

Table 6.1: Summary of performance parameters of devices with different amount of Cu.

Cu (Å)	**V_{oc} (mV)**	**J_{sc} (mA/cm²)**	**FF (%)**	**PCE (%)**	**R_{sh} ($\Omega.cm^{-2}$)**	**R_s ($\Omega.cm^{-2}$)**	**n**	**J_0 (mA/cm²)**
0	767	19.33	69.3	10.3	2010	24	-	-
10	818	19.7	70.6	11.4	2883	12.9	1.46	$2.70x10^{-8}$
20	825	19.4	70.6	11.3	3174	11.7	1.65	$2.34\ x10^{-8}$
50	820	18.9	72.9	11.3	3506	11.3	1.55	$2.34\ x10^{-8}$
100	815	19.8	73.2	11.8	3514	6	1.67	$2.27x10^{-7}$

EQE measurements carried out on these devices (*Fig. 6.1.b*) showed a reduction in recombination losses when Cu was added to the back contact. Back surface recombination can be detected in the CdS/CdTe EQE curve in the range of ~ 800 to 840 nm. The device with no intentional Cu doping exhibits high recombination losses in this range where the EQE is lower compared with devices that have been Cu treated. Since the main diode and back contact diode are not independent, the back-contact barrier leads to enhanced minority carrier transport to the back contact (in this case electrons). The reduction in back surface recombination losses indicates that doping the back-contact surface with Cu creates a narrower junction for majority carriers (holes) at the

back contact to pass through which can limit the recombination and increase the V_{OC} and FF.

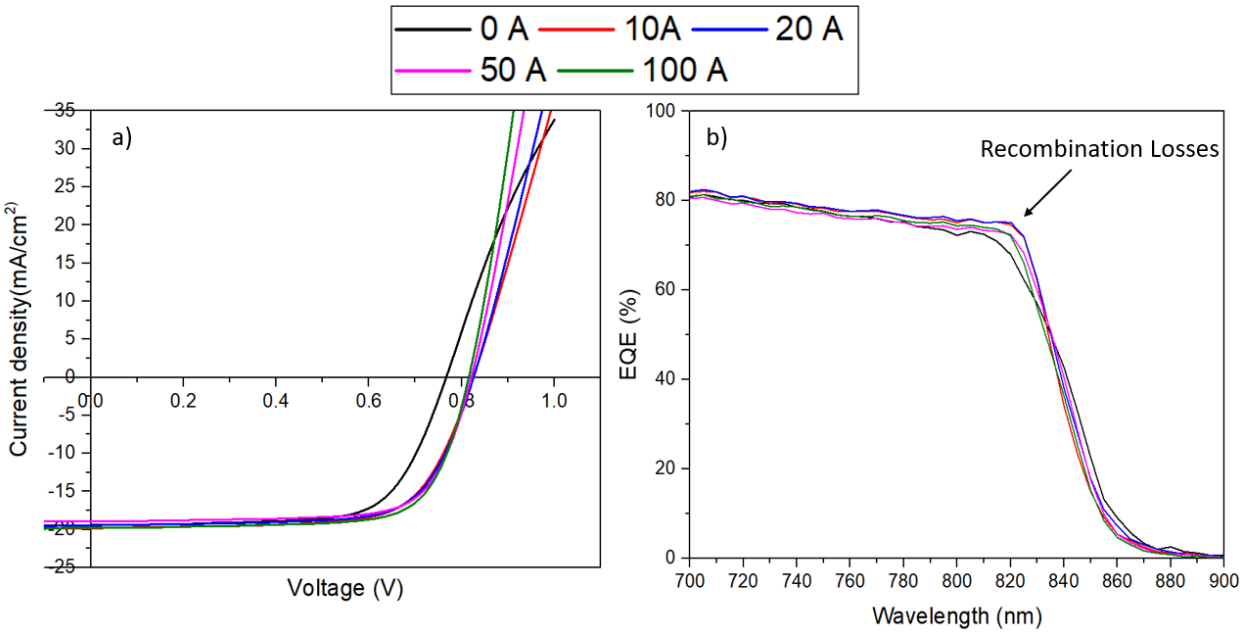
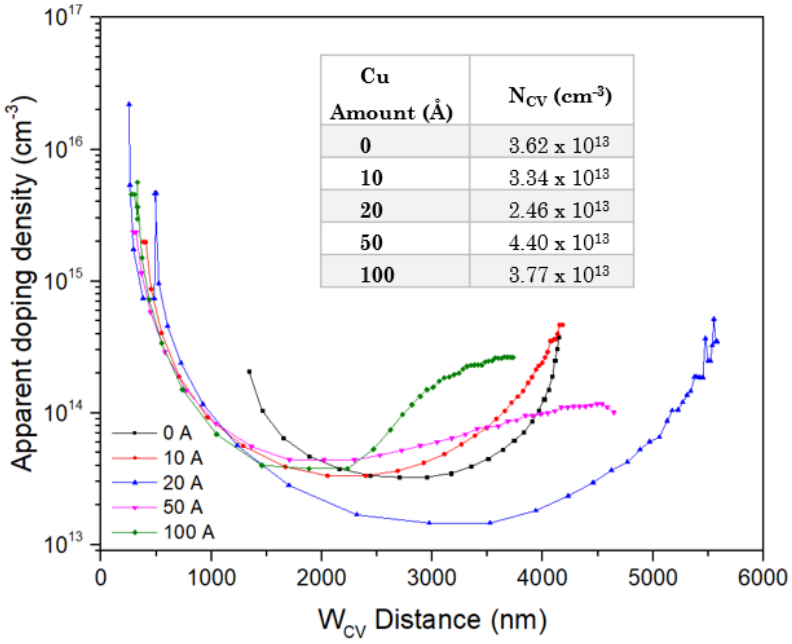


Fig. 6.1:a) J-V and b) EQE of representative cells for different Cu layer thicknesses at the back contact.

C-V measurements were carried out on the investigated samples to determine the net acceptor densities (*Fig.6.2*). A comparison between the investigated samples showed no significant change or trend in net acceptor density between samples with different amounts of Cu at the back contact. Hence, the amount of added Cu was found to be independent of doping densities. This effect has been also observed by Ferekides et al. for $CuTe_2$ contacted samples [8].

It is reported that Cu increases the net acceptor density by one order of magnitude (from x 10^{13} to x 10^{14}) [9] however, the C-V results presented here do not exhibit the same behaviour. This can be attributed to samples not receiving a surface modification step prior to back contact deposition. In this case, Cu acts as a substitutional acceptor of the available intrinsic V_{Cd}. Since these are limited, the net acceptor density remains unaffected. Note that it is not possible to distinguish surface and bulk acceptor densities from C-V measurements. Moderate doping of the absorber is not enough to increase the net acceptor

densities of the whole device, but adequate to induce performance improvements.



Cu Amount (Å)	N_{CV} (cm^{-3})
0	3.62 x 10^{13}
10	3.34 x 10^{13}
20	2.46 x 10^{13}
50	4.40 x 10^{13}
100	3.77 x 10^{13}

Fig. 6.2: Doping profiles of representative cells with different amount of Cu at the back contact.

To investigate if Cu inclusion lowers the barrier height or causes a tunnelling junction as previously suspected, the barrier height at the back contact was measured using the method proposed by Koishiyev et al. [10]. Here, the dark temperature dependent J-V was measured in 10 K steps in the range between 195 to 315 K and the turning current (the current which 'roll-over' appears), J_T, was extracted for each temperature and plotted in an Arrhenius plot of $\ln(J_T/T^2)$ vs. 1/T. The slope of the linear fit represents the barrier height ($q\Phi_b$) and the intercept is the Richardson constant (A) as derived from eq. 6.1 below.

(*eq. 6.1*)

$$J_T = A\,T^2 e^{-\frac{q\Phi_b}{kT}}$$

Representative devices with 0Å and 10Å of added Cu showed similar extracted Φ_b of 0.49 and 0.48 eV respectively (*Fig. 6.3*). The results show that since the barrier height remains similar, performance improvements must be due to the

formation of a tunnelling junction at the back contact. Enough V_{Cd} are replaced by Cu to moderately dope the CdTe's back surface which creates a tunnelling junction through narrowing the barriers depletion width. This improves the V_{OC} and the FF and the 'roll-over' effect in the J-V disappears.

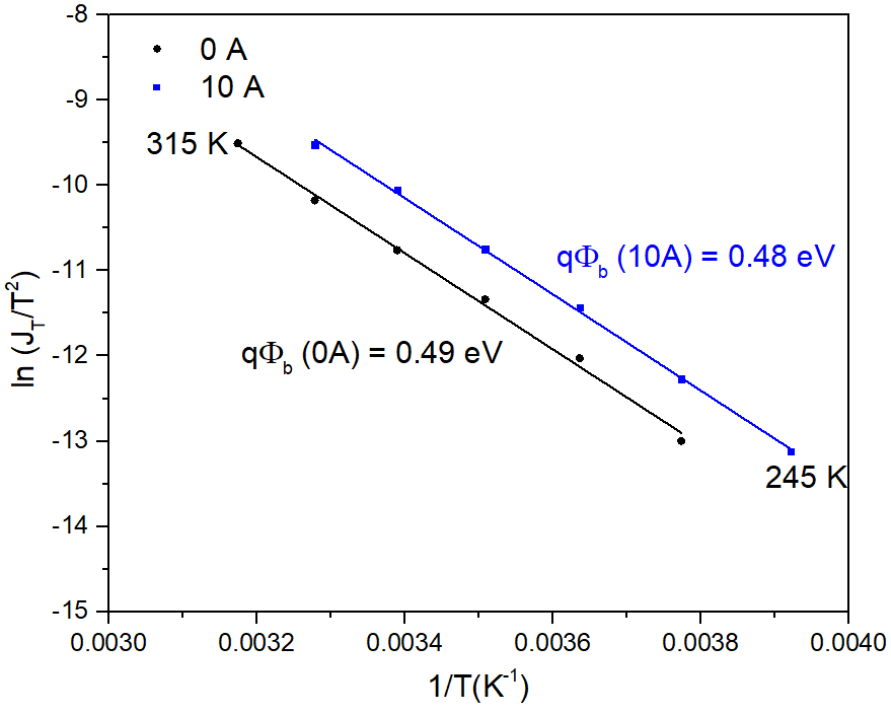


Fig. 6.3: Arrhenius plots of turning currents J_T with 0Å and 10Å Cu doped solar cells. Back contact barrier heights $q\Phi_b$ extrapolated from the slope of the linear fits are displayed.

In *Fig. 6.4* box plots with all the performance indicators for each cell on the investigated samples are illustrated. The V_{OC} and FF significantly increased by adding any amount of Cu to the back contact. The resulting tunnelling junction allows holes to flow more easily, reducing the effects of the opposing diode at the back contact [2]. However, the distribution was found to vary with different amounts of added Cu. Generally, by increasing the amount of Cu the V_{OC} and FF uniformity across a sample tend to decrease. This behaviour can be attributed to non-uniform Cu incorporation due to surface oxidisation. As a product of V_{OC} and FF, efficiency follows the same trend with a significant increase when Cu is added at the back contact. The efficiency distribution variation is more pronounced with low performing and high performing cells found across a sample. J_{SC} stays relatively the same for Cu and non-Cu doped samples, in accordance with literature [3].

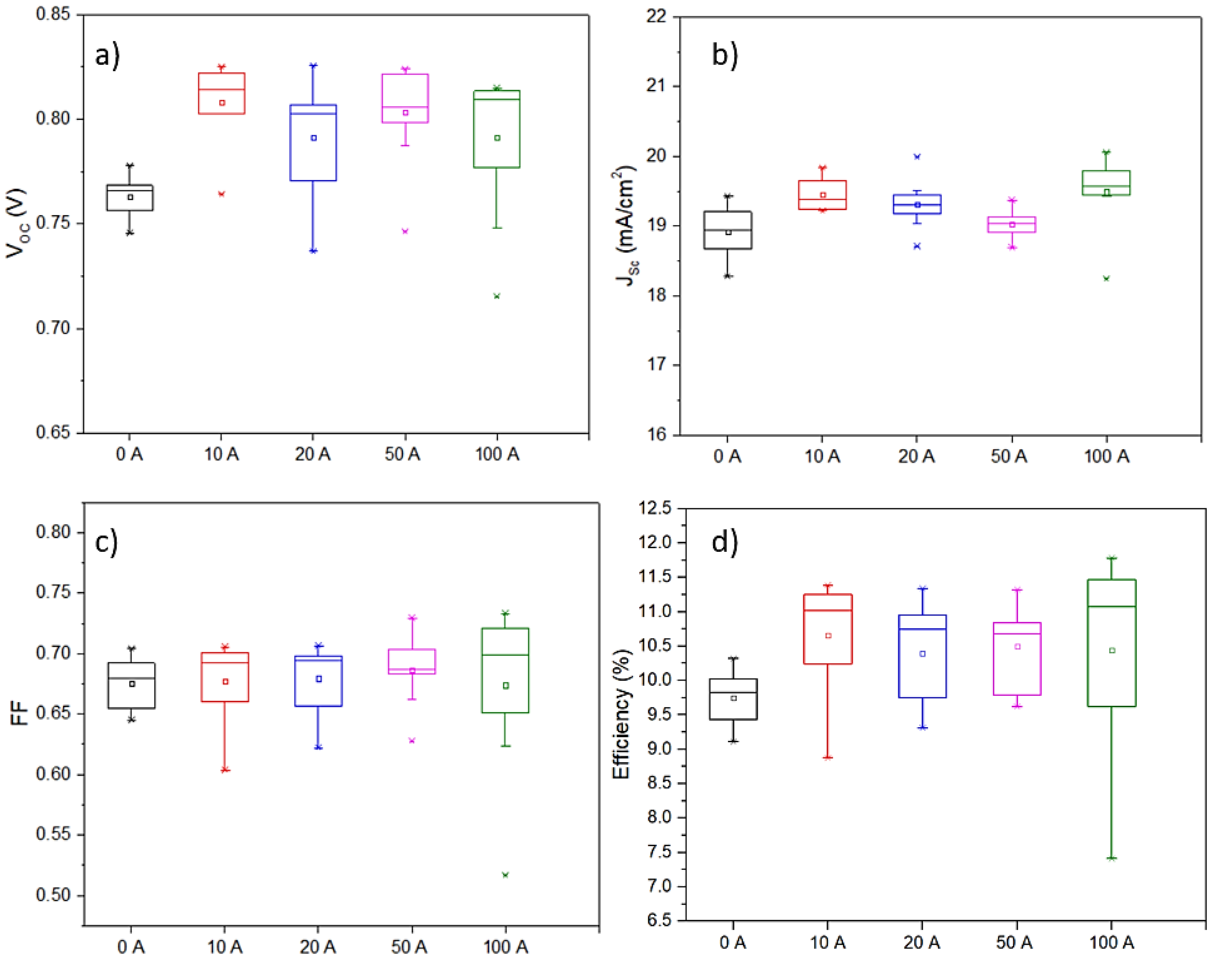


Fig. 6.4: Boxplots of a) V_{OC}, b) J_{SC}, c) FF and d) efficiency of devices with different amount of Cu at the back contact.

6.2.2 Degradation study of non- etched devices with Cu

In this section the effects of device degradation of non-etched Cu doped CdTe solar cells are investigated. As shown in the previous section, Cu can moderately dope the back surface of the absorber layer on non-etched samples which is sufficient to cause performance improvements, especially of the V_{OC} and FF. However, as previously discussed there are numerous reports that attribute degradation of CdS/CdTe devices to Cu migration from the back contact [11][12][13]. Specifically, it was reported that Cu can act as a doping compensating agent (Cu_{Cd} is responsible for deep acceptor levels in CdS) when diffused inside the CdS thus limiting the device performance by reducing the emitter/absorber inversion and consequently the V_{OC} [14].

Devices with Cu kept in the dark for 150 days exhibit significant degradation as illustrated in *Fig. 6.5*. The initial performance of the device is represented with straight lined boxes while the performance after 150 days in dark is represented by dashed lined boxes. The device without any amount of Cu in the back contact showed a negligible reduction in performance after it was kept for 150 days in the dark compared with its initial performance. V_{OC} remained the same, while FF showed a slight reduction. This can be attributed to the measurement uncertainty of the equipment used. The J-V curves before and after degradation (*Fig. 6.6*) of this device, show that the J-V remained unaffected under normal operation, however the 'roll-over' has evidently increased in the forward bias. This could imply an increase in the back-contact barrier, nevertheless the change is not significant enough to cause a reduction in V_{OC}.

All the devices with any amount of evaporated Cu exhibit performance degradation. While these devices exhibit similar current density on day 0 and day 150 (negligible differences due to solar simulator measurement uncertainty), the V_{OC} and FF have degraded substantially. *Table 6.2* summarises the V_{OC} and FF performance of the initial devices and after 150 days.

A comparison between the J-V curves of the 10Å and 20Å Cu containing devices before and after, showed that the 'roll-over' in the forward bias reappeared after the device was rested for 150 days in the dark. For clarity purposes the 50Å and 100Å Cu containing samples are not illustrated in *Fig. 6.6* (they exhibit the same behaviour as the previously discussed samples). This is indicative that Cu has migrated from the back contact, reducing back surface p-type doping, and thus expanding the depletion width of the back-contact barrier. Holes cannot effectively tunnel through the back-contact barrier and the current saturates at the back contact forming a 'roll-over'. Since there is no effective tunnel through the barrier for holes, there is voltage reduction due the opposing diode. These observations agree with literature where similar results have been obtained in etched devices with Cu at the back contact [3][5].

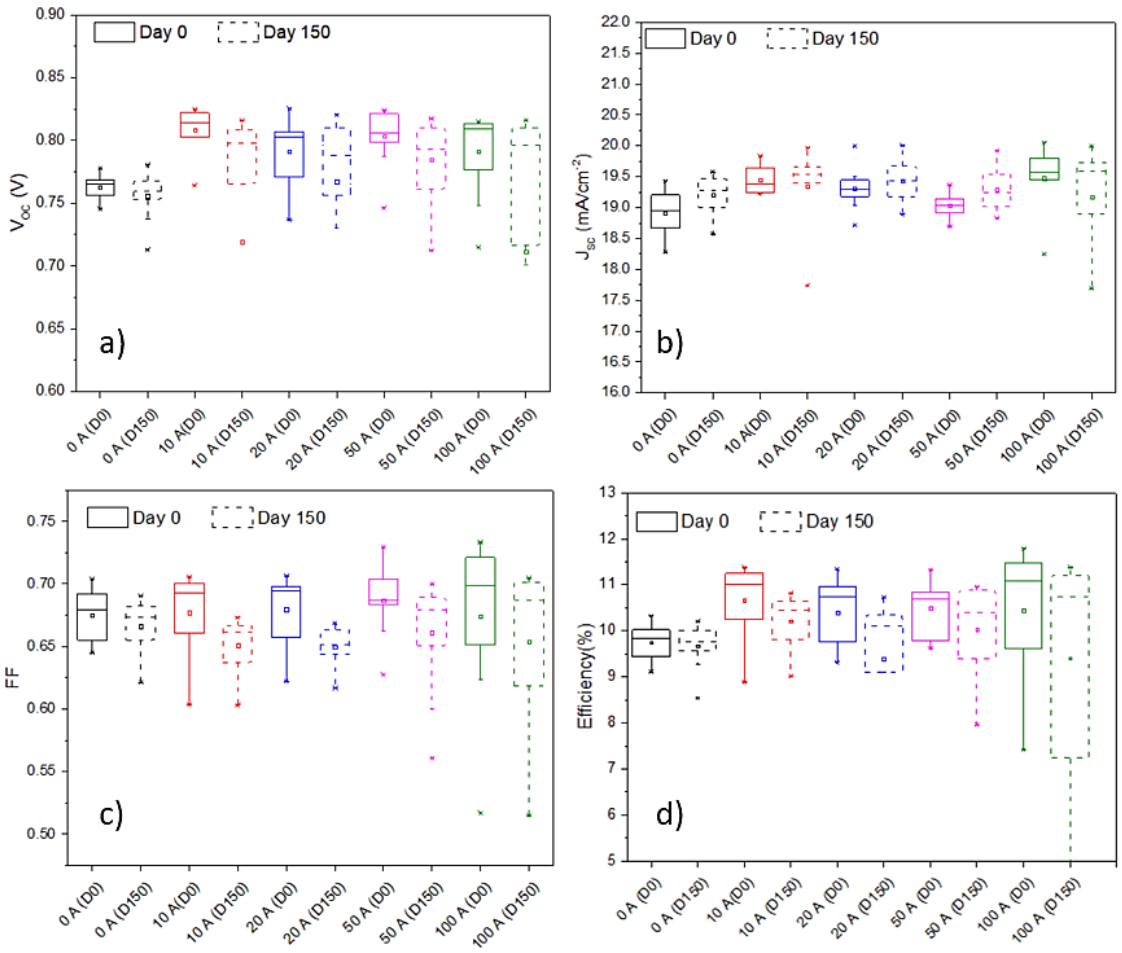


Fig. 6.5: Box blots of a) V_{OC}, b) J_{SC}, c) FF and d) efficiency of devices with different amount of Cu at the back contact. Solid lines represent the initial performance of the devices while dotted lines represent the performance after the devices were kept for 150 days in darkness.

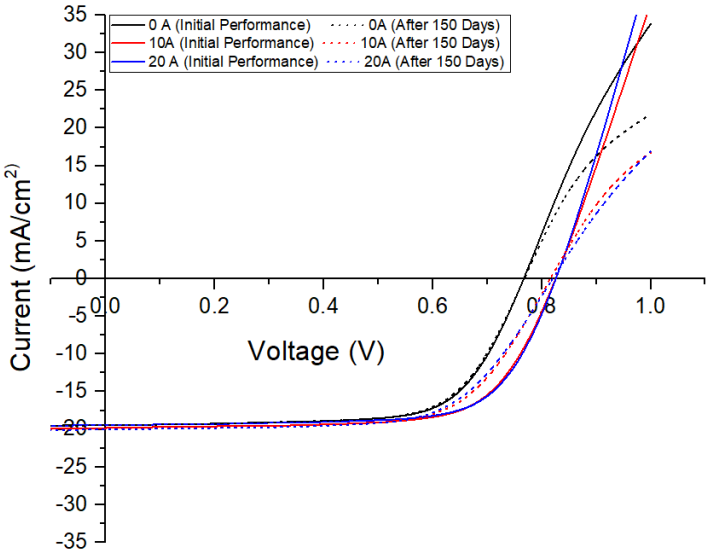


Fig. 6.6: J-V curves for representative devices with 0Å, 10Å and 20Å Cu-doped devices. Solid lines represent the initial performance of the devices while dotted lines represent the performance after the devices were kept for 150 days in darkness.

Table 6.2: Comparison between V_{OC} and FF of initial and degraded performance of representative solar cells with different amount of Cu at the back contact.

	Initial Performance		**After 150 days**	
Cu Amount (Å)	V_{OC} (mV)	FF (%)	V_{OC} (mV)	FF (%)
0	766	69.2	763	68.5
10	825	69.6	815	66.4
20	825	70.6	820	65.0
50	820	72.9	810	69.9
100	815	73.2	716	34.0

A comparison between net acceptor densities of the investigated samples measured with C-V is shown in *Table 6.3*. There is a reduction in net acceptor densities for all the investigated devices regardless of the Cu amount. The net acceptor density decrease is more pronounced in devices with Cu at the back contact. All Cu contacted devices exhibit a net acceptor density difference of > 1.5×10^{13} after 150 days when compared with their initial performance. This further supports that Cu has migrated away from the back-contact, either

decreasing the absorber's back contact surface doping density and/or by reducing the n-type doping density of the emitter. Migration of Cu inside the CdS can form Cu_{Cd} which acts as deep acceptor [14], which can result in reduced net donor densities. Unfortunately, with C-V measurements it is not possible to isolate these two effects and both mechanisms are proposed as the reason for the reduction in net acceptor densities observed.

Table 6.3: Summary of initial and degraded net acceptor densities (N_{C-V}) of representative solar cells with different amount of Cu at the back contact.

Cu thickness (Å)	**N_{C-V} (cm^{-3}) Initial performance**	**N_{C-V} (cm^{-3}) After 150 days**
0	3.62×10^{13}	3.00×10^{13}
10	3.34×10^{13}	1.04×10^{13}
20	2.46×10^{13}	0.935×10^{13}
50	4.40×10^{13}	2.93×10^{13}
100	3.77×10^{13}	1.54×10^{13}

Significant degradation still occurs in non-etched Cu-contacted devices. Not performing a surface modification step to control the formation of $Cu_{2-x}Te$ bonds has not achieved the intended purpose of limiting device degradation. This investigation suggests that Cu diffusion is not limited to devices that have been subjected in thermal or light stresses. The investigated Cu devices were prone to degradation even though they were kept in the dark for 150 days while there was a negligible degradation of the non-Cu contacted device. This is indicative that Cu migration is caused not only by stress but also by the highly diffusive nature of Cu in CdTe and weak $Cu_{2-x}Te$ bonds which can easily dissociate at room temperature. This illustrates the need of a stable back contact for CdTe devices which can prevent the formation of a Schottky barrier and not cause performance degradation. This is investigated in the next section of this chapter through the development of a substrate configuration baseline and the use of MoO_x as a back-contact buffer layer.

6.3 Absorber /back-contact interface development through CdTe substrate configuration

The aim of this section is to study the effects of MoO_x buffer layers on the back-contact interface through the realisation of a substrate baseline process for CdTe solar cells. Specifically, the O_2 content during RF sputtered MoO_x deposition was found to have a strong effect on thin films and finished solar cell properties.

So far, in this thesis the superstrate configuration was utilised to investigate various interface effects. Superstrate configuration provided a repeatable baseline process which enabled interface optimisation through comparative studies. Nonetheless, junction formation and interdiffusion between CdS and CdTe can present a significant challenge for the investigation of the back-contact interface. Oxygen, chlorine and sulphur migration through grain boundaries during high temperature fabrication processes makes it almost impossible to isolate the effects of the absorber/back contact interface [15].

In substrate configuration the back-contact buffer/metal must be able to withstand the subsequent high temperature processes involved in fabrication of CdTe solar cells. Mo has been chosen as the secondary contact (metal) because of the matching expansion coefficient with CdTe, low cost, extensive use in CIGS devices and compatibility with variety of substrates. MoOx proved to be a suitable primary contact (buffer) candidate for back contact applications due to the high work functions reported in literature (up to 6.8 eV) [16], which can potentially reduce the barrier height at the back contact. Most importantly, by varying the O_2 concentration during reactive sputtering, the optical and electrical properties could be adjusted [17]. This effect could be used to create a moderately doped MoO_x layer which could act as a tunnelling junction between CdTe and Mo.

6.3.1 Methodology

For this experimental procedure, MoO_x films were deposited by reactive sputtering at a pressure of 1 mTorr for 15 min from a metallic Mo target. O_2

concentration in Ar was varied in the range from 0% to 26%. For each run, the target was cleaned for 15 minutes with the shutter closed, before introducing any O_2. This was done to remove any target oxidation from prior depositions. Characterisation of MoO_x was carried out by deposition on SLG substrates. For CdTe solar cells, MoOx films were deposited on 1 mm soda lime glass (SLG) substrates with ~ 2 µm of RF sputtered Mo supplied by M-Solv Ltd. Prior to MoO_x deposition, Mo thin films exhibited a sheet resistance of ~ 0.3 Ω/sq.

CdTe deposition was carried according to deposition parameters found in *section 3.2.2* using CSS. To keep the temperature profile and the substrate-source separation consistent (2 mm) with the superstrate baseline process, two more 1 mm SLG substrates were placed between the substrate graphite block and the Mo/MoO_x coated substrates. T_{Sub}, T_{Sou} and pressure were kept at 515°C, 630°C and 1 Torr respectively. CdTe thickness optimisation was carried out by varying the deposition time between 2 and 5 minutes in 1-minute intervals. The resulting average CdTe thickness was found to be 2.6 µm, 4.4 µm, 7.5 µm and 9.3 µm for 2, 3, 4 and 5 minute of CdTe depositions respectively.

The $CdCl_2$ treatment was carried out using thermal evaporation of 0.5 g of $CdCl_2$ and subsequently annealed on a hot plate at a dwell temperature of 425°C for 1 minute, as per baseline process in *section 3.3.3*. CdS was deposited by ultrasonically assisted chemical bath deposition, where an ultrasonic probe was used to agitate the bath. The deposition was carried out for 1 hour in a 70° C preheated bath as per *section 3.2.3.a*.

The top contact was formed by the deposition of a bilayer consisting a thin (~ 50 nm) high resistive intrinsic zinc oxide (i-ZnO) layer, followed by a thick (~ 500 nm) highly conductive Al-doped ZnO layer (AZO), by RF sputtering. The i-ZnO deposition was carried out for 15 min in 1% O_2 in Ar environment. The subsequent AZO deposition was carried out from a 2 wt% Al_2O_3 doped ZnO target for 1 hour resulting in a sheet resistance of ~ 15 Ω/sq. Both depositions were carried out at room temperature at a working pressure of 1 mTorr.

Finally, the front grid deposition was carried out by thermal evaporation of silver (~ 500 nm) through a shadow mask onto the TCO. Individual cells of an

area of 0.25 cm^2 were mechanically scribed. An example of a finished sample is shown in *Fig. 6.7*.

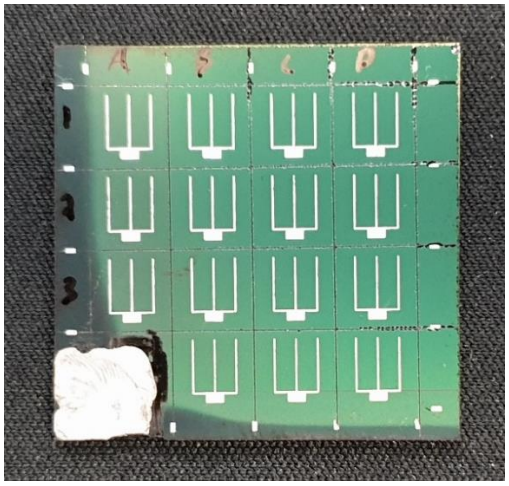


Fig. 6.7: A representative finished CdTe substrate device.

6.3.2 Substrate configuration baseline process

In *Fig.6.8* the performance parameters including V_{OC}, J_{SC}, FF and efficiency of samples subjected to different CdTe deposition times are shown in the form of boxplots. Device performance showed a curvilinear trend with optimum CdTe deposition time found at 3 minutes with an average efficiency of 4.3%. The average V_{OC} increased between the 2-minute and 3-minute deposition by approximately 100 mV. Further increase in CdTe deposition time resulted in a progressive decrease in V_{OC} to ~ 430 mV. The J_{SC} showed a gradual reduction with increasing CdTe thickness, where the 5-minute deposited sample exhibited the lowest average J_{SC} value of ~ 15 mA/cm^{-2}. The FF showed a similar trend with V_{OC} where the 3-minute deposited sample exhibited the highest average FF of ~ 45%.

Similar results for substrate configuration devices on Mo substrates with varying absorber thickness have been also observed by B.L Williams et al. [18] where the optimum absorber thickness was found to be at approximately 4 µm.

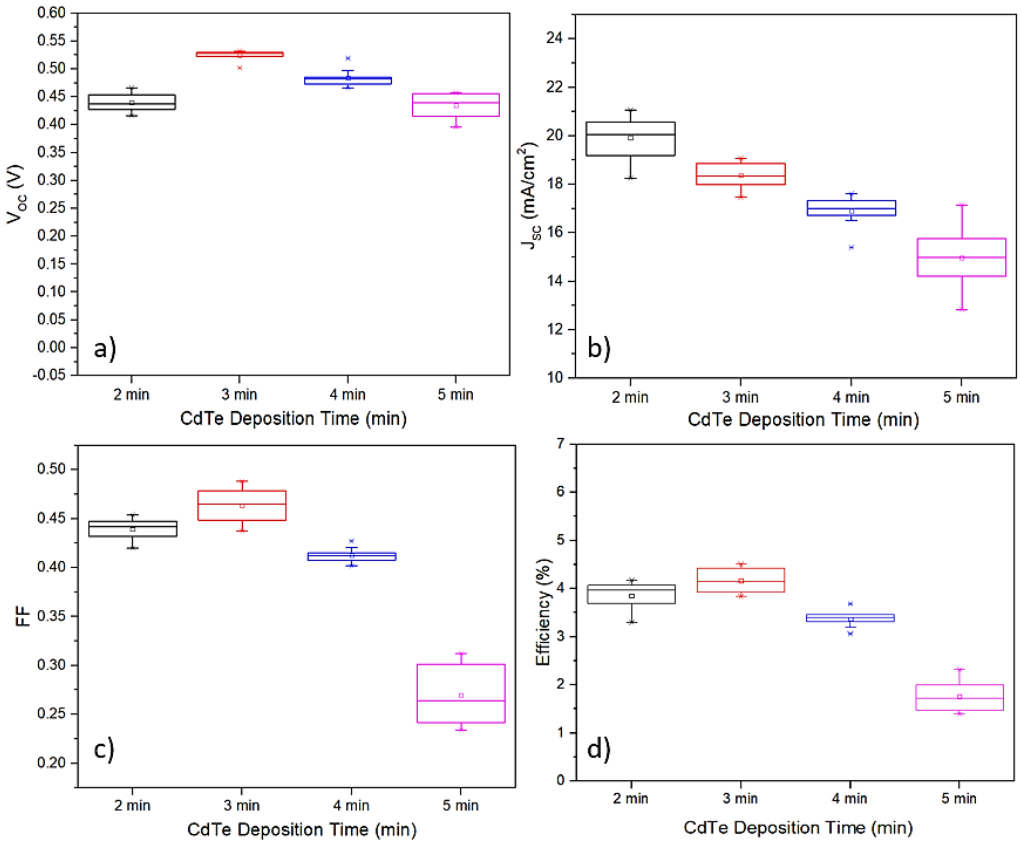


Fig. 6.8: Boxplots of a) V_{OC}, b) J_{SC}, c) FF and d) efficiency of substrate devices with different CdTe deposition times.

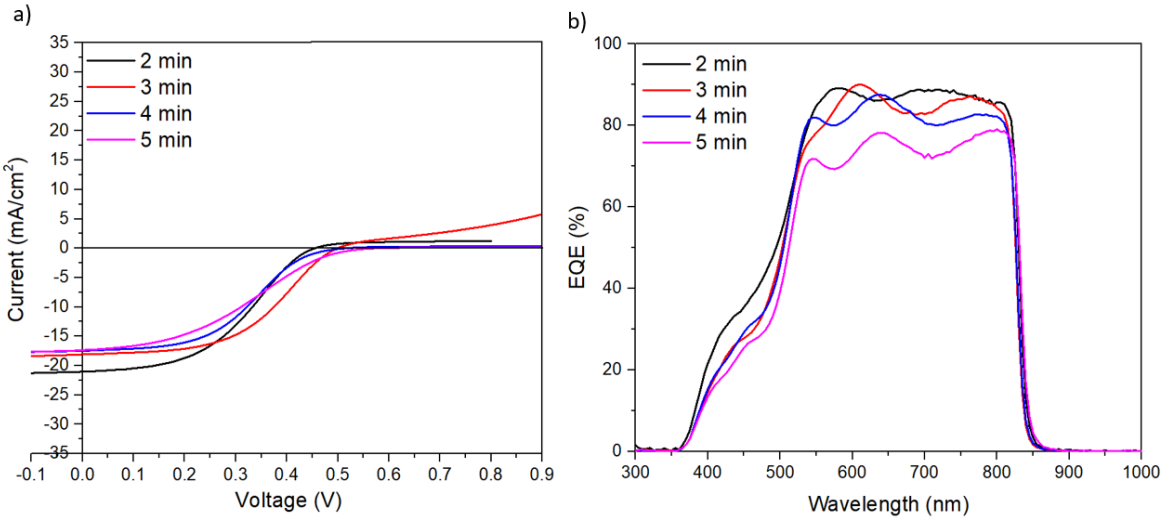


Fig. 6.9: a) J-V curves and b) EQE of best cells of CdTe substrate devices with different absorber deposition times.

Fig.6.9.a shows the J-V curves and EQE response on the best devices for each CdTe deposition duration. The J-V curves follow the results discussed earlier,

where the optimum CdTe thickness was found to be ~ 4.4 µm (3-minute deposition). The EQE (*Fig. 6.9.b*) shows a uniform progressive reduction in the range between 500 nm and 850 nm with increasing absorber thickness which confirms the J_{SC} reduction observed earlier. This can be attributed to the effectiveness of the $CdCl_2$ activation treatment with increasing CdTe thickness [19]. Since the $CdCl_2$ has not been reoptimized to account for the varying thickness of the absorber poor passivation of the grain boundaries leads to greater recombination losses limiting the device performance. However, the optimisation of the $CdCl_2$ activation treatment was outside of the scope of this study and further research needs to be undertaken for future efficiency improvements. The 3-minute CdTe deposition device was selected as the baseline process for future work. All the performance parameters of the investigated devices are summarised in *Table 6.4*.

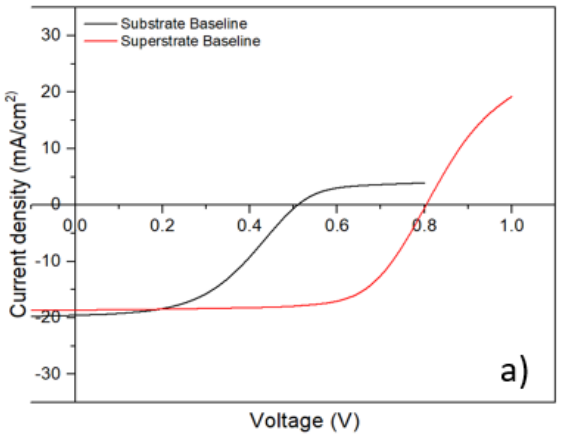
Table 6.4: Summary of performnce parameters of CdTe substrate solar cells with different absorber thicknes.

CdTe Deposition Time (Min)	*Thickness (µm)*	*V_{OC} (mV)*	*J_{SC} (mA/cm²)*	*FF (%)*	*η (%)*
2	2.6	456	21.0	43.5	4.2
3	4.4	528	17.7	48.3	4.5
4	7.5	519	16.9	41.0	3.6
5	9.3	453	17.3	29.7	2.3

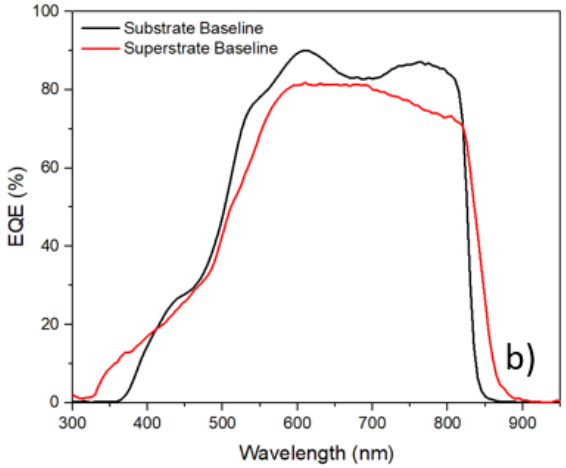
6.3.3 Substrate and superstrate configuration comparison

As previously mentioned, for this investigation it was important to minimise interdiffusion between CdS and CdTe to be able to isolate potential effects of the absorber/back-contact interface. *Fig.6.10* show a comparison between the J-V curves, EQE spectra and the bandgaps of champion cells for substrate and superstrate reference baselines. It is observed that substrate devices suffer a significant lower performance due to lower V_{OC} and FF. Additionally, the roll-

over effect is more pronounced in substrate than superstrate configuration (*Fig. 6.10.a*). This is attributed to the formation of a large Schottky barrier, which limits the V_{OC} exhibited in these devices. Consequently, the identification of back contact effects on device performance were more noticeable in this device structure. When compared, the substrate device exhibits higher J_{SC} (1 mA/cm^2). This is confirmed by the EQE, where the substrate configuration device showed superior response in the approximate range between 500 and 800 nm. This is attributed to reduced optical losses, where incident light does not need to pass through the glass substrate to reach the absorber. However, in the range between 830 and 870 nm the superstrate device exhibits better EQE. This originates from the formation of the $CdTe_{1-x}S_x$ ternary compound due to the CdS/CdTe interdiffusion process [20]. Interdiffusion is responsible for shifting the bandgap to longer wavelengths by narrowing the absorber layer bandgap, this effect is illustrated in *Fig. 6.10.d*. The superstrate configuration device exhibits a bandgap of ~ 1.46 eV which is associated with $CdTe_{1-x}S_x$ [2], while the substrate configuration device exhibits a bandgap of ~ 1.49 eV, a value much closer to the CdTe bandgap indicating limited interdiffusion between CdS and CdTe. The fact that interdiffusion is limited in substrate configuration, enables the investigation of the back-contact interface without any masking effects from other interfaces.



Parameter	Substrate	Superstrate
V_{OC} (mV)	510	804
J_{SC} (mA/cm^2)	19.5	18.63
FF (%)	47.5	69.0
η (%)	4.73	10.3



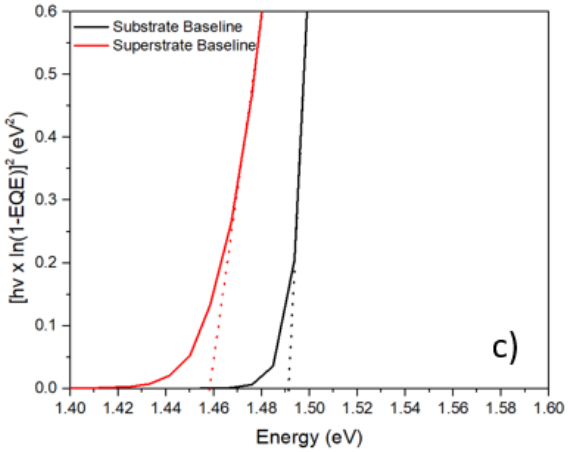


Fig. 6.10: Comparison between substrate and superstrate basleline processes, a) J-V curve, b) EQE spectra and c) exrapolated E_g. The table summarises the performance indicators between the two devices.

6.3.4 MoO_x as back contact barrier for CdTe substrate solar cells

Fig. 6.11.a shows the deposition rate as a function of O_2 concentration of MoO_x thin films. It was found that the deposition rate in the range investigated, can be divided in two regions. In region A, the deposition rate increases with increasing O_2 concentration up to 24.5% O_2 in Ar. Further increase of O_2 lead to a rapid decrease of the deposition rate, resulting in thinner MoOx thin films (region b). Similar behaviour was also reported by J. Scaraminio et al. [21] and can be attributed to target poisoning.

Transmission measurements (*Fig. 6.11.b*) showed a progressive increase in transparency of MoO_x thin films with O_2 concentrations. It was also found that there is an exponential relationship between average transmission (*Fig. 6.11.c*)

and O_2 concentration during MoO_x deposition. For O_2 concentration up to 20%, the average transmission was below 10% while for O_2 concentration above 20%, the average transmission rapidly increased up to 80%. The optical bandgap (E_g) was extrapolated using Tauc plots. In literature, the E_g for MoO_x was found to show both indirect and direct transitions, depending on the Mo oxidation state and film crystallinity [17][22]. For this reason, E_g extrapolation was carried out assuming both indirect and direct band transitions ($\alpha h\nu^n$ *vs* $h\nu$), where n is assumed to be 0.5 for indirect and 2 for direct transition respectively. E_g strongly depended on O_2 concentration during RF sputtering. For both, direct and indirect transitions (*Fig. 6.11.d*) the E_g increased with increasing O_2. However, only in the case when an indirect transition was assumed, the results were in good agreement with reported known values (2.4 to 3.2 eV) [21][17][23]. The increase in optical bandgap can be attributed to the increase in Mo oxidisation [24]. XRD analysis (*Fig. 6.11.d*) showed that the MoO_x RF sputtered deposited thin films exhibited an amorphous structure with only a broad peak at ~ 26 °, again in good agreement with literature [17][23][25]. The Mo film deposited without any oxygen showed a dominant peak at 40.5 ° corresponding to the (110) preferred orientation in the Mo cubic crystal structure according to JCPDS 3-065-7442 card.

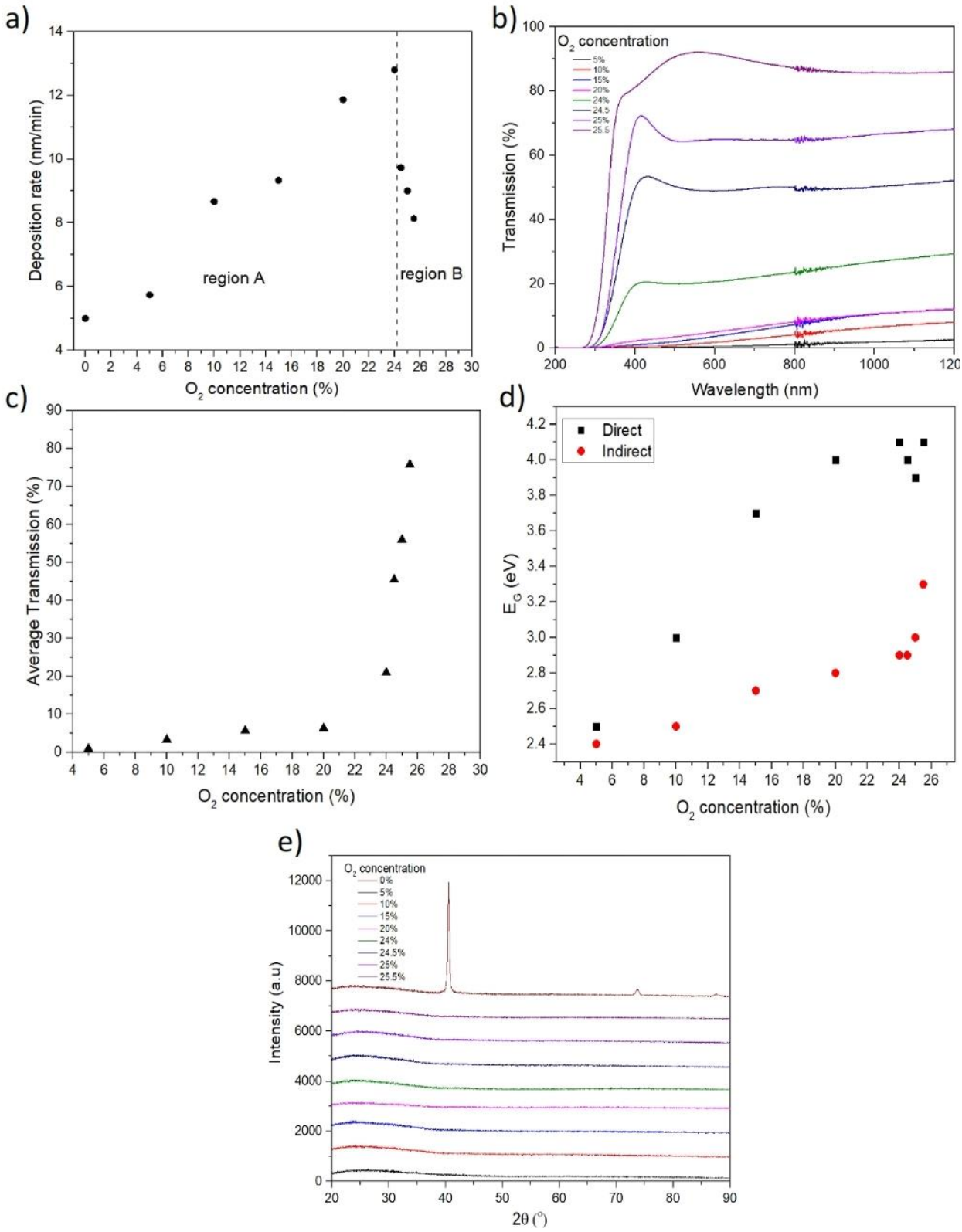


Fig. 6.11: a) Deposition rate, b) transmission curves, c) average transmission, d) extrapolated E_g and e) XRD of MoO_x thin films with different O_2 concentrations during RF sputtering.

Hall effect measurements were carried out on the investigated MoO_x thin films to determine the effect of O_2 on the resistivity and carrier concentration. As mentioned in *Chapter 1*, the depletion width of the back-contact barrier strongly depends on the absorber doping density. A highly p-type doped semiconductor will yield a narrow depletion width (W_a) allowing tunnelling of carriers through the back-contact barrier. For MoO_x to act as a tunnelling junction between Mo and CdTe, it is important for the carrier concentration to be in the range between CdTe and Mo (~10^{16} -10^{18} cm^{-3}). *Fig.6.12* shows the progressive increase of resistivity with increasing O_2 percentage during RF sputtering. Resistivity was found to remain below 10^{-2} Ω.cm for oxygen concentrations up to 24%. Further increase in O_2 resulted in a rapid increase of resistivity up to 10^3 Ω.cm (thin film with 25% O_2). Thin films produced with more than 25% O_2, were found to be completely insulating. It was reported that MoO_2 provides conductive films, while thin film transition to MoO_3 provides high resistivity films [26]. This is attributed to the decrease in oxygen vacancies in the thin films when transitioning from MoO_2 to MoO_3 [27]. Likewise, MoO_x deposited thin films showed metallic carrier concentrations (range of 10^{22} cm^{-3}) up to 24% O_2. Further increase in O_2 resulted to a progressive decrease in carrier concentrations down to 10^{16} cm^{-3}, which again was exhibited at 25% O_2.

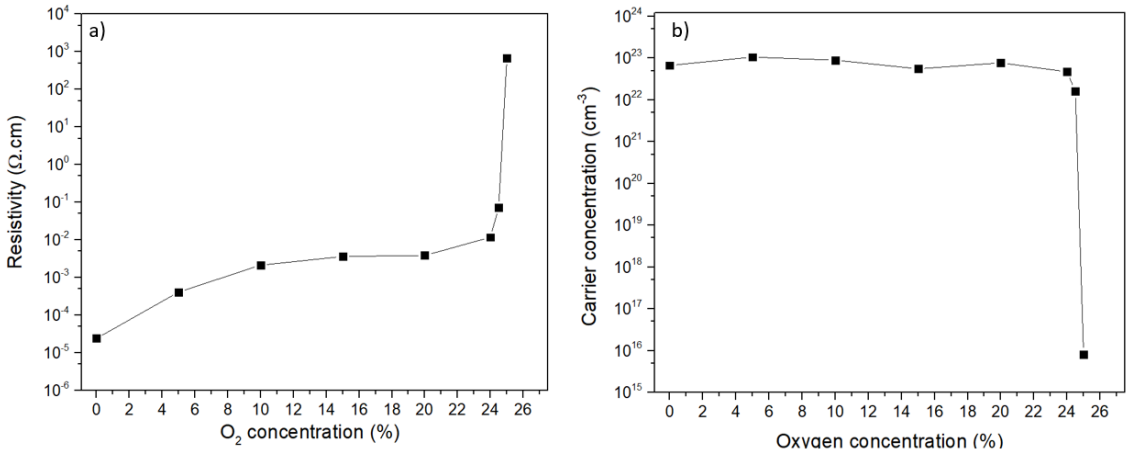


Fig. 6.12: a) Resistivity and b) carrier concentration of MoO_x thin films with different O_2 concentrations during RF sputtering.

These results, in combination with the transmission and bandgap measurements suggest that RF sputtering from a metallic target with O_2 concentrations up to 24%, is likely to promote the deposition of the metallic MoO_2 thin films. These thin films exhibit lower transmission, narrower bandgap values, and metallic resistivity and carrier concentrations. Thin films deposited at O_2 concentrations more than 24% are likely to transition to MoO_3, which exhibit higher transmission, wider bandgap and highly resistive films. However, since the MoO_x composition could not be directly measured, this remains a speculation and further research needs to be carried out in this direction.

To evaluate the effect of MoO_x back contact buffer on substrate CdTe solar cells, devices with 24%, 24.5%, 25% and 25.5% were completed and compared with the baseline process. This range was decided in order for devices to reflect both the metallic, semi-metallic and insulating doping densities exhibited from these films.

Fig.6.13 shows the boxplots of all the performance indicators of substrate devices with MoO_x as back contact buffer layer. V_{OC} (*Fig. 6.13.a*) was found to progressively increase with increasing O_2 concentrations up to 25% of O_2 during deposition. The average V_{OC} has increased from 530mV to 580 mV when devices with 0% and 25% O_2 containing buffer layers are compared. The device with 25.5% MoO_x buffer showed a significant average V_{OC} loss of ~ 70 mV. For devices up to 24.5% O_2, J_{SC} exhibited a slight decrease (*Fig. 6.13.b*), which can be attributed to back surface recombination losses due to the increased resistivity of the MoOx thin films when compared with pure Mo. However, the device with 25% O_2 exhibited the highest average J_{SC} (17.5 mA/cm^{-2}), while presenting higher thin film resistivity. This effect suggests better carrier transport to the back electrode. The highest average FF (*Fig.6.13.c*) was exhibited from the device with the buffer deposited at 25% O_2 and it was found to be significantly higher than the baseline process (~7% difference). All the other devices with MoO_x buffer layers showed average FF values lower than the baseline process.

Since the device with 25% O_2 deposited MoO_x back contact buffer layer, exhibited the highest V_{OC}, J_{SC} and FF, the average achieved efficiency was found

to be ~ 1% more than the baseline process (4.2%). This effect is most likely attributed to the narrowing of the back-contact barrier depletion width which could lead in the formation of a tunnelling junction between CdTe and Mo. This may explain the increase in V_{OC}, FF and J_{SC} observed, since the barrier would not impede majority carrier transport to Mo. Devices with MoO_x buffer layers with lower or higher O_2 concentrations than 25% exhibited efficiencies lower that the baseline process because of reduced J_{SC} and FF. This is likely attributed to the metallic behaviour of MoO_x thin films which was exhibited at lower O_2 concentrations and the low doping densities of MoO_x of thin films deposited at higher O_2 concentrations. Metallic MoO_2 exhibits high doping densities (~10^{22} cm^{-3}), which leads to the formation of a large back contact depletion width between CdTe and MoO_x (similar to the case with Mo). Transitioning from metallic MoO_X phase to a semi-metallic MoO_X phase could lead to a beneficial situation where the MoO_x acts as moderately doped buffer layer creating a tunnelling junction between CdTe and Mo. However, further increase of O_2 concentrations produces highly resistive films with very low doping densities (which could not be measured in this Hall system) causing the collapse of the V_{OC} and FF. The proposed mechanism could explain the behaviour observed by these devices, however performance improvements could also arise from lowering the back-contact barrier height or by O_2 induced doping. MoO_3 was found to exhibit high work functions up to 6.8 eV [16] and recently Gretener et al argued that MoO_x performance improvements in V_{OC} and FF could arise from doping the CdTe back surface [25]. O_2 induced doping could arise from the transfer of oxygen from MoO_3 to CdTe increasing the back-surface doping of the absorber [27]. For better understanding of these mechanisms further research is required in this direction.

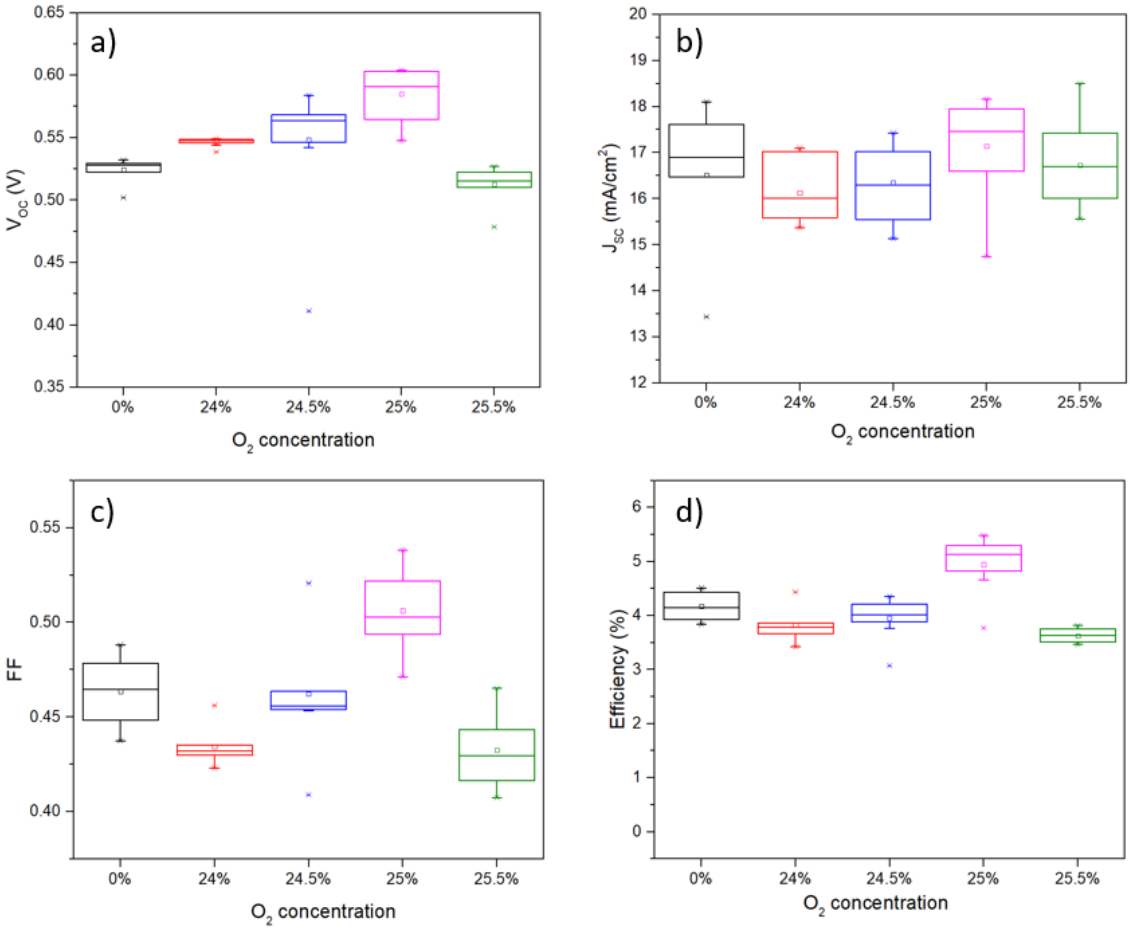


Fig. 6.13: Boxplots of a) V_{OC}, b) J_{SC}, c) FF and d) efficiency of substrate devices with different O_2 concentrations of MoO_x buffer layers for the back-contact.

6.4 Concluding remarks

In conclusion, the aim of this chapter was the interface optimisation of the absorber/back-contact interface. The first part focused on the role of Cu on the performance, controllability and stability of non-etched CdTe solar cells. The second part of this chapter described the implementation of a new baseline process, based on substrate configuration of CdS/CdTe devices. The achieved baseline was used for the investigation of a Cu-free back contact, based on transitional metal oxides (TMO's) and specifically MoO_x.

Introduction of Cu at the back contact, was found to induce a moderately doped surface which creates a tunnelling junction. This did not affect the barrier height, however the back-contact Schottky diode depletion width decreased. Reducing the width allowed the majority carriers to tunnel through the barrier and transported effectively to the back electrode translating in improvements in V_{OC} and FF. Additionally, it was shown that performing a surface modification step prior to back contact deposition is not necessary. Intrinsic V_{Cd}'s inside the CdTe were sufficient to form enough Cu_{Cd} substitutional acceptors and induce a tunnelling junction at the back-contact achieving a maximum efficiency of 11.8%. However, it was shown that significant degradation still occurred in non-etched Cu-contacted devices. Limiting the formation of $Cu_{2-x}Te$ bonds by not performing a surface modification step to control did not prevent device degradation. This investigation suggests that Cu diffusion is not limited to devices that have been subjected in thermal or light stresses. The investigated Cu devices were prone to degradation even though they were kept in the dark for 150 days while there was a negligible degradation of the non-Cu contacted device. This is indicative that Cu migration is caused not only by stress but also due to the highly diffusive nature of Cu in CdTe and weak Cu bonds which can easily dissociate at room temperature. It can only be safely assumed that when these devices are subjected to thermal or light stresses, further degradation is to be expected. The natural progression here would be to dope CdTe with other elements, which was not able to be shown here. Recent research showed that elements such as Se, As, Sb and Ph could be

incorporated in the device structure and further increase the performance of CdTe solar cells.

A repeatable baseline process for CdTe solar cells in substrate configuration was realised for the investigation of the absorber/back-contact interface. The optimum CdTe thickness of closed devices was found to be ~ 4 µm, with an average efficiency of 4.3%. The measured absorber E_g of devices was found to be 1.49 eV, suggesting that interdiffusion between CdS and CdTe is limited. This effect, and the fact that back-contact surface modification with traditional methods such as etching is impossible, made the effects of the back contact more pronounced. Future improvements of the substrate baseline process could arise from further optimisation of the $CdCl_2$ treatment, and through absorber/emitter band alignment engineering. Specifically, the utilisation of alternative buffer materials acting as emitters such as ZnO or MZO could provide an alternative to the traditional CdS structure.

MoO_x was found to be a promising candidate as a back-contact buffer layer for the formation of an ohmic contact. RF sputtered MoOx films showed that thin film properties strongly depend on O_2 concentrations during film deposition. Increasing O_2 concentration increased the transparency and widen the E_g of films. Resistivity and carrier concentration measurements of MoO_x films showed a sharp transition at ~ 24.5% O_2 concentration from metallic to semi-metallic/insulating thin film properties. This is most likely the transition between MoO_2 to MoO_3. Finished devices showed the best device performance at 25% O_2 concentration with average efficiencies of ~ 5.5%. This was most likely caused by either the narrowing of the barrier's depletion width and/or the reduction of the Schottky barrier height. However, this remains a speculation and further research is needed in this direction. Devices showed a progressive increase of V_{OC} with O_2 concentrations up to 25% of O_2 in Ar. However, when compared with the baseline process, FF and J_{SC} appear to be lower at O_2 concentrations below and above 25%. This was likely attributed to the metallic behaviour of MoO_x thin films which was exhibited at lower O_2 concentrations and the high resistivity MoO_x of thin films with low doping densities, deposited at higher O_2 concentrations.

However, the role of O_2 during RF sputter deposition of MoO_x films and the effects on device performance are not entirely understood and further research is needed in this direction. Additionally, temperature and pressure are equally important parameters during RF sputtering which could significantly change the electrical, morphological and optical properties of MoO_x films. The investigation of these parameters could provide further efficiency improvements in CdS/CdTe substrate devices.

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Chapter 7. Conclusion

CdTe solar cells are currently the most commercially successful thin film technology which have secured approximately half of the thin film market share. In recent years, technology developments from extensive research in the field have improved the financial competitiveness with conventional power generation technologies. Efficiency improvements were mainly achieved through laboratory scale advances and growing understanding of the materials used. However, CdTe solar cells have only reached 70% of their theoretical maximum efficiency. Interface engineering and optimisation is one of the techniques that can further aid in the quest for efficiency improvements and financial viability of this technology.

This thesis focused on possible ways of improving the performance of CdTe solar cells through interface optimisation. Specifically, interface optimisation was divided into three parts: absorber/emitter, window/emitter and absorber/back contact interface.

Initially, a repeatable baseline process was presented, which enabled further investigation of interface optimisation through comparative studies. This was the first baseline process for CdTe solar cells achieved in CREST which was enabled through the design and implementation of a bespoke CSS system. CdTe source preparation showed that compacting and baking the CdTe powder (sintering) as well as etching the source plate's quartz substrate, prior to source plate fabrication, increased the sublimation rates and improved the adhesion of the CdTe for subsequent thin film depositions. Device optimisation showed that the addition of O_2 during CSS was beneficial for the device performance. O_2 was found to prevent total consumption of the CdS layer by reducing sulphur diffusion through grain boundaries. It also acts as a nucleation aid when introduced during CdTe sublimation leading to homogeneous films.

$CdCl_2$ activation treatment optimisation showed that the electrical performance is interlinked with the amount of evaporated $CdCl_2$ used during the activation process of the device. PL imaging was demonstrated to be a useful

non-contact technique which can qualitatively identify the presence of Cl inside the CdS layer due to formation of $(V_{Cd}Cl_S)^{\cdot}$ + Cl_S^{+} complexes and provide qualitative information about the uniformity and the effectiveness of the $CdCl_2$ treatment on CdS/CdTe devices.

Absorber/emitter interface optimisation included the addition of Cl compounds during the CdS chemical bath. Cl compounds such as $CdCl_2$ during CdS chemical bath deposition were found to act as a doping mechanism for CdS thin films and enhance the V_{OC} and the FF through reduced interface recombination. This was achieved by reducing the amount of available V_{Cd} which usually forms acceptor centers, contributing to self-compensation of carriers inside the CdS and S substitution with Cl, inducing a larger absorber inversion at CdS/CdTe interface. Results were verified through modelling of the baseline process. The optimum $ClCl_2$ concentration during the CdS chemical bath deposition was found to be 7.29 mM which provided an average performance of 10.4%. CdS doping in this thesis focused on substitution of the S site with Cl. Investigation of other materials for CdS doping during CdS could be explored for further efficiency improvements. Group III elements such as Ga and Al could be used as dopants to substitute the Cd site during CdS deposition.

Other aspects of the absorber/emitter interface optimisation included the investigation of the effect of the cooling cycle during the $CdCl_2$ activation treatment. It was concluded that the cooling cycle strongly affects the formation of self-compensating defects which can lead to recombination of carriers either in CdTe or in CdS. At high cooling down temperatures, not enough Cl is able to reach the CdS layer, this leads to a reduction in V_{OC} and was attributed to the presence of high number of V_{Cd} acceptor centers inside the CdS layer. At lower cooling temperatures there is a decrease in the net acceptor densities which cause the degradation of the V_{OC} due to the formation of Cl_{Te} compensating donors. The optimum temperature range during the cooling cycle of the activation treatment was between 300℃ and 250℃. The best performance was 10.3% at 300℃ cooling temperature.

The window/emitter interface optimisation focused on improving the J_{SC} of CdTe devices. Experiments focussed on the effects of reducing the CdS

thickness, the effects of adding a high resistive transparent layer (HRT) in the CdS/CdTe structure and their possible utilisation as alternative emitters for CdTe devices. Reducing the thickness of the CdS did not improve the J_{SC} and caused either partial or total consumption of the emitter (CdS) by the absorber (CdTe). This resulted in lower performance of devices with significant drop in V_{OC} and FF.

SnO_2 introduction as an HRT buffer allowed the reduction of CdS film. This resulted in the increase of both the J_{SC} and V_{OC} without the formation of shunt paths. Devices with efficiencies of ~ 12% were achieved. However, despite the performance improvements, the CdS buffer still presents a significant loss of photogenerated carriers through absorption.

It was successfully demonstrated that it is possible to utilise HRT layers as alternative emitters. However, not all HRT's proved suitable alternatives. SCAPS 1D band diagram simulations showed that SnO_2 based HRT's can suffer from an unfavourable band alignment (cliff) with CdTe, resulting in low V_{OC} due to increased interface recombination. This was also demonstrated by the low performance exhibited from devices with SnO_2 buffer layers. ZnO buffer layers proved to be a more suitable candidate for CdS buffer substitution. Due to the formation of a zero-conduction band offset (flat) with CdTe, ZnO/CdTe devices could retain most of the V_{OC} compared to CdS/CdTe and improve the J_{SC} due to less absorption of photogenerated carriers leading to performance improvements. ZnO is a well-known material with extensive use as an HRT layer in both CIGS and CdTe devices, however most of the existing research was concentrated on the utilisation of this layer as an HRT and not as the emitter of the device. Further investigations could be conducted around the optimisation of ZnO sputter deposition acting as the emitter. Specifically, tuning some of its characteristics during deposition, could benefit band alignment with CdTe and provide further performance improvements.

Absorber/back-contact interface optimisation focused on the role of Cu on the performance, controllability and stability of non-etched CdTe solar cells. Introduction of Cu at the back contact, didn't affect the schottky barrier height, suggesting that performance improvements were more likely caused from a

reduction of the back contacts barrier width due to Cu doping. This allowed the majority carriers to tunnel through the barrier and transported effectively to the back electrode resulting in significant improvements in V_{OC} and FF. Additionally, it was shown that performing a surface modification step prior to back contact deposition is not necessary. Intrinsic V_{Cd}'s inside the CdTe were sufficient to form enough Cu_{Cd} substitutional acceptors and induce a tunnelling junction at the back-contact achieving a maximum efficiency of 11.8% for devices with 100Å of evaporated Cu. However, significant degradation was found in devices with Cu doping after kept 150 days in the dark. This demonstrated the highly diffusive nature of Cu in CdTe, which can be attributed to weak Cu bonds that can easily dissociate at room temperature. The natural progression here would be to dope CdTe with other elements, which was not able to be shown here. Recent research showed that elements such as Se, As, Sb and Ph could be incorporated in the device structure and further increase the performance of CdTe solar cells.

Finally, absorber/back contact interface optimisation included the investigation of a Cu-free back contact, based on transitional metal oxides (TMO's) and specifically MoO_x. This was investigated through the implementation of a new baseline process based on substrate configuration of CdS/CdTe. MoO_x as a Cu-free back contact has presented encouraging initial results improving the performance of devices from ~4.3% to ~5.5%. This remarkable increase was achieved mainly through an increase in V_{OC} and was most likely caused by either the narrowing of the barrier's width and/or by a reduction of the schottky barrier height. However, the role of O_2 during RF sputter deposition of MoO_x films and the effects on device performance are not entirely understood and further research is needed in this direction. Specifically, films showed that optical and electrical properties strongly depend on O_2 concentrations during film deposition. MoO_x films with varying O_2 concentrations at room temperature showed a transition from metallic to semi-metallic/insulating thin film properties which could be attributed to different MoO_x oxidation states. Temperature and pressure are equally important parameters during RF sputtering which could significantly change the

electrical, morphological and optical properties of MoO_x films. The investigation of these parameters could provide further efficiency improvements in CdS/CdTe substrate devices.