Layer by Layer Printing of Nanomaterials for Large-Area, Flexible Electronics

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Abstract

Large-area electronics, including printable and flexible electronics, is an emerging concept which aims to develop electronic components in a cheaper and faster manner, especially on those non-conventional substrates. Being flexible and deformable, this new form of electronics is regarded to hold great promises for various futuristic applications including the internet of things, virtual reality, healthcare monitoring, prosthetics and robotics. However, at present, large-area electronics is still nowhere near the commercialisation stage, which is due to several problems associated with performance, uniformity and reliability, etc. Moreover, although the device's density is not the major concern in printed electronics, there is still a merit in further increasing the total number of devices in a limited area, in order to achieve more electronic blocks, higher performance and multiple functionalities.

In this context, this Ph.D. thesis focuses on the printing of various nanomaterials for the realisation of high-performance, flexible and large-area electronics. Several aspects have been covered in this thesis, including the printing dynamics of quasi-1D NWs, the contact problem in device realisation and the strategy to achieve sequential integration (3D integration) of the as-printed devices, both on rigid and flexible substrates. Promisingly, some of the devices based on the printed nanomaterial show a comparable performance to the state-of-the-art technology. With the demonstrated 3D integration strategy, a highly dense array of electronic devices can be potentially achieved by printing method.

This thesis also touches on the problem associated with the circuit and system realisation. Specifically, graphene-based logic gates and NW based UV sensing circuit has been discussed, which shows the promising applications of nanomaterial-based electronics. Future work will be focusing on extending the UV sensing circuit to an active matrix sensor array.

List of Publication

Selected portions of work discussed in this thesis are published or under preparation for publication as listed below.

Journal Articles

1) van der Waals Contact Engineering of Graphene Field-Effect Transistors for Large-Area Flexible Electronics
   F. Liu, W. T. Navaraj, N. Yogeswaran, D. H. Gregory, R. Dahiya
   ACS Nano, 13 (3), 3257-3268 (2019)
2) Heterogeneous Integration of Contact-Printed Semiconductor Nanowires for High-Performance Devices on Large Areas
   C. G. Núñez, **F. Liu**, W. T. Navaraj, A. Christou, D. Shakthivel, R Dahiya
   Microsystems & Nanoengineering 4 (1), 22 (2018)
3) Ultra-Flexible, Printed Active Matrix for Wearable UV Sensor Array (under preparation)

Conference Proceedings

1) Flexible Logic Circuits by using Van Der Waals Contacted Graphene Field-Effect Transistors
   F. Liu, N. Yogeswaran, W. Navaraj, R. Dahiya
   In ***IEEE International Symposium on Circuits and Systems (ISCAS)***, 1-5 (2019)
2) 3D Integrated Electronics with Layer by Layer Printing of NWs
   F. Liu, A. Christou, R. Dahiya
   In ***IEEE International Conference on Flexible and Printable Sensors and Systems (FLEPS)*** (2019)

Book and Monograph

1) Integration Techniques for Micro/Nanostructure-Based Large-Area Electronics
   C. G. Núñez, **F. Liu**, S. Xu, R. Dahiya
   Cambridge University Press (2018)

Papers which are linked to the overall project but beyond the scope of this thesis are listed below:

Journal Articles

1) Large-Area Soft ESkin: The Challenges beyond Sensor Designs.
   R. Dahiya, N. Yogeswaran, **F. Liu**, L. Manjakkal, E. Burdet, V. Hayward, H. Jörntell
   Proceedings of the IEEE (in press)
2) Large-Area Self-Assembly of Silica Microspheres/Nanospheres by Temperature-Assisted Dip-Coating
   C. G. Núñez, W. T. Navaraj, F. Liu, D. Shakthivel, R. Dahiya
   ACS Applied Materials & Interfaces 10 (3), 3058-3068 (2018)
3) ZnO Nanowires-Based Flexible UV Photodetector System for Wearable Dosimetry
   C. G. Núñez, A. Vilouras, W. T. Navaraj, **F. Liu**, R Dahiya
   IEEE Sensors Journal 18 (19), 7881-7888 (2018)
4) Piezoelectric Graphene Field Effect Transistor Pressure Sensors for Tactile Sensing
   N. Yogeswaran, W. T. Navaraj, S. Gupta, F. Liu, V. Vinciguerra, L. Lorenzelli, R. Dahiya
   Applied Physics Letters 113 (1), 014102 (2018)

Conference Proceedings

1) Graphene-ZnO NWs Hybrid Film for Lrge-Area UV Photodetector
   F. Liu, N. Yogeswaran, W. Navaraj, R. Dahiya
   In ***IEEE Sensors Conference*** (2018)
2) Contact-Printing of Zinc Oxide Nanowires for Chemical Sensing Applications
   C. G. Núñez, L. Manjakkal, **F. Liu**, R Dahiya
   In ***IEEE Sensors Conference*** (2018)
3) Transforming the Short-Term Sensing Stimuli to Long-Term E-skin Memory
   F. Liu, W. Taube, N. Yogeswaran, D. Gregory, R. Dahiya
   In ***IEEE Sensors Conference*** (2017)
4) ZnO Nanowires based Flexible UV Photodetectors for Wearable Dosimetry
   C. G. Nunez, W. Taube, **F. Liu**, R. Dahiya
   In ***IEEE Sensors Conference*** (2017)
5) Nanomaterials Processing for Flexible Electronics

D Shakthivel, F Liu, CG Núñez, W Taube, R Dahiya

In ***IEEE 26th International Symposium on Industrial Electronics (ISIE)*** (2017)

6) Towards Flexible Magnetoelectronics for Robotic Applications

   H. Heidari, **F. Liu**, R Dahiya

   In ***2nd Asia-Pacific Conference on Intelligent Robot Systems (ACIRS)***, 295-298 (2017)

7) Modelling of Nanowire FETs based Neural Network for Tactile Pattern Recognition in E-Skin

   W. Taube, **F. Liu**, A. Vilouras, D. Shaktivel, C. G. Nunez, H. Heidari, F. Labeau, D. Gregory, R. Dahiya

   In ***IEEE Biomedical Circuits and Systems Conference (BioCAS)***, 572-575 (2016)

This dissertation is dedicated to my family, friends and those people who have helped and supported me in the past.

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Author’s Declaration

I, Fengyuan Liu, hereby declare that except where explicitly reference is made to the contribution of others, this thesis is the result of the work of the named and has not been submitted for any other degree at the University of Glasgow or any other institution.

Definitions/Abbreviations

1D: one-dimensional

1T1S: one transistor-one sensor

2D: two-dimensional

2T: two-terminal

3D: three-dimensional

3D WLP: 3D wafer-level packaging

3D-SICs: 3D stacked ICs

3D SIP: 3D system in package

4T: four-terminal

AFM: atomic-force microscope

ALD: atomic layer deposition

CMOS: Complementary-Metal-Oxide-Semiconductor

CMP: chemical mechanical polishing

CNT: carbon nanotube

ConH: contact height

ConL: contact length

CV: capacitance-voltage

CVD: chemical vapour deposition

CVT: chemical vapour transport

DTBDT-C6: dithieno[2,3-d;2′,3′-d′]benzo[1,2-b;4,5-b′]dithiophene

DOS: density of states

Ebeam: electron-beam

EBL: electron beam lithography

FET: field-effect transistor

GFET: graphene based field-effect transistor

IC: integrated circuit

IV: current-voltage

LED: light-emitting diode

NT: nanotube

NW: nanowire

OFET: organic field-effect transistor

PCDTBT:PCBM: poly[N-9-heptadecanyl-2,7-carbazole-alt-5,5-(4′,7′-di-2-thieny-2′,1′,3′-benzothiadiazole)]:[6,6]-phenyl-C71-butyric acid methyl ester

PECVD: plasma enhanced chemical vapour deposition

PEDOT:PSS: poly (3,4-ethylenedioxythiophene) polystyrene sulfonate

PI: polyimide

PMMA: Poly (methyl methacrylate)

P(NDI2OD-T2): poly{[N,N′-bis(2-octyldodecyl)naphthalene-1,4,5,8-bis(dicarboximide)-2,6-diyl]-alt-5,5′-(2,2′-bithiophene)}

PS: polystyrene

PVP: Poly(4-vinyl-phenol)

PUA: poly (urethaneacrylate)

RIE: reactive ion etching

RTA: rapid thermal annealing

SEM: scanning electron microscope

SOA: State of the art

TRL: transistor resistor logic

TSV: through silicon vias

UV: ultraviolet

h-BN: hexagonal boron nitride

diF-TES-ADT: 2,8-Difluoro-5,11-bis-(triethylsilylethynyl)anthradithiophene. TU-3 denotes benzobis(thiadiazole) derivative

vdW: van der Waals

1. Chapter 1. Introduction

The shrinking of the individual electronic device is expected to approach its physical limits in the very near future. The Moore's law, which provided a development roadmap for IC technology, is likely to lose its magic [1, 2]. In order to further advancing the development of IC technology, various solutions have been proposed including the use of 3D integration: a stack of electronic devices on different layers, unlike current CMOS technology, which arranges all the devices on the same plane, can further increases the device's density without tackling the barriers existing in the device miniaturisation. Another benefit of 3D integration of the devices is that the layout and interconnect of the circuit/system can be greatly simplified [3]. In general, the concept of realising electronics in a 3D manner is appealing and to meet this target various gaps need to be filled.

Meanwhile, large-area electronics, including flexible and printable electronics, is an emerging concept, which adopts a new way to make and use electronic devices and circuits [4]. Being flexible and printable, this can have applications in various aspects such as healthcare monitoring, the internet of things, robotics and prosthetics in a cost-effective manner, leading to a profound and revolutionary consequence to the daily life of people in the post-silicon era (see Figure 1.1) [5-8].

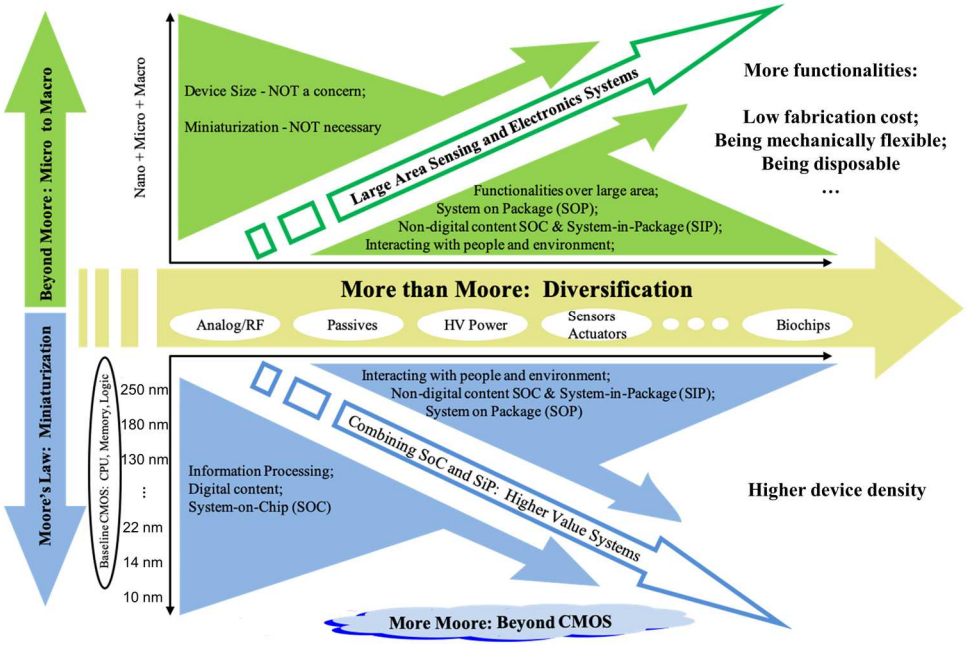


Figure 1.1: The schema showing the two possible roadmaps of electronics development, which can be classified as "More Moore" and "More than Moore".

While achieving a high device density is not the top priority in large-area electronics, merits still exist in utilizing the 3D integration strategy. For example, interconnects is studied to greatly limit the performance of an electronic system in terms of power consumption and signal delay [9]. And this aspect will become increasingly serious if various electronic systems with multiple functionalities are integrated together. The 3D integration, in the meanwhile, can greatly reduce the wiring length and increase the performance [3, 9]. Therefore, realising electronic components in a 3D manner by printing technology has its benefit and few studies have explored this direction.

This thesis aims to study the printing of various nanomaterials on flexible substrate and to further realising electronic devices and circuits in a 3D manner. Specifically, the objectives of this thesis can be summarised as follows:

a) To study the printing of nanomaterials including quasi-1D NWs and quasi-2D graphene, on both rigid and flexible substrates.
b) To realise functional devices and circuits from those printed nanomaterials, on both rigid and flexible substrates.
c) To realise the 3D stacking of these devices and circuits.

This thesis covers these aspects and is arranged into seven chapters. Meanwhile, during the development of 3D integrated electronics, some other meaningful results, such as the study on contact problem in printed electronics, were also obtained and detailed research into them was carried out. These studies were included in this thesis as well. Here, a brief description of the content of each chapter is given to provide some more detail about this Ph.D. thesis.

Chapter 2 presents an overview of the state of the art in printed and 3D integrated electronics. For this, various printing techniques are reviewed, including inkjet printing, screen printing, contact printing, transfer printing, and their roll-to-roll equivalents. A comparison between the listed printing techniques are made to highlight their advantages and disadvantages. Afterwards, the advances in 3D integration techniques are summarised, including a brief overview of 3D integration of chips and ultra-thin chips (parallel integration) and recently developed 3D printed devices and circuits (mainly sequential integration). A comparison between the listed works on 3D integrated electronics is made to highlight the advantages and disadvantages of the 3D integration by printing techniques.

Based on the literature review in Chapter 2, Chapter 3 explores and further advances the printing technology used in this thesis. This chapter is arranged in 3 sections. The first section (3.1) provides an in-depth study of the NW printing process. For this, a home-made contact

printing setup was realised with a close-loop control system, which enables precise control of the printing parameters including the printing pressure, the sliding speed and the sliding distance over the entire process. Afterwards, a data analysing method, which could extract the important figure of merits from the SEM images of printed NWs, is described and verified. This was achieved by slightly modifying a software (GTFiber) proposed in a previous work on organic fibres [10]. With these prerequisites, the NW printing mechanism is studied, clarifying the NW printing mechanism on flexible and uneven substrates. Section 3.2 presents a brief process flow for graphene transfer. The impact of extrinsic factors, such as solvent cleaning and rapid thermal annealing process is investigated. In Section 3.3, a study on screen printed Ag ink is presented. The influence of the processing parameters has been investigated. The study described in this chapter lays the foundation for later work presented in this thesis, which aims to realise a 3D integrated, flexible electronic system in a printable manner.

Chapter 4 discusses the contact problems in printed electronics. Unlike traditional CMOS technology where the contact is achieved by high temperature annealing and silicide formation, the contact obtained by printing methods are often weakly bonded with a vdW interaction. Such contacts can be achieved at low temperature (<150 °C), which is compatible with flexible substrate, but its contact quality is a major concern. In this regard, this section presents an experimental study of the vdW contact for various materials including graphene and ZnO NW. The experimental results show a completely different contact quality for these two materials: while a low contact resistance can be achieved between graphene and Au, the vdW contact appears to be unreliable for ZnO NWs, showing a Schottky type contact. A qualitative explanation has been proposed for this significant contrast. Next, effort has been made to further understand the graphene-Au vdW contact. Raman characterisation has been performed to reveal the mechanical properties of graphene-Au contact. A model proposed in previous studies have been adopted to determine the change of fermi level of graphene with respect to the change of graphene-Au separation [11]. A direct tunnelling equation has been utilised to calculate the vertical current in a uniformly biased graphene-Au junction. And this was further extended into a FET by combining with a modified resistor network model. The calculated results have been compared with the experimental data. Finally, the limitation of this theory has been indicated and future work following this direction has been discussed.

Chapter 5 discusses the realisation of flexible devices and circuits. This is discussed in various aspects including substrate preparation, contact strategy validation, dielectric material examination, device fabrication and circuit realisation. Specifically, flexible GFETs and ZnO

NW based UV photodetectors have been realised and characterised. The GFET is also used to realise logic circuits, which could potentially lead to flexible circuits over large area.

Chapter 6 discusses the realisation of 3D integrated electronics. For this, technical challenges in realising 3D integration is discussed in Section 6.1. Afterwards, two kinds of layout, which are Wheatstone bridge and 1 transistor-1 sensor (1T1S) structure based on printed NWs, have been discussed and realised in Section 6.2 and 6.3, respectively.

Chapter 7 concludes this thesis and indicated some future work which may be worth pursuing. The key findings in this thesis are summarised as follows:

a) A systematic study of NW printing mechanism on soft and uneven substrates has been carried out, which provides a preliminary guideline for NW printing on flexible substrates in a 3D manner.
b) In order to realise the study described in a), a user-friendly, home-made contact printing setup with close-loop control has been built, enabling the controllable and uniform NW printing over large-area.
c) Regarding the vdW contact between graphene and Au, before the study carried out in this thesis [12], no systematic investigation is available, and its nature is not clearly understood. The mainstream of the research in this field focuses on strategies of top-contact and edge contact. However, these two approaches have their benefits as well as drawbacks and they may not be so suitable for flexible electronics under the limitation of the thermal sensitive flexible substrate. For these reasons, a bottom contact method with a vdW graphene-Au interaction was adopted and systematically studied. An excellent contact performance has been achieved by engineering the graphene-Au vdW contact without the use of harsh thermal annealing. In addition, the vdW contact was realised on flexible substrate and its stability upon mechanical deformation was examined. Because of these benefits, a promising future is revealed to the long underestimated vdW contact.
d) A 3D integrated electronic system with a stack of transistors and sensors has been realised by using a layer-by-layer printing method.

Considering the key achievements listed here, this Ph. D. thesis may be of interest to a wide range of readers, including the researchers who work on 1D and 2D materials, printed and flexible electronics, etc.

2. Chapter 2. The State of the art in printed and 3D integrated electronics

This chapter presents an overview of the current state of the art in printed and 3D integrated electronics. It starts with a review of various mainstream printing techniques from both material and equipment perspectives, covering the electronic devices and circuits realised by inkjet printing, screen printing, contact printing, transfer printing, and their roll-to-roll equivalents. Then, a comparison is made between the listed printing techniques to highlight their advantages and limitations. The mainstream 3D integration technologies are described and reviewed, including parallel integration and sequential integration. Finally, the recent advances in 3D integration realised by printing technologies are summarised and compared, as these open up a new frontier in using printing technologies for large-area, high density, flexible electronics.

2.1 Printing technologies

In the film "Minority Report", people are reading newspapers on the subway. It is the year 2054 and the newspapers are not only 'papery', but also electronic: they are composed of a flexible display on the paper substrate and they can be bent, flexed and disposed of after reading. This is one example given by Prof. Zhenan Bao, when answering why and where flexible and disposable electronics are needed [13]. Researchers are currently working towards these aims, in which electronics are not realised on rigid substrates, but on flexible, stretchable, bio-compatible and even disposable platforms. The device size and density are not the primary concern for this new form of electronics. Instead those novel properties, such as bendability and disposability, take a greater priority. This innovation requires a change in fabrication technology. It should be cost-effective, realised under a low temperature and also capable of obtaining a high performance for various electronic applications.

One technology which potentially meets those requirements is printing. Unlike conventional micro-fabrication techniques which usually involve a high temperature process, printing can be realised at room temperature. Therefore, printing has been regarded as a promising approach to be used in flexible electronics, where most of the currently used deformable substrates are thermally sensitive. Various types of materials, including conductors, semiconductors and dielectrics, have been demonstrated to be achievable *via* printing [14], which has fostered the possibility of the realisation of all printed devices and circuits (see Subsection 2.1.4). This section aims to provide a general overview of printing technologies and is arranged as follows: first, typical donor materials of various bandgap have been summarised (Subsections 2.1.1 to

2.1.4). Then, several mainstream printing techniques for electronic applications have been reviewed with their advantages and challenges (Subsection 2.1.5). Finally, a comparison is made between the listed printing techniques (Subsection 2.1.5).

2.1.1 Conductors

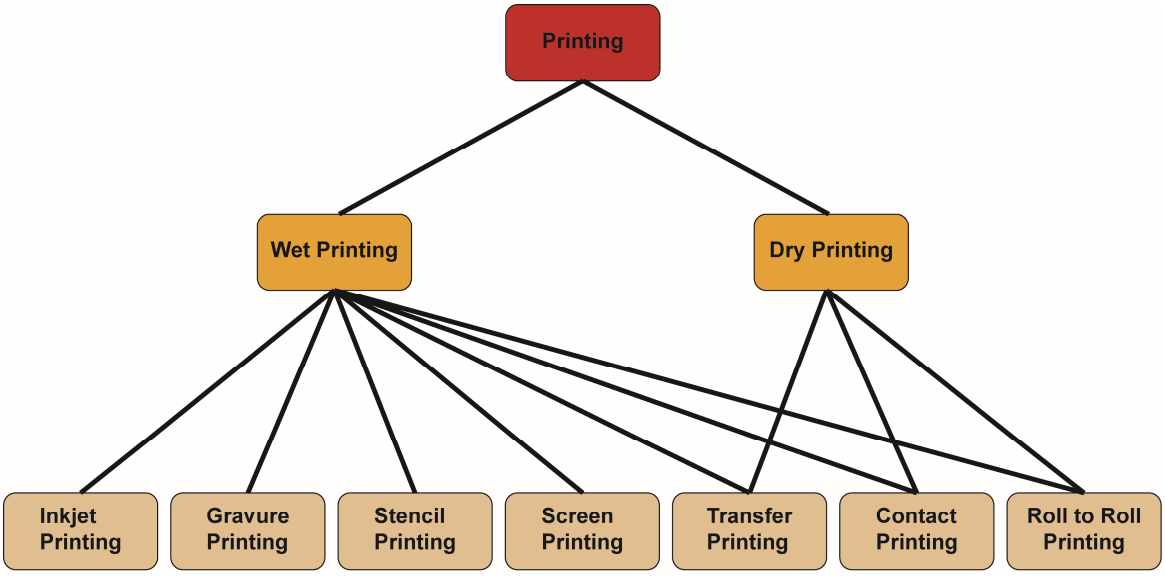


Figure 2.1: The block diagram showing the classification of various printing techniques.

Generally, all printing techniques can be classified into two categories, which are wet printing and dry printing (See Figure 2.1). Wet printing refers to a printing process where liquid is involved, either in the form of "ink" or in the form of transfer medium. Dry printing refers to a process without involving any liquid. Some printing techniques can be classified into both categories, depending on the actual environment of the printing process. For example, transfer printing can be realised in a dry condition, where the contact interface between the donor and receiver does not involve any other materials [15]. It can also be achieved in a wet condition, where a liquid transfer medium is used to modify the interaction between the donor and the receiver [16]. A similar classification can be found in contact printing as well, where mineral oil is optionally used as a lubricant to improve the printing process [17]. Overall, this form of classification depends on specific printing techniques (Figure. 2.1) and detailed discussion can be found in Subsection 2.1.5.

With regard to the conductive film obtained by wet printing, the conductive ink needs to be prepared (see Figure 2.2 for wet printing). Therefore, three main types of ink have been developed and they are a) metal precursor ink, b) conductive polymers and c) carbon based ink

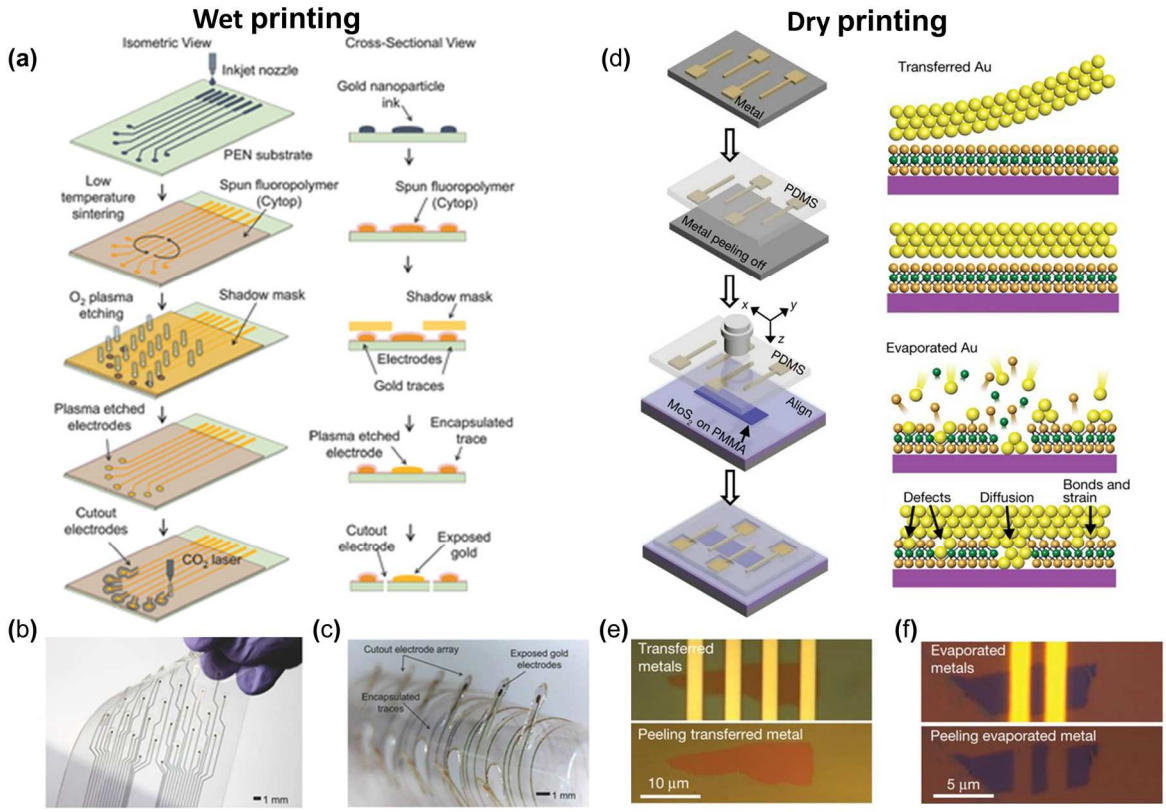


Figure 2.2: The schema and examples for wet printed and dry printed contact pads. (a). (b) and (c) The typical schema and example of wet printed contacts. (d) and (e) The typical schema and example of dry printed contacts. (f) The example of metal contacts fabricated by conventional microfabrication process including photolithography and metal deposition on to the active material, leading to a contact with many defects and surface states Reprinted and adapted with permission. (a), (b) and (c) are from Ref [24]. Copyright © John Wiley and Sons. (d), (e) and (f) are from Ref [46]. Copyright © Springer Nature.

[14, 18]. A typical example of the first type is an ink based on metal nanoparticles such as Ag [19, 20], Au [21], Pt [22], and Pd [23]. These varieties provide not only more freedom in controlling the band structure of the metal semi-conductor contact but also more functions for other applications. For example, Au nanoparticles show good bio-compatibilities. In this regard, they are widely used in various bio-medical applications [24] (Figure 2.2 a, b and c). Other considerations involve aspects such as the cost, the mechanical flexibility, the stretchability and the magnetic properties [25]. For various applications, different metal nanoparticles can be used accordingly as the variety of the metal nanoparticle inks facilitates various conductor applications in a printable manner.

Commercial metal nanoparticles based inks are dispersed in suspension. However, one of the biggest problems is the agglomeration between the nanoparticles, since they have large

Hamaker constants that make them strongly attractive to each other [26]. This is addressed by decorating the metal particles' surface with non-conductive ligands, which significantly increases their dispersibility and stability, leading to a long shelf life [27, 28]. Meanwhile, although this is crucial for the ink stability, it leads to a concern in electrical property as most of the ligands are insulating, forming a transport barrier between the metal nanoparticles. Therefore, the thickness of the ligands should be carefully controlled. Practically, a sintering step is adopted to partially remove the ligands after printing. This can be done by a thermal approach, which is the most common method [29]; or by other methods such as chemical sintering [30], electrical sintering [31], laser beam exposure [32] and microwave radiation [33]. In flexible electronics, additional concern is raised because of the use of mechanically flexible but thermally sensitive polymeric substrate. Therefore, the method of sintering should be chosen depending on the proposed use of the specific substrates. Another technical problem in this process is the adhesion between the printed materials and the substrate. This can be addressed by using a polymer-based binder following an increase in the surface energy [34]. Currently, three types of binder have been principally investigated, which are poly(4-vinyl-phenol) (PVP), poly (methyl methacrylate) (PMMA) and teflon. However, unlike the ligands which are necessary, the polymer binders are only adopted in certain cases as they further complicate the electrical transport because of their insulating nature.

The second type of commonly used conductive ink are conductive polymers such as polyacetylene and poly (3,4-ethylenedioxythiophene) polystyrene sulfonate (PEDOT:PSS). Compared to the metal nanoparticle based inks, the conductive polymers generally have greater flexibility as a result of the smaller Young's modulus from organic materials [35]. However, this would lead to concerns in terms of stability as some inks show vulnerability when exposed to various conditions such as UV light, heat stimuli, moist environment or even ambient conditions [36], and, to this end, suitable encapsulations are often necessary. Since this is not the major focus of this Ph.D. research, details in the recent advances for encapsulation are not included. Relative studies can be found in several previous reviews and books [37, 38].

Carbon based materials such as carbon nanotube (CNT), graphene and their derivatives have also been explored as good candidates for conductor applications. To that end, the preparation of their suspensions is a crucial step towards printing. Typical strategies include oxidation assisted dispersion [39], surfactant assisted dispersion [40] and distillation assisted dispersion [41]. The printed films show a high flexibility and good resistance to external environment, but their conductivity is a concern (~10^3 S/m for carbon based ink and ~10^7 S/m for metal

nanoparticle ink [18]). Therefore, the carbon based ink is usually used in applications where high conductivity is not required.

While these approaches are all based on a wet printing strategy, researchers have also developed dry printing methods for realising conducting films. This mainly refers to a physical transfer process (transfer printing or stamp printing) where an elastomer polymer is used to pick up and release the pre-fabricated metal films [42-45] (see Figure 2.2 for dry printing). The advantage of this approach is that it enables the merging of the traditional micro-fabrication process with the flexible electronics: the conventional micro-fabrication process which involves the high temperature treatment can be first realised on the rigid substrate and the as-fabricated materials and devices can be then transferred onto the flexible platform.

Unlike the conventional micro-fabrication process which inevitably introduces impurities (as a result of photoresist or solvent residues) and damages (as a result of physical bombardments on the material surface) the interface between donor and receiver, the dry printing method can achieve a pure and intrinsic interface as a result of a van der Waals (vdW) contact (see Figures 2.2 d, e and f) [46]. Recently, interesting results have been realised by exploring the vdW contact between metal film and MoS_2, leading to the experimental validation of the long hypothesised Schottky-Mott relationship in the system of metal-MoS_2 vdW contact [46]. The vdW contact between metal and 2D material is another important part of this research which focuses on the exploration of graphene-Au vdW contact as realised by the transfer printing method and its applications in large-area flexible electronics. This will be discussed in Chapters 4 and 5.

Finally, a table has been included to compare the properties of the conducting materials printed by different methods.

Table 2.1: Summary of printed conductive materials.

Material	Fabrication method	Minimum thickness	Conductivity	Special requirement	Ref #
Ag ink	Ink-jet or screen printing	Down to ~ 10 nm	~10^6 S/m	Sintering required	[19,20]
Au ink	Inkjet printing	Down to ~ 10 nm	~10^7 S/m	Sintering required	[21]
PEDOT: PSS	Inkjet printing	Down to ~10 nm	10^{-1}~10^3 S/m	Lack of stability	[35]

Carbon based ink	Inkjet printing	Down to ~10 nm	~10^3 S/m	NA	[18]
Metal film	Transfer printing	Down to ~1 nm	10^8~10^9 S/m	NA	[46]

2.1.2 Semiconductors

Various semiconducting materials including organic molecules and polymers [47, 48], inorganic nanowires (NWs)/nanotubes (NTs) [17, 49], thin films [50] and quantum dots [51], can be realised by a printing method over a large-area. As discussed earlier, the printing of semiconductors is categorised into dry and wet methods and promising results have been obtained using both approaches.

The mainstream of the wet printing for semiconductor applications include methods such as inkjet printing and screen printing. For this, suitable "inks" or "pastes" containing the desired semiconducting materials, both organic and inorganic, need to be prepared. Unlike the scenario for conductor applications where a binder can be used, the polymer binders are not favoured in preparing semiconducting inks, especially for printing organic films, since it introduces impurities to the device channel and reduces the performance. Instead, crystalline, high quality semiconductor film is regarded as indispensable for realising high carrier mobility of the FET and sustained efforts have been made to realise high crystalline organic film by using printing methods [52]. Although initial results of printed organic FET exhibit a low performance (~0.01 $cm^2V^{-1}s^{-1}$) with bad crystallinity [53], significant advances have been made in this direction with single crystal up to several hundred micrometres achievable [52] (see Figure 2.3a). This leads to devices with a mean carrier mobility ~16.4 $cm^2V^{-1}s^{-1}$, comparable to the best reported organic field-effect transistor (device mobility up to 43 $cm^2V^{-1}s^{-1}$ [54]). Given the abundant material library for organic semiconductors, various functional electronic components with

high-performance can potentially be realised in a cost-effective manner over the large area, both on rigid and flexible substrates.

The wet printing approach can also be used to print inorganic semiconductors such as ZnO NWs, semiconducting CNTs and amorphous indium-gallium-zinc oxide (InGaZnO) nanofilms [55-58] (Figure 2.3 b and c). Often the printed inorganic semiconductor films are composed of randomly stacked inorganic crystals without any alignment preference, leading to complex and uncontrolled carrier transport properties [57, 59, 60]. In contrast, for inorganic semiconductors, because of their high stability and crystallinity, transfer or contact printing are more popular [61-64], since this provides greater freedom in material processing and alignment, and benefits the realisation of high-performance electronics (see Subsections 2.1.5.3 and 2.1.5.4). It should be noted that these two methods can be realised without the use of liquid, thus categorizing

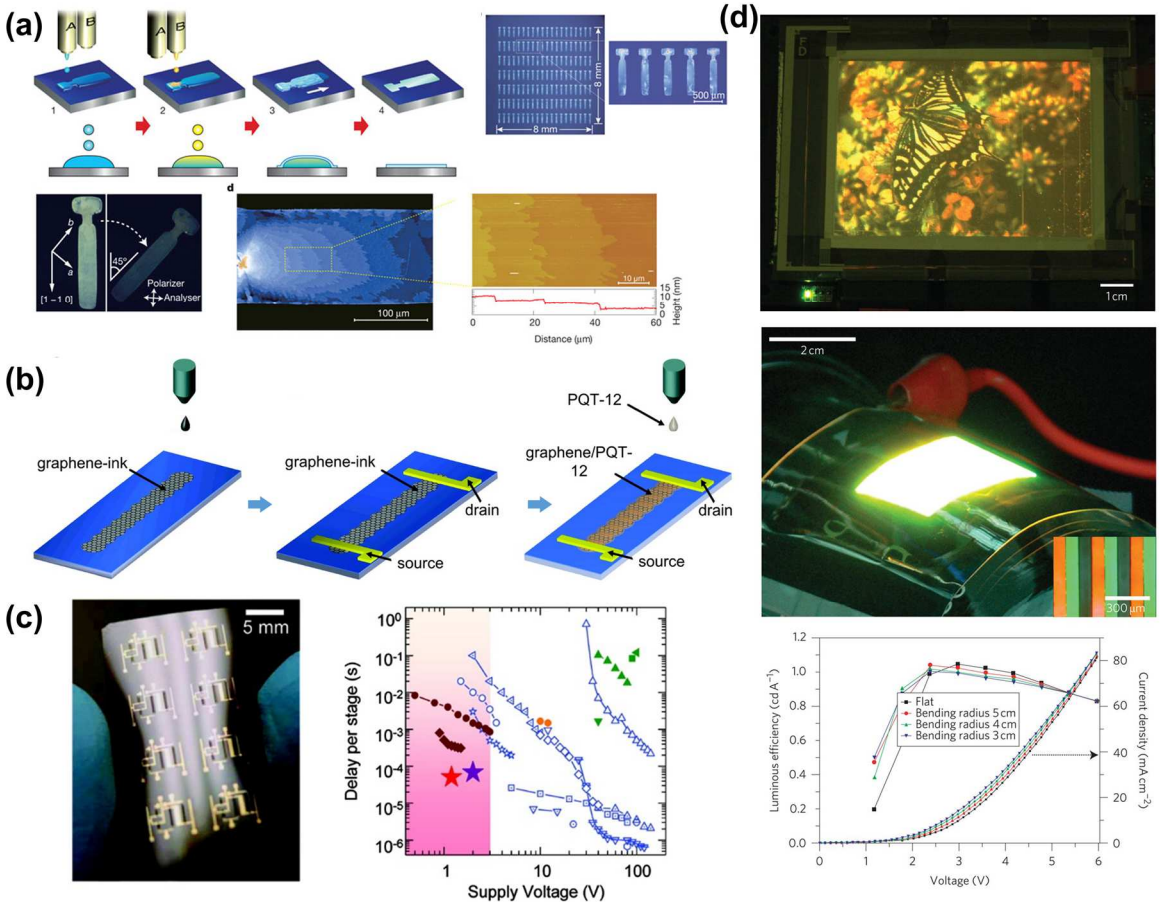


Figure 2.3: Typical examples of printed semiconductors. (a) The inkjet printing of single crystal of C8-BTBT layer and its characterisations. The POM image shown on the bottom left indicates its crystallinity. (b) The inkjet printing of graphene based FET. (c) The wet printed CNT circuits with reasonable performance. (d) Printed quantum dots for illuminating application. Reprinted and adapted with permission. (a) and (d) is from Ref [52].and [51], respectively. Copyright © Springer Nature. (b) and (c) are from Ref [98] and [58], respectively Copyright © American Chemical Society.

them as dry printing approaches. Compared to wet printing, dry printing of semiconductors leads to much cleaner interfaces. This is one crucial aspect towards the realisation of high-performance electronics based on nanomaterials, and has been demonstrated in many systems including organic and 2D materials [65-67].

Finally, a table has been included to summarize the properties of the printed semiconductors listed here for various applications.

Table 2.2: Summary of printable semiconducting materials.

Material	Printing method	Product quality	Application	Ref #
Organic semiconductors	Inkjet or screen printing	Comparable to the SOA	FETs, solar cells, etc	[52]
Inorganic NWs/NTs	Inkjet, transfer or contact printing	Comparable to the SOA	FETs, sensors, etc	[60]
2D materials	Transfer printing	SOA	FETs,	[61, 67]
Quantum dots	Transfer printing	NA	LEDs, etc	[51]

2.1.3 Dielectrics

Dielectrics are the final building blocks for electronic devices. However, in the development of printable electronics, such as FETs, many of the studies used a Si substrate with SiO_2 layer acting as a gate dielectric by a bottom gate strategy. This strategy avoids the fabrication of the gate terminal thus dramatically decreasing the process difficulties, but it is at the cost of high operation voltage as well as the inability to control the device individually. Therefore, for those circuit applications with an array of FETs, realising locally controlled gate terminals with low film thickness, high dielectric constant and strength, is desired. At present, two major types of materials have shown promising compatibilities with printing technologies and these are a) cross-linked polymer blend dielectrics and b) sol-gel based dielectrics [14]. The first type of materials are organic polymers, with typical examples of polystyrene (PS), and PMMA. Compared to conventional inorganic dielectrics such as SiO_2 and Si_3N_4, the organic polymers show a better suitability with soft-electronics because of their higher flexibility [68]. Therefore, replacing the brittle insulator to these polymer-based dielectrics would potentially lead to a soft

electronic device with greater flexibility. However, various limitations exist for the organic polymers when compared to standard dielectrics from a conventional micro-fabrication process. To be more specific, one major drawback of polymer based dielectric materials is their low dielectric constant (<10) [69]: this value is usually >20 for those high-κ materials. It should lead to a much higher requirement in thickness control, if the same level of areal capacitance is to be achieved. Other problems with the printed organic polymer dielectrics include low film quality with pinholes and uncontrolled film thickness via printing, which can be seen in the pioneering work during the initial stage [70-72]. Promisingly, all these concerns have been largely solved. This is because, thanks to the abundant material library for organic materials, organic polymers with high dielectric constant (>60), low surface roughness (~0.72 nm) and well controlled film thickness have been successfully found and achieved by printing technologies [69].

Meanwhile, inorganic dielectric layers, such as metal oxides, have also shown their printability with a sol-gel method. For example, highly smooth AlO_x film with low leakage current and high areal capacitance have been demonstrated by printing, with well-controlled thickness down to 10 nm (see Figure 2.4 a) [73]. The performance of the printed metal oxide layers has become comparable to those materials realised by conventional microfabrication technologies such as atomic layer deposition (ALD) and sputter, enabling the realisation of high-performance printed electronics.

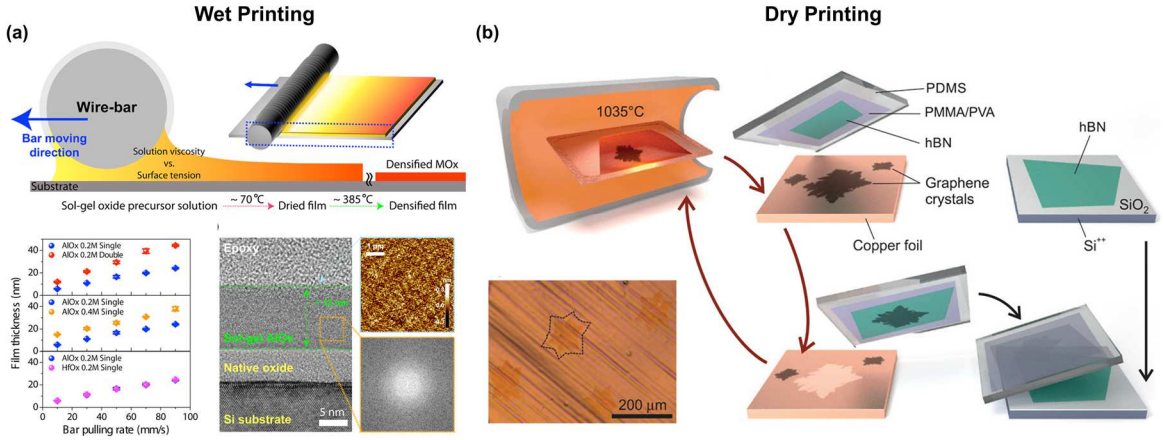


Figure 2.4: Typical examples of printed dielectrics. (a) The printing of solution based dielectric materials and corresponding characterisations. (b) The stamp printing of hBN for dielectric and encapsulation of GFET. Reprinted and adapted with permission. (a) is from Ref [73]. Copyright © John Wiley and Sons. (b) is from Ref [82]. Open access article.

Apart from these wet printing approaches, dry printing has also been explored for the realisation of dielectrics. This mainly refers to those studies where hexagonal boron nitride (h-BN) is used as the dielectric layer and transferred onto the target location of the receiver substrate by a transfer printing method (Figure 2.4 b). The novelty of these studies is partly because of the material itself, since h-BN has been suggested as an ideal dielectric material with unique advantages of ultralow thickness (~0.33 nm for monolayer), ultra-flat surface, high breakdown voltage (>0.5 V/layer) and a perfect crystal plane without any dangling bonds [74-79]. In this regard, much research has explored the h-BN as a dielectric material in FETs, leading to the realisation of many novel devices with unprecedented performance [78, 80-82].

Despite these advantages, barriers exist in realising an ideal h-BN/semiconductor interface from a technical point of view. This includes the high-quality synthesis of h-BN and its subsequent clean, controllable and reproducible transfer. Specifically, how to achieve a uniform contact interface between the dielectric and semiconductor, by using the transfer printing method, is a critical problem. Although this aspect has seldom been mentioned in related research articles (possibly because of a different focus) [80, 81], the non-uniform vdW gap with bubble formations has been observed in the transfer printing process, and reported in other research from different groups [79, 83, 84]. In this regard, how to achieve a high-quality contact interface over large-area between h-BN and various semiconductors is a problem yet to be solved for near future printed electronics.

Finally, Table 2.3 directly compares all the dielectric materials mentioned in this section.

Table 2.3: Dielectric properties of various materials.

Material	Fabrication method	Minimum thickness	Dielectric constant	Dielectric strength	Surface roughness	Young's Modulus	Ref #
SiO_2	Thermally grown	Down to 1 nm	3.9	10^7 V/cm	R_a ~ 0.2 nm	6.6×10^{10} N/m^2	[85]
$BaTiO_3$	Inkjet printed	NA	NA	NA	Particle size of 100 ~ 200 nm	NA	[71]
Benzocyclobutene	Spin-coated	Down to 10 nm	NA	$>3\times10^6$ V/cm	NA	NA	[72]
PMMA	Spin-coated	Down to 100 nm	2.89~3.66	$>2\times10^6$ V/cm	R_a ~ 0.3 nm	1×10^9 N/m^2	[86, 87]

AlO_x	Bar pulling	Down to 10 nm	NA	$>2\times10^6$ V/cm	R_{RMS} ~ 0.08 nm	NA	[73]
P(VDF-TrFE-CFE)	spin-coated	~160 nm	>60	$>2.5\times10^6$ V/cm	R_{RMS} ~0.72 nm	NA	[69]
h-BN	Mechanical exfoliated	Down to ~0.3 nm	3.38 or 6.61 depending on the field direction	~ 10^6 or 10^7 V/cm depending on the field direction	R_a < 0.1 nm	~8.6×10^{11} N/m^2	[76, 88, 89]

2.1.4 All printed electronics

In Subsections 2.1.1 to 2.1.3, the printing of materials with various bandgaps has been summarised and some of the preliminary device applications have been demonstrated. However, the examples listed above are only "partially printed": the devices are realised by combining the printing techniques with the standard microfabrication processes. One may wonder with the advances in printing technology described above, if it is possible to achieve an "all printed" device. This subsection explores this direction by reviewing the state of the art in various "all printed device", including solar cells, sensors, memories and FETs. Surprisingly, some of these prototype devices have shown a comparable performance to those state-of-the-art non-printed devices, which shows the great potential held by printing technology for the development of near future large-area electronics.

All printed solar cells

As previously highlighted, an inkjet printer is able to print various types of materials in a "drop on demand" manner. With suitable inks (semiconductors and conductors), a solar cell can be successfully realised in ambient condition by printing technology [90]. The printed device shows reasonable power conversion efficiency, with an average value of 2%. This is partially limited by the top contact (Ag electrode, as shown in Figure 2.5a), since the replacement of the printed Ag film by vacuum evaporated contacts would lead to a dramatic increase of the efficiency to 5%. Further study also indicates that the inkjet printed poly[N-9-heptadecanyl-2,7-carbazole-alt-5,5-(4′,7′-di-2-thieny-2′,1′,3′-benzothiadiazole)]:[6,6]-phenyl-C71-butyric acid methyl ester (PCDTBT:PCBM) layer shows similar behaviour to the spin-coated film, which has revealed the potential of the printing technologies in energy harvesting applications.

All printed sensors

A ZnO NW based UV photodetector is demonstrated by an inkjet printing method [91] (see Figure 2.5 b). ZnO is a wide-bandgap semiconductor and its allotropes, such as NWs and thin films, have been widely used for various sensing applications including UV detection [92, 93]. Unlike conventional NW based UV photodetectors where the channel is based on a single crystal material, this work adopted a thermal calcination method where the ZnO NW is converted from the printed zinc acetate (ZnAc) film and leads to a polycrystalline ZnO NW. Notably, such a change appears to reversely benefit the photodetector performance with a much lower dark current and ultra-high detectivity up to 3.3×10^{17} Jones. This enhancement is attributed to the band-edge modulation because of the existence of the grain boundaries. This study suggests that, although the printed film would be of low quality in the materials perspective (polycrystalline vs monocrystalline), such properties may reversely benefit the intended application and lead to a higher performance by the device.

All printed memory devices

Memristor is a device whose state (resistance) is dependent on its operational history of electrical stimuli. Because of its high endurance [94], high on/off ratio [95], long retention time [94, 96] and great potential for scaling down, memristor has been suggested as a promising candidate for next generation data storage device. Memristor usually has a metal-insulator-metal configuration, and is made by mature microfabrication techniques such as lithography, metal deposition, ALD and sputtering. With the development of printing technologies, there is a strong interest in developing electronics by printing method. For example, Lien *et al*. realised a C/TiO2/Ag based memory cell by using all printing methods (screen printing and inkjet printing, see Figure 2.5 c) [97]. The performance of the as-realised cell is still in its initial stage, with an endurance of ~100. However, the benefit of this method is in large scale processing on an arbitrary substrate, for example on a paper substrate which can be disposed after usage. This study, although quite preliminary, can encourage advances in future disposable electronics.

All printed FETs

FET is one basic building block for electronic circuits and systems. Realising high performance FET by a printing approach can greatly benefit the development of printable electronics. One exploration in this direction is the ability to print 2D materials for FETs' application and in this regard both dry printing and wet printing have been realised. With regard to wet printing, this refers to a process where 2D material based ink is prepared and then printed by tools such as an inkjet printer. A typical example is the work done by Torrisi *et al.*, where graphene ink was

prepared and printed as the channel for the FET [98] (see Figure 2.5 d). The benefit of this process is its low cost and extendibility to large-area process, but its performance is limited (~95 $cm^2V^{-1}s^{-1}$, one to two orders of magnitude lower than the state of the art). This is a result

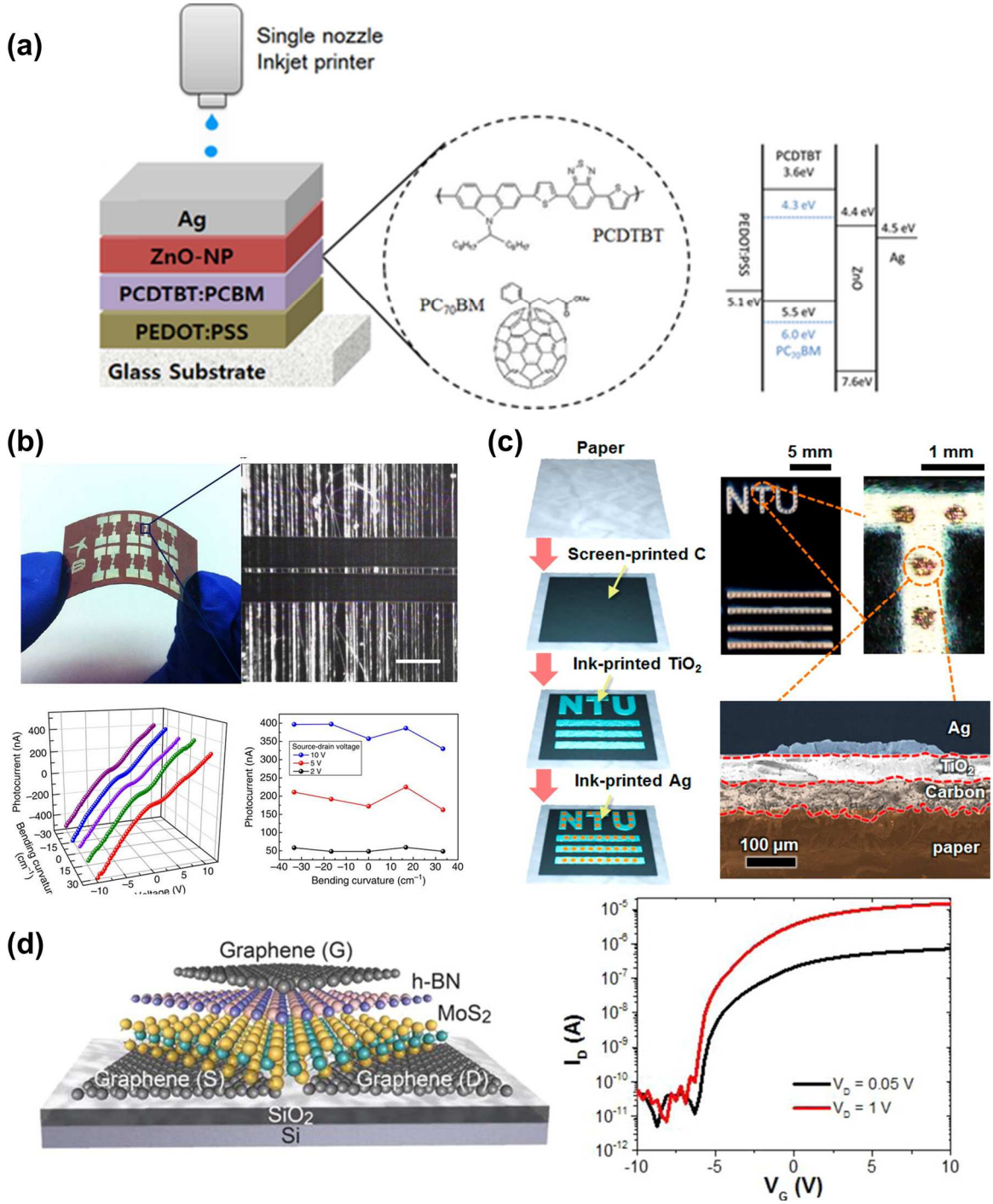


Figure 2.5: All printed electronic devices. (a) The solar cell fabricated by inkjet printing (b) The photodetectors realised by inkjet printing (c) All printed memory device (d) A all 2D material based transistor realised by transfer printing. Reprinted and adapted with permission. (a) is from Ref [90]. Copyright © John Wiley and Sons. (b) is from Ref [91]. Open access. (c) is from Ref [97]. Copyright © American Chemical Society. (d) is from [81]. Copyright © American Chemical Society.

of an imperfection from the channel materials, as well as the poor-quality interface. Therefore, the dry printing approach is more favoured.

With respect to the dry printing of 2D materials, often this refers to a process where various materials are picked up from a donor substrate and mechanically transferred to the target location of the receiver substrate, forming a vdW contact or vdW heterostructures [99, 100]. As no thermal annealing is required, this strategy is compatible with flexible electronics. Meanwhile, unlike the inkjet printed devices, the device realised by transfer printing shows a far greater performance [46, 67]. Specifically, by using this physical transfer method, a total 2D materials based FET has been realised, with a device mobility of up to 33 $cm^2V^{-1}s^{-1}$for MoS_2 [81, 101]. This value is comparable to the state-of-the-art device, showing the great potential of the dry printing method for high performance electronics.

In summary, this subsection reviews the recent advances in all printed electronic devices. Indeed, some of the listed devices show a limitation in performance as a result of restricted processing conditions and the gaps between those printed devices are not insurmountable. In fact, in some scenarios, the performance of these two types of devices is even comparable. Considering the advantages held by printing technology and its compatibility to flexible electronics in a roll-to-roll processing manner (See the discussion in Subsection 2.1.5), printing is believed to be one of the most promising techniques for the realisation of near future large-area, flexible electronics.

2.1.5 Methodologies in printable electronics

The focus of this section is on printing methodology. In order to provide a comprehensive overview, various mainstream printing approaches are summarised with their advantages and disadvantages. Furthermore, the possibility of extending printing technologies to roll-to-roll fabrication is discussed, with several pioneering laboratory scale demonstrations. Finally, a comparison between the listed printing methods is made, showing their unique properties and suitability for different applications.

Inkjet printing and e-printing

Inkjet printing is a technique which enables the ink to be printed at the desired location of the substrate from a computer-controlled nozzle, in either a continuous manner or a “drop-on-demand” manner. In a conventional inkjet printer, the ink is pushed out of the nozzle and forms a droplet for printing under heat or force stimuli. Other parameters, such as the size and the moving speed of the nozzle, the voltage bias used to drive the printing, the ink and the substrate

(stage) temperature, can also control the quality of the printed ink [102, 103] (see Figure 2.6 a). For conventional inkjet printer, its resolution is a major concern, with a minimum printed feature size down to ~20 µm [104]. This is as a result of the limitation of the diameter of the nozzle as the flow of the ink will be drastically blocked in a nozzle smaller than 20 µm. Therefore, a traditional ink-jet printer is mainly used for realisation of a large size device,

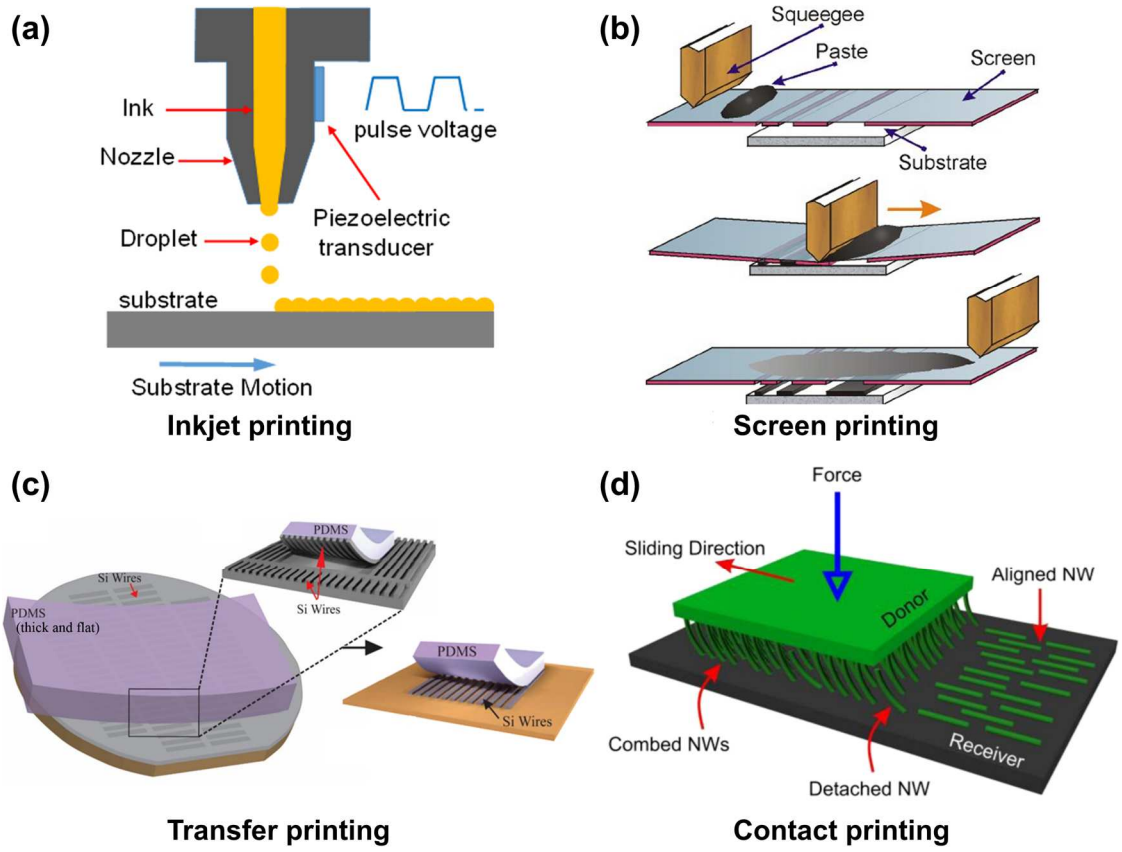


Figure 2.6: Schema of various printing technologies. (a) Inkjet printing (b) Screen printing (c) Transfer printing and (d) Contact printing. Reprinted and adapted with permission. (a) is from Ref [90]. Copyright © John Wiley and Sons. (b) is from Ref [107]. Copyright © American Scientific Publishers. (c) is from Ref [64]. Open access. (d) is from [123]. Copyright © Cambridge University Press.

especially for those materials such as organics which are vulnerable to a conventional micro-fabrication process [47, 48].

In the meantime, researchers are working to improve the resolution of the inkjet printer for a wider range of applications. This has been achieved by either modifying the printed substrate or the printing setup. With respect to the first approach, "dewetting" of the printed ink was studied and utilised, leading to a controlled gap formation (down to 250 nm) in the printed film [105]. This structure can serve as the source and drain electrodes of a short channel FET. Although this overcomes the inject printer's limitation in resolution, an additional lithography step is needed to pattern the surface of the target substrate for the dewetting. In this regard, the

benefit of the simple printing is obscured. Alternatively, researchers have been working on modifying and updating the conventional inkjet printing system, targeting a reliable printing method with features down to microns or sub-microns. First reported by Park *et al*., an e-jet printer is developed as an advanced version of an inkjet printer. Unlike the conventional setup which utilises thermal or physical stimulus to extrude the ink, a high electric field is adopted to provide a more precise control of the ink formation and printing in the e-jet printer, leading to a significant resolution increase from tens of micrometres to several hundreds of nanometres [106]. However, it should be noted that this improvement results in a slower printing speed, since the operation and control of a high electric field takes longer than the conventional thermal or mechanical methods.

Screen printing and stencil printing

Screen printing and stencil printing refer to a similar process where pastes (inks) are poured onto a mask and are slid over the mask using a squeegee. By doing so, the pastes are forced to penetrate through the mask, forming a film on the target substrate in a reverse pattern (see Figure 2.6 b) [107]. The mask can be made of various materials. Generally, a mesh mask is used in screen printing while for stencil printing the mask is made of metal or other materials. Another difference between the two printing technologies is the distance between the sample and the mask. In stencil printing, the mask is in direct contact with the sample while in screen printing there is a gap between the two.

The resolution is also a major problem for screen or stencil printing. In this scenario, it directly depends on the mask, whose resolution is limited by the resolution of the emulsion; the minimum feature size that can be achieved on this material is ~100 μm [108]. In the meantime, unlike inkjet printing where a film down to several nanometres can be reliably printed [52], thickness control is another concern for screen printing, with a typical printed film of several micrometres in thickness [109]. This is detrimental for printing an organic semiconductor for electronic devices such as FETs, since a thicker channel material leads to an increased Schottky barrier width, suppressed tunnelling probability and a much poorer device performance with worse contact [109]. To this end, researchers have attempted to decrease the thickness of printed film down to several tens of nanometres. This is achieved by using a low viscosity ink combined with two polymer banks in order to maintain the shape and crystallinity of the film [109]. This, although increasing the complexity of the fabrication, can successfully facilitate the screen printing of thinner films, leading to a screen printed OFET with better contact.

Transfer printing

Along with the development of nanomaterial and technology, the term "transfer printing" has been used to describe two similar processes which are used to transfer the specific materials from the donor to the receiver substrate. One process refers to a method which uses an elastomer stamp with a sticky surface to "pick up" the target materials from their carrying wafer, and release them onto the desired location at the receiver substrate [42, 110] (see Figure 2.6 c). To achieve this, the contact interface property is crucial and needs to be controlled in order to successfully deliver the picking up and releasing steps at specific locations over the large area. To be more precise, the interaction between the materials and substrate is quantified by a characteristic energy release rate *G*. To achieve the successful picking up of the material from the donor, the requirement is $G_{materials-donor} < G_{materials-stamp}$; similarly, to realise the releasing step, the contact interface should meet the requirement of $G_{materials-stamp} < G_{materials-receiver}$ [111]. These can be experimentally achieved by various approaches, such as surface functionalisation and control of the peeling rate [112, 113].

Resolution is another concern for transfer printing and is limited by the feature size of the inks (materials) as well as the alignment accuracy. While the former is determined by the material itself, it is not very relevant to the research on printed electronics. In contrast, the alignment accuracy is a more fundamental problem for transfer printing, and, to this end, sustained efforts have been devoted to improve this figure of merit [114-116]. At present, an alignment accuracy down to 100 nm has been successfully achieved over large-area [117], showing much promise for future development of large-area, high-performance electronics via a stamp printing method.

As well as this method where an elastomer stamp was used for the materials transfer, transfer printing also refers to a process where a polymer solution is spin-coated onto the donor substrate and the as-formed polymer film is used for the realisation of the transfer process. Unlike the previous approach, the detachment of the active materials is achieved by either etching the underlying substrate or mechanically peeling off the coated polymer film. In this regard, this method does not require any control of the picking up process, and therefore it has been developed to transfer those nanomaterials which are strongly bonded to the donor substrate [118, 119]. In terms of the material releasing step, this is achieved by similar means used in stamp printing where the interaction of the material and receiver substrate is guaranteed by a physical contact and further promoted by some dry and wet approaches [15, 16, 120]. After this, the polymer film is removed by dissolving it in the solvent. While this method does

not need a precise control of interface properties, disadvantages exist because of the involvement of other chemicals. It has been suggested that this, in many cases, can lead to a contamination of the as-transferred nanomaterials and alter their electrical properties [16, 121].

Contact printing

Contact printing is an approach which is specifically developed to transfer and align quasi-1D materials [17, 122, 123]. It refers to a process where the donor substrate with vertically grown NWs and NTs is pressed towards the receiver substrate and directionally slides one over the other. By doing so, the NWs can be detached from the donor and anchored onto the receiver, with preference alignment in the sliding direction (see Figure 2.6 d). Currently, the research interest in NW printing studies is mostly focused on the following two kinds: a) a highly aligned, closely packed NW film; and b) a single NW located at a specific location with controlled orientation. Both of these have been explored *via* the contact printing approach. The performance of the FET, based on the latter, can probe the electrical property of a single NW. With such devices, creating a device array with uniform performance over a large area is challenging since the NW to NW variations (such as diameter and doping) can lead to a large variation in their electrical characteristics [124]. In contrast, the printed NW film with high density, uniform distribution and good alignment shows a much smaller variation in device performance because of the average effect from a group of NWs. However, such devices usually show a higher off-current and thus increased power consumption as a trade-off for the high uniformity. Therefore, both types of device have their own benefits and are of interest on their own.

With respect to the realisation of highly aligned, close-packed NW film printing, initial studies have revealed the influence of contact pressure and surface functionalisation on the contact printing results [17]. With these parameters controlled, good printing performance (in terms of NW length, density, alignment and uniformity) has been successfully achieved over large area. A subsequent study indicated that the anchoring force hinders the precise alignment of NWs. By separating the anchoring region and aligning region, the NW alignment can be dramatically improved by using the "combing method" [125]. Notably, contact printing can not only be achieved on a conventional substrate like Si, but also on some unconventional receivers such as polymeric flexible substrates and rigid substrates but with a non-planar surface. This has shown the great compatibility of the contact printing approach and opens new avenues for the fabrication of near future flexible and 3D integrated electronics [17, 126, 127].

The other research interest is in using the contact printing approach to print single NWs at specific location. This has been explored by fabricating anchors with specific shape and dimension on the receiver substrate to "capture" the single NW, because of the drastic local friction increase by introducing the NW catcher on the receiver substrate [125, 128]. For example, by using a combing method along with narrow (~1 µm wide) coplanar electrodes, a single NW can be captured with a high yield (~90%) [125]. A similar trial has also been shown to be effective by using a dry printing process, but with a triangular or more complicated "NW catcher" [128]. Overall, these initial studies have shown the feasibility of the single NW transfer at the desired location with the contact printing method, indicating its great potential, good compatibility and versatility for various applications.

Roll-to-Roll printing

Potentially, all of these methods can be extended to a roll-to-roll process for a flexible substrate as an advantage of the printing technology. With respect to the inkjet printing, screen printing and stencil printing, roll-to-roll fabrication can be realised by mounting the flexible substrates on some gear-controlled rollers and integrated with the printer in the desired alignment [129] (see Figure 2.7).

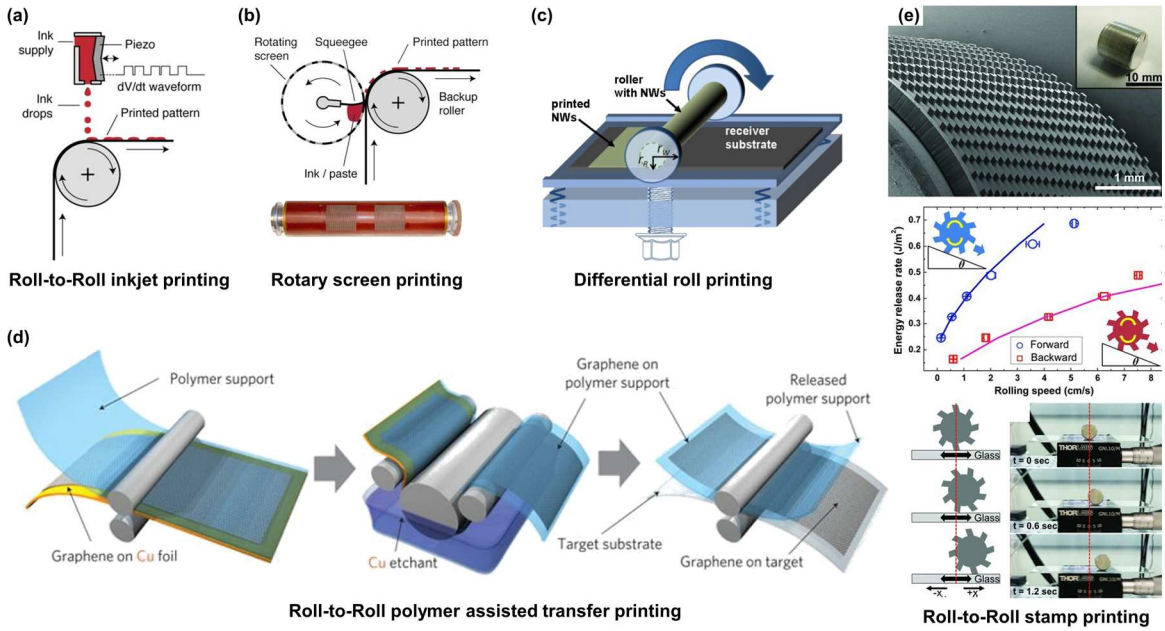


Figure 2.7: Roll-to-Roll printing technology. The Roll-to-Roll version of (a) inkjet printing, (b) screen printing, (c) contact printing, (d) polymer assisted transfer printing and (e) stamp assisted transfer printing. Reprinted and adapted with permission. (a) and (b) are from Ref [129]. Copyright © John Wiley and Sons. (c) is from Ref [133]. Copyright © AIP Publishing. (d) is from [131]. Copyright © Springer Nature. (e) is from Ref [130]. Copyright © John Wiley and Sons.

With respect to the transfer printing method, roll-to-roll transfer has also been demonstrated by several groups [130-132]. For example, as shown in Figure 2.7 e, a flexible stamp with angular posts has been wrapped around a cylinder surface, serving as the roller. The stickiness of the stamp can be tuned by changing its movement direction [130]. In this regard, the roll-to-roll pickup and releasing of materials can be realised. Meanwhile, the concept of roll-to-roll production has also been demonstrated for polymer assisted transfer. By integrating the polymer adhesion gear, a metal etching chamber and a polymer releasing gear, the effective roll-to-roll transfer of graphene up to 30 inch has been demonstrated [131] (Figure 2.7 d).

Finally, the roll-to-roll version of contact printing is realised by a differential roll printing method [133]. This uses a donor substrate in a cylindrical shape with NWs vertically grown on the surface, and rolls it on the receiver substrate under certain pressure. As described earlier, the alignment of NWs is a result of the sheer force generated in the printing process. Similarly, in order to realise successful NW printing and alignment with this method, a relative movement between the inner and outer roller, which generates the sheer force, is essential. This is achieved by adopting an intentionally mismatched pair of inner and outer rollers with different diameters (Figure 2.7 c). By doing this, the NW can be printed in a highly aligned manner with roll-to-roll configuration over large-area. Compared to the contact printing process where the contact between the donor and receiver is planar, the cylindrical donor delivers a small contact area at a time, which mostly preserves the freshness of the donor substrate. This unique property is highly beneficial for realising uniform NW printing over large area.

Overall, unlike a traditional micro-fabrication process, the printing technologies are simple and cost effective, and can be easily extended to roll-to-roll production, which holds great promise for the development of future, flexible electronics over large-area. To conclude this section and to summarise these printing technologies, Table 2.4 illustrates the advantages and disadvantages of each printing method.

Table 2.4: Comparison of the properties of various printing techniques.

Technology	Lateral resolution	Thickness	Donor format	Printing speed	Applications	Ref #
Inkjet printing	Down to ~20 µm	10~1000 nm	Ink	Medium	FETs, circuits, solar cells, photodetectors, etc	[22, 47, 48, 52, 59, 104]
e-jet printing	Down to ~100 nm	1~100 nm	Ink	Slow	FETs, circuits, solar cells,	[105, 106]

					photodetectors, etc	
Screen/Sten-cil printing	~100 µm	5~100 µm	Paste	Fast	Mainly for conductive layers such as contacts	[108]
Transfer printing	Down to ~100 nm	Not limited	Materials on a donor substrate	Depends	FETs, circuits, solar cells, photodetectors, etc	[61, 110, 111, 120]
Contact printing	NA	Not limited	Quasi-1D materials	Fast	Mainly for NW based devices	[17]

2.2 3D integration technologies

The idea of 3D integration can be traced back to the 1980s, when there were attempts to further increase packaging density by exploring its vertical dimensions [134, 135]. However, this idea did not draw much attention at that time since the device scaling in the 2D plane was an easier and cheaper option. Currently, since the conventional scaling of individual devices has almost approached its physical limit, the 3D integration concept has again been picked up and is regarded as one of the major strategies to extend the life of Moore's Law. Until now, 3D integration has become a very broad concept which is used to describe a number of strategies for the realisation of electronics stacked on the vertical dimension, including 3D wafer-level packaging (3D WLP), 3D stacked ICs (3D-SICs), 3D system in package (3D SIP) and monolithic 3D ICs [136]. Technologically, these strategies can be mainly categorised into two: parallel integration and sequential integration. Parallel integration refers to a process where several electronic layers are fabricated individually, and then bonded together to achieve the 3D integration. The above-mentioned 3D WLP, 3D SIC, 3D SIP all belong to this strategy. By contrast, sequential integration, also known as 3D integration, describes a concept where the electronic layers are built in sequence on the same substrate, from the bottom to the top. Both of these strategies can significantly increase the device density.

Another interesting aspect for 3D integration is that it has a very wide applicability. With regard to the printed electronics, the device density is greatly limited due to the printing resolution. However, by stacking the printed components in the third dimension, the total number of printed devices can be significantly increased. This is another important aspect which will be explored in this Ph.D. study.

This section is arranged as follows: First, a brief overview is given on 3D integration by stacking thinned chips (3D WLP, 3D-SICs, 3D SIP) in subsection 2.2.1. Then the recent advances in using printing techniques to realise 3D integration (monolithic 3D) are reviewed (Subsection 2.2.2). Finally, a comparison is made between the listed works on monolithic 3D integration by printing technologies (Subsection 2.2.2).

2.2.1 Parallel integrated 3D electronics

As explained earlier, parallel integration refers to a strategy where several strata are fabricated individually and stacked together. Each stratum is realised by mature industrial manufacture technology such as CMOS. The as-fabricated components are thinned down and stacked together by various bonding techniques to achieve the 3D integration. This section provides a brief summary and overview of the major steps towards parallel integration, including thinning, bonding and interconnects realisation [137].

Thinning technologies

Usually, the as-fabricated wafers and chips need to be thinned before the 3D integration. One main reason for this is the requirement for interconnect formation through silicon vias (TSV) techniques: the strata need to be etched through and filled with metallic leads to connect the electronic devices on each layer. With thinner substrates, the TSV process could become easier and cheaper. In addition, the decrease in vertical dimension for each stratum also provides a possibility for a higher packaging density, but to achieve this, other factors also need to be considered.

In general, various techniques are available to decrease the thickness of the wafers and chips, including grinding, wet etching, dry etching, chemical mechanical polishing (CMP), proton induced exfoliation and layer transfer [137, 138]. For example, grinding refers to a process where a grinding wheel is used to mechanically remove the substrate material by continuous pressing and rotating. The rear of the wafer is faced towards the wheeler while the top is covered by a protection layer. This strategy provides a fast route to thin down the wafers and chips, but it can potentially lead to some damage to the crystal structure inside the substrate, which may pose issues for the later process. Moreover, the uniformity of this process is another concern since the material removal process is not precisely controlled [137]. Meanwhile, the dry etch provides a precise way to uniformly thin down the substrate, but at a relatively slow rate with a higher cost. Overall, various techniques are capable of thinning down the wafers or chips with their own advantages and disadvantages.

Bonding

The as-thinned strata are stacked together in order to realise 3D integration. For this, a bonding step is required for a strong and reliable mechanical attachment. Typical bonding techniques include metal-metal bonding, SiO_2-SiO_2 bonding and hybrid bonding [137]. With regard to the metal-metal bonding, materials such as SnAg [139], Cu–Sn [140], and Cu–Cu [141], have been explored. In general, the advantage of metal-metal type bonding is its conductivity, which could provide a direct electrical connection between the bonded wafers and chips. However, such bonding shows a low stability, especially with thermal stimuli. As a result, the metal-metal bond is mostly used for two wafers' integrations [137]. Meanwhile, the SiO_2-SiO_2 bond has also been explored to bond the wafers or chips. Unlike the previous type, this bond shows a good stability upon mechanical or thermal stimulus, but it cannot provide an electrical connection because of its material nature [142]. In this regard, an extra process is needed to connect the two wafers and chips electrically. With respect to the hybrid bonding, it uses multiple materials to bond the wafers. Normally by using this bond, the stability and electrical conductivity can both be achieved at the same time. However, such bonding requires a more complicated process with better alignment accuracy and a much cleaner surface [143]: its applicability is a concern.

Interconnects

After bonding, there is a need to realise an electrical connection between some modules from different strata. In this regard, an interconnect which bridges different layers is needed. Several methods have been used for this purpose including wire bonding [144] and TSV techniques [145]. Wire bonding is a technique which is widely used at the packaging level. This is one of the most mature interconnect techniques, but its density is a concern. The density of the bonded wires is limited for the sake of reliability as well as to avoid crosstalk problems [137].

Meanwhile, TSV refers to a process where the silicon substrates are totally etched through and metal connections are filled inside. Compared to the wire bonding technique, it has the advantage of high density, good reliability and less resistance as a result of its shorter length. Therefore, it is widely used in 3D integration technologies [145].

Other concerns in 3D integration

These three processes are major steps towards parallel integration. However, this does not mean the wafers or chips can be stacked infinitely. There are several concerns which limit the number

of the total stacks. One of the major concerns is the heat dissipation as a stack of various strata will greatly increase the heat generation so that the layout of the total system should be designed to accommodate this problem [146]. In practice, this problem is usually relieved by arranging the logic module near a thermal sink. Another problem in 3D integration is its success yield. For example, if the fabrication yield of each stratum is *x* and the success rate of making the inter-connect realisation is *y*, then for the 3D integrated system, the final success rate should be yx^n, where *n* represents the total number of layers in the 3D integrated system. It can be seen that, with more stacked layers, the yield of the entire system would greatly decrease. Therefore, the number of the stacked layers should be limited and determined by the yield and the cost [137].

2.2.2 Monolithic 3D electronics by printing techniques

While these strategies are all for parallel integration, they are more mature and some of them have been realised at an industrial level. Another strategy for realising vertical stacked electronics is monolithic 3D integration. This refers to a process where the entire system is realised in a layer by layer manner, starting from the bottom. This strategy provides more freedom from the material and device perspective. Considering that the focus of this study is on printable electronics, this section has only summarised the work on monolithic 3D integration by printing techniques.

Printing of quasi-1D materials for monolithic 3D electronics

As discussed earlier, quasi-1D semiconducting NWs can be printed in an aligned manner by a contact printing approach. This method is also capable of printing NWs on a 3D surface, which holds the possibility of the realisation of 3D integrated electronics. Demonstrated by Javey *et al.* [127], the 3D stacking of NW FETs has been successfully realised. This is achieved by layer-by-layer NW printing and FET fabrication (Figure 2.8). One crucial requirement of the 3D stacked devices is that the fabrication of the new layer should not impact the previous realised devices. For this, an isolation material is needed to electrically isolate the devices from the previous layers. In this work, a thick (300 nm) SiO_2 layer is deposited by PECVD or Ebeam evaporation as the intervening material, which largely preserves the electrical properties of the FET over the entire 3D integration process.

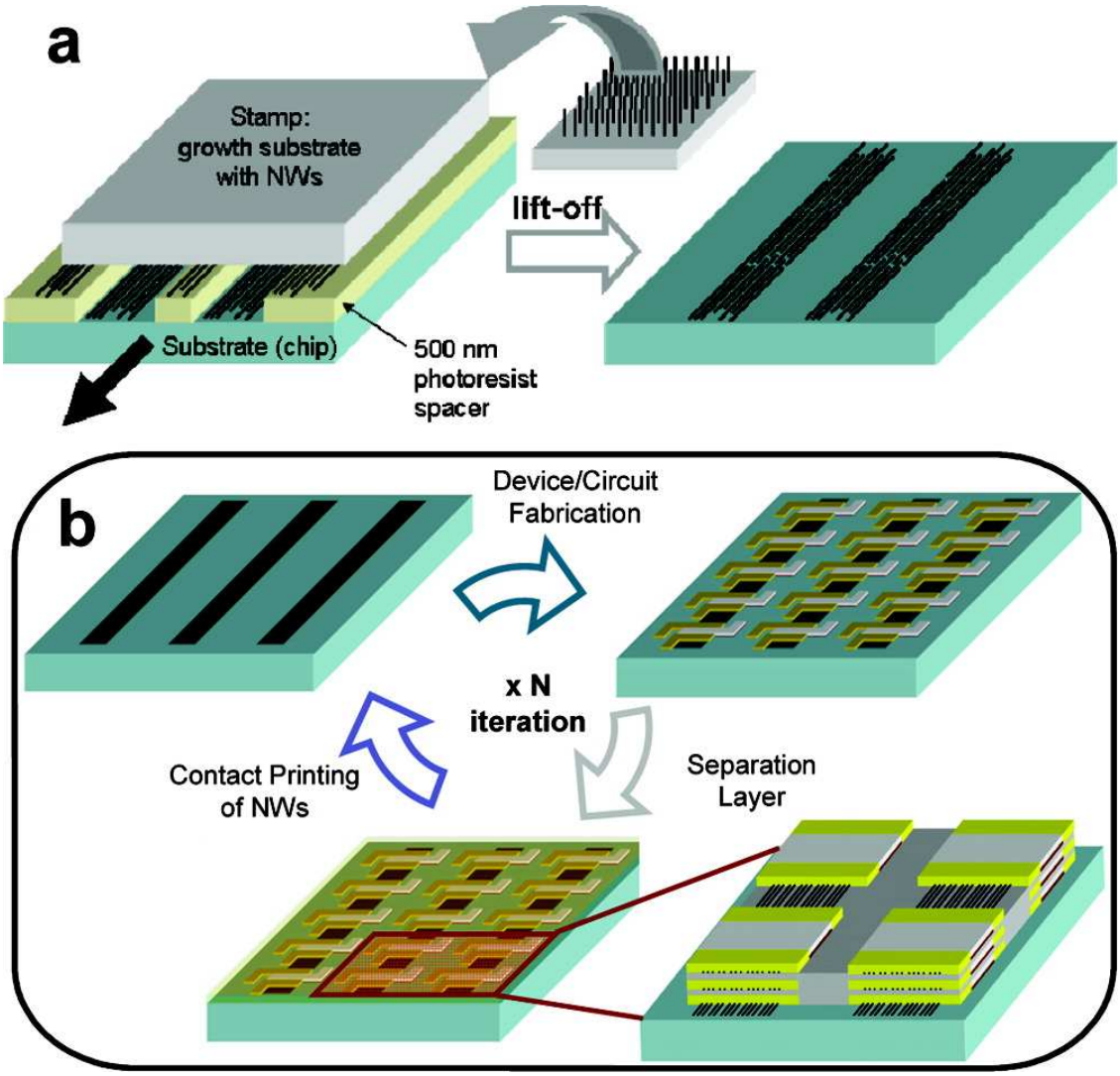


Figure 2.8: Contact printing NWs for the realisation of 3D electronics [127]. (a) The schema illustration of contact printing process. (b) The schema illustrating the method to achieve 3D integrated electronics. Reprinted and adapted with permission. (a) and (b) are from Ref [127]. Copyright © American Chemical Society.

This methodology is also capable of developing NW based electronics with more functionality on non-conventional substrate. For example, a NW based electronic system composed of NW logic devices and NW based floating memories has been successfully realised by printing NWs on a flexible Kapton tape [127].

Single wall, semiconducting CNT is another type of quasi-1D materials which can be used for device application. Demonstrated by Zhao *et al.*[147], the 3D integration of the CNT based circuits has been fabricated on flexible PI substrate. Taking advantage of the 3D integration, the p-type and n-type FETs can be realised on different layers with a common gate terminal (shared gate). In this regard, the fabrication process as well as the layout of the logic circuits, is greatly simplified. It should be noted that in this work a randomly distributed NW network

is used for the channel of the FET, which would lead to a degradation of the device performance.

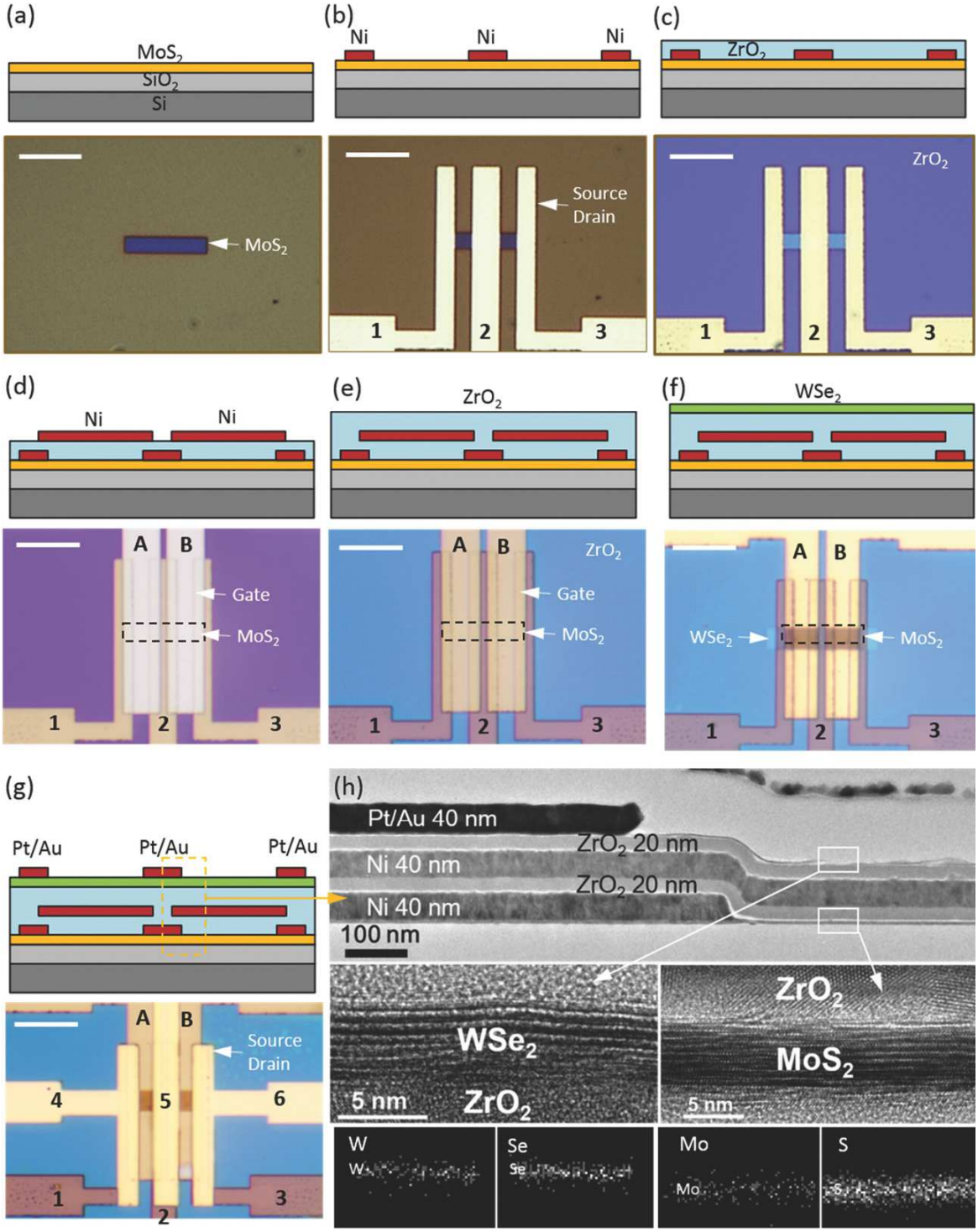


Figure 2.9: The fabrication process flow for realisation of 3D integrated electronics from quasi-2D materials and corresponding characterisation images. (a) Transfer of MoS_2. (b) Metallisation of the source and drain contacts for 1st layer device. (c) The deposition of dielectric material for 1st layer device. (d) The deposition of the shared gate electrodes. (e) The deposition of gate material for 2nd layer device (f) The transfer of WSe2 on the 2nd layer. (g) Metallisation of the source and drain contacts for 2nd layer device. (h) The TEM characterisation of the cross section of the fabricated 3D device. Reprinted and adapted with permission. (a) to (h) are from Ref [151]. Copyright © John Wiley and Sons.

Ideally, contact printed, highly aligned NWs could serve for the channel materials for the FETs, which could potentially lead to a higher performance.

Taking one step further, a concept of "X3D" was proposed and demonstrated to realise the heterogeneous integration of arbitrary NWs and NTs [148]. Benefiting from the advantages of each material, its 3D integration holds great promise for a wide range of applications. Moreover, this method also uses the same fabrication process for each layer, which greatly simplifies the process flow. Although the quasi-1D materials in this concept are realised by solution based drop-casting, dry printing techniques with aligned NWs/NTs can be potentially used and lead to better device performance.

Printing semiconducting 2D materials for monolithic 3D electronics

As alternatives for silicon, layered semi-conductors have shown great potential for various electronic applications including FETs and circuits. In addition, because of its ultra-thin nature, these materials are considered to be a promising candidate for flexible electronics [149, 150]. In the past fifteen years, various prototype devices based on 2D materials have been demonstrated on flexible substrates, but these have mostly been limited to a planar arrangement and the 3D integration of the 2D materials based devices have not been realised for a long time. First demonstrated by Sachid *et al.*[151], monolithic 3D CMOS have been successfully achieved with 2D materials in a laboratory scale demonstration with the EBL process. PMOS and NMOS were respectively fabricated by using WSe_2 and MoS_2 as the channel. A shared gate strategy was adopted to act as the common gate terminal for the devices on both layers. Compared to the 2D arrangement, the monolithic 3D layout provides an area reduction of 42%, as per design rules for the 14 nm technology node (Figure 2.9).

From the fabrication point of view, transfer printing is widely used in the study related to 2D material and this technique is potentially compatible with large-area flexible electronics. However, the current work is often limited within a small area on a rigid substrate. Two major barriers are in the way of its mass production. One is the large-area, high quality material synthesis and transfer; the other is the efficient contact realisation between metal and 2D materials, especially on flexible substrates. If these problems are overcome in the future, high-performance, printed electronics based on 2D materials over large area should be relatively straightforward.

Printing semiconducting organics for monolithic 3D electronics

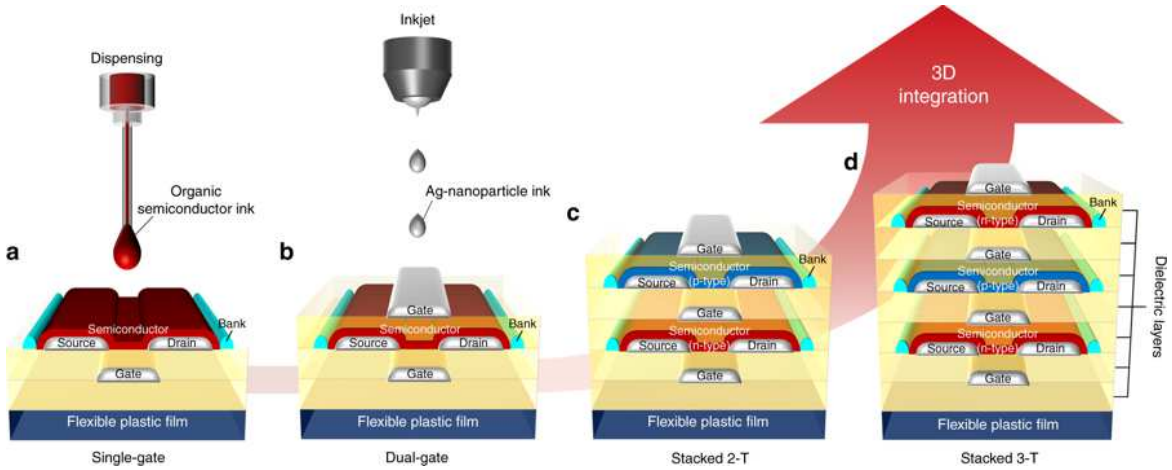


Figure 2.10: The schema showing the fabrication process flow to realise the 3D integrated electronics based on organic material by inkjet printing. (a) The realisation of single gate device. (b) The realisation of dual gate device. (c) The realisation of the vertically stacked two transistors by inkjet printing. (d) The realisation of the vertically stacked 3 transistors by inkjet printing. Reprinted and adapted with permission. (a) to (c) are from Ref [158]. Open access.

The exploration of organic semiconductors for electronic applications can be dated back to the 1980s [152], and since then extensive explorations have been made in this area to improve their performance as an alternative to Si [52, 53, 70, 90]. Although still not comparable to the Si based CMOS technology in terms of their electrical performance, organic materials have shown great potential in flexible electronics as a result of their low Young's modulus [35, 153]. To this end, some flexible electrical components, which do not require a high carrier mobility (e.g., display), have already been demonstrated in a laboratory scale demonstration and have been commercialised [154]. However, with regard to the 3D integration of organic based electronics, there was little exploration until 2008, when the stack of bottom gate, top contacted organic FETs, based on pentacene, were proposed and demonstrated [155]. The first prototype demonstration was realised by conventional micro-fabrication methods including lithography and metal deposition. A passivation layer was needed to protect the devices on the first layer from potential damage from the later micro-fabrication processes. In addition, since the operation voltage for organic FETs is usually higher than inorganic based FETs, the 3D stack of the OFETs would require a thick isolation layer, to totally isolate the electrical influence from the devices on different layers. In this regard, a 40 mm thick poly (urethaneacrylate) (PUA) layer was used for isolation as well as serving as the substrate for the fabrication of the second layer [155]. The 3D integration of the printed organic FETs was demonstrated few years later, where a drop-on-demand inkjet printer was used to print the semiconducting materials and the conductive contacts [156, 157] (Figure 2.10). In general, although the mobility of the OFET is

still limited~10 $cm^2V^{-1}s^{-1}$, the barriers to device yield and stability have been solved [157, 158], showing good promise for those low-end electronic components where high mobility devices are not required.

Finally, a table is made to compare the work have been done so far in the field of printed and 3D integrated electronics.

Table 2.5: Comparison of various parameters and strategies for 3D integrated electronics by printing techniques.

Channel Materials	Channel width/length	Source and drain contacts	Adopted printing method	Isolation layer and thickness	Targeted Applications	Ref #
Ge/Si (core/shell) NWs	200 µm/2 µm	Ebeam evaporated Ni	Contact printing	SiO_2 (~300 nm)	Flexible logic and memory circuits	[127]
Single wall CNT	100 µm/20 µm	Ebeam evaporated Ti/Au	Transfer printing	Si_3N_4 (NA)	Flexible logic gates and ring oscillator	[147]
MoS_2 and WSe_2	NA	Ebeam evaporated Ni and Pt/Au	Transfer printing	ZrO_2 (NA)	Digital and analog circuits on rigid substrate	[151]
P(NDI2OD-T2) and diF-TES-ADT	~900 µm /10~90 µm	Inkjet printed Ag	Inkjet printing	Parylene diX-SR film (230~440 nm)	Logic gates on rigid substrate	[157]
TU-3 and DTBDT-C6	~900 µm /10~90 µm	Inkjet printed Ag	Inkjet printing	Parylene diX-SR (NA)	Logic gates on flexible substrate	[158]

Note: P(NDI2OD-T2) refers to poly{[N,N´-bis(2-octyldodecyl)naphthalene-1,4,5,8-bis(dicarboximide)-2,6-diyl]-alt-5,5´-(2,2´-bithiophene)} and diF-TES-ADT refers to 2,8-Difluoro-5,11-bis-(triethylsilylethynyl)anthradithiophene. TU-3 denotes benzobis(thiadiazole) derivative and DTBDT-C6 denotes dithieno[2,3-d;2´,3´-d´]benzo[1,2-b;4,5-b´]dithiophene

2.3 Summary

This chapter has presented the state of the art in printed electronics, both from a material and technology perspective. So far, various materials, including conductors, semiconductors and dielectrics, have shown their compatibility with printing. Moreover, some of the printed

materials have shown an outstanding performance, which is comparable with the state of the art. This opens the possibility to realize high-performance, printed electronics. With these advancements, it is possible to achieve “all printed device”, as have been explored by some pioneering work listed in Section 2.1.4. Afterwards, several popular printing techniques, including inkjet printing, screen printing, contact printing and transfer printing have been reviewed and their applicability have been discussed. The possibility to extend each of these technologies to a roll-to-roll process has also been discussed.

Then, a discussion on the use of 3D integration technology in printed electronics has been provided. It starts with a brief review on various 3D integration techniques and then the focus is fixed on the monolithic 3D integration due to its compatibility with printed electronics. Several recent works on using printing methods, such as contact printing, inkjet printing and transfer printing, to realize vertical integration of electronic components have been discussed and compared.

Overall, this chapter clarifies the background of this Ph.D. thesis and highlights the importance of the printing technologies to the development of large-area, flexible electronics. Moreover, by adopting the vertical integration strategies, some of the fundamental limitations of printed electronics, such as low density of devices, can be alleviated. These also lay the foundation for the rest of work presented in this thesis, which aims to print NWs and graphene for large-area, flexible electronics.

3. Chapter 3. Printing nanomaterials on rigid and flexible substrates

As was discussed in Chapter 2, the printing approach has been regarded as one of the most promising strategies for large-area, flexible electronics. This chapter presents an experimental study on the printing process of several kinds of nanomaterials, which will be later used for the development of 3D integrated electronics. Specifically, Section 3.1 discusses the printing of the quasi-1D NWs. A shear force assisted printing method was used to transfer and align NWs from donor to receiver substrates. In order to obtain controllable printing over large-area, a home-made set up was developed with a close-loop control on the printing parameters over the entire process. The as-printed NWs were analysed by SEM. In order to compare the printing results quantitatively, an image analysis process has been adopted, which vectorises the NWs in the SEM images and analyses the results automatically. With these two prerequisites, the NW printing mechanics were studied, especially on soft (flexible) and uneven (3D) surfaces (Section 3.1.3).

In Section 3.2, the transfer printing process for 2D material (graphene) is discussed. A detailed experimental process flow has been provided to transfer chemical vapour deposition (CVD) grown graphene from copper foil to other substrates. The as-transferred film is subjected to a rapid thermal annealing (RTA) treatment and characterised by various tools including AFM, Raman, and electrical characterisation. The quality of the transferred film is evaluated.

The final part of this chapter (Section 3.3) presents a study on the screen printing process for interconnect application. Basic properties of the screen-printed Ag films are analysed and characterised. The as-printed layer will be used for the later development of flexible and 3D integrated electronics.

3.1 Printing of quasi-1D NWs for large-area, flexible electronics

Vertical NWs (ZnO and Si) synthesised by top-down and bottom-up approaches were used in this study and printed by a shear force assisted process (contact printing, see Section 2.1.5). As has been discussed in Chapter 2, contact printing was developed to directionally transfer quasi-1D materials. Since its development, studies have been carried out in this area on both the printing mechanism and the realisation of functional devices by using this method. However, some gaps still exist in this field, especially for the NWs' printing process achieved on flexible and uneven substrates. To this end, this section provides the experimental details for the

realisation of NW printing on flexible and uneven substrates as well as the characterisations of the as-printed NWs. In addition, the NW printing mechanism has been explored in a series of comparative studies. This section is arranged as follows: (1) a brief literature review is made to clarify why and how NW is good for flexible electronics (3.2.1); (2) a contact printing set-up has been developed and tested to achieve precisely controlled, uniform NW printing over large-area (3.2.2); (3) an image analysis process has been set up to quantify the figure of merits from printed NWs (3.2.3); (4) with these two prerequisites, the NW printing mechanism has been explored under various conditions (3.2.4).

3.1.1 Why and how NW is good for flexible electronics?

With the advent of the end of Moore's law, there is a shift from using bulk semiconductor materials to their low dimensional counterparts for electronic application, which could potentially address the physical limitation in individual device realized by CMOS technology. NW is one of the quasi-1D materials with the diameter ranging between 1 nm to 100 nm. Due to its high aspect ratio and low dimension, it has many unique properties, such as quantum confinement effect, enhancement of sensitivity to external stimuli, etc [91, 93, 124]. Moreover, the NW show significant higher bendability than its bulk counterpart, which holds a great promise in developing next generation flexible electronics. During the last two decades, sustained efforts have been made in using NWs for various flexible device applications including FETs, photovoltaics, sensors, LEDs, etc [159-161]. This thesis focuses on using ZnO NWs for FETs and UV photodetector applications, especially in a printable manner. Here, a short review on NW synthesis and alignment techniques have been summarized below and their compatibility with flexible electronics is clarified.

NW Synthesis

Generally speaking, there are two philosophically different approaches to synthesis NWs, which are top-down and bottom-up methods [162]. Top-down approach refers to a process where bulk material is selectively etched to achieve NW. This can be realized by wet method, with the use of noble metal as catalyst; or by means of dry etch such as RIE [162]. Such methods could potentially achieve NWs with extremely fine diameter, but its surface smoothness and further crystalline structure should be carefully examined.

Meanwhile, the bottom-up method focuses on the synthesis of NWs from molecular growth, which comprises chemical vapor deposition (CVD), molecular beam epitaxy (MBE), laser ablation and solution-based growth and etc [162]. Among these, the CVD method is the most popular one because of its low cost and high quality outcome. So far, such technology is mature enough to produce the NWs with uniform diameter, controlled doping concentration, well

defined NW-to-NW spacing and reasonable NW length, which lays a strong foundation in using NWs for various electronic applications [162].

However, it should be noted that despite of these achievements, most of the NW synthesis methods are realized under harsh conditions and are not compatible with flexible substrate. In order to tackle this, one general strategy is to transfer the as-synthesized material onto the flexible substrate is needed.

NW Transfer

There are multiple criteria of a good transfer of NWs, such as control over the NW density, alignment, transfer yield, etc. Overall, a highly controlled NW transfer technique is still a matter of interest in the research community. Towards that, several methods have been developed so far such as Langmuir-Blodgett (LB) method, Blown bubble method, field-assisted alignment and contact printing method [163]. While all of these methods are compatible with flexible electronics, most of them requires the use of liquid in the transfer process, which can have negative impact on the devices realized based on that as discussed in Section 2.1.2. By contrast, contact printing can be realized in a dry condition, with high transfer yield, good NW density and alignment, as have been previously discussed in Section 2.1.5. Therefore, this thesis adopted the contact printing method for the later study.

3.1.2 A home-made, close-loop controlled contact printing set-up

Although the contact printing method has been known for over a decade [17], an instrument which can precisely control the printing parameter over the entire process has not yet been reported. In this section, a home-made, close-loop controlled contact printing setup has been realised, with the aim of achieving uniform NW printing over a large area. This also lays the foundation for further studies of the contact printing process, since each experiment can be controlled precisely with this set-up.

The contact printing process principally involves two steps: (a) the realisation of conformable contact between the donor substrate (with vertically grown NWs) and the receiver substrate at certain pressures; (b) the sliding of a donor with respect to the receiver at certain speeds. To meet these requirements, a set-up comprising of several linear stages integrated on a load cell was developed (Figure 3.1). This was achieved by cooperation with Dr. Carlos Garcia Nunez. Specifically, the researcher conceived the general idea of the setup and assembled the individual components. Dr. Nunez made the Labview code which enables the close-loop control on the printing parameters.

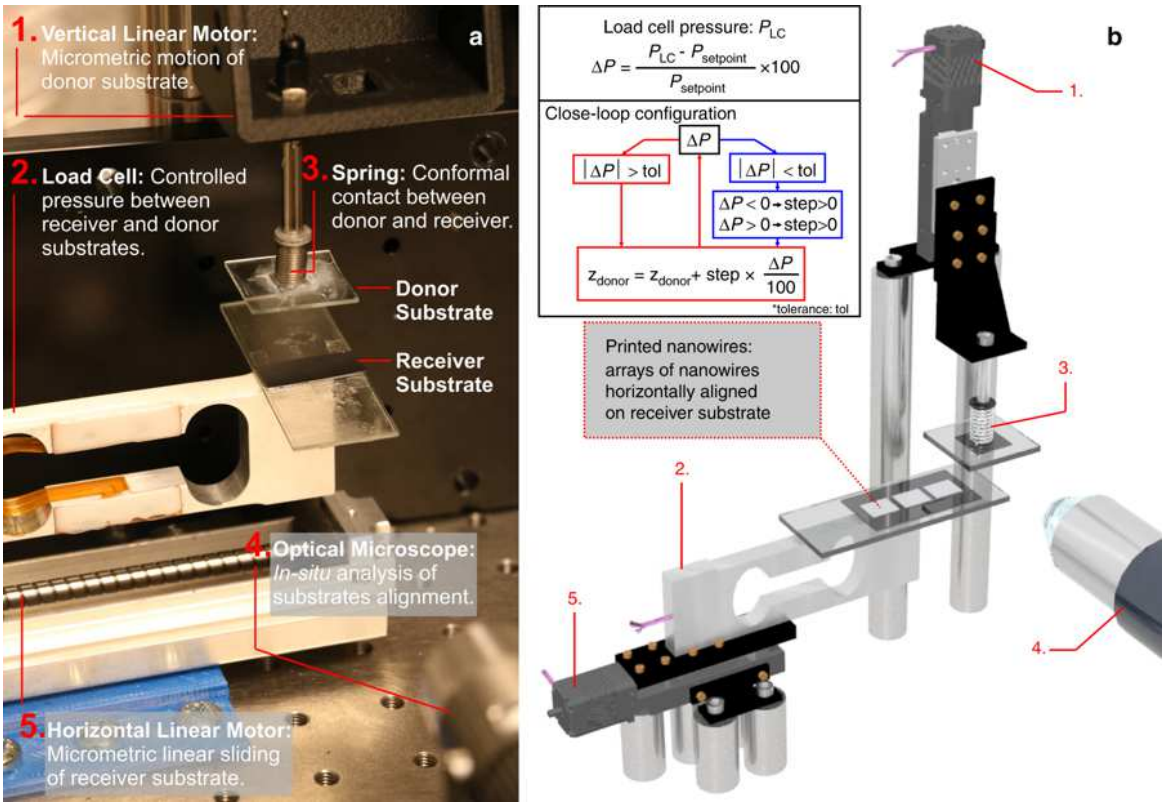


Figure 3.1: The photograph (a) and the schematic illustration (b) of the contact printing setup, version 1. Reprinted and adapted with permission. (a) and (b) are from Ref [176]. Open access.

Figure 3.2: The self-adjustable platform used in the 2nd version of the contact printing system.

As illustrated in Figure 3.1a, the contact printing system consists of five parts, which are: (1) a linear motor which could move vertically; (2) a load cell which enables the monitor of the contact force; (3) a spring which enables a conformable contact between the donor and the receiver substrate; (4) an optical microscope which enables the *in-situ* observation of the entire process and (5) another linear motor which is able to move horizontally to provide the sliding motion. The logic diagram of this home-made contact printing system is shown in Figure 3.1b.

Briefly, the load cell (2) monitors the force applied by the vertical motor (1). By comparing this value with the set-point, the later movement of the vertical motor can be determined and the motor moves downwards (upwards) if the monitored force is less (larger) than the set-point. Such close-loop control of the force is executed during the entire printing process, with a force difference tolerance of 2.5%. By using this arrangement, a precise control of the force to the set point throughout the printing process can be guaranteed. Meanwhile, the sliding of the receiver substrate is determined by the horizontal linear stage (5) with a precision given in micrometres. These are two important aspects which guarantee the controllable and uniform NW printing.

Another aspect which governs successful NW printing is the conformable contact between the donor and the receiver substrates throughout the sliding, without which the uniform NW printing cannot be achieved. In the first version of the contact-printing set-up, this aspect was realised by a spring-attached platform. While this arrangement can facilitate the conformable contact under static scenario, it cannot be guaranteed for the sliding process, especially when the sliding motion is fast. To solve this problem, the second version of the contact printing set-up was developed.

In the second version a self-adjustable platform has been developed. This part of the work was carried out by Mr. Adamos Christou. The design is shown in Figure 3.2, which includes two adjustable platforms. Each platform can only be tilted uniaxially. When the two stages come into contact, the self-adjustable mechanism could lead to a conformable contact between the two platforms.

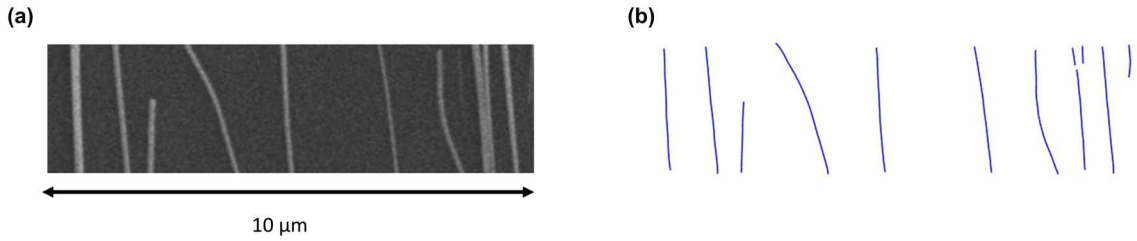


Figure 3.3: Validation of the modified software to vectorise the NWs from the SEM image. (a) A specifically cropped SEM image, with the image width covering 10 µm; (b) the vectorised NWs from the software. It should be noted that ZnO NWs are used in this validation but this method is applicable for all the types of NWs.

3.1.3 An image analysis approach

The as-printed NWs are characterised by scanning electron microscopy (SEM). To study the results in a reliable and efficient manner, an automatic approach to quantify the performance of the NW printing is needed. To this end, open source software was adopted with slight

modifications. The software was developed and used by other researchers to evaluate the alignment of organic nanofibers by vectorising the quasi-1D materials in the characterisation images [10], and such a process was found to be compatible with inorganic NWs as well. The software modification was done by Mr. Christou and details of this are not included in this thesis.

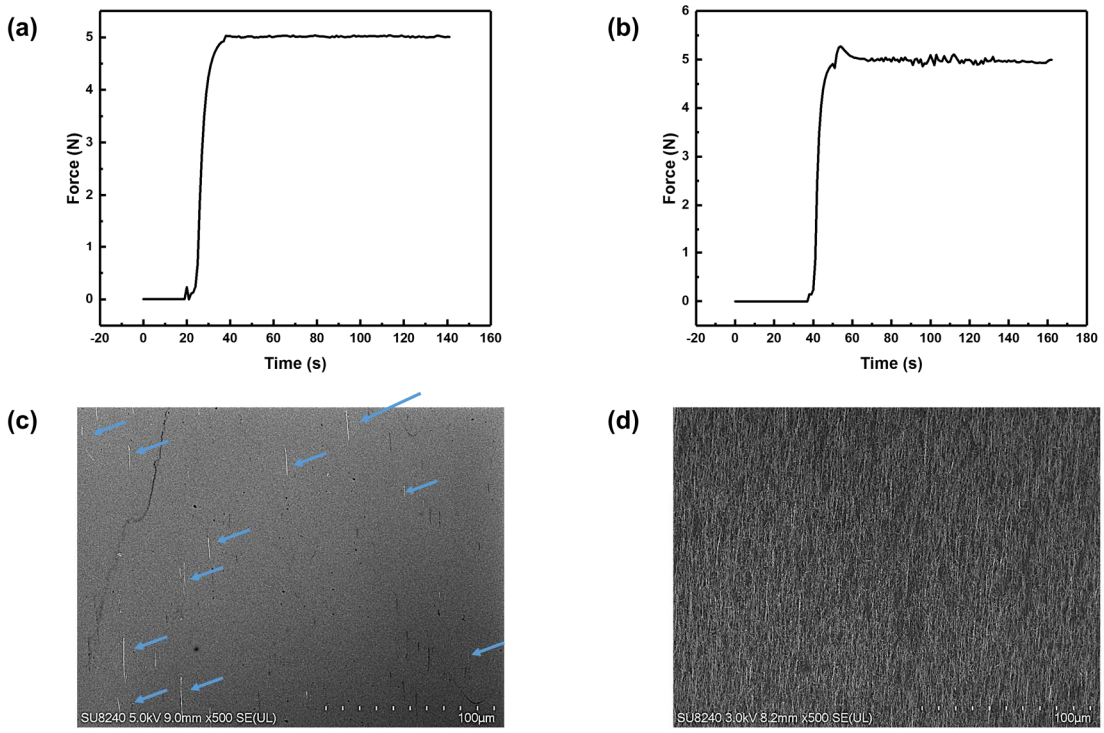


Figure 3.4: The comparison between the wet and dry printed NWs. (a) and (b) show the contact force applied in the wet and dry printing process, respectively. (c) and (d) show the SEM characterisation of the printed NWs from the wet and dry printing, respectively.

The modified process was first validated on a SEM image of small size (10 µm in width) with clearly defined ZnO NWs (Figure 3.3). There are twelve NWs in the original SEM image while in the vectorised image, twelve NWs are recognised and plotted. The largest value in terms of length and width of NWs from the original image was measured to be ~2.58 µm and 200 nm, respectively. The recognised values for these two parameters from the software were ~2.6 µm and 198 nm, respectively. These are two important figures of merit in analysing NW printing performance, and the results from the two approaches (hand measuring and software measuring) were almost the same, indicating a successful NW identification and size measurement. It should be noted that there are still some minor discrepancies between the original and vectorised images, which usually originate from a bundle of NWs or very fine (thus very dim in the SEM image) NWs. However, since the chance of such a recognition error is not high, this modified software is still regarded as a reliable and efficient method to quantify

the NW printing process. Other important parameters, such as NWs linear density (/µm), NWs area coverage (%), NWs alignment and the average length and width of NWs can also be automatically obtained from the output of the software.

3.1.4 The study of the NW printing mechanics

Wet and Dry printing

With the second version of the contact printing set-up, a comparative study between wet and dry printing was realised. Wet printing involves the use of mineral oil (from Sigma Aldrich) as lubricant in the printing process. Dry printing refers to a process where no liquid is used. Two donor substrates (in similar size) with ZnO NWs grown under the same conditions were used in this study. The receiver substrates are Si with 300 nm SiO_2 layer. The printing force was set to 5 N. As can be seen in Figure 3.4, by involving lubricant in the NW printing, the process is

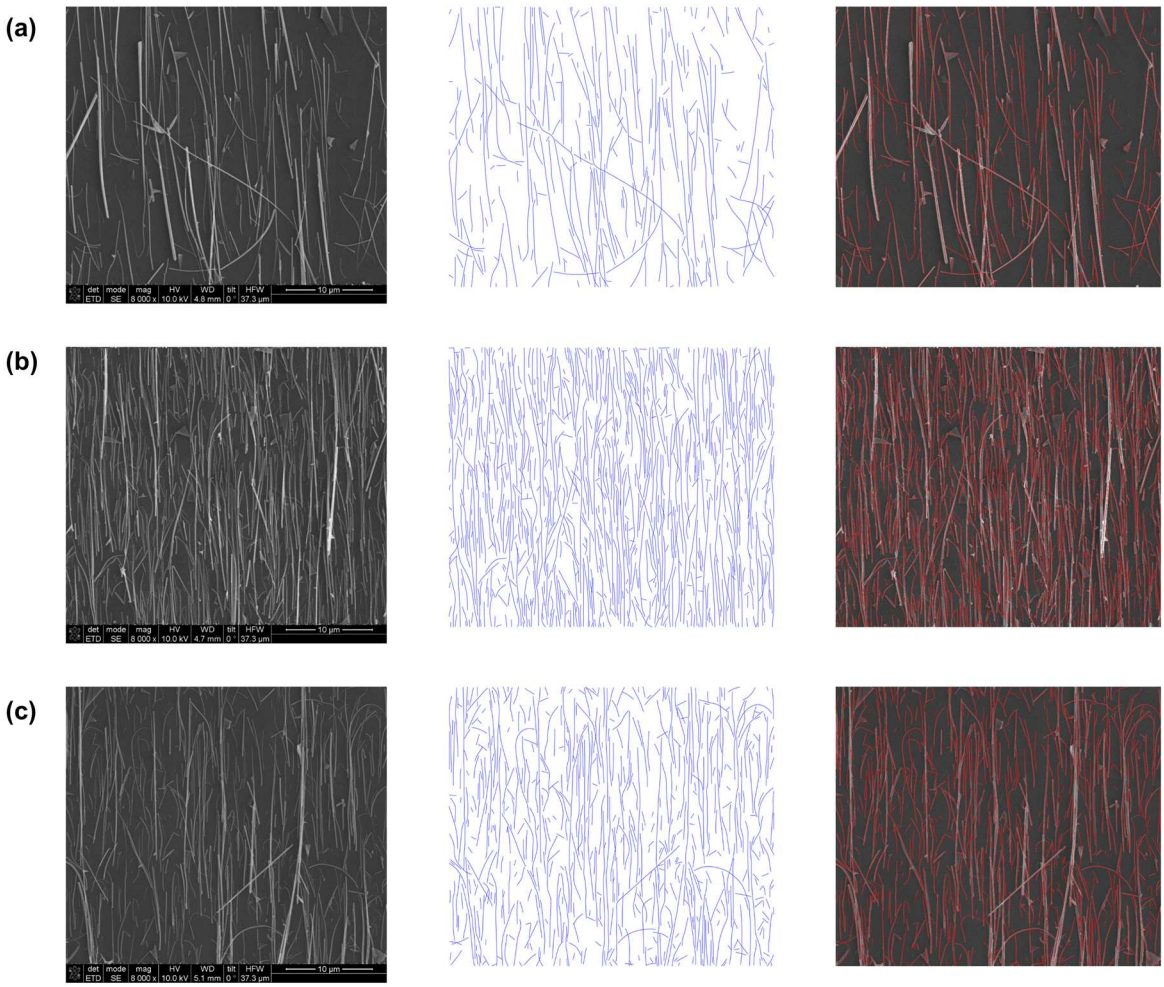


Figure 3.5: The SEM image of NWs printed on Si/SiO_2 substrate (a) without plasma treatment; (b) and (c) with plasma treatment. The results shown in (b) was printed within 30mins after plasma treatment while in (c) the NWs were printed after 24hrs after plasma treatment. The images on left, middle and right represent the original, the vectorised, and the overlapped images, respectively. Copyright © 2019 IEEE. Reprinted, with permission, from [164].

smoother: the use of lubricant significantly reduces the friction between the donor and the receiver substrates (Figure 3.4a). In the case of dry printing, the fluctuation of the force is larger, indicating a bumpy motion (Figure 3.4b). The printing results obtained from the two processes appear to be completely different although the donor and receiver substrates are almost the same. NWs are loosely distributed on the substrate which was printed with the lubricant, (Figure 3.4c), showing a low transfer yield of the NWs. By contrast, in the case of dry printing, densely packed NWs can be seen on the substrate surface with a good alignment (Figure 3.4d). This big difference between the two samples can probably be attributed to the difference in friction. With larger friction, a higher chance of NW breakage is expected, leading to a higher transfer yield. In order to achieve a high NW density, a dry printing approach is used in all later works. However, it should be noted that this conclusion contradicts the observation from a previous study [17], where it was suggested that the use of lubricant enhances the printing performance, leading to a higher NW printing yield and better NW alignment.

Effect of oxygen plasma treatment

Then the effects of oxygen plasma treatment to the NW's printing process has been studied and this study has been published in a conference proceeding [164]. Three donor substrates of similar size were used in this study, with NWs grown under the same conditions. With regards to the receiver substrates, three different conditions were used; (A) no plasma treatment; (B) and (C) oxygen plasma treated at 150 W for two minutes. For sample B, the printing process was done within thirty minutes of the plasma treatment. For sample C, the printing process was done twenty-four hours after the plasma functionalisation. The results of printed NWs are shown in Figure 3.5. The figure shows that, with oxygen plasma treatment (Figures 3.5b and

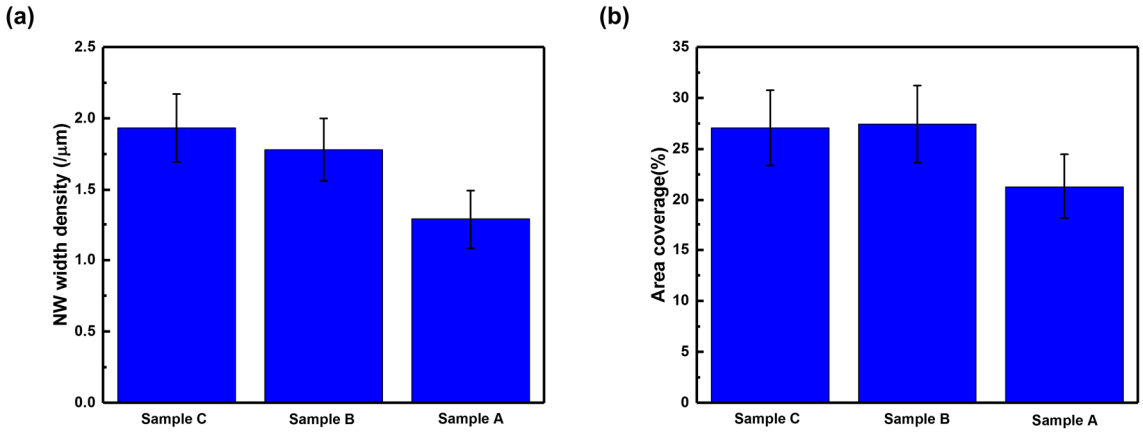


Figure 3.6: Comparison of width density (a) and area coverage (b) for ZnO NWs printed onto Si/SiO_2 substrates treated under different conditions. Copyright © 2019 IEEE. Reprinted, with permission, from [164].

c), the printed NWs show higher density. This is also confirmed by the data analysis shown in Figure 3.6: without the oxygen plasma treatment, both the width density and area coverage are relatively low, with a value of 1.29 / µm and 21.3%, respectively. With plasma treatment, the two figures of merits both increased (1.93 / µm and 27.1% for sample B, 1.78/µm and 27.4% for sample C). It is, therefore, possible to conclude that oxygen plasma offers some improvement to the NW printing process. This is probably because of the OH- group generated by plasma, which leads to a larger interaction between the receiver substrates and the NWs.

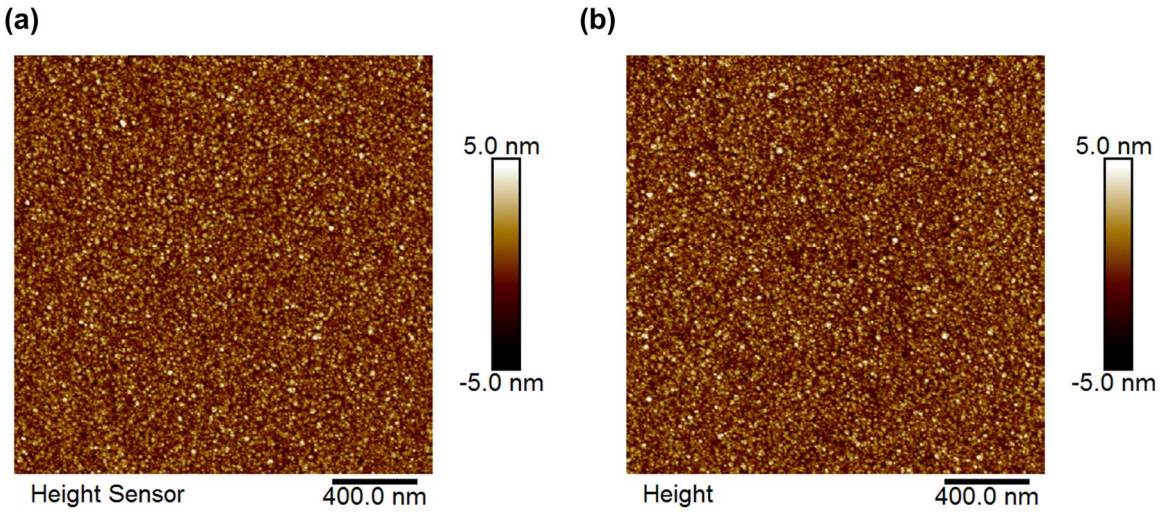


Figure 3.7: The AFM characterisation of the (a) rigid substrate and (b) flexible substrate. The rigid substrate refers to the Si/SiO_2 wafer deposited with 100 nm Si_3N_4, while the flexible substrate refers to the spin-coated PI film deposited with 100 nm Si_3N_4. The carrier wafer for the spin-coated PI film is Si/SiO2. Copyright © 2019 IEEE. Reprinted, with permission, from [164].

This result also aligns with a previous study in NW printing where particular SAM on the receiver substrate was found to increase the NW transfer yield dramatically [17]. Moreover, the plasma effect seems quite persistent under ambient condition, as can be seen from Samples B and C. As a result, the receiver substrates were treated by oxygen plasma for two minutes in all later comparative studies.

NW printing on rigid and flexible substrates

In order to understand the NW printing process on flexible substrates, a series of comparative studies have been carried out. Two types of receivers were used: the first is a Si/SiO_2 wafer, which is usually used as the rigid substrate for realising electronic devices and the second is a silicon wafer with spin-coated PI film on top; the PI was spin-coated at 4000 rpm for 1 min and cured at 250 °C for 1 hour. After curing, it can be mechanically peeled off from the carrier wafer, which leads to a freestanding flexible substrate. Previous studies indicate that the change

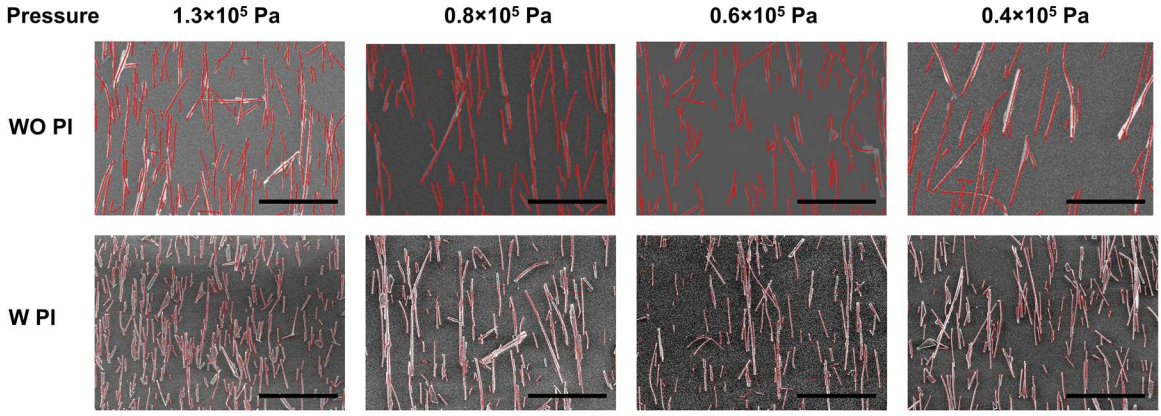


Figure 3.8: The SEM characterisations of the NWs printed onto rigid and soft substrates under various pressures. WO and W represent without and with, respectively.

in surface roughness/materials can lead to a significant difference in the NW printing results [128]. In order to exclude such effects, a 100 nm Si_3N_4 layer has been deposited on top of both types of samples by a PlasmaPro System 100 ICP180 RIE. By doing this, the difference in the printing results can only come from the difference in the substrate's hardness. This is further confirmed by the AFM characterisations from both substrates. As shown in Figure 3.7, the surface morphology of the two substrates appear to be similar, with surface roughness R_a~1 nm.

The NWs were printed at four different pressures ranging from 0.4×10^5 Pa to 1.3×10^5 Pa, and characterised by SEM. Typical examples of the SEM images from each printing conditions have been shown in Figure 3.8.

As shown in the figure, the NWs printed on PI substrates show a shorter length, but the printed NW density becomes higher. These observations have also been confirmed by the statistical data obtained from over 3 locations from each printing condition, as illustrated in Figure 3.9.

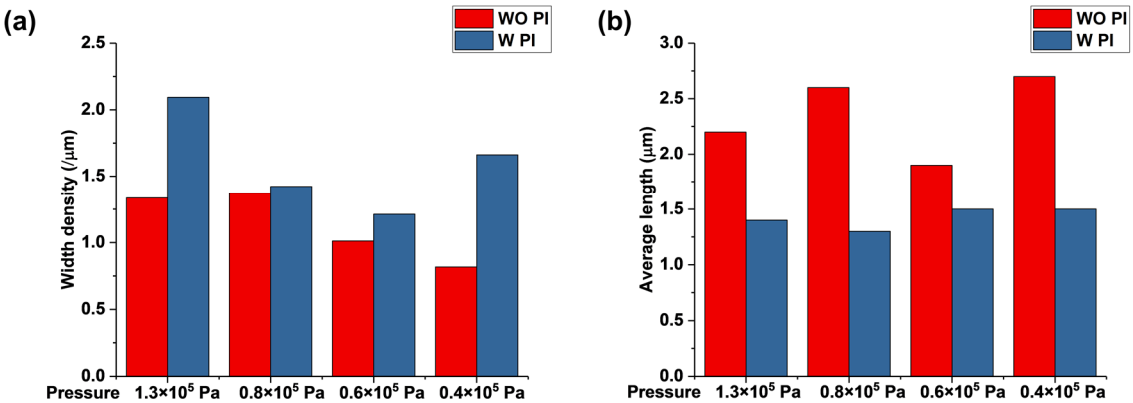


Figure 3.9: The statistical results of the NWs printing performance onto rigid and flexible substrates. (a) and (b) shows the width density and average length of the printed NWs under different pressures, respectively.

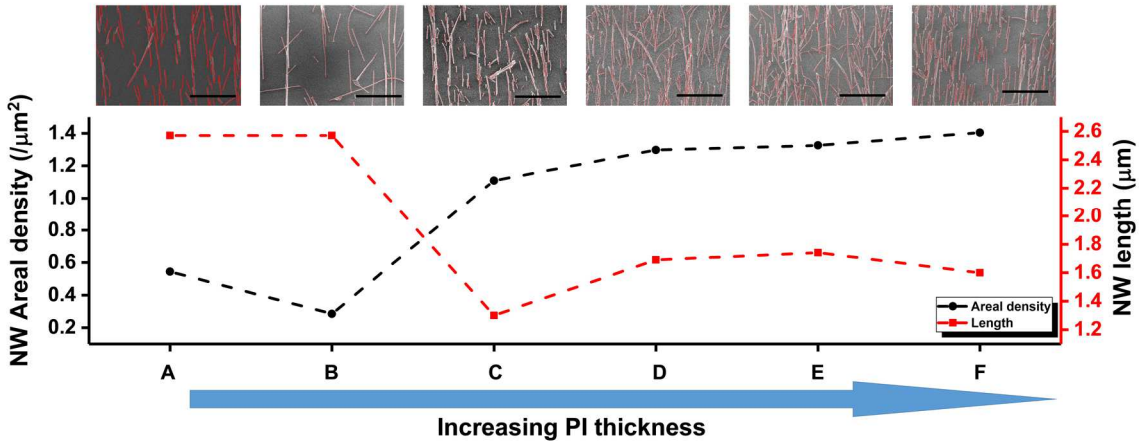


Figure 3.10: ZnO NWs printed onto PI film with various thickness.

Notably, the width density of the printed NWs does not show a clear dependence of the printing pressure, which may indicate that this parameter only plays a minor role in the NW printing process and can be easily obscured by other extrinsic factors. But we do observe a threshold pressure for successful NW printing: below a certain pressure, the NW cannot be printed in an aligned manner. Nevertheless, all the pressures used here are above that threshold so that successful NW printing was carried out.

In order to further understand the NW printing mechanism on flexible substrate, the NWs were printed onto PI films of various thickness and the details of the receiver substrates are summarised in Table 3.1. Like the previous study, a 100 nm Si_3N_4 layer was deposited on top of each receiver substrate to exclude the influence from any other factors such as surface roughness and materials. All the printing experiments were carried out at the same printing pressure (~0.8×10^5 Pa) with the same donor substrates (ZnO NWs).

Table 3.1: Details for various receiver substrates used in the contact printing study.

Substrate	Carrier substrates	PI processing conditions	Thickness of PI film
A	Si/SiO_2	Not coated	0
B	Si/SiO_2	Spin-coated at 8000 rpm for 60s, once	1.35 μm
C	Si/SiO_2	Spin-coated at 4000 rpm for 60s, once	1.64 μm
D	Si/SiO_2	Spin-coated at 2000 rpm for 60s, once	2.66 μm
E	Si/SiO_2	Spin-coated at 2000 rpm for 60s, three times	9.12 μm

F	Si/SiO_2	Spin-coated at 2000 rpm for 60s, five times	13.89 μm

As can be seen from Figure 3.10, the thickness of the PI film does play a role in the NW printing process. When the PI film is very thin (conditions A and B), the length of the printed NWs is relatively longer, but fewer NWs can be printed (less areal density); when the PI film is thicker (conditions C, D, E, F), more NWs can be printed onto the receiver substrates but they are shorter in length. This observation is also consistent with phenomenon shown in Figures 3.8 and 3.9. It should be noted that point C does not follows the overall trend proposed here, which can be attributed to the experiment error. Actually, although each data point is calculated from more than 5 SEM images, the experimental error in each experiments is unavoidable. However, based on the results showing in Figures 3.8 and 3.9, and also the later results shown in Section 5.3, it is reasonable to conclude that the NW printed on flexible substrates shows shorter length. Here, a qualitative explanation is given to explain the observed phenomenon. Figure 3.11 shows the schema where a donor substrate with NWs is brought into contact with the receiver substrate. Assuming all the NWs are rigid and non-bendable, then only part of the NWs from the donor can be in contact with the receiver substrate, if the surface of the receiver substrate is also rigid (Figure 3.11a). However, if the surface of the receiver is soft, because of the

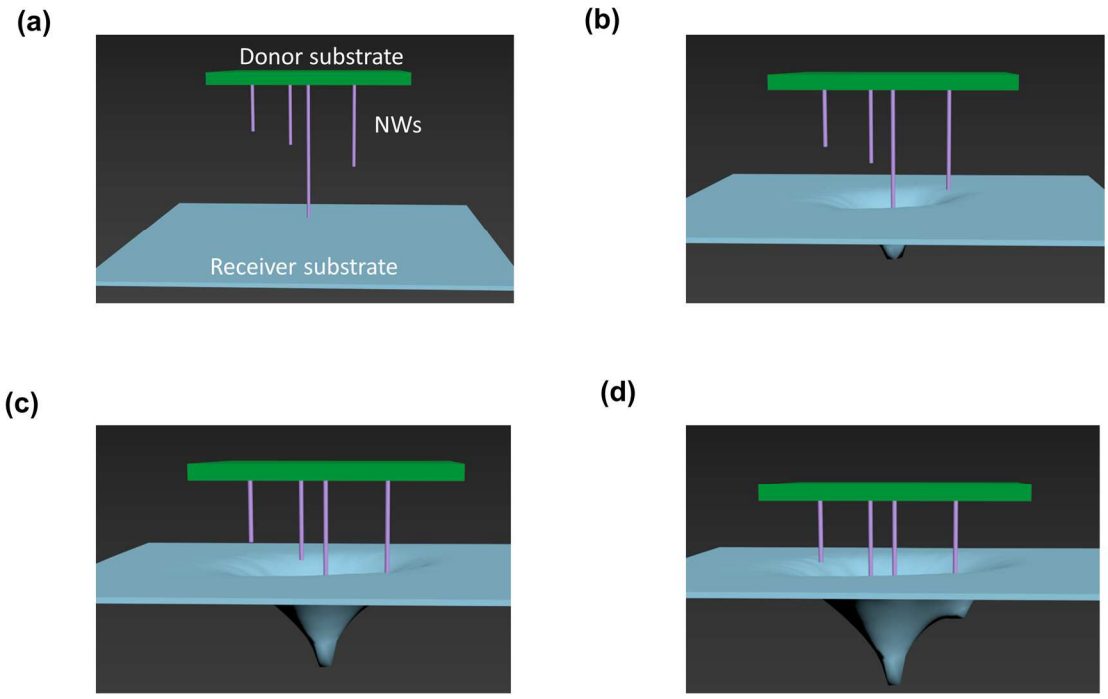


Figure 3.11: The schemas showing NW printing on receiver substrates with different deformability.

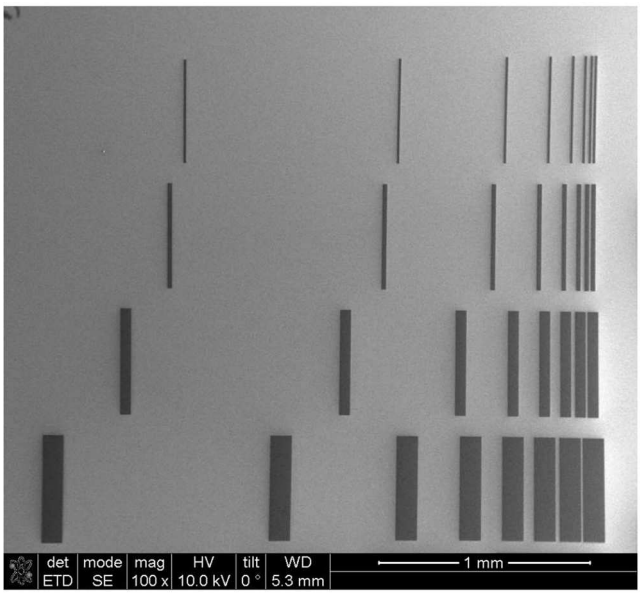


Figure 3.12: The SEM image showing the surface of the receiver substrate with various features on top.

deformation of the surface, more NWs can be brought into contact with the receiver substrates, which may lead to a greater chance of NW transfer (phenomena seen in Figure 3.8 and 3.9). The more deformable the receiver substrate that is used, the more NWs will be in contact and transferred (Figure 3.10). This is one possible reason for the impact of the PI's thickness on the

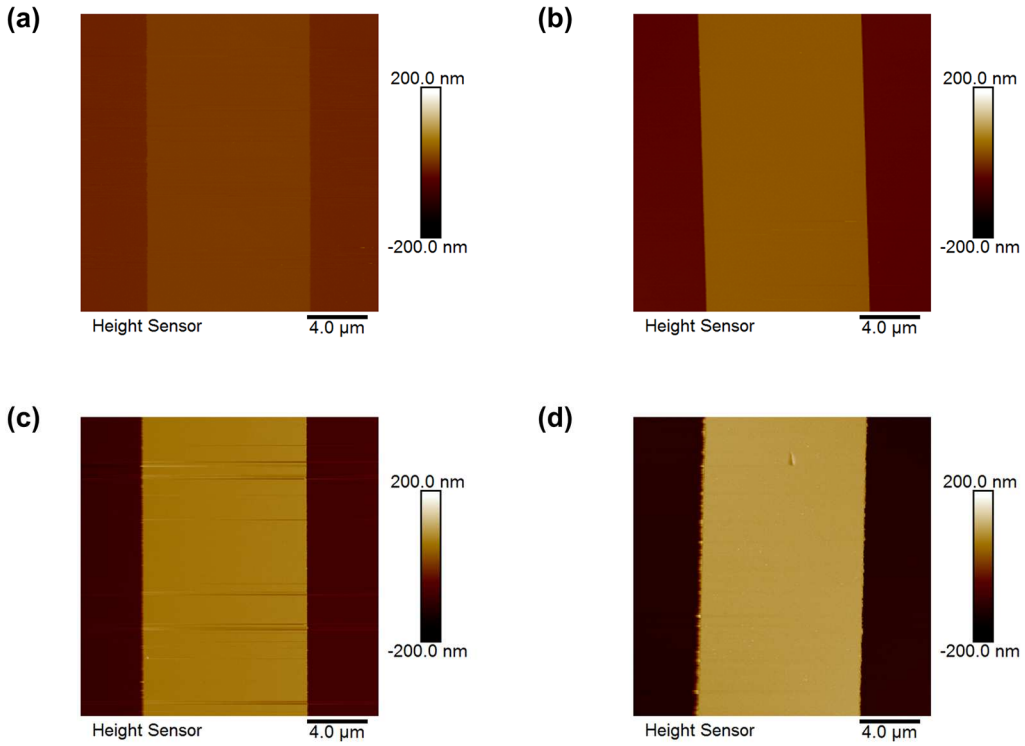


Figure 3.13: The AFM characterisation of the receiver substrates with features of various height.

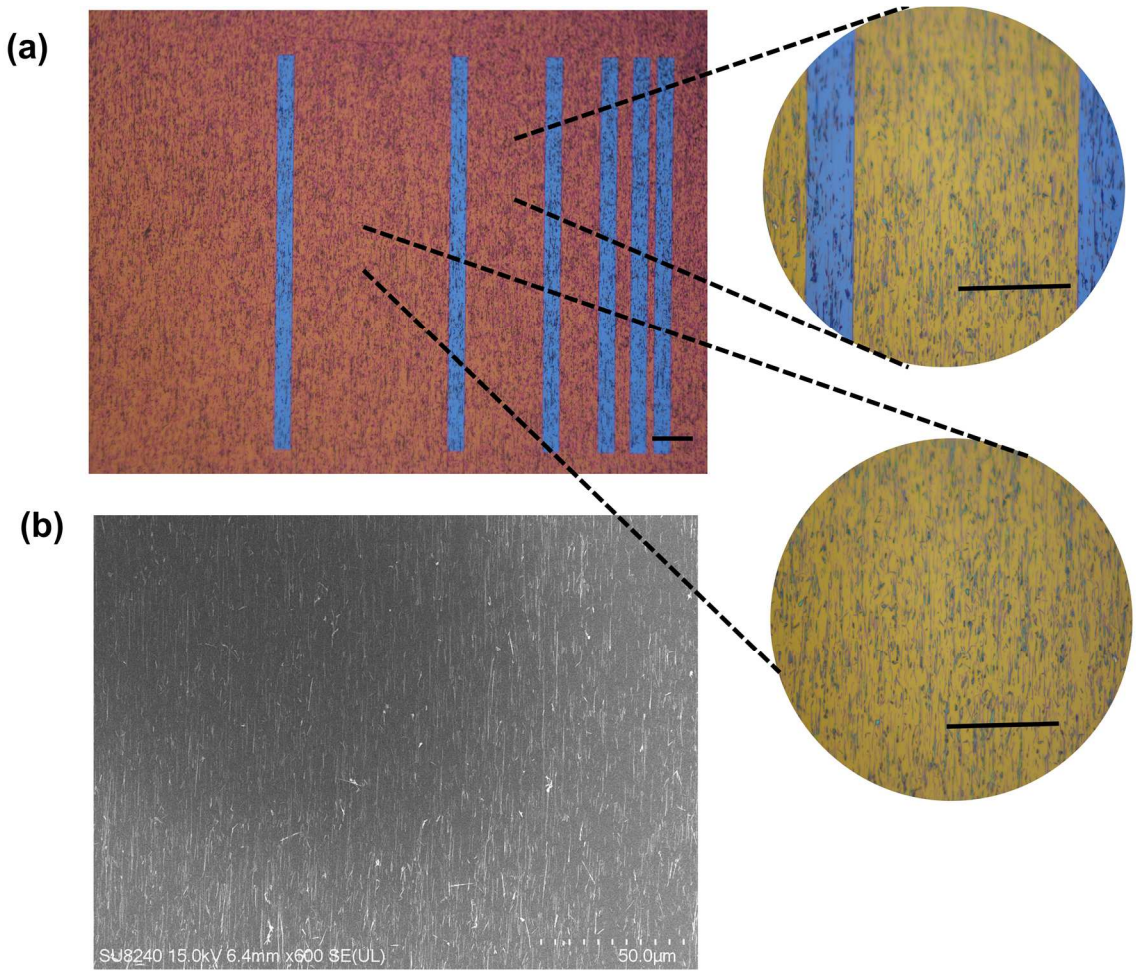


Figure 3.14: Images of NW printing onto uneven substrate. (a) The optical microscope image showing the NWs printed on the receiver substrate with features of 20 nm. All the scale bars are 50 µm. (b) The SEM characterisation of the printed NWs.

NW printing. The real case can be more complicated since both the NWs and the surface of the receiver substrate are deformable. This only gives a qualitative explanation for the NW printing process on flexible substrate. In addition, the change in NW length as observed in Figures 3.8-3.10, has not been clearly clarified and well understood. In order to obtain a deeper understanding of the NW printing mechanism, the finite element method (FEM) is required to simulate the breaking conditions of NWs on flexible substrate. However, since this deviates slightly from the main aim of this thesis, this study has not been included in this section and can be considered for possible future research.

NW printing on non-planar surface

Finally, the NW printing on non-planar surface is briefly explored. Metal lines with various width and spacing (see Figure 3.12) were realised on silicon substrates with different thicknesses ranging from 20 - 200 nm. Similar to the previous study, a 100 nm Si_3N_4 layer was

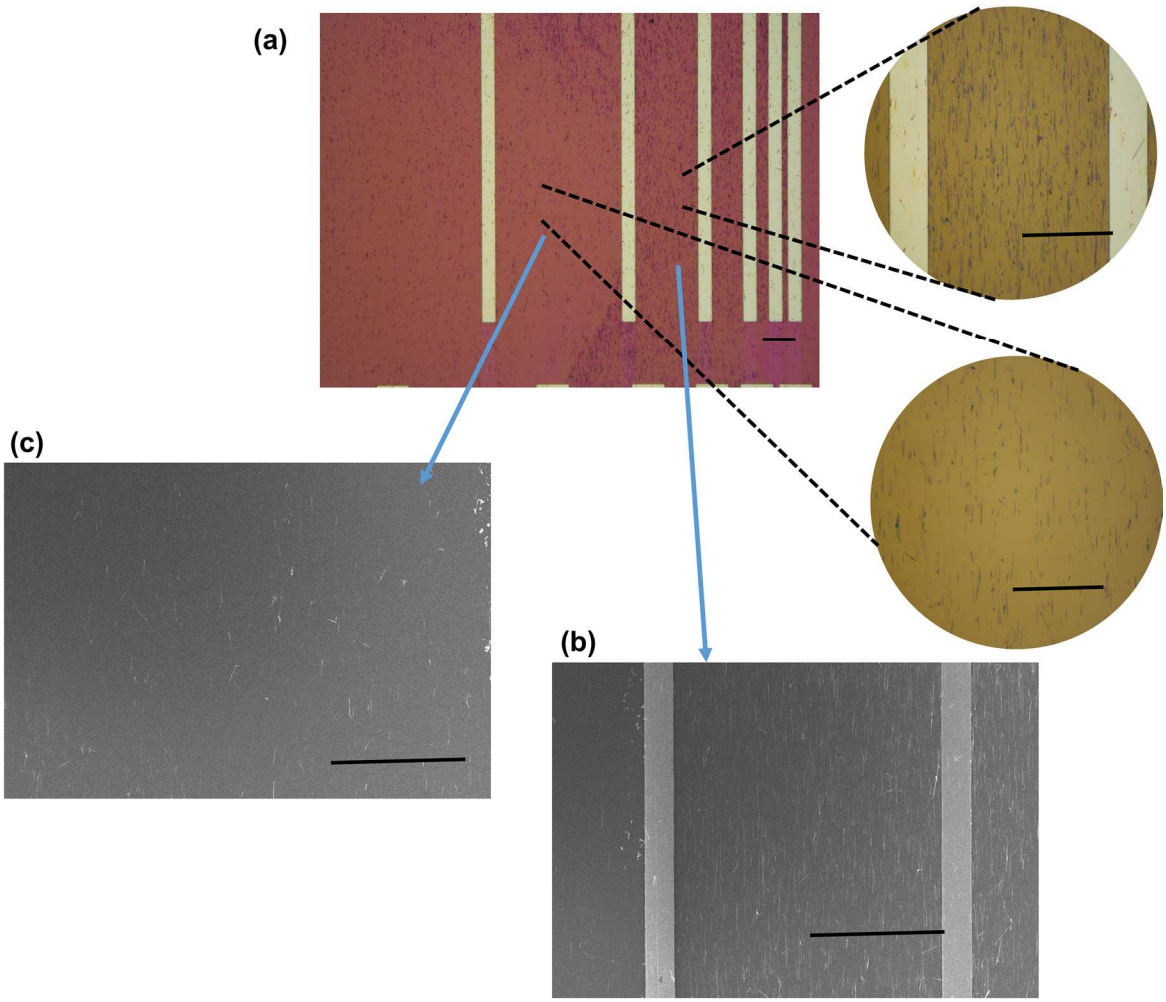


Figure 3.15: Images of NWs printed onto uneven substrates. Optical microscope (a) and SEM images (b and c) showing the results of NWs printed onto uneven substrates, with the printing direction parallel to the feature direction. All the scale bars are 50 µm.

deposited on each sample in order to maintain the same surface condition. Before printing, AFM was used to characterise the surface of the receiver substrates and the results are shown in Figure 3.13.

ZnO NWs were synthesised under the same conditions on a Si substrate and these were used as the receiver substrates. The printing pressure was kept as ~ 0.8×10^5 Pa for all the samples. After printing, an optical microscope, together with SEM, was used to characterise the NW printing results. Interestingly, as shown in Figure 3.14, when the features realised on the receiver substrate are low in height (i.e. 20 nm), the NWs were printed uniformly across the entire substrate. This may indicate that, such small geometry change does not have a significant impact on NWs printing; the NWs diameter is ~100 nm. However, by increasing the height of the features on the receiver, the difference in the printing becomes significant. For a feature height of 200 nm, a significant NW density modulation can be seen. The density of the printed

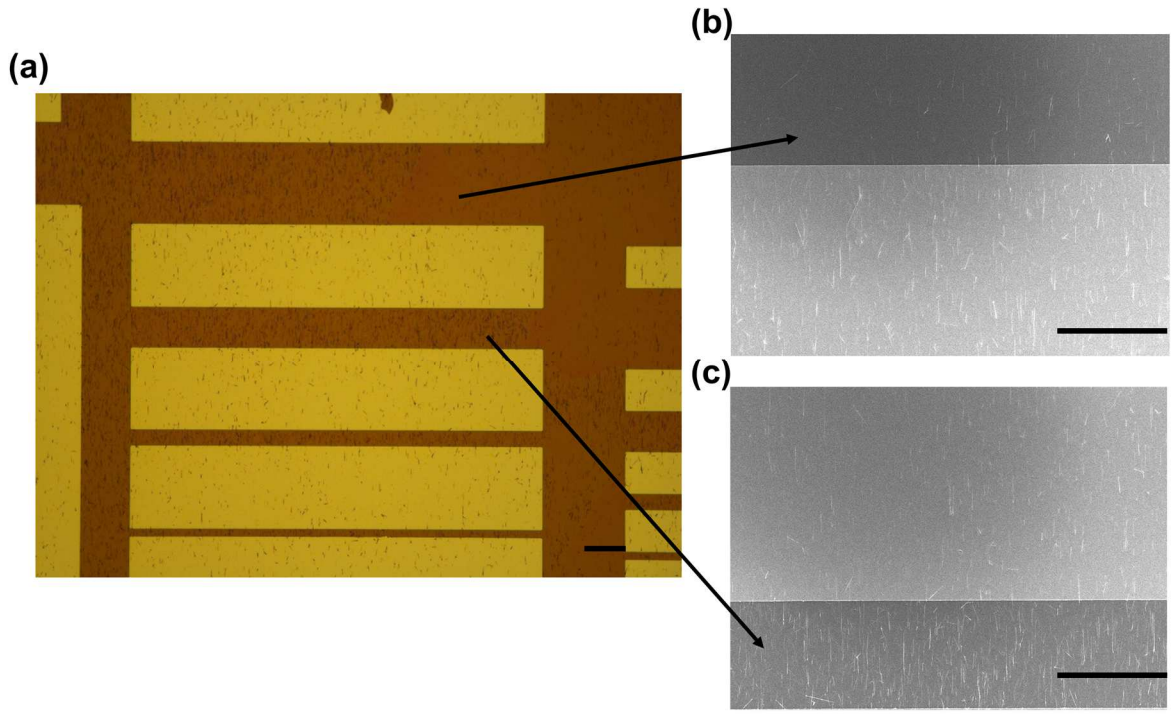


Figure 3.16: Characterisation of NWs printed onto uneven substrates. Optical microscope (a) and SEM images (b and c) showing the results of NWs printed onto uneven substrates, with the printing direction perpendicular to the feature direction. All the scale bars are 50 µm.

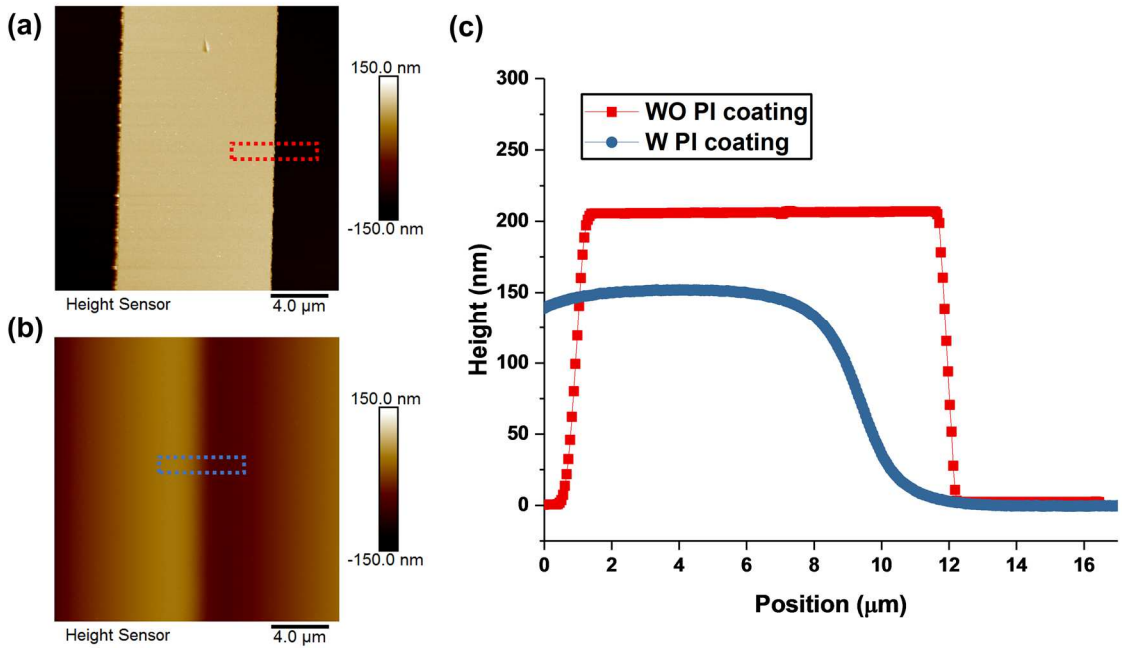


Figure 3.17: The AFM characterisations of the features before and after flattening. (a) and (b) The AFM scans of the features before and after PI flattening. (c) The line profiles of the box indicated in (a) and (b).

NWs is lower in the areas with surface features and higher in the featureless areas (gaps). Meanwhile, the width of the gap and the printing direction also seem to play significant roles

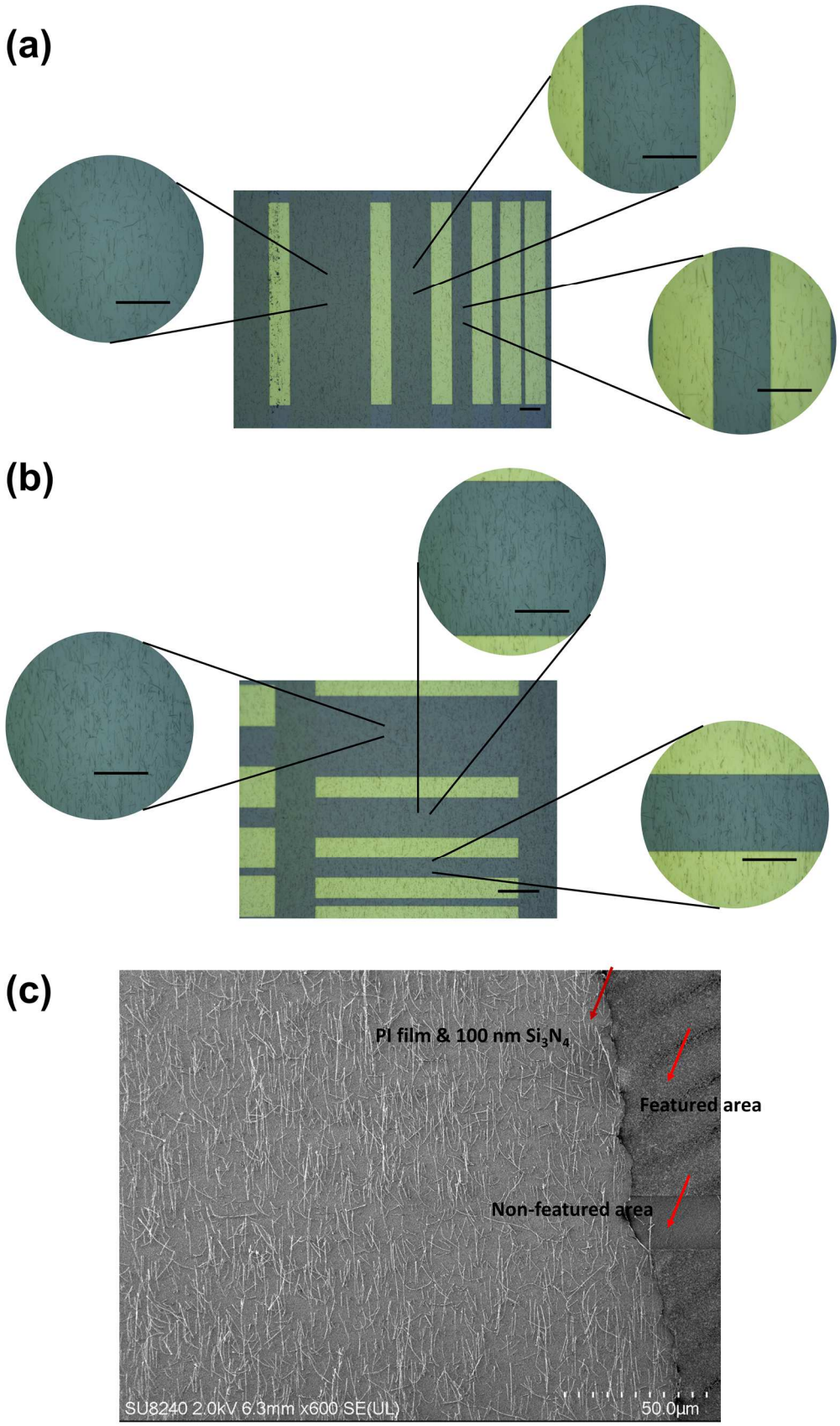


Figure 3.18: Images of NWs printed onto flattened substrates. (a) and (b) Optical microscopy images (c) SEM images. All the scale bars are 50 µm.

in the NW printing process, as shown in Figures 3.15 and 3.16. This opens a new avenue in

how to control the printed NW density. By creating gaps with enough depth, NW printing can be effectively confined inside. However, since this study also slightly deviates from the aim of this study, detailed exploration has not been carried out. The major aim of this research is to obtain a uniform NW layer by using a printing method.

In order to realise uniform NW printing on the non-flat receiver substrate, a flattened step has been adopted. A PI film has been spin-coated on the receiver substrates at 4000 rpm for one minute and cured at 250 °C. After coating, the sample was characterised by AFM and compared with the non-coated sample. As shown in Figure 3.17, the surface of the non-coated sample shows an abrupt change in height between those featured and non-featured areas. However, with a PI film spin-coated on top, this change in height becomes alleviated and the surface of the receiver substrate has been flattened. The same printing experiments have been carried out on these flattened receiver substrates and are characterised by an optical microscope and SEM. As can be seen in Figure 3.18, the NWs were printed uniformly on both the featured and non-featured areas. Therefore, by doing so, uniform NW printing in a layer-by-layer manner can be successfully achieved. This strategy will be later adopted in the 3D integration and a detailed study on PI processing will be included in Chapters 6.

3.2 Transfer printing graphene for large-area, flexible electronics

3.2.1 Why and how graphene is good for flexible electronics?

Graphene is a single layer of graphite. It is composed of one layer of carbon atoms packed in the honeycomb lattice. Due to its special crystal lattice, the band structure of graphene is unique: at K-points, it can be regarded as a Dirac cone as shown in Figure 3.19 [165, 166]. The bottom of the conduction band and top of the valence band merges at one point, which is the Dirac point. And the carrier density of graphene is zero when its fermi level is at Dirac point.

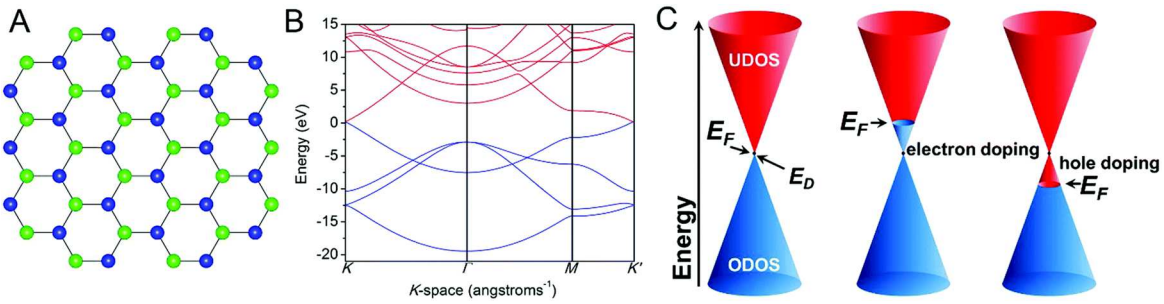


Figure 3.19: The lattice and band structure of graphene. A The honeycomb lattice structure of graphene. B The calculated band structure of graphene. C The schema showing the liner dispersion relationship near the Dirac cone. This figure is reused from Ref [166]. Copyright © The Royal Society of Chemistry.

Since its conduction band is in contact with valence band, graphene is regarded as a semi-metal. However, unlike the conventional metal with large and untunable carrier density, the carrier density of graphene can be modulated by tunning its fermi level [166]. This opens the possibility of using graphene as an active material for FET application which is explored later in this thesis.

Another unique property of graphene is its liner dispersion relationship (E-κ). Unlike many other semiconductors with "parabolic-like" band structure, the carrier in graphene is Dirac fermions, which behaves as a realistic particle with zero rest mass [166]. This leads to many unique electrical property, such as a certain value of conductivity even at dirac point, quntum hall effect with half integral filling factors, etc.

Graphene is also regarded as a material with record mechanical strength: the Young's modulus of the single crystal graphene film is 1 TPa and the breaking strength is 42 N/m [167]. However, in practice, the defect free single crystal film normally exists in small area and when it comes to large-area polycrystalline film, defects and grain boundaries can significantly affect its mechanical properties. For polycrystalline CVD graphene, interestingly, as suggested by an experimental study, its mechanical property is almost as good as a single crystal film, which implies a broad industrial application of CVD graphene [168]. Meanwhile, as a quasi-2D material, it has a great flexibility. Being strong and flexible, graphene is regarded to hold great promise in flexible electronics.

Synthesis

So far, many methods have been developed to synthesis graphene, such as mechanical exfoliation, chemical exfoliation, laser reduction, epitaxial growth on SiC and CVD method [165]. Among them, the mechanical exfoliation method is able to produce the graphene film with highest quality. However, the obtained sample size is limited to several to tens of micrometre. In this regard, it is not suitable for large-area electronics [165]. Meanwhile, chemical exfoliation and laser reduction method are able to produce large-area graphene in a short time. However, the obtained products are of many defects, functional groups and dangling bonds, which is not feasible for high-performance FET application [165]. And in this regard, these methods are not adopted in this thesis. Considering the requirements in both quality and quantity, the CVD method is one of the best method for graphene synthesis. Therefore, CVD grown graphene was used to realize FETs and circuits in this Ph.D thesis.

To give a complete view of the process flow, a description of the CVD process is provided as follows: in CVD method, graphene was synthesized with the use of metal catalyst. Copper is one of the most common type of catalyst which could lead to monolayer graphene coverage

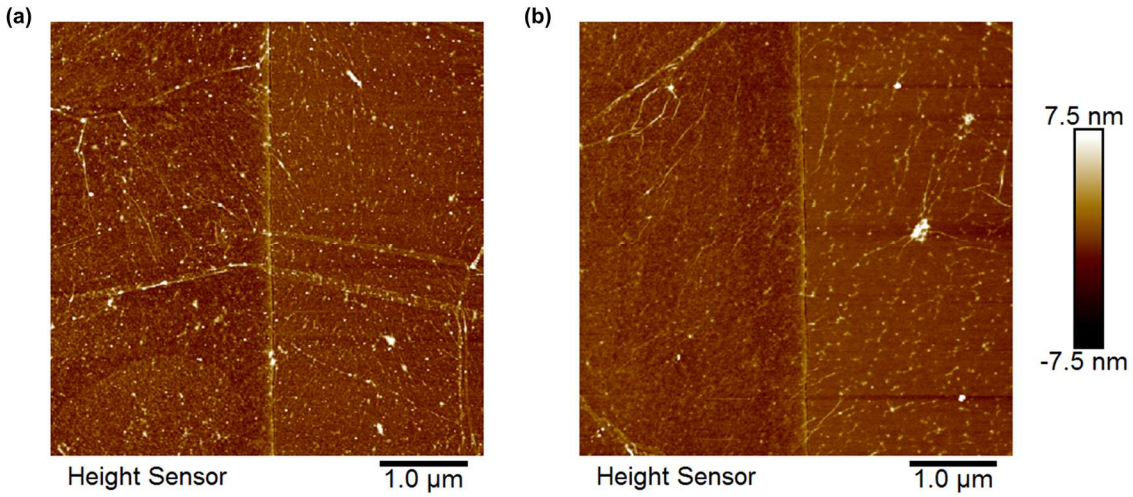


Figure 3.20: AFM characterisation of the transferred graphene. (a) as-transferred film (b) transferred film after a thermal annealing process in an RTA furnace.

[165]. The process is realized in a CVD furnace at a temperature between 1000 °C to 1075 °C. Prior to the synthesis, normally an annealing process of the copper foil is adopted. The annealing temperature is between 1050 °C to 1100 °C, which aims to smooth the surface of the copper foil. The smooth copper surface is one key factor which guarantees high-quality graphene synthesis with large domain. After annealing, a mixture of gas of CH_4, Ar and H_2 is introduced to the CVD chamber. The CH_4 serves as the carbon source, decomposes at high temperature, gets adsorbed at the surface of copper foil and finally forms graphene. H_2 has dual roles in the graphene growth process, which is a) acting as a surface active agent for carbon element and b) etching the graphene. The change of the ratio of CH_4:Ar has been proved to affect the morphology and domain size of the synthesised graphene [165]. After synthesis, the furnace is cooled down to room temperature with the protection of Ar.

With regards to the CVD graphene used in the later work, it was purchased from Graphenea. (https://www.graphenea.com/collections/buy-graphene-films/products/monolayer-graphene-on-cu-4-inches). But in general, the synthesis process flow is similar to the one described above.

3.2.2 The graphene transfer process

In order to realise electronic devices from the CVD-synthesised graphene on the desired substrates, a transfer process is needed. Until now, various methods have been developed to achieve the graphene transfer process. These processes were detailed in the researcher's Master's dissertation as well as in some of previous publications from other researchers [120, 131, 169]. As a result, it is not the main focus of this thesis. However, since this process was

frequently used in the later studies, a general process flow is included here for a complete view of the entire device fabrication.

The transfer process starts with the spin-coating of a PMMA solution on top of copper foil with graphene at the rotation speed of 2000 rpm for one minute (twice). The spin-coated sample was then dried at room temperature for four hours. Afterwards, the rear of the copper foil was etched by a short (20~30 s) and mild (100 W) oxygen plasma to remove the graphene grown on the rear side. In order to transfer graphene, the treated copper foil was etched by a $FeCl_3$ solution, leaving the PMMA/graphene bilayer in the etchant. This bilayer film then underwent a critical cleaning process to thoroughly clean the bottom surface of the film [120]. Finally, the bilayer was rinsed in IPA and transferred onto the desired substrate at 150 °C [16]. After transfer, the PMMA support layer was removed by acetone and acetic acid. It should be noted that this transfer method is compatible with various substrates including polyimide (PI) film with Au contacts. This process will be used in work described in Chapter 4 to realise an array of GFETs directly from transfer printing.

The as-transferred film was then subjected to an annealing step (250 °C for 10 mins) in an RTA system. Figure 3.20 shows the AFM characterisation results from the as-transferred graphene and the transferred graphene after annealing. As shown in the figure, more polymer residues and wrinkles can be seen on the graphene surface before thermal annealing, which indicates that a process like this does help to clean the surface of graphene [170]. Generally, there are several criteria for a high quality transfer of the graphene film: (1) the surface of the transferred

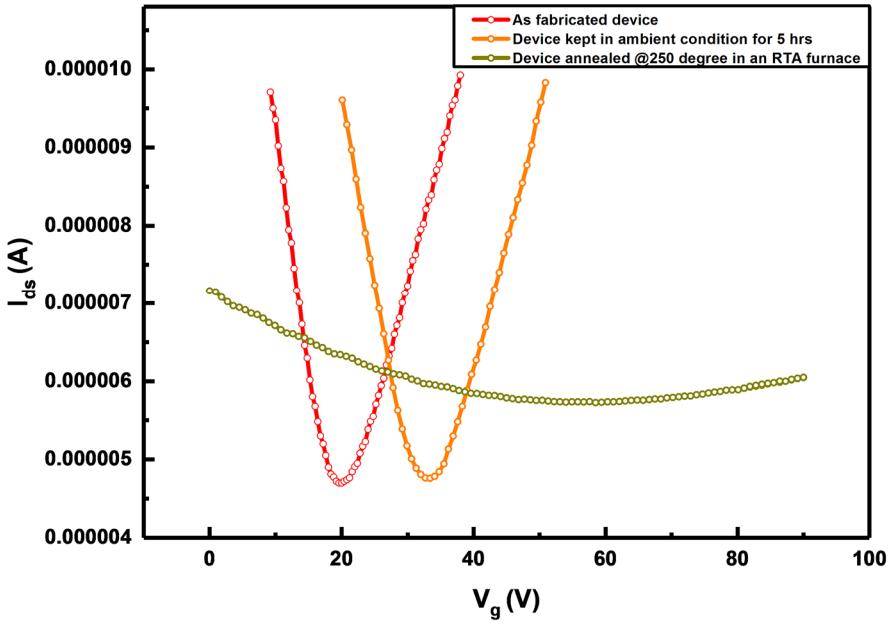


Figure 3.21: The change of the transfer curve of GFET under different conditions

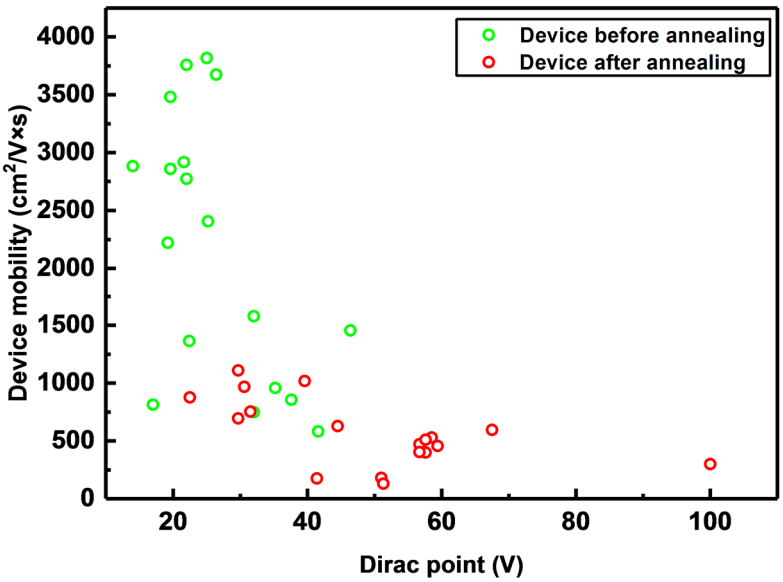


Figure 3.22: Device performance of GFETs before and after the thermal annealing in an RTA furnace at 250 °C.

graphene should be clean without other contaminations; (2) the film should be intact with minimum material loss (pores); (3) the doping of the transferred film can be controlled. Therefore, it is important to monitor the doping and the quality of the transferred graphene film except for the surface cleanness. To further analyse these factors, a batch of GFETs was fabricated and the device performance was measured before and after annealing (fabrication details can be found in Chapter 4). As can be seen in Figure 3.21, the Dirac point of the as-fabricated devices is ~20 V. By exposing the device to the ambient condition for ~5 hrs, the Dirac point was shifted to ~34 V. This is probably because of the p-type doping effect from the oxygen and water vapour in the air [16]. However, after the annealing process, the Dirac point of the GFET was shifted to ~60 V along with a significant decrease in the on/off ratio. This indicates that the graphene quality was strongly disturbed and degraded after the RTA process, leading to a poorer device performance. This phenomenon was further confirmed by analysing the field-effect mobility and the Dirac point for the entire group of devices. As can be seen in Figure 3.22, by annealing the graphene FETs in the RTA system, the device mobility decreased drastically with a strong p-type doping introduced to the channel. As a result, the annealing step was avoided in all later fabrication processes.

In this section, the device mobility was extracted by a fitting method [171]. However, this approach considers the contact resistance to be constant under all carrier densities, and would usually lead to a higher estimation of the charge carrier's mobility. A more precise way to extract contact resistance and device mobility is to use a four terminal measurement method,

which will be adopted in Chapter 4 to systematically study the contact problem in printed electronics.

3.3 Screen printing of conductive electrodes for interconnect application

Interconnects are required for electrical communication in 3D integrated electronic systems. Normally the height difference between adjacent layers is in the range of micrometres. In order to realise a reliable electrical connection between the devices that feature different layers, especially under bending conditions, a thick and preferably stretchable metal film is required. Because the resolution needed for an interconnect is not high (feature size of ~100 µm), a screen printing approach, together with a stretchable silver paste, was adopted for this purpose. The stretchable silver ink (PE873) was purchased from DUPONT^{TM}. And detailed information regarding the silver ink can be found in the supplier's website: https://www.dupont.com/content/dam/dupont/amer/us/en/products/ei-transformation/documents/PE873.pdf.

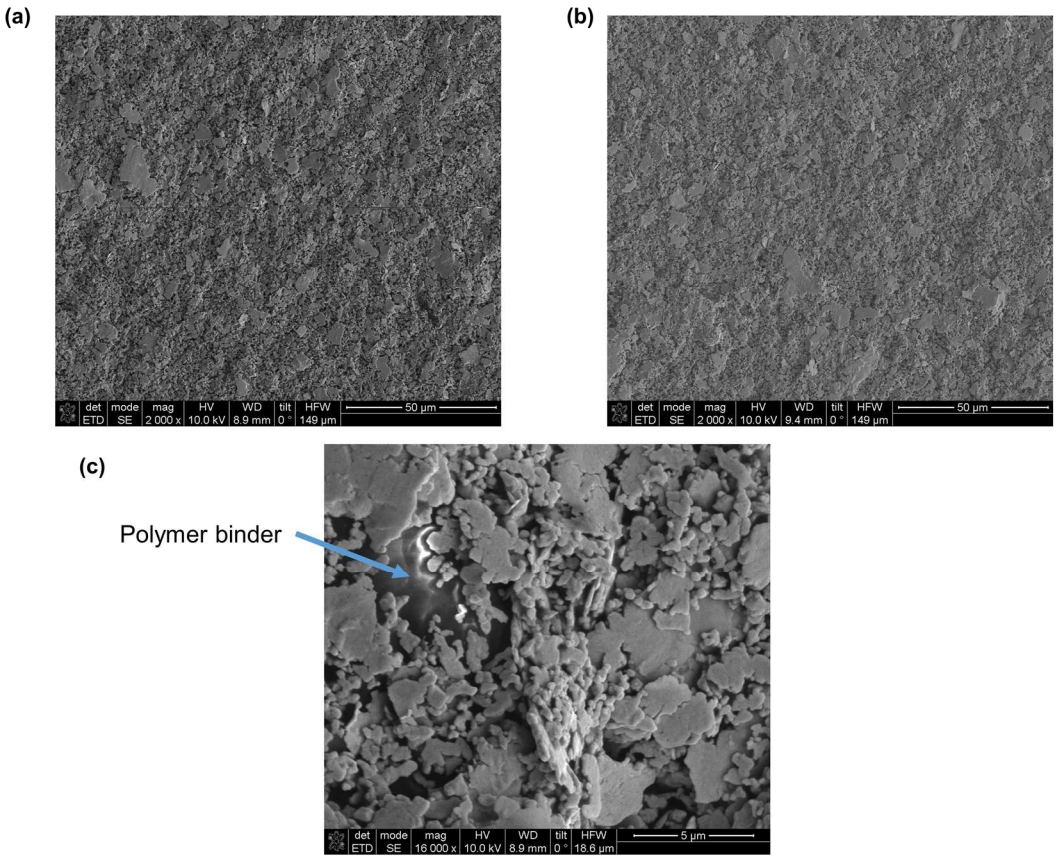


Figure 3.23: The SEM characterisations of the screen printed silver film. (a) Sample A (b) Sample B (c) The enlarged SEM image (from sample A), showing the polymer binder in the screen-printed Ag paste.

This section provides a preliminary study on the screen-printed Ag ink, including the process flow of the printing and the characterisation of the printed film using various tools, such as SEM and a profile meter. It should be noted that the work presented in this section was realised by cooperation with Miss Martina Costa Angeli, who was a visiting Ph. D. student in the BEST group. Specifically, the screen printing process and the profile meter characterisation were done by Miss Angeli and the author contributed to the SEM characterisation of all the samples. Both contributed to the electrical characterisation and data analysis.

The printing process involved a few simple steps. A mask with desired features was placed on the screen holder from the printer. The receiver substrate was loaded into the equipment and aligned with the mask. During the printing, a squeegee applied the necessary pressure to bring the mesh into contact with the substrate. Simultaneously, the paste, having previously been poured on the topside of the screen, was forced to penetrate through the openings and to be transferred on the substrate to form the desired pattern.

The as-printed sample was then subjected to a curing process in an oven. In order to obtain a preliminary understanding of the screen printing process, various samples were prepared under different conditions, and characterised as shown below.

3.3.1 The influence of the surface treatment of the receiver substrate

Silicon with a 300 nm oxide layer was used as the substrate for printing. In order to reveal the impact of the surface treatment on the printing process, the following comparative study was carried out and two substrates, named Sample A and Sample B, were prepared for screen printing. Sample A was exposed to oxygen plasma for 2 minutes with a power of 150 W; for Sample B no plasma treatment was employed. Then silver ink was printed on both surfaces using the same printing and curing conditions (160 °C for 10 minutes). The printed Ag ink was first analysed by SEM. As shown in Figure 3.23 the printed film was composed of individual flakes and particles. No obvious differences were found from the SEM images from either of the substrates. The thickness of the printed ink was then analysed by a profile meter. Both of the samples showed a thickness of ~4.5 μm, which indicates that the plasma treatment did not have an observable impact on the screen printing process. This was further confirmed by the electrical characterisation: indeed, both samples show a similar resistance ~ 3.5 Ω.

3.3.2 The influence of the curing temperature and duration

To study the influence of the curing temperature and its duration, three different curing conditions were used, which were: (i) 160 °C for 10 minutes, (ii) 60 °C for 10 minutes and (iii) 60 °C for 60 minutes, respectively. The other parameters were all kept the same in this

comparative study. All samples show similar surface morphologies and thickness, as confirmed by SEM and profile meter characterisations. However, in terms of the resistance, a major difference was observed: the resistance of the film cured at 160 °C shows a significantly lower resistance (~ 3.5 Ω) when compared to the sample cured at a lower temperature (60 °C). With respect to the curing time, little increase was observed when it was increased from 10 minutes to 60 minutes. As a result, the curing temperature dominates the resistance of the printed film, which can probably be attributed to the different level of polymer binder residue left in the printed films under various curing conditions.

3.3.3 The influence of printing cycles

Finally, the relationship between the film thickness and the number of printing cycles were studied. The Ag ink was printed on the same substrates under the same conditions, but for one, two and three cycles, respectively. After each printing, a curing process was adopted in order to stabilise the film. The thickness of the printed film was characterised by a profile meter. As can be seen from Figure 3.24, the thickness of the printed film shows a near linear dependence on the printing cycles; each one corresponds to a layer of ~4.5 µm. The width of the printed film was also monitored. As can be seen from Figure, no observable difference can be found in the three samples, showing a good ability to maintain the lateral resolution.

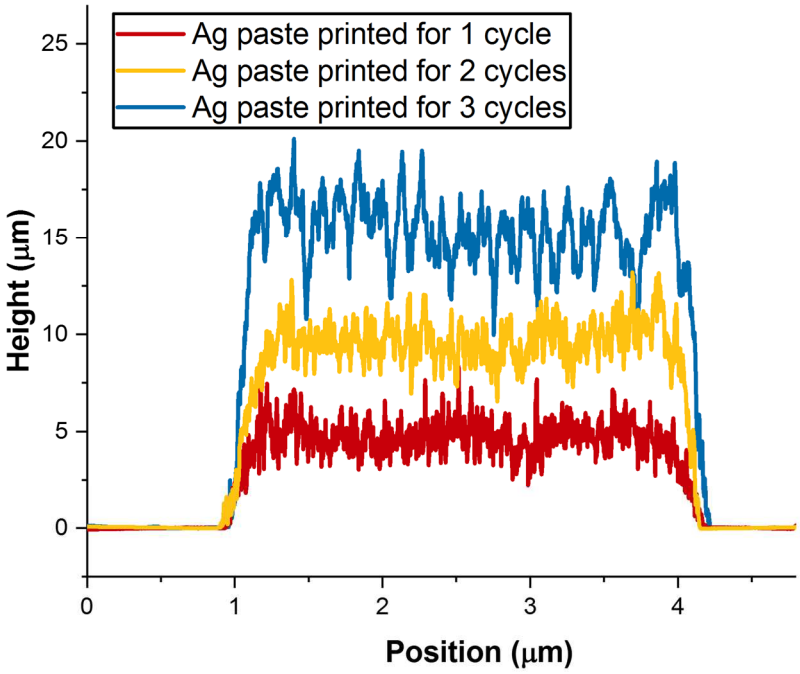


Figure 3.24: The profile of the printed ink characterised by Contact Profiler Dektak.

3.4 Summary

In summary, this chapter has outlined the printing process for quasi-1D materials, quasi-2D materials and a conductive Ag film. The as-printed materials have been characterised by various tools such as AFM, SEM and Contact Profiler (Dektak). Specifically, the printing of quasi-1D NWs on flexible and uneven substrates have been studied. And how to achieve a uniform printing of NWs on these special substrates have also been explored. The printing methods described here lay the foundation for the later studies in this thesis.

4. Chapter 4: Contact problem in printed and flexible electronics

In CMOS technology, contact realisation requires a sophisticated process involving doping and sintering at a high temperature (450 °C) [172]. Due to the thermal sensitive nature of the flexible polymeric substrates, such a strategy cannot be used in flexible electronics and instead the fabrication techniques realised under low temperatures are needed. Luckily, the contact realisation for nanomaterials may not need such a critical process. This chapter discusses the contact problem in printed and flexible electronics in the system of quasi-1D ZnO NW and quasi-2D graphene. This chapter is arranged as follows: first, two philosophically different approaches, which are contact electrodes first (bottom-contact) and nanomaterials first (top-contact), are explained and discussed (4.1). Afterwards, bottom- and top- contacted ZnO NW FET are studied and compared. The output characteristics of bottom-contacted ZnO NW FET shows a rectifying behaviour, which indicates an inefficient contact. Meanwhile, top-contacted ZnO NW FET shows a linear output characteristic, which is proof of Ohmic type contact between ZnO NW and metal electrodes. In this way, the contact strategy for ZnO NW related devices have been determined.

Then, the discussion is shifted to graphene-based devices, where the motivation for using the bottom contact strategy to realise large-area GFETs is clarified (section 4.2). The experimental process of the proposed strategy has been discussed and the device performance has been analysed; a comparison between the contact resistances with the state-of-the-art technology has been made to show the potential of the vdW contact for GFETs (section 4.3). In order to further elucidate the nature of vdW contact between graphene and Au, the Raman spectrum has been utilised, followed by a discussion of the tunnelling current of a uniformly biased graphene-Au junction. Such discussion is extended to FETs by combining with the classic resistor network model. In this way, the obtained experimental results can be qualitatively explained; and the contact strategy for graphene-based devices have been determined for all later studies in this thesis.

Finally, the big difference between the vdW contacted GFET and ZnO FET have been briefly discussed. The reason has been attributed to both the material aspect and the morphology aspect (section 4.4). It should also be noted that the majority of the results discussed in Chapters 4 and 5 have been published in some scientific journals and conference proceedings [12, 173]. Copyright permissions have been obtained from the publishers in order to include these materials in this Ph. D thesis.

4.1 The vdW contacted ZnO NW FET

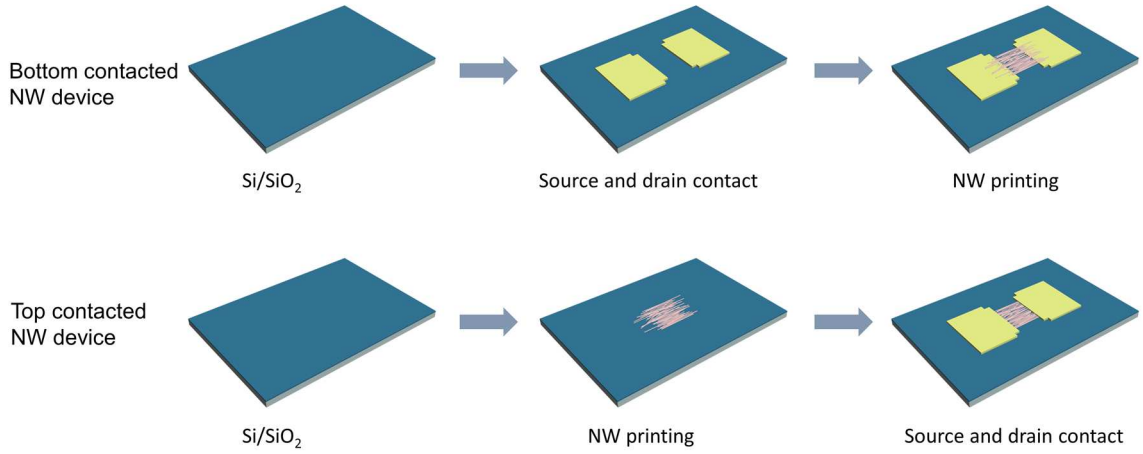


Figure 4.1: The schema showing the fabrication process flow of botton- and top-contacted ZnO NW FET.

For nanomaterial-based devices such as FETs and sensors, there are two philosophically different manners to realise the metal contact, which are metal electrodes first and nanomaterials first, respectively. The first strategy refers to a process where metal contacts have been first realised on the substrates in a desired layout. The nanomaterials, such as ZnO NWs and graphene, are then printed on top of the as-realised contacts. The benefit of such a strategy is that it minimises the micro-fabrication processes which need to be carried out on nanomaterials, thus substantially avoiding many technical problems such as material degradation and difficulty in lift-off [174, 175]. However, realised by a physical transfer process, the interaction between the transferred nanomaterials and pre-fabricated metal

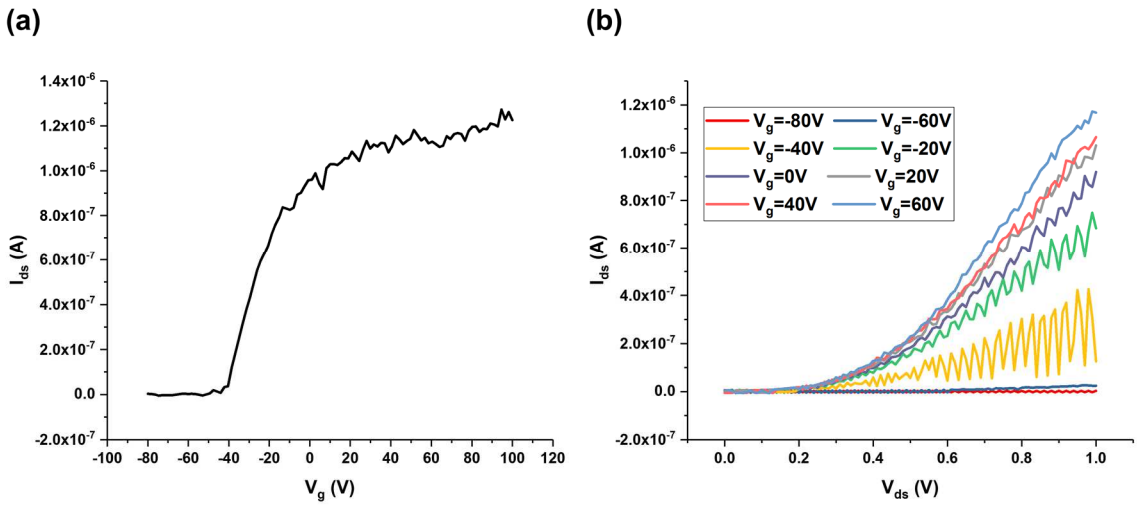


Figure 4.2: The electrical characterisations of the vdW contacted ZnO NW FET. (a) transfer curve (b) output curve.

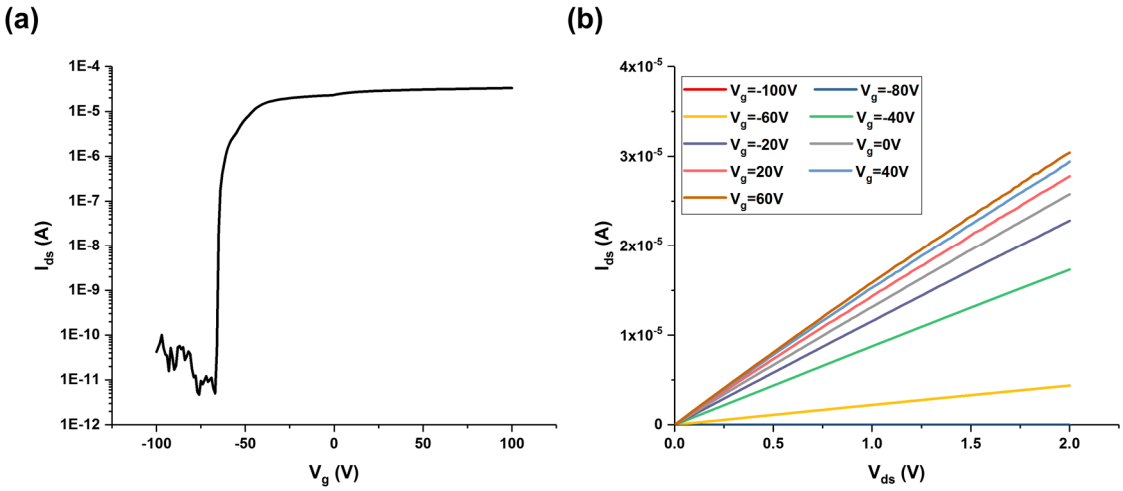


Figure 4.3: The electrical characterisations of the top-contacted ZnO NW FET. (a) transfer curve (b) output curve.

electrodes usually lies in the vdW interaction regime. How well the contacts held by the "weak" vdW force perform is a concern. In contrast, the second strategy refers to a process whereby nanomaterials have been first printed onto the substrates, followed by the standard photolithography, metallisation and lift-off process to realise the device. In this manner, the interaction between the deposited metal atoms and nanomaterials are stronger, thus the contact realised by this method is more reliable.

This section specifically discusses the bottom- and top- contacted ZnO NW FETs.

The fabrication process flow of the bottom- and top- contacted ZnO NW FET is shown in Figure 4.1. The ZnO NWs were synthesised by using the CVT method on Si substrate as reported previously [176], which serves as the donor of the NWs. Meanwhile, the receiver substrate (Si with 300 nm SiO_2 layer) patterned with the contact electrodes (Au) was realised by the same method which will be described later (Section 4.3). After that, a contact printing process has been used to transfer the ZnO NWs from the donor to the receiver substrate. The sliding direction is perpendicular to the pre-patterned contacts, which leads to a highest chance of the transferred NWs bridging across the two neighbouring electrodes. This method presents a way to realise ZnO NW based devices by direct printing. The sample was subjected to a heating process on a hotplate at 180 °C for 5 minutes before measurement. The realisation of top-contacted ZnO NW FET is similar. The ZnO NW was synthesised by the same method as has just been discussed. The receiver substrate was a Si wafer with 300 nm SiO_2 layer. After a contact printing process, the ZnO NWs were directionally transferred onto the receiver. Then the sample was subjected to a heating process on a hotplate at 180 °C for 5 minutes to increase the interaction between ZnO NWs and the underlying substrate. After heating, a UV

photolithography process was employed to define the desired pattern for source and drain, followed by metallisation by the E-beam evaporator and standard lift-off process.

The electrical characteristics of the bottom-contacted ZnO is shown in Figure 4.2. As shown in the figure, the vdW contact seems to be an inefficient contact strategy for ZnO NW based FETs, judging from the non-linear and noisy output characteristics. Actually, in our experiments, ~30 devices were tested with a ConH of 80 nm as well as a ConH of 1.8 nm. However, only several devices can be successfully operated as FETs. This is because the large contact resistance between the NW and the source and drain contact. The influence of the contact resistance is so large that no channel property can be reflected by the FET; it only shows an open-circuit behaviour. In the meantime, top-contacted ZnO NW FETs have also been fabricated and tested. The typical results of the top-contacted ZnO NW FET have been shown in Figure 4.3. The device shows an ohmic contact with linear output characteristics, which indicates that the quality of the top contact is far better than that from a vdW contacted device. As a result, it is concluded that the vdW contact is not a promising strategy for realising ZnO NWs based devices such as FETs.

4.2 Motivation for realising bottom contacted GFETs

Graphene and GFETs have attracted broad interests for various applications including sensors and RF devices since its discovery in 2004 [177-179]. One barrier towards the realisation of high-performance GFETs is the contact realisation. Although ultra-low contact resistance (< 100 Ω·μm) has been achieved by top- and edge- contact strategies (see Figure 4.4), it is mostly realised by EBL process and thus restricted to a small area; UV photoresist has been suggested to lead to a serious residue problem on the surface of graphene which hinders the realisation of good contact [174, 175]. Other methods such as ozone/ion beam treatment are also capable to realise a clean contact interface and thus low contact resistance, but they require a delicate

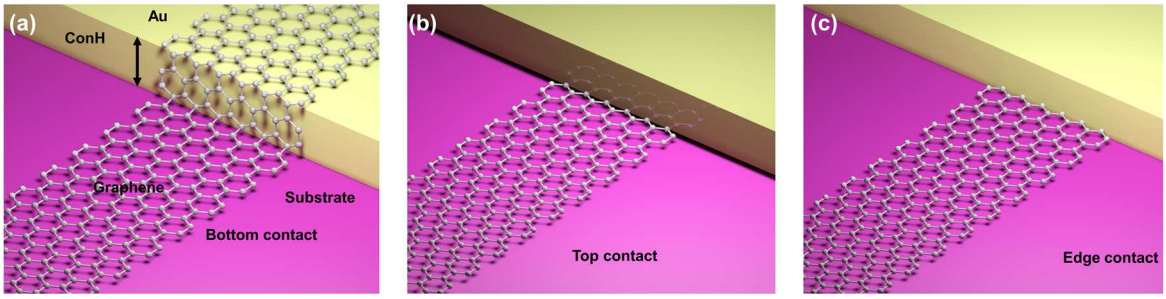


Figure 4.4: The schema showing the concept of bottom-, top- and edge- contacted GFETs. Copyright © American Chemical Society. Reprinted, with permission, from [12].

control over the process in order to maintain the quality of the graphene. And in this regard they are less promising for large-area electronics [174, 180-186].

Recently, bottom-contacted GFETs with a vdW interaction have drawn increasing research interests and have been used for various applications [15, 187-190]. In this strategy, the contact is achieved by transfer printing graphene to a pre-patterned substrate and thus circumvents cumbersome lithography process for realising contacts, which holds natural suitability for large-area electronics. Nevertheless, compared to the top- and edge- graphene-metal contact which has been studied for long time, the nature of the vdW contact has not been thoroughly elucidated. Specifically, there are three fundamental but unanswered questions associated with vdW contacted GFETs:

1) What is the influence of the geometry on the contact properties in a bottom contact device?

2) What is the range of transfer length in these devices as the contact geometry is varied?

3) What are the major differences in carrier transport mechanism between vdW and non-vdW contacted GFETs?

Without an understanding of these problems, it is rather inevitable that high contact resistance could arise in bottom-contacted GFETs as have been confirmed by several preliminary studies [187, 190].

In this regard, a systematic study has been performed on the bottom contacted GFETs, which is discussed in the later sections (section 4.3 to 4.6).

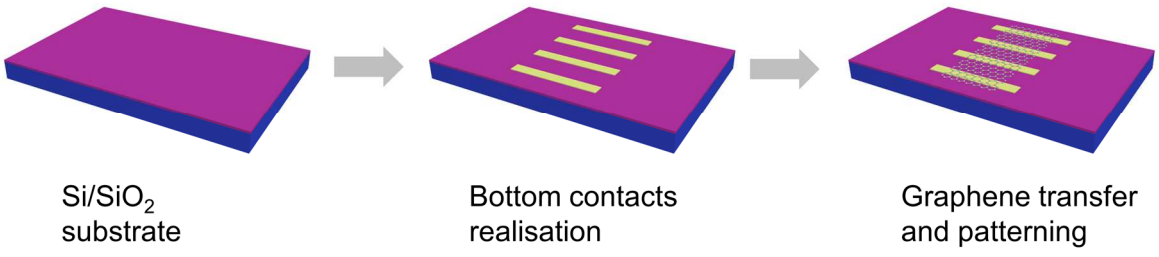


Figure 4.5: The schema showing the fabrication process flow of bottom-contacted GFET on rigid substrate.

4.3 The experimental process to realise bottom contacted GFETs

The bottom contacted GFETs were realised by transfer printing monolayer graphene onto the pre-patterned substrate with Au contacts as shown in Figure 4.5. The monolayer graphene was purchased from Graphenea. The fabrication process started with the fabrication of pre-patterned substrate on silicon wafer with 300 nm thick thermal oxide layer. UV lithography was used to define the desired patterns on top, followed by metallisation and a standard lift-off process. In order to avoid the residue problems on the developed metal contacts, the baking temperature was modified from 115 °C (as suggested by the photoresist supplier) to ~ 65 °C. Such modification is crucial for the realisation of the metal electrodes with clean surface. To illustrate the influence of this, AFM characterisations have been performed. As shown in Figure 4.6, when realised at high temperature, the surface of the metals are partially covered by photoresist residues, especially on the edge of the feature. Meanwhile, the metal pads realised under low temperature show a clean surface without photoresist contamination. Notably, this aspect is important for the realisation of the low contact resistance from bottom contact, since

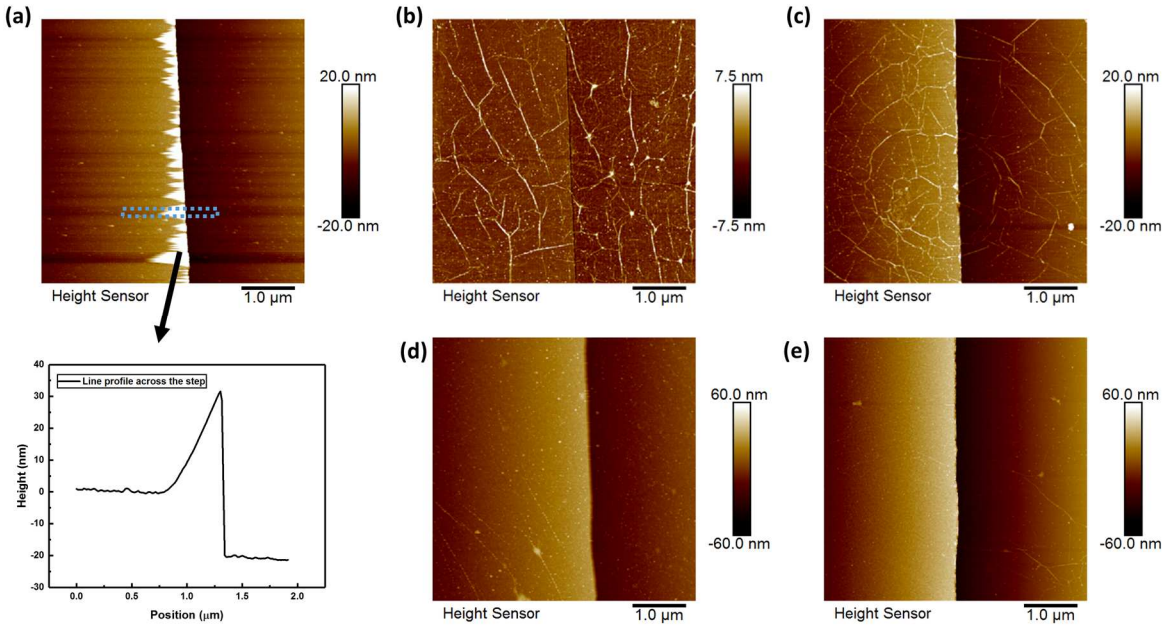


Figure 4.6: The AFM characterisations of the surface of the metal contacts. (a) The metal contacts realised at high temperature and its line profile. (b), (c), (d) and (e), metal contacts realised at low temperature with various ConH. A monolayer graphene has been transferred on top. Copyright © American Chemical Society. Reprinted, with permission, from [12].

the existence of the polymer residue would decrease the carrier injection between the two materials.

By using the modified process, metal contacts with various thickness ranging from 1.8 nm to 80 nm have been used in order to reveal its influence on the contact quality. Specifically, in

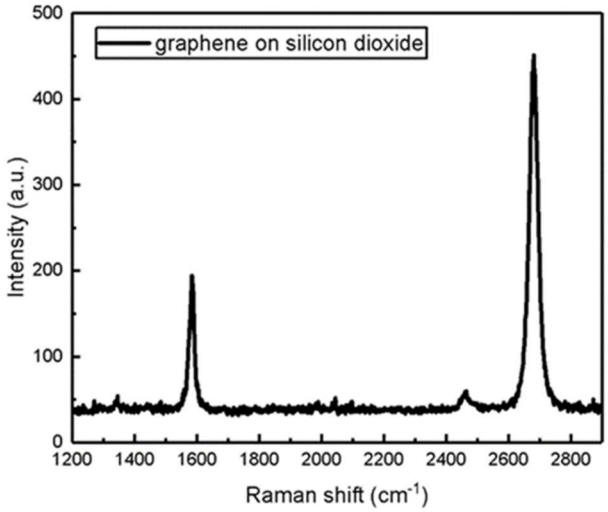


Figure 4.7: The Raman spectrum of the as-transferred graphene on Si/SiO_2 substrate. Copyright © American Chemical Society. Reprinted, with permission, from [12].

order to realise a metal contacts with an effective thickness of 1.8 nm, a trench ~20 nm was first created by RIE (reactive-ion etching) process with a mixture of CHF_3 and Ar. Afterwards, a metal film with thickness of ~21.8 nm was deposited inside the trench, leading to a net height of 1.8 nm.

Monolayer graphene was then transferred to the pre-patterned substrate with the methods described in Section 3.2. In order to electrically isolate each device on the sample, an additional etching step was required. This was achieved by spin-coating PMMA2041 as interfacial material and photoresist s1805 as a photosensitive layer to define the desired pattern. After lithography and development, the graphene and the interfacial PMMA were etched by RIE (Oxford instrument, Plasmalab 80 plus) with the oxygen plasma. Finally, the PMMA and photoresist was removed by acetone and rinsed by IPA to leave the patterned graphene at the surface. In order to determine the quality of the transferred graphene film, Raman spectrum was employed. As can be seen from Figure 4.7, the intensity ratio of the 2D: G bands I_{2D}/I_G is larger than 2.75, which indicates the single layer nature. No significant D band has been observed, which implies a high-quality transfer. The as-fabricated devices were then subjected to the electrical measurement without any post annealing process.

4.4 The measurement of vdW contacted GFETs on rigid substrate

The device was measured by semiconductor parameter analyser Keysight B1500A. A gated four terminal measurement method is used to extract the value of the contact resistance with the equation [181]:

$$R_C = \frac{1}{2} \times (R_{2T} - R_{4T}) \quad (1)$$

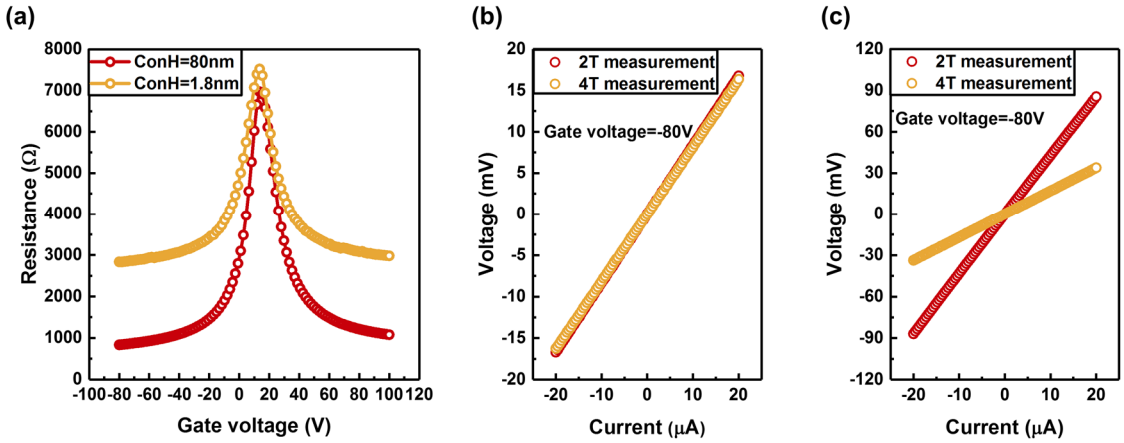


Figure 4.8: The Electrical characterisation of the bottom contacted GFETs. (a) The transfer curves obtained at ConH of 1.8 and 80 nm, respectively. (b) and (c) The output curves obtained at ConH of 80 and 1.8 nm, respectively. The ConL is 30 μm for the data shown in this figure. Copyright © American Chemical Society. Reprinted, with permission, from [12].

Typical transfer and output characteristics have been shown in Figure 4.8. From the figure, one can see that the on/off ratio of the device is larger under higher contact height (ConH). This is attributed to the change of contact quality—the on state current of devices with lower ConH deteriorate significantly thus leads to a lower on/off ratio [191-193]. Such difference is also observable from the output characteristics: the two terminal and four terminal output curve (at gate voltage of -80 V) shows an insignificant (significant) change under high (low) ConH, which indicates a big difference in the contact resistance from the two type of devices.

One fact should be highlighted is that the output curve was obtained at V_g of -80 V, corresponding to a gate induced carrier density ~1.75×10^{12} cm^{-2}. For both a transfer line method (TLM) and a 4T measurement method, the reliability of the R_C extraction depends on the homogeneity of the doping of the channel [183, 194, 195]. Under high gate bias voltage (Vg=-80 V in this case), the gate-induced carrier density is far larger than the fluctuation of the residual carrier density in the channel, which guarantees a reliable estimate of the contact

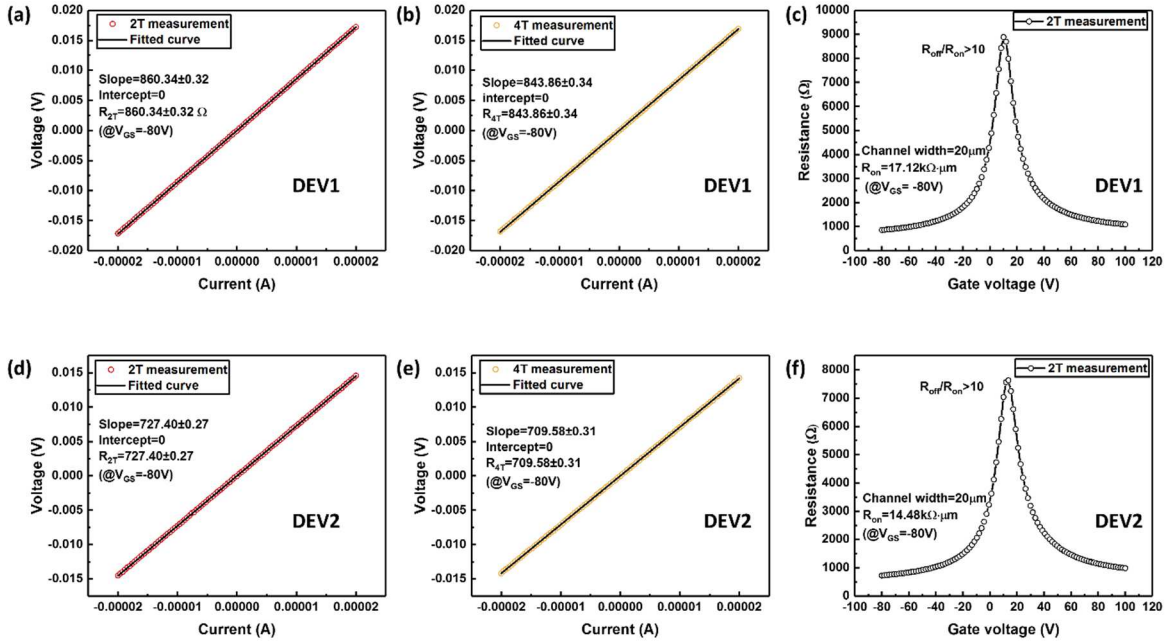


Figure 4.9: Bottom-contact GFETs with contact resistance lower than 100Ω·μm. (a), (d) are the output curves from 2T measurements @VGS=-80V; (b), (e) are the output curves from 4T measurements @V_{GS}=-80V; (c), (f) are the transfer curves from 2T measurements. Copyright © American Chemical Society. Reprinted, with permission, from [12].

resistance. Another fact which should be noted is that the calculated contact resistance includes the contribution both from the lead resistance (resistance of metal) and the graphene-metal contact resistance. While this is almost negligible if the real R_C is far larger than the resistance of metal leads (under low ConH), it plays a nonnegligible role for those devices with a small R_C [183]. In this regard, the estimation of R_C should therefore take the lead resistance into account.

Here, the bottom-contacted GFETs with a ConH of 80 nm and ConL of 30 μm has been used as an example to illustrate the extraction of the contact resistance. 10% of these devices exhibits a contact resistance lower than 100 Ω·μm and more than half shows a contact resistance less than 200 Ω·μm (at the gate voltage of -80 V). Typical output curve for 2T and 4T measurements are plotted in Figure 4.9. As has been discussed, the measured resistance not only includes the junction resistance between graphene and Au, which is twice the real contact resistance, but also includes the lead resistance, which is comprised of the resistance of the metal lead and the resistance of the probe tip-metal electrode contact resistance. The estimation of the graphene-metal contact resistance should exclude the contribution from the lead resistance when the

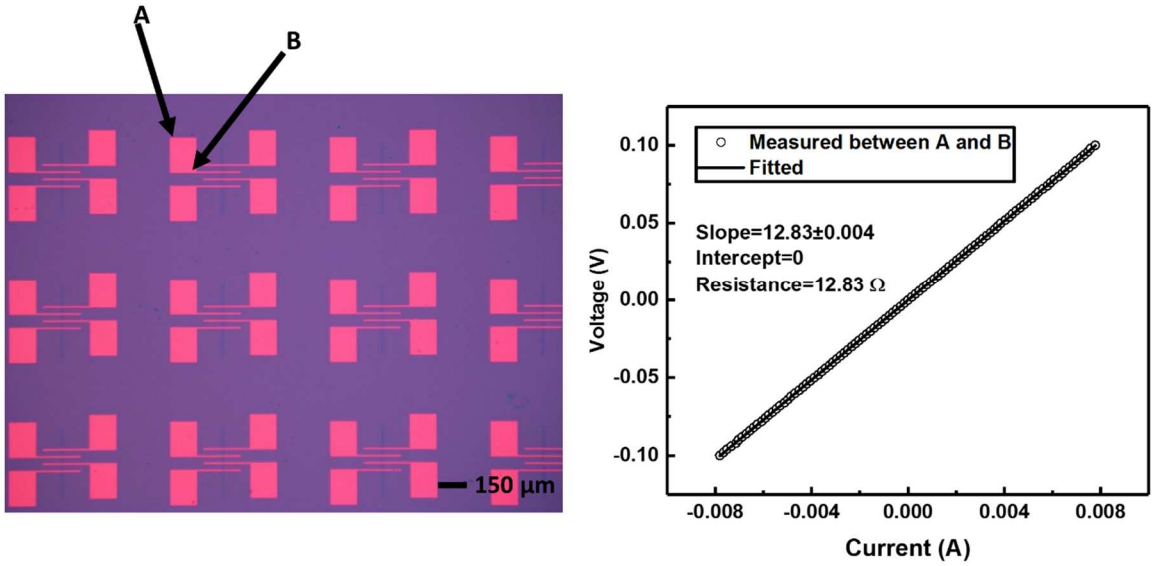


Figure 4.10: (Left) A schematic of how the lead resistance was estimated by probing point A and point B in the same electrode. (Right) A plot of a voltage-current sweep showing the value of the lead resistance. Copyright © American Chemical Society. Reprinted, with permission, from [12].

value of the two is comparable [183]. In our work, the lead resistance R_{Lead} is estimated by probing two points, A and B, on the same electrodes, as shown in Figure 4.10 (left). The tested result is plotted in Figure 4.10 (right), indicating a resistance of ~12 Ω (the lowest value we could obtain). We thus estimate the lead resistance in our system is ~10 Ω, which is an underestimation of the lead resistance. Correspondingly, since the real contact resistance R_C is equal to $\frac{R_{2T}-R_{4T}-R_{Lead}}{2}$, the result of the contact resistance is overestimated. The subtraction of the lead resistance was employed to calculate the contact resistance of all the devices.

Thus, the normalised contact resistance extracted from DEV1 (device 1) and DEV2 (device 2) shown in Figure 4.7 are 64.8 ± 6.6 Ω·µm and 78.2 ±5.8 Ω·µm, respectively. Although the devices are based on wet-transferred CVD graphene and measured under ambient atmosphere at room temperature, they still show a high-performance. For both devices, their on/off ratio are both higher than 10 (Figure 4.7 c and f), with the on-state resistance ~15 kΩ·µm. Comparatively, current state-of-the-art bottom-contacted GFETs show a contact resistance of 910 ± 340 Ω·µm, with an on/off ratio of ~3 and an on-state resistance~125 kΩ·µm [187]. By

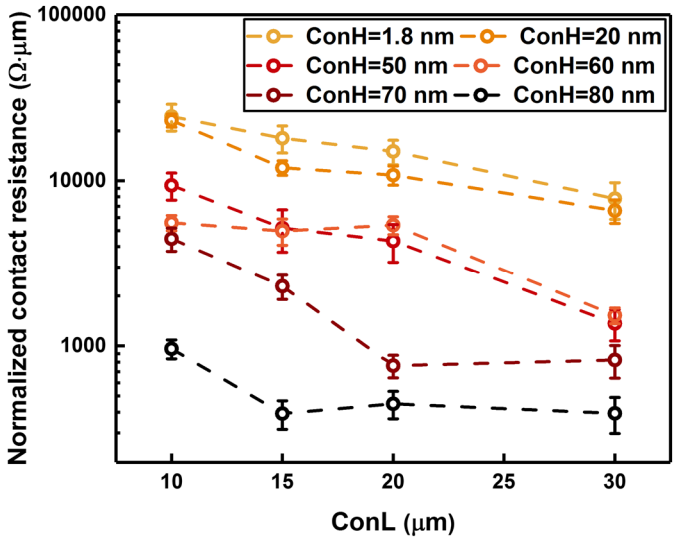


Figure 4.11: The dependence of the contact resistance on various ConL and ConH. Copyright © American Chemical Society. Reprinted, with permission, from [12].

comparison, for top-contacted GFETs based on wet-transferred CVD graphene (requiring EBL and thermal annealing), the state-of-the-art contact resistance is ~124.6 Ω·μm [183], still higher than the value obtained in this work. A detailed comparison is presented in Table 4.1.

Table 4.1: Comparison of device performance with the state of art CVD graphene FET. Copyright © American Chemical Society. Reprinted, with permission, from [12].

Contact Architec-ture	Fabrication techniques/ Cost	Channel width/length (μm/μm)	Measurement environment	R_C (Ω·μm)	On/Off ratio	On-state resistance (kΩ·μm)	Mobility (cm^2/V·s)	Ref #
Top-contact (Pd/Au)	EBL/High	2/5	Vacuum &room temperature	124.6	NA	NA	>3000	[183]
Bottom-contact (Au)	UV lithography/ Low	50/30	Ambient condition &room temperature	910±340	~3	125	1240	[187]
Bottom-contact (Au)	UV lithography/ Low	20/30	Ambient condition &room temperature	64.8±6.6	>10	15	2271	This work

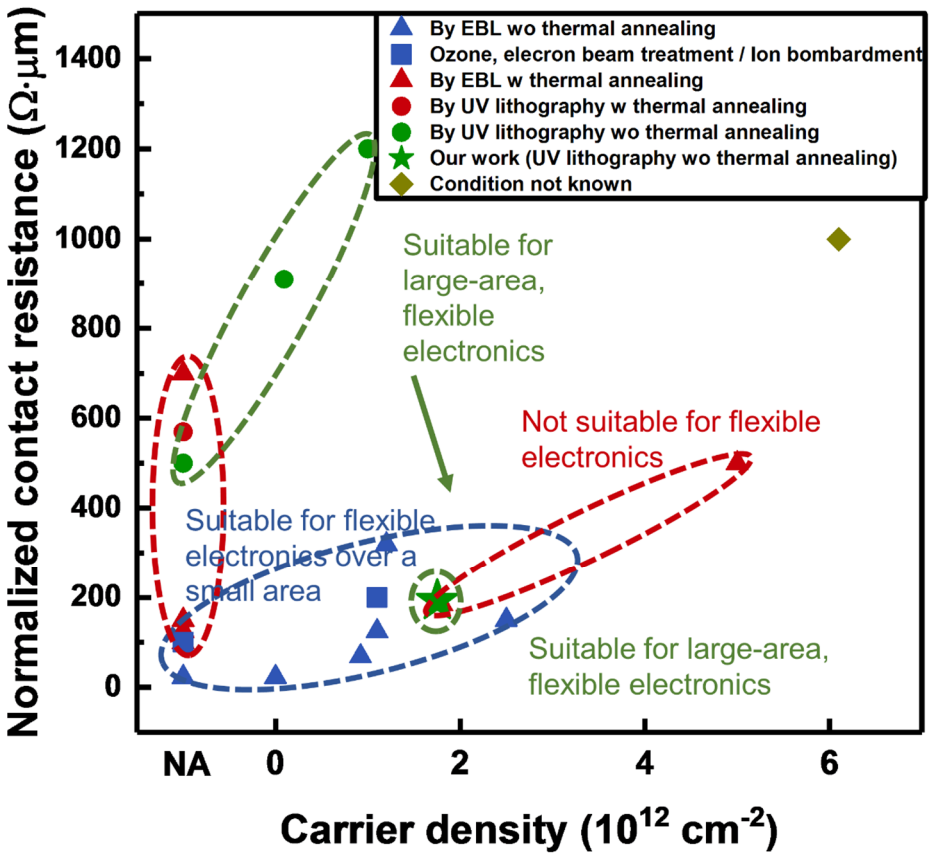


Figure 4.12: The comparison between the contact resistance versus carrier density from various work. Copyright © American Chemical Society. Reprinted, with permission, from [12].

Further, by using the methods described above, the contact resistance has been extracted for the devices with various ConH and ConL, and plotted in Figure 4.11. Interestingly, for the bottom-contacted devices used in the study, a large dependence between ConL and the normalised R_C has been observed, which contradicts the result from top-contacted GFETs from previous studies. In conventional top-contacted GFETs, normally no significant dependence between the normalised R_C and the ConL should be observed under a contact length (ConL) in the range of several micrometres or longer, which is attributed to the so called "current crowding effect" [196, 197]. Such dependence only becomes significant under nanoscale contact, where ConL is much smaller than the transfer length L_T [198]; the L_T ranges from approximately 100 nm to 1.7 µm for top-contacted GFETs [194, 198, 199]. This result indicates that for bottom-contact GFETs, especially for those devices with low ConH, the current does not crowd at the edges. According to the Figure 4.11, the L_T is expected to be larger than 30 µm for a ConH of 1.8 nm. With the increase of the ConH, the L_T decreases. With a ConH of 80 nm, no significant dependence between ConL and normalised R_C has been observed, which may indicates a fact that the L_T is lower than 10 µm. Overall, the bottom contacted GFETs with

a weak vdW interaction shows a much larger L_T compared to the conventional top contacted GFETs realised by deposition. And the impact of this unique fact depends on the targeted applications. For example, there will be a serious problem in device miniaturisation for the FETs with large L_T, thus such FETs are not favoured for those devices which requires high density. However, with large L_T, the local heat at contact can be significantly reduced along with a decrease in the *1/f* noise [200]. Considering the fact that this Ph.D. study focuses on large-area electronics with high performance, the ability to achieve low contact resistance is more important than the density/dimensions of devices. As a result, a FET with longer transfer length is not regarded as a disadvantage. And therefore, in this section it is focused on the width-normalised ($\Omega \cdot \mu m$) rather than the area-normalised ($\Omega \cdot \mu m^2$) contact resistance. Another interesting phenomenon in Figure 4.11 is that the normalised R_C decreases with the increase of ConH as has been previously discussed in Figure 4.6. With a ConH of 80 nm, 60% of devices show a contact resistance under 200 $\Omega \cdot \mu m$ (ConL of 30 µm). The lowest value obtained from our devices is ~65 $\Omega \cdot \mu m$ (see Figure 4.9 and 4.10), which is the best reported value to date among both bottom- and top- contacted GFETs and is comparable to state-of-the-art edge-contacted GFETs produced via expensive EBL process techniques [172, 186], delicate thermal annealing processes [201, 202] and complex contact optimisation (see Table 4.2 at the end of this section) [181, 203]. While many contact strategies with top- and edge- contact are less promising for large-area electronics due to the reasons mentioned in section 4.1, the method described here is well-suited to this application (see Figure 4.12). The only critical step in this method is the realisation of clean metal electrodes without photoresist contaminations, which have been previously described in Section 4.3. Given the recently developed large-area, high quality and low-cost graphene synthesis and transfer technique [204, 205], potentially this method can be used for large-area, cost-effective GFETs fabrication. Attempt has also been made to increase the ConH of the devices to 100 nm. However, in this scenario, breakage of the graphene film along the contact edge was observed, leading to a decreased successful rate [87]. In addition, those working devices show no significant additional decrease in contact resistance. It is therefore concluded that the 80 nm is an optimised value of ConH for large-area electronics.

Finally, the device mobility has been extracted based on the 2T and 4T measurements, with the equation $\frac{dI_{ds}}{dV_{ds}} = \frac{\mu WCV_g}{L}$. Generally, the device mobility extracted by 2T measurement should be less than that extracted from 4T measurement, due to the contribution from the contact resistance. This is also reflected in the results shown in Figure 4.13 for all the ConH (ConL of

30 µm). Further, as can be seen from the figure, the ratio of the $\frac{\mu_{2T}}{\mu_{4T}}$ increases while the ConH of the devices increases, which further confirms the dependence between the contact resistance and the ConH.

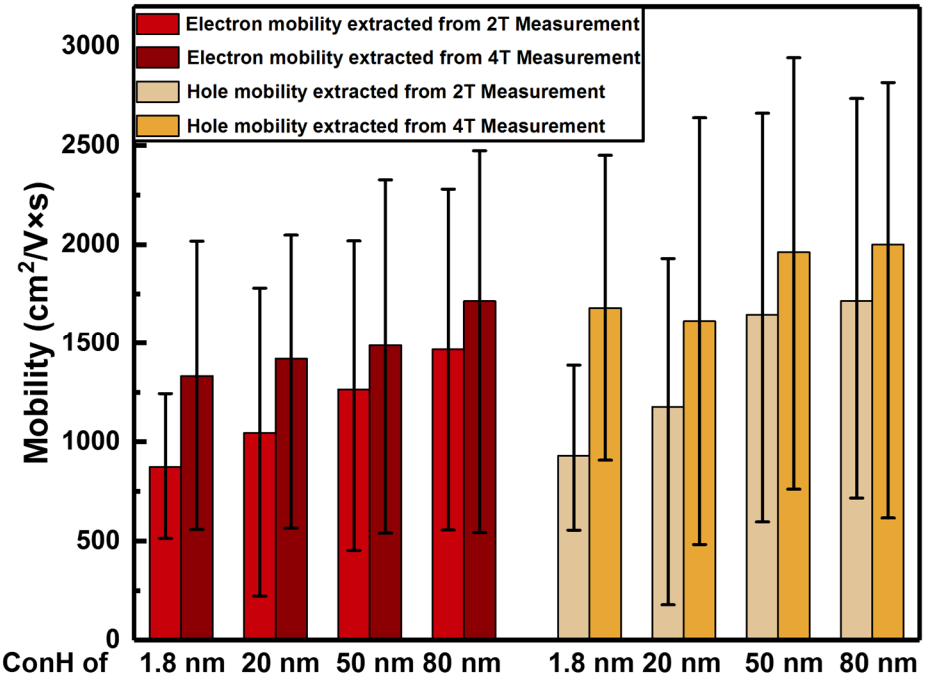


Figure 4.13: The comparison between the field-effect mobility extracted by 2T and 4T measurement under different ConH.

Table 4.2: Comparison of monolayer graphene-metal contact properties at room temperature. Copyright © American Chemical Society. Reprinted, with permission, from [12].

Electrode	Contact Architecture	Graphene Type	Normalised Contact Resistance (Ω·µm)	Contact Resistivity (Ω·µm²)	Compatibility with large-area, flexible electronics	Carrier density (cm^{-2})	Ref #
Ni/Au	Top-contact	Mechanical exfoliated	500	~500	No (Annealed at 300°C/EBL)	5×10^{12}	[196]
Ti/Au or Cr/Au	Top-contact	Mechanical exfoliated	10^3 to 10^6	NA	No (Annealed at 300°C/EBL)	5×10^{12}	[196]
Ni or Au	Top-contact	CVD grown	~7000	NA	NA	$1.9\sim2.5\times10^{12}$	[192]
Pd	Top-contact	CVD grown	~1000	NA	NA	6.1×10^{12}	[192]

Ti	Top-contact	Mechanical exfoliated	700±500	NA	No (Annealed at 300°C/EBL)	NA	[206]
Pd/Au	Top-contact	Mechanical exfoliated	185±20	NA	NA	1.8×10^{12}	[194]
Ti/Au	Top-contact	CVD grown	<200	NA	No (Delicate ozone treatment)	1.1×10^{12}	[174]
Ni	Top-contact	Mechanical exfoliated	NA	~1000	No (EBL)	0.9×10^{12}	[207]
Pd/Au	Top-contact	Mechanical exfoliated	69	NA	No (EBL)	0.9×10^{12}	[183]
Pd/Au	Top-contact	CVD grown	124.6±37.9	NA	No (EBL)	1.1×10^{12}	[183]
Pd	Top-contact	CVD grown	570	NA	No (RTA)	5.2×10^{12}	[193]
Ti/Au	A mix of top and edge-contact	CVD grown	23	NA	No (EBL)	NA	[182]
Au	A mix of top and edge-contact	CVD grown	23	NA	No (EBL)	0×10^{12}	[185]
Ni/Al	A mix of top and edge-contact	CVD grown	Most of under 500 with lowest value~130	NA	Yes	2.9×10^{12}	[208]
Pd	A mix of top and edge-contact	CVD grown	100	NA	No (Ion-bombardment)	NA	[186]
Cu	A mix of top and edge-contact	Epitaxial growth on SiC	125	NA	No (Annealed at 350°C/EBL)	NA	[203]
Ni	A mix of top and edge-contact	Mechanical exfoliation	100	NA	No (Anneal at 580°C/EBL)	NA	[181]

Pd/Au	A mix of top and edge-contact	CVD grown	~150	0.22	No (Annealed at 300°C/EBL)	NA	[200]
Cr/Pd/Au	Edge-contact	Mechanical exfoliation	150	NA	No (EBL)	2.5×10^{12}	[180]
Ti/Pd/Au	Top and bottom contact	CVD grown	320, with lowest value ~260	NA	No (EBL)	1.2×10^{12}	[191]
Au	Bottom-contact	CVD grown	910±340	NA	Yes	$<9.2\times10^{10}$	[187]
Au	Bottom-contact	CVD grown	1200±250	NA	Yes	1×10^{12}	[190]
Au	Bottom-contact	CVD grown	Most of under 200 with lowest value~65	~1000	Yes	1.8×10^{12}	This work

4.5 Analysis of graphene-Au separation in vdW and non-vdW contacted devices

To clarify the large difference in R_C at ConH of different values (Figure 4.11), the transfer process used for realising the contacts was investigated. As have been discussed in chapter 3, the transfer process started with poly (methyl methacrylate) (PMMA) spin-coating on Cu foil, which serves as a mechanical support. After etching and cleaning procedures, the PMMA/graphene film was transferred to a substrate pre-patterned with metal electrodes. In order to realise an intimate contact between graphene and the underlying substrate, slowly the sample was heated to 150°C on a hotplate [120]. This leaded to the evaporation of the transfer medium (isopropanol) and the generation of a capillary force on the film towards the substrate. Meanwhile, increasing the temperature above the glass transition temperature of PMMA (~115°C) causes the film to change from a hard, glassy state to a rubbery state, guaranteeing a uniform, close contact between graphene and the underlying substrate with a strong, reliable vdW interaction. It is rational to speculate that the close contact within the vdW interaction regime was not attained all together for the whole PMMA/graphene film, but rather certain isolated areas of the film attach to the substrate in the first instance. These areas are referred as

"anchor points" and the total length between two anchor points across the metal-dielectric interface (see Figure 4.14 a). In this scenario, the length of the film should follow the equation:

$$L_{total} = L_{top} + \sqrt{L_{bottom}^2 + h^2} \quad (2)$$

After the transfer printing of graphene, the film forms a stable vdW interaction with the substrate separated by a vdW gap. The film was locally strained, and, length of the film should be given by:

$$L_{total}^{'} \approx L_{top} + h + L_{bottom} \quad (3)$$

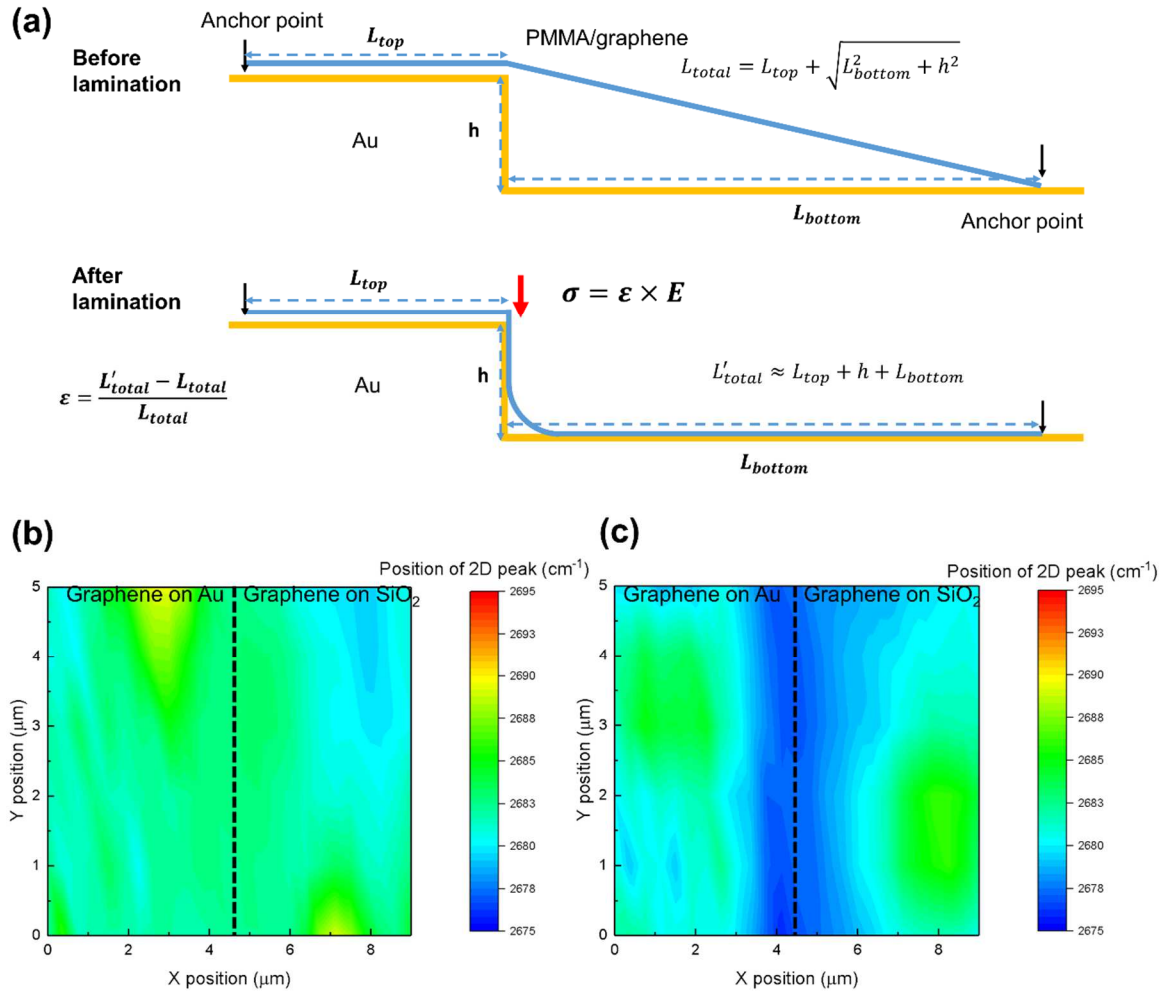


Figure 4.14: (a) The schema showing the transfer process of graphene/PMMA bilayer onto substrates patterned with metal contacts. (b) and (c) The Raman mapping of 2D peak of graphene transferred onto metal/dielectric interface, with ConH of 1.8 nm and 80 nm, respectively. Copyright © American Chemical Society. Reprinted, with permission, from [12].

Such localised strain in graphene has been further confirmed by Raman spectroscopy. The results of the two-dimensional mapping of the graphene 2D band across the metal-dielectric interface were respectively illustrated in Figure 4.14 b and Figure 4.14 c, corresponding to a

ConH of 1.8 nm and 80 nm, respectively. While almost no shift of the 2D band has been observed in Figure 4.14b, there is a drastic shift of the band in Figure 4.14 c. According to previous study, such band shift would correspond to a tensile strain of ~ 0.6% [209]. Meanwhile the strain of the film ε can be calculated by:

$$\varepsilon = \frac{L_{total}^{'} - L_{total}}{L_{total}} \qquad (4)$$

By assuming L_{top} is equal to L_{bottom}, we can roughly estimate the L_{top} and L_{bottom} to be ~ 15 μm ($h = 80\ nm$). Regarding the applied stress σ, it is proportional to the strain under elastic deformation:

$$\sigma = E \times \varepsilon \qquad (5)$$

where E stands for the Young's modulus of the PMMA film (~1×10^9 Pa) [87]. As a result of that, the PMMA/graphene bilayer is anticipated to receive an applied stress of ~6×10^6 Pa (illustrated by the red arrow in Figure 4.14 a). Such a big pressure applied to the film is expected to reduce the vdW gap between the electrode and graphene film. The real scenario may be more complex since it may involve a redistribution of the strain along the film; the above analysis only provides an approximate, semi-quantitative explanation. However, it is enough to conclude that the graphene-Au vdW contact can be engineered by transferring graphene film to metal contact with different ConH. In the meanwhile, we checked the intensity of the D peak by Raman spectroscopy for the graphene transferring across the metal-dielectric interface. The typical result of the measurement has been shown in Figure 4.15: no significant D peak has been detected, which indicates that the defects are insignificant in the strained graphene film.

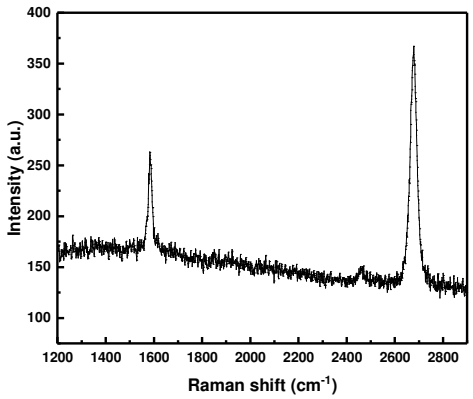


Figure 4.15: The typical Raman spectrum obtained from the graphene at the edge of the metal contact. Copyright © American Chemical Society. Reprinted, with permission, from [12].

It is thus believed that the carrier injection from defects (edge contact) is not dominating in this scenario.

For comparison, the graphene-Au separation for the case of a top-contact GFET, which has been previously studied at the level of density functional theory [11], is discussed below. When the species of wetting metal (Co, Ni, Pd, etc.) evaporated on a graphene surface, the metal atoms are more aggressive and chemisorbed on the surface. In this scenario, the equilibrium separation between the metal atoms and the graphene is considered to be smaller than 2.3 Å [11, 191, 210]. By comparison, in the scenario of a non-wetting metal (Au, Pt, Al, Cu, Ag, etc.) deposited onto graphene, the metal atoms are less aggressive; graphene only interacts weakly with these metal atoms, which leads to mainly physisorption (vdW interaction) at the surface. The equilibrium separation between metal atoms and graphene is thus larger (*ca*. 3.2~3.3 Å) [11, 198]. In previous studies, one major approach to decrease the graphene-metal contact resistance is to minimise the equilibrium separation. This can be achieved by means such as using Pd to form a layer of palladium-carbide at the contact interface [194, 210] and exploiting the edge-contact strategy resulting from a shorter bonding distance (~1.42 Å) and a larger orbital overlap [180]. However, for the case of vdW contacted GFET, the effective gap between the two is much larger (>3.3 Å, normally ~1 nm as suggested in Ref. [211]), which would superficially appear to lead to worse contact.

4.6 Carrier transport mechanism in graphene-Au vdW and non-vdW contact

Considering the above discussion, the carrier transport mechanism is first studied in a vertical graphene-Au junction. Various transport regimes exist, including thermionic emission, Fowler–Nordheim tunnelling and direct tunnelling. The output characteristic is linear without any rectifying behaviour. Therefore, the thermionic emission is not deemed as a dominanting mechanism in graphene-metal contact [172]. Fowler–Nordheim tunnelling usually takes place at high electric field (> 10^9 V/m) [212, 213]. In these devices, the voltage difference between source and drain is smaller than 300 mV (lower than 100 mV in a high gate bias of -80 V). By assuming the voltage drop on the channel equals the voltage drop on the contact, the voltage dropped on the graphene-Au junction should be lower than 25 mV under a high gate voltage bias, which corresponds to an electric field of 2.5×10^7 V/m (assuming a vdW gap of 1 nm). This is almost two orders of magnitudes lower than the required electric field for Fowler–Nordheim tunnelling, which suggests that Fowler–Nordheim tunnelling is not likely occurring in these devices. Therefore, the vertical carrier transport in the graphene-Au vdW junction is

attributed to a direct tunnelling process [206], which has already been extensively used to describe the vertical current for graphene based vdW heterostructures [215-217]. The vertical current $I_{vertical}$ and the contact resistivity ρ_C ($\Omega \cdot \mu m^2$) of the graphene-metal junction follows the equations:

$$I_{vertical} \propto \int DOS_B(E) \times DOS_T(E - e \times V) \times [f(E - e \times V) - f(E)] \times T(E) dE \qquad (6)$$

$$\rho_C = \frac{k \times V}{I_{vertical}} \qquad (7)$$

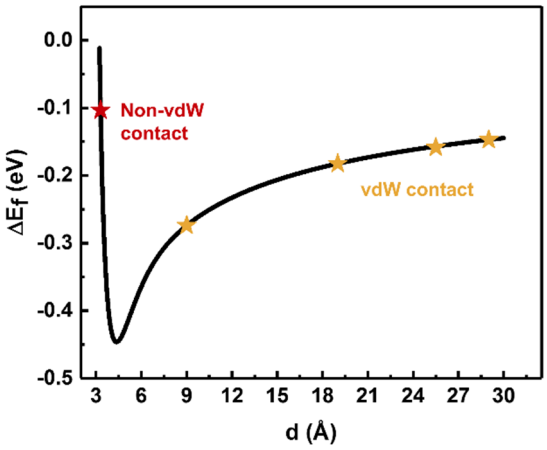


Figure 4.16: The relationship between the fermi level shift of graphene and the graphene-metal separation *d*. Copyright © American Chemical Society. Reprinted, with permission, from [12].

Here, *E* denotes the energy; *V* denotes the bias between graphene and Au; *k* is the normalisation constant (in the unit of μm^2); $DOS_T(E)$ and $DOS_B(E)$ respectively represent the density of states for graphene and Au; *f(E)* is the Fermi-Dirac distribution; *m** is the effective mass of the tunnelling process; $\hbar$ is the reduced Planck constant; ρ_C denotes the contact resistivity, and *d* and *U* are the barrier width and barrier height respectively. *T(E)* is the is the tunnel probability and follows the equation [215]:

$$T(E) \approx e^{\frac{-2d\sqrt{m^*(U-E)}}{\hbar}} \qquad (8)$$

In principle, the density of states of graphene would be zero at the Dirac point, which would result in an ultra-large contact resistivity. However, when the graphene film is contacted with Au, there would be charge transfer between the two materials which leads to the doping of the graphene [11, 218]. Under thermal equilibrium, the relationship between the Fermi level shift ΔE_f in graphene and the graphene-metal separation *d* can be modelled by approach proposed in Ref. [11]. Thus, the Fermi level shift under different contact scenarios can be modelled. The

relationship between the fermi level change of graphene and the change of separation *d* has been plotted in Figure 4.16.

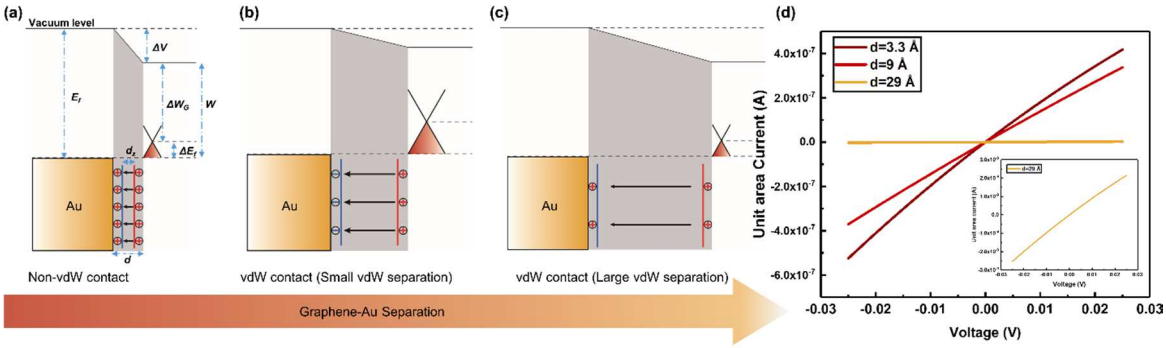


Figure 4.17: The fermi level of graphene under various graphene-Au separation and its influence on the current density. (a), (b) and (c) The schema showing the influence of graphene-metal separation d to the change of the fermi level of graphene. (d) The calculated unit area current under various graphene-Au separations. Copyright © American Chemical Society. Reprinted, with permission, from [12].

In a top-contacted FET, Au is deposited on the surface of graphene, the separation between the two is suggested to be ~ 3.3 Å (as previously discussed). In this scenario, the Fermi level of graphene is strongly affected by the formation of interfacial dipoles, which leads to a ΔE_f with a value of ~-0.103 eV (see Figure 4.16 and Figure 4.17a). In the meanwhile, for the bottom-contacted FET, there is only a weak vdW interaction between graphene and Au; the separation between the two is much larger (normally >1 nm) [211]. Under this condition, the effects from the interfacial dipole is suggested to be significantly reduced, the Au work function is determined only by the charge transfer between graphene and Au (Figure 4.17b). Hence, the doping of the graphene film (ΔE_f) under certain graphene-Au separation (Figure 4.16) can be significantly larger than that seen in the top-contact case. However, the further increase in the vdW gap between graphene and Au decreases the doping of the graphene film significantly, which signifies, graphene is not influenced by the existence of Au (Figure 4.17c). The two can be regarded as not in contact.

With these understandings, the contact resistivity in a simple graphene-Au junction (graphene is uniformly biased) can be clarified: the contact resistivity is determined by the density of states of graphene as well as the tunnelling probability through the tunnelling barrier. Although the equilibrium separation between Au and graphene is believed to be much larger in a vdW contact than that in a top-contact, the difference in the density of states (or ΔE_f) can compensate for the negative influence from the decrease of the tunnelling probability. This implies that in the case of a vdW contact with certain equilibrium separation, the contact resistivity can be similarly low to that in a top-contact, even though the latter has a much smaller graphene-Au

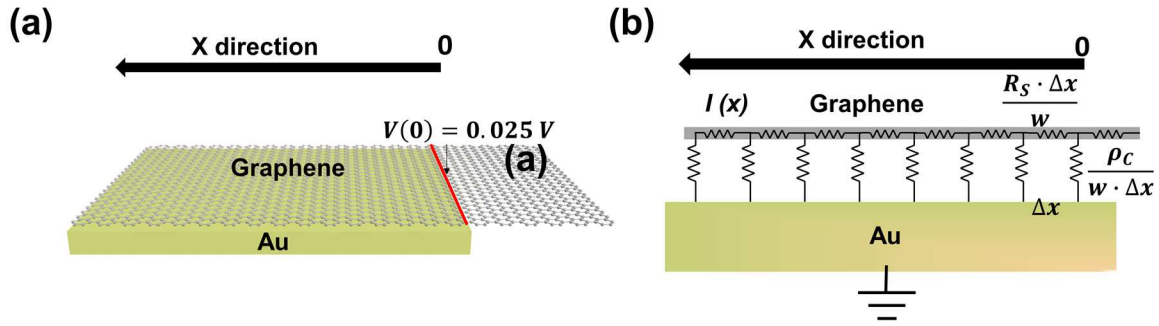


Figure 4.18: The illustration of the resistor network model. (a) The schema showing the graphene-metal bottom contact. (b) The schema showing the resistor network model for the graphene-metal bottom contact. Copyright © American Chemical Society. Reprinted, with permission, from [12].

separation (d and hence z_d). This statement can be quantitatively illustrated by fitting ΔE_f into equation (6) with different values of d. As shown in Figure 5.4d, the unit area current is almost the same under d = 3.3 Å and d = 9 Å. In the meantime, further increasing d to 29 Å can result in a reduction in both the doping level (Figure 4.16) and the tunnel probability, which leads to a decrease in the tunnelling current by two orders of magnitude.

4.7 Carrier transport mechanism in vdW contacted GFET

In this section, the carrier transport mechanism in a FET is discussed. Here, presumptions are made that the carrier transported in the graphene lattice can either: (a) horizontally propagate within the graphene plane or (b) irreversibly inject into the Au pad [194]. With these two presumptions, a modified resistor network model is employed to clarify the problem. The schematic of the resistor network model is illustrated in Figure 4.18. Since the polycrystalline CVD graphene has been used in this study, it is reasonable to assume a total diffusive transport within the CVD graphene plane at room temperature. $V(x)$ and $I(x)$ refer to the voltage and current along the graphene plane and are given by:

$$\frac{dI(x)}{dx} = -\frac{V(x)}{\left(\frac{\rho_C}{w}\right)} \qquad (9)$$

$$\frac{dV(x)}{dx} = -I(x)\frac{R_S}{w} \qquad (10)$$

where w is the contact width, R_S is the sheet resistance of a CVD graphene film in contact with Au and ρ_C is the contact resistivity. Combining the equations (6), (7), (8), (9), (10) with the boundary conditions, i.e. $V(0)$=0.025 V (start of the contact), $I(L)$=0 (end of the contact), the voltage drop on the contact, contact resistivity and normalised contact resistance with respect

to ConL can thus be calculated (Figure 4.19). As has been previously discussed, the ΔE_f for graphene in top-contact with Au is assumed to be -0.103 eV with a value of d~3.3 Å. The ΔE_f in vdW contacted scenario can be obtained from Figure 4.16 by inputting different vdW gap, d. By assuming the tunnelling effective mass m^* is equal to the electron mass, m_e and the tunnelling barrier height is ~7.8 eV [219, 220], the calculated curve fits well with our experimental results (Figure 4.19 d), with d = 9 Å, 19 Å, 25.5 Å and 29 Å for bottom-contact GFETs with ConH = 80 nm, 53 nm, 20 nm and 1.8 nm, respectively. The sheet resistance of the CVD graphene is assumed to be 550 Ω/□ for top-contact GFET and 150 Ω/□, 390 Ω/□, 460 Ω/□, 480 Ω/□, respectively for bottom-contact GFET with ConH values of 80 nm, 53 nm, 20 nm and 1.8 nm, respectively (since the doping level changes according to Figure 4.16).

Thus, the influence of ConL on other contact parameters can be evaluated. Assuming a voltage bias is connected to graphene at the start of contact (X = 0) with a value of 0.025 V (Figure

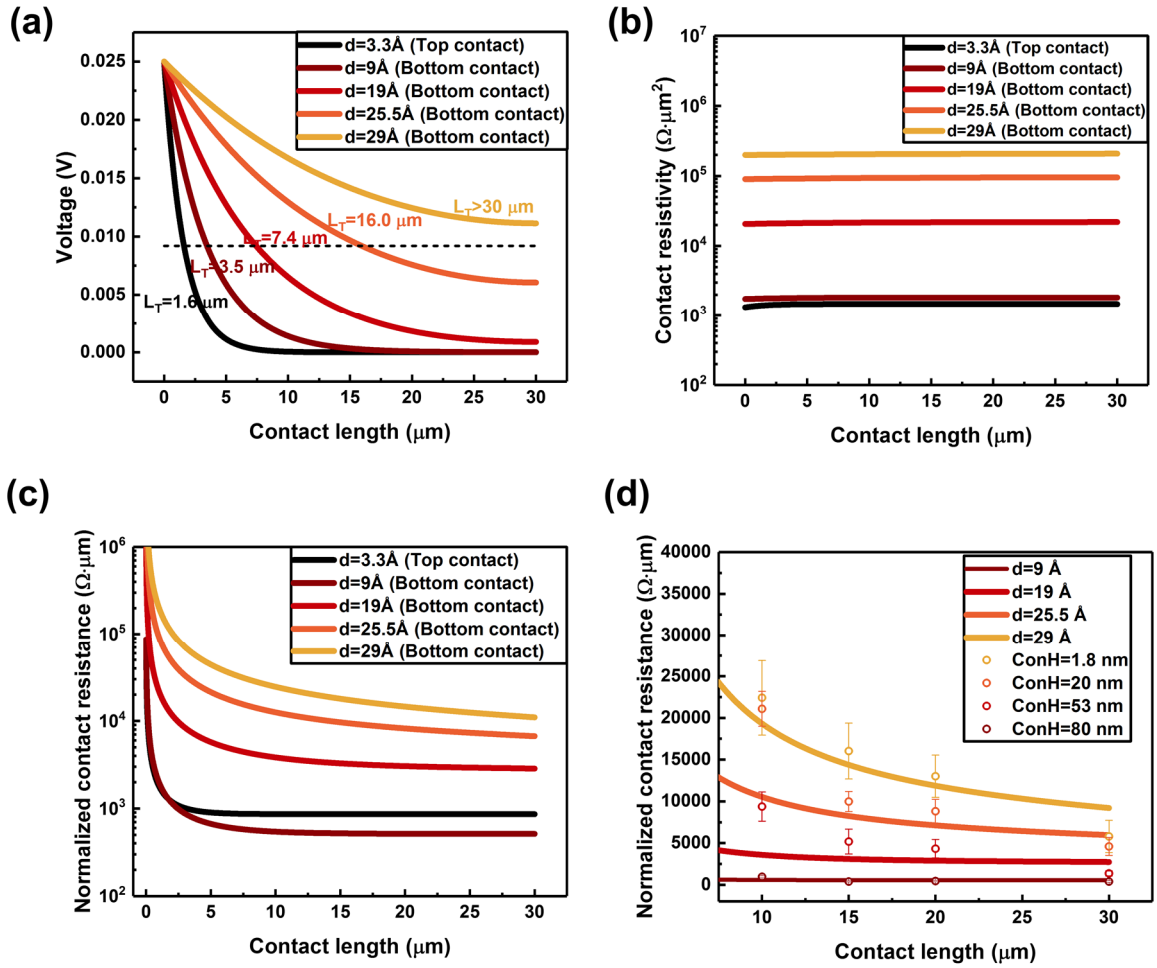


Figure 4.19: The calculated contact parameter under various vdW gap. The voltage drop (a), contact resistivity (b) and normalized contact resistance (c) under various contact length. (d) The comparison between the calculation and the experimental data in terms of contact resistance. Copyright © American Chemical Society. Reprinted, with permission, from [12].

4.18 a), the voltage drop on graphene in the contact region with varying ConL can be obtained (see Figure 4.19a). Further, with this curve, the transfer length L_T in the top-contact GFET can be calculated to be ~1.6 µm, which is consistent with previous reported values (1.4~1.65 µm for holes) [199]. In contrast, the transfer length in a bottom-contacted GFET is 3 µm when the tunnelling barrier width equals to 9 Å (i.e. corresponding to a bottom-contact GFET with a ConH of 80 nm). As a decrease in ConH leads to an increase of the vdW gap (barrier width), the calculated L_T becomes larger. Specifically, the GFET with a ConH of 1.8 nm shows a L_T larger than 30 µm. In all calculated cases listed in Figure 4.17 a, the transfer length of a vdW contacted device is larger than that from a top-contacted device. This is attributed to: (1) a smaller sheet resistance of graphene in the bottom contact scenario due to a higher doping level and (2) a comparable or much larger contact resistivity in the bottom contacted device with a large vdW separations. According to the classic resistor network model, a lower sheet resistance and higher contact resistivity together lead to a longer L_T. And this still holds true for a graphene-metal contact.

Another measure of the quality is the contact resistivity. With respect to the top-contacted FET, the calculated contact resistivity is ~950 $\Omega \cdot \mu m^2$, which is consistent with previously reported value [196, 207]. In the meantime, the contact resistivity in a bottom-contacted GFET increases significantly with the increase of the vdW gap d from 9 Å to 29 Å. This is similar to the results shown in Figure 4.15, as the contact resistivity varies slightly over different ConL (Figure 4.19 b).

Finally, the normalised contact resistance is discussed, which is determined by the L_T and the contact resistivity ρ_C together. In principle, an obvious optimum option to achieve a good contact is a low contact resistivity (strong coupling) combined with a long L_T (long efficient contact). However, since the L_T is positively associated with the contact resistivity, such option is not possible. Then the next two choices left are either a high contact resistivity (weak coupling) combined with a large L_T or a low contact resistivity combined with a small L_T (short efficient contact). Coincidently, the same problem has been studied in the system of CNT, which reveals the latter is more favourable for the realisation of lower contact resistance [221]. Interestingly, this phenomenon is also valid in graphene-metal contacts. As can be seen in Figure 4.19 c, the width normalised contact resistance from a bottom-contacted FET with ConH = 80 nm (a weak coupling but long transfer length, d = 9 Å L_T = 3.5 µm) shows a lower value than that from a traditional top-contacted device (a strong coupling but short transfer length, d = 3.3 Å L_T = 1.6 µm), provided that ConL is longer than 2.5 µm. However, this becomes invalid when the Au-graphene coupling is too weak, even if the L_T is expected to be higher than 30 µm

in this scenario. The calculated results from this model match reasonably well with most of our experimental data, as plotted in Figure 4.19 d.

It should be noted that a negative bias (V=-0.025 V) was hypothesised above to extract the contact resistance (Figures 4.18 and 4.19), where the Au contact has a lower voltage potential than the graphene film. However, in a real bottom-contacted (or top-contacted) GFET, the two cases coexist; on one side the Au has a higher voltage potential while on the other side the graphene's potential is higher. Therefore, the contact resistance measured in the experiments should lie between the above described two extremes. To get an idea of another extreme condition, the contact resistance is calculated under a positive bias (V=+0.025 V). and presented in Figure 4.20. It can be seen that the calculated contact parameters were found to be almost the same. Therefore, the assumption made in Figure 4.18 would not lead to much deviation.

However, it should be noted that the model discussed in this section does not consider the junction resistance arisen due to a carrier transported from graphene under metal to graphene in the channel. While this part is almost negligible at high doping concentration for holes due to the Klein tunnelling [194, 222], it cannot be neglected for electrons. Therefore, the model discussed in this section is expected to lead to a lower estimation of the contact resistance (or higher estimation of the vdW gap). Nevertheless, from the beginning we do not aim to extract any parameters quantitatively from this calculation since many extrinsic factors affects the performance of the CVD graphene-based FET. Rather, the intention of this calculation is to offer a mean to qualitatively or semi-quantitatively illustrate the big difference between bottom-contact and top-contact GFETs.

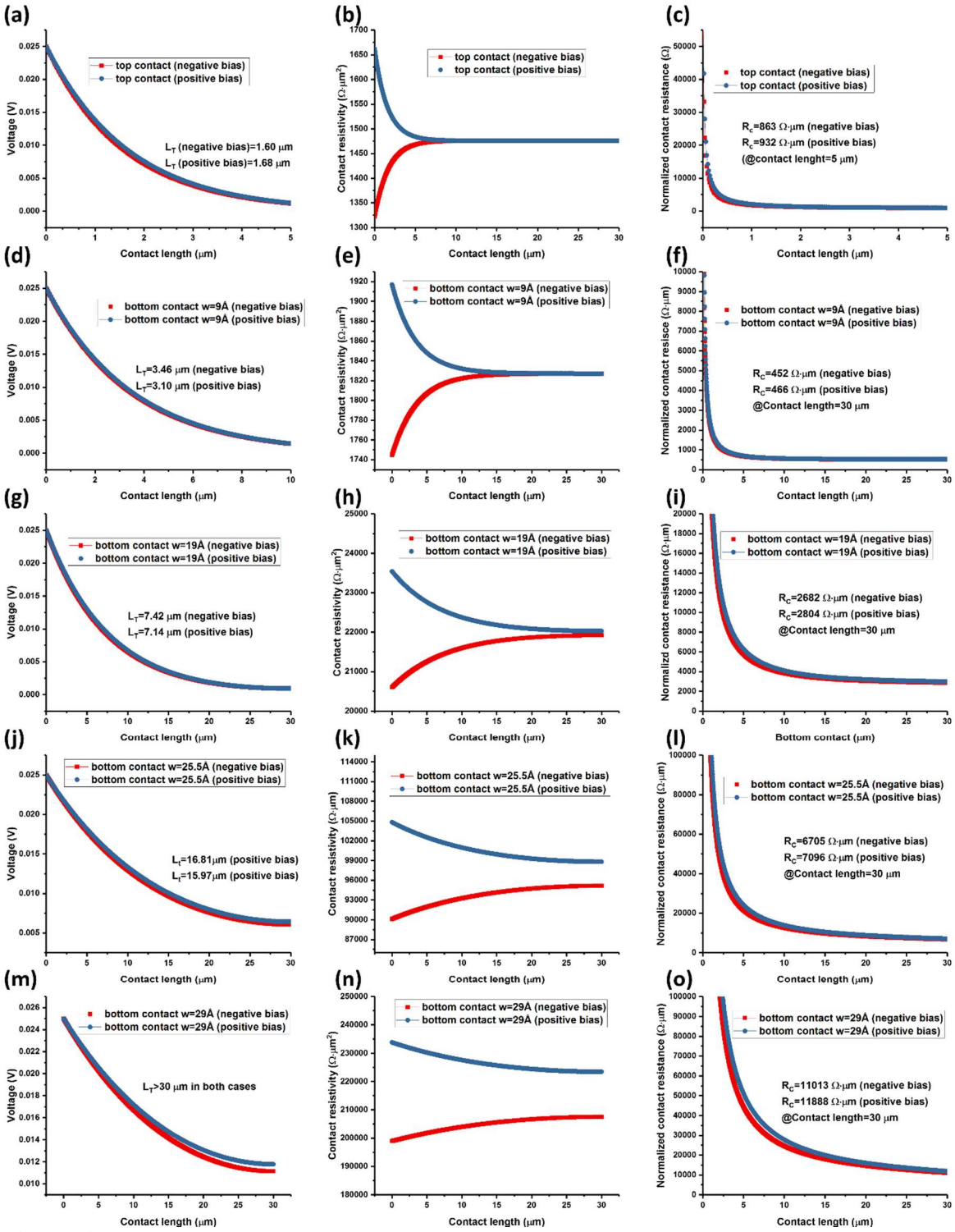


Figure 4.20: Comparisons of voltage drop, contact resistivity and width normalized contact resistance calculated at positive and negative bias. (a)-(c) show the scenario of a top-contacted GFET. (d) to (f), (g) to (i), (j) to (l) and (m) to (o) show the situations of a bottom-contacted GFET with vdW gap of 9, 19, 25.5 and 29 Å, respectively. Copyright © American Chemical Society. Reprinted, with permission, from [12].

4.8 Difference in graphene-Au vdW contact and ZnO-Au vdW contact

Here, a qualitative explanation has been made to explain the two distinct behaviours observed in graphene-Au and ZnO NW-Au vdW contact. Graphene is a semi-metal with its fermi level controlled by external stimuli such as field-effect. The contact between graphene and Au is regarded as a metal-metal contact without any Schottky barrier. However, the graphene-metal contact can still show a large contact resistance. This is mainly due to the small DOS of graphene near the Dirac point. With respect to the vdW contact between graphene and Au, due to its single layer nature, the DOS of graphene can be largely modulated by its contact with Au in vdW regime, leading to a high doping of the graphene film. Such doping is beneficial to achieving low contact resistance. In contrast, ZnO NW is a wide bandgap semiconductor with a cylindrical shape. By using the vdW contact approach, the carriers in the NW need to overcome two barriers for carrier injection, which is a tunnelling barrier and a Schottky barrier. This reason itself makes the vdW contacted ZnO NW FET less efficient. Moreover, with respect to the tunnelling barrier, it is dependent on the distance between NW and the contact electrode. Unlike graphene, the cylindrical shaped NW cannot lead to any intimate contact between the NW and the contact electrode in the bottom contact scenario, which further deteriorates the contact quality. Therefore, vdW contact strategy cannot lead to a good contact for ZnO NW based device.

4.9 Summary

To conclude, the contact resistance from the vdW contacted GFETs depends largely on the vdW separation between graphene and the Au contact. Two effects co-exist and play a role on the contact resistance by decreasing the vdW gap. They are: a) the tunnelling probability of the charge carriers decreases exponentially, which decreases the contact resistivity; b) the doping of the graphene increases due to its coupling with Au [11]. Compared to the undoped graphene, doped graphene results in not only a higher tunnelling current (because of larger DOS of graphene) but also a longer transfer length. In a FET, a higher tunnelling current (lower contact resistivity) and longer transfer length can both improve the quality of the contact. This demonstrates the overall possibility of achieving low contact resistance by vdW gap engineering.

5. Chapter 5: Realising flexible electronics by printing approaches

This chapter discusses the methodology and challenges to realise electronic devices and circuits on flexible substrate, including 1) how to prepare the flexible substrate and further carry out standard microfabrication processes on top (Section 5.1); 2) how the dielectric material (a 100 nm thick Si_3N_4 layer) behaves in various bending conditions (Section 5.2); 3) how to realise the ZnO NW based UV photodetector, together with their performances under various bending conditions (Section 5.3). In addition, the previous chapter proposes that vdW contact between graphene and Au could be an excellent alternative to top- and edge- contacted GFET. In this chapter, the reliability of the graphene-Au vdW contact under various flexible scenarios has also been examined and discussed (Section 5.4). Finally, flexible GFET and logic circuit, based on vdW contact, have been realised (Section 5.5). The stability of the as realised device has been tested up to 100 bending cycles, with a bending radius of 40 mm.

5.1 Substrates in flexible electronics

In flexible electronics, various polymeric thin films, which can facilitate a mechanical deformation, have been explored as the substrates for the realisation of flexible electronic devices and circuits. In this Ph.D. study, a PI film was used as the substrate for the realisation of the flexible devices and circuits. Here, a preliminary investigation into the surface properties of the spin-on PI was carried out and compared with other substrates. For a broad study on the properties of various flexible substrates, several previous papers can be referenced [223, 224]. A PI solution (PI2545 from HD Dupont) was spin coated onto a Si/SiO_2 substrate. The spin speed was set to 500 rpm for 5 s and 2000 rpm for 60 s. The spinning process was repeated twice and after each cycle the sample was heated by a hotplate at 140 °C for 5 minutes (soft bake). The film then was fully cured in an oven at 250 °C for 2 hours. The as-cured film can be subjected to other microfabrication processes to realise various electronic components on top, but the maximum processing temperature is 350 °C; processing at a higher temperature would lead to damaging the polymeric substrate. After all the fabrication steps, the PI along with the fabricated electronic components, can be peeled off from its carrier wafer, leading to freestanding and flexible electronic devices. It should be noted that the successful detachment of the PI is guaranteed by two important factors: 1) Si with a 300 nm SiO_2 layer, instead of pure Si, has been used as the carrier wafer. This is because PI forms a stronger bond with Si, which leads to difficulties in the peeling process; 2) Standard process, as suggested by the

supplier HD Dupont, requires the substrate to be primed by VM-651 or 652 before the spin-coating of the PI solution. This procedure was not followed since it would again lead to a stronger interaction between the carrier wafer and the spin-coated PI film. The photograph of the as-peeled PI film can be seen in later sections.

Surface roughness is an important factor for the substrates used in electronics. In this regard, AFM was used to characterise the surface of the spin-on PI processed under various conditions. Furthermore, commercial PI film (Kapton film from RS components) is also available and can be used for the development of flexible electronics. In order to compare the quality of both substrates, AFM characterisation has also been carried out on the commercial Kapton film. We

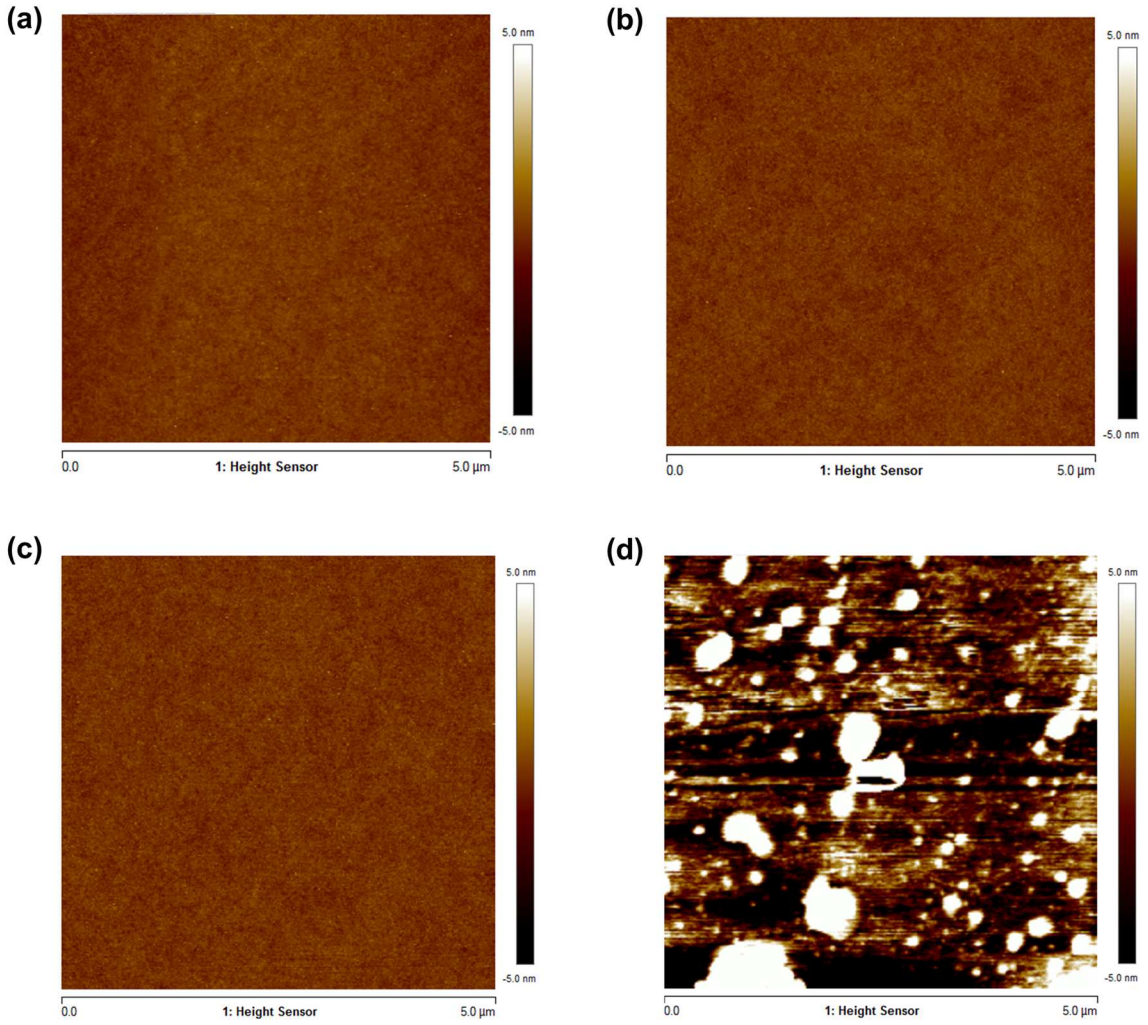


Figure 5.1: The comparison of the surface roughness between spin-coated PI and commercial PI film. (a) PI2545 spin-coated at 2000 rpm for 1min with Primer, Ra~0.18 nm. (b) PI2545 spin-coated at 2000 rpm for 1min without Primer, Ra~0.22 nm. (c) PI2545 spin-coated at 2000 rpm, 1 min for twice without Primer, Ra~0.23 nm. (d) A commercial PI film (Kapton film), Ra~1.5 nm. Copyright © 2019 IEEE. Reprinted, with permission, from [164].

first study the influence of the Primer solution to the surface roughness of the spin-coated film.

As can be seen from Figures 5.1 a and b, the use of Primer does not affect the surface roughness of the film significantly, with R_a changing from 0.18 nm to 0.22 nm for the film coated with and without use of Primer, respectively. The thickness of the PI film can be increased by repeating the spinning process multiple times. To check its influence on surface roughness, AFM characterisation was employed on the sample coated with PI for two times (Figure 5.1 c); the R_a in this scenario is ~0.23 nm. And thus, we conclude that multiple spin-coating cycles would not significantly affect the surface roughness of the film. Finally, the Kapton film from RS components has also been characterised and presented in Figure 5.1d. Compared with the images shown in Figure 5.1 a, b and c, the surface of the Kapton film is very rough with many contaminations on the surface, even after a standard solvent cleaning process. The R_a of the film is ~1.5 nm, which is significantly larger than that of a spin-on PI. As a result, the spin-on PI is used as a substrate for all the later realisation of flexible devices. In addition, the thickness of the PI film spin-coated under various speeds and cycles have also been characterised by

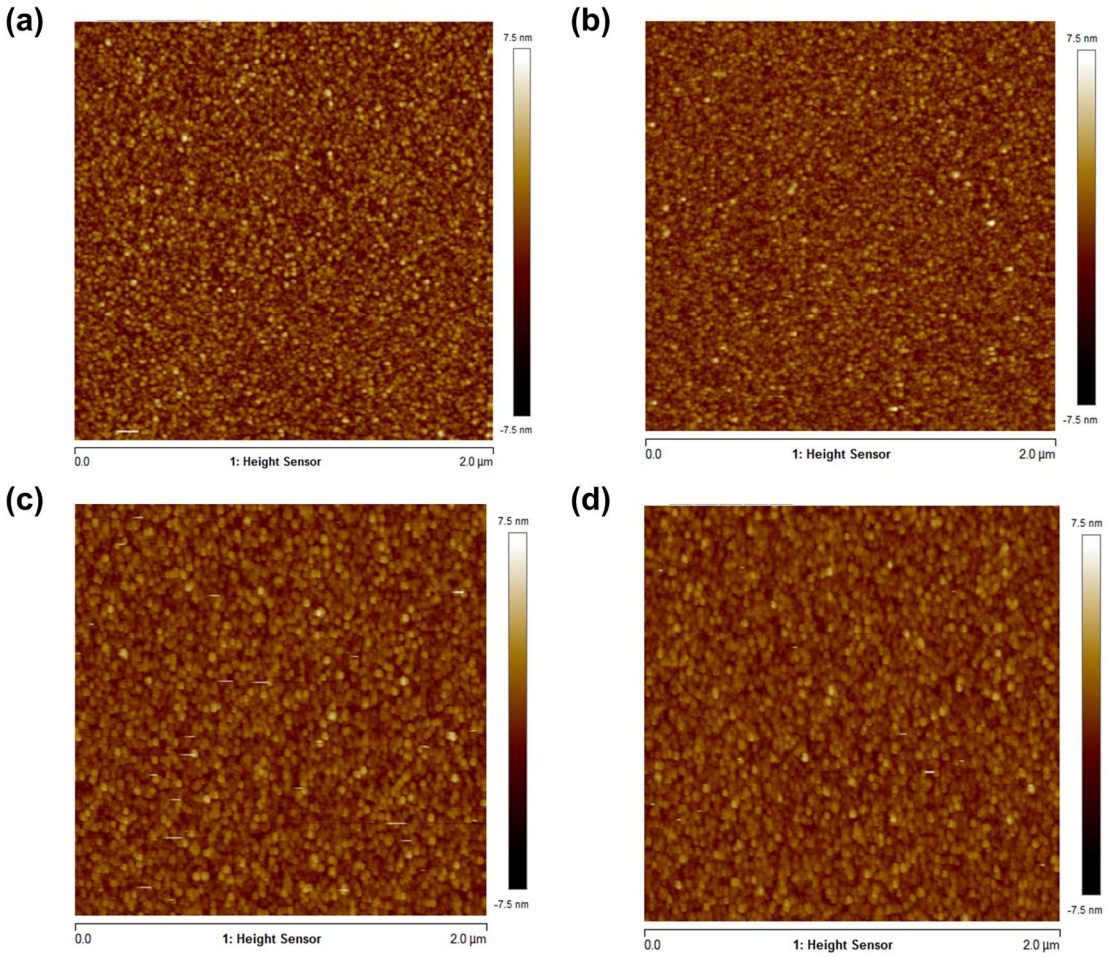


Figure 5.2: AFM characterisations of a 100 nm Si_3N_4 deposited at (a) room temperature on silicon substrate, R_a ~0.92 nm (b) 200 °C on silicon substrate, R_a ~0.76 nm (c) room temperature on PI, R_a ~0.75 nm (d) 200 °C on PI, R_a ~0.68 nm.

Contact Profiler Dektak. The result has already been presented in Chapter 3 (Table 3.1) and will not be included here.

5.2 Dielectrics in flexible electronics

Dielectrics is another problem in flexible electronics. For this, a Si_3N_4 layer has been deposited and characterised, both on Si and PI substrates.

The Plasmalab System 100 ICP-RIE (Oxford Instruments) was used to deposit Si_3N_4. The processing temperature was fixed at room temperature (RT) and 200 °C, respectively. AFM characterisations were first carried out to study the surface roughness of the film. As shown in Figure 5.2, the surface roughness (R_a) of the film becomes lower by increasing the deposition temperature. Meanwhile, the Si_3N_4 deposited on PI film shows a slightly lower roughness than that deposited on Si.

In order to study the dielectric constant and dielectric strength of the film deposited under various conditions, metal-insulator-metal structured capacitors were fabricated with standard

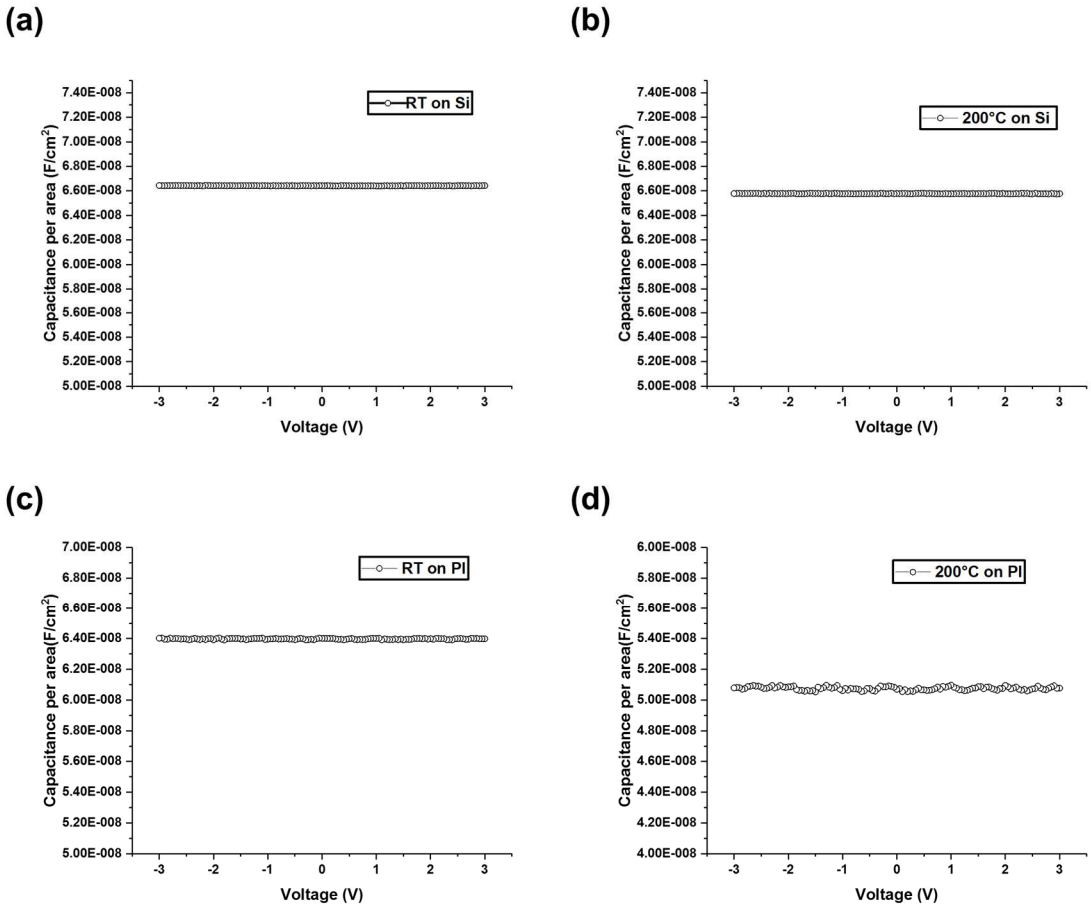


Figure 5.3: The CV characterisation of the Si_3N_4 based capacitors. (a) The film was deposited at room temperature on silicon substrate (b) The film was deposited at 200 °C on silicon substrate (c) The film was deposited at room temperature on PI (d) The film was deposited at 200 °C on PI.

microfabrication processes on both Si and PI substrates. A 3 nm NiCr and 50 nm Au layer were used as the contacts for both top and bottom electrodes. The device geometries for all the capacitors were kept the same. After fabrication, CV and IV measurements were carried out. As shown in Figure 5.3, the capacitance (thus dielectric constant) of all the devices are similar, indicating that the deposition temperature and substrate type (Si or PI) have almost no influence on this figure of merit: the calculated dielectric constant for Figures 5.3 a, b, c, d are 7.4, 7.4, 7.2, 7.2, respectively. In the meantime, the dielectric strength was evaluated by the IV measurement and the data was then shown in Figure 5.4. It can be seen that for both substrates, the film deposited at a higher temperature shows a lower leakage current under the same voltage bias. This result is consistent with the AFM characterisation, where the higher deposition temperature would lead to a smoother surface.

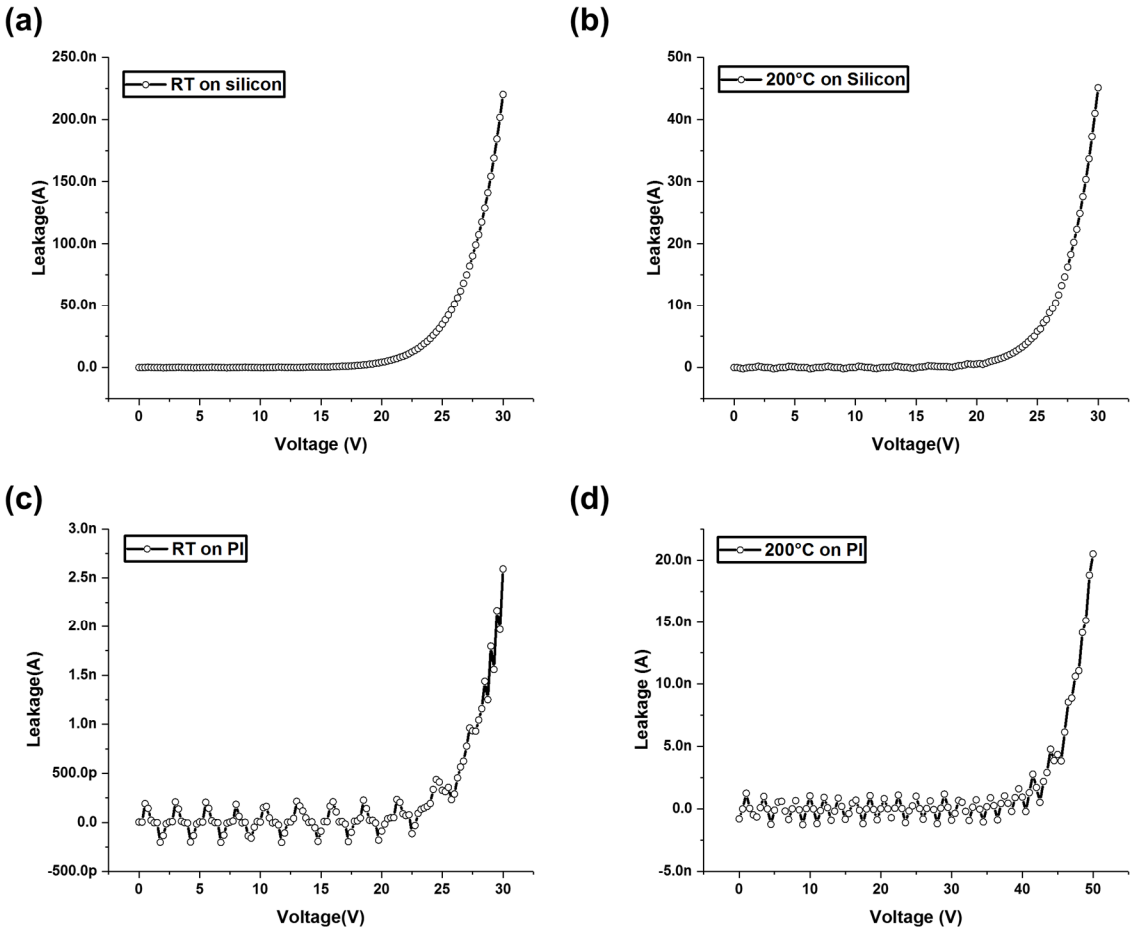


Figure 5.4: The leakage current of the Si_3N_4 based capacitors. The film was deposited at (a) room temperature on silicon substrate (b) 200 °C on silicon substrate (c) room temperature on PI (d) 200 °C on PI.

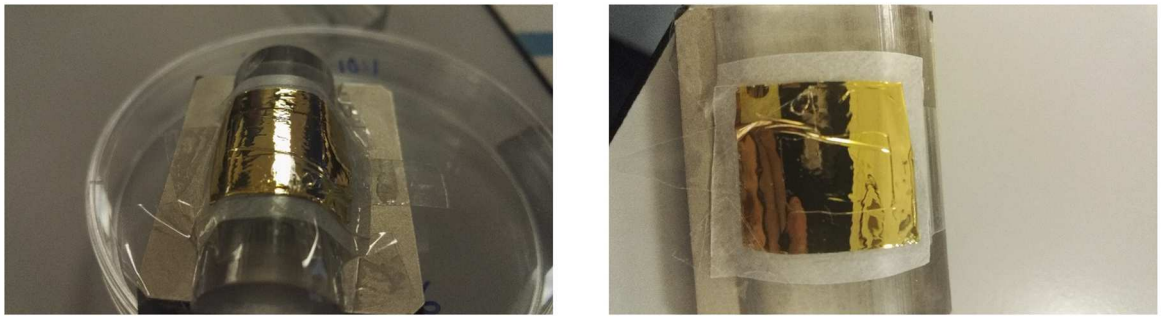


Figure 5.5: The photograph showing the test of flexible capacitors on a specific bending condition.

The dielectric properties of Si_3N_4 were further examined after mechanical peeling off the PI film from its carrier wafer. The as-peeled PI, together with the Si_3N_4 based capacitors were bended at various bending radius by using 3D printed moulds as shown in Figure 5.5. In order

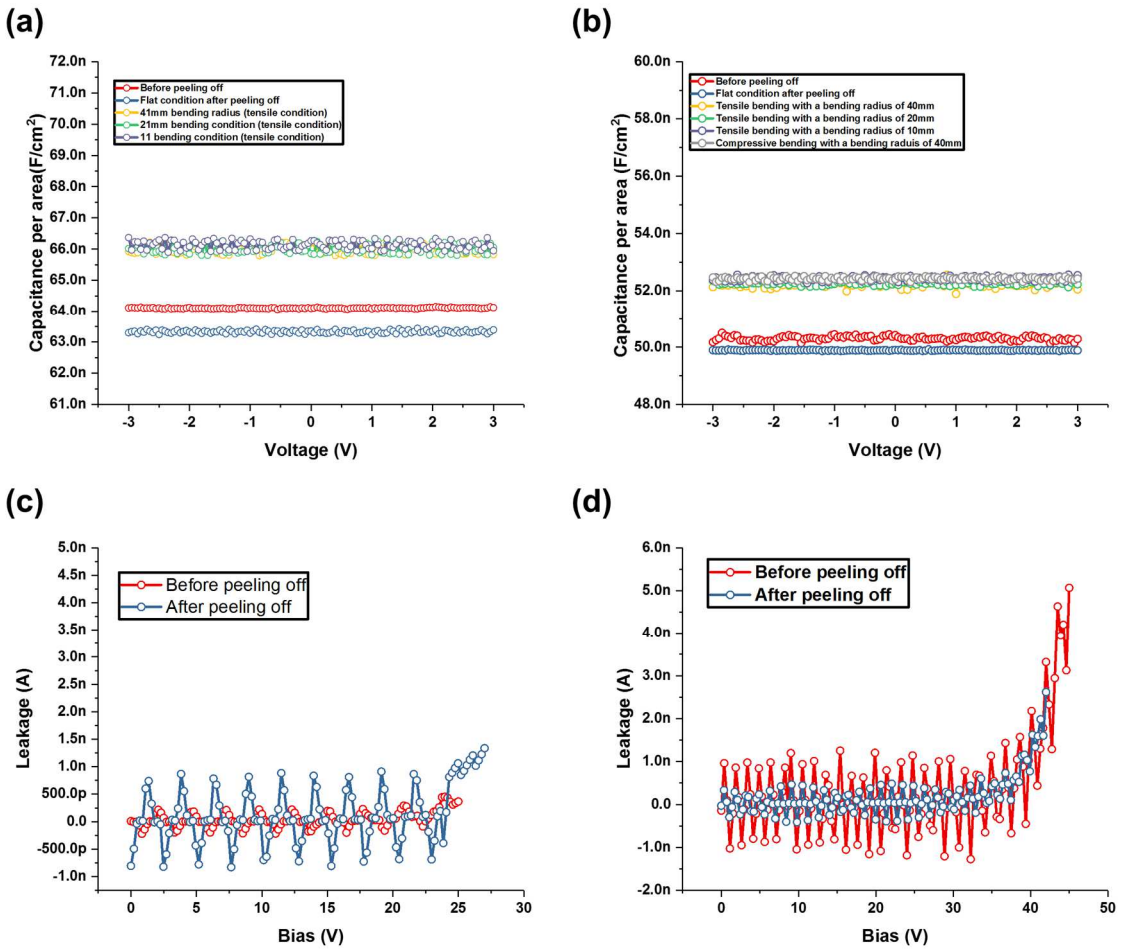


Figure 5.6: The CV and IV measurements under various conditions. (a) and (c): The CV and IV measurement of capacitor based on 100 nm Si_3N_4 deposited at room temperature. (b) and (d): The CV and IV measurement of capacitors based on ~123 nm Si_3N_4 deposited at 200 °C.

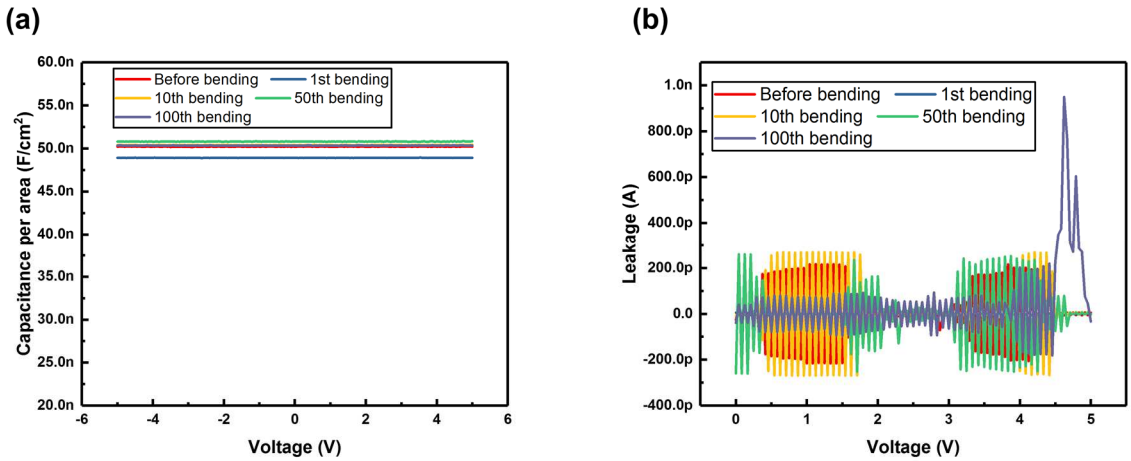


Figure 5.7: Cyclic bending test of the flexible capacitor with a bending radius of 40 mm. (a) The CV measurement and (b) the IV measurement.

to evaluate the impact of the peeling process, CV and IV measurement were performed before and after the peeling process, as well as later at various bending conditions. The measurement results have been shown in Figure 5.6. It can be seen that both the capacitance and the leakage current did not show significant changes after peeling off the PI film from its carrying substrate, which indicates a reliable process for realising flexible devices on spin-on PI film. Moreover, under various tested bending conditions, the capacitance remains almost unchanged, which indicates that Si_3N_4 could be used as a dielectric for flexible FETs. We further explored the retention of this material under various bending cycles and the results have been plotted in Figure 5.7. As can be seen from the figure, the dielectric remains stable for up to 100 cycles of bending test, with a bending radius of 40 mm.

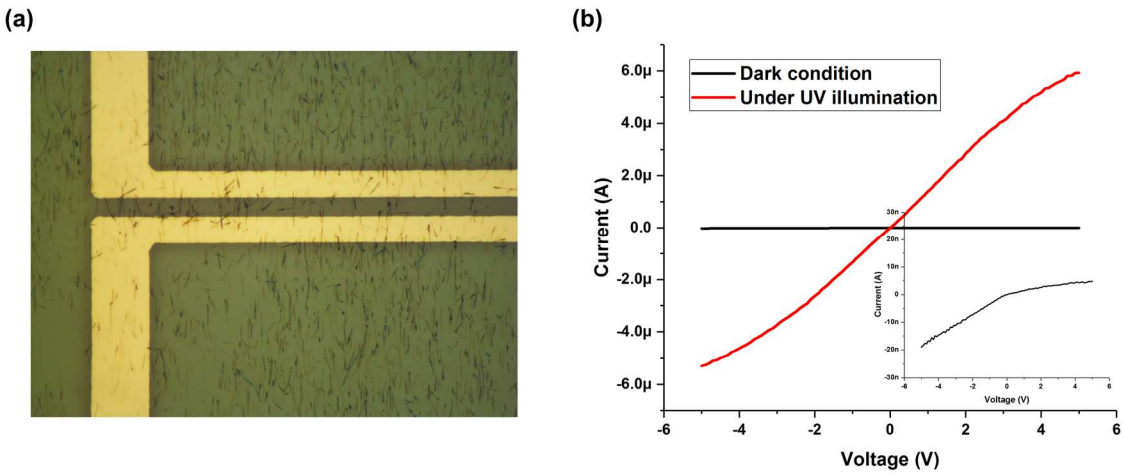


Figure 5.8: The printed ZnO NW UV photodetector. (a) The optical microscopy image of the flexible ZnO NW based UV photodetector on PI film. (b) The I-V characteristics of the device under dark condition and UV illumination (Inset: the enlarged plot of the dark current). The power density of the UV light is ~1 μW/cm^2.Submitted to EDTM 2020.

For all the capacitors presented here, a leakage current is observable. This indicates that the carrier in the capacitor can migrate under external bias. Carrier tunnelling under external voltage bias is one of the reasons for this phenomenon despite of the large tunnel barrier introduced by the dielectric material. Another reason can be due to the defect in the dielectric, which can effectively lower the tunnelling barrier. Overall, it is common for the existence of the leakage current for a capacitor. Since the capacitor is crucial for a successful realisation of FET, it is reasonable to consider whether such leakage is in the suitable range or not. Practically, the FET can work successfully under a leakage current ~10 nA without disturbing the field-effect. Therefore, it is conclude that the capacitor realised here can be used later for the realisation of flexible FET device.

5.3 Flexible ZnO NW based UV photodetector

In this section, the fabrication and characterisation of flexible ZnO NW based UV photodetectors are discussed. The same process was employed to realise the PI film which serves as the flexible substrate. After deposition of a 100 nm thick Si_3N_4 layer, NWs were printed on the PI film, followed by metallisation to define contacts electrodes, as has been discussed in Chapter 4. The deposition of the Si_3N_4 is to encapsulate the as-coated PI film, without which further microfabrication processes realised on top would become problematic. The as-fabricated devices were characterised before and after the peeling off the film from its carrying wafer, as well as at various bending states.

Figure 5.8 a shows the as-fabricated ZnO NW based UV photodetector on PI substrate. Each device contains several ZnO NWs as the channel material. The photoresponse of the as-fabricated devices were characterised by a UV LED ($365 < \lambda < 370$ nm). As shown in Figure 5.8 b, the dark current of the device is ~several nano amperes. Once the UV light has been shone on the device, a significant increase in the current can be observed, indicating a sensitive detection in the UV light. The significant UV sensitivity of the device is attributed to the surface states in the ZnO NWs [93, 225]. Under an ambient condition (dark condition), abundant oxygen molecules are chemisorbed on the NW's surface, which leads to electron depletion in the NWs by capturing the free electrons (O_2 (g) + e^- → O_2^- (ad)). With UV illumination, the electron hole pairs are generated ($h\nu \rightarrow h^+ + e^-$). The generated holes react with the chemisorbed oxygen species and create unpaired electrons in the NWs ($h^+ + O_2^-$ (ad)→ O_2 (g) + e^-). These extra electrons are accelerated under external bias and collected by the electrodes, leading to a net current (photocurrent). To study the response speed of the photodetector, time

resolved measurement was carried out. As can be seen in the Figure 5.9, the device shows a fast and drastic rise after the UV LED was switched on. However, once the UV light was switched off, the decay of the signal is shown to be relatively slow and smooth. For ZnO NW based photodetector, there are generally two ways to define the rise and decay time. The first way is to model the change of photocurrent by a sum of exponential functions [124]:

$$I_{photo}(t) \sim \sum_{i=1}^{N} A_i \exp(-t/\tau_i)$$

Where N is the exponential term, A_i is a normalisation constant for each exponential term and τ_i is the parameter to characterise the rise and decay time. As shown in Figure 5.9, the rise time can be fitted into one exponential term with τ_{rise} ~10.0 s. And the change in the decay of the photocurrent can be fitted into two exponential functions, with τ_{decay1} ~7.6 s and τ_{decay2} ~47.3 s, respectively. However, it should be noted that for photodetectors realised by printing, neither the total number nor the diameter of the printed NWs are accurately controlled at this stage. In this regard, it is common to fit the photocurrent in various number of exponential terms for different device, which may lead to some inconvenience to the later study. Another way to define the rise (decay) time is to measure the time it takes for the photocurrent to change from

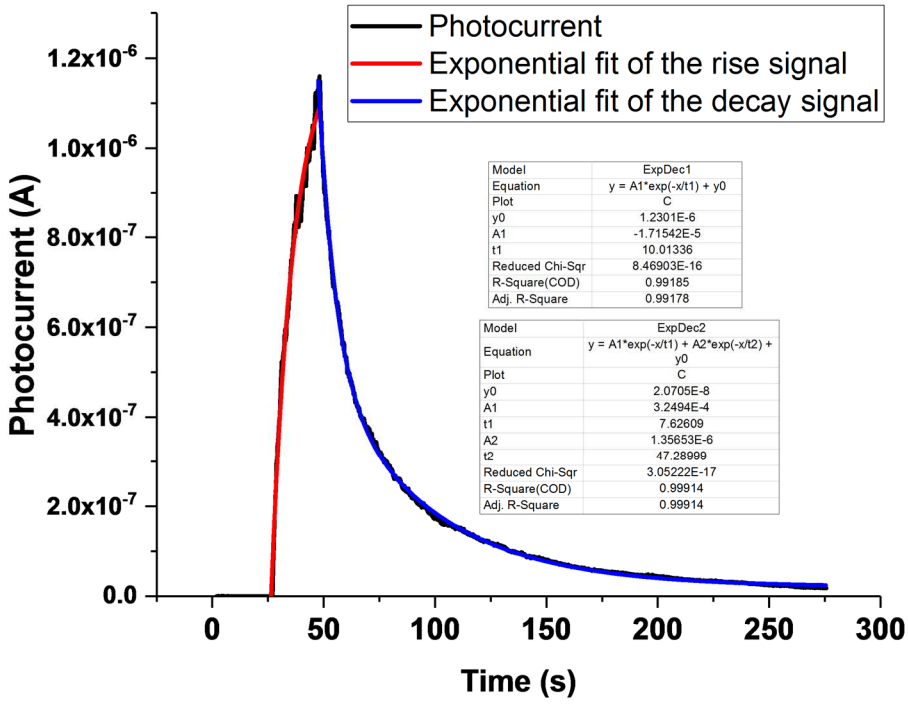


Figure 5.9: The time resolved measurement showing the rise and decay of the photocurrent. The power density of the UV light is ~0.43 μW/cm^2.

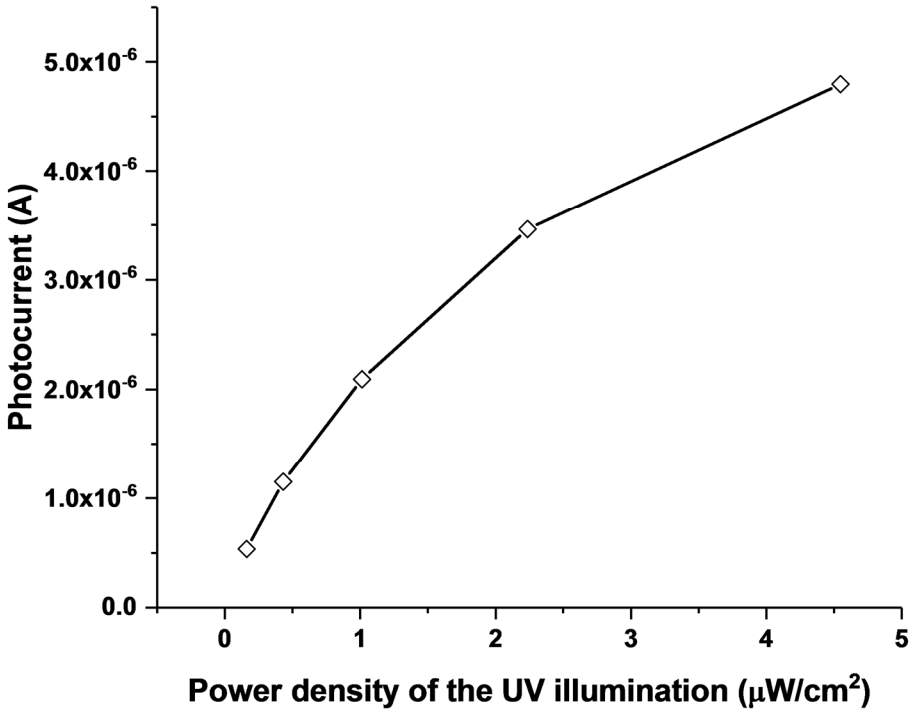


Figure 5.10: The relationship between the photocurrent and the power of the UV LED. Submitted to EDTM 2020.

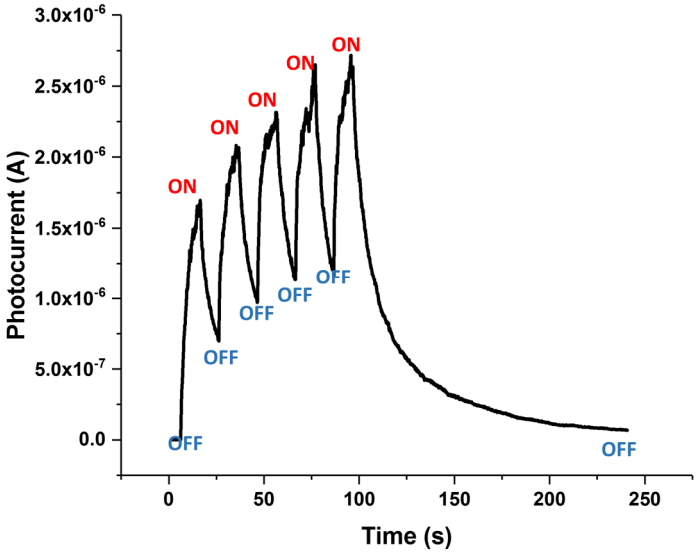


Figure 5.11: Multi-cycles measurement of the photocurrent. Submitted to EDTM 2020.

10% (90%) to 90% (10%) of its total value. The $\tau_{rise\ 10\%\ to\ 90\%}$ and the $\tau_{decay\ 90\%\ to\ 10\%}$ are calculated to be ~18.2 s and 77 s, respectively. And such definition is adopted in later studies. We further studied the relationship between the photocurrent and the power intensity of the UV illumination. As can be seen in Figure 5.10, the photocurrent increases sub-linearly with respect to the power intensity of the UV light. This can be understood by the limitation in the surface states: when the illumination power is low, all the photogenerated holes can be trapped at the surface states and thus lead to the increase of the unpaired electrons; when the

illumination power is high, only part of the photogenerated holes can be trapped at the surface states, which results in a sublinear increase of the photocurrent. Furthermore, with the value of the photocurrent under various powers of illumination, it is common to calculate the responsivity R of the photodetector by using the equation $R = \frac{I_{Photo}}{P}$, where P represents the power of the UV light illuminated on the NWs. However, since the device is composed of multiple NWs with various diameters, it is difficult to extract the exact power illuminated on the NW channel. Therefore, we can only study the relationship between the photocurrent and the power density of the UV illumination, as shown in Figure 5.10.

To further examine the cyclic sensing performance of the photodetector, the device was exposed to periodical UV illumination with a power density of ~1 μW/cm^2. As can be seen from Figure 5.11, although the on/off ratio of the photodetector decreased during the test (due to the long decay time needed), the device showed a robust response to UV illumination.

In order to investigate the bendability of the flexible UV photodetector, the as-fabricated device was subjected to cyclic bending test with a bending radius of 40 mm. The characterisation results are shown in Figure 5.12. As can be seen from the figure, the device shows a robust response to the UV illumination even after bending for 1000 cycles. Furthermore, we have extracted the photocurrent, rise time and decay time of the device under various bending cycles,

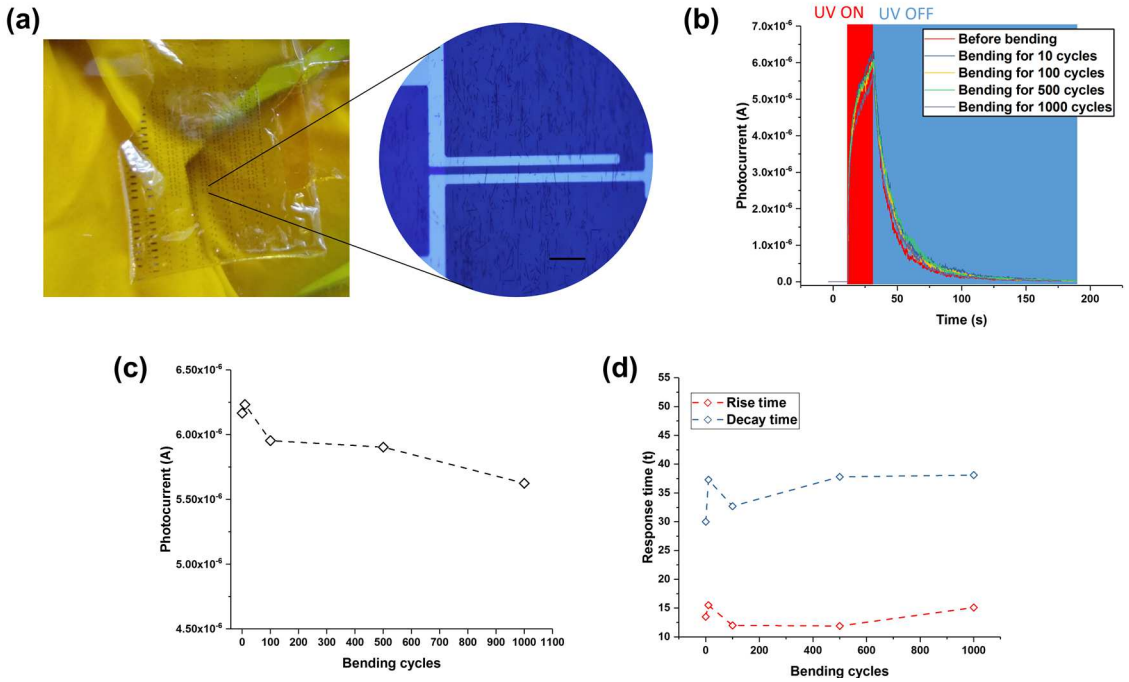


Figure 5.10: The characterisations of the flexible UV photodetector. (a) The photograph and optical microscopy images of the flexible UV photodetectors based on printed ZnO NWs. (b) The relationship between the photocurrent and time. (c) and (d) The photocurrent, rise time and decay time under various bending cycles. The power density of the UV light is ~0.3 μW/cm^2. Submitted to EDTM 2020.

all of which have shown an insignificant change upon the bending test. Thus, we conclude that the flexible UV photodetector has been successfully realised by a printing method. The demonstrated device shows a strong and robust sensitivity to UV illumination and can be bent up to 1000 cycles. However, its response time is not fast compared to other materials [226, 227]. In this regard, it is proposed that the demonstrated sensor is appropriate for UV dosimetry application, which does not require a fast response.

5.4 vdW contact in flexible electronics

Previous subsection discusses the NW based flexible sensors. In this section, the research interest is focused on the graphene. As has been discussed in Chapter 4, vdW contact can lead to a high-performance GFET. Moreover, since it is realised by transfer printing, it has a natural suitability for flexible electronics [223, 224]. However, compared to other molecular-level interactions such as a covalent bond, vdW force is regarded to be a weak force and is highly dependent on the vdW separation. In this regard, whether the morphological deformation (generated by bending) will lead to a change in the vdW gap and therefore lead to a significant

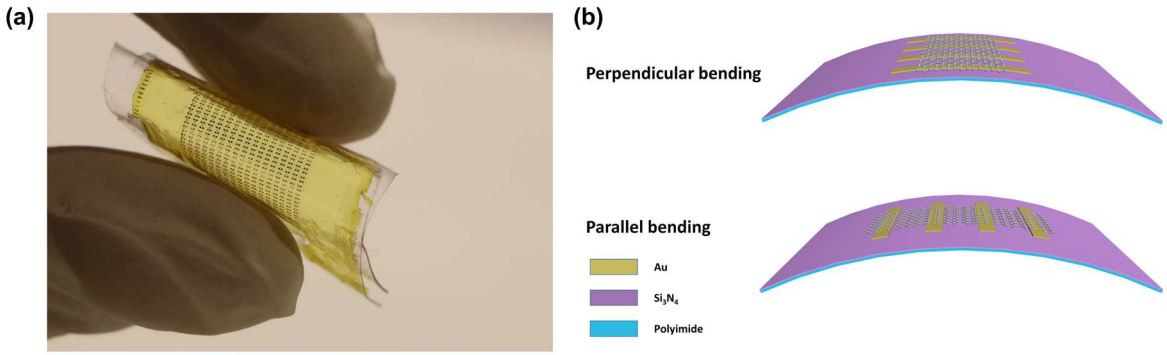


Figure 5.11: The photo and illustration of the graphene-Au vdW contact on flexible substrate. (a) The photograph of the graphene-Au vdW contact on PI substrate (b) The schema showing the definition of the perpendicular and parallel bending. Copyright © American Chemical Society. Reprinted, with permission, from [12].

variation in the performance of the vdW contact has not been carefully examined. Such an understanding is necessary if the proposed vdW contact is going to be used in the flexible electronics. Therefore, a study intended to investigate the influence of mechanical deformation on the reliability of bottom-contacts was carried out. The graphene-Au vdW contact was realised on a PI film (Figure 5.13 a). The fabrication procedure is similar to the one described in Chapter 4, except a PI film with a 100 nm Si_3N_4 has been used as the substrates. Nine measurements were performed under different mechanical deformation states, as specified in Table 5.1.

Table 5.1: Tested conditions for graphene-Au vdW contact.

Serial Number	Direction	Type of Bending	Bending Radius (mm)
A	NA	Flat	∞
B	Parallel type	Tensile bending	40
C	Perpendicular type	Tensile bending	40
D	Parallel type	Tensile bending	20
E	Perpendicular type	Tensile bending	20
F	Parallel type	Compressive bending	40
G	Perpendicular type	Compressive bending	40
H	Parallel type	Compressive bending	20
I	Perpendicular type	Compressive bending	20

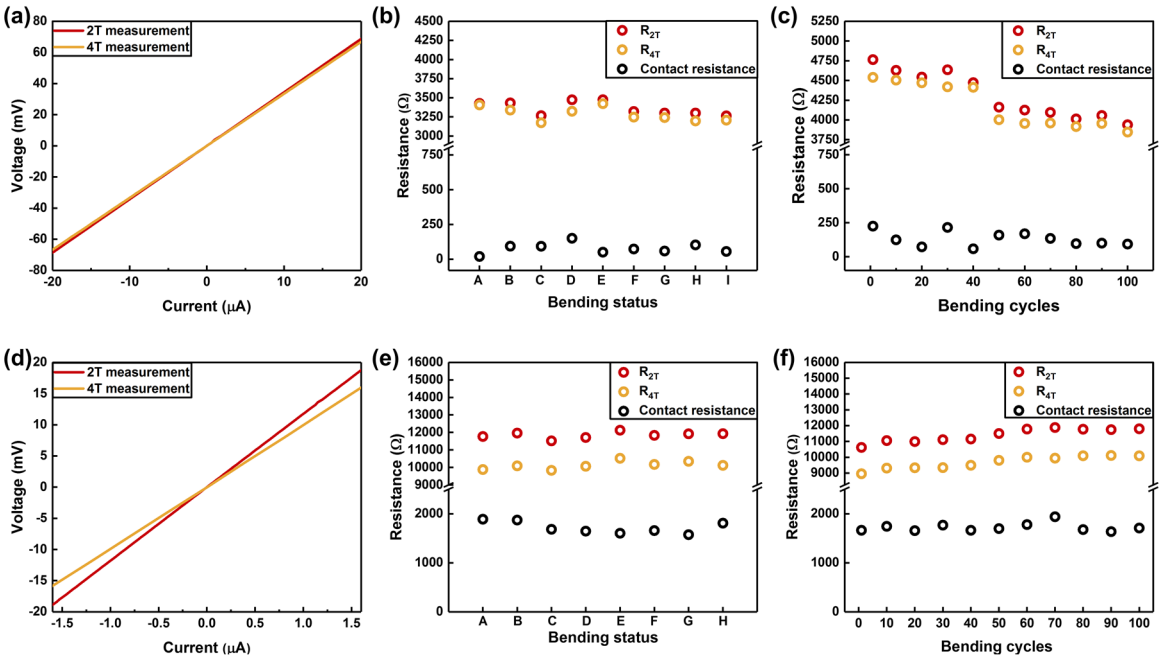


Figure 5.12: The contact resistance under various bending conditions. The 2T and 4T output characteristics measured under high (|~80 nm, a) and low (~2 nm, b) ConH. The contact resistance extracted under various bending status under high (b) and low (e) ConH. The cyclic test of contact resistance under high (c) and low (f) ConH. Notably, the data in (b) and (c) are taken from different devices with the same ConH. The ConL is 30μm for all the cases. Copyright © American Chemical Society. Reprinted, with permission, from [12].

The bending direction used in the table is defined in Figure 5.13 b. The contact resistance was extracted under various bending conditions and the data was plotted in Figure 5.14. The ConL of the devices is 30 μm for both cases and the ConH is ~80 nm and ~2 nm for the data shown in Figures 5.14 a and d, respectively. Typical output characteristics, for graphene-Au vdW

contact realised under high and low ConH have been plotted in Figures 5.14 a and d, respectively. The change in contact resistance is similar to the phenomenon discussed in Chapter 4, indicating a significant modulation of contact resistance by controlling ConH. Then, we examined the contact resistance under various bending conditions. As can be seen from Figures 5.14 b and e, no significant change can be observed, which likely indicates a stable vdW interaction upon mechanical deformation. Cycling tests were also performed to study the retention of such vdW contact, which has been shown in Figures 5.14 c and f respectively for the condition of high and low ConH. The contact resistance only shows minor changes after

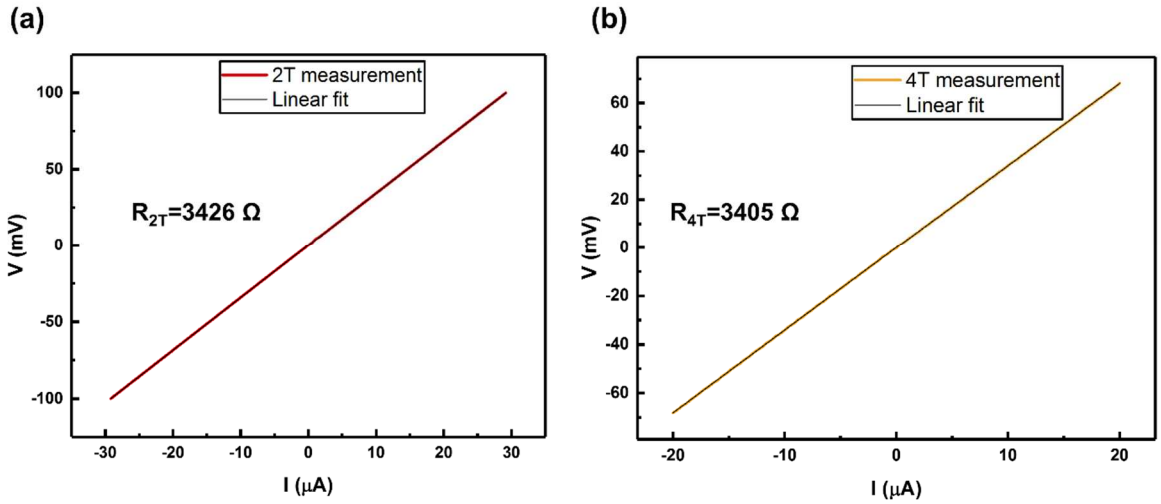


Figure 5.13: The 2T and 4T output characteristics measured under high ConH of ~80 nm at condition A. Copyright © American Chemical Society. Reprinted, with permission, from [12].

100 cycles of tensile bending (bending direction parallel to the graphene channel) while the bending radius was kept as 40 mm. Furthermore, those minor variations are believed to have originated from the change of contact resistance between the probe tip and the metal pad on the device. Since the morphology of the device varies under different bending conditions, the contact between the probe tip and the metal pad is likely to be changed in an uncontrollable manner. However, with existing data, it is enough to conclude that the resistance from graphene-Au vdW contact shows an insignificant change.

It should be noted that a low contact resistance is also achievable with a vdW contact approach on a flexible substrate. As shown in Figure 5.14 b and Figure 5.15, a contact resistance down to ~210 Ω·μm has been achieved (Condition A), similar to previous values extracted on rigid substrates (see Chapter 4). This is the first time that a relatively accurate extraction of the contact resistance from flexible GFETs has been possible by using four terminal measurement methods: all previous work (see Table 5.2) has adopted a fitting method proposed in Ref. [228],

which assumes a constant contact resistance for all carrier densities. Even when considering these inaccuracies, the previous minimum contact resistance is ~300 Ω·µm and so it is indeed possible to improve on this historic value.

To conclude, this section studies the graphene-Au vdW contact on flexible substrates. Such contact shows a stable nature under various bending tests, which guarantees its reliability for large-area flexible electronics. Benefitting from this feature, flexible FETs and circuits can be realised with stable performance on flexible substrates (see Section 5.5).

Table 5.2: Comparison of monolayer graphene-metal contact properties on flexible substrate at room temperature. Copyright © American Chemical Society. Reprinted, with permission, from [12].

Electrode	Contact Architecture	Extraction method	Normalised Contact Resistance (Ω·µm)	Sub-strate	Compatibility with large-area flexible electronics	Carrier density (cm^{-2})	Ref #
Au	Top-contact	Fitting method	8000	PET	No	NA	[229]
Ti/Pd/Au	Top-contact	Fitting method	300	PEN	No	NA	[230]
Ni/Au	Top-contact	Fitting method	~7500	PI	No	NA	[231]
Au	Top-contact	Fitting method	~800	PI	NA	NA	[232]
NA	Top-contact	Fitting method	20000	PI	No	NA	[233]
Graphene	Top-contact	Fitting method	1164000	PEN	Yes	NA	[234]
Au	Top-contact	Fitting method	~8000	PET	No	NA	[235]
Au	Bottom-contact	Four terminal measurement	Down to 210	PI	Yes	1.75×10^{12}	This work

PET: Polyethylene terephthalate, PEN: Polyethylene naphthalate, PI: polyimide.

5.5 Flexible GFETs and logic circuits

This section discusses the fabrication and characterisations of flexible GFETs and corresponding logic circuits based on GFET. For this, PI film has been used as the substrate

for the flexible devices and circuits; a 100 nm Si_3N_4 has been used for the dielectric materials, and the vdW contact strategy has been adopted to realise the source and drain contacts. The detailed fabrication process has been described as follows:

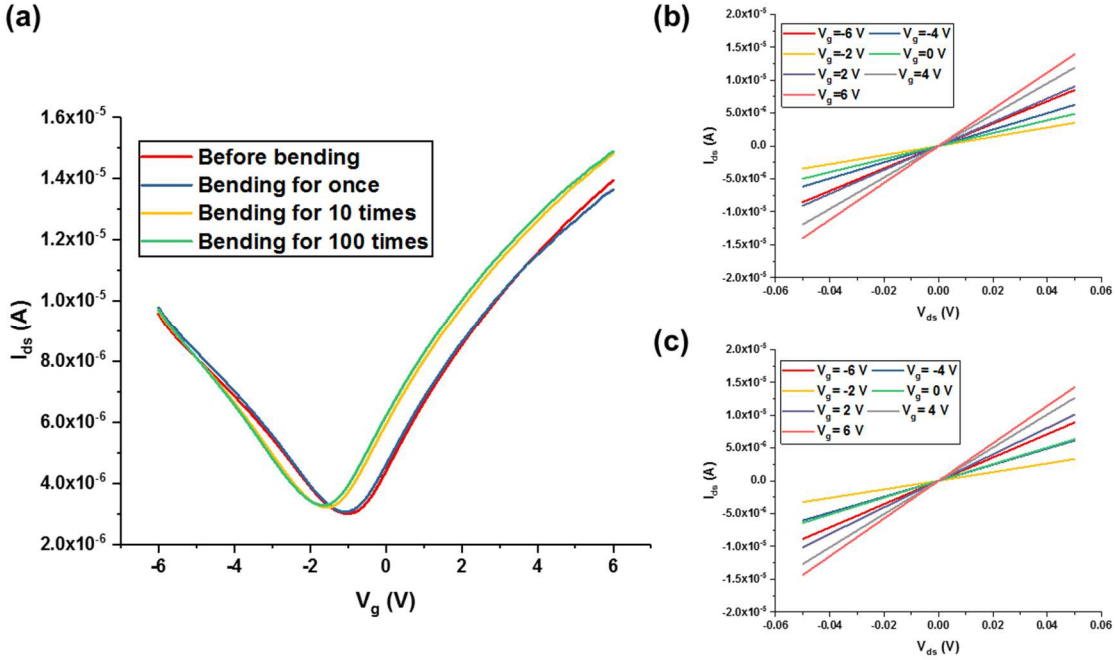


Figure 5.14: The electrical characterisation of flexible GFET. (a) The transfer curves measured at various conditions. V_{ds}=50 mV. (b) and (c) The output characteristics of the flexible GFETs before and after 100 cycles of bending at a bending radius of 40 mm.

A polyimide solution was spin coated onto a silicon/silicon dioxide and cured as previously described. After the PI process, an isolation layer of 100 nm Si_3N_4 was deposited at 200 °C. The PI/Si_3N_4 film serves as the substrate for realising flexible devices. Afterwards, a 35 nm Au electrode was deposited by E-beam evaporation which acts as the gate contact. A 100 nm Si_3N_4 deposited at 200 °C was used as the gate dielectric material. After a short treatment by hexamethyldisilazane (HMDS), photoresist S1805 (from MicroChem) was spin coated on the substrate at 4000 rpm for 30s, followed by a soft bake at 65 °C for 1 minute. Then UV lithography, metallisation and standard lift-off process were each employed to realise the source and drain contacts with 80 nm NiCr/Au. Afterwards, monolayer graphene was transferred onto the processed flexible substrate to form the contacts between the graphene and source and drain terminals. The transferred graphene film was finally patterned into individual stripes to realise the large-area GFETs array.

The as-realised FET was first characterised as shown in Figure 5.16. As can be seen from the figure, the device can work successfully even after 100 cycles of bending, with a bending radius of 40 mm. No obvious performance degradation has been observed. Only minor shift of the Dirac point has been seen in Figure 5.16 a, which can be attributed to the doping from the

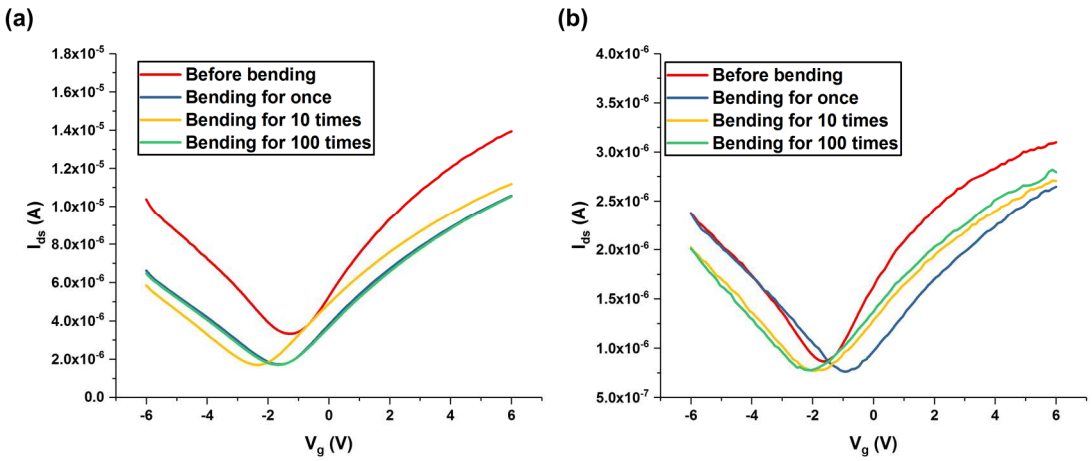
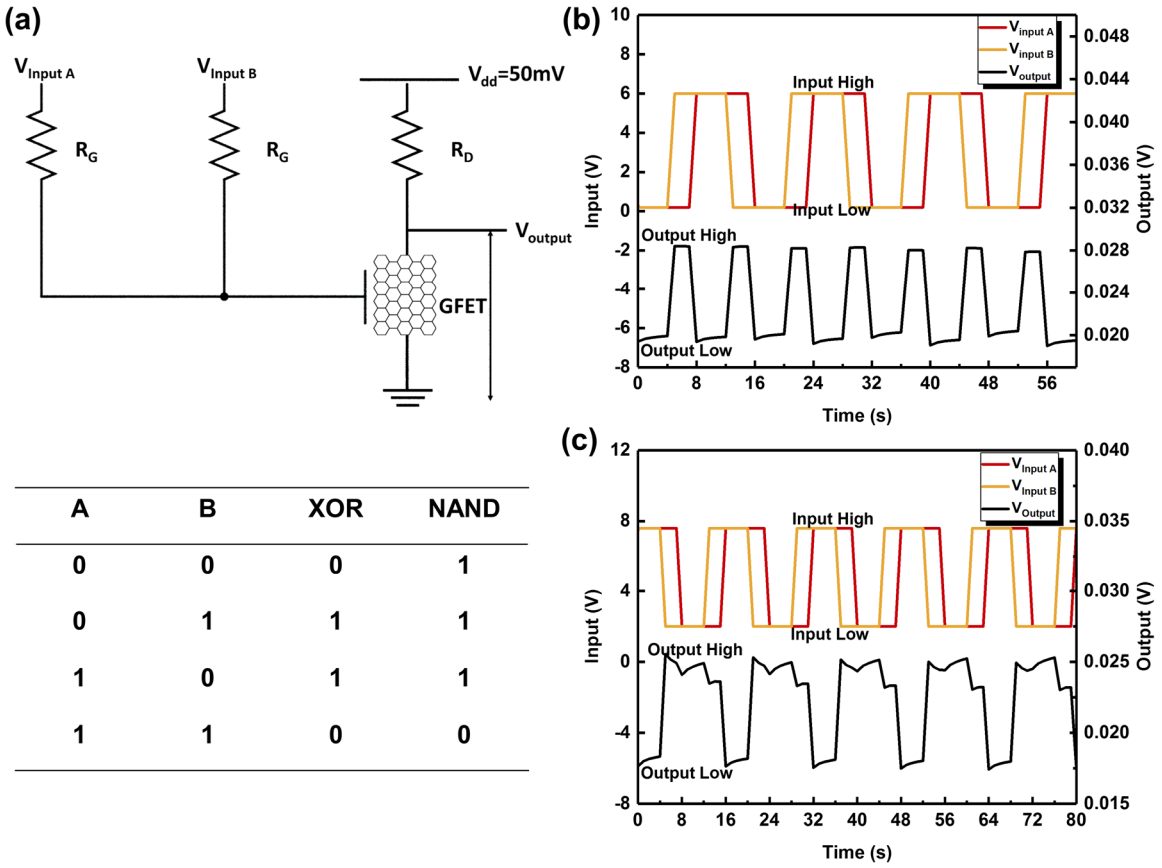


Figure 5.15: The change of transfer curves under various cycles of bending for another two devices.

ambient environment. Multiple devices were checked to further confirm the stability of the flexible devices under the bending test. The changes of transfer curve with respect to the bending test have been presented in Figure 5.17 for another two devices. As can be seen from the figure, except from the Dirac point shift, no obvious degradation were observed.

Next, XOR and NAND logic circuits were realised by using the transistor-resistor logic (TRL) strategy as shown in Figure 5.18. This strategy minimises the number of transistors used for the logic circuits so is suitable for fast demonstration. The resistance of R_G and R_D was 42 kΩ and 10 kΩ, respectively. As can be seen from the Figure 5.18 b and c, the circuits can work properly to provide the logic function.

Here, by taking XOR gate as an example, the working mechanism of the graphene-based logic gates has been explained. As shown in Figure 5.18 a, both the voltage inputs A and B were connected to the gate terminal of the GFET. Assuming the transfer curve of GFET is symmetric with respect to the Dirac point, the value of the input high (1) and low (0) are deliberately selected to be two bias voltages on the hole and electron branch of the transfer characteristics, and generate the same number of charge carriers. When the input for (A, B) is (1, 0) or (0, 1), the gate terminal of the FET is biased at the value of V_{Dirac}. In this case, the resistance of GFET reaches its highest and thus leads to the largest output voltage from the voltage divider. Meanwhile, when the input signal for (A, B) becomes (0, 0) or (1, 1), the $|V_G-V_{Dirac}|$ has the largest deviation from the Dirac point. The resistance of the FET becomes lowest, which further



A	B	XOR	NAND
0	0	0	1
0	1	1	1
1	0	1	1
1	1	0	0

Figure 5.16: The electrical characterisation of flexible logic circuits. (a) The logic diagram and the truth table for the graphene based logic circuits. (b) and (c) The electrical characterisation of the XOR and NAND gate, respectively after 100 cycles of bending. Copyright © 2019 IEEE. Reprinted, with permission, from [173].

results in a lowest output voltage. In this way, the value of the output voltage can be controlled by changing the input (A, B), which provides the function of logic operation.

As explained above, the performance of the logic gate is directly related to the position of the Dirac point as well as the gate capacitance of the dielectric. For the XOR gate fabricated on the rigid substrate (data not shown), the Dirac point of GFET was ~14.5 V. In this case, the input high and input low should be on each side of the Dirac point, with the value of each being chosen as 9 V and 20 V, respectively. Meanwhile, for the XOR gate demonstrated on the flexible substrate, the Dirac point was ~3.1 V (data not shown). Thus, the value for input high and low could be chosen as ~6 and ~0.2V, respectively. For a decent logic circuit, one important criterion is that the input and output signal should match with each other. Although it is not realised in Figure 5.17, this aspect can be theoretically achieved by either tuning the dielectric thickness to a lower value or controlling the Dirac point position to ~0 V. This will be achieved in future work.

Finally, it should be noted that The logic gate was realized with one single GFET connecting three off-the-shelf resistors. This demonstrates the proof of concept that using GFET can realise

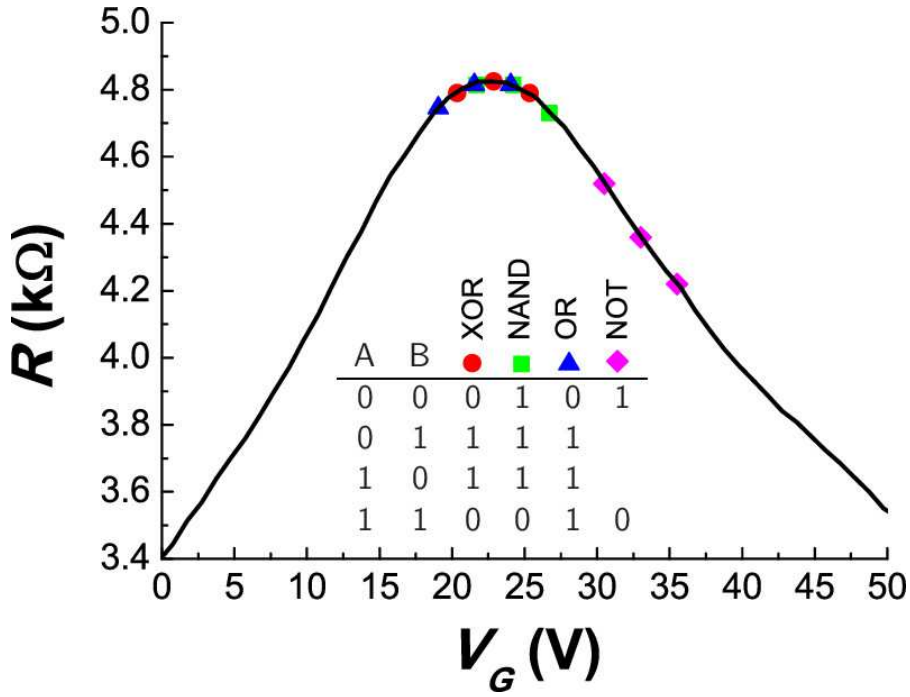


Figure 5.17: The figure illustrating the choice of the input voltage with respect to the Dirac point for various types of circuit. Inset: the truth table for various circuit. This figure is reused from ref [236]. Copyright © AIP Publishing.

various logic circuit. Moreover, the same arrangement can work as various logic circuits, depending on the selection of the voltage high and low. And a figure showing how to choose the input high and low with respect to the Dirac point for various logic circuit application has been included in Figure 5.19 [236].

5.6 Summary

In summary, this chapter presents a step-by-step fabrication and characterisation of various flexible electronic components. Specifically, the use of PI film as a substrate for flexible electronic devices and circuits is a common strategy in the research community. This chapter follows this methodology and presents the process flow in detail. Such detailed study can benefit the new researchers who would like to step into this field. Moreover, this chapter also explores the realisation of capacitors on flexible substrate. The as-realised capacitor can work reliably under various bending conditions. This lays the foundation for the future realisation of various functional flexible devices and circuits. Based on these results and the strategy developed in Chapter 4, FETs, sensors and circuits have been demonstrated. All show stable performance under the mechanical bending test. Compared to other works, the work presented in this chapter "partially printed". And some of the figure of merits from these devices (for example, the contact resistance from GFETs) are comparable to the state of the art. It is believed

that these work could benefit the future development of all printed, high-performance flexible electronics.

6. Chapter 6: 3D integration in printed electronics

As have been discussed in Chapters 1 and 2, 3D integration is a universal strategy to increase the device density as well as lowering the power consumption, for both printed and non-printed electronics. This chapter discusses the 3D integration of printed electronics and is arranged as follows: Section 6.1 discusses the technical problems in 3D integration, which includes the isolation material's deposition, vias opening, and interconnects realisation. Afterwards, the strategies to realise 3D integrated circuits based on printed nanomaterials have been discussed (Sections 6.2 and 6.3). The circuit diagram, the layout, and the characterisation of individual devices on different layers have been presented. Finally, the function of the circuits is briefly discussed but not tested, which will be realised in future work.

6.1 Technical challenges in 3D integration process

In this section, the general strategies for 3D integration have been discussed, including the separation layer deposition, vias opening and interconnect realisation. NWs have been printed on each layer to realise resistors and sensors. Various characterisations, including Optical Microscopy, AFM and SEM, have been used to characterise the developed 3D integrated electronics.

6.1.1 Separation layer and planarisation problem

It is common that microfabrication process would lead to an uneven surface, which poses problems in the realisation of 3D integration. For example, lithography has been suggested to be preferentially realised on a planar substrate. On a non-flat surface, its reliability would be a

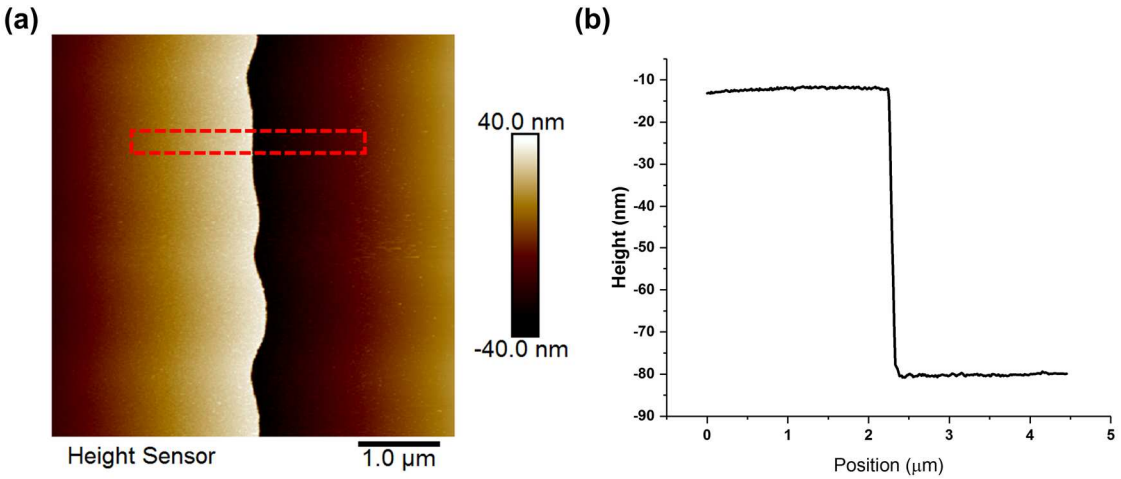


Figure 6.1: The characterisation of a step feature (a) The AFM scan (b) The line profile.

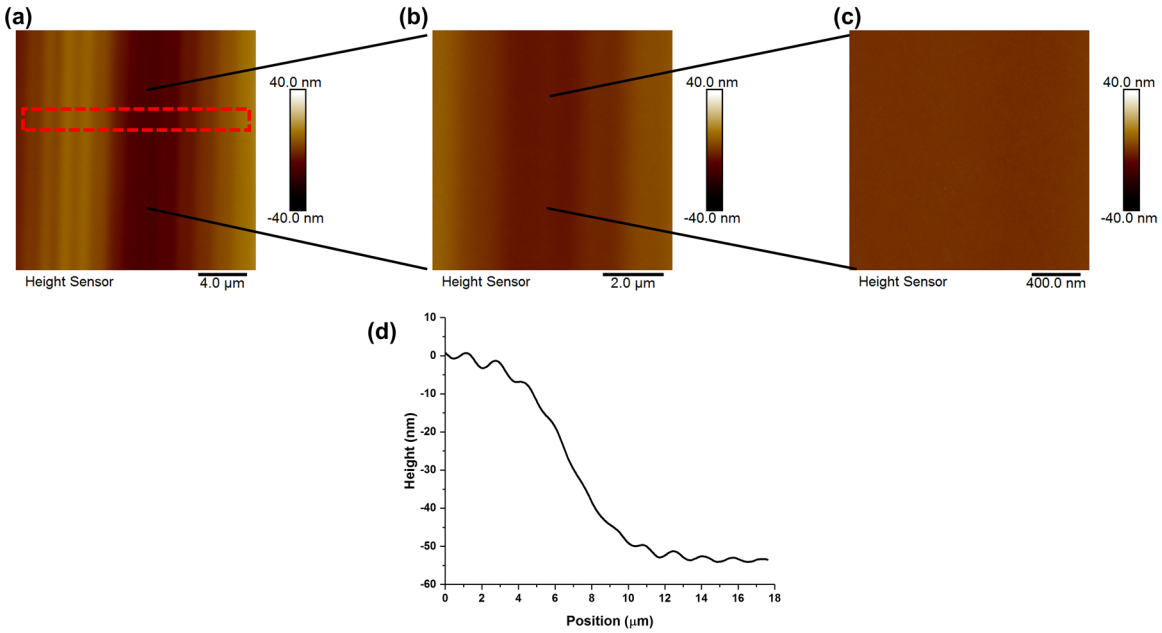


Figure 6.2: The characterisation of the step feature after flattening. (a), (b) and (c) The AFM characterisations of the metal film after spin-coated with PI solution at 4000 rpm for twice. (d) The line profile of the structure.

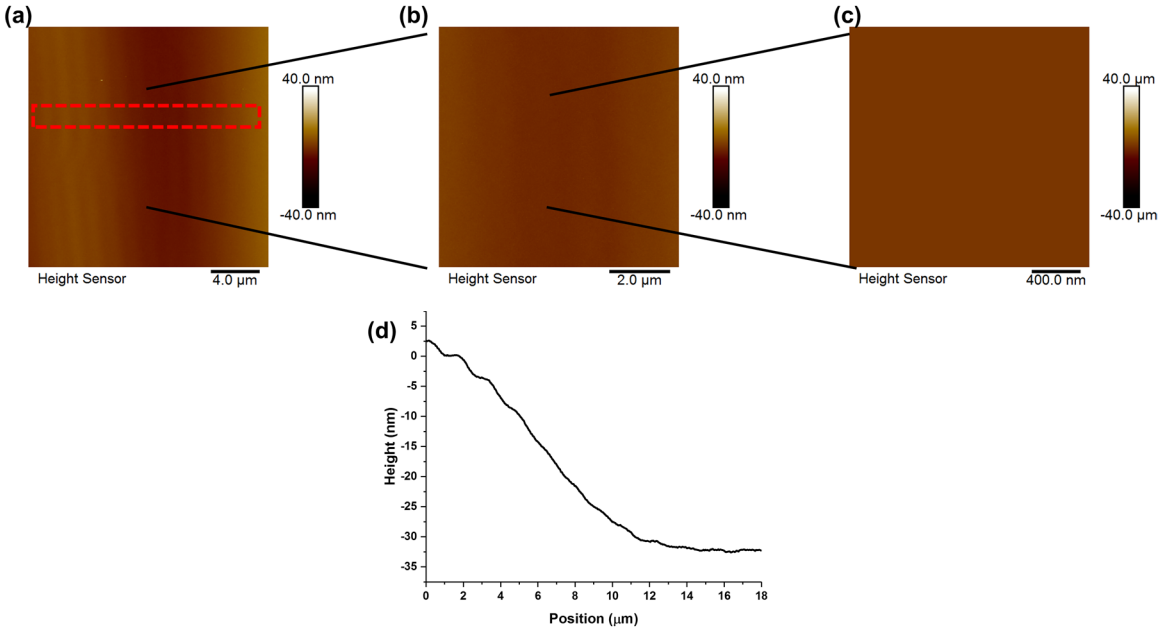


Figure 6.3: The characterisation of the step feature after flattening. (a), (b) and (c) The AFM characterisations of the metal film after spin-coated with PI solution at 4000 rpm for four times. (d) The line profile of the structure.

concern [237]. In this regard, surface planarisation is an important aspect in 3D integration and this subsection mainly discusses the problems related to interlayer deposition and the subsequent planarisation problem.

Previous studies presented in Chapter 3 have indicated that PI can lead a flattened surface. Moreover, NW can be printed uniformly on such samples. Considering this, the PI film (with a 100 nm Si_3N_4) is used to isolate the as-fabricated devices as well as to planarise the surface. Here, in order to evaluate the surface change before and after the PI spin-coating process, three samples, named Sample A, B and C, have been prepared with the same features on top. The feature height is~70 nm as confirmed by AFM. PI solution was spin-coated on Sample B and C at 4000 rpm for 60 s. The spin-coating process was repeated for twice and four times for Sample B and C, respectively. For sample A, no PI was coated on top. Afterwards, AFM has been used to characterise the three samples.

The AFM image of the Sample A, as well as a line profile scan, have each been shown in Figure 6.1, with them both indicating a high and sharp step.

With regard to the Sample B, it was subjected to a PI coating process for twice. And the feature step was smoothened with a gradual change in height over a large scale (~20 µm), as shown in Figure 6.2. And Locally, the surface after spin-coating is rather flat, as can be seen from the zoomed in AFM image. The planarisation can be further improved by increasing the spin-coating cycle as shown in Figure 6.3. In general, the spin-coated PI film can serve as an isolation as well as a planarisation layer. The planarisation effect can then be controlled by the number of spin-coating cycles.

However, it should be noted that a pure PI layer is not suitable for the realisation of further devices on top due to a deformation and shrinking problem when immersing in acetone for a long time (data not shown, similar to the scenario discussed in Chapter 5). In order to solve this issue, a 100 nm Si_3N_4 layer was deposited on top of the PI film. By doing this, the fabrication of new devices on top can be successfully carried out.

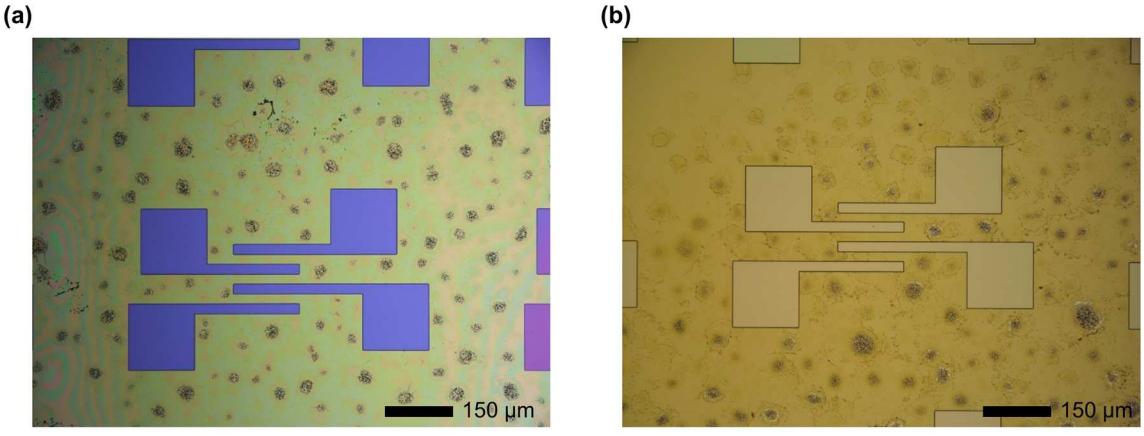


Figure 6.4: The optical microscope images of the fully cured PI films after a dry etching. The film was spin-coated at 4000 rpm for 60s for once (a) and twice (b), respectively.

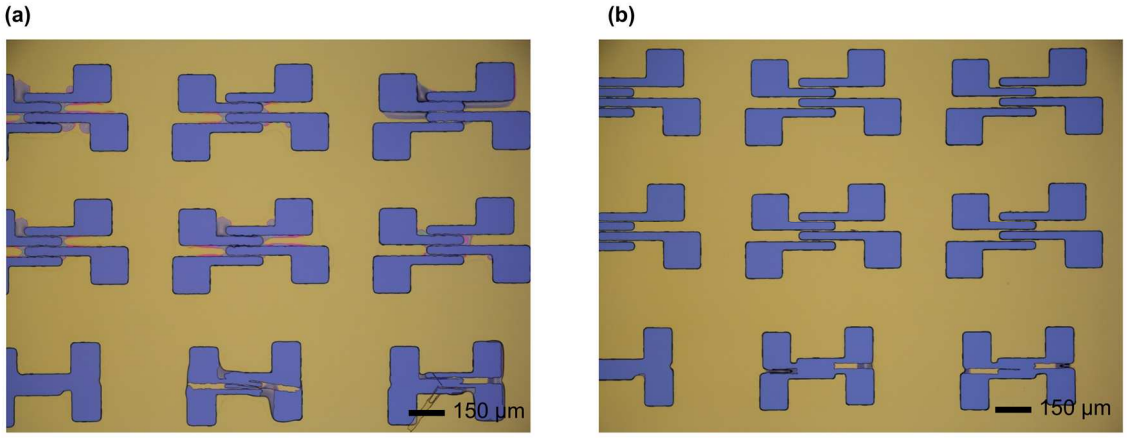


Figure 6.5: The optical microscope images of the soft-cured PI film after a wet etching process. The PI film was soft cured at 140 °C for (a) 2.5 mins and (b) 5 mins, respectively.

6.1.2 Vias opening

The last subsection discussed the using of the PI/Si_3N_4 stack as the isolation layer for 3D integration. In order to get access to the electronic devices underneath the isolation materials, vias needs to be created selectively. Here, in this subsection, the methods for etching PI and Si_3N_4 are discussed, respectively, which are later used in the development of 3D integrated electronics. It should be noted that the vias opening process described in this subsection is quite different from the standard CMOS technology, where TSV is adopted in order to create deep Si vias for 3D integration [238]. For this work, since most of the separation material is PI, the etching process in this regard is not as critical and complex as the case of Si.

The PI film can be patterned by dry and wet etch methods. For dry etch, the PI film was fully cured by following the method described in Chapter 5. After a conventional photolithography and development process, the film was etched by using RIE with a gas flow of 5 sccm CF_4 and 95 sccm O_2. Two samples spin-coated with one layer and two layers of PI have been prepared for this study. Each layer of PI was spin-coated at 4000 rpm for 60s. As can be seen from Figure 6.4, the first layer of PI has been completely removed in the 10 mins' etching process, while the sample spin-coated with double layer PI shows an incomplete etching. We can also check the film thickness to estimate the etching rate, which is calculated to be around 1.8 µm/10mins.

The PI film can also be patterned by using a wet etching method. For this, the PI film cannot be totally cured until the etching process has been completed and the photoresist has been removed. Also, the soft baking process is critical to the wet-etching process. To study this, two conditions have been tried. The PI film was soft baked at 140°C for 2.5 minutes and 5 minutes, respectively. A treatment of MF-319 for 2.5 minutes was used to etch the film. The results are

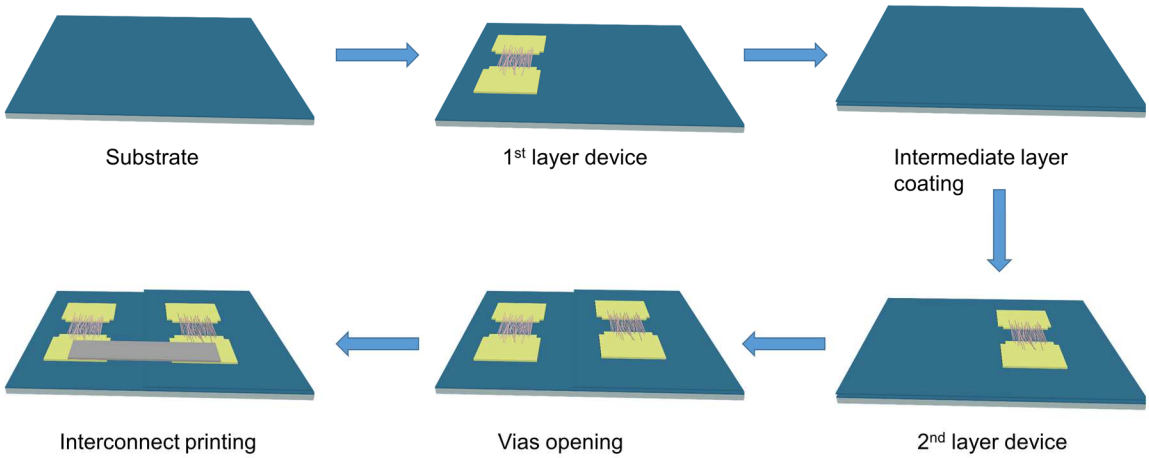


Figure 6.6: The schema showing the process flow of 3D integrated devices.

presented in Figure 6.5. For both conditions, the film can be completely etched. By increasing the soft-baking duration, the definition of the etched pattern is better. But still the resolution is not comparably to the pattern defined by dry etching methods (Figure 6.4). Therefore, the dry etching process has been adopted for the later development of 3D integration.

It should be noted that, some damage can be seen on the PI film after the dry etching process as shown in Figure 6.4. This is attributed to the complete removal of the photoresist protection layer. Such a problem can be avoided by adopting a photoresist layer with higher thickness, which can be seen in later results.

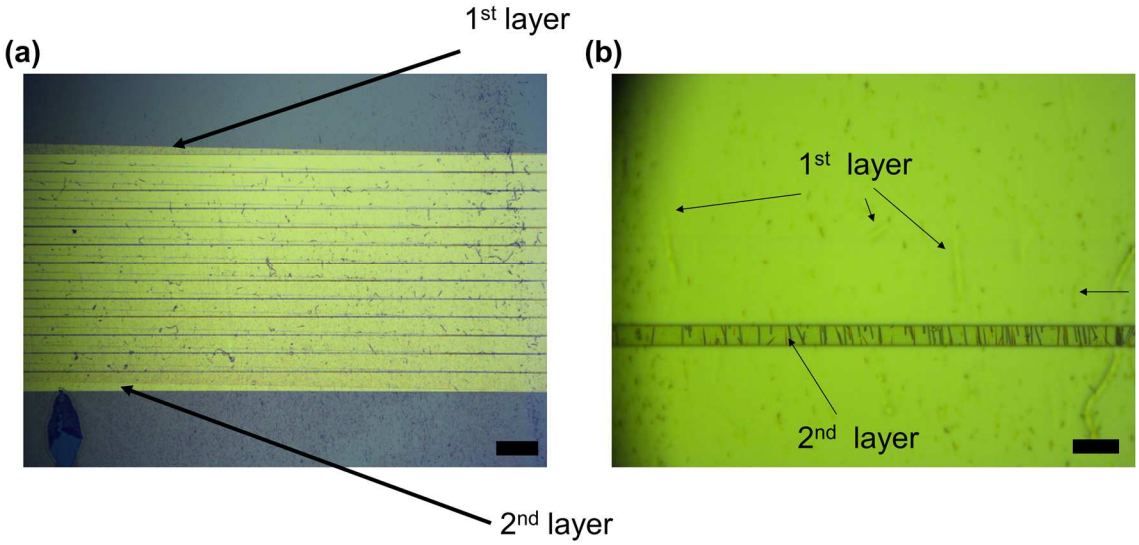


Figure 6.7: The optical microscope images of the as-fabricated 3D integrated devices. The scale bar in (a) and (b) are, 50 µm and 5 µm, respectively. Copyright © 2019 IEEE. Reprinted, with permission, from [164].

Meanwhile, the Si_3N_4 film can be etched by RIE using the same recipe as used for the SiO_2 etch (see Chapter 4). The etching velocity and outcome in the two scenarios are almost the same and therefore will not be discussed in detail within this subsection.

6.1.3 Interconnects realisation

In this subsection, the technical problems associated with the interconnects realisation to wire the devices from both layers have been discussed. In order to clarify this problem more clearly, the ZnO NW based devices were fabricated in a layer by layer printing manner. However, the performance of these devices will only be discussed in later sections since this section focuses on the technical problems towards 3D integration.

The realisation of the 3D integration is schematically illustrated in Figure 6.6. It starts with Si/SiO_2 substrate. The ZnO NWs were prepared by CVT methods and printed by a contact printing approach as previously discussed (see Chapter 3). After printing, the metal contacts were defined by photolithography, metallisation and a standard lift-off process. The processed samples were then spin-coated with PI and deposited with a 100 nm thick Si_3N_4 for device isolation (see Subsection 6.1.1). The as-deposited materials planarised the surface and acted as

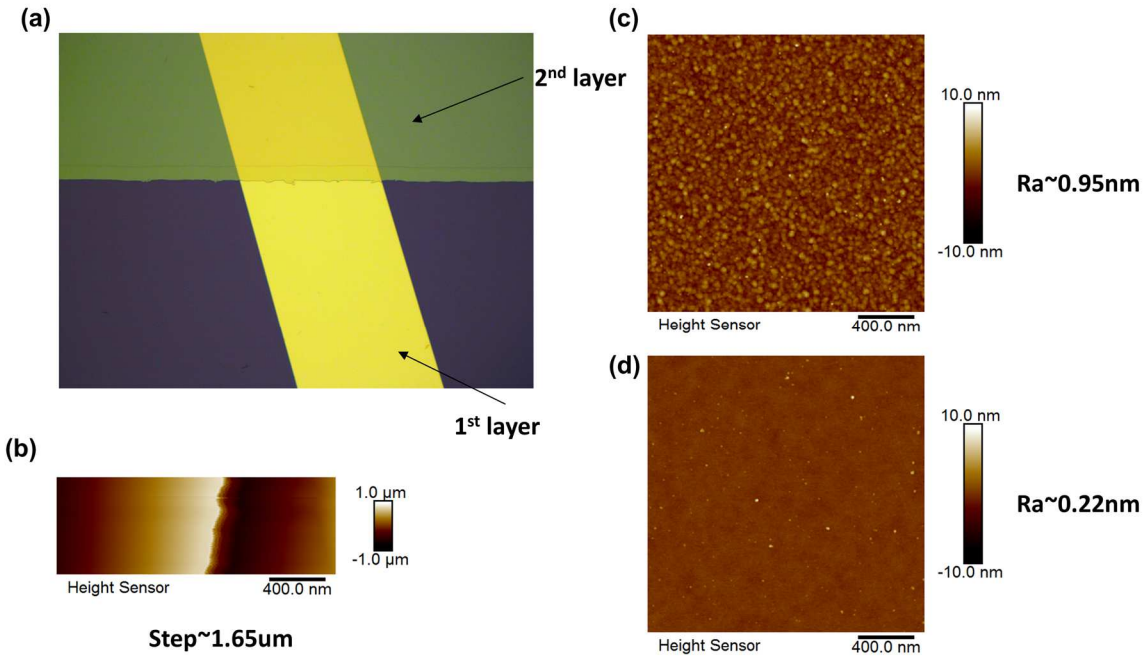


Figure 6.8: The via opening process.(a) The optical microscope image showing the interface between 1st and 2nd layers. (b) The AFM characterisation of the step height between 1st and 2nd layers. (c) and (d) The AFM characterisation of the surface from 2nd and 1st layers.

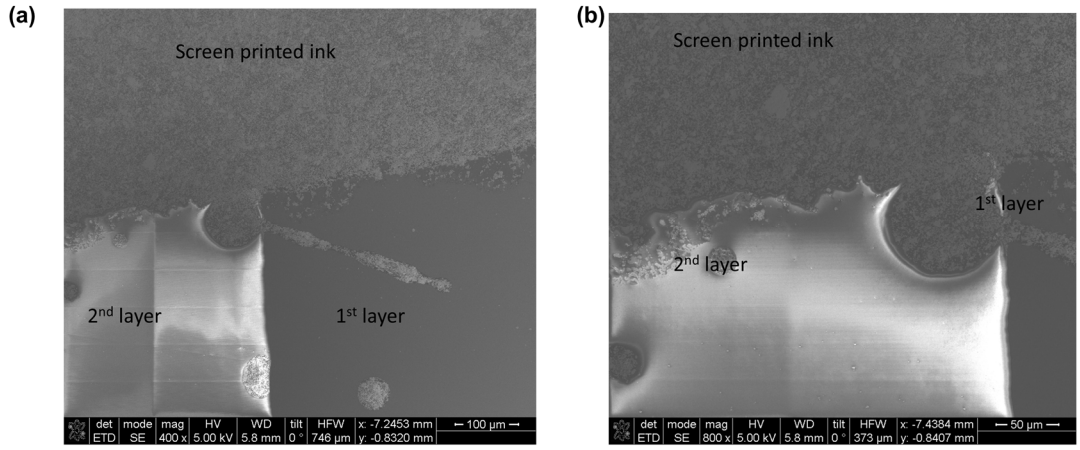


Figure 6.9: SEM characterisation of the screen printed Ag ink at the interface from the 1st and 2nd layers.

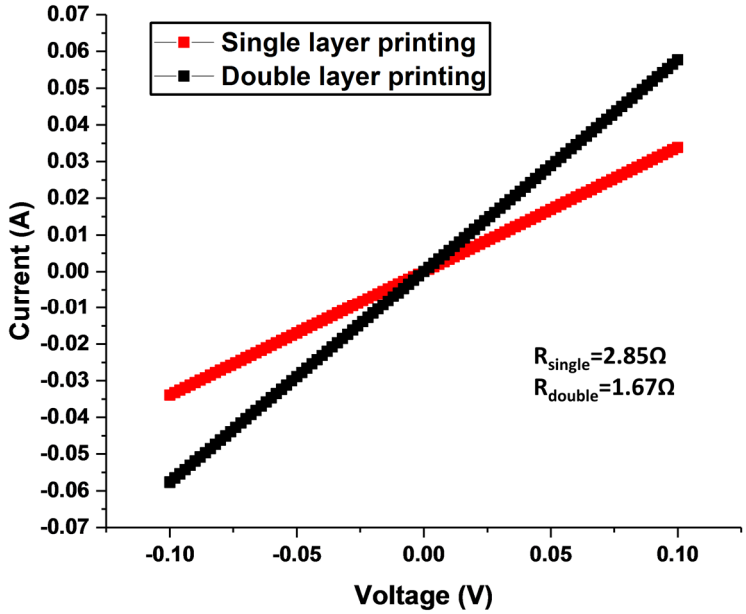


Figure 6.10: I-V characteristics of the screen-printed Ag paste.

the substrate for the realisation of a new layer of devices. Similar approaches including NW printing, photolithography, metallisation and the lift-off process have been employed again in order to realise the devices on the second layer. After fabrication, the vias were opened by the methods described in Subsection 6.1.2 and interconnects were realised by the screen printing method described in Section 3.3. Characterisations, including optical microscope, AFM, and SEMs have been used to study the realised 3D devices. As can be seen from Figure 6.7, the 3D stacked NWs based devices have been successfully fabricated. The surface roughness of the first and the second layers are ~0.22 nm and ~0.95 nm, respectively (Figure 6.8 c and d), which

is consistent with previous values. The height difference between the two layers is ~1.65 µm, as characterised by AFM (Figure 6.8 a and b).

In order to bridge the devices from both layers, Ag paste has been printed by using screen printing method as discussed in Section 3.3. The as-printed paste has been characterised by SEM. As can be seen in the Figure 6.9, no discontinuity has been observed, especially at the step region. This is because the thickness of the Ag film (~4.5 µm per layer) is several times larger than the step height (~1.65 µm). Electrical measurement has also been performed to characterise the resistance of the printed interconnect: both the single layer and double layer printing leads to a resistance lower than 5 Ω (Figure 6.10).

In summary, this section demonstrates the applicability of the screen printed Ag paste for the realisation of interconnects in the 3D integration system.

6.2 3D integrated Wheatstone bridge based on Si and ZnO NWs

The last section discusses the technical problems in realising 3D integrated electronic devices. In this section, such a strategy has been adopted to integrate the Si NW based resistors and ZnO

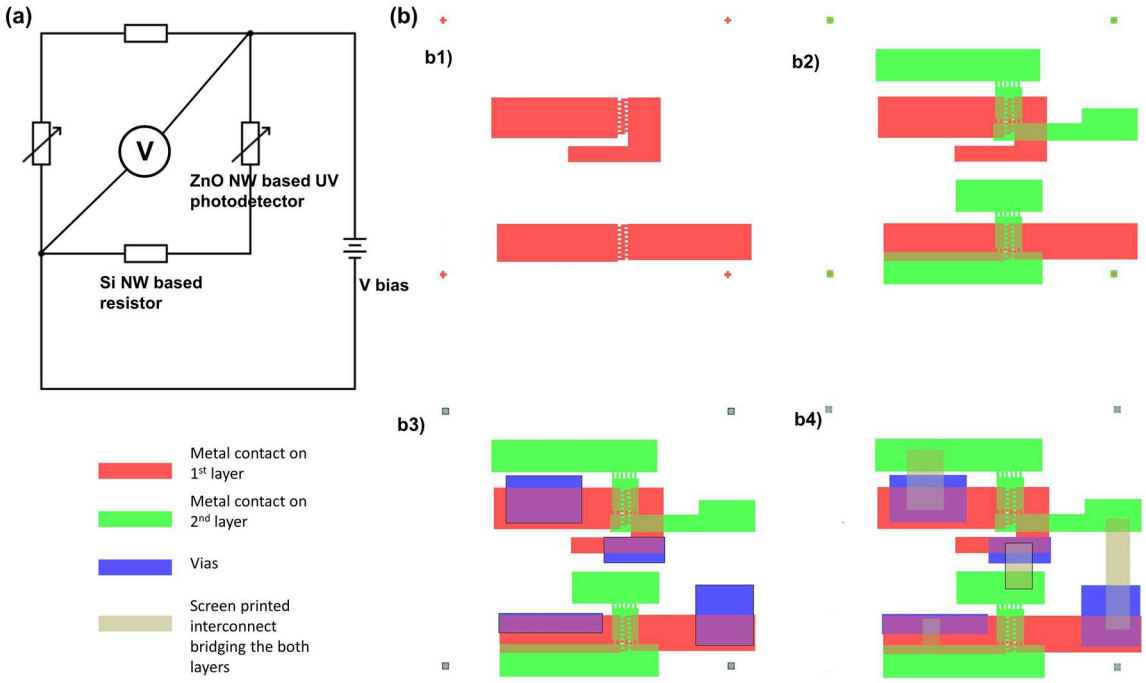


Figure 6.11: The circuit diagram and layout of a 3D integrated Wheatstone bridge. (a) The circuit diagram of the Wheatstone bridge. (b) The layout for the 3D integrated Wheatstone bridge. b1) The mask for metal contacts on the first layer; b2) The mask for metal contacts on the first and second layer; b3) The mask showing the via opening process after the fabrication of both layers; b4) The mask showing the location of the screen printed silver ink, aiming to connect the devices on both layers.

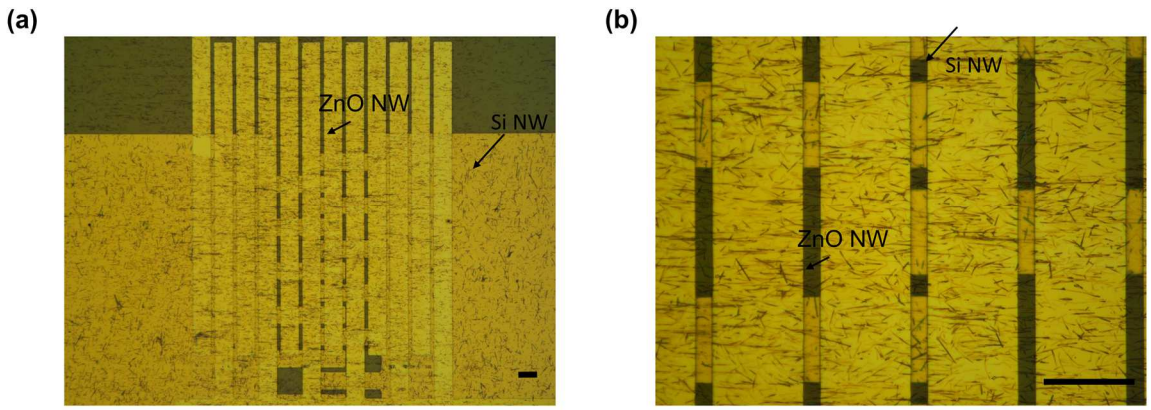


Figure 6.12: The optical microscopy images showing the as-fabricated 3D integrated Wheatstone bridge. The scale bars in both images are 30 µm.

NW based UV photodetectors in a 3D manner, aiming to realise a 3D Wheatstone bridge circuit.

The circuit diagram and the layout of the Wheatstone bridge are shown in Figure 6.11. The Wheatstone bridge consists of two voltage dividers (or two arms). Each arm consists of one Si NW based resistor and one ZnO NW based UV photodetector, as shown in Figure 6.11 a. This arrangement, compared to the single voltage divider, can lead to a higher sensitivity. Here, a layer by layer printing method has adopted for the 3D Wheatstone bridge fabrication (see Figure 6.11 b for the step by step fabrication layout). Briefly, the Si NWs were printed on the initial substrate (Si/SiO_2 substrate or a PI film on a carrier wafer), followed by a standard photolithography, metallisation and lift-off process to define the source and drain contacts

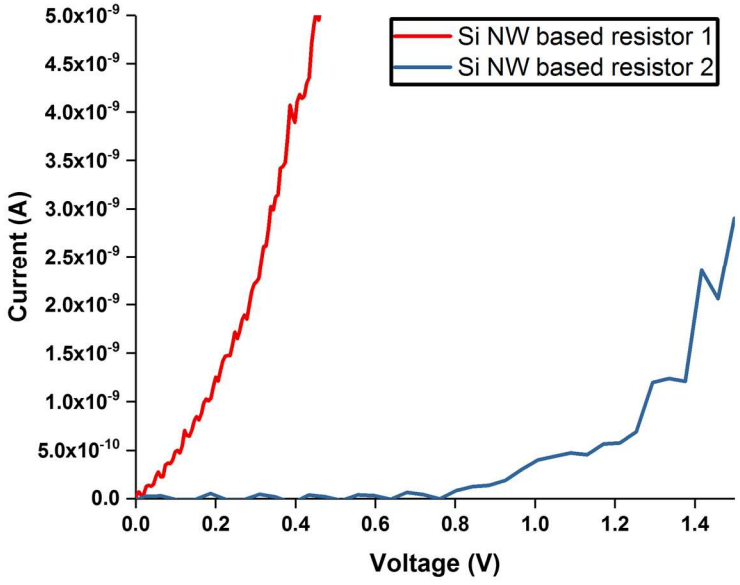


Figure 6.13: The I-V characteristics of the Si NW based resistors.

(Figure 6.11 b1). Afterwards, a separation was realised by using the methods discussed in section 6.1. This separation layer smoothens the surface and serves as the substrate for the device fabrication on the second layer. Similarly, for the devices on the second layer, NW printing, metallisation and the lift-off process were employed again to realise the UV photodetector based on ZnO NWs (Figure 6.11 b2). Vias were created on the separation layer in order to access the devices buried underneath (Figure 6.11 b3). Finally, silver paste based interconnects should be printed by screen printing to connect the devices on both layers in a configuration of the Wheatstone bridge circuit (Figure 6.11 b4).

Optical microscopy images have been taken for the as-fabricated sample, as shown in Figure 6.12. Si NWs were printed vertically on the first layer while the horizontally distributed NWs were ZnO NWs. Electrical characteristics have been obtained from the devices from both layers, as shown in Figures 6.13 and 6.14, which demonstrates the successful 3D integration of ZnO NW based devices on top of Si NWs. It should be noted that the I-V curves shown in Figure 6.13 is non-linear, which indicates a non-ohmic contact. This is because the doping of the NW, especially in the contact region, is not controlled. Moreover, the resistance of the two resistors show a large mismatch. However, such mismatch does not affect the working of the Wheatstone bridge since a calibration step can eliminate such difference. Actually, the purpose of the Wheatstone bridge is to integrate two arms of voltage dividers in the opposite manner, which could lead to double sensitivity compared to the single voltage divider. Further steps

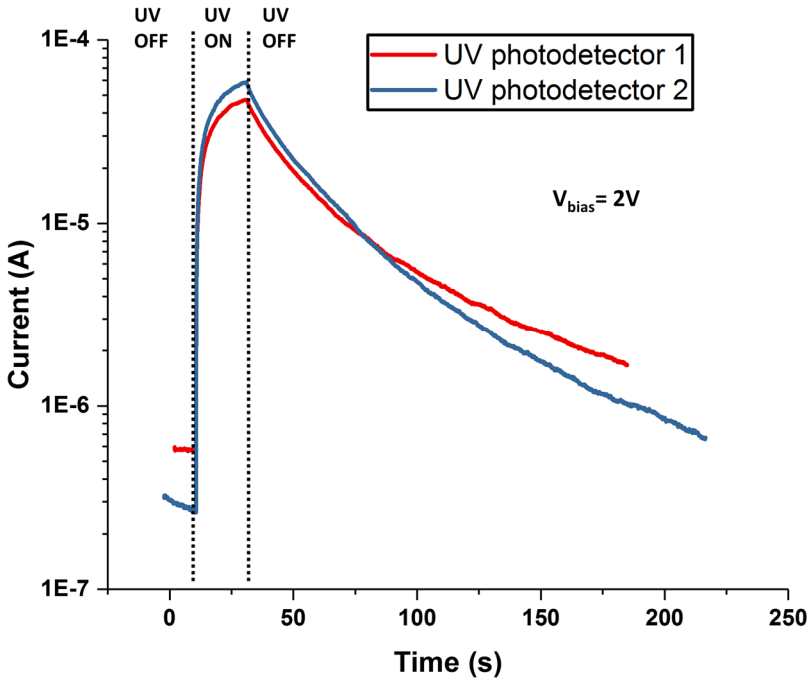


Figure 6.14: The I-t relationship of the photodetector under various conditions.

include using screen printed Ag ink to bridge the devices on both layers, and testing its response under UV illumination. Limited by time, this part of work will be carried out in the future.

6.3 3D integrated FETs and sensors for large-area active matrix application

This section presents the fabrication process and characterisation results of the two-layer electronic system: the first layer is composed of ZnO NW based FETs and the second layer composed of ZnO NW based UV photodetectors. Vias have been opened to enable the access to the devices fabricated on the first layer. Strategies on how to connect the sensors and FETs, which lead to a 1T1S structure, have been discussed. The implementation of the 1T1S structure will be carried out in future work.

The circuit diagram for the 1T1S structure has been shown in Figure 6.15 a. The drain terminal of the transistor is connected to a constant voltage bias while the source terminal is connected to a UV sensor. The transistor can be operated like a switch by changing the gate voltage bias with respect to the threshold voltage. When the gate voltage is lower than the threshold voltage,

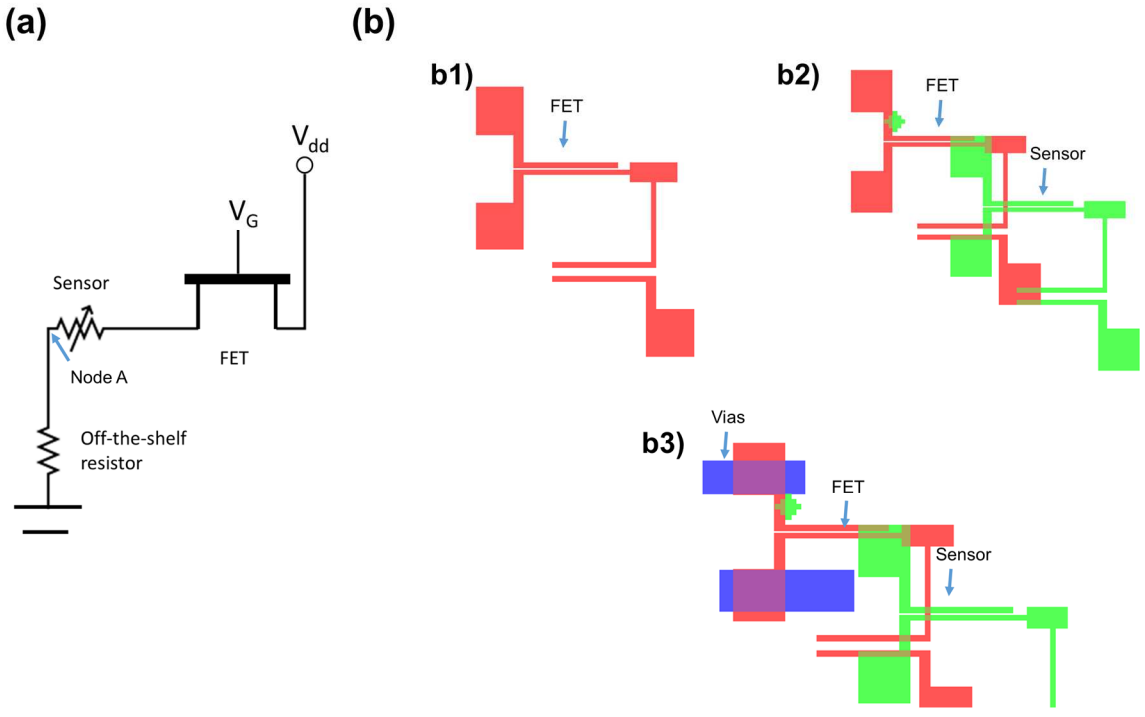


Figure 6.15: The circuit diagram and layout of a 3D integrated 1T1S struture. (a) The circuit diagram of the 1T1S structure. (b) The layout for the 3D integrated transistors and sensors. b1) The mask for the source and drain contact for ZnO NW based transistors on the first layer; b2) The mask for the metal contacts for the UV photodetector on the second layer; b3) The mask showing the via opening process after the fabrication of both layers. The mask has been repurposed.

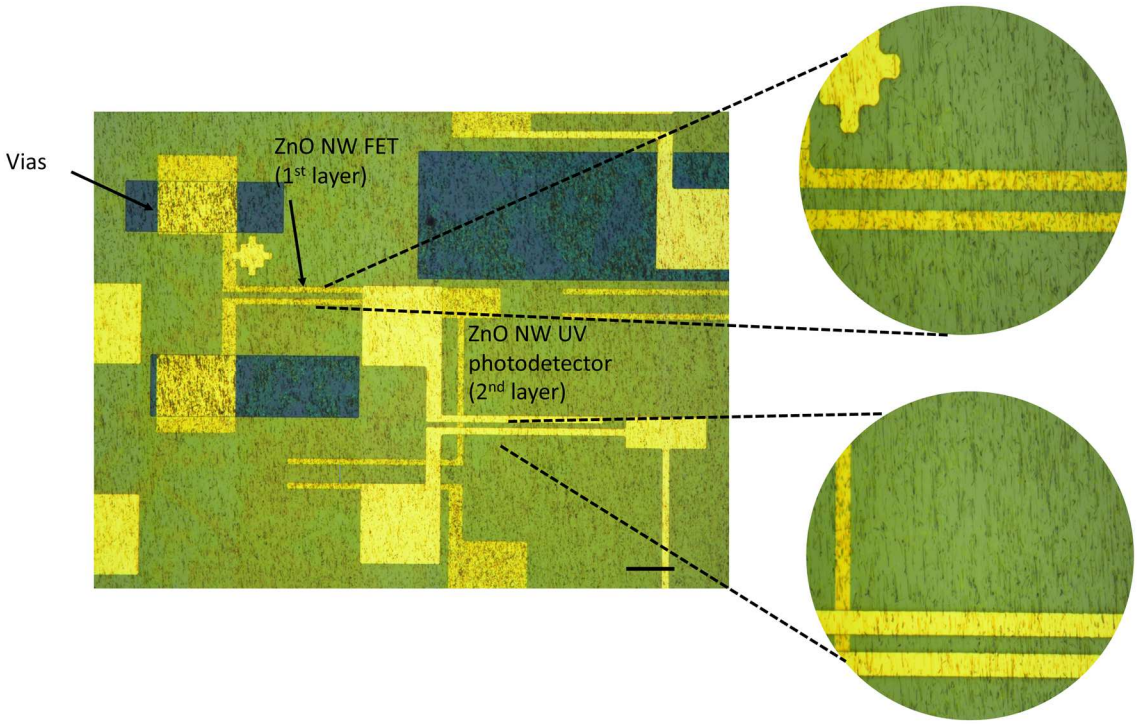


Figure 6.16: Optical microscopy image showing the 3D integration of UV photodetectors on FETs.

the transistor is in the OFF state and the entire circuit is open loop; the output of the node A is zero. When the gate voltage is higher than the threshold voltage, the transistor is on; the output of the node A is $V_{dd} \times \frac{R_{sensor}}{R_0+R_{sensor}+R_{FET}}$. Here, R_0, R_{sensor} and R_{FET} represent the resistance of the off-the-shelf resistor, the sensor and the FET, respectively. In this way, by operating the gate voltage of the FET, the sensors can be selected and dis-selected. The 1T1S structure presented here is the basic building block towards an active matrix sensor arrays, which can be used for various wearable applications.

Here, a step by step fabrication layout of the 3D integrated 1T1S structure has been illustrated in Figure 6.15b. A similar layer by layer printing method, as has been discussed previously, has been used to realise the 3D integrated 1T1S structure: The ZnO NWs were printed on Si substrate with a 300 nm SiO_2 as the dielectric layer. After printing, source and drain contacts (3 nm Nicr/70 nm Au) were realised by electron-beam evaporation. The as-realised device utilised the entire Si substrate as the gate terminal (bottom gate device), and its transfer and output characteristics will be discussed later in Figure 6.17. In order to fabricate another layer of devices on top of the as realised ZnO NW FET, a separation layer comprising of ~1.55 µm PI and 0.1 µm Si_3N_4 has been deposited. Afterwards, another ZnO NW printing process was again carried out, followed by photolithography, metallisation and the lift-off process to realise the ZnO NW based UV photodetector on the second layer (see Figure 6.15 b2). After that, an

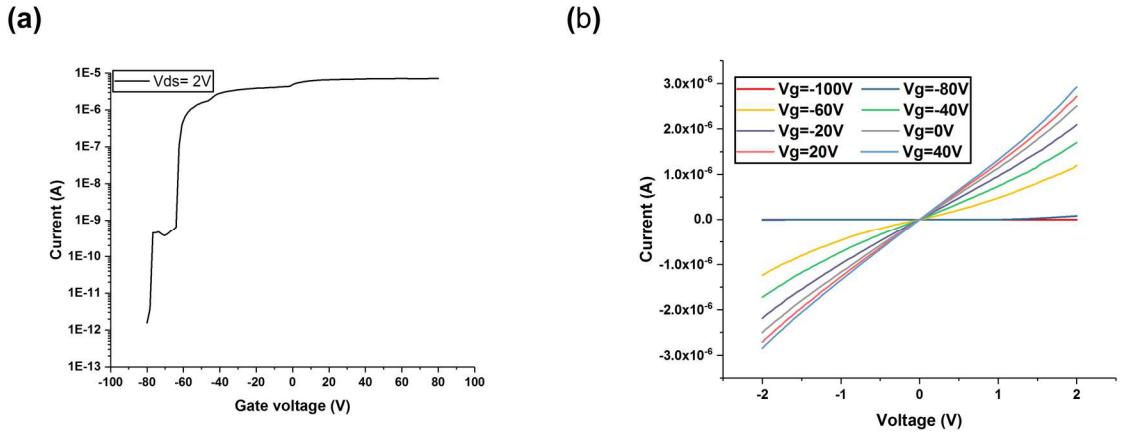


Figure 6.17: The electrical characterisations of the printed ZnO NW FET after 3D integration. The ZnO NW FET is on the first layer. (a) The transfer curve (b) The output curve.

RIE process was employed to create the vias, which enables access to the devices on the first layer (see Figure 6.15 b3). Finally, in order to realise the 1T1S structure, the devices on both layers should be connected. This can be achieved by screen printing method, as has been discussed previously in Section 6.1.3. Limited by time, this will be realised in the future.

Figure 6.16 shows the optical microscopy image of the as-realised double layer electronic system. The ZnO NW FET is on the first layer with the entire Si/SiO_2 substrate acting as the

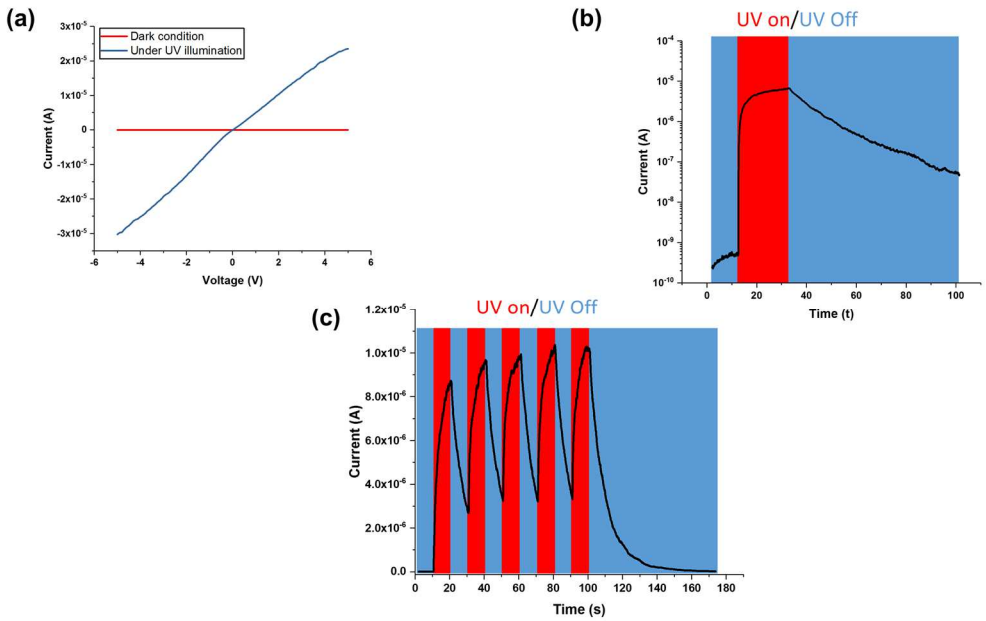


Figure 6.18: The UV electrical characterisations of the UV photodetector. (a) The I-t relationship under dark condition and UV illumination. The power density of the UV light used here is ~1 $\mu W/cm^2$. (b) The time resolved measurement showing the rise and decay of the current under UV and dark conditions. (c) The cyclic test of the sensor with and without UV illumination. The power density of the UV light used in (b) and (c) are ~0.43 $\mu W/cm^2$.

back gate. The transfer and output characteristics of the FET after realisation of the second layer has been tested and shown in Figure 6.17. As can be seen from the figure, the performance of the ZnO NW FET is similar to that has been shown in Chapter 4, which demonstrates that the strategy for realising 3D integration is compatible with FET as well.

Then we measured the ZnO NW based UV sensor on the second layer. As can be seen from Figure 6.18, the photo to dark current ratio, rise and decay time, etc, are similar to the data presented in Chapter 5. Thus, we conclude that the proposed strategy is also compatible to realise the 3D integration of sensors and FETs.

6.4 Summary

In summary, this chapter discusses the possible methodology to realise 3D integrated electronics in a layer by layer manner The proposed method is compatible with large area processing, and can potentially increase the device density, which is a fundamental limitation in printed electronics. The demonstrated device is expected to have a long longevity due to the robustness of the inorganic materials such as graphene and ZnO. Moreover, compared to other work, this chapter for the first time presents the 3D integration of Wheatstone bridge and 1T-1S structure, which can be further extended to active matrix sensor arrays. This lays a strong foundation for the future development of 3D, flexible and printable electronics.

7. Chapter 7. Conclusion and Future Perspective

This chapter concludes all the work presented in this thesis and points out the opportunities for possible future work.

7.1 Conclusion

Large-area electronics is an innovative way to make electronics, where the components are fabricated in a cheaper and faster manner. For this, printing technology has been regarded as one of the most promising methods. This thesis discusses the problems associated with printable electronics and its application within flexible and 3D integrated electronics. The major findings are summarised as follows:

(a) Contact printing is a method used to directionally print quasi-1D NWs from donor to receiver substrate. Although it has been more than a decade since its first demonstration, no systematic study has been done regarding the NW printing on flexible substrates and the substrates with uneven features on top. This thesis presents the first experimental study into this and tries to provide a qualitative explanation for the observed phenomenon.

(b) In addition to (a), a home-made contact printing setup has been realised, which enables the precise control of the entire printing process.

(c). This thesis explores the vdW contact in the system of ZnO NW as well as graphene, with Au selected as the example electrode. Regarding the ZnO NW, the vdW interaction between ZnO NW and Au leads to an inefficient contact with non-linear output characteristics. In contrast, the graphene-Au vdW contact leads to an ohmic type contact. The reason accounting for this difference has also been qualitatively explained.

(d) In addition to (c), a systematic study in graphene-Au vdW contact has been carried out for the first time. The contact resistance from vdW contacted GFET has been proven to be on a par with the best reported value from the state-of-the-art top- and edge- contacted GFETs. A model has also been developed to explain this outstanding performance. Furthermore, the graphene-Au vdW contact has also been shown to be stable under various bending conditions, which makes it an excellent alternative to top- and edge- contacted GFETs, especially in large-area flexible electronics.

(e) This thesis also studies the fabrication and characterisation of flexible devices, sensors and circuits based on ZnO NWs and graphene. These devices were achieved by combining printing technology with the standard CMOS process.

(f) Finally, 3D integrated NW based electronics have been realised by using a layer by layer printing method.

This work is believed to advance the current understanding through various aspects, especially on printable and flexible electronics.

7.2 Future perspective

It should also be noted that there are several limitations to this thesis. Possible future work, which could improve current studies, has also been indicated below:

(a) Currently, all the NW printing experiments have been carried out under a constant pressure and constant sliding speed. With the developed contact printing setup, NW printing in a more diverse manner can be realised. How the NWs will be printed in these scenarios has not been carefully studied nor clearly understood. This may open new avenues in further controlling the NW printing process. Meanwhile, the NW printing mechanics, especially regarding those non-conventional substrates, are still not very clear. Efforts need to be made in this direction as well to further understand the NW printing process.

(b) Regarding the graphene-Au vdW contact, effort has been made in using C-AFM to directionally illustrate the contact resistance under various ConH. However, this has not been successful due to significant noises caused by many extrinsic factors. This could initiate the need for a potential study to gain further understanding of graphene-Au vdW contact. Meanwhile, an attempt has also been made to develop a quantitative model to explain the detailed graphene-Au vdW contact. However, it seems to be very challenging since it together deals with macroscopical force (pressure during graphene transfer) and microscopic interaction (vdW interaction). This could potentially be a future work.

(c) Regarding the development of the 3D integrated Wheatstone bridge and 1T1S structure, interconnects have not been realised to bridge the devices from both layers due to the delay of the mask-providing company. But, technically, there are no barriers towards this, as has been shown in Chapter 3.

(d) The 1T1S structure can be further extended to sensor arrays controlled by an active matrix. How to realise this, especially on the flexible substrate, will be the final part of the future work.

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