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GaN-Based High Efficiency Transmitter for Multiple-Receiver Wireless Power Transfer

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To the Graduate Council:

I am submitting herewith a dissertation written by Ling Jiang entitled "GaN-Based High Efficiency Transmitter for Multiple-Receiver Wireless Power Transfer." I have examined the final electronic copy of this dissertation for form and content and recommend that it be accepted in partial fulfillment of the requirements for the degree of Doctor of Philosophy, with a major in Electrical Engineering.

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GaN-Based High Efficiency Transmitter for Multiple-Receiver Wireless Power Transfer

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ABSTRACT

Wireless power transfer (WPT) has attracted great attention from industry and academia due to high charging flexibility. However, the efficiency of WPT is lower and the cost is higher than the wired power transfer approaches. Efforts including converter optimization, power delivery architecture improvement, and coils have been made to increase system efficiency.

In this thesis, new power delivery architectures in the WPT of consumer electronics have been proposed to improve the overall system efficiency and increase the power density.

First, a two-stage transmitter architecture is designed for a 100 W WPT system. After comparing with other topologies, the front-end ac-dc power factor correction (PFC) rectifier employs a totem-pole rectifier. A full bridge 6.78 MHz resonant inverter is designed for the subsequent stage. An impedance matching network provides constant transmitter coil current. The experimental results verify the high efficiency, high PF, and low total harmonic distortion (THD).

Then, a single-stage transmitter is derived based on the verified two-stage structure. By integration of the PFC rectifier and full bridge inverter, two GaN FETs are saved and high efficiency is maintained. The integrated DCM operated PFC rectifier provides high PF and low THD. By adopting a control scheme, the transmitter coil current and power are regulated. A simple auxiliary circuit is employed to improve the light load efficiency. The experimental results verify the achievement of high efficiency.

A closed-loop control scheme is implemented in the single-stage transmitter to supply multiple receivers simultaneously. With a controlled constant transmitter current, the

system provides a smooth transition during dynamically load change. ZVS detection circuit is proposed to protect the transmitter from continuous hard switching operation. The control scheme is verified in the experiments.

The multiple-reciever WPT system with the single-stage transmitter is investigated. The system operating range is discussed. The method of tracking optimum system efficiency is studied. The system control scheme and control procedure, targeting at providing a wide system operating range, robust operation and capability of tracking the optimized system efficiency, are proposed. Experiment results demonstrate the WPT system operation.

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1 INTRODUCTION

1.1 Wireless power transfer

In the recent decades, due to many merits, such as high flexibility, convenience, and safety, wireless power transfer (WPT) has attracted great attention in electric vehicles (EV) and consumer electronics, such as mobile devices, monitors, household appliances, and medical implants, as shown in Fig. 1.1. Recently, efforts have also been made towards dynamically charging vehicles in driving and smart tables which enable simultaneous charging of multiple devices on a single surface.

According to the power rating, WPT systems are categorized into three levels. (1) Low power, up to 15 W, typically used to charge medical or mobile devices. (2) Medium power range up to a few hundred watts for monitors, laptop and multiple consumer electronics. (3) High power mainly for industrial automation and EV charging application.

The wireless power market total revenue is expected to reach 8.5 billion by 2018. As reported in Pike Research, the number of wireless powered products will triple by 2020 to a $ 15 billion USD market [1].

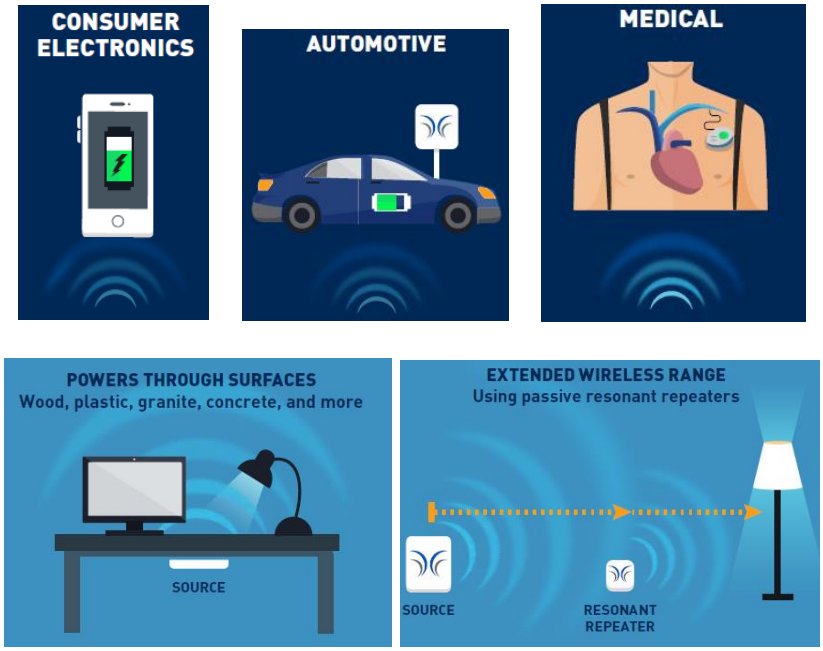


Fig. 1.1. The application of WPT [1].

1.1.1 The background of wireless power transfer

Wireless power transfer enables power transfer from source to load through an air gap, without interconnecting wires. This idea is first verified by Nikola Tesla in the 1910s through the Wardenclyffe Tower based on inductive and capacitive coupling. Even though he failed to popularize these findings at that time, this method is now widely used in near-field wireless power systems. The earliest commercial product using inductive coupling is the inductive heating at the 1971 national association of homebuilder convention in Houston, Texas. The operation frequency of this system is 25 kHz. The magnetic flux induced by the high frequency output current of transmitter generates large eddy currents in a pot, heating it [2]. One of the first commercial product based on inductive wireless charging is the electric toothbrush in the early 1990s. Normally, the toothbrush is placed in a moist environment and needs to be regularly charged. A wired charger in the moist

environment causes electric shock for the users. The development of an inductive charger for electric toothbrush can fully enclose and insulate the plugs and wires. Therefore, it improves safety.

Wireless charging technologies can be classified into near-field (non-radiative), based coupled charging, and far-field (radiative RF) charging as shown in Fig. 1.2. The near-field technique consists of inductive coupling and capacitive coupling. Inductive coupling can be further divided into the magnetic inductive coupling and magnetic resonant coupling. In capacitive coupling, the achievable amount of coupling capacitance is dependent on the surface area of devices. Since consumer electronics typically have limited size, it is hard to implement this technique [3], [4]. But it is feasible in the EV charging application. The far-field technique includes direct RF power beamforming and non-direct RF radiation. The former requires knowing the exact location of the receiver for power transfer [3].

The research in this thesis aims at consumer electronics application with inductive coupling techniques. And the following discussion refers to inductive power transfer.

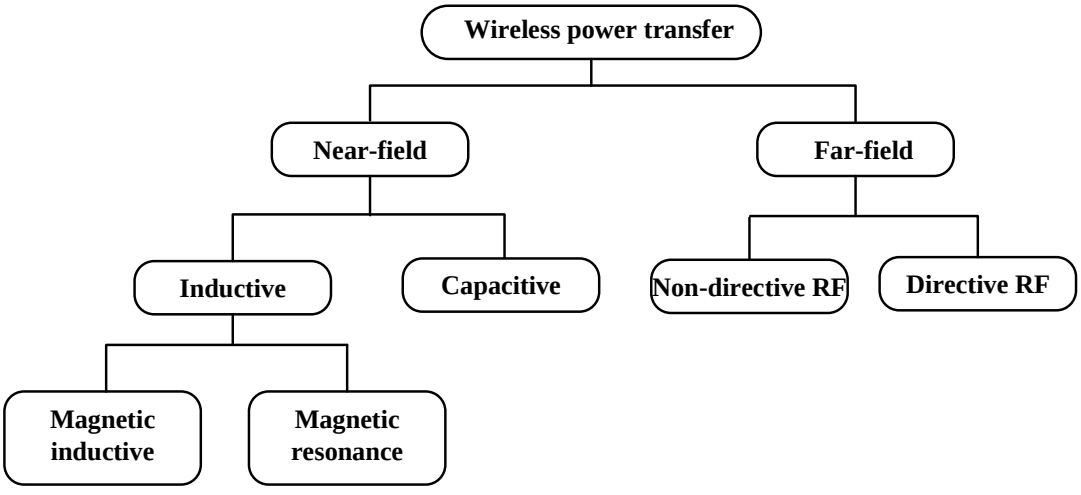


Fig. 1.2. Categories of WPT technologies.

1.1.2 Magnetic inductive coupling

Inductive power transfer works by creating an alternating magnetic field in a transmitter coil and converting that flux into an electrical current in the receiver coil. Fig. 1.3 shows inductively coupled coils. The transmitter coil is driven by high frequency ac current. Depending on the coupling coefficient, a fraction of the magnetic flux generated by the transmitter coil penetrates the receiver coil and contributes to power transmission. The amount of flux coupled to the secondary coil is proportional to the cross-section area that presents to the magnetic field. The perfect coupling which has coupling coefficient k=1 is obtained when all the flux generated by the primary coil is coupled to the secondary coil. The maximum k can be obtained when the secondary coil has identical dimensions to the primary and the two coils are placed close to each other. Since the flux drop with distance, the secondary coil has to be placed as close as possible to the primary coil.

Because of this feature, the effective charging distance of inductive coupling is typically within 20 cm [3], [6]. Charging is also sensitive to misalignment in the X and Y directions. The transmitter and receiver should use the same coil and be perfectly aligned [7] to get the most efficient power transfer system. There are three methods that are typically used to ensure perfect alignment, as shown in Fig. 1.4. The first approach in Fig. 1.4(a) is using a magnet for positioning. The second approach in Fig. 1.4(b) is moving the position of transmitter coil to the location of the detected device. The third one in Fig. 1.4(c) is to use a large number of transmitter coils, and only power the coil aligned to the receiver.

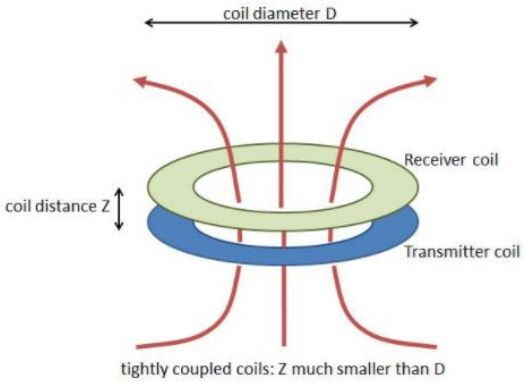
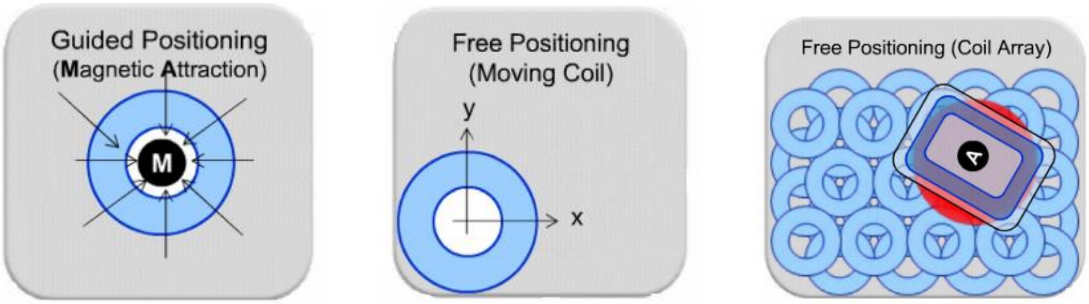


Fig. 1.3. Tightly coupled coils [5].



(a) (b) (c)

Fig. 1.4. (a) Approach 1: guide the positioning charging. (b) Approach 2: free positioning based on a mechanically moveable primary coil. (c) Approach 3: free positioning based on the selective excitation of a coil array [8].

1.1.3 Magnetic resonant coupling

Magnetic resonant coupling was first introduced by the research group at Massachusetts Institute of Technology (MIT) in 2007 [9]. The basic idea of resonant coupling is that the two resonant coils are tuned at the same frequency. The magnetic resonant coupling typically operates at megahertz frequency, and the quality factors of coils are high, facilitating low power loss in coils. High *Q* coils can help mitigate the sharp decrease in the coupling coefficient when the distance increases [3]. As reported, extending the effective power transfer distance to meter range is possible [3]. Therefore, the resonant coupling also refers to loosely coupled technique. Fig. 1.5 shows the loosely coupled coils. There are several key capabilities of resonant coupling compared to magnetic inductive coupling due to high frequency and fully resonant features. With resonance, the charging position has higher spatial freedom in X, Y and Z directions. Devices are placed on the right, left, the top or bottom side of the charging station. Compared to the inductive coupling, the resonant coupling has a higher tolerance to the misalignment.

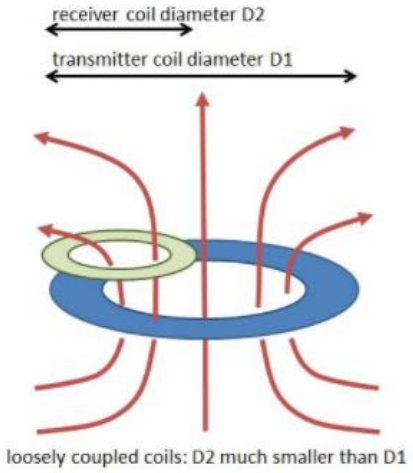


Fig. 1.5. Loosely coupled coils [5].

- The resonant coupling allows a single transmitter to charge multiple devices simultaneously. Each device, as it is put close to the charging station, can efficiently pick up the power it needs. Adding or removing one device will not impact the rest.
- Resonant coupling wireless power can be transmitted through some materials, such as wood, stone, glass, or concrete. This feature allows the transmitter to be placed under the table or embedded in the concrete wall[10].

1.1.4 The standards for WPT

There are four standards (three for consumer electronics, one for EV application) developed in the past few years.

(1) Wireless power consortium (WPC) was established in 2008 [11]. The standard set by WPC is named as "Qi." The most recent Qi specification V1.2.3 in 2017 calls for an ac frequency in the primary coil of between 87 and 205 kHz for the power range from 5 W to 30 W [7]. WPC has planned to develop classes up to 2.5 kW. The technology also includes foreign object detection (FOD) such that the charger does not expend energy heating up conductive objects that have been accidentally placed in the field [5].

(2) Power matters alliance (PMA) is another industry consortium developing WPT standards [12], for an ac frequency between 277 kHz and 357 kHz, up to 20 W. PMA has proposed solutions up to 2.4 kW for kitchen appliances [13].

(3) In 2012, the Alliance for wireless power (A4WP) developed another standard, "Rezence", for 6.78 MHz magnetic resonant coupling. A4WP is aiming at extending the charging distance and improving spatial freedom[14]. The power rating under this standard is up to 70W for the transmitter, and 50 W for a receiver according to the baseline

specification,V1.3, in 2014 [15]. In 2015, PMA and A4WP were merged into a new organization named AirFuel Alliance [16].

(4) SAE International is working on specifications for wireless charging of electric and plug-in hybrid vehicles [17]. Standard SAE J2954 for EVs announced that the low-frequency band centers at 85 kHz (range from 81.38-90 kHz) in 2013. It also defines three power levels for EVs, WPT 1 (maximum power rating is 3.7 kW), 2 (maximum power rating is 11 kW) and 3 (maximum power rating is 22 kW) [4].

Table 1.1 concludes these four standards. Generally, the inductive coupling has a lower operating frequency which makes the design for power circuits easier. Lower frequency can also help reduce the losses in the switches and inductors. The high frequency resonant coupling works at MHz frequency range, increasing the design complexity of converters. The high frequency operation also brings in the potential electromagnetic interference (EMI) challenges.

Fig. 1.6 shows the four WPT standards with respect to different coupling methods and power level.

1.2 Motivation and strategy

To further popularize the application of WPT system, significant efforts are made and will be made towards high efficiency and high power density, lowering the bill of material, improving the system robustness and enhancing the interface to provide user better experience. System integration on the converter level is an approach to increase the efficiency, reduce the system volume and component count. The implementation of simultaneously charging of multiple receivers can bring in higher spatial freedom for the users. This thesis mainly focuses on the transmitter design.

TABLE 1.1 COMPARISON OF WPT STANDARDS

Standard	SAE	WPC (Qi)	AirFuel Alliance	
			PMA	A4WP
Technology	LF-resonance	Inductive and LF-resonance	Inductive	HF-resonance
Supported by the companies	WiTricity, BWM	Apple, LG, Motorola, Sony, Samsung	Dell, EPC, Starbucks, WiTricity, Duracell, Power mat	
Members	/	433 [18]	150 [19]	
Certified products	/	1304 [18]	29 [19]	60
Power range	Up to 22 kW	5 W-30 W	0-20 W	Up to 70 W
Operation frequency	85 kHz	87-205 kHz	277-357 kHz	6.78±MHz

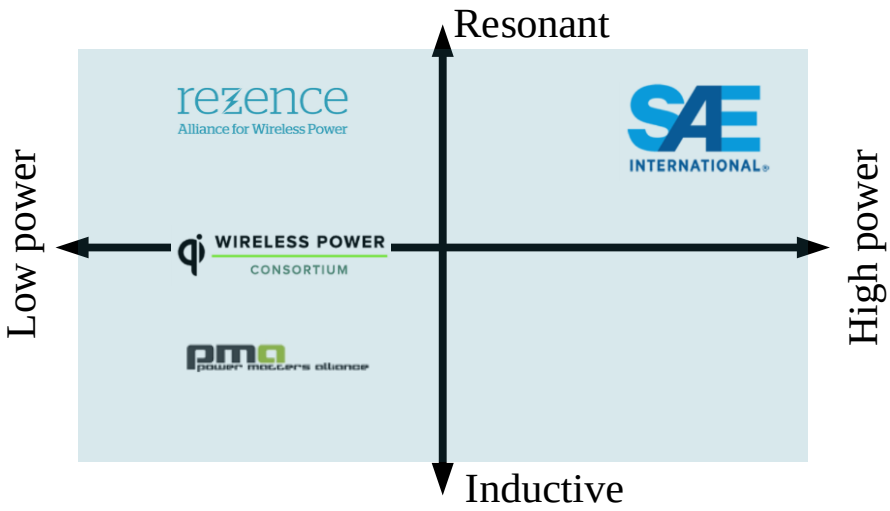


Fig. 1.6. WPT standards landscape.

1.2.1 The innovation of transmitter architecture

Multiple-stage transmitter architecture is a conventional structure, as shown in Fig. 1.7. Generally, it is comprised of a full bridge diode rectifier which converts utility frequency ac power to dc, a PFC, a dc-dc converter that processes dc voltage to the desired bus value, and a dc/ac inverter which converts the dc bus voltage to a high frequency ac current which drives the transmitter coil. This architecture has merits in the decoupling of individual converter functions. Each stage employs the best design for the specific ratings. However, it exhibits low end-to-end (dc-dc) efficiency and bulk size due to the number of cascaded conversion stages. Therefore, reducing the number of power conversion stages is one potential approach to improve system efficiency.

1.2.2 A single transmitter for multiple receivers charging application

Resonant coupling techniques allow multiple devices to be charged concurrently by a single transmitter. This achievement further improves the convenience and reduces the use of wires. In the future, the transmitter can be placed on the wall or ceiling of a room. Then all those electric devices in the room including light, mobile devices and TVs can be powered wirelessly, as shown in Fig. 1.8. In addition, when the clocks, radios, music players and remote controllers are powered up wirelessly, the batteries inside them can be removed. As reported, this can reduce 6 billion batteries disposed of each year, reduce a large source of toxic waste and groundwater contamination [20].

In this thesis, the transmitter is designed to provide the possibility for the multiple receivers concurrently charging application.

Fig. 1.9 shows the simplified schematic of the multiple charging cases, assuming no cross-coupling among the receivers.

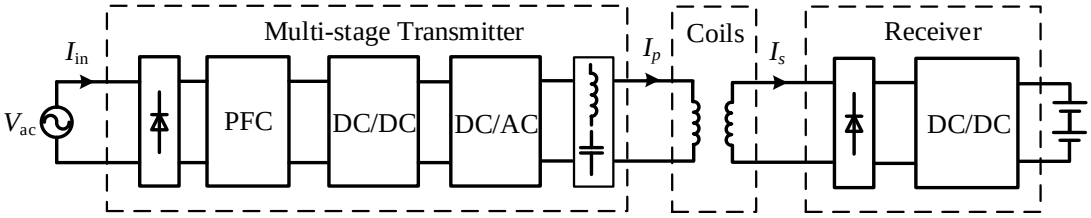


Fig. 1.7. WPT system with the multi-stage transmitter.

Fig. 1.8. Multiple devices charging application [21].

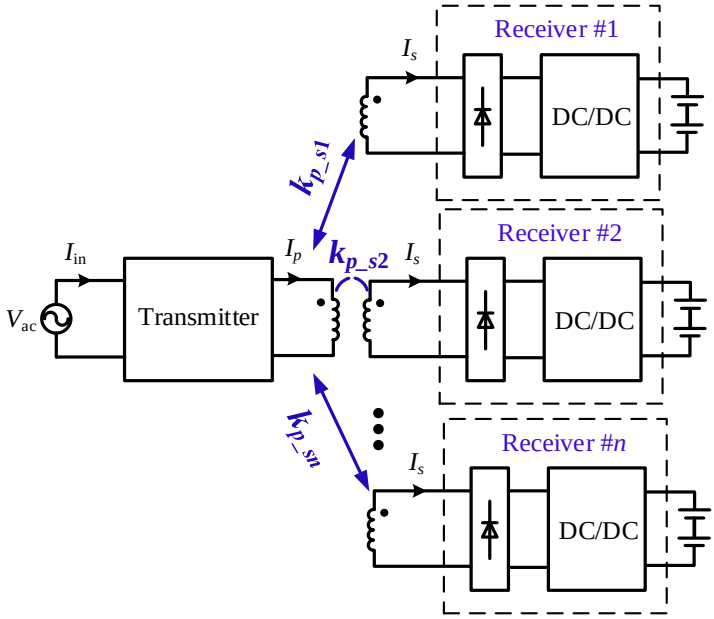


Fig. 1.9. The sketch of single transmitter charging multiple devices.

1.3 Dissertation outline

The outline of this dissertation is as follows:

Chapter 2 presents the literature review of the WPT architecture, the converter topologies, the compensation network, soft switching techniques and the control strategy in the WPT system.

Chapter 3 designs a two-stage transmitter for high PF, low THD, high efficiency and low part count. The inverter together with compensation network maintains constant current behavior for multiple receiver application.

Chapter 4 develops a single-stage transmitter for high PF, low THD, high efficiency and low part count. The control scheme is proposed to regulate the input current and output power simultaneously. An auxiliary circuit is proposed to improve the light load efficiency. The loss model is derived. The comparison among different topologies has been made.

Chapter 5 implements a closed-loop control scheme to regulate constant transmitter current at the output of the single-stage transmitter during a dynamic load change. A full power range operation is achieved by combining heavy load mode and light load mode operation.

Chapter 6 discusses a WPT system operation with the implementation of the single-stage transmitter. The system level control scheme is introduced. The capability and approach of achieving wide system operating range and optimum system efficiency are addressed.

Chapter 7 concludes this work and presents future work.

2 LITERATURE REVIEW

This chapter reviews the state-of-the-art of WPT system, in terms of architecture, impedance matching network and control strategies. This review helps to understand the opportunities and challenges for the research in the future.

2.1 WPT architecture

This section reviews the state-of-the-art WPT architecture, including the consumer electronics application, high power application, industrial products and academic work. The achievement of different topologies will be concluded. And the opportunities for improvement will be investigated.

2.1.1 The state-of-art industrial WPT products

The consumer electronics WPT system includes low power (few watts) to medium power (few hundred of watts) ranges. The front-end ac-dc rectifier usually either uses a wall adapter which converts ac to dc in a rectifier or alternatively, a dc voltage source from a battery or other dc supply in the technical products [22], [23].Therefore, most of the literature about WPT system design in this power range start from dc input. Fig. 2.1 shows an example.

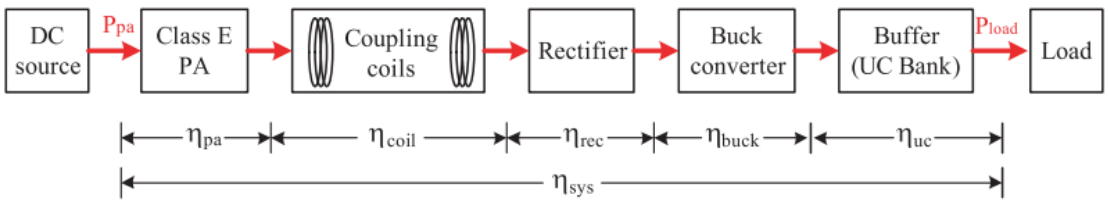


Fig. 2.1. System configuration for the commercial consumer electronics application [24].

The market of the WPT system in consumer electronics is classified into 3 categories [25]:

(1) Finished products. There are thousands of Qi and Airfuel certified products available in the market, including standalone charging pads for mobile phones, monitor, and laptops. Mophie provides a Qi-certified wireless charging pad for the iPhone [26]. There are also many WPT systems that are embedded in other systems. For example, a wireless charger embedded in a table clock or a monitor as shown in [27].

(2) Modules [25]. A branch of business focuses on the parts and modules for building a WPT system. WiTricity has WiT-5000 reference design board, 6.78 MHz, 24 W input (12V, 2A). The dc-dc (including the inverter, coils and the secondary rectifier, also refer to end-end) efficiency is 60 %. Coil to coil efficiency achieves 90%. The distance between the transmitter coil and receiver coil (Z range) is 5mm-45mm [28]. The communication of transmitter and receiver uses Bluetooth. The topology is not reported. EPC developed many transmitter boards and receiver boards. The transmitters cover 10 W-60 W power rating, while receivers include 5 W and 10 W power rating. The topologies of the transmitter are either class D or class E amplifiers. EPC 9512 is a class D amplifier [29], as shown in Fig. 2.2. The input is required to connect to a 19 V dc source. The SEPIC converter boosts bus voltage to 80 V. The efficiency of the ZVS class D amplifier is 90.6 % [30]. The development board EPC 9083 is a 60 W class E wireless transmitter and requires 40 V dc bus input [31]. The 5 W receiver develop board EPC 9513 is comprised of a diode rectifier and a subsequent SEPIC dc-dc converter which controls the output voltage to 5 V [32], as shown in Fig. 2.3. The efficiency of these development boards is not reported. Wurth worked with Texas Instruments (TI) on a WPT system reference design, as shown in

Fig. 2.4. Wurth contributes to the coil design, while TI on the circuit design with their own semiconductors and controller. A class D amplifier is used to provide high frequency ac current at the primary side. The diode rectifier and a subsequent dc-dc converter at the secondary side are for dc voltage regulation [13].

(3) Chipset. IC manufactures work actively on integrated circuits for the WPT system control applications. NXP launched NXQ1TXH5 which is a chip-based 5 W Qi-certified wireless transmitter at 2016. It utilizes a full bridge inverter and reports 85% efficiency [33]. TI launched an integrated receiver bq51011 (93% efficiency) [34] and bq5105xB (90% efficiency) [35] based on Qi V1.2 in 2012. The late one integrates a battery charger into the chip. ST promoted the STWBC-EP that complies with Qi V1.2.3 for a 15 W transmitter and STWLC33 for a 15 W receiver [36]. This receiver achieves 97% peak efficiency [37].

Industry has also developed WPT for EV applications. WiTricity claimed the DRIVE 11 evaluation system achieves a grid-to-battery peak efficiency for a 3.6-11 kW system up to 94% [38]. Evatran began to sell their Plugless L2 WPT system to the public in 2014 [4]. Now they have 7.2 kW system for TESLA model S, BMW 13, NISSAN LEAF [39].

In a summary, the front-end ac-dc rectifier is not included in the WPT design for consumer electronics application. An extra adapter is used in the standalone charger. Or the dc source is provided is WPT charger is embedded in the other systems. And dc input of resonant inverter has typically low voltage.

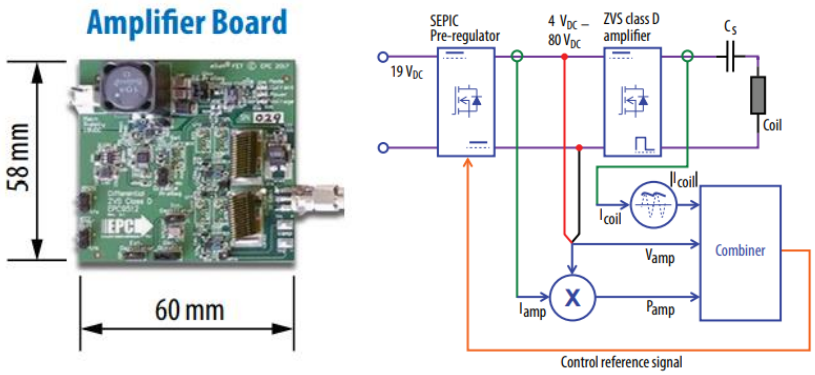


Fig. 2.2. EPC9512 amplifier board and schematic configured as 33 W Class-D amplifier [29].

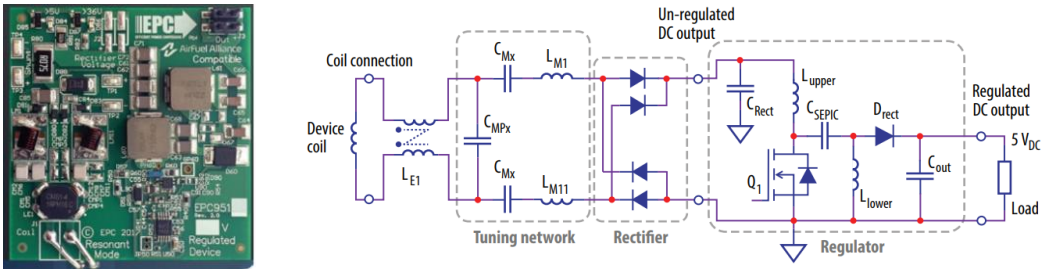


Fig. 2.3. EPC9513 rectifier board photo configured as 5 W [32].

Fig. 2.4. TI Transmitter board bq500211AEVM-210 with class D amplifier [13].

2.1.2 The state-of-art academic WPT architectures

2.1.2.1 Consumer electronics WPT system

The system architecture of the WPT system in the academic work is similar to commercial products, as shown in Fig. 2.1. The front-end ac-dc rectifier either uses a wall adapter or a dc voltage source [4], [40], [24].

Fig. 2.5 shows a common architecture for the WPT system [41]. It is comprised of a Class E inverter, coupling coils and diode full bridge rectifier. The Class E inverter is known to be a promising topology for high frequency and low power applications thanks to the simple circuit and soft switching.

Many systems are derived based on this architecture. Class E inverters can be paralleled to increase the power delivery capability. [42] uses dual class E inverters in parallel at the primary side. [43] employs six inverters in parallel to achieve a power up to 301 W. The end-to-end efficiency achieves 84.7%. The Class E^2 dc-dc converter with 6.78 MHz operation frequency is proposed in [44], [45], as shown in Fig. 2.6. It is comprised of a primary class E transmitter and a secondary class E rectifier. The measured peak end-end efficiency is 80 % at 20 W output power [45]. The Class EF^2 converter is derived by adding an LC network across the switch. It achieves lower voltage stress on the switch and lowers THD of the amplifier output current compared to Class E amplifier. The peak efficiency is reported as 71% at 29 W output power [46].

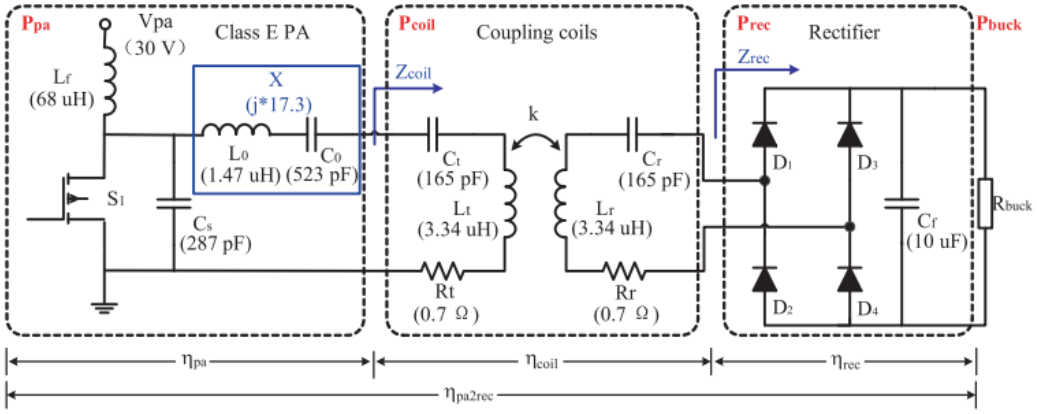


Fig. 2.5. The configuration of class E with secondary side diode rectifier for WPT application [41].

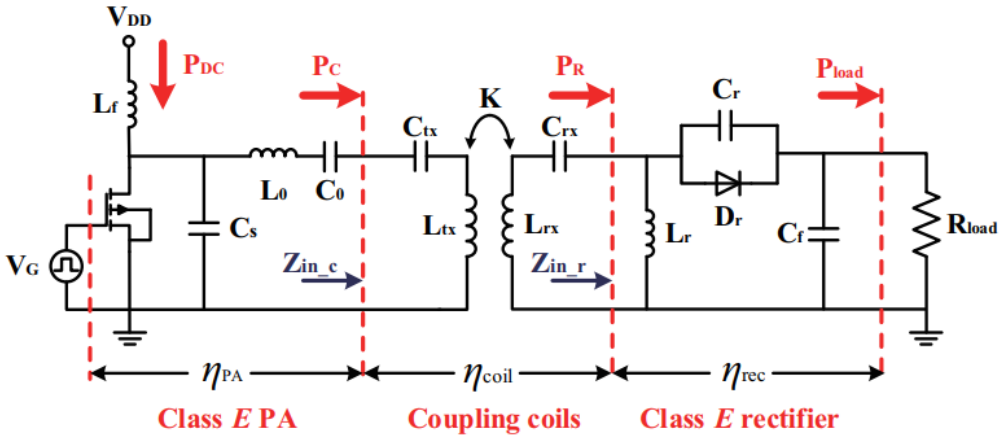


Fig. 2.6. The configuration of Class E^2 dc-dc converter for WPT application [45].

For low power applications, the Class E inverter is widely adopted due to the simple circuitry. However, since it has large voltage stress on the main device, for the medium power range application, the Class D inverter is more common [47], as shown in Fig. 2.7. More details about the class D inverter will be discussed in Section 2.2.2. In addition, a synchronous buck converter is implemented after the diode rectifier to pick up the demanded power.

The full bridge resonant inverter has a higher capability of delivering power than a half-bridge inverter. Besides, two-phase legs enable the use of phase shift modulation to adjust the output voltage. Therefore, it is also widely used [48], [49], especially in the medium-to-high power applications. Shown in Fig. 2.8, the primary side is a full bridge resonant inverter with 80 V input voltage, and the secondary side implements a diode rectifier. The reported end-end efficiency is 78% [49].

All the above-mentioned architectures are based on a dc input. To complete a whole system, an extra commercial adapter is required. Thus the system optimization is hard to achieve. A transmitter based on the line frequency ac input is proposed in [40], as shown in Fig. 2.9. The motivation of this approach is to design the front-end ac-dc rectifier and high frequency resonant inverter together, thus obtaining an optimized system design, reduced number of power conversion stage and improved system efficiency.

Table 2.1 concludes the comparison among the typical WPT architectures for consumer electronics. First, the front-end ac-dc rectifier usually is not included in the research scope. Second, significant efforts are made on the Class E inverters/rectifier at high frequency and lower power level. Third, attention starts to be given to the integrated system architectures.

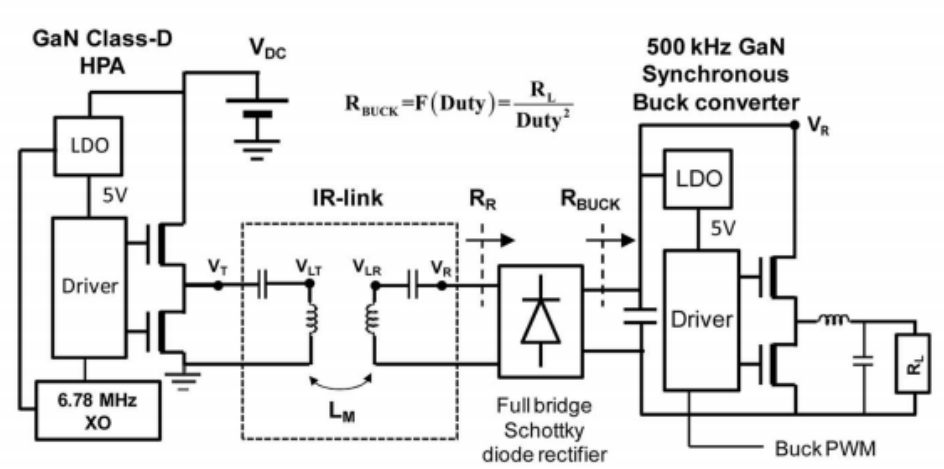


Fig. 2.7. The wireless power transfer system with class D amplifier and diode bridge rectifier [47].

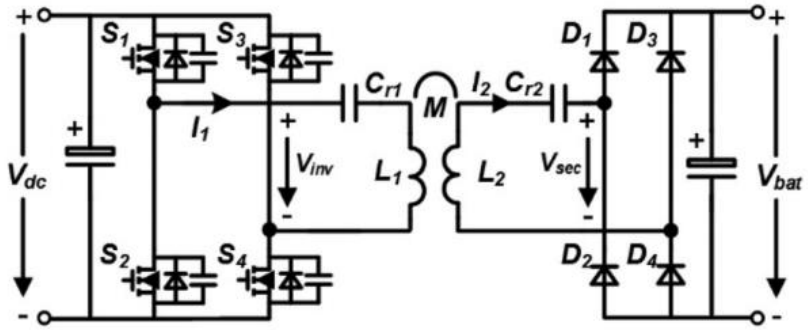


Fig. 2.8. A wireless power transfer system with full bridge inverter and diode rectifier [49].

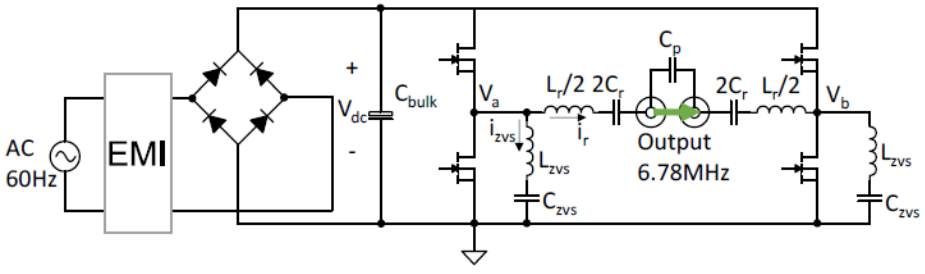


Fig. 2.9. A single-stage ac-ac transmitter is proposed for WPT system application [40].

TABLE 2.1 COMPARISON OF WPT ARCHITECTURE ON THE CONSUMER ELECTRONICS

Input	Architecture	f_o	Distance/k	P_o	η	Ref.
dc	Pri: Class E Sec: load	6 MHz	30 cm	105 W	77% dc-load	[50]
dc	Pri: Class E Sec: diode rectifier	6.78 MHz	45 mm	10 W	72.1% dc-dc	[42]
dc	Pri: Dual Class E Sec: diode rectifier	134 kHz	10 mm	295 W	75.7% dc-dc	[42]
dc	Pri: 6 Class E Sec: diode rectifier	6.78 MHz	42 mm	301 W	84.7% dc-dc	[43]
dc	Pri: Class E Sec: Class E	6.78 MHz	--	20 W	80% dc-dc	[45]
dc	Pri: Class EF2 Sec: Class EF2	6.78 MHz	--	29 W	71 % dc-dc	[46]
dc	Pri: Class D inverter Sec: diode rectifier+buck	6.78 MHz	50 mm	44 W	73 % dc-dc	[47]
dc	Pri: Full bridge inverter Sec: rectifier	97.6 kHz	k: 0.44	5 W	71% dc-dc	[48]
dc	Pri: Full bridge inverter Sec: diode rectifier	--	k: 0.1	60 W	78% dc-dc	[49]
ac	Pri: Full bridge diode+inverter Sec: --	6.78 MHz	--	50 W	92 % ac-primary load	[40]

2.1.2.2 High power WPT system

In this section, previous research on the single-phase high power WPT system is reviewed. So far, the high power WPT systems are mainly for EV charging. The power rating typically greater to kW.

Fig. 2.10 shows a typical high power WPT system architecture [51], [52]. Different from consumer electronics, these high power systems typically are designed including the front-end ac-dc rectifier. The ac-dc rectifier converts line frequency ac to a regulated dc bus. It can regulate the output power by adjusting the bus voltage. Include this stage in the design scope, then the subsequent dc-dc converter that was introduced in the consumer electronic WPT systems can be eliminated. The secondary side can employ either the diode rectifier or the active rectifier.

The front-end ac-dc PFC rectifier in the conventional EV wireless charging system is typically comprised of a diode rectifier and a PFC circuit [53], [54], [55]. Fig. 2.11 shows the state of the art EV wireless charging system which is comprised of a bridgeless totem-pole PFC rectifier, full bridge inverter, coils and secondary rectifier [56]. Employing this totem-pole rectifier into transmitter while keeping the subsequent high frequency inverter, the number of power conversion stages is reduced[57], [58], [59]. As reported in [58], the power efficiency at 7.7 kW achieves 96.5% and the PF is 0.99. The control IC for the totem-pole rectifier has been implemented by the IC companies, such as NXP [60]and TI [61].

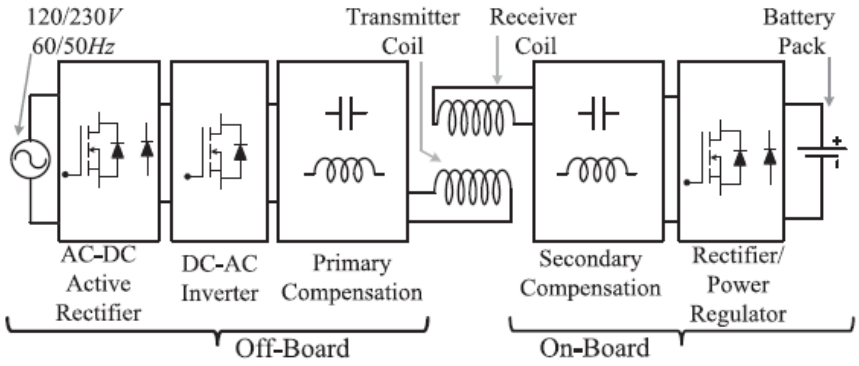


Fig. 2.10. WPT system in EV application with ac power supply [52].

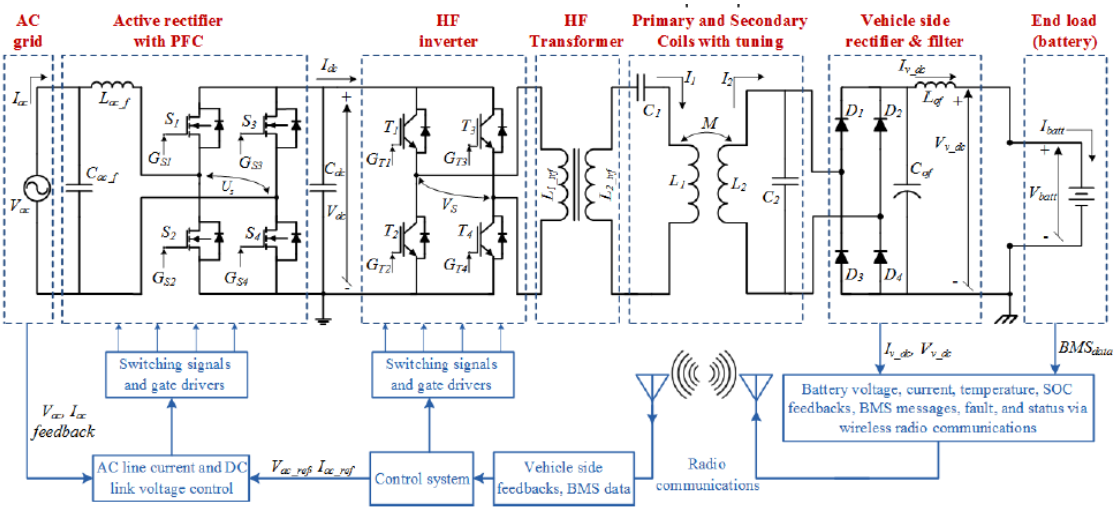


Fig. 2.11. Schematic of EV wireless charging system [56].

References [62], [63]and [64] introduce a full bridge, current fed, direct ac-ac converter in EV WPT applications, as shown in Fig. 2.12. It is a boost-derived topology. Duty cycle and phase shift are employed to control the input current and output voltage with low THD of the input current. The load power is regulated and soft switching is achieved for the inverter switches. However, since the bus voltage is not regulated, significant double line frequency ripple exists on the bus. This double line frequency ripple flows through the coils to the receivers bringing in other harmonics and increasing the radiation from the coils. The impact of low-frequency ripple on the battery is still unknown. Moreover, the actual semiconductor count is high.

The high power WPT system in Fig. 2.13 is formed by a primary integrated Z-source converter and a diode rectifier at the second side. The Z-source converter regulates the input current and output power. However, it is limited to low frequency (for example 20 kHz) applications due to hard switching. Furthermore, a significant double line frequency ripple exists at the output of the transmitter.

Table 2.2 summarizes the comparison among the typical high power WPT architectures for EV charging. In all of those architectures, the design of the ac-dc PFC rectifier is included. The main difference among these architectures is the transmitter structure. Different approaches are investigated to reduce the number of semiconductor devices at the transmitter side.

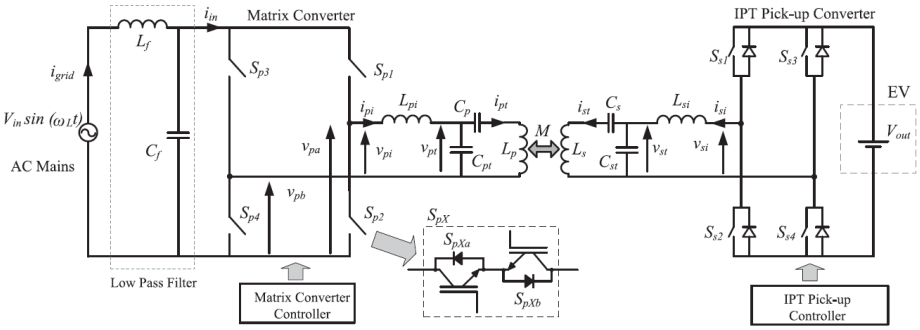


Fig. 2.12. Matrix transmitter proposed in [64].

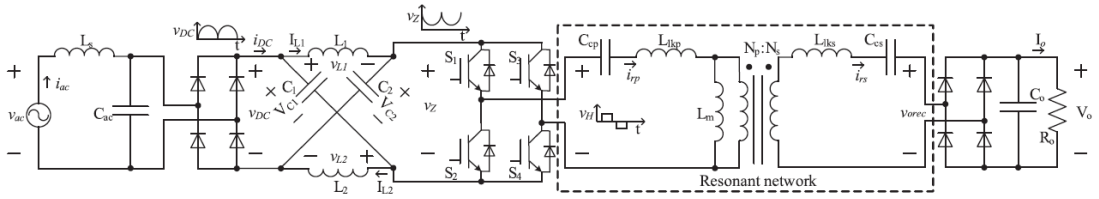


Fig. 2.13. Z source converter based two-stage transmitter [65].

TABLE 2.2 COMPARISON OF WPT FOR EV APPLICATION

Architecture	f_o	distance	P_o	η	Device counts	*Ref.*
Pri: diode rectifier+inverter Sec: diode rectifier	30 kHz	120 mm	3 kW	96 % ac-load	14	[54]
Pri: Totem-pole rectifier+inverter Sec: diode rectifier	22 kHz	162 mm	6.6 kW	92% ac-load	12	[56]
Pri: Matrix converter Sec: diode rectifier	50 kHz	--	1.2 kW	--	12	[62]
Pri: Matrix converter Sec: active rectifier	20 kHz	--	1 kW	89.6 % ac-load	12	[64]
Pri: Zsource converter Sec: diode rectifier	20 kHz	200 mm	1 kW	71% ac-load	12	[65]

2.2 The converter topologies of the transmitter

The transmitter converts utility line frequency ac power to high frequency ac power for driving the transmitter coil. This section provides a literature review of the state of the art of individual power conversion stage. The challenges and opportunities of different topologies in terms of efficiency, voltage and current stress of semiconductor stress and the part count are investigated to guide future research.

2.2.1 Ac-dc rectifier

Since the design for the low power to medium power range WPT system typically employs a commercial adapter as a dc source for the following transmitter stage, the-state-of art ac-dc adapters in the industry and academic area are reviewed in this section.

The diode full bridge rectifier is the simplest rectifier circuit. Depending on the application, a subsequent dc-dc converter might be used to adjust the bus voltage. The flyback is the most popular topology for this dc-dc power conversion due to a low parts count, low cost and simplicity [66], [67], [68] as shown in Fig. 2.14. The well-known flyback converter suffers from high voltage stress during the main switch turns off and high switching loss during the turn on. Therefore, a resistor-capacitor-diode (RCD) clamp [66] or active clamp [69] typically are adopted to solve those issues. In addition, the input current of flyback is discontinuous which requires larger input filter. As a result, the flyback is mainly used for low power level applications. As addressed in [66], the flyback converter is prevalent at lower power levels (below 45 W). [69] shows 94.5% peak efficiency in a 45 W system (90 V ac input voltage, 20 V output voltage) with 25 W/in^3 power density.

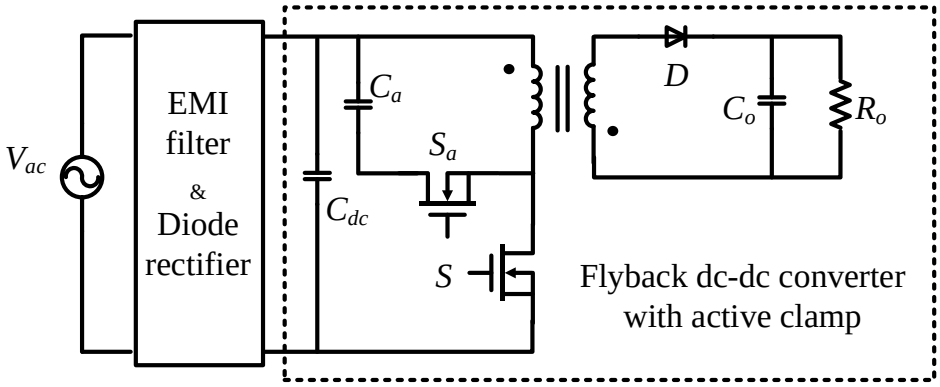


Fig. 2.14. The combination of diode rectifier and flyback for ac-dc converter.

The input current harmonic content of an off-line converter impacts other electronic equipment connected to the grid. The standard IEC-61000-3-2 [70] gives a limitation of the harmonic components for different equipment. Equipment is classified into four categories: (1) Class A includes the balanced 3-phase equipment. (2) Class B includes portable tools. (3) Class C is the lighting equipment. (4) Class D includes monitors, screens, TV, and computers which have input power between 75 W and 600 W.

For higher power application where PFC is required (when power is larger than 75 W), a boost PFC rectifier is often used [71], as shown in Fig. 2.15. The Boost PFC has continuous input current, so it is superior to other topologies such as buck and flyback for smaller input filter design. In addition, the resistive input impedance of boost converter ensures higher PFC and low THD of input current with small control effort. Moreover, buck type PFC rectifier has dead angles during the time intervals when the input voltage is lower than the output voltage. As a result, the boost PFC rectifier offers a cheap and straightforward solution, thus is widely used in industry [72].

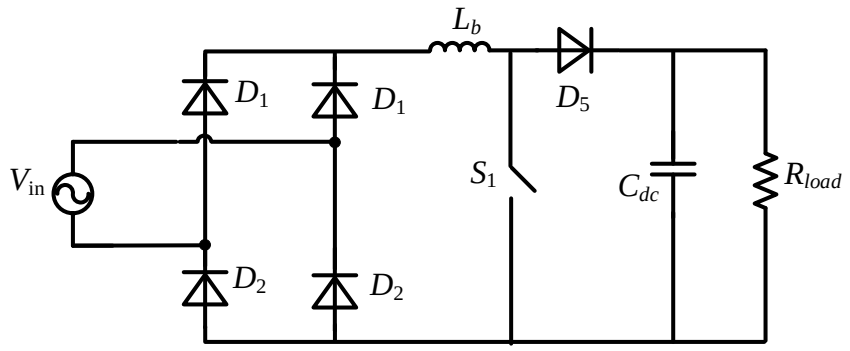


Fig. 2.15. PFC boost rectifier.

The output voltage of the boost PFC must be higher than the peak of the input line voltage. For example, the universal line-voltage range is 90-265 Vrms. If this is the application, the output voltage of the boost PFC must be greater than 380-400V. If the application requires or prefers this voltage rating for the output, then this topology is a good candidate. But for the adapter application which requires low output voltage such as 48 V, 24 V, or 12 V, a high step down dc-dc converter is needed. The resonant LLC converter is typically implemented for the subsequent dc-dc converter due to high efficiency by featuring soft switching and compact size [72], [73], [74], [67], [75]. [72] achieves 95.3 % efficiency and 11.7 W/in^3 power density based on the paper design of a 100 W system. [76] addresses a design case with diode rectifier, boost PFC and LLC for a 150 W adapter that achieves 94.2% efficiency. The peak frequency of PFC and LLC are 1 MHz and 500 kHz respectively. The reported power density is 21.4 W/in^3. In [77] the adapter consists of a diode full bridge rectifier and half-bridge LLC converter with 90 % efficiency. The commercially-available adapters typically have 6 W/in^3 power density. And the best-in-class commercial adapter achieves 12 W/in^3 for 150 W system [78]. A comparison is made based on the literature review, shown in Table 2.3.

TABLE 2.3 COMPARISON OF ADAPTER

Topologies	Power density	P_o	η	Topologies	*Ref.*
Literature	25 W/in^3	45 W	94.5%	flyback	[69]
Literature	11.7 W/in^3	100 W	95.3%	PFC rectifier+LLC	[72]
Literature	21.4 W/in^3	150 W	94.2%	PFC rectifier+LLC	[76]
AN3233	--	150 W	91%	PFC rectifier+LLC	[79]
AN2749	--	40 W	80%	flyback	[80]
DEMO_5ASAG_60W1	--	60 W	83%	flyback	[81]
DEMO-IDP2303A-100W	12 W/in^3	100 W	88.3%	PFC rectifier+LLC	[82]
ADP-65JH HBAN	15.5 W/in^3	90 W	84%	--	[83]
DPS-120AB-3	3.4 W/in^3	120 W	88%	--	[84]

The full bridge diode rectifier in the boost PFC rectifier causes high conduction loss. By integrating of the diode bridge and the boost PFC, the number of semiconductors in the line-current path is reduced. Thus conduction loss is decreased. Bridgeless PFC rectifier [85, 86] achieves lower parts count and higher efficiency by integrating the diode full bridge rectifier with subsequent PFC stage. There are several types of bridgeless PFC rectifiers, such as buck bridgeless rectifier[87], buck-boost bridgeless rectifier, bridgeless flyback rectifier [88], bridgeless SEPIC rectifier [89], [90] bridgeless Cuk PFC [91],[72] rectifier and bridgeless boost PFC [92],[93], [94], [92].

Buck type PFC rectifiers exhibit the above-mentioned disadvantages. The bridgeless buck PFC in [87] integrates a flyback into the circuit which helps improve the dead angle issue. But it increases the complexity of the circuit significantly. The measured PF is 0.95 and efficiency is below 90%. Bridgeless flyback rectifier in [88] suffers from high voltage stress on the main switch. The bridgeless SEPIC rectifier requires 7 passive components [89]. The bridgeless Cuk PFC is derived by integrating the boost PFC and LLC resonant converter. The advantages of this topology include isolation and step-up and down capability. The main issue of this topology is the high voltage stress on the main switches. In addition, a snubber circuit is required to avoid over voltage the main switch.

For non-isolated applications, the bridgeless boost PFC, shown in shown in Fig. 2.16 [86] has many merits including simple circuitry, high efficiency and achievable high PF and low THD with simple control. Compare with the conventional PFC rectifier in Fig. 2.15, two diodes are eliminated. As a result, there are always two semiconductors placed in the line-current path, resulting in reduced conduction losses. At the positive half-line cycle, D_1, S_1 and S_2 form the current path. During the negative half-line cycle, D_2, S_2

and S_1 start to operate. However, this bridgeless PFC rectifier has significantly higher common-mode noise than the conventional PFC boost rectifier [95], [96]. The operation at the positive half- line period when S_2 has connected the output ground to the ac source is normal. But at the negative half-line period, the output ground is connected to the ac source with high frequency pulses. The amplitude of those pulses is equal to high bus voltage. Those high frequency voltage pulses charge and discharge the equivalent parasitic capacitance between the output ground and the ac line ground, resulting in the asymmetrical on the two half line period, eventually causing a high common-mode noise [92].

A modification of this original bridgeless rectifier is totem-pole rectifier as shown in Fig. 2.17. This totem-pole rectifier considerably reduces the common mode noise issue by exchanging the position of D_1 and S_2. At the positive period, rectifier ground is connected to the ac source via D_1, at the negative period, ac source is connected to the constant positive bus terminal. Thus, the high frequency pulses on the ground as discussed above is eliminated. So, the common mode noise is reduced. Because of the low component counts, high efficiency and low common mode noise, this totem-pole rectifier has been widely investigated for the charger and data center power supply applications[93]. Recently Texas Instrument launched a reference design for 1.6 kW GaN based 1 MHz CRM interleaved totem-pole rectifier. This reference design achieves 98.7% efficiency at full load and 250 W/in^3 power density [61]. The adapter consists of a CCM front-end totem-pole rectifier and subsequent LLC resonant converter that achieves 94.5% efficiency in a 500 W prototype [97].

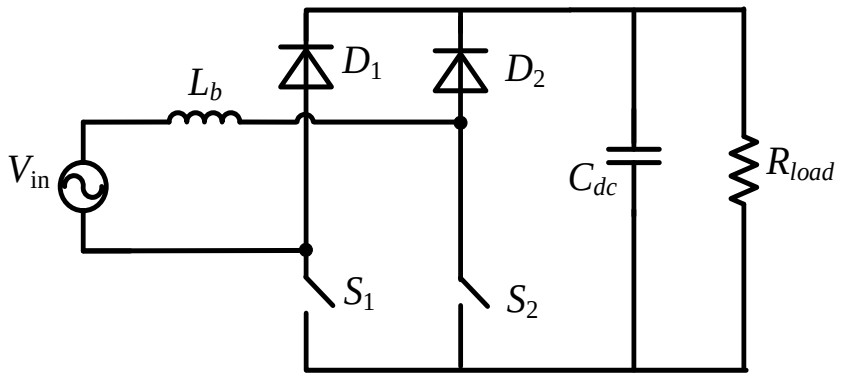


Fig. 2.16. Basic bridgeless boost rectifier.

2.2.2 High frequency resonant inverter

Class E and class D are two popular power amplifiers due to high efficiency and simple circuitry.

A. Class E inverter

The schematic of Class E amplifier is shown in Fig. 2.18. It is comprised of a transistor and a load network. The transistor operates as an on/off switch and the load network shapes the voltage and current waveforms to achieve the lowest power loss via soft switching. The main advantage of class E amplifier is that it only consists of a single transistor and gate driver. Moreover, it absorbs parasitic capacitance of the transistor as a natural part of the operation.

However, it has many limitations.

(1) The voltage stress on the switch is 3.56 times the bus voltage V_{DD} [98]. In practice, when the C_{oss} of transistor replaces C_s, the non-linear variation of C_{oss} with drain voltage can further increase the voltage stress across the semiconductor, reaching a value of almost 4.4 times the input voltage [99].

(2) The Class E amplifier is sensitive to load variation. To achieve high efficiency, ZVS is necessary for this class E amplifier. The output network is tuned inductively for a specific load for the soft switching operation. In loosely coupled WPT systems, there is load variation due to variation in the coupling between the transmitter and receiver, introducing changes in the load impedance seen by the amplifier, as shown in Fig. 2.19. When the load increases, the pre-tuned network changes from inductive to capacitive, therefore resulting in high switching loss. When the load decreases, it becomes more inductive and causes in high loss due to diode conduction.

There are different methods proposed to extend the soft switching range of the class E inverter. In [50], the resonant tank is tuned at a higher resonant frequency ω_{oTx} than the receiver's resonant tank frequency ω_{oRx}. The transistor switching frequency is ω_d. $\omega_{oTx} > \omega_{oRx} = \omega_d$. By adjusting ω_d, the effective C_s can be changed, that is, the effective equivalent resistance and inductance of the primary tank can change for different operation scenarios. However, there are some limitations. For example, the effective C_s should always be larger than the C_{oss} of the transistor. This also helps reduce the impact of the nonlinearity of C_{oss} in the practical operation. [42] proposes implementing dual-channel class E instead of single-ended class E amplifier to improve the power efficiency at light load. Dual-channel allows the system to shut down one of the channels at light load. When both the channels are enabled, the equivalent inductance across both inductors is L_r /2, while if one channel is enabled, the equivalent inductance becomes L_r. However, when the number of channels increases, the problems caused by device mismatches might outweigh the benefits. Also, the loss in L_{out} will increase due to doubled ESR in the L_r.

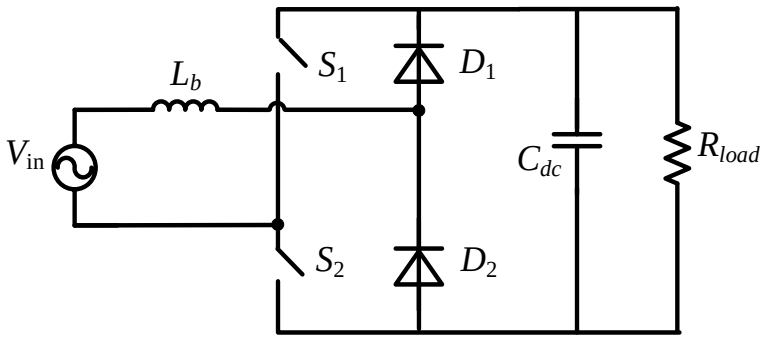


Fig. 2.17. Improved bridgeless boost rectifier (Totem-pole bridgeless rectifier).

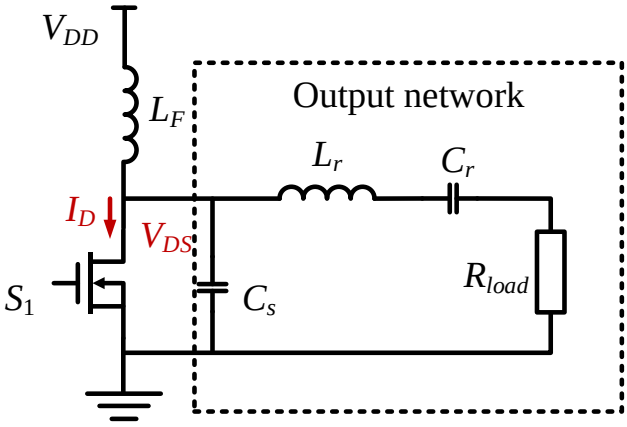


Fig. 2.18. Class E power amplifier.

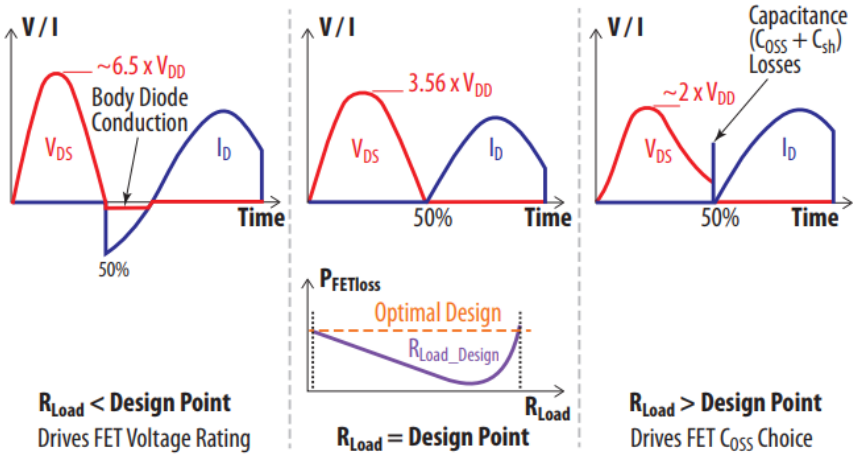


Fig. 2.19. Class E operation under various load conditions [31].

B. Class D inverter

The Class D amplifier [100], can be categorized into two topologies, half-bridge and full bridge configurations. Fig. 2.20 shows a half-bridge class D amplifier. Soft switching has to be implemented in the high switching frequency application for high efficiency. There are two methods for the ZVS operation. First, tuning the load to be inductive, allows the load current to provide enough current during dead time for ZVS. Second, an auxiliary circuit to assist with ZVS operation can be introduced as shown in Fig. 2.20 [101], [40], [102]. Table 2.4 compares several high frequency resonant inverters from academic papers and commercial products.

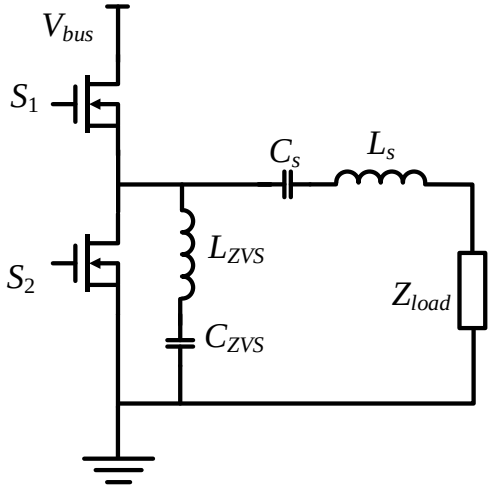


Fig. 2.20. Class D transmitter(half-bridge configuration).

TABLE 2.4 COMPARISON OF HIGH FREQUENCY RESONANT INVERTER

Input	Architecture	f_o	P_o	η	*Ref.*
Literature	Class E inverter	1 MHz	366 W	96.6 % dc-ac	[103]
Literature	Class E inverter	6.78 MHz	30 W	90% dc-ac	[104]
Literature	Derivation of class E inverter	1 MHz	13 W	90.3% dc-ac	[105]
NXQ1TXH5	ZVS class D	110~205kHz	5 W	85% dc-ac	[33]
EPC9052	Class E inverter	6.78 MHz	33 W	90% dc-ac	[30]
EPC 9065	ZVS class D	6.78 MHz	33 W	92.5% dc-ac	[30]
EPC 9512	ZVS class D	6.78 MHz	33 W	90.6% dc-ac	[30]

2.2.3 Single-stage ac-ac converter for induction heating and lighting

To reduce the parts count and to achieve high efficiency and high power density, single-stage ac-ac topologies have been studied in various applications, such as induction heating and lighting. For the WPT applications, it is still a new and interesting topic.

The single-stage converter in [106-109] is developed by integrating a bridgeless totem-pole PFC and half-bridge inverter. However, the operating range of this topology is limited. The rectifiers addressed in [106] and [107] operate in discontinuous conduction mode (DCM). The switching frequency is fixed, while the duty cycle is used to control dc bus voltage and regulate output power simultaneously. This control scheme results in a narrow operating range. In the induction heating application [108], [109], bus voltage allows large double line frequency ripple, so continuous conduction mode (CCM) with a fixed switching frequency and duty cycle within the line period is implemented. However, this

solution is not suitable for WPT systems, because low-frequency harmonic content increases the power loss and radiation in the coils.

Another single-stage ac-ac converter is derived by integrating a bridgeless totem pole PFC and full bridge inverter [110-112]. Using a full bridge inverter instead of a half-bridge potentially improves the output power capability, and enables phase-shift control. Because the converter is used for induction heating applications, the suppression of large double line frequency ripple on the dc bus is not required in [111]. The output power regulation is not discussed in [112].

2.3 Compensation network

The compensation network also referred to an impedance network (IMN), is comprised of inductors and capacitors. The IMN is typically placed on the transmitter side and receiver side, as shown in Fig. 2.21.

There are many different types of compensation networks for different design goals. But, generally they are built to achieve the following one or several targets:

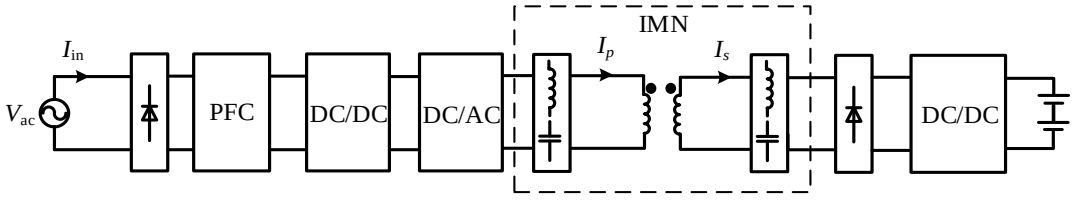


Fig. 2.21. Impedance matching network in the WPT system.

(1) To transfer power through transmitter coil and the receiver coil, the leakage and magnetizing inductance of those coils bring in high reactive power. And the circulating current increases system losses. Capacitors are added either in parallel or series to cancel the inductance. The basic idea is to use the compensating capacitor at the receiver side to resonate with the secondary coil, further to maximize the power transfer. The primary capacitor is designed to cancel the reactance and therefore achieve unity power factor at the output of the transmitter [113].

(2) The maximum achievable efficiency of the WPT system is decided by parameters, such as the coupling coefficient, quality factor of coils [50], and the efficiency of the high frequency inverter and rectifier. Actually, the compensation network can be designed to improve the efficiency of the inverter by assisting it to obtain ZVS operation if MOSFETs are employed for the active switches. If the load current is lagging the voltage of the inverter, ZVS is achievable. Adjusting the capacitors of the compensation network can help provide inductive load behavior for the inverter, therefore help for ZVS.

(3) A compensation network is designed to help in obtaining constant voltage [114] or constant current. There are many parameters in the WPT system that are variable. For example, the distance between the transmitter coil and receiver coil changes in the transcutaneous energy transmission system when the patient is breathing. The number of loads changes in the multiple receiver applications, when one cell phone is suddenly added to the system where several other cell phones in the middle of charging. So proper design for the compensation network can help reduce the control complexity of the varied parameters.

(4) The bifurcation phenomenon in the WPT system denotes the situation in which the frequency of zero phase angle is not unique[115], [116]. The number of frequency points for the zero phase angle is determined by the load condition, compensation network design and the range of frequency swing [116]. In [114] and [117], the bifurcation phenomenon is used to get constant output voltage within a frequency range. But if the system requires bifurcation-free impedance within a certain frequency range, then the compensation network should be designed carefully.

There are four basic compensation networks: SS, SP, PS, PP [118], [119], [120], [115], [121]. The schematic of those four basic compensation topologies is shown in Fig. 2.22. The first S or P indicates series or parallel compensation of the primary coil and the second S or P stands for series or parallel compensation of the receiver coil. L_p and L_s are the transmitter coil and receiver coil inductance respectively. C_p and C_s are the resonant capacitors of transmitter and receiver. Their design is quite flexible according to application requirement. For example, the resonant capacitor can be designed to resonate with the self-inductance of the coil or the leakage inductance of the coil. The former one can obtain a higher ratio between the active power and reactive power, while the latter can maximize the transferred power [119]. But, generally, they have the following features.

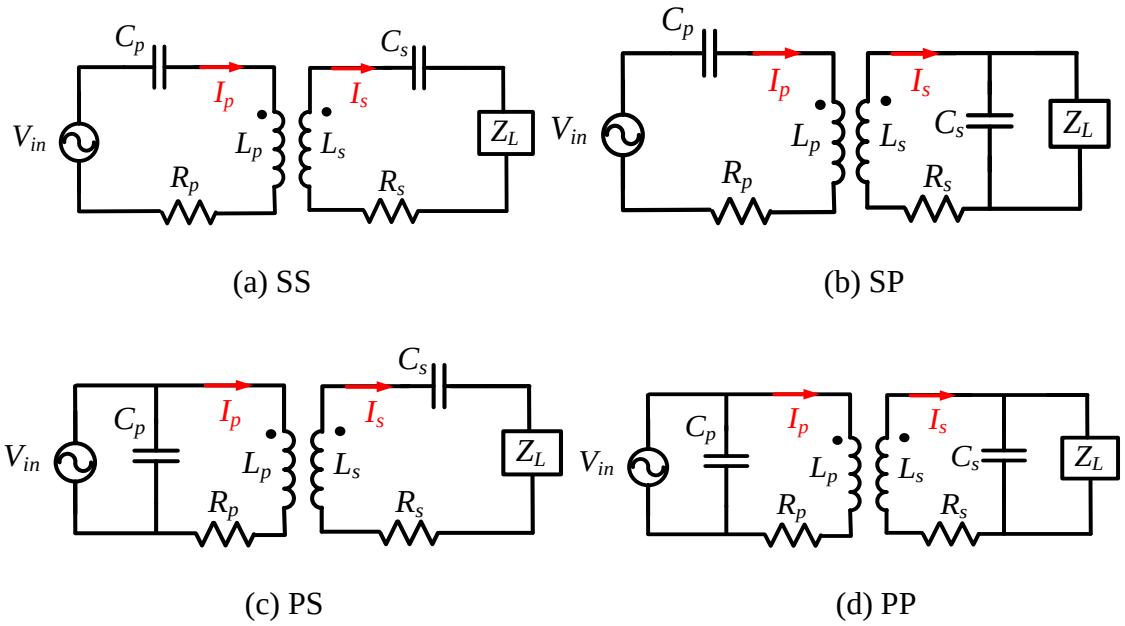


Fig. 2.22. Basic compensation networks.

(1) SS network. The compensation parameters are independent of the coupling coefficient and load. Therefore, it is best suited for the conditions where the load dramatically changes, or the position of receiver frequently moves. If L and C are properly designed, the constant current I_s or constant output voltage on the load can be obtained at the system output [115]. Since the capacitor is connected in series with an inductor, the voltage stress on it might be high. This is a drawback in the high power application. The resonant capacitor voltage can reach 10 kV[4, 122].

(2) SP network. It can be used to obtain the fixed voltage gain if the mutual inductance is constant. The selection of compensation capacitor C_p is dependent on the coupling coefficient [119], [120].

(3) PS and PP network. PS circuit compensation technique has low sensitivity to misalignment. One of the drawbacks of PS and PP is that voltage source cannot be used to drive them directly. An inductor can be placed between the network and inverter to solve this problem [118]. In addition, the desired C_p for unity power factor is dependent both on coupling coefficient and load.

Besides these four topologies, there are many different compensation networks. more L, C elements are added to extend the design flexibility and achieve a specific target. For example, LCC/S [115] network is shown in Fig. 2.23, and LCL/S network [123] in Fig. 2.24. The terminologies for those compensation networks in different literature might be different. For example, LCL/S in Fig. 2.24 is named as LC/S in [119]. LCC/S and LCL/S can be designed to achieve a constant I_p. This feature is beneficial for the dynamic load changing, such as dynamic charging EV during driving or multiple receiver applications. In addition, these IMN are also investigated to assist with the soft switching

in [124], [125]. The secondary side can be designed as series (as shown in Fig. 2.23 and Fig. 2.24) or parallel, or other LC combinations. If secondary LC is in series, the output voltage can be constant. If it is in parallel, then the secondary current I_s can be constant [115].

As discussed above, the design of compensation networks is quite flexible. Many different combinations of inductance and capacitance can be employed for practical applications.

2.4 Soft switching techniques of PWM converters

With the increasing requirements of high efficiency, small size, high power density, and excellent EMI performance for power electronics converters, the switched mode power conversion technologies developed from PWM converters to resonant converters, then to PWM converter with soft switching auxiliary circuits which can eliminate or reduce switching, further increase the whole system efficiency and reliability.

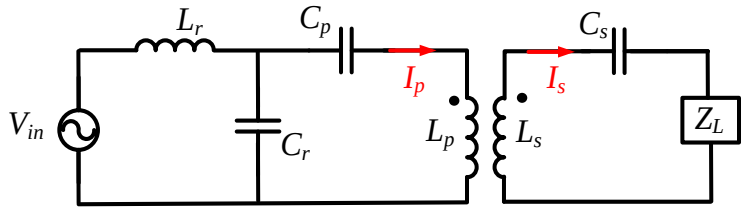


Fig. 2.23. LCC/S network.

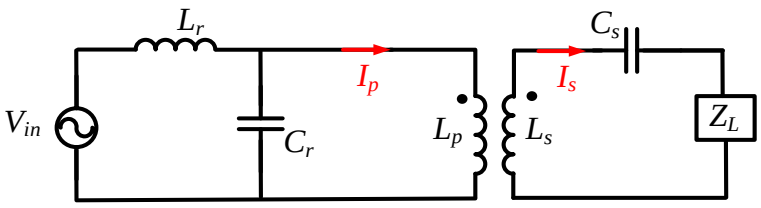


Fig. 2.24. LCL/S network.

2.4.1 The principle of soft switching

The two main circuit topologies in electronic power converter technology are Pulse-Width Modulation (PWM) converters and resonate converters. Commonly PWM converters suffer from high switching loss. Compared with PWM converters, resonant converters have less switching loss [126]. Nevertheless, resonant converters process power in sinusoidal or near sinusoidal waveforms resulting in a higher circulating current. The large circulating current brings in high conduction loss on semiconductors and passives. In addition, the electric stress on a semiconductor is high and might bring in devices failure due to overcurrent or overvoltage. This will make filter design more difficult and impact EMI performance as well [127].

Generally, soft switching PWM converters can be classified to zero voltage switching (ZVS) PWM converters and zero current switching (ZCS) PWM. ZVS method reduces the capacitive turn-on loss by discharging the capacitors in parallel with switching devices to zero just before the gate signal is applied. A parallel capacitor can help reduce the turn off switching loss by slowing down the voltage rising, therefore reducing the turn off overlap loss [127]. In [128] this near-ZVS manner is defined as ZVS turn off. ZCS techniques eliminate the voltage and current overlap by redirecting the switch current to zero before the voltage across the devices rises. Notice that ZCS is not helpful for the capacitive loss during semiconductors turning on.

Generally, for the switching loss, diodes mainly suffer from the reverse recovery loss during their turn off period. ZCS turn off can minimize this loss and also can suppress the ringing issue during turn off. ZCS turn off can reduce the reverse recovery loss in some range, but it might bring in severe ringing at the same time. For MOSFET, ZVS turn on

can eliminate the capacitive loss and overlap loss, ZVS or ZCS turn off can reduce the turn off loss. ZCS is more useful for minority carrier devices such as IGBT [129]. Because they exhibit a current tail at turn off causing considerably high turn off losses.

There are several different ways to obtain resonant behavior for soft switching operation. For basic PWM converters, which have inductors connected to the switching nodes, and those inductors can be utilized as resonant inductors if adopting proper values. One classic method for soft switching in the PWM converter is shown in Fig. 2.25. To get ZVS turn on for S_1, L_b is designed carefully to provide proper negative current. For specified load conditions, this negative current discharges the output capacitor of S_1 and charges the output capacitor of S_2 during the dead time t_0. This resonant behavior brings V_A from zero to V_{in} before turning S_1 on. This operating mode is also called quasi-square waveform (QSW) [130], [131], [132]. For the resonant converter, when the load impedance is designed to give appropriate inductance, the switches will be provided enough energy to discharge the output capacitors before tuning on.

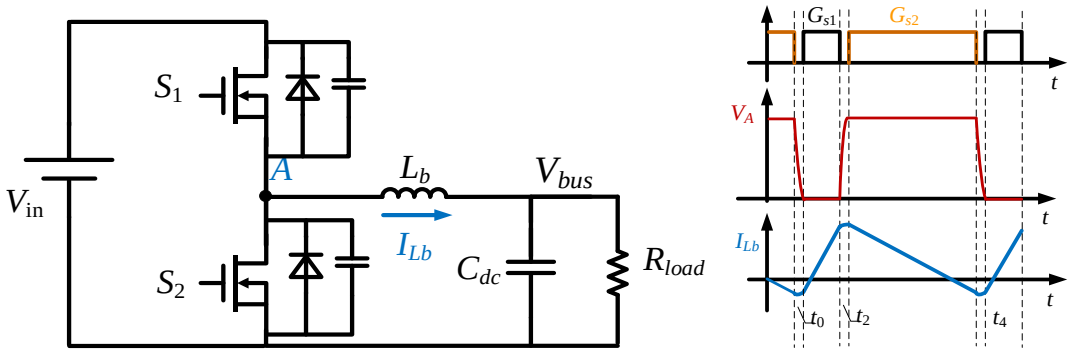


Fig. 2.25. ZVS converter.

2.4.2 Auxiliary circuit to assist with ZVS

For those converters without an inductor connected to the switching node, or the inductive load is not able to be designed for soft switching operation, employing an auxiliary circuit might be a solution. The auxiliary circuits, shown in Fig. 2.26, can be classified into passive auxiliary circuits and active auxiliary circuits [133], [134], [135]. The passive auxiliary circuit is comprised of inductors and capacitors [136], while the active circuit has extras active switches to control the auxiliary current [137]. An active auxiliary circuit such as the active clamped circuit in flyback helps reduce the voltage stress and reduce the switching loss [69]. However, it increases the control circuit complexity. The passive auxiliary circuit has low flexibility, but it is simple and low cost. Besides the auxiliary circuit, the auxiliary converter is another solution for achieving or extending the soft switching range [138]. An example is addressed in Appendix A.

2.5 The control strategy of the wireless power transfer system

The control targets of a WPT system include (1) fast response to the parameter changes of the system, such as load variation and coupling coefficient changes [24], [139], [140]. (2) Achieve the specific requirements according to different applications, such as control output voltage, current or/and power flowing control [59], [141], [142]. (3) Track the maximum efficiency at each operating point [117], [143], [144].

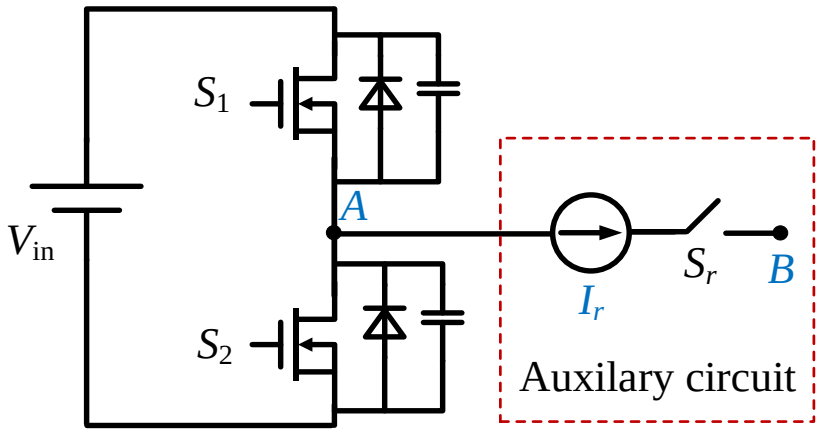


Fig. 2.26. The principle of an auxiliary circuit for soft switching.

2.5.1 The control scheme for single receiver WPT system

Different techniques have been presented in the literature to regulate the output against coupling and load variation. These methods can be categorized into three kinds: primary side-control, secondary side-control, and dual side-control [145].

In primary side-control, the power flow is mainly controlled at the transmitter side. This control strategy can minimize the interaction with secondary-side electronics. For example, by control transmitter, the output power can be adjusted even if the receiver side only has diode rectifier. The receiver side information (output voltage, current, load) can be sensed and transmitted to the transmitter side by a communication link [59]. There are mainly three strategies implemented to accomplish the primary side control.

(1) Changing the switching frequency of transmitter or receiver to regulate the output power/output voltage when it is the control target. Varying the switching frequency adjusts the impedance looking into the transmitter load network [146]. Depending on the control goal, different designs can be implemented. In [114] and [117], the output voltage is desired to be independent of the load. The output voltage has two separate peak frequencies in the

"over coupled" region. The switching frequency is adjusted towards the peak frequency to increase the output voltage/power, and vice versa. In [116], the output of the transmitter is controlled to be zero phase angle for minimum reactive power rating by variable frequency. The ideal control point is difficult to determine if there are multiple zero phase angle conditions within the frequency range. This phenomenon (bifurcation) can be observed especially when the load increases. If the variable frequency control scheme cannot deal with the uncertainty in the bifurcation region, the selected frequency might make the operation drift away from the desired point or move unstably between several undesired operation points.

(2) The impedance matching network is dynamically tuned to control the output voltage. By changing the capacitance or inductance in the impedance matching network, the voltage conversion ratio can be controlled to the desired value. Discrete capacitor arrays with active switches are needed in the tunable IMN [147], [24].

(3) Control the output voltage via a dc-dc converter. This dc-dc converter can be placed before the inverter stage (pre-regulation) [148], or after the rectifier at receiver side (post-regulation) [147]. This method increases the overall size and reduces efficiency.

(4) Control the output voltage of the inverter by adjusting the phase shift or/and duty cycle. Generally, the phase shift and duty cycle have a limited ZVS operating range.

Secondary side control requires active rectifier or post-regulation stage. It is also widely used in the multiple receiver application [145].

Dual side control with communication between transmitter and receiver is so far the most popular control method. It extends the optimum operating range of the system and increases the system robustness. The signal delay caused by the communication is a system

bottom neck [149]. There are different approaches to achieve control targets. (1) Control the output voltage/power with pre-regulation and post-regulation together [117],[143]. (2) All those methods introduced in section A for the primary side control can be implemented. If active rectifier is served, it can be controlled together with primary side circuit to adjust the power flow. Or the post-regulation can be implemented for the control purpose.

2.5.2 The control scheme for the multiple-receiver WPT system

As discussed before, the power of single receiver system can be regulated from the primary side. However, for multiple receiver systems, this control scheme is not applicable. The frequency tracking, automatic impedance tuning and so on at transmitter side cannot individually regulate the power flow for the individual receivers [150]. The secondary side is mainly controlled by individual controllers at receiver side since each receiver has a unique power requirement.

Ideally, the system is desired to achieve high performance, high reliability and high efficiency. However, the increased load and coupling variables (including the cross-coupling) in the multiple-receiver system significantly increases the control complexity.

In [151], [149], [152], [140], [153] time-division multiplexing (TDM) are introduced in the WPT system. In this control, at any time, there is at most one receiver being charged. Each receiver had its own control and communication with the transmitter. The power flow is controlled by managing the charging time of each receiver. With this control methodology, the system operates similarly to a single receiver system.

In the application of a single transmitter charging multiple receivers, [24], [139],[140] regulate the output current as a constant current source by adjusting the input voltage through closed-loop control between the transmitter and receiver. The transmitter in [154]

is controlled as a current source by adjusting the phase shift between inverter phase legs. However, these approaches are limited by the communication and control bandwidth, resulting in poor dynamic response to a sudden load change. At the output of the class E amplifier [155], [142], and the output of full bridge inverter [156],[157], an LCL impedance matching network (IMN) is added to obtain constant current behavior from a voltage source. This constant current output smooths the response to dynamic load changing in the multiple receiver application. The design parameters of the LCL network depends on the control target, such as minimum component count, high efficiency, simplicity, and low harmonics.

The cross-coupling of receivers will impact the power distribution. Efforts have been made to compensate/reduce the impact from cross-coupling [158], [21]. The time-division charging strategies reviewed above avoid the cross-coupling issue.

In the other works, the assumption is made that each receiver keeps a large enough distance with each other, therefore, the cross-coupling effect is negligible [24], [139],[140].

2.6 ZVS detection

Since the switching frequency of the converter in the system is 6.78 MHz, ZVS is typically adopted to minimize switching losses [40], [110], [101]. However, ZVS is designed based on a certain operating range. When the converter runs into unexpected condition, for instance, a large capacitive load, it loses ZVS. Significant switching loss due to hard switching may damage the converter. In order to improve the robustness and efficiency of the system, ZVS detection is reviewed.

The drain-source voltage V_{ds} of the switch is sensed cycle by cycle in [159], [160], [161]. The device is turned on after V_{ds} drops to zero. V_{ds} of high-side FET is measured via

an auxiliary winding in [159]. This method requires auxiliary winding that complicates the magnetic design. In addition, this method is hard to be implemented in the 6.78 MHz switching converter, since detecting the voltage zero cross point at this high frequency suffers from severe noise and significant signal delay. In [160], ZVS is detected by sensing the gate supply voltage and compared to the drain voltage in the gate driver. In [161], V_{ds} is sensed through an auxiliary diode in the gate driver. The detection circuits in [160] and [161] are integrated into the gate driver, so noise and the signal delay are limited. However, it requires great efforts on the IC design. ZVS is detected by sensing the voltage slope of a switching node in [162]. A half-wave rectifier converts the pulse voltage that presents the voltage slope to dc voltage. An auxiliary switch is added to reset the stored charge on the holding capacitor every switching cycle. This method avoids directly sensing high frequency V_{ds}. However, the auxiliary switch requires independent high frequency PWM and gate driver which increase the loss and complexity of the circuit.

2.7 Summary

This section summarizes the literature review from three aspects:

(1) Fig. 2.27 concludes the efficiency number from the literature review in this chapter. The squares indicate efficiency reported in academic papers, while circles denote the efficiency of commercial products.

The front end ac-dc rectifier in the consumer electronics application is well-researched. According to the plots, high efficiency is achieved in both industry and academic works. Thus typically it is neglected in the design or optimization of the consumer electronics WPT system. Significant efforts are made towards the subsequent power conversion stage design, including the high frequency resonant inverter, secondary side receiver, or design

of the inverter and secondary receiver together (refer to the dc-dc stage). A commercial ac-dc adapter or alternatively, a dc voltage source from a battery or other dc supply is implemented to provide input voltage for the subsequent converter. This separated design approach causes several problems:

- Even if each individual stage achieves high efficiency and high power density, the cascaded structure will result in lower efficiency and power density for the overall system. For example, [30] demonstrates 92.5% efficiency in a 33 W 6.78 MHz class E inverter. If the adapter with 95.3% efficiency (maximum power is 100 W, 11.7 W/in^3 power density) [72] is employed to supply this inverter, the overall efficiency of the transmitter drops to 87%. And 8.5 in^3 will be added to the inverter to form the complete transmitter.
- The dc output of the commercial adapter is typically a fixed value. This fixed input voltage of inverter limits the efficiency optimization.
- When the transmitter needs different input voltage for output voltage/power regulation, an extra dc-dc stage will be added in front of the power amplifier, as shown in Fig. 2.28. As a result, additional components, volume, and loss will be added.

Alternatively, a transmitter considering the rectifier and inverter design together has been proposed for the low WPT application where PFC is not required [70]. It achieves high ac-ac efficiency as shown in Fig. 2.27. There are several ac-ac single stage converters have been proposed and verified in the lighting and induction heating application in the above-mentioned literature. However, no prior work has investigated the feasibility of a single-stage transmitter in the WPT application.

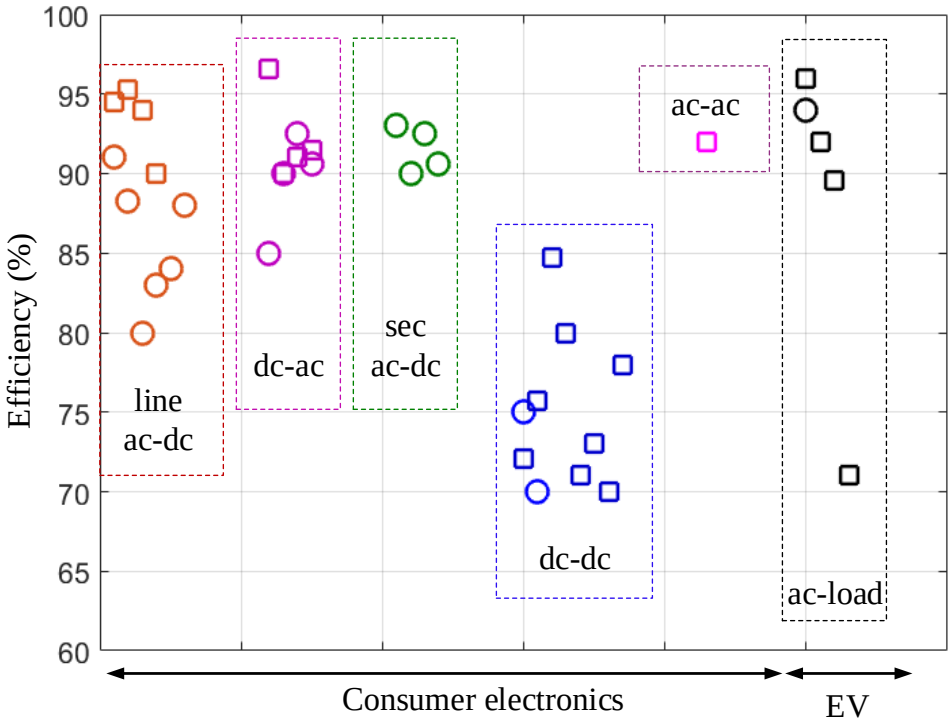


Fig. 2.27. The reported efficiency from the literature review.

(2). With the emerges of WBG power devices, designing the high efficiency and high frequency (up to 13.56 MHz) resonant inverter with hundreds of volts bus voltage is achievable [40]. When boost type PFC rectifier is implemented because of high PF and low THD via simple control, the output voltage does not need to be stepped down to tens of volts for the subsequent resonant inverter. Therefore, one step-down dc-dc stage can be saved.

(3). The application of single transmitter with multiple receivers will be the direction of the future consumer electronics WPT system. However, the WPT system with multiple receivers significantly increases the system complexity. (1) The load condition is complicated. The impedance of each is entirely different. And the required power of each load is also not unique. (2) The system must have fast response to guarantee “drop and

charge" for each device. As a result, the design consideration for the multiple receiver application should focus on: the control of power flow and ensure the fast response to load step changes.

This research focuses on the transmitter design. The efficiency and cost of the transmitter are the main considerations. The efficiency and the number of power semiconductors in the state-of-art 6.78 MHz transmitters within 100 W power range are summarized in Fig. 2.29. In terms of efficiency, since extra PFC circuits are required for the transmitter with larger than 75 W power level, the transmitter efficiency at lower power application is generally higher than the ones' at higher power application. In terms of cost, the number of power semiconductors is used to estimate the cost, because the cost of semiconductors that capable of switching at very high frequency is expensive. Table 2.5 breaks down the number and the price of semiconductors in the transmitter. According to the values in Table 2.5, the total price of power semiconductors in the 6.78 MHz transmitter is high. And it might take a large part of total converter cost. Thus using the number of power semiconductors in the 6.78 MHz transmitter to compare the converter cost among different transmitters is valid.

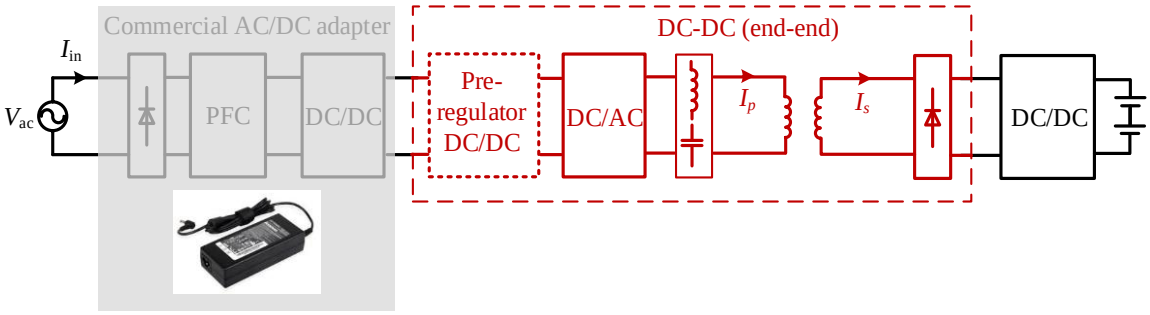
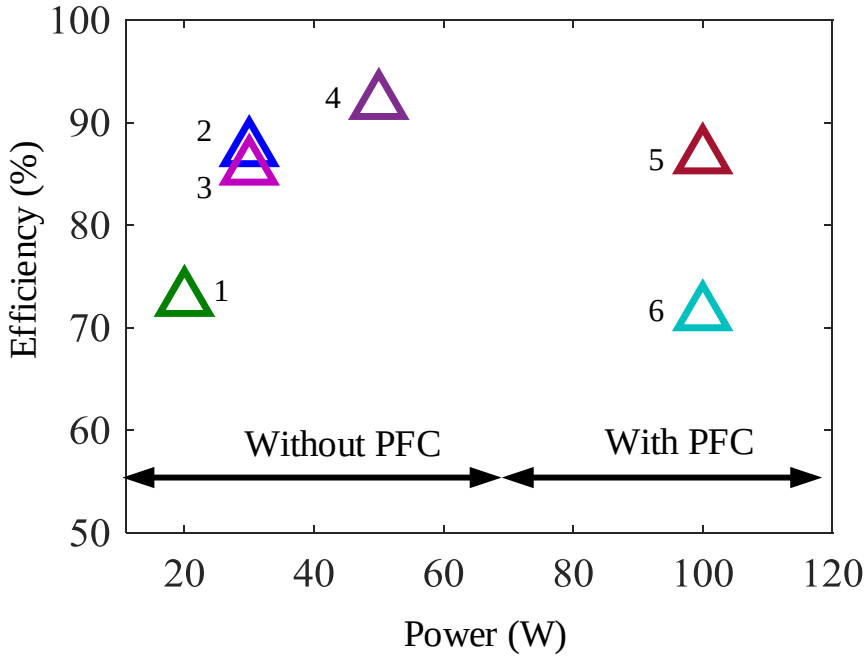


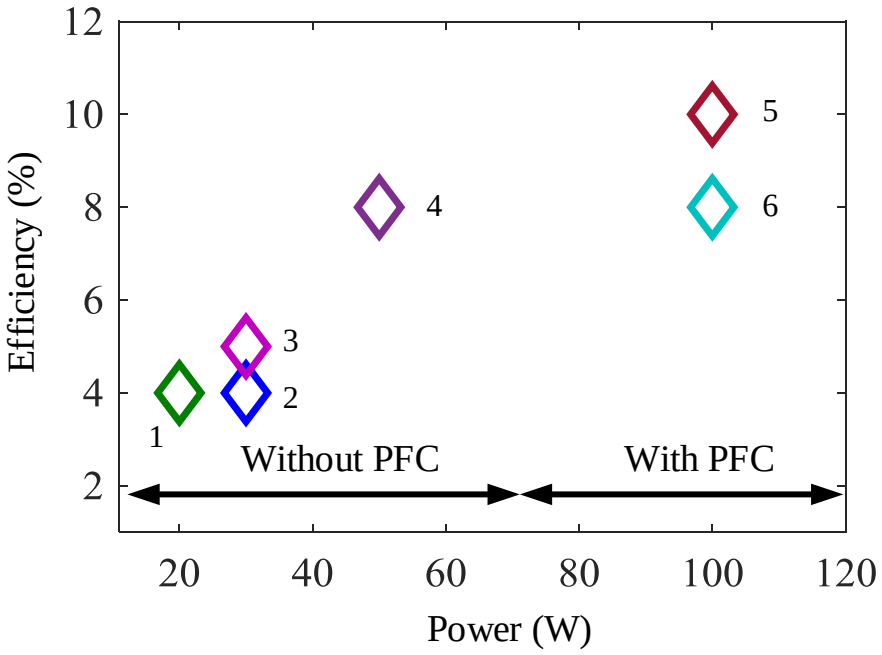
Fig. 2.28. Traditional WPT system in the consumer electronics application.

TABLE 2.5 NUMBER OF POWER SEMICONDUCTORS BREAK DOWN

Transmitters	6.78 MHz devices	Kilo herds devices	60Hz devices	Total
#1	1($2/each)	3($2.7/each)	0	4
#2	1($2.2/each)	3($2.7/each)	0	4
#3	2($2.3/each)	3($2.7/each)	0	5
#4	4($12/each)	0	4($--/each)	8
#5	6($--/each)	4($--/each)	0	10
#6	4 ($31/each)	4($--/each)	0	8



(a) The efficiency of the state-of-art transmitter



(b) Number of power semiconductors in the state-of-art transmitter

Fig. 2.29. The state-of-art transmitter in the consumer electronics application.

3 TWO-STAGE TRANSMITTER DESIGN

For multi-stage transmitter systems, even if each conversion stage exhibits low component count, high efficiency, and high power density, when the overall transmitter is evaluated, those achievements of the individual stage will be sabotaged.

In this chapter, a two-stage transmitter for the consumer electronics application (100 W) will be designed and implemented. The WPT system with this two-stage transmitter is shown in

Fig. 3.1.This two-stage transmitter is designed to achieve:

(1) Obtain high power efficiency with less component count than the multiple stage transmitter of the conventional approach.

(2) Achieve high PF and low THD of the input current

(3) Constant output current I_p for charging multiple devices.

3.1 Topology selection

3.1.1 Bridgeless PFC rectifier

As discussed in Section 2.2.1, the bridgeless PFC rectifier achieves high efficiency by reducing the number of components in the current path. Several bridgeless PFC rectifier, reviewed in Chapter 2 are summarized in TABLE 3.1. Based on the efficiency, THD, and device count, the bridgeless Cuk, and totem-pole rectifier are selected as candidates for the PFC stage.

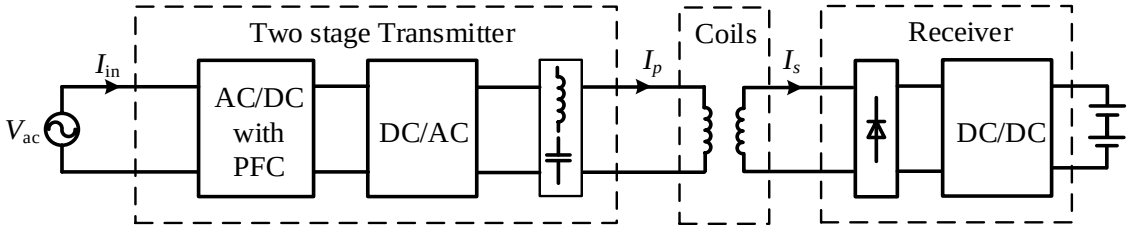


Fig. 3.1. WPT system with the two-stage transmitter.

TABLE 3.1 COMPARISON OF BRIDGELESS PFC RECTIFIER

Topologies	P_o	η	device counts	passive counts	merits	limitations	*Ref.*
Bridgeless buck	700 W	96.4%	6	4	Simple	High THD (43%)	[163]
Bridgeless flyback	70 W	88%	6	2	Isolated	Need snubber	[88]
Bridgeless SEPIC	60 W	96.7%	4	6	High efficiency, low THD	High part counts	[89]
Bridgeless Cuk	100 W	95.6%	4	3	Isolated	Need snubber	[72]
Bridgeless Boost	350 W	98.5%	4	2	High efficiency, PF, low THD	High bus voltage	[164]

A. Bridgeless Cuk PFC rectifier design

The bridgeless Cuk PFC is derived by integrating the boost PFC and LLC resonant converter [72], as shown in Fig. 3.2. L_b is the boost inductor, S_1 and S_2 are connected in back to back and form a bidirectional switch. C_r and L_r form a resonant circuit. S_3 and S_4 are used as the synchronous rectifier. At the positive ac input period, the switching cycle can be separated into two periods. When S_1 and S_2 are turned on, V_{ac} is applied to L_b resulting in a linearly increasing boost current I_{Lb}. Meanwhile, S_3 is turned on, and S_4 is off. So, C_r, L_r, S_1, S_2, and S_3 form a resonant circuit. When the resonant current reaches zero at t_s, S_1, S_2 and S_3 turn off, S_4 turns on. Since at this time i_r is zero, during this switching transition, i_r is forced to increase to I_{Lb} immediately. This fast transient results in a high voltage across S_1. A snubber circuit based on Zener diodes can be implemented to limit the peak voltage [91]. The voltage ratio in this topology is:

$$M = \frac{V_o}{V_{in}} = n\frac{1}{1-D} \tag{3-1}$$

where n is the transformer turns ratio, D is the duty cycle of boost. As seen, the output voltage is determined by n and D. Thus M can be designed less than 1. As a result, low voltage stress can be applied to the subsequent inverter.

A paper design is conducted to investigate the feasibility of this topology for the two-stage transmitter application. As shown in the 100 W design case in [72], the highest loss results from hard switching in the devices. Thus CRM operated boost is implemented to achieve ZVS operation. The design parameter are shown in Table 3.2.

TABLE 3.2 DESIGN SPECIFICATION OF CUK RECTIFIER

Parameters	Values	Parameters	Values	Parameters	Values
Vin	120 V	f_s	100-700 kHz	L_b	103 µH
P_o	100 W	f_r	350 kHz	n	5 turns
Vo	40 V	L_r	0.39 µH	S_1/ S_2	EPC 2025
Vs	200 V	C_r	0.53 µF	S_3/ S_4	EPC 2035

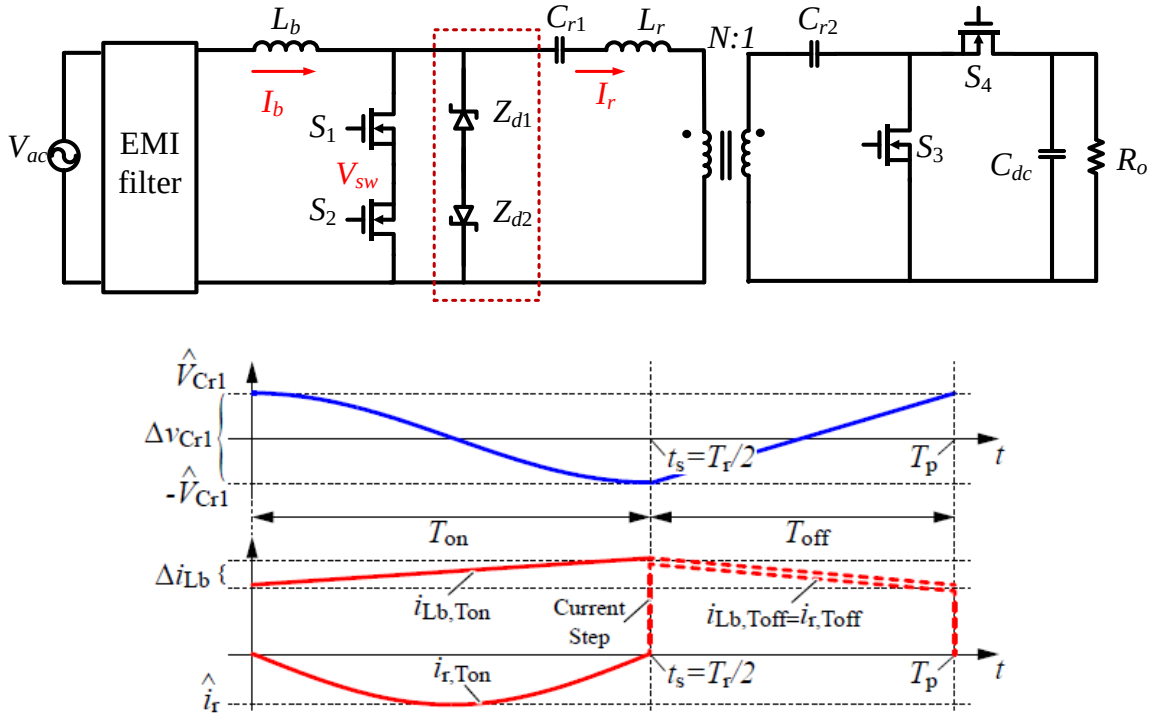


Fig. 3.2. Bridgeless Cuk PFC rectifier [72].

The device loss at 100 W is 1.5 W which is obtained from simulation with the actual models of semiconductors. Substantial ringing on S_1/ S_2 is observed when they are turned off, and the waveform is shown in Fig. 3.3. With the 200 V bus voltage design, 360 V peak voltage is observed. This feature makes the implementation of EPC 2025 into this rectifier impossible. So, a Zener snubber (Z_{d1} and Z_{d2}) can be added as shown in the red box in Fig. 3.2. Extra loss is expected from Zener diodes. In addition, the output capacitance of $Z_{d1}$and Z_{d2} will be added to the output of S_1 and S_2,that increases the effective C_{oss}, eventually requiring larger negative current for ZVS.

B. Bridgeless totem-pole rectifier design

The Totem-pole rectifier shown in Fig. 2.17 is evaluated next. Since the operation of totem-pole rectifier has been reviewed in Section 2.2.1, this section only addresses the design specification and results. The design parameters are shown in Table 3.3. The boost inductor is the same as the design of bridgeless Cuk rectifier. CRM operation is also implemented for ZVS operation. EPC 2025 is used for all the four devices S_1-S_4. The total loss in those four devices is 0.4 W.

The comparison between Cuk rectifier and totem-pole rectifier is concluded in Table 3.4. Both of them have four active switches. S_3 and S_4 in both topologies can be replaced by the diodes. The Cuk rectifier has a higher number of components. Ideally, the leakage inductance of the transformer can be used as L_r, saving one component. The bridgeless Cuk is isolated by the transformer while the totem-pole rectifier does not have this capability. Thus, if the application requires insolation, the Cuk rectifier is superior. The voltage regulation of the Cuk can achieve M<1. This feature increases the design flexibility of the subsequent inverter stage.

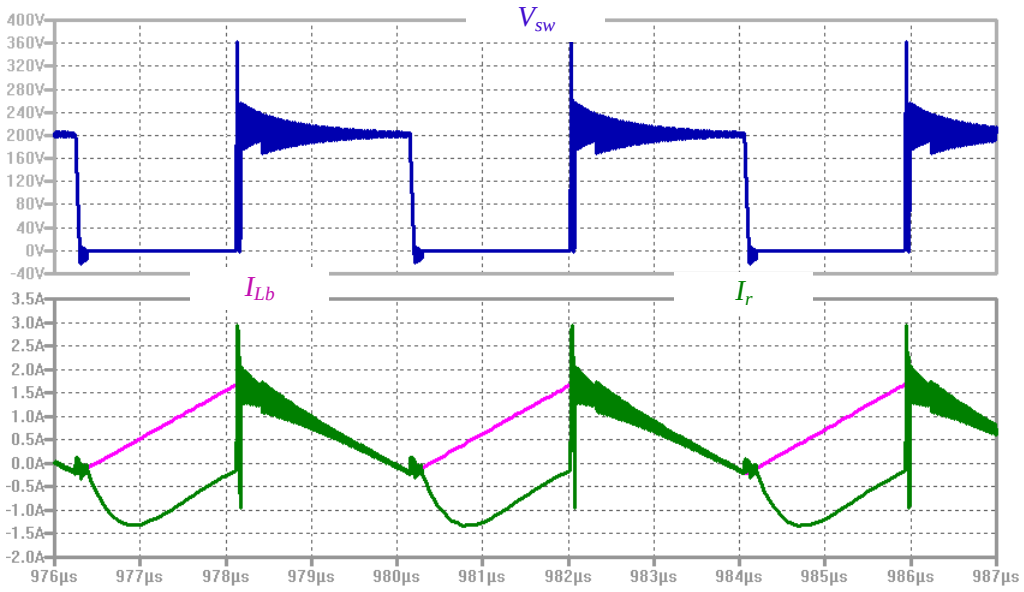


Fig. 3.3. The main waveforms of bridgeless Cuk PFC rectifier in simulation.

TABLE 3.3 DESIGN SPECIFICATION OF TOTEM-POLE RECTIFIER

Parameters	Values	Parameters	Values
V_{in}	120 V	f_s	100-700 kHz
P_o	100 W	L_b	103 µH
Vs	200 V	S_3/S_4	EPC 2025

TABLE 3.4 THE COMPARISON BETWEEN THESE TWO TOPOLOGIES

Items	Semiconductor counts	Total part counts	Isolation	$M=V_o/V_{in}$
Cuk	4	9	Yes	$n/(1-D)$
Totem-pole	4	6	No	$1/(1-D)$
Items	Device loss	Voltage stress on S_1/S_2	Voltage stress on the subsequent stage	Design complexity
Cuk	1.5 W	350 V	low	high
Totem-pole	0.5 W	200 V	high	medium

For example, low voltage GaN devices can be implemented. The minimum output voltage of a totem-pole rectifier is the peak value of input voltage. In practice, some design margin has to be applied, resulting in higher output voltage. This high bus voltage limits the choice of switching devices in the inverter. The loss in the devices is compared by simulation. The Cuk rectifier has a higher loss due to large ringing occurring during the turn off period of S_1, S_2, and S_4. The voltage stress on S_1 and S_2 in the Cuk rectifier is much higher than in the totem-pole rectifier. The Cuk rectifier has higher design complexity, including the resonant tank design and transformer design. Those design parameters are only used for the topology comparison and might be different from the final design. But still, consider these design parameters are valid. The input voltage is 120 V/rms, then the smallest bus voltage is 170 V. Due to huge voltage spike during turn off in the bridgeless Cuk rectifier, the design of high bus voltage should be avoided. Thus, 200 V is chosen. 50 V output voltage of bridgeless Cuk is selected because this value is usually used as the input voltage of the subsequent resonant inverter.

According to this comparison, the totem-pole rectifier is chosen for the two-stage transmitter for the following reasons:

- It has low part counts, lower device loss, and low voltage stress.
- With the new GaN devices, the subsequent inverter stage can operate at high voltage and high frequency with low loss.
- This WPT system is aimed at the multiple devices charging application. The transmitter and coil are supposed to be installed under the table or in the wall. Thus the isolation is not required.

3.1.2 The selection of high frequency inverter

In the literature review, the high frequency resonant inverter topologies have been reviewed. The comparison among class D (half-bridge and full bridge inverter) and the class E inverter is concluded in TABLE 3.5.

The full bridge inverter has the highest number of components. Hence it potentially increases the overall cost and volume of the system. The device voltage stress is equal to the bus voltage. The inverter output voltage swings between –Vbus and + Vbus. The duty cycle of two-phase legs and the phase shift between the two legs can be used to control the output voltage/current/power.

The half-bridge inverter is comprised of two active switches. Thus it has a lower cost compared to full bridge inverter. Since it needs two capacitors between bus to the ground to block the dc component for the output, the size is not necessarily small. The voltage stress on the devices is equal to V_{bus}. The inverter output voltage swing between $-V_{bus}/2$ to $+V_{bus}/2$ at 50% duty cycle. If the switching frequency is fixed, then only the duty cycle of the single-phase leg is used for the output regulation.

The class E inverter has the lowest active switch count. So it has the lowest cost compared to the other two. However, due to its resonant operation, the device voltage and current stress are much higher than the class D inverter, which threatens the reliability of the device. In order to ensure the circuit reliability when implemented in a WPT system, a switch with a maximum voltage rating of at least four times the input voltage may be required. Therefore, the class-E inverter is suitable for low power and low voltage systems [165, 166]. This comparison is concluded in TABLE 3.5.

TABLE 3.5 COMPARISON OF CLASS E AND CLASS D AMPLIFIER

P_o	Class E	Half-bridge	Full bridge
Number of switches	1	2	4
Voltage stress on the switches	3.56 V_{bus}	V_{bus}	V_{bus}
Peak value of V_{ab}	3.56 V_{bus}	0.5 V_{bus}	V_{bus}

According to this comparison, the full bridge resonant inverter is selected for the two-stage transmitter for several reasons:

- The voltage stress on the devices is small compared to class E inverter.
- For the same amount of power and bus voltage, the current flow through devices and output current is smaller than a half-bridge inverter.
- Full bridge inverter can achieve lower harmonic output voltage than a half-bridge inverter.

3.2 The design of Totem-pole rectifier

Fig. 3.4 shows the two-stage transmitter, including a bridgeless totem pole rectifier and high frequency full bridge resonant inverter. Components L_b and $S_1 \sim S_4$ comprise the front-end bridgeless rectifier which converters utility ac input to a desired DC bus voltage. S_1 and S_2 switch at high frequency, while S_3 and S_4 switch at line frequency. MOSFETs S_5~S_8 form a full bridge inverter operating at 6.78 MHz to generate the ac output. L_r and C_r are tuned to a 6.78 MHz resonant frequency.

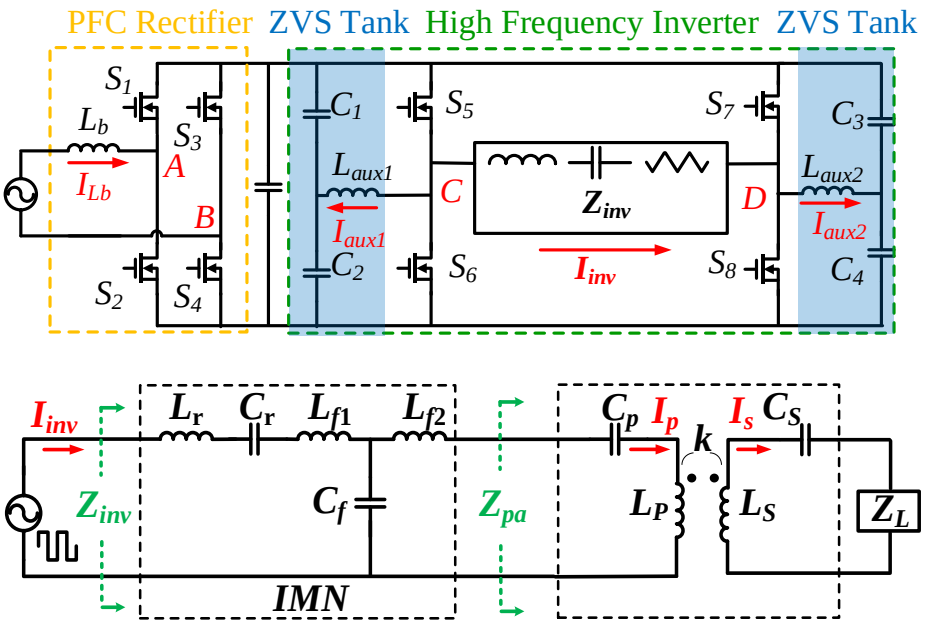


Fig. 3.4. Two-stage converter for wireless power transfer transmitter.

An equivalent circuit of the impedance loading the inverter, Z_{inv}, is given in Fig. 3.4. It is comprised of a resonant tank (L_r and C_r), an IMN (L_{f1}, L_{f2} and C_f), a series-series (SS) compensation network, the two WPT coils, and the equivalent load impedance of receiver Z_L. The IMN is designed to convert the voltage source at the output of the inverter (V_{ab}) to a constant current source at the output of transmitter (I_P). This constant current feature is to ensure a smooth dynamic transition when load change in the multiple receiver application.

L_{aux1}, C_1 and C_2 are the ZVS tank to help S_5 and S_6 achieve soft switching. L_{aux2}, C_3 and C_4 have the same purpose for S_7 and S_8.

3.2.1 The operation of Totem-pole rectifier with CRM

The schematic of the totem-pole rectifier and the waveform of a switching cycle at positive half line period is shown in Fig. 3.5. To implement ZVS operation, CRM is used

in this totem-pole rectifier. The waveform of one switching cycle at positive half line period is shown in Fig. 3.5, where S_4 is always on. The one switching cycle T_s is divided into five stages.

Assume the input voltage is:

$$V_{in}(t) = V_m \cdot sin(2\pi f_{line} \cdot t) \tag{3-2}$$

When S_1 turns off, the negative inductor current I_{Lb} starts to discharge the output capacitor of S_2 and charge the C_{oss} of S_1, resulting V_A resonates from V_{bus} to zero. Then S_2 achieves zero voltage turn on at t_1. As long as S_1 is on, I_{Lb} increases linearly. The increase in inductor current is,

$$\Delta I_{Lb} = \frac{V_{in} \cdot T_{on}}{L_b} \tag{3-3}$$

At t_2, S_1 turns off. At this time, I_{Lb} is at the positive peak value and starts to charge the output capacitor of S_2 and bring V_A to V_{bus}. At t_3, S_1 is turned on at zero voltage. Then the inductor current starts to decrease linearly.

$$\Delta I_{Lb} = \frac{(V_{bus} - V_{in}) \cdot T_{off}}{L_b} \tag{3-4}$$

The switching frequency f_s is:

$$f_s = \frac{1}{T_{on} + T_{off}} = \frac{V_{in} \cdot (V_{bus} - V_{in})}{L_b \cdot V_{bus} \cdot \Delta I_{Lb}} \tag{3-5}$$

The resonant periods will be discussed in the following section. They are ignored in this section for simplicity. Then

$$\Delta I_{Lb} = 2I_{in}(t) = \frac{2P_{in}}{V_m} \cdot sin(2\pi f_{line} \cdot t) \tag{3-6}$$

Combine (3-2) into (3-6), then

$$I_{in}(t) = \frac{V_{in}(t) \cdot T_{on}}{2L_b} \tag{3-7}$$

If T_{on} is a constant value, then I_{in} follows V_{in} well. Therefore, high power factor can be obtained by this CRM operation.

The switching frequency f_s is derived:

$$f_s = \frac{1}{T_{on} + T_{off}} = \frac{V_m^2 \cdot (V_{bus} - V_{in})}{2L_b \cdot V_{bus} \cdot P_{in}} = \frac{V_m^2 \cdot (1 - \frac{V_{in}}{V_{bus}})}{2L_b \cdot P_{in}} \quad (3\text{-}8)$$

It changes along the input line voltage, as shown in the

Fig. 3.6. When the input voltage is near zero, f_s reaches the peak value, while it has the lowest value at the peak of the input voltage. This frequency curve can be used to guide the design for L_b. As seen, larger inductance leads to a lower frequency. This is determined by the design target. To pursue high power density converter, relatively high f_s, and small L_b should be chosen. The reason is that high f_s helps reduce the volume of passives, while passives take the largest space in a converter.

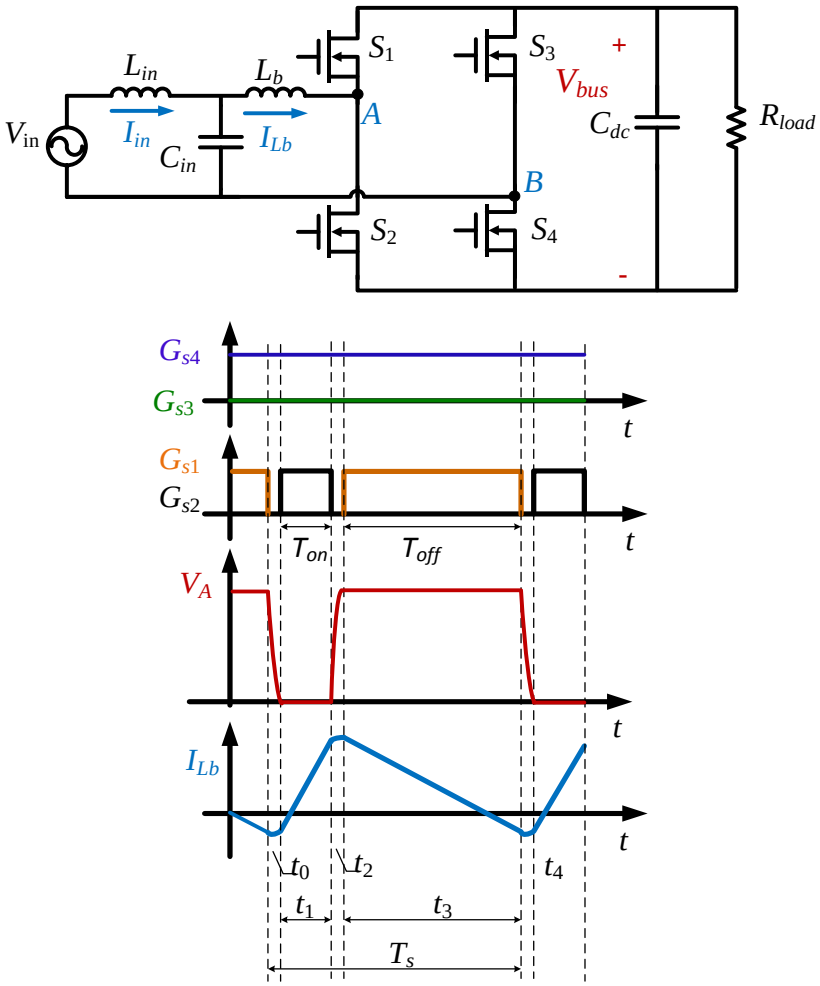


Fig. 3.5. Totem-pole rectifier and the waveform.

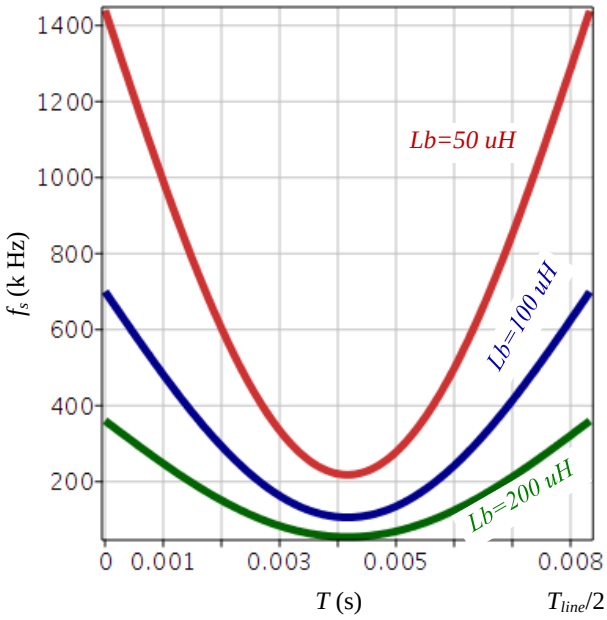


Fig. 3.6. f_s change along with line period in CRM.

3.2.2 ZVS condition for CRM totem-pole rectifier

Even if CRM is implemented in the rectifier, ZVS cannot be maintained over the whole line period. The reason will be discussed next. State plane analysis [14] is applied to analyze resonant behavior during the dead time of S_1 and S_2 and to derive the necessary conditions for ZVS across the line period, as shown in Fig. 3.7. I_r is the inductor current during the dead time. I_r is normalized as J_r ($J_r = I_r / I_{base}$, $I_{base}= V_{base} / R_0$, $R_0=(L_b/C_{oss})^{0.5}$), and V_{ds} is normalized as M_{sw} ($M_{sw}= V_{ds}/ V_{bus}$) in this state plane. M is the normalized DC source, $M= V_{in}/ V_{bus}$.

When $V_{in} =0.5V_{bus}$, if the initial current of I_r is zero, then it just satisfies the ZVS condition. As shown in the green curve, V_{ds} of the main switch resonates from V_{bus} to zero. When $V_{in} \leq 0.5V_{bus}$, with zero initial current, V_{ds} resonates to zero with less time. Under this condition, there is extra resonant current that results in extra conduction loss. In addition, it increases the THD of the input current. When $V_{in} \leq 0.5V_{bus}$, with zero initial current, V_{ds} cannot resonate to zero, as shown in the purple curve. In this case, the main switch experiences hard switching. Fig. 3.8 shows the ZVS region and non-ZVS region within one line cycle according to this analysis.

A negative initial current I_{r0} is needed when $V_{in} > 0.5V_{bus}$ to maintain ZVS operation, as shown in Fig. 3.9. J_{r0} is the normalized value of I_{r0}.

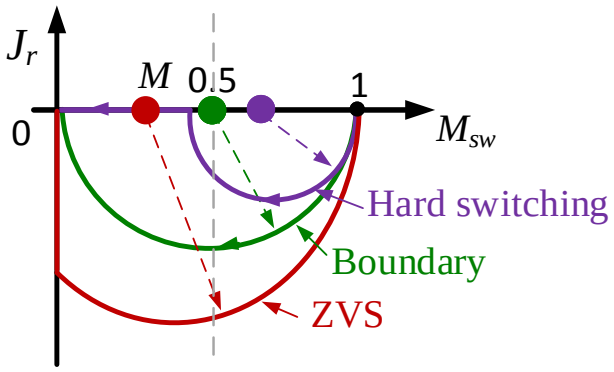


Fig. 3.7. The trajectory of resonance for the CRM with different M_n.

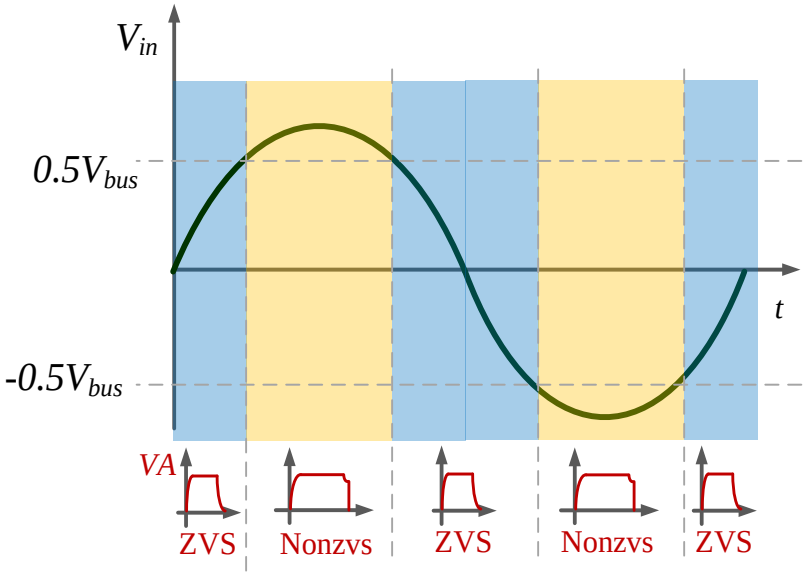


Fig. 3.8. Natural ZVS region and non-ZVS region in a line cycle with CRM.

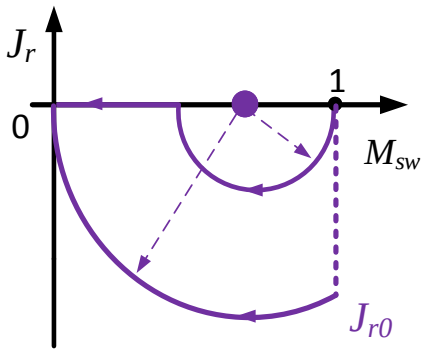


Fig. 3.9. Initial current J_{r0} for ZVS when V_{in} is larger than $0.5Vb_{us}$.

I_{r0} is obtained by solving the state plane.

$$I_{r0} = V_{bus}\sqrt{\frac{C_{eq}}{L_b}\left(\frac{2V_{in}}{V_{bus}} - 1\right)} \tag{3-9}$$

I_{r0} depends on V_{in}, V_{bus}, L_b and the equivalent output capacitance C_{eq} of MOSFETs S_1 and S_2. $C_{eq} = \frac{1}{V_{bus}}\int_0^{V_{bus}} C(v)dv$, $C(v)$is got from the C_{oss} vs V_{ds} curve in the datasheet.

The required initial current varies along the line period according to (3-9).

Various methods of simplification have been implemented to facilitate an embedded implementation. In [8], [10], [15], I_{r0} as a function of V_{bus}, $V_{in}(t)$, L_b and C_{eq} is pre-calculated, then stored as Look-Up-Table (LUT) in a digital signal processor (DSP). However, this method limits the resolution of operation points. $I_{r0,}$ the minimum initial negative current for ZVS, changes along with the input voltage. Real-time calculation causes heavy calculation burden in the digital controller. To simplify the implementation of I_{r0}, a constant negative reference current I_{ref} along the line cycle is used in this work. According to the analysis above, when the input voltage reaches the peak value V_m, switches need largest negative current to discharge/charge the capacitor. Thus, I_{ref} is selected according to the required minimum negative current when $V_{in} = \pm V_m$,

$$I_{ref} = V_{bus}\sqrt{\frac{C_{eq}}{L_b}(\frac{2V_m}{V_{bus}} - 1)} \tag{3-10}$$

3.2.3 Control implementation and THD reduction

The sensing circuit and control scheme is shown in Fig. 3.10(a). An outer voltage control loop regulates the bus voltage using a PI controller. An inner current control loop regulates instantaneous inductor current to achieve CRM operation. Sensed inductor current (I_{sen}) during the T_{off} period is measured from a sensing resistor R_f placed in the rectifier return path.

Fig. 3.10(b) gives select time domain waveforms describing the current control operation, where G_{s1} and G_{s2} are the logic-level switching signals for each device. During the positive half of the line cycle, S_3 is held on; M_1 and M_2 are switched with variable frequency in CRM. A comparator between $R_f I_{sen}$ and $R_f I_{ref}$ determines the falling edge of G_{S1}. $R_f I_{ref}$ is set to a value less than zero to ensure ZVS is achieved. As discussed before, PLL is implemented to sense input voltage. Accurate zero crossing detection is critical to ensure that no current spike occurs during the transition of input voltage polarity changing.

From Fig. 3.10(b), there is resonant behavior on inductor current I_{Lb} during dead time *dt*. Because of this resonant behavior, the negative peak current I_r is present during the switching dead time. Especially when $V_{bus} >> V_{in}(t)$, this negative current is significant if a constant dead time is implemented. The extra resonant current I_r, alter the input impedance, resulting in distortion of the input current. Fig. 3.11 shows the distorted input current I_{indis} which should be sinusoidal for unity PF as shown by I_{in_ideal}. As seen, near the voltage zero-crossing, this distorted current becomes more obvious and results in increased THD of the input current.

ΔT_{on} compensation is introduced in this work to reduce THD of the input current. Constant T_{on} control based on voltage feedback and variable ΔT_{on} compensation for THD improvement based on line frequency is implemented. This proposed method has the only moderate computational burden and can be implemented in a general DSP.

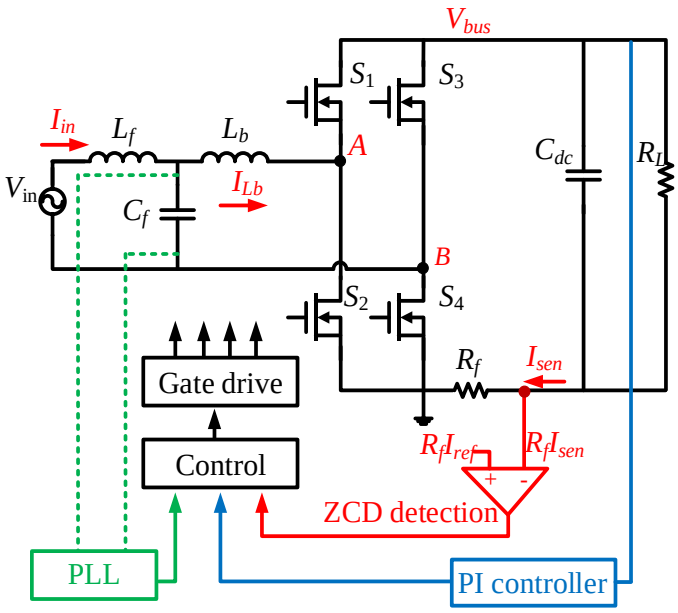
According to the analysis addressed above, the negative current I_r needs to be compensated.

$$I_r = \sqrt{\frac{C_{eq}}{L_b} \cdot [2V_{bus} \cdot (V_m - V_{in}) + {V_{in}}^2]} \tag{3-11}$$

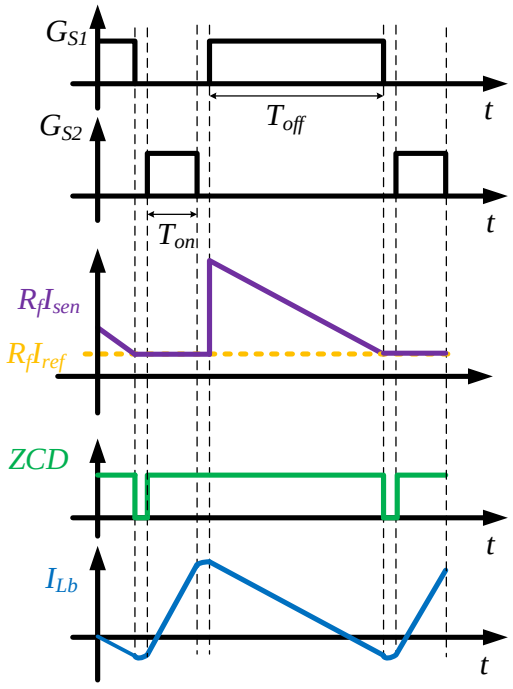
The required additional on-time compensation is

$$\Delta T_{on} = \frac{L_b \cdot I_r}{V_{in}} \tag{3-12}$$

Fig. 3.12 shows the effect of T_{on} compensation on inductor current. The offset I_r is canceled out. Thus, the rectifier input impedance is able to maintain resistive behavior necessary for inherent PFC. Then the ideal input current curve, is shown as a green curve in Fig. 3.11, will be achieved.



(a) Circuit and control diagram of a rectifier



(b) Waveforms at CRM (positive half line period)

Fig. 3.10. Totem-pole rectifier in CRM.

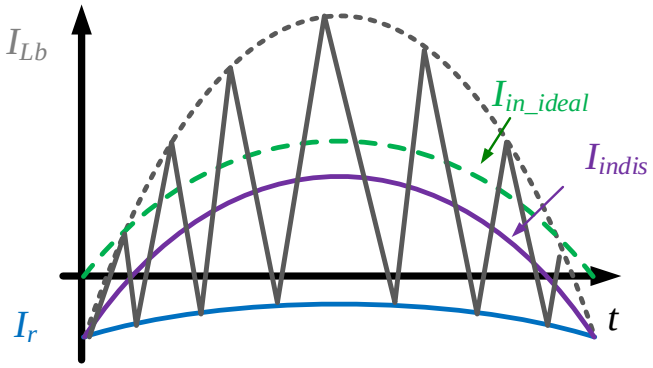


Fig. 3.11. Input current and inductor current with negative current extension for ZVS.

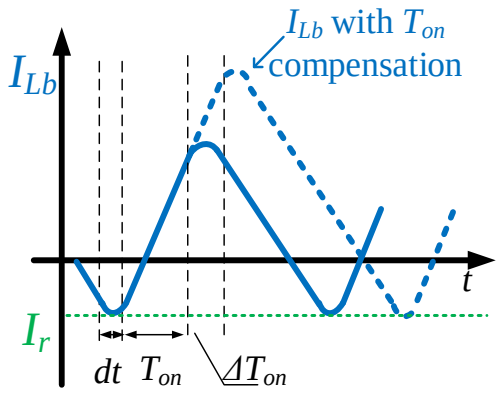


Fig. 3.12 ΔT_{on} compensation for THD improvement.

3.2.4 The current spike issue at the input voltage zero cross

When the input voltage near zero cross point, if S_3 and S_4 cannot turn on/off precisely with the input voltage zero-crossing, there will be a current spike, as shown in Fig. 3.13.

The suppression of the inductor current spike near input voltage zero crossings is a challenge in totem-pole rectifier design. Efforts have been made to discuss this issue and propose solutions. In [16], several control schemes are proposed to adjust switching on-time and frequency near the zero crossing to reduce the current spike issue. However, these control schemes are complicated for practical implementation.

Fig. 3.14 shows the root cause of this issue. Fig. 3.14(a) and (b) present the status of the switches at the positive line period. S_3 remains off while S_4 stays on. When S_2 turns on, the voltage on the inductor is $V_L=V_{in}$, the inductor current increase linearly. When S_1 is on, $V_L = V_{bus} - V_{in}$, the inductor current decreases linearly. The issue will occur when input voltage crosses zero and changes from positive to negative as shown in Fig. 3.14(c) and (d). At this exact point, S_4 should be turned off, and S_4 turned on. However, there are much reasons that might cause S_3 and S_4 to miss the right time for switching. First, the zero cross point of the input voltage may not be sensed correctly due to noise in the sensing circuit. This noise would be significant near the voltage zero-crossing points since the useful signal is too small. Second, a delay occurs in the sensing and control circuit. When the input voltage becomes negative, if S_4 still keeps on, there will be a large inductor current. When S_1 turns on, $V_L = V_{in} + V_{bus}$, which is larger compared to the normal value, either V_{in} or $V_{bus} - V_{in}$. This increased V_L, brings in current spike, as shown in Fig. 3.14(d).

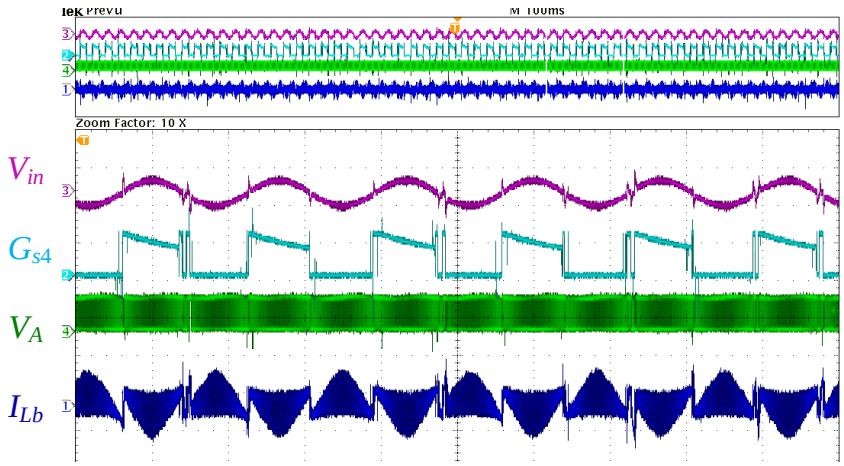


Fig. 3.13. Current spike issue near input voltage zero cross point.

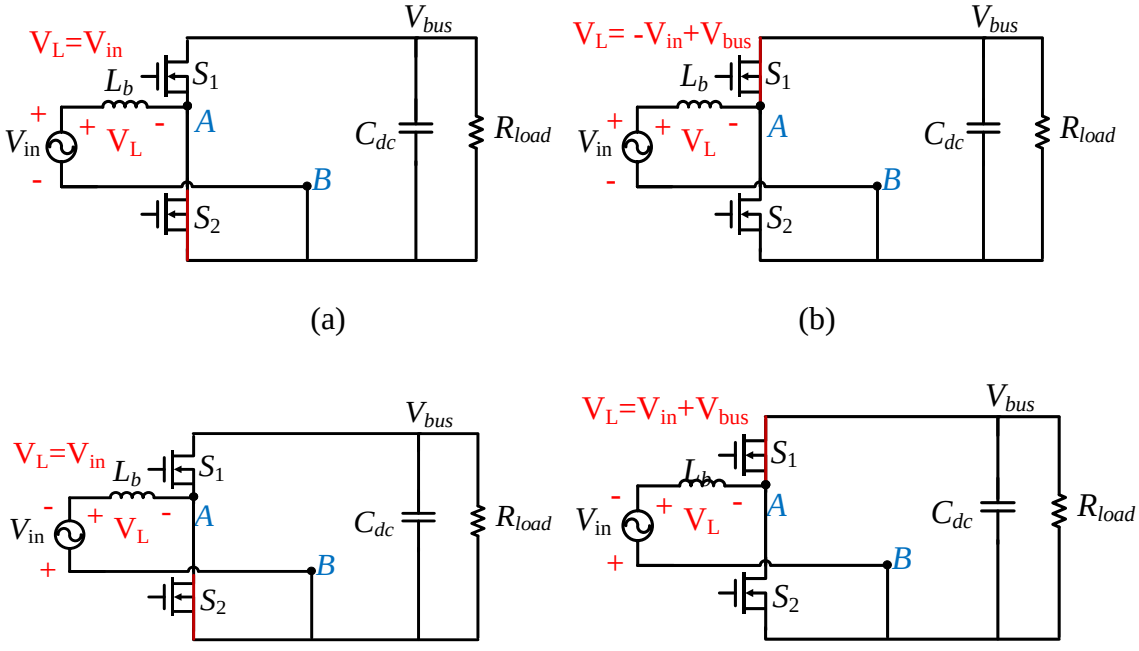


Fig. 3.14. Totem-pole rectifier in CRM.

A phase-locked loop (PLL) is implemented to sense the input voltage and achieve accurate zero crossing detection, therefore increasing the sensing accuracy of the input voltage zero cross point. With input voltage angle information from the PLL, the error in zero crossing point detection is minimal, allowing near-synchronous switching when the input voltage changes polarity. In addition, S_2 is designed to remain on for few switching cycles when the input voltage switches polarity from positive to negative, as shown in Fig. 3.15. When the polarity of input voltage changes from negative to positive, S_1 holds off for a few switching cycles.

3.3 Full bridge resonant inverter

3.3.1 Inverter operation

Following the PFC stage, the second stage high frequency resonant inverter is implemented using a conventional full bridge inverter, 6.78 MHz resonant tanks, and an output filter. The full bridge inverter operates at the 6.78 MHz switching frequency, 50% duty cycle, and 180° phase shift. The gate control signals for S_5~S_8, switching node voltage V_{CD}, and inverter output current I_{Zinv} (assuming a purely resistive load) are shown in Fig. 3.16.

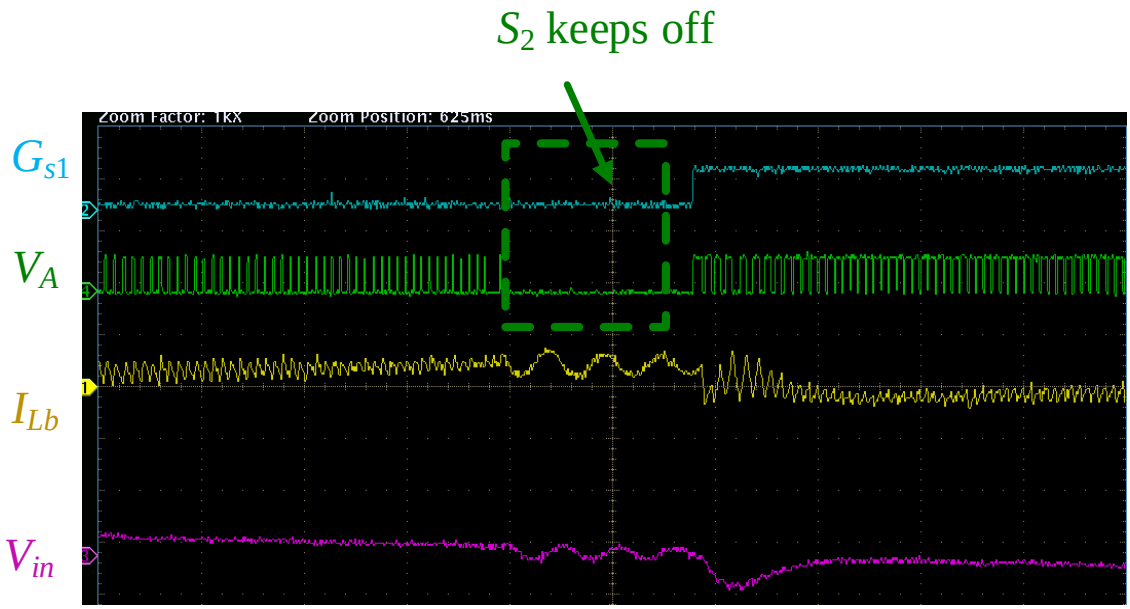


Fig. 3.15. Suppression of the current spike.

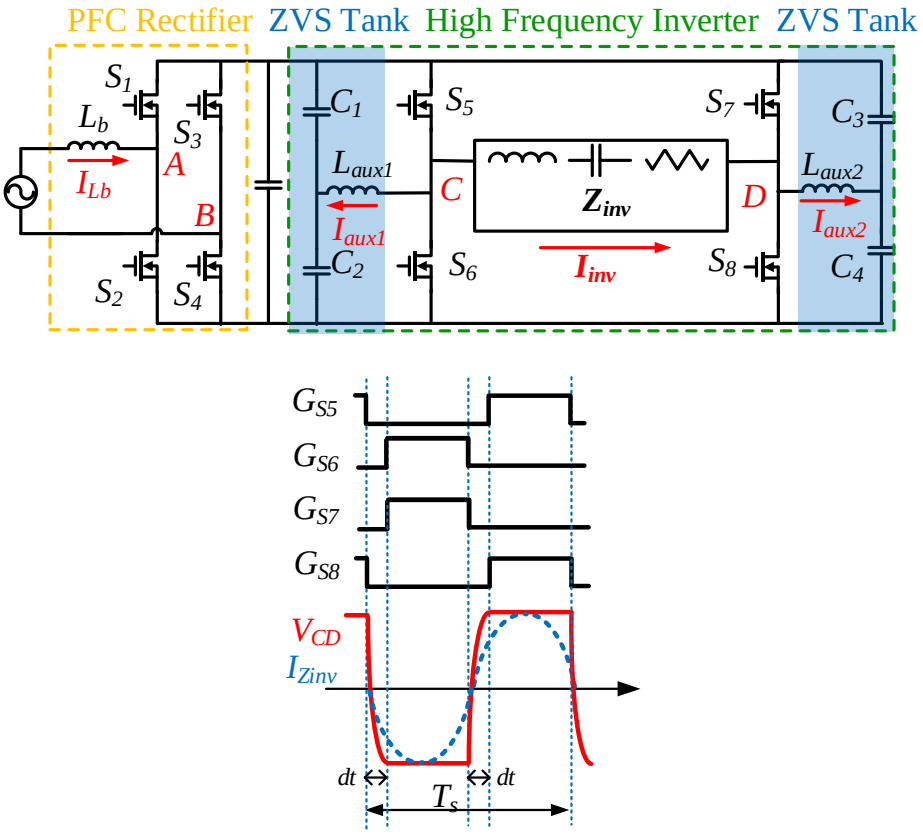


Fig. 3.16. Full bridge operation waveforms.

3.3.2 ZVS tank design

Because S_5~S_8 operate at 6.78 MHz with large bus voltage, any loss of ZVS will result in significant switching loss. A resonant tank is used to ensure soft switching. The tank circuit and auxiliary current waveforms are shown in Fig. 3.17. This ZVS tank provides enough energy to discharge output capacitors of MOSFETs during dead time *dt*, thus obtaining ZVS. So, dead time and ZVS tank are design values interactional design variables. Higher energy stored in ZVS tank reduces discharge time, decreasing the required deadtime. However, with the same current, high energy in ZVS tank indicates either larger auxiliary current or larger inductance that would bring in larger conduction loss. Longer deadtime helps reduce conduction loss but reduces the power delivered to the output simultaneously. Thus, based on equivalent output capacitance of MOSFETs, rated bus voltage, switching frequency and duty cycle, dead time and ZVS tank are adjusted to obtain the highest efficiency at full power.

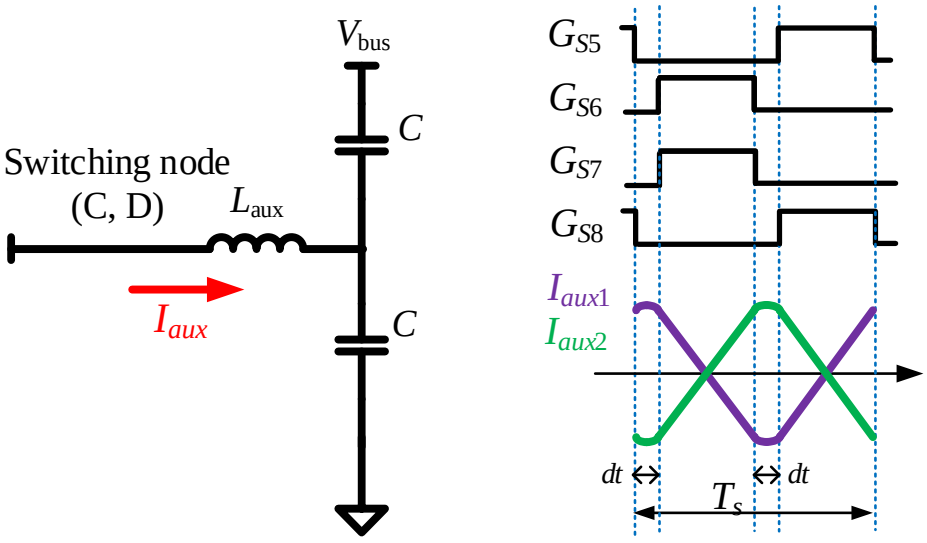


Fig. 3.17. ZVS tank and waveforms.

3.3.3 Device selection

Since soft switching is employed in this high frequency resonant inverter, the soft switching figure of merit (FOM) has been used to assess available devices [167]. In the ZVS operation, the output charge Q_{oss} can be recovered. However, Q_{oss} determines the amplitude of the required circulating current. Higher Q_{oss} requires higher current. So, the FOM of the soft switching can be used to assess available the device.

$$FOM = \frac{1}{R_{on} \cdot Q_{oss}} \tag{3-13}$$

In this work, seven devices including 4 Si FETs and 3 GaN FETs, are compared for device selection.

Fig. 3.18 shows the C_{oss} curves from the datasheets. Two Si devices (STD7N65M2 and TK5P60W) are out of the plot range. Thus they are not shown in the figure. Fig. 3.19 shows the devices with R_{on} and the Q_{oss}. Table 3.6 gives the equivalent capacitance based on charge C_{eqQ}, Q_{oss}, R_{on} and FOM of the seven devices based on 200 V voltage which is the bus voltage of the inverter.

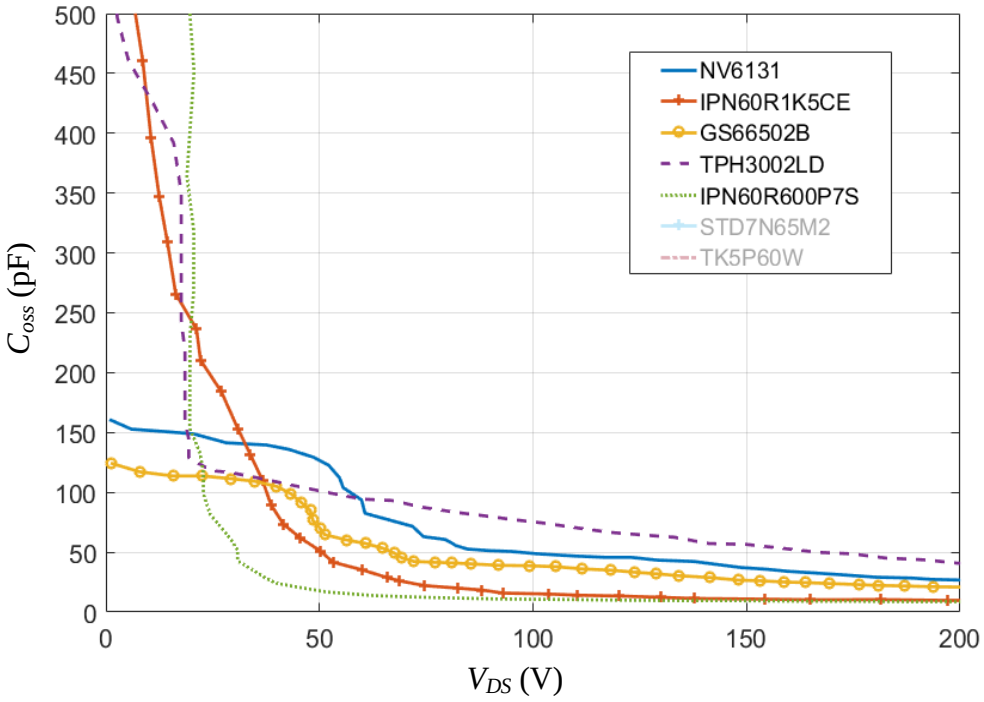


Fig. 3.18. C_{oss} curves vs V_{ds}.

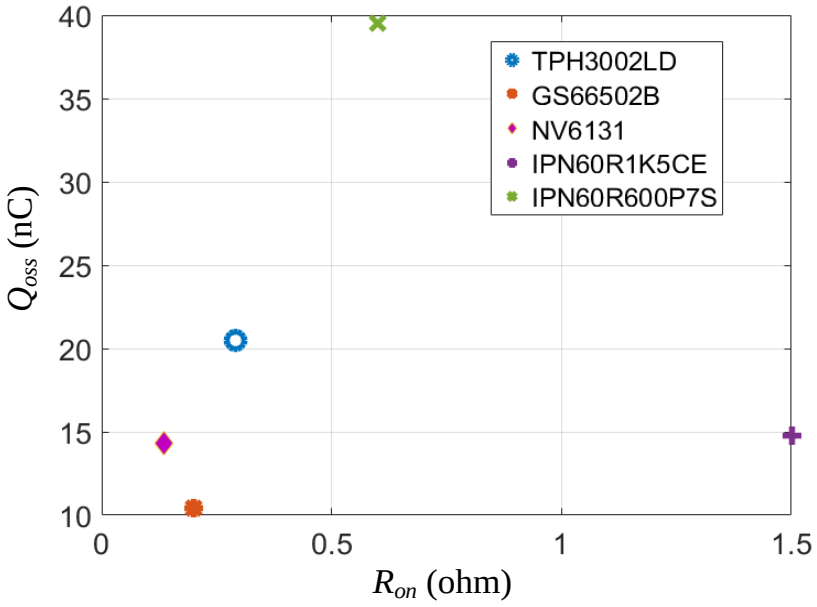


Fig. 3.19. FOM of five candidates.

TABLE 3.6 DEVICES COMPARISON AT V_{DS}=200 V

Devices	Technology	C_{eqQ} (pF)	Q_{oss} (nC)	R_{on}(mΩ)	FOM
TPH3002LD	GaN	103	20.5	0.29	0.17
GS66502B	GaN	52.2	10.4	0.2	0.48
NV6163	GaN	71	14.3	0.135	0.52
IPN60R1K5CE	Si	73.8	14.8	1.5	0.045
IPN60R600P7S	Si	198	39.5	0.6	0.04
STD7N65M2	Si	1651	330	1.15	0.003
TK5P60W	Si	3156	631	0.77	0.002

As shown, GS66502B and NV6131 have competitive FOM. NV6131 has lower R_{on} and GS66502B has smaller Q_{oss}. The selection of device should be determined by the specific design. If the current conducted in the devices is quite large, and the switching frequency or/and the voltage is low, then the device with small R_{on} should be adopted. So, loss model should be built to guide the selection of devices.

3.4 Impedance matching network for constant current output behavior

The design of the IMN is investigated for the two-stage transmitter application. The targets of this IMN include:

- Provide low reactive power, and be insensitive to the coupling coefficient change and load change.
- Provide constant current for multiple receiver application.
- Suppress harmonic current

3.4.1 Basic compensation network

In this section, these four basic networks are investigated for the IMN design.

A. SS compensation network

Fig. 3.20 shows the SS compensation circuit, where R_p and R_s are the ESR of the transmitter coil and receiver coil respectively. The impedance of receiver is Z_s

$$Z_s = j\omega L_s + \frac{1}{j\omega L_s} + R_s + Z_L \tag{3-14}$$

If Z_s is reflected to the transmitter side, the equivalent load impedance of transmitter is

$$Z_{pa} = j\omega L_p + \frac{1}{j\omega C_p} + R_p + \frac{(\omega M)^2}{Z_s} \tag{3-15}$$

If L_s and C_s are chosen such that

$$f_s = \frac{1}{2\pi\sqrt{L_s C_s}} \tag{3-16}$$

Assume R_s=R_p≈0. Then (3-15) becomes

$$Z_{pa} = j\omega L_p + \frac{1}{j\omega C_p} + \frac{(\omega M)^2}{Z_L} \tag{3-17}$$

The selection of compensation is determined by the application and the specific requirements. To get zero phase angle at the output of the transmitter is one design approach for minimizing reactive power rating. In this case, the primary capacitance is deliberately designed to compensate both the primary self-inductance and the reflected impedance. This forces the zero phase angle frequency of the load model to equal the secondary resonant frequency. The zero phase angle analysis for Z_{pa} is based on the resistive load Z_L.

To get zero phase angle, the compensation capacitor of transmitter C_p is

$$C_p = \frac{L_s C_s}{L_p} \tag{3-18}$$

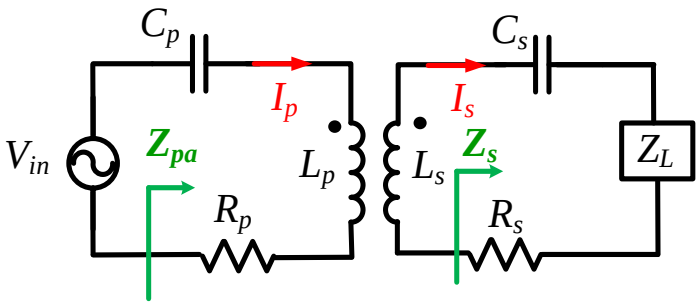


Fig. 3.20. SS compensation network.

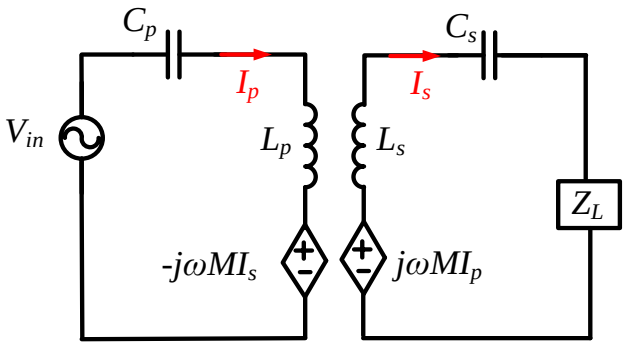


Fig. 3.21. M model of SS circuit.

According to (3-18), C_p is independent of mutual inductance and load. Therefore, SS is not sensitive to the load and coupling coefficient. It is widely used in these areas that experience dynamic load changing or/and position changing due to this feature.

Fig. 3.21 shows the *M* model of SS compensation network. Then receiver output current I_s is:

$$I_s = j\frac{V_{in}}{\omega M} \tag{3-19}$$

I_s is load independent. Considering a fixed *M*, I_s will be a constant current source.

B. SP compensation network

Fig. 3.22 shows the SP compensation circuit. The impedance of receiver is Z_s

$$Z_s = R_s + j\omega L_s + \frac{Z_L}{1 + j\omega C_s Z_L} \tag{3-20}$$

The equivalent load impedance of the transmitter is

$$Z_{pa} = j\omega L_p + \frac{1}{j\omega C_p} + R_p + \frac{(\omega M)^2}{Z_s} \tag{3-21}$$

Considering R_s=R_p≈0, Z_s is simplified to:

$$Z_s = \frac{Z_L + j\omega[C_s Z_L^2 + L_s + L_s(\omega C_s Z_L)^2]}{1 + (\omega C_s Z_L)^2} \tag{3-22}$$

According to (3-22), Z_s must be inductive if Z_L is a pure resistor. If the resonant frequency of L_s and C_s is f_s, Z_s becomes:

$$Z_s = \frac{Z_L + j\omega L_s}{1 + (\omega C_s Z_L)^2} \tag{3-23}$$

Z_{pa} is then:

$$Z_{pa} = j\omega L_p + \frac{1}{j\omega C_p} + \frac{(\omega M)^2(1 + j\omega C_s Z_L)}{j\omega L_s - \omega^2 C_s L_s Z_L + Z_L} \tag{3-24}$$

$$= j\omega L_p + \frac{1}{j\omega C_p} + \frac{(\omega M)^2(1 + j\omega C_s Z_L)}{j\omega L_s} \tag{3-25}$$

$$= j\omega L_p - j\frac{1}{\omega C_p} - j\frac{(\omega M)^2}{\omega L_s} + \frac{(\omega M)^2 C_s Z_L}{L_s} \tag{3-26}$$

To achieve a unity power factor of transmitter output current, the compensation capacitance at the transmitter side should be

$$C_p = \frac{C_s L_s^2}{L_s C_s - M^2} \tag{3-27}$$

C_p is related to the mutual inductance. When the coupling coefficient changes, the resonant frequency also changes. Z_{pa} changes along with M^2, thus SP is sensitive to variable position (misalignment).

Fig. 3.23 shows the M model of SP compensation network. When C_p satisfies (3-27) , I_p is:

$$I_p = \frac{V_{in} L_s^2}{M^2 Z_L} \tag{3-28}$$

The secondary circuit can be simplified as Fig. 3.24. The load voltage V_o is

$$V_o = j\omega M \frac{V_{in} L_s^2}{j\omega L_s M^2 Z_L} \cdot Z_L = \frac{V_{in} L_s}{M} \tag{3-29}$$

As seen, the output voltage is independent of load Z_L. The secondary acts as a voltage source.

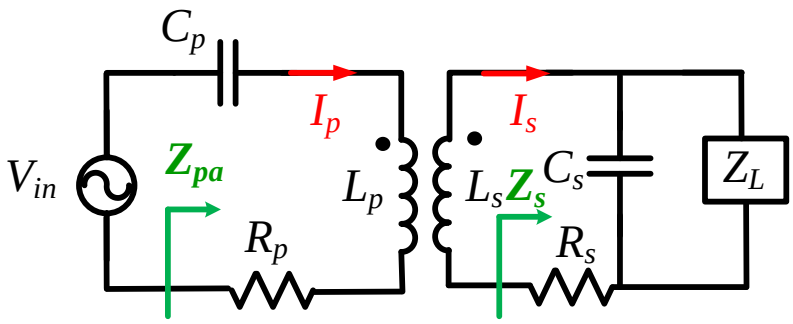


Fig. 3.22. SP compensation network.

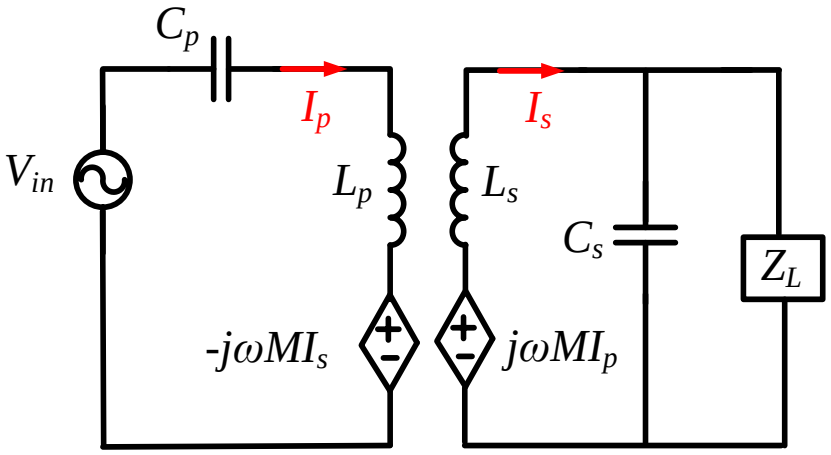


Fig. 3.23. M model of SP circuit.

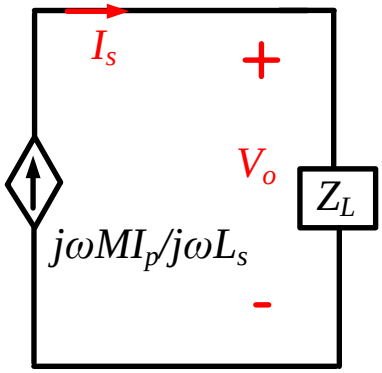


Fig. 3.24. The equivalent circuit of the secondary side.

C. PS compensation network

Fig. 3.25 shows the PS compensation circuit. The impedance of receiver is Z_s

$$Z_s = j\omega L_s + \frac{1}{j\omega C_s} + R_s + Z_L \tag{3-30}$$

The equivalent load impedance of the transmitter is

$$Z_{pa} = \frac{1}{\frac{1}{R_p + j\omega L_p + \frac{(\omega M)^2}{R_s + Z_L + j\omega L_s + \frac{1}{j\omega C_s}}} + j\omega C_p} \tag{3-31}$$

The resonant frequency of L_s and C_s is f_s, then

$$Z_s = Z_L \tag{3-32}$$

Furthermore, Z_{pa} is

$$Z_{pa} = \frac{1}{\frac{1}{j\omega L_p + \frac{(\omega M)^2}{Z_L}} + j\omega C_p} \tag{3-33}$$

$$= \frac{j\omega L_p Z_L + (\omega M)^2}{Z_L - \omega^2 L_p C_p Z_L + j\omega C_p (\omega M)^2} \tag{3-34}$$

$$= \frac{\left[j\omega L_p Z_L + (\omega M)^2\right] \cdot \left[Z_L - \omega^2 L_p C_p Z_L - j\omega C_p (\omega M)^2\right]}{(Z_L - \omega^2 L_p C_p Z_L)^2 + (\omega C_p (\omega M)^2)^2} \tag{3-35}$$

$$= \frac{j\omega L_p Z_L \left(Z_L - \omega^2 L_p C_p Z_L\right) - j\omega C_p (\omega M)^4 + (Z_L - \omega^2 L_p C_p Z_L)(\omega M)^2 + \omega^2 C_p L_p Z_L (\omega M)}{(Z_L - \omega^2 L_p C_p Z_L)^2 + (\omega C_p (\omega M)^2)^2} \tag{3-36}$$

To get zero phase angle of the transmitter output current, C_p is derived according to

$$j\omega L_p Z_L \left(Z_L - \omega^2 L_p C_p Z_L\right) - j\omega C_p (\omega M)^4 = 0 \tag{3-37}$$

Then

$$C_p = \frac{L_p Z_L^2}{L_p^2 Z_L^2 \omega^2 + (\omega M)^4} = \frac{L_p Z_L^2}{L_p^2 Z_L^2 C_s L_s + L_s^2 C_s^2 M^4} \tag{3-38}$$

The achievement of the unity phase angle of PS is related to the variable mutual inductance and load. But it is less sensitive than SP according to (3-36). Another limitation of PS is that it requires the current source to drive it. From the schematic, if placing a voltage source parallel with C_p, then the paralleled resonant tank L_p and C_p are considered as an open circuit.

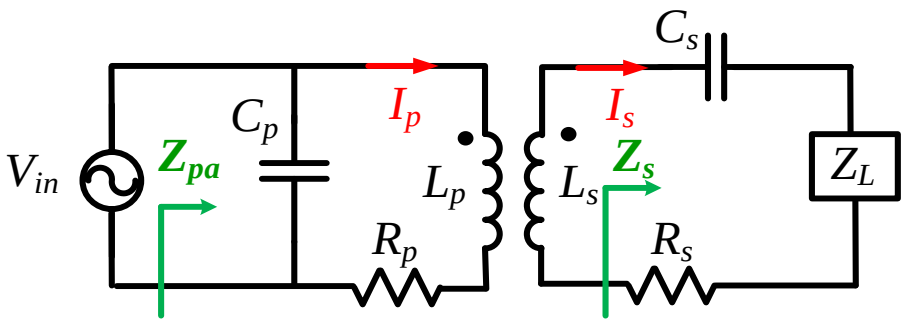


Fig. 3.25. PS compensation network.

D. PP compensation network

Fig. 3.26 shows the PS compensation circuit. The impedance of receiver is Z_s

$$Z_s = R_s + j\omega L_s + \frac{Z_L}{1 + j\omega C_s Z_L} \tag{3-39}$$

The equivalent load impedance of the transmitter is

$$Z_{pa} = \frac{1}{\dfrac{1}{R_p + j\omega L_p + \dfrac{(\omega M)^2}{R_s + j\omega L_s + \dfrac{Z_L}{1 + j\omega C_s Z_L}}} + j\omega C_p} \tag{3-40}$$

The resonant frequency of L_s and C_s is f_s, then

$$Z_s = \frac{Z_L + j\omega L_s}{1 + (\omega C_s Z_L)^2} \tag{3-41}$$

Furthermore, Z_{pa} is

$$Z_{pa} = \frac{1}{\frac{1}{j\omega L_p + \frac{j\omega L_s(\omega M)^2}{1 + j\omega C_s Z_L}} + j\omega C_p} \tag{3-42}$$

To get zero phase angle of transmitter output current,

$$C_p = \frac{(L_P L_s - M^2) C_s L_s^2}{\frac{M^2 C_s Z_L}{L_s} + (L_P L_s - M^2)^2} \tag{3-43}$$

The same as PS, PP can only be driven by a current source.

From the analysis, SS compensation network is the most insensitive to the load and coupling coefficient for unity phase angle requirement (low reactive power). It is beneficial for the application where load or the coupling coefficient frequently changes.

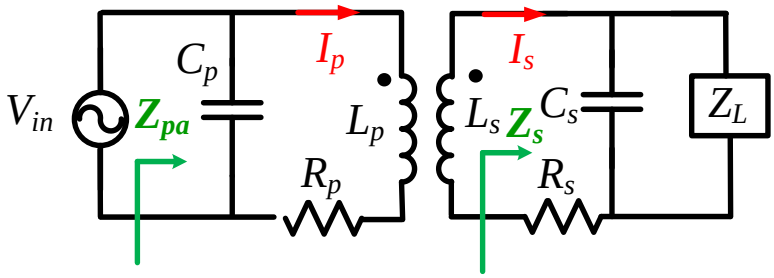


Fig. 3.26. PP compensation network.

3.4.2 Multiple receivers charging application

In the application of single transmitter charging *n* receivers simultaneously, the receiver coil is significantly smaller than the transmitter coil, resulting in loose coupling. The coupling coefficient *k* is typically less than 0.5 [16]. Fig. 3.27(a) gives the simplified circuit of a multi-receiver resonant WPT system with series-series (SS) compensation. The relationships between V_{pa} and the coil currents (I_p, I_{si}, i=1..n) is given by

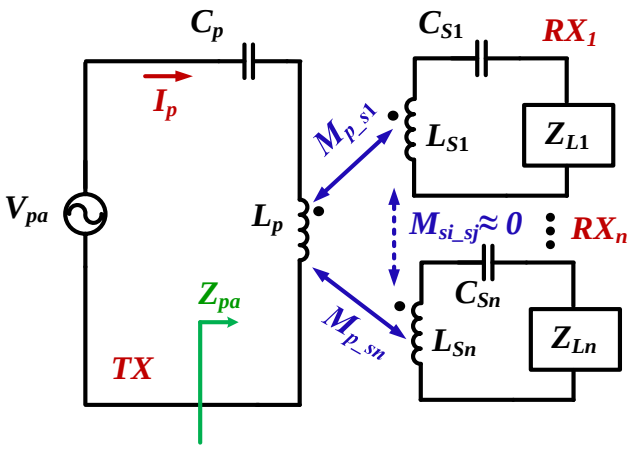
$$\begin{bmatrix} V_{pa} \\ 0 \\ \vdots \\ 0 \end{bmatrix} = \begin{bmatrix} R_p & j\omega M_{p\_s1} & \dots & j\omega M_{p\_sn} \\ j\omega M_{p\_s1} & R_{s1} + Z_{L1} & \dots & j\omega M_{s1\_sn} \\ \vdots & \vdots & \vdots & \vdots \\ j\omega M_{p\_sn} & j\omega M_{s1\_sn} & \dots & R_{sn} + Z_{Ln} \end{bmatrix} \begin{bmatrix} I_p \\ I_{s1} \\ \vdots \\ I_{sn} \end{bmatrix} \tag{3-44}$$

Considering no overlap among the receivers, the mutual couplings within RX_n are negligible. With M_{si_sj}=0, (i,j=0..n), (3-44) is

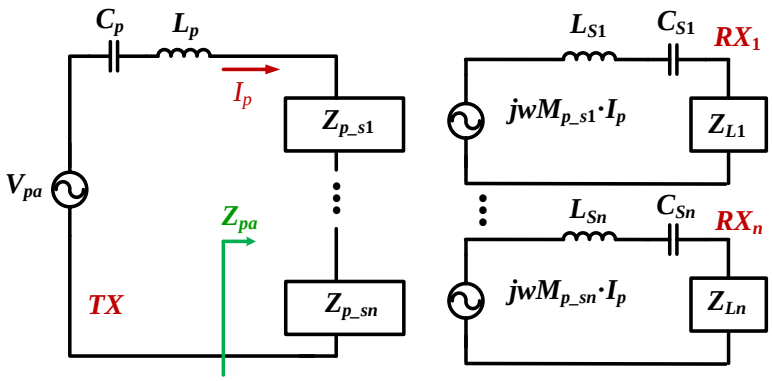
$$\begin{bmatrix} V_{pa} \\ 0 \\ \vdots \\ 0 \end{bmatrix} = \begin{bmatrix} R_p & j\omega M_{p\_s1} & \dots & j\omega M_{p\_sn} \\ j\omega M_{p\_s1} & R_{s1} + Z_{L1} & \dots & 0 \\ \vdots & \vdots & \vdots & \vdots \\ j\omega M_{p\_sn} & 0 & \dots & R_{sn} + Z_{Ln} \end{bmatrix} \begin{bmatrix} I_p \\ I_{s1} \\ \vdots \\ I_{sn} \end{bmatrix} \tag{3-45}$$

(3-45) is solved for Z_{pa}, which is the equivalent load of the transmitter. Z_{pa} is the sum of *n* reflected loads of the *n* receiver side $Z_{p\_sn}=\omega^2 M^2_{p\_sn}/(R_{sn}+Z_{Ln})$. According to (3-46), Z_{p_si} are placed in series as shown in the Fig. 3.27(b). If the output current of transmitter I_p remains constant, the power delivered to each load is independent of the presence or loading conditions of other receivers. Therefore, constant output current behavior is superior to voltage source behavior in this multiple receiver application.

$$Z_{pa} = \frac{V_{pa}}{I_p} = R_p + \frac{\omega^2 M^2_{p\_s1}}{R_{s1} + Z_{L1}} + \cdots + \frac{\omega^2 M^2_{p\_sn}}{R_{sn} + Z_{Ln}} = R_p + Z_{p\_s1} + \cdots + Z_{p\_sn} \tag{3-46}$$



(a)



(b)

Fig. 3.27. The equivalent circuit of a single transmitter with multiple receivers.

3.4.3 IMN design for the constant output current behavior

According to section 3.4.1, the compensation network will be designed based on SS network as shown in Fig. 3.28. C_s and L_s are designed to resonate at 6.78 MHz, same as C_p and L_p. Under this condition, if Z_L is a resistive load, Z_{Pa} will always be resistive. When reflecting the primary side, the output network of the transmitter is simplified as Fig. 3.29(a). In practice, in order to suppress common mode noise from the asymmetric circuit, all of these components in the IMN are split into two identical ones as shown in Fig. 3.29(b), where L_{x_1}=L_{x_2}=0.5 L_x, C_{x_1}=C_{x_2}=2 C_x.

According to section 3.4.2, the constant current behavior is preferred at the output of the transmitter. To obtain constant I_p, the basic compensation network is not enough. Therefore, another network including resonant tank L_r and C_r, a T-type filter L_{f1}, $L_{f2,}$ C_f are added. In this section, the compensation network indicates SS network, and IMN refers to the L_r, C_r, L_{f1}, L_{f2} and C_f.

According to KVL and KCL, the inverter output impedance Z_{inv} is

$$Z_{inv} = \frac{(Z_{pa} + Z_{lf2})Z_{cf}}{Z_{pa} + Z_{lf2} + Z_{cf}} + Z_{lf1} + Z_{lr} + Z_{cr} \tag{3-47}$$

Since L_r and C_r are tuned to resonate at 6.78 MHz, the impedance at the resonant frequency is zero, $\mathrm{Z_{lr}} + \mathrm{Z_{cr}} = 0$. The T-type filter is designed as L_{f1}=L_{f2}= L_f, and the resonant frequency of L_f and C_f is 6.78 MHz. So, at this frequency,

$$Z_{lf1} = Z_{lf2} = Z_{lf} \tag{3-48}$$

$$Z_{cf} = -Z_{lf} \tag{3-49}$$

when plugged into (3-47), simplifies the inverter impedance to

$$Z_{inv} = \frac{(Z_{lf})^2}{Z_{pa}} \tag{3-50}$$

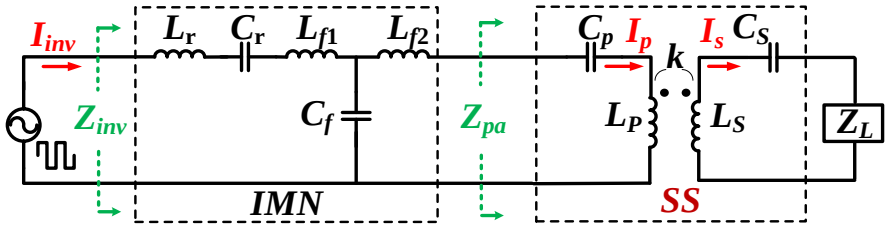
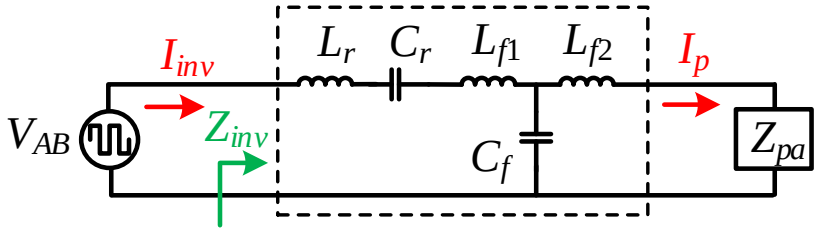
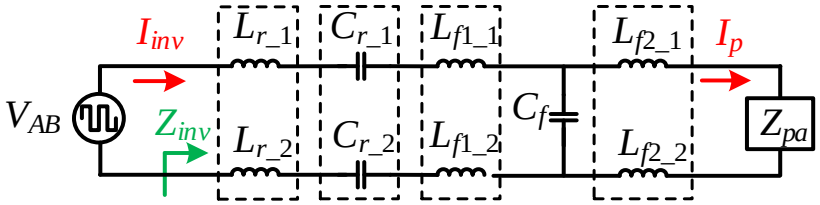


Fig. 3.28. The compensation network.



(a)



(b)

Fig. 3.29. Output network of the inverter.

With a constant V_{ab1}, the transmitter coil current is

$$I_p = \frac{V_{ab1}}{\sqrt{2}Z_{lf}} \tag{3-51}$$

Thus, I_p is independent of load Z_{pa}, and the constant current source is ensured with a constant V_{ab1}. L_r and L_{f1} can be combined into a single inductor, the same as L_{f2} and L_p.

Since the derivation of constant I_p is based on fundamental harmonic analysis, unattenuated harmonics beyond the fundamental may degrade the constant behavior of I_p. The resonant tank L_r and C_r are designed to attenuate the other harmonics. The conversion ratio between the transmitter coil current I_p and V_{AB} is defined as $g(f)=I_p/V_{AB}$. To address the attenuation of harmonic content, the normalized conversion ratio $g_n(f) = g(f)/g(f_s)$ plotted in Fig. 3.30 for varying L_r. From the plots, $g_n(f_s)=1$ indicates all the fundamental content passes through the network. The lower value of $g_n(f)$ at other frequency presents effective attenuation. Larger L_r provides higher attenuation at 2nd, 3rd and 5th harmonic as shown in Fig. 3.30. However, larger L_r leads to higher inductor volume and/or higher power loss according to the inductor loss model in Chapter 4. In this work, L_r is finally selected as 19.68 μH to obtain higher than 97% attenuation at the high order harmonics, while maintaining its loss below 15% of the converter loss. After L_r is determined, C_r is calculated to maintain resonance at f_s.

With these designed parameters, a simulation verifies the constant current behavior at the output of the transmitter as shown in Fig. 3.31. I_{in} (the blue waveform)changes in accordance with load, while I_p (the green waveform) maintains constant for the varied load.

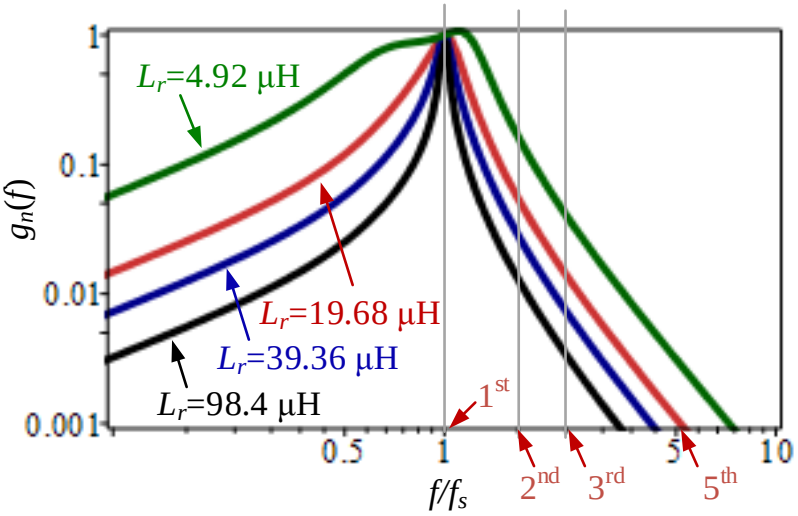


Fig. 3.30. Transfer gain with different L_r.

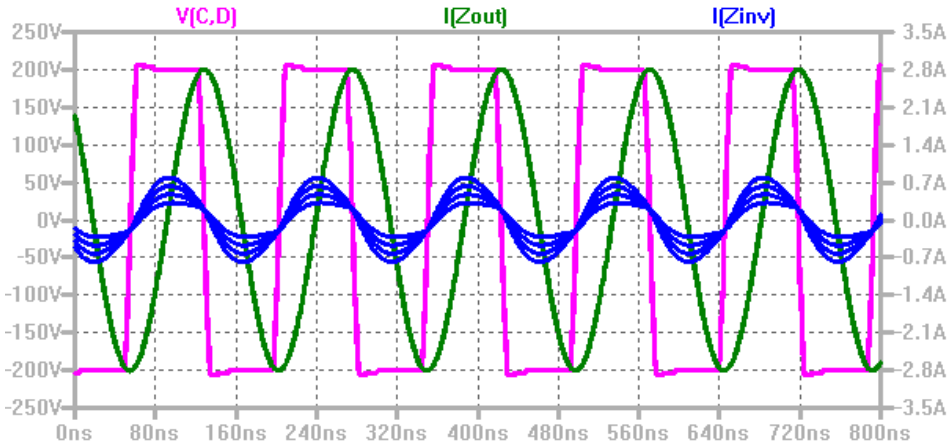


Fig. 3.31. Simulation verification for the inherent current source behavior.

3.5 Experimental verification

Prototypes of both rectifier and inverter are constructed to verify the two-stage power WPT transmitter. The main design parameters are listed in TABLE 3.7 Prototypes are shown in Fig. 3.32. For all experimental results, the DSP controller development board and all auxiliary voltage rails, including the gate driver supplies, are powered from a benchtop voltage source. Power supplied from this source is not included in measured efficiency, but is approximately 1W during operation.

The rectifier power efficiency is measured up to 100 W, shown in Fig. 3.33. The power stage efficiency at full load is 98.6%. Measured waveforms are shown in Fig. 3.34 for operation at full output power, P_o=100 W.

Measured THD of the input current is 4.5% and PF is 0.99. THD is defined

$$THD = \frac{\sqrt{I_2^2 + I_3^2 + \cdots + I_n^2}}{I_1} \tag{3-52}$$

where *n* indicates orders of harmonic current. Measured input current has slight distortion near the input voltage zero crossing period. As discussed in the last section, variable T_{on} compensation is implemented to improve THD. According to theoretic compensation, ΔT_{on} is infinite near the input voltage zero crossing; practically, the implementation of large ΔT_{on} results in ringing between the boost inductor and the input EMI filter. This ringing is shown in inductor current at zero crossing periods in Fig. 3.34. Thus an upper limit for ΔT_{on} is set in DSP to minimize experimental THD.

TABLE 3.7 PARAMETER OF PROTOTYPE

Description	Symbol	Value
Input voltage	V_i	120V/60Hz
Bus voltage	V_{bus}	200V
Load power	P_o	100W
Switching frequency of rectifier	f_{s_rec}	10k~400kHz
Switching frequency of inverter	f_{s_inv}	6.78MHz
MOSFETs used in rectifier	$M_1 \sim M_4$	THP3002LD
Digital signal processor	DSP	TMS320F28069

Fig. 3.32. A prototype of the two-stage transmitter.

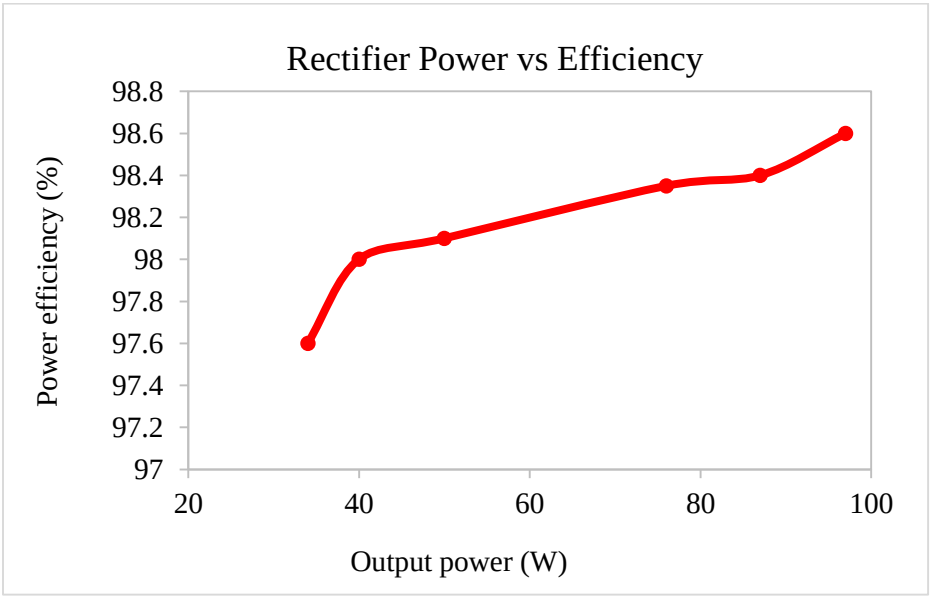


Fig. 3.33. Experimental rectifier power efficiency

Fig. 3.35 shows measured power efficiency of the full bridge inverter together with an output filter. The system is operated with V_{bus} = 200 V and f_s = 6.78 MHz. The efficiency at full power is 93%. The switching node voltage waveform V_{CD}, shown in Fig. 3.36, demonstrates that soft switching is achieved.

The load impedance is varied and the output current is measured to verify constant output current behavior. Fig. 3.36 gives inverter waveforms for a load impedance of 15 Ω and 30 Ω. These impedances represent 50 W and 100 W output power, respectively. RMS inverter output current changes from 0.27 A to 0.51 A, but output current I_{Zout_rms} only varies by 0.02 A, from 1.83 A to 1.81 A. Further verification of constant current behavior is given in Fig. 3.37, which shows the RMS output current as load impedance is changed from 5 Ω to 30 Ω. In this range, which spans 15 W to 100 W output power, the change in RMS current is less than 1%.

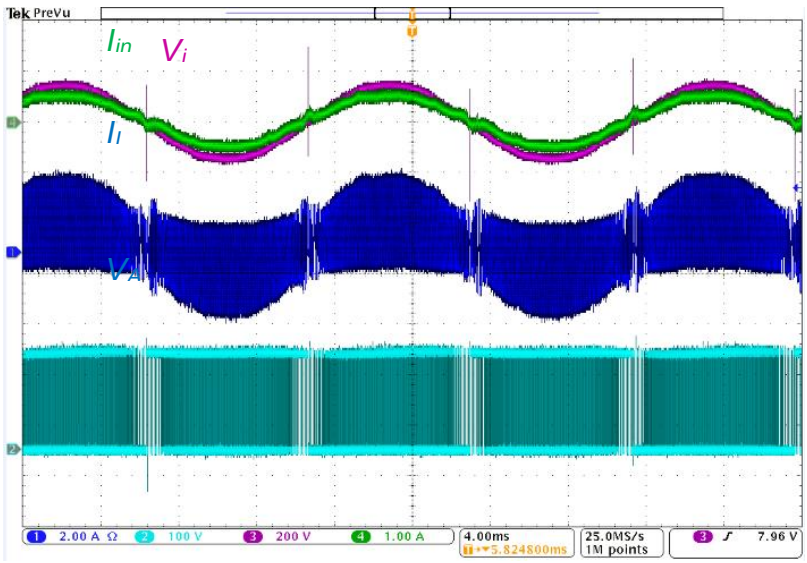


Fig. 3.34. Experimental rectifier waveforms.

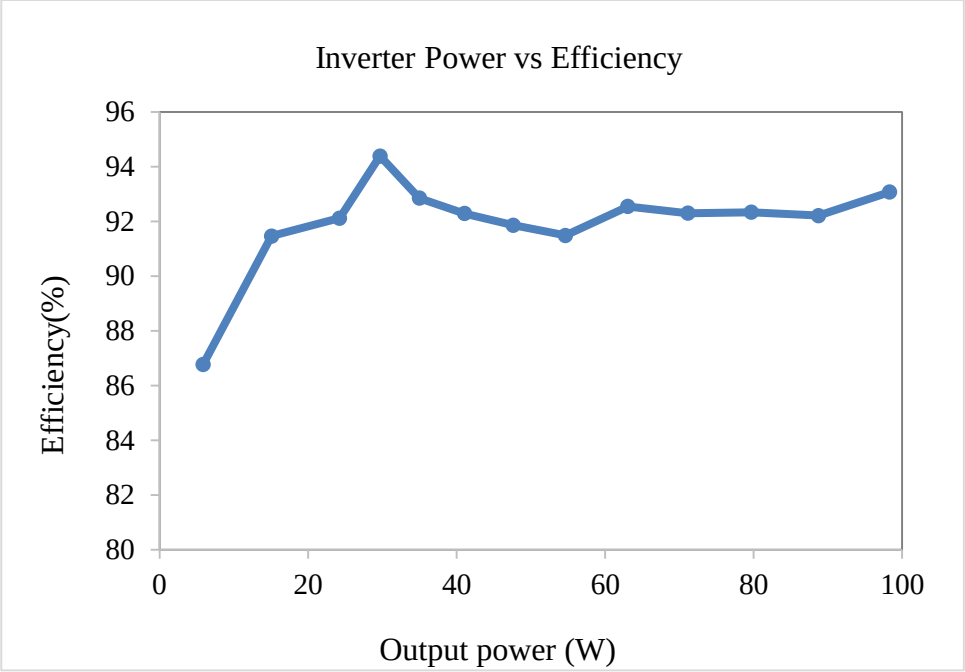
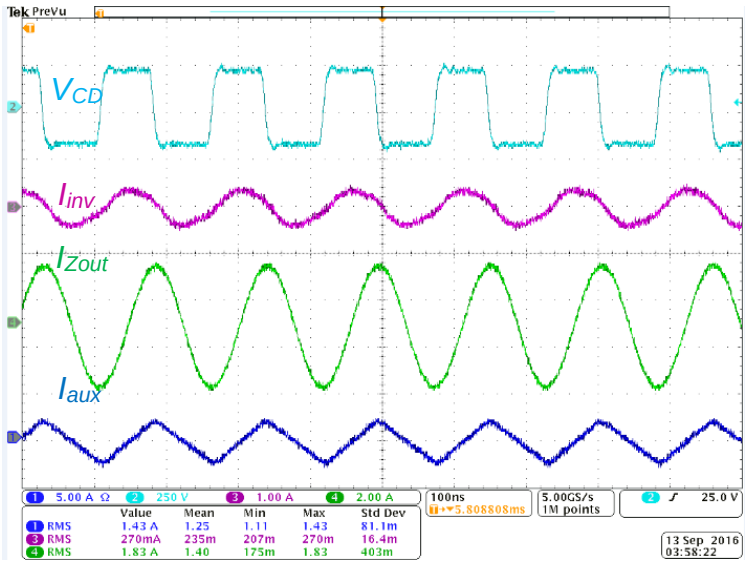
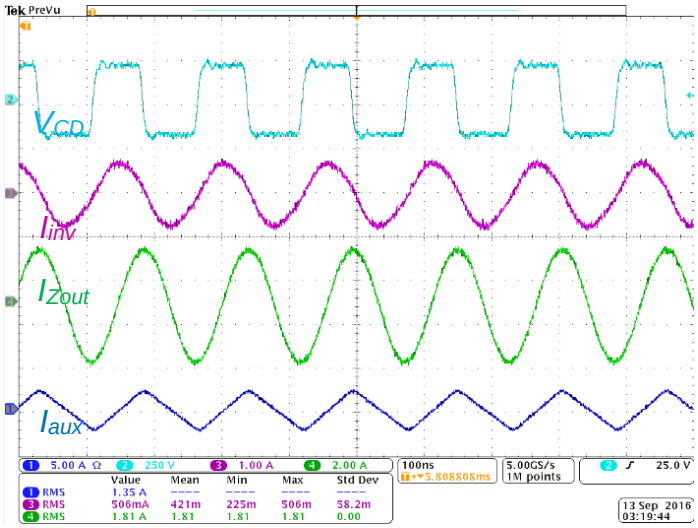


Fig. 3.35. Experimental inverter power efficiency.



(a) Waveforms at Z_{out}=15Ω



(b) Waveforms at Z_{out}=30Ω

Fig. 3.36. Experimental inverter waveforms for constant current behavior verification.

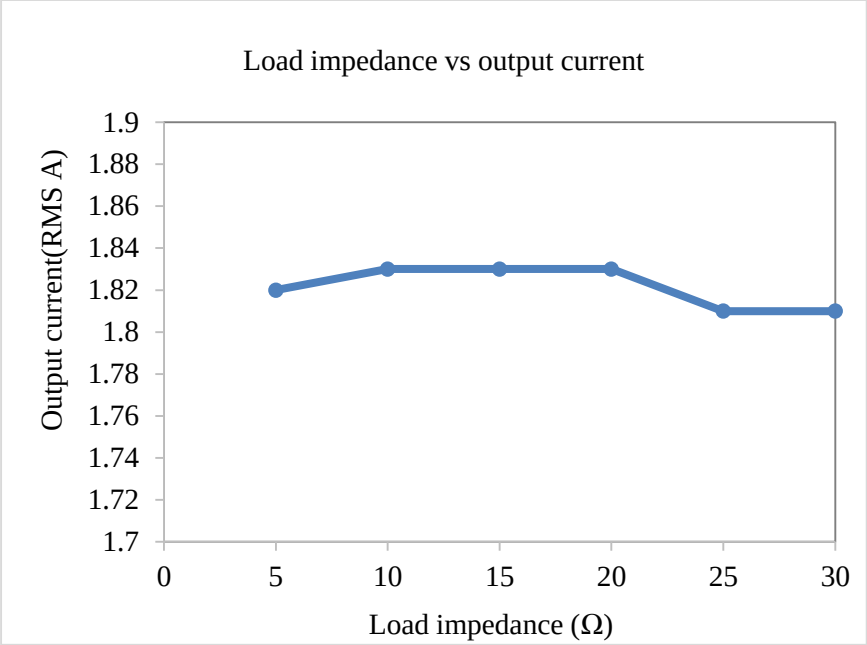


Fig. 3.37. Experimental results for constant current behavior verification.

3.6 Summary

This thesis proposes a two-stage ac/RF WPT transmitter with inherent current source behavior. By implementing a front-end totem pole rectifier with soft switching, high power efficiency is achieved. Via variable T_{on} time compensation, low THD and high PF are obtained. A 6.78MHz resonant inverter with inherent current source behavior is designed by implementing an output filter network capable of producing constant current across varying load impedance. A 100W two-stage prototype is built to verify the theoretical analysis. ZVS is achieved along the full line cycle with the simplified negative current design. Experimental results demonstrate 98.6% and 93% power efficiency of rectifier and inverter, respectively, at 100W. The overall power efficiency of this two-stage ac/RF converter under full power is 91.7%. With the T_{on} compensation method, 4.5 % THD and 0.99 PF are achieved. The constant current behavior is also verified.

4 SINGLE-STAGE TRANSMITTER DESIGN

Chapter 3 has discussed a two-stage transmitter that has achieved high power efficiency with fewer components count.In this chapter, a single-stage transmitter for the medium power application (100 W) is investigated. The WPT system with this single-stage transmitter is shown in Fig. 4.1. This single-stage transmitter is designed to achieve:

- Obtain high power efficiency with lower component count than the two-stage transmitter.
- Integrate the ac-dc rectifier and dc-ac resonant inverter into a single stage.
- Exhibit small double line frequency ripple on the dc bus voltage, simultaneous input PFC and output power regulation.
- Be capable of charging multiple devices.

4.1 Single-stage transmitter

The single-stage transmitter shown in Fig. 4.2(a) is derived from the two-stage transmitter which is discussed in Chapter 3. By integrating the fast switching phase leg of the rectifier and one phase leg of the full bridge resonant inverter, this single-stage transmitter is obtained, as shown in Fig. 4.2(a). Components L_b, D_1, D_2, phase leg A (S_1 and S_2) form a bridgeless totem-pole PFC rectifier. Phase leg B (S_3 and S_4) cooperates with phase leg A to generate a 6.78 MHz ac output current I_{inv}. As seen, phase leg A is shared by the rectifier and the inverter and provides functionality for both. Z_{inv} models the equivalent load of the inverter that includes IMN, transmitting coils, and receiver of the WPT, as shown in Fig. 4.2(b). L_{zvsa}, $C_{1,}$ and C_2 are the zero voltage switching (ZVS) tank to help S_1 and S_2 achieve soft switching; L_{zvsb}, $C_{3,}$ and C_4 have the same purpose for S_3 and

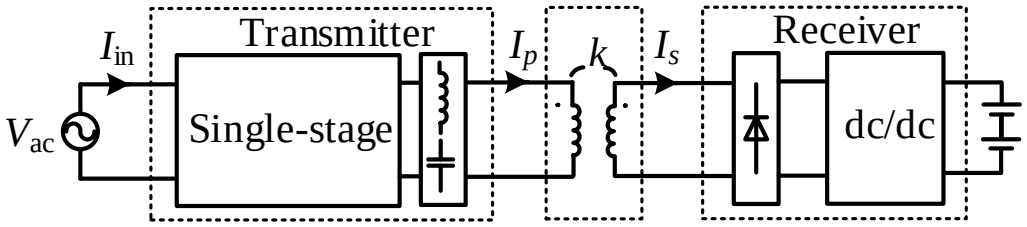
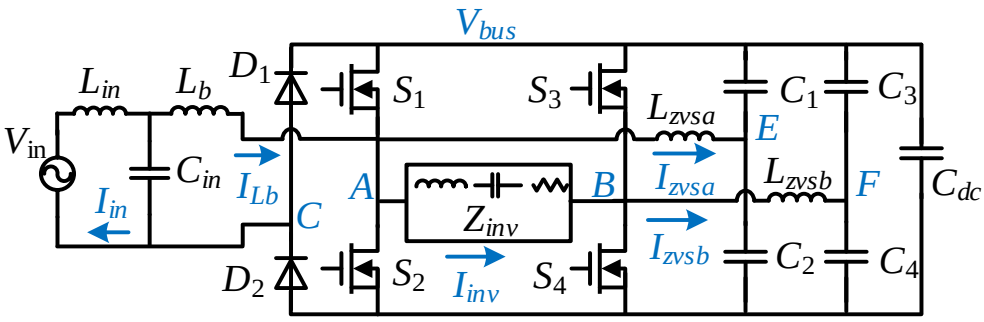


Fig. 4.1. The single-stage transmitter in the wireless power transfer system.

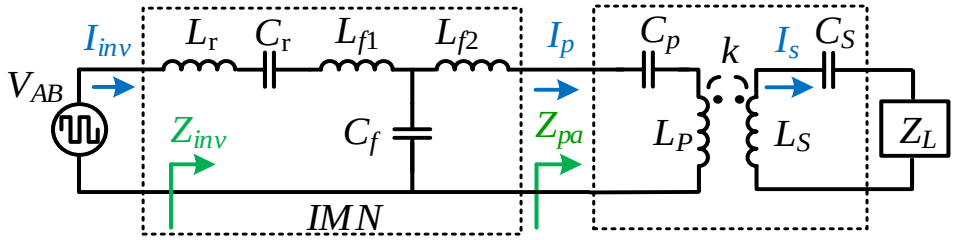
S_4. Considering the ISM band in this MHz WPT system, a constant system operating frequency (f_o=6.78 MHz) is preferred. Therefore, phase leg A and B switch at fixed 6.78 MHz. Fig. 4.2(c) shows the main waveforms, where G_{s1}-G_{s4} are the gate signals of S_1-S_4, respectively, and the remaining waveforms correspond to the schematic in Fig. 4.2(a).

4.1.1 Operation principle

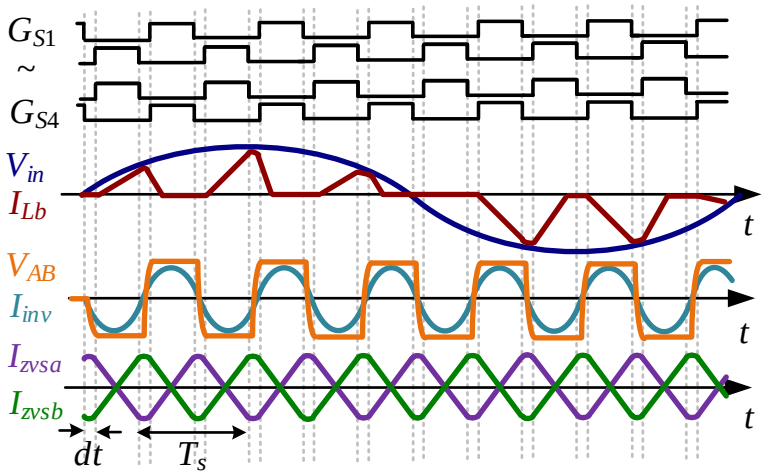
The rectifier is designed to provide high PF and minimal THD of the input current while regulating bus voltage V_{bus}. In general, a totem pole rectifier may be operated in continuous conduction mode (CCM), critical conduction mode (CRM) or DCM. CRM, although facilitating soft-switching without additional elements, exhibits a variable switching frequency, preventing it from being simply integrated into inverter operation. CCM requires feedback control to achieve PFC with low THD and has exacerbated requirements for circulating current for soft switching, which results in extra conduction loss. Additionally, a variable duty cycle is required along the line period for a constant dc bus voltage, which will increase the inverter control complexity significantly. DCM operation is selected for this application due to its possibility of high PF and low THD with constant-frequency and duty cycle over the line period, and near-ZVS operation.



(a)



(b)



(c)

Fig. 4.2. Schematic and operation waveforms.

PF and THD of input current under DCM control are analyzed to guide control design. The line input voltage is

$$V_{in}(t) = V_m \cdot sin(2\pi f_{line} \cdot t) \tag{4-1}$$

where V_m is the peak value of input voltage V_{in}, and f_{line} represents the line period. The input current of an ideal DCM boost is

$$i_{in}(t) = i_{Lb\_ave}(t) = \frac{V_{in} \cdot T_{on}^2 \cdot f_s}{2L_b \cdot (1 - \frac{V_{in}}{V_{bus}})} \tag{4-2}$$

Combining (4-1) and (4-2), the input current becomes

$$i_{in}(t) = \frac{d_a^2 \cdot V_{bus}}{2L_b \cdot f_s} \cdot (\frac{sin(2\pi f_{line} \cdot t)}{M - sin(2\pi f_{line} \cdot t)}) \tag{4-3}$$

where T_s is the switching period, f_s is the switching frequency, $M=V_{bus}/V_m$ is the modulation index, $d_a=T_{on}/T_s$ is the rectifier duty cycle, and T_{on} is the on-time of the main switch in the rectifier. When the polarity of the input voltage is positive, S_2 is defined as the main switch. Otherwise, S_1 is the main switch.

According to (4-3), constant switching frequency f_s and unity PF can be obtained if d_a is varying along with sinusoidal input voltage. To simplify control complexity, constant d_a control is implemented with acceptable THD and PF. Thus, in this single-stage design, DCM operation with constant f_s is implemented, and d_a only changes along with output power.

Power factor is defined as

$$PF = \frac{P}{S} = \frac{\frac{1}{T_{line}} \int_0^{T_{line}} V_{in}(t) \cdot i_{in}(t) dt}{V_{in\_rms} \cdot i_{in\_rms}} \tag{4-4}$$

where P is active power and S is apparent power. T_{line} is the line period. Plugging equation (4-1) and (4-3) into (4-4), PF is

$$PF = \frac{\sqrt{\frac{2}{T_{line}}}\int_0^{T_{line}} \frac{sin^2(2\pi f_{line}\cdot t)}{M - sin(2\pi f_{line}\cdot t)}dt}{\sqrt{\int_0^{T_{line}} (\frac{sin(2\pi f_{line}\cdot t)}{M - sin(2\pi f_{line}\cdot t)})^2 dt}} \tag{4-5}$$

Additionally,

$$PF = \frac{1}{\sqrt{1+THD^2}}\cdot cos\theta \tag{4-6}$$

where θ is the phase angle between the input current and input voltage. Ideally, θ is zero under DCM modulation. Thus, THD is derived according to (4-6).

$$THD = \sqrt{\frac{1}{PF^2} - 1} \tag{4-7}$$

According to (4-5) and (4-7), the curves of PF and THD as a function of *M* are demonstrated in Fig. 4.3. Larger *M* provides a higher PF and a lower THD. However, larger *M* causes larger dc bus voltage, therefore increasing the voltage stress on the switches (S_1~S_4, D_1, and D_2). In this work, *M*=2 is chosen for moderate bus voltage and acceptable PF and THD.

To keep rectifier operating in DCM, equation (4-8) needs to be satisfied:

$$d_a \le 1 - \frac{1}{M} \tag{4-8}$$

where *M* = 2 is chosen for this work, then $d_a \le 0.5$. The input power of rectifier is

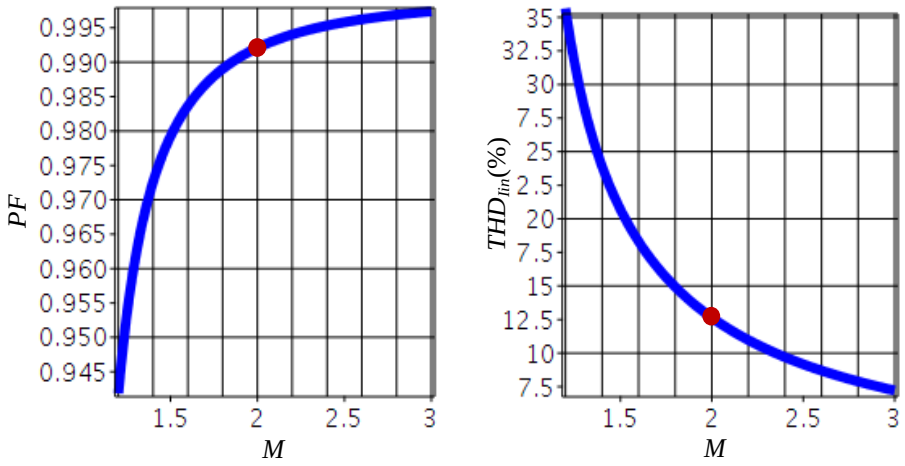
$$\begin{aligned} P_{in} &= \frac{1}{T_{line}}\int_0^{T_{line}} V_{in}(t)\cdot i_{in}(t)dt \\ &= \frac{1}{T_{line}}\cdot\frac{d_a^2\cdot V_m\cdot V_{bus}}{2L_b\cdot f_s}\int_0^{T_{line}} \frac{sin^2(2\pi f_{line}\cdot t)}{M - sin(2\pi f_{line}\cdot t)}dt \end{aligned} \tag{4-9}$$

Assume lossless in the converter, thus P_{in}=P_o. (4-9) is rearranged:

$$d_a = \sqrt{P_o \cdot \frac{2L_b \cdot f_s \cdot T_{line}}{V_m \cdot V_{bus} \cdot \int_0^{T_{line}} \frac{sin^2(2\pi f_{line} \cdot t)}{M - sin(2\pi f_{line} \cdot t)} dt}} \tag{4-10}$$

The rectifier is designed to keep constant V_{bus} at different load conditions to simplify the control scheme and provide minimal voltage stress on the switching devices. To maintain a constant V_{bus}, d_a varies along with P_o in DCM operation.

As discussed before, V_{bus} is a function of both rectifier duty cycle d_a (duty cycle of phase leg A) and load Z_{inv}. In order to maintain constant voltage, d_a needs to be varied with load changing. To get a higher degree of freedom in output power control, asymmetrical voltage cancellation (AVC) [168] is introduced. AVC combines conventional phase-shift control [169] and asymmetrical duty-cycle control [170]. In the previous literature, AVC scheme is used to extend the ZVS operating range [171], [145], reduce the harmonic output and improve the efficiency [168]. Fig. 4.4 gives example waveforms with AVC modulation. Parameters β_a, β_b, α_+ and α_- are the control angles for output power regulation while β_a also represents the duty cycle of the rectifier ($\beta_a = 2\pi d_a$).



(a) PF (b) THD

Fig. 4.3. PF and THD of input current as a function of M.

According to Fourier series, the amplitude of fundamental harmonic of V_{ab} is V_{ab1}

$$V_{abh} = \frac{V_{bus}}{\pi}\sqrt{a_h^2 + b_h^2} \tag{4-11}$$

where

$$a_h = \sin[h \cdot (\beta_a - \alpha_+)] + \sin(h \cdot \beta_a) + \sin(h \cdot \alpha_-) \tag{4-12}$$

$$b_h = 1 - \cos\ [h \cdot (\beta_a - \alpha_+)] - \cos(h \cdot \beta_a) + \cos(h \cdot \alpha_-) \tag{4-13}$$

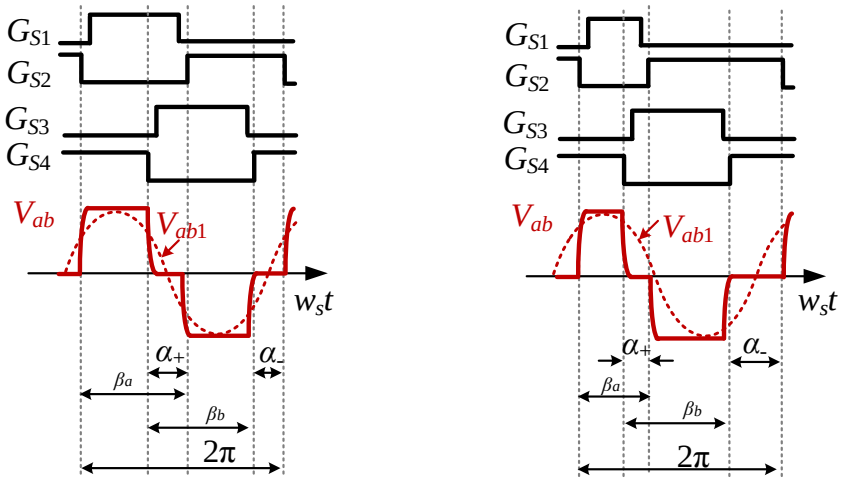
The dashed waveform (V_{ab1}) in Fig. 4.4 represents the fundamental harmonic of V_{ab}. The amplitude of V_{ab1} is

$$V_{ab1} = \frac{V_{bus}}{\pi}\sqrt{[\sin(\beta_a - \alpha_+) + \sin(\beta_a) + \sin(\alpha_-)]^2 + [1 - \cos(\beta_a - \alpha_+) - \cos(\beta_a) + \cos(\alpha_-)]^2} \tag{4-14}$$

The output power is

$$P_o = \frac{V_{ab1}^2}{2|Z_{load}|^2} \cdot R_{load} \tag{4-15}$$

where R_{load} is the real part of Z_{load}. According to (4-11) - (4-15), the output power can be controlled from zero to full power by three variables: α_+, α_- and β_a. Since β_a is used to maintain constant bus voltage at different load conditions, α_+ and α_- are used to control output power. The impact of dead time is not considered in this model.



(a) Modulation at heavy load (b) Modulation at light load

Fig. 4.4. The modulation of the inverter.

4.1.2 Constant output current achievement

Because this system is designed for multiple receiver applications, driving the transmitter coil with a current source is preferred for smooth transient performance. Two methods can be utilized to achieve constant current behavior. First, phase-shift and duty cycle can be regulated through current mode control. Due to the resonant nature of the converter and complexity of low-delay, isolated current sensing, it will be difficult to achieve cycle-by-cycle current regulation. Second, as employed in this work, the inverter can produce a controlled constant-voltage output V_{ab1}, which is then converted to a constant current I_p through a passive impedance network. Assuming the presence of a large DC bus capacitance, as required for line frequency decoupling, V_{bus} has a negligible ripple at frequencies well above 120 Hz, resulting in a minimal disturbance in I_p with load variation without the need for control bandwidths approaching 6.78 MHz. This section describes

the modulation scheme used to obtain a constant V_{ab1}, while the IMN design for constant current is presented in the following section.

Equations (4-14) indicates that there is a continuous solution space of values for α_+ and α_- which achieve a given V_{ab1}. In this work, the solution is selected by adding the constraint: $\beta_b=\pi$. Therefore,

$$\alpha_- = \pi - \beta_a + \alpha_+ \tag{4-16}$$

where $\beta_a > \alpha_+$. Two benefits are provided by setting $\beta_b=\pi$. First, the duty cycle of phase leg B is set to a constant 0.5, reducing control complexity. Second, the THD of V_{ab} is low. THD of V_{ab} is defined as

$$THD(\%) = 100 \cdot \sqrt{\frac{\sum_{n=2}^{\infty}(a_h^2 + b_h^2)}{a_1^2 + b_1^2}} \tag{4-17}$$

If plug (4-10), (4-12), (4-13) into (4-15), replacing α_- with β_b ($\alpha_- = 2\pi - \beta_a - \beta_b + \alpha_+$) and set P_o=100 W (as an example), THD_{Vab} contour respect to β_b and α_+ is plotted in Fig. 4.5. The dead time of phase leg A and B is not taken into consideration for simplification. As a result, THD_{Vab} under this estimation will be higher than the practice, especially at high-order harmonics. However, this simplified model is still considered valid for the comparison of THD_{Vab} among different β_b. Results in Fig. 4.5 show that when $\beta_b \approx \pi$, the lowest THD_{Vab} is obtained. Decreased THD_{Vab} reduces the size, electrical stress and suppresses the radiated EMI in coils. Therefore, $\beta_b=\pi$ is chosen in this work.

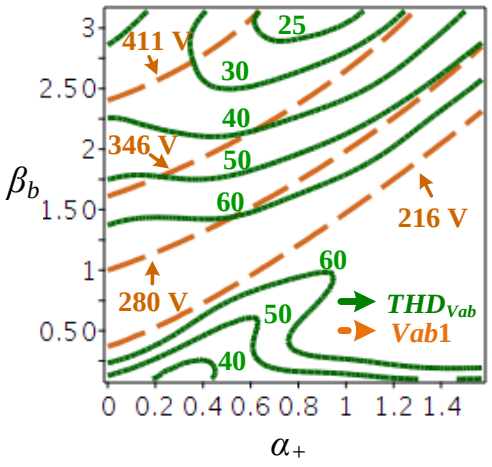


Fig. 4.5. THD contours.

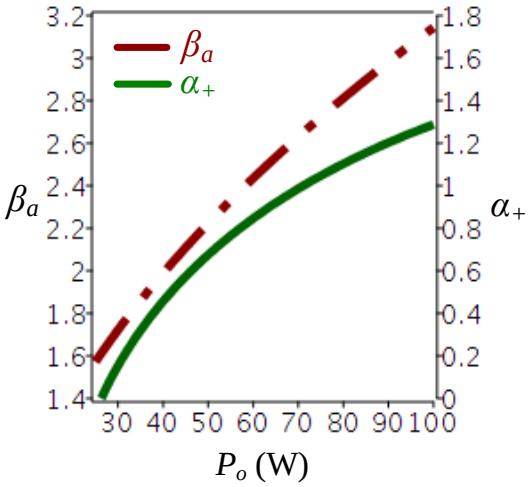


Fig. 4.6. Control trajectory.

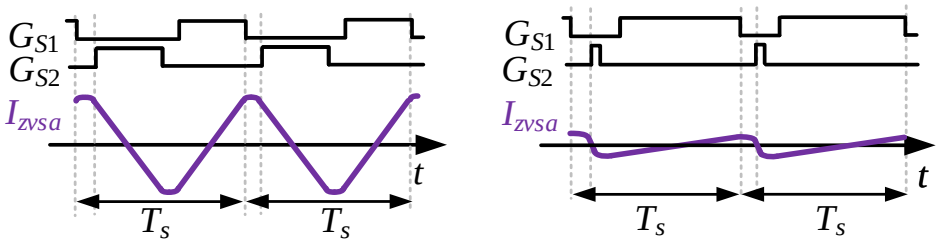
Replacing α_- with β_b in (4-14), the V_{ab1} contours are plotted in Fig. 4.5. Larger V_{ab1} results in lower THD_{Vab}. However, V_{ab1} is limited by the modulation. For the full bridge inverter, if two phase legs have 0.5 duty cycle and 180-degree phase shift, then V_{ab1}=433 V. For the half-bridge inverter, V_{ab1}=216 V when the duty cycle is 0.5. In addition, higher V_{ab1} increases the power loss in the T-type filter in the IMN which will be discussed in the following section. In this work, V_{ab1}=346 V is chosen to balance the THD_{Vab} and the power loss in the T-type filter.

Plugging equation (4-10), (4-14) and (4-16) into (17), the control trajectory with V_{ab1}=346 V is given in Fig. 4.6, for varying loads. In a practical implementation, β_a can be regulated in a closed-loop based on the feedback of V_{bus}, and α_+ is updated in real time according to the model and the value of β_a.

Based on the constant V_{ab1}, utilizing the IMN introduced in section 3.4.3, then constant I_p is achieved.

4.2 The improved single-stage transmitter

The single-stage transmitter achieves high efficiency with ZVS operation with the assistance of the two ZVS tanks. However, the amount of ZVS tank current available to aid in ZVS is determined by the duty cycle of each inverter leg. Due to DCM operation in PFC rectifier, the duty cycle of phase leg A decreases as the load is reduced. As the transmitter approaches zero load, near-zero d causes insufficient ZVS tank current for phase leg A to maintain ZVS, as shown in Fig. 4.7. Because of the high DC voltage and large switching frequency, efficiency drops dramatically if hard switching occurs.



(a) At heavy load (b) At light load

Fig. 4.7. ZVS tank current.

4.2.1 Operation principle

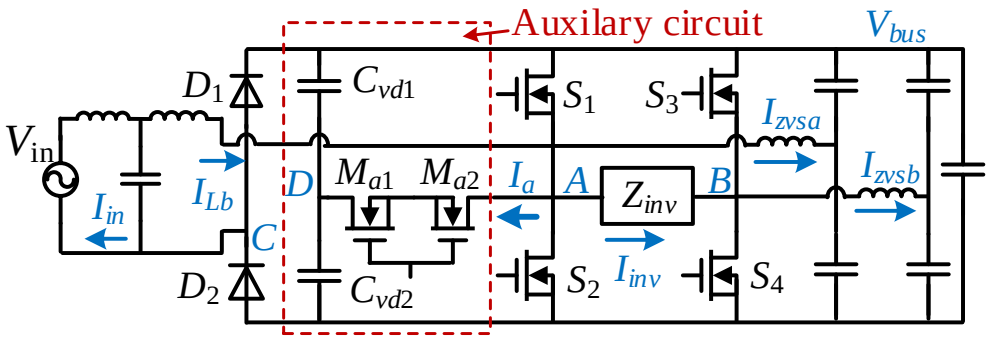
To improve the efficiency at light load, an auxiliary circuit, composed of a bidirectional switch (implemented with two identical MOSFETs M_{a1}, M_{a2} connected back to back), and two capacitors C_{vd1} and C_{vd2}, are added. The modified single-stage transmitter is shown in Fig. 4.8(a). At output powers sufficiently large to maintain ZVS, M_{a1} and M_{a2} are turned off, and the auxiliary circuit negligibly impacts the operation of the circuit as reviewed in the previous section. At light load, the circuit operation is changed by turning on M_{a1} and M_{a2} and turning off S_1 and S_2. In this mode, C_{vd1}, C_{vd2}, D_1, and D_2 form a voltage doubler

rectifier (VDR) [172-174] while S_3 and S_4 comprise a half-bridge inverter to provide the 6.78 MHz ac output. Fig. 4.8(b) demonstrates the main waveforms at light load mode. Since this mode is only used at light load, where regulated PF and THD are not required (P<75 W), name it as light load mode. The operation with PFC that discussed above is heavy load mode. VDR operation eliminates hard switching at light load and reduces light-load conduction losses by decreasing the ZVS tank current I_{zvsa} to zero. M_{a1} and M_{a2} switch only when changing operation modes and conduct current only at light load, allowing the use of low-cost silicon transistors. The addition of C_{vd1} and C_{vd2} allows a corresponding decrease in C_{dc}, mitigating the impact of their addition on converter size and cost. Therefore, this auxiliary circuit does not result in a significant hardware addition.

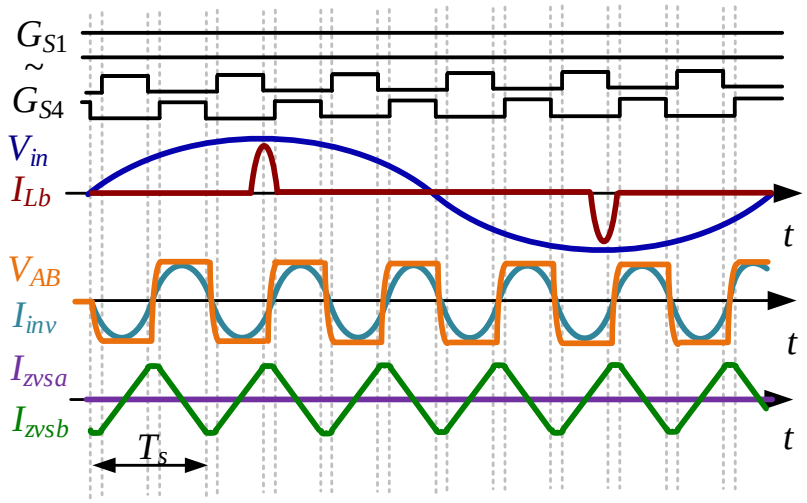
The simplified equivalent circuits of each mode are given in Fig. 4.9(a) and Fig. 4.9(b), respectively. Fig. 4.9(c) gives the main waveforms of each operating mode. At heavy load mode, the voltage ratio is designed as $m=V_{bus}/V_m=2$, where V_{bus} is the bus voltage and V_m is the peak value of ac input voltage. At light load mode, the rectifier output V_{bus} will be nearly twice V_{in_pk}. As a result, ideally V_{bus} remains constant in both operating modes with a smooth transition between each mode.

4.2.2 Design considerations for C_{vd} and C_{dc}

Ideally, in the VDR operation, $V_{bus} = 2V_m$. In the heavy load mode, V_{bus} is actively regulated to $M = V_{bus}/V_m = 2$ through duty cycle modulation. Consequently, V_{bus} remains constant in the two operation modes. This feature minimizes output disturbance during mode transitions. In practice, the ripple voltage and average bus voltage depend on load, C_{vd1}, C_{vd2} and C_{dc}. The schematic and waveforms of the VDR are illustrated in Fig. 4.10.

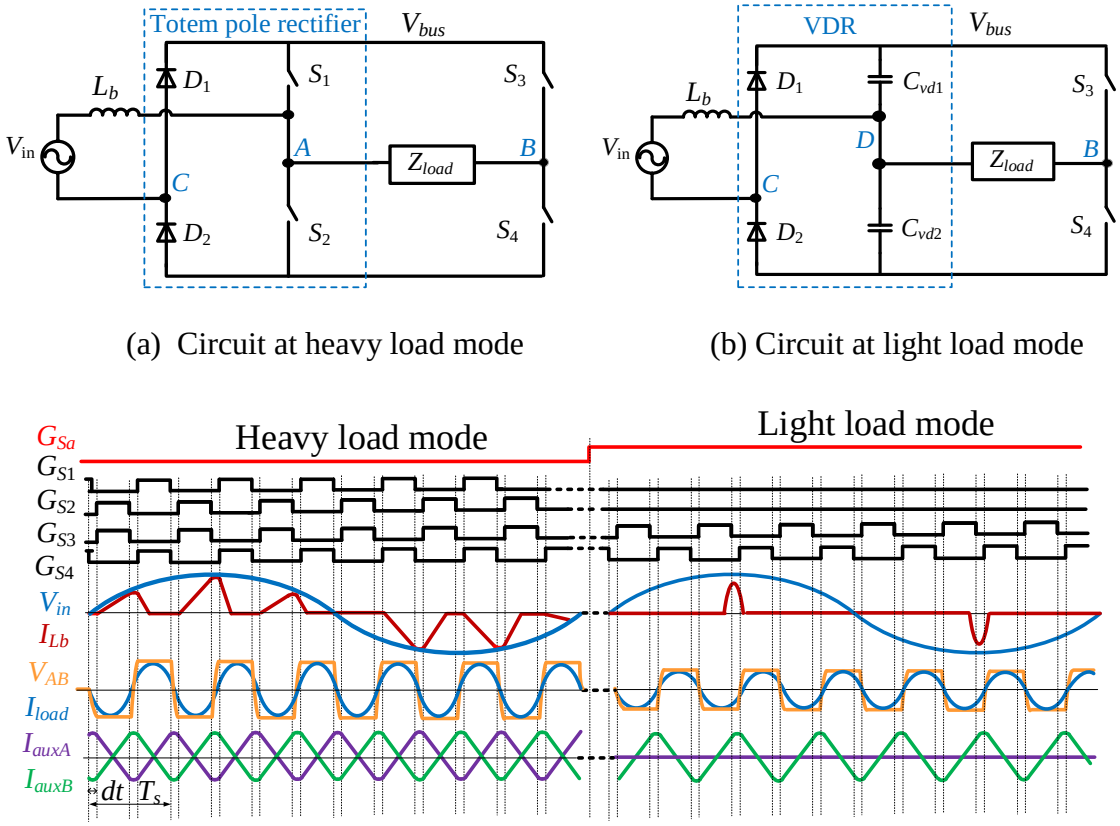


(a) Schematic



(b) Main waveforms

Fig. 4.8. Schematic and operation waveforms at light load mode.

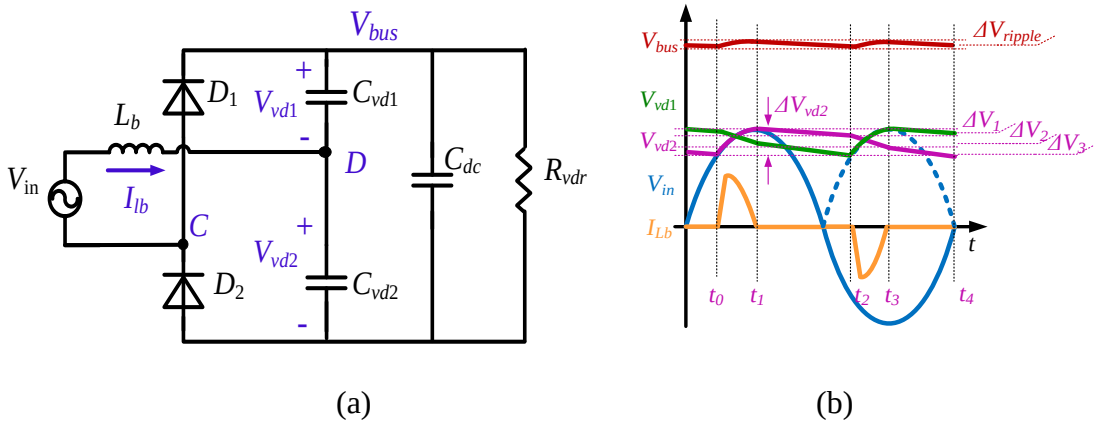


(a) Circuit at heavy load mode

(b) Circuit at light load mode

(c) The main waveforms at the two-operation modes

Fig. 4.9. Two-operation modes of the single-stage transmitter.



(a)

(b)

Fig. 4.10. Schematic and waveform of VDR.

The load of VDR is modeled as a resistive load R_{vdr}. Without loss of generality, it is assumed that $C_{vd1} = C_{vd2} = C_{vd}$.

Mode 1 ($t_0 \leq t \leq t_1$): during this time, D_2 is forward biased and conducts current I_{Lb}. The voltage on C_{vd2} is changed by

$$\Delta V_{vd2} = V_m \cdot (1 - sin(\omega t_0)) \tag{4-18}$$

Mode 2 ($t_1 \leq t \leq t_2$): when V_{vd2} reaches V_m, D_2 becomes reverse biased, C_{vd2} is discharged through C_{vd1}, C_{dc} and R_{vdr}. The decreased voltage is ΔV_1.

$$\Delta V_1 = V_m \cdot (1 - exp(\frac{-(t_2 - t_1)}{R_{load} \cdot (0.5C_{vd} + C_{dc})})) \tag{4-19}$$

Mode 3 ($t_2 \leq t \leq t_3$): The voltage on C_{vd1} is changed by ΔV_{vd1}through C_{vd2} and C_{dc}. Since $C_{vd1} = C_{vd2}$, ΔV_{vd1} is equal to ΔV_{vd2} in (2). So, the voltage change on C_{vd2} during this time is ΔV_2.

$$\Delta V_2 = \Delta V_{vd2} \cdot \frac{C_{dc}}{C_{vd} + C_{dc}} \tag{4-20}$$

Mode 4 ($t_3 \leq t \leq t_4$): ΔV_3 is the voltage change of C_{vd2} during this time.

$$\Delta V_3 = \Delta V_1 \tag{4-21}$$

According to

$$\Delta V_{vd2} = \Delta V_1 + \Delta V_2 + \Delta V_3 \tag{4-22}$$

And

$$\frac{T_{line}}{2} = t_2 - t_0 \tag{4-23}$$

ΔV_1, ΔV_2, ΔV_3 and ΔV_{vd2} are obtained by solving equations (4-18) ~ (4-23). The ripple bus voltage is

$$\Delta V_{bus} = \Delta V_{vd1} + \Delta V_{vd2} = 2 \cdot \Delta V_1 \tag{4-24}$$

The average bus voltage is

$$V_{bus} = 2 \cdot (V_m - 0.5\Delta V_{vd2}) \tag{4-25}$$

According to this derivation, the ripple bus voltage and average bus voltage depend on R_{vdr}, C_{vd1}, C_{vd2} and C_{dc}.

To suppress double line frequency voltage ripple on dc bus, the required energy storage ΔE at full power (100 W) is

$$\Delta E = \int_{\frac{T_{line}}{4}}^{\frac{3T_{line}}{4}} (P_{ave} - P_{ac}(t))dt = \frac{P_{ave}}{\omega} = 265\ mJ \tag{4-26}$$

As an example, if allowed maximum ripple voltage at full power is 5 V and V_{bus}=340 V, the required capacitance across the dc bus is

$$C_{eng} = \frac{\Delta E}{V_{bus} \cdot \Delta V_{bus}} = 0.5C_{vd} + C_{dc} = 155\ uF \tag{4-27}$$

By combining equation (4-24) and (4-27), the relation between ripple bus voltage ΔV_{bus} and k_c=C_{dc}/C_{vd} is solved and plotted in Fig. 4.11. Higher output power causes larger ripple voltage, while K_c has limited influence over ΔV_{bus}. The relation between average bus voltage V_{bus} and k_c is determined by solving equation (4-25) and (4-27). V_{bus} is given as a function of k_c and output power in Fig. 4.12. According to the curves, k_c has significant impacts on the average value of V_{bus}. And a smaller k_c results in the average bus voltage V_{bus} closer to the ideal value $2V_m$=340 V.

In terms of performance, small k_c is preferred. However, when taking the volume of dc capacitors (C_{dc}, C_{vd1} and C_{vd2}) into consideration, the selection of k_c might be different. A small k_c means smaller capacitance of C_{dc} and a larger value for both C_{vd1} and C_{vd2}. According to equation (4-27), if C_{dc} reduces by C_x, C_{vd1} and C_{vd2} will increase by $2C_x$.

However, this doesn't necessarily imply a larger volume, because the rated voltage of C_{dc} is higher than C_{vd1} and C_{vd2}. Generally, higher voltage rating increases the size of the capacitor. As a result, there is no general design rule to select K_c in accordance with the compact volume of dc capacitors. The size of C_{dc}, C_{vd1} and C_{vd2} should be calculated according to the available commercialized capacitor.

4.2.3 The selection of M_{a1} and M_{a2}

The selection of M_{a1} and M_{a2} impacts the converter loss. This section will discuss the consideration of device selection. C_{ma} is the junction capacitors of M_{a1}/M_{a2} while C_q is the junction capacitance of S_1/S_2 as shown in the Fig. 4.13. When M_{a1} and M_{a2} are off (at heavy load mode), two C_{ma} are connected in series to switching node *A*. To perform ZVS in phase leg A, the total capacitance that needs to be fully charged/discharged now becomes $C_{tot}=2C_q$ +0.5 C_{ma}, where $C_{ma} \ll 4 \cdot C_{vd}$. The additional capacitance coming from the auxiliary circuit requires higher ZVS tank current for soft switching. Consequently, higher conduction loss is incurred. To limit this impact, MOSEFTs with small junction capacitance are preferred for M_{a1} and M_{a2}.

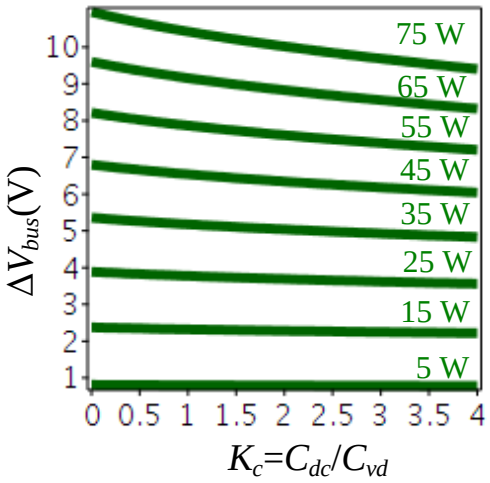


Fig. 4.11. Ripple bus voltage vs C_{dc}/C_{vd}..

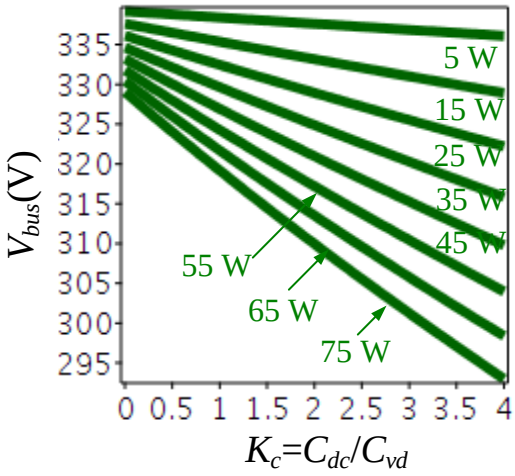


Fig. 4.12. Average bus voltage vs C_{dc}/C_{vd}..

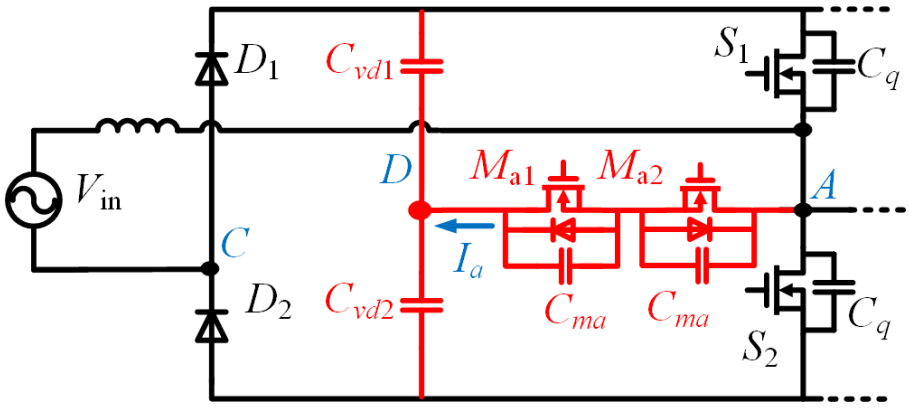


Fig. 4.13. The practical design of the auxiliary circuit.

In addition, the current flowing through M_{a1} and M_{a2} (I_a), should remain within the maximum current of devices. I_a is the sum of input current I_{Lb} and the load current I_{load}. In this system, the maximum power is 100 W, and bus voltage is 340 V, so, I_{load} is quite small. Devices M_{a1} and M_{a2} only conduct current at light load, I_{load} is negligible under this condition. Therefore, I_a is approximated to I_{Lb}. At heavy load, $I_a \approx 0$. At light load, when M_{a1} and M_{a2} are turned on, there are two situations. When the diode is reverse biased ($t \leq t_0$, $t_1 \leq t \leq t_2$ and $t_3 \leq t \leq t_4$), I_a=0. When the diode forward biased ($t_0 \leq t \leq t_1$ and $t_2 \leq t \leq t_3$), I_a is

$$I_a = \frac{V_{in}}{Z_c} \tag{4-28}$$

where Z_c is the output impedance of V_{in}.

$$Z_c = \frac{(Z_{vd} + Z_o)Z_{vd}}{2Z_{vd} + Z_o} \tag{4-29}$$

where $Z_{vd}=1/j\omega C_{vd}$, and

$$Z_o = \frac{R}{1 + j\omega C_{dc} R} \tag{4-30}$$

Considering the output capacitance and current capability of M_{a1} and M_{a2}, MOSFET IPD50R3K0CE is chosen in this application. The calculated energy-based equivalent junction capacitance is C_{ma} = 11 pF. Only a negligible 5.5 pF of capacitance is added to switching node A.

4.3 The transitions between the two operation modes

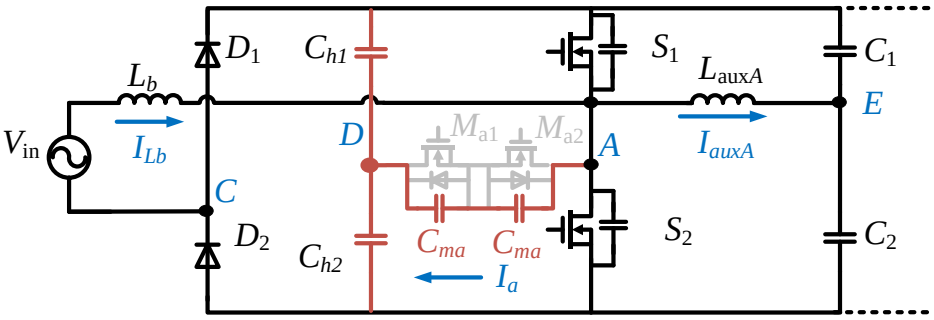
As discussed above, there are two operation modes for the single-stage transmitter. When the load dynamically change, the required output power also changes. To maintain high efficiency in a wide range, the heavy load mode and light load mode should be employed whenever the one gives the highest efficiency. Thus, mode changing around will

frequently occur. The following part will discuss the approaches to ensure smooth mode changing.

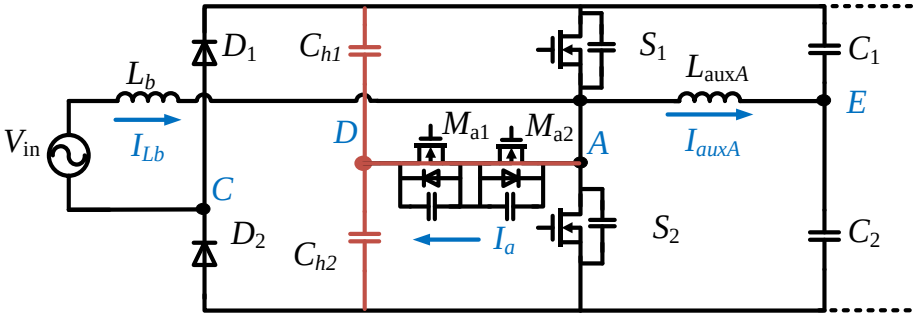
4.3.1 The transition from heavy load mode to light load mode

Fig. 4.14 shows the simplified circuit at heavy load mode and light load mode. Since phase leg B does not participate in the mode transition, it is removed from the schematic. M_{a1} and M_{a2} keep off during heavy load mode. However, their output capacitors are always connected to the switching node A. Because C_{vd1} and C_{vd2} have much larger capacitance than C_{ma}, they will be treated as a short circuit during resonant periods.

To achieve a smooth transition, S_1 and S_2 are turned off during their dead time, then M_{a1} and M_{a2} are turned on after a certain delay time. This delay time helps prevent short circuit by turning on S_1 or S_2, M_{a1} and M_{a2} at the same time. Fig. 4.15 shows the initial measurement waveforms during the transition. I_{auxa} has large ringing after the mode changes.



(a) Heavy load mode



(b) Light load mode

Fig. 4.14. Simplified circuit.

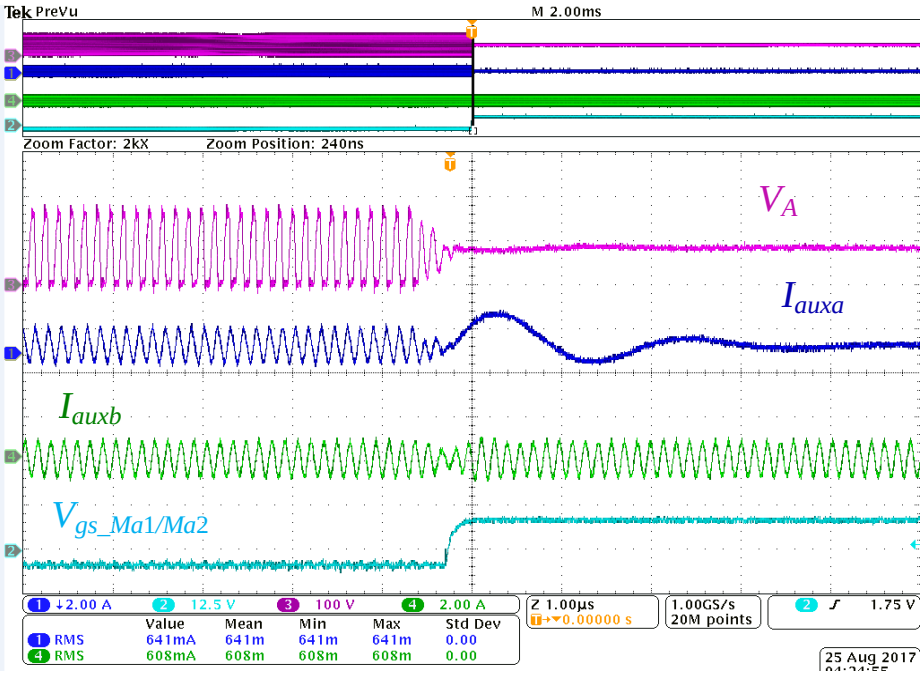


Fig. 4.15. Initial waveform of transition from heavy load mode to light load mode.

The circuit operation is analyzed to solve this ringing issue. Fig. 4.16 shows the main waveforms at heavy load mode. As seen, the rising slope of V_A is higher than the falling slope at the positive half line period, while the negative period has the opposite result. At the positive half-line period, before S_2 turns on, the resonant current which brings V_A from zero to V_{bus} is $I_{Lb}(0)+I_{auxa}$. During this time, I_{Lb} is near zero. Thus resonant current is near I_{auxa}. However, after S_2 turns off, the current that charing/discharging the output capacitance of S_1 and S_2 is $I_{Lb}(pk)+I_{auxa}$. I_{Lb} has a peak value at this time. Thus the resonant current is relatively high. As a result, the rising slope is higher than the falling slope. For the negative half-line period, the mirrored result is obtained. This asymmetric V_A results in line frequency ripple on V_D, because V_A charges C_{vd1}/C_{vd2} through the output capacitors of M_{a1} and M_{a2} during heavy load mode. V_E does not contain line frequency ripple due to the small capacitance of C_1 and C_2.

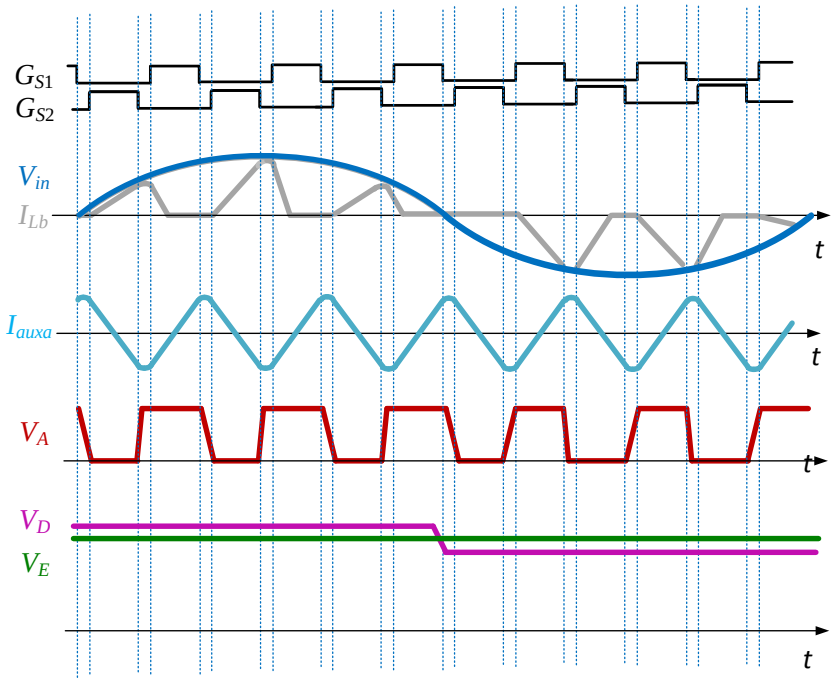


Fig. 4.16. Main waveforms at heavy load mode.

The voltage difference on the V_D and V_E cross L_{auxa} causes in the ringing after S_1 and S_2 are off and M_{a1} and M_{a2} are turning on. When the transition happens at zero cross point of the input voltage, the resonant bebaivor will be avoid. At this point, V_D=V_E.

This analysis and solution are verified in the simulation. Fig. 4.17 shows the waveforms which match with the analysis above. V_E contains the double line frequency from the bus voltage.

If turn on M_{a1} and M_{a2} when the input voltage is positive as shown in Fig. 4.18(a), then large ringing is observed on I_{auxa} as shown in Fig. 4.18(b).

If turn on M_{a1} and M_{a2} near the input voltage zero cross point as shown in Fig. 4.19(a), then negligible ringing remains on I_{auxa} as shown in Fig. 4.19(b). Therefore, a smooth transition from the heavy load mode to light load mode is achieved. This approach is verified in the experimental results.

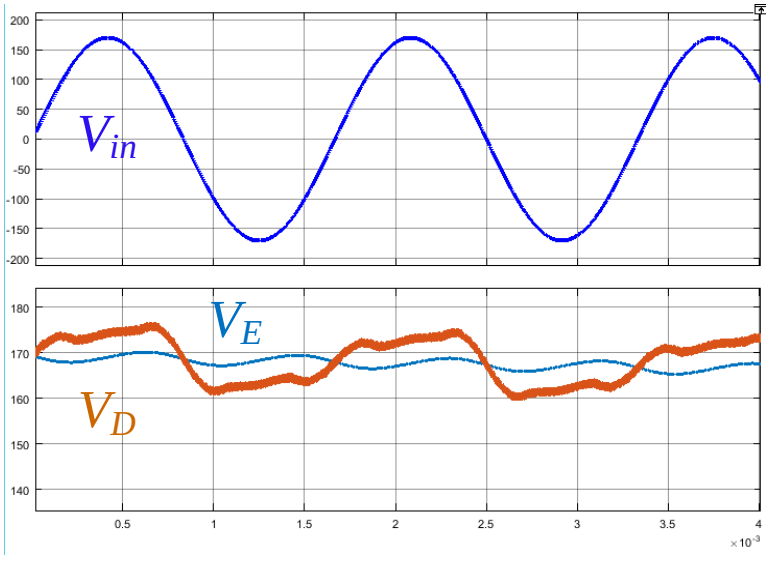
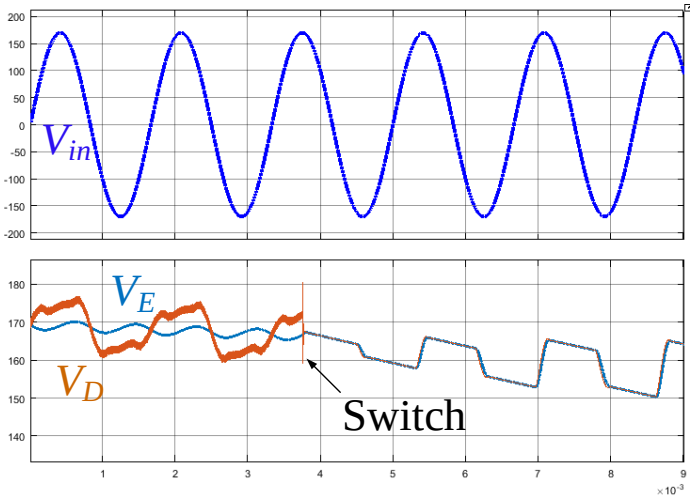
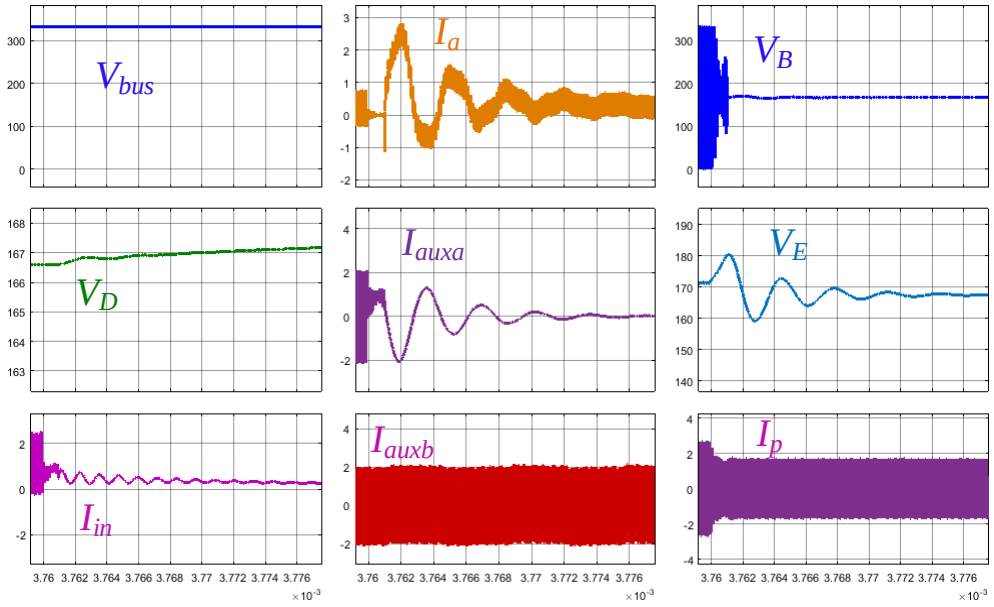


Fig. 4.17. Simulation waveform of V_E and V_D at heavy load mode.

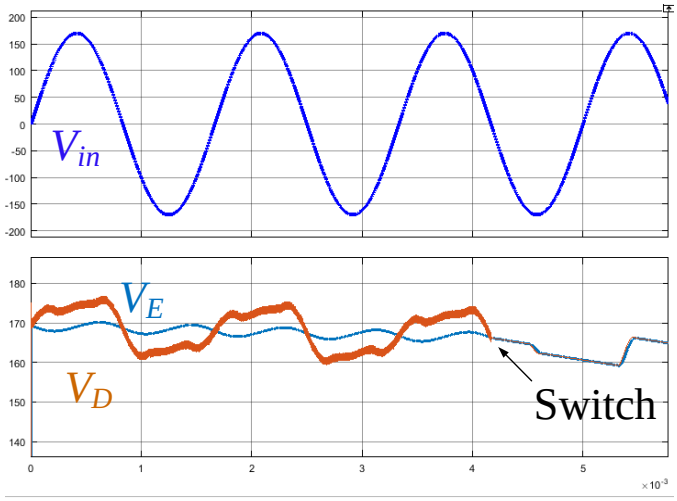


(a)

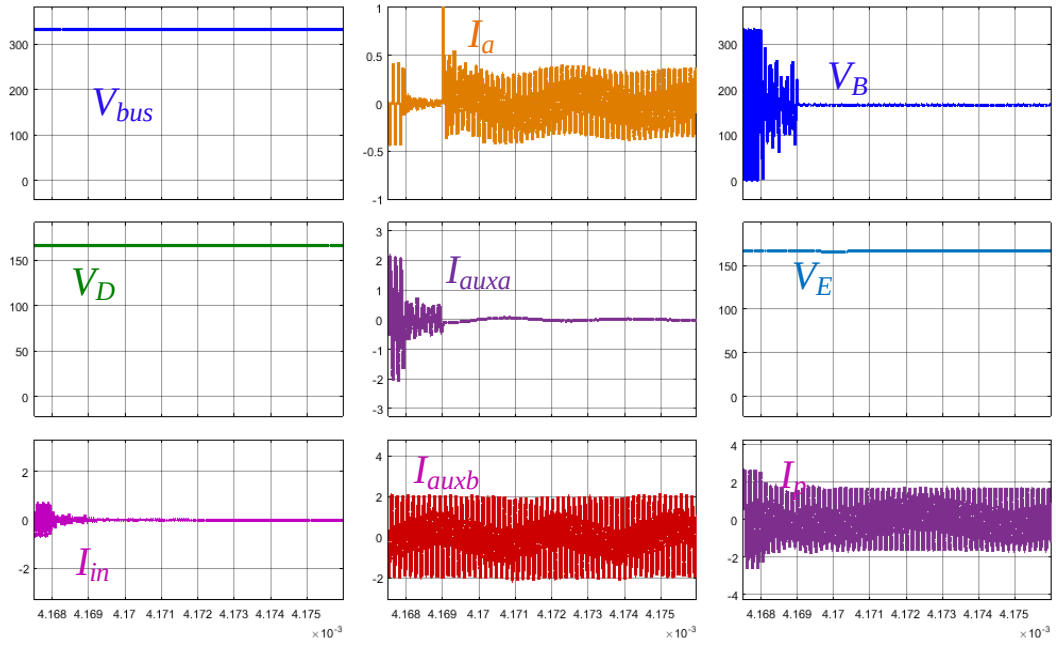


(b)

Fig. 4.18. Simulation waveform during the transition at positive line voltage.



(a)



(b)

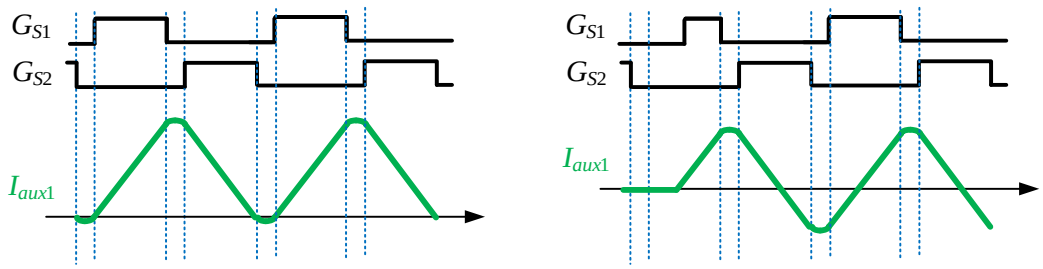
Fig. 4.19. Simulation waveform of the transition at input voltage zero cross point.

4.3.2 The transition from light load mode to heavy load mode

The challenging during the mode transition from the light load to heavy load is to deal with the hard switching at first few switching cycles. Two methods are introduced in this section to reduce the hard switching cycles.

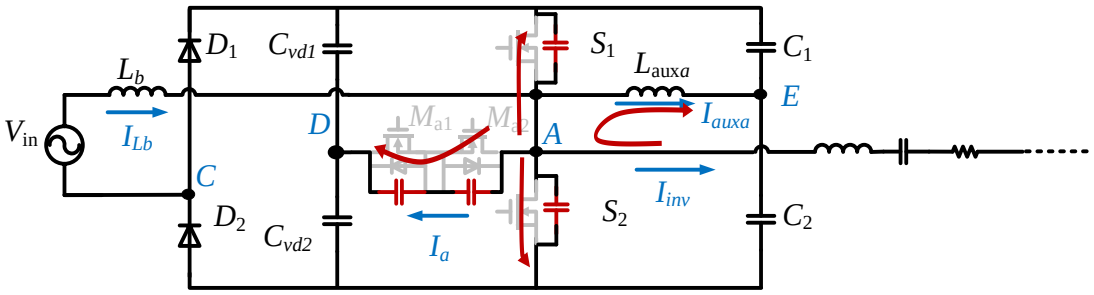
(1) The T_{on} of the first switching cycle is set to be 0.25 T_s. Assume S_1 is the device will be turned on first. If S1 is turned on as normal, I_{auxa} will increase to a large peak value since the initial current is zero, as shown in Fig. 4.20(a). If adopts the solution, I_{auxa} will reach the normal peak quickly, as shown in Fig. 4.20(b).

(2) Turn on S_1 when V_A is resonated to the positive peak value. Shows the schematic during the transition when M_{a1} and M_{a2} are turned off and before S_1 and S_2 on. The waveforms of the line input voltage and current are shown in the (b). Processing the transition when I_{Lb} is small (near zero in the green blocks), the resonant current in the circuit will only be output current Iinv. In this condition, resonate behavior on the V_A is easier to estimate, as shown in the (c). The best turn-on time can be obtained by referring the switching pattern of S_3 and S_4. This idea is verified in the experimental results.

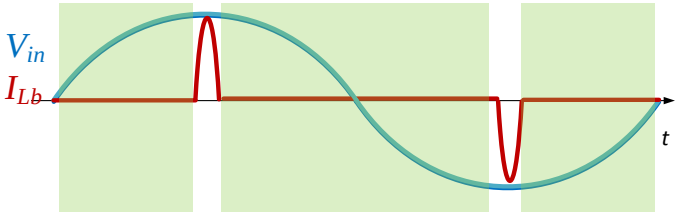


(a) (b)

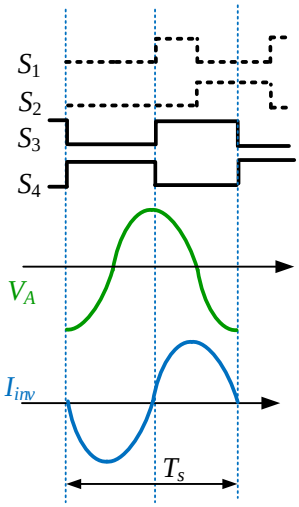
Fig. 4.20. Two different turns on strategies.



(a)



(b)



(c)

Fig. 4.21. Resonant behavior during the transition dead time.

4.4 The loss model and efficiency estimation

Since soft switching is obtained, the main power losses in this converter are conduction loss of devices (S_1~S_4, S_{a1}, S_{a2}, D_1 and D_2), and core loss and copper loss of the inductors (L_b, L_{zvsa}, L_{zvsb}, L_r, $L_{f1,}$ and L_{f2}).

D_1 and D_2 are Schottky diodes which have negligible reverse recovery loss. The conduction loss in D_1 and D_2 is P_d.

$$P_d = V_F I_{in\_ave} = \frac{2V_F}{T_{line}} \int_0^{\frac{T_{line}}{2}} i_{in}(t)dt \tag{4-31}$$

where $i_{in}(t)$ is presented in equation (4-2).

To estimate power loss in devices S_1~S_4, i_{Lb} (t), $i_{zvsa}(t) = i_{zvsb}(t)$ and $i_{inv}(t)$ are

$$i_{Lb}(t) = \begin{cases} \dfrac{v_{in} \cdot t}{L_b} & t < t_{on} \\ -\dfrac{V_{bus} - v_{in}}{L_b} \cdot t + \dfrac{V_{bus} \cdot T_s \cdot d}{L_b} & t_{on} \le t \le T_s \end{cases} \tag{4-32}$$

$$i_{zvsa}(t) = \begin{cases} \dfrac{V_{bus} \cdot (1-d)}{L_{zvsa}} \cdot (t - \dfrac{T_s \cdot d}{2}) & t < t_{on} \\ -\dfrac{V_{bus} \cdot (1-d)}{L_{zvsa}} \cdot (t - \dfrac{T_s \cdot d}{2}) & t_{on} \le t \le T_s \end{cases} \tag{4-33}$$

$$i_{inv}(t) = \frac{V_{ab1}}{|Z_{load}|} \cdot sin(2\pi f_s \cdot t) \tag{4-34}$$

The current flowing through S_1 and S_2 in one switching period i_{s12} is the sum of i_{Lb}, $i_{inv,}$ and $i_{zvsa.}$ Their waveforms in one switching cycle are shown in Fig. 4.22.

$$i_{s12}(t) = i_{Lb}(t) + i_{zvsa}(t) + i_{inv}(t) \tag{4-35}$$

The conduction loss in S_1 and S_2 is P_{cond_s12}

$$P_{cond\_s12} = R_{on} \cdot I_{rms\_s12}^2 \tag{4-36}$$

where R_{on} is the on-state resistance of S_1/ S_2 . The RMS value of i_{s12} over a line cycle is I_{rms_s12}

The current flowing through S_3 and S_4 in one switching period is the sum of i_{inv} and i_{zvsb}. The waveforms in one switching cycle are given in Fig. 4.23 .

$$\mathrm{i_{s34}(t) = i_{zvsb}(t) + i_{inv}(t)} \tag{4-37}$$

The conduction loss in S_3 and S_4 is P_{cond_s34}

$$\mathrm{P_{cond\_s34} = R_{on} \cdot \frac{2}{T_{line}} \int_0^{\frac{T_{line}}{2}} i_{s34}^2(t)dt} \tag{4-38}$$

The current in S_{a1} and S_{a2} is the sum of i_{Lb} and i_{inv}. Conduction loss in S_{a1} and S_{a2} is P_{cond_sa}

$$P_{cond\_sa} = 2R_{on\_sa} \cdot \frac{2}{T_{line}} \int_0^{\frac{T_{line}}{2}} [i_{Lb}(t) + i_{inv}(t)]^2 dt \tag{4-39}$$

Inductor losses are estimated according to core loss and copper loss. Core loss is calculated according to the methods provided by the core supplier [175]. Copper losses, comprised of dc copper loss R_{dc} and high-frequency ac copper loss R_{ac} resulting from skin effect and proximity effect, are taken into the calculation. According to the Dowell's equation [176], a single layer winding with an assumption that pitch/diameter (P/D) =1:

$$\frac{R_{ac}^*}{R_{dc}} = \frac{\xi}{2} \frac{sinh(\xi) + sin(\xi)}{cosh(\xi) - cos(\xi)} \tag{4-40}$$

where $= \frac{\sqrt{\pi}}{2} \frac{\mathrm{D}}{\delta}$, is the skin depth, P is the pitch of wires and D is the diameter of round conductor. When $P/D \neq 1$, a correction equation is implemented [177].

$$\frac{R_{ac}}{R_{dc}} = (\frac{R_{ac}^*}{R_{dc}} - 1) \cdot \frac{d}{P} \cdot K_1 \cdot K_2 + 1 \tag{4-41}$$

where K_1 is the winding P/D correction factor, and K_2 is the core proximity correction factor.

Based on this loss model, power loss as a function of output power for two operation modes is given in Fig. 4.24. As seen, the heavy load mode is superior to light load mode when the output power is high, while light load mode exhibits superior efficiency at lower power. Power loss in light load mode increases significantly with increased load due to high conduction loss in S_{a1} and S_{a2}. As a result, to have high efficiency over the full load range, the crossing point is taken as operation mode switching point with the condition that power is less than 75 W. The circles in the plot are the control trajectory for highest efficiency.

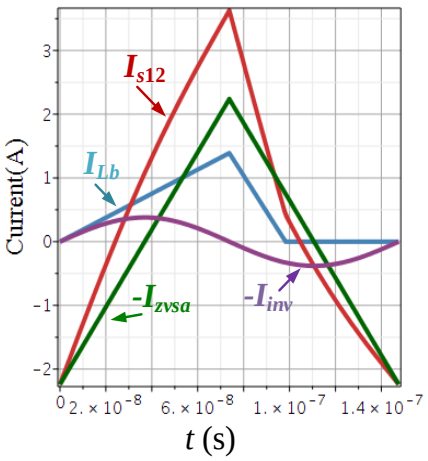


Fig. 4.22. Current flow through S_1 and S_2.

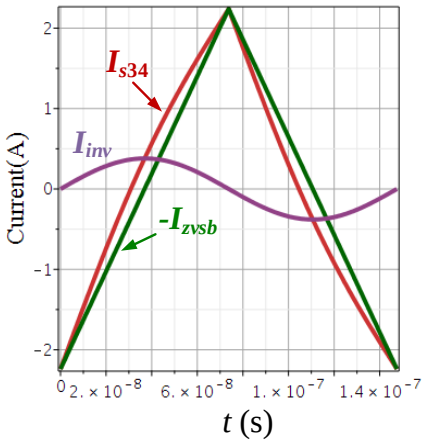


Fig. 4.23. Current flow through S_3 and S_4.

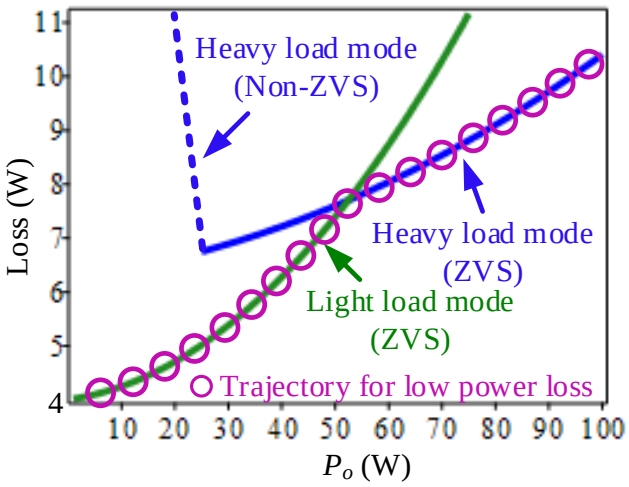


Fig. 4.24. Calculated power loss curves.

4.5 Topologies comparison

This proposed single-stage transmitter is derived from two-stage totem-pole rectifier with a full-bridge inverter (TRFB). It has a similar structure to the two-stage totem-pole rectifier with a half-bridge inverter (TRHB). To consider the merits of each, a comparison in terms of efficiency, power density and cost among all three topologies are made based on the same design specifications, including input voltage, bus voltage and output current.

This proposed single-stage transmitter integrates a totem-pole rectifier with a full-bridge inverter, sharing one phase leg. To assess the merit of the topology, the proposed transmitter is benchmarked against comparable two-stage implementations in TABLE 4.1, Fig. 4.25, and Fig. 4.26. Each topology is assessed by efficiency, cost, and power density, with common input and output specifications for each design.

Each of the two-stage topologies in Table I is comprised by a totem-pole rectifier (TR) and either a full bridge (FB) or half-bridge (HB) inverter. Each of the topologies requires that the inverter operates at 6.78 MHz. However, because the rectifier and inverter are decoupled in the two-stage topologies, the rectifier and inverter are not constrained to

utilizing the same switching frequency, as is required for the single-stage architecture operation presented in Section II-A. Thus, both low-frequency CCM (C) and 6.78 MHz DCM (D) modulation are considered in the rectifiers in the two-stage topologies. The selection of switching frequency in the two-stage rectifiers is independent design freedom which can be used to control a tradeoff between boost inductor size and ac-related losses. In the CCM implementations, f_s=70 kHz is used, which results in the highest efficiency over a range of available commercial magnetic cores. In the following figures, topologies are named according to their rectifier, inverter, and modulation scheme, e.g., TRFB(D) is a two-stage totem pole rectifier with full bridge inverter, where the rectifier is operated in DCM and TRHB(C) is a totem pole rectifier in CCM with a half-bridge inverter.

In all designs, one ZVS tank is dedicated for each phase leg switching at 6.78 MHz, as shown in Table I. A dedicated IMN is designed for each topology. In each case, the IMN uses the same magnetic cores for each component and is designed for an identical transmitter coil current I_p. The same magnetic cores are utilized because of two reasons: (1) when comparing single-stage transmitter with TRFB(C) and TRHB(C), the dominant differences of the size and loss come from ZVS tanks and L_b, instead of the IMN. Implementing different magnetic cores for the IMN barely changes the comparison result; (2) when comparing the single-stage transmitter with TRFB(D) and TRHB(D), the difference comes from the inverter stage. Realizing the inverter side IMN with identical cores ensures the similar volume, thus provides a fair condition for the efficiency comparison.

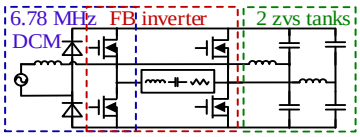
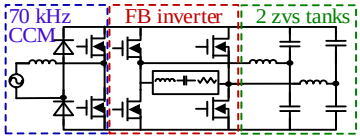
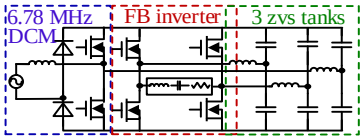
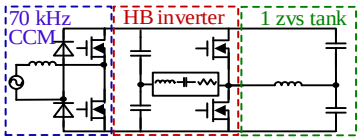
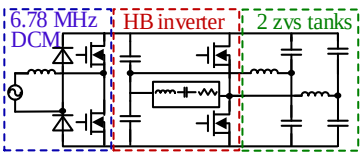
Using the developed loss models, the five topologies of Table 4.1 are analyzed with respect to power loss in Fig. 4.25 and Fig. 4.26. Fig. 4.25 shows power loss as a function

of output power. A power loss breakdown at full power is given in Fig. 4.26 for each of the topologies.

Because 6.78 MHz switched DCM rectifier exhibits higher loss than low-frequency CCM rectifier in passive components and switches, the single-stage transmitter, TRFB(D) and TRHB(D) have higher loss than TRFB(C) and TRHB(C) as shown in Fig. 4.25. On the other hand, 6.78 MHz DCM rectifier ensures smaller converter size than 70 kHz CCM. So, the efficiency comparison is emphatically made among the three topologies (single-stage converter, TRFB(D) and TRHB(D)) which have a similar converter size. The main differences among these three topologies come from the inverter stages: (1) The full bridge inverter has a larger loss in ZVS tanks and switches because every 6.78 MHz switched phase leg needs an individual ZVS tank. (2) A half-bridge inverter has larger I_{inv} than a full bridge inverter when processing the same amount of power with the same V_{bus}, causing higher conduction loss in the inverter and higher loss in the resonant tank. But this difference eventually becomes negligible due to the reduced I_{inv} when output power decreases. (3) The loss in L_{f2} is fixed over a wide load range due to constant current I_p conducted in L_{f2} and dominates other mechanisms at the low power. And it is higher in FB topology compared to HB topology due to a larger value of L_{f2} in full bridge than half-bridge inverter for a constant I_p. By combining the above three factors, the loss in TRFB(D) is higher than TRHB(D). Differently, the single-stage transmitter has lower loss than TRHB(D) at high power, whereas it could have higher loss than TRHB(D) if the light load mode operation is not applied. Once the light load mode operation replaces heavy load mode when $P_o < 50$ W, the lowest loss is achieved among the three two-stage DCM topologies over the full power range.

The topology comparison is summarized in the spider map in Fig. 4.27. Only passive components and the area of power FETs are counted in the transmitter size estimation. In terms of cost, since all of the 6.78 MHz switching power devices are GaN FETs, which contribute significantly to the main cost in the converter, the number of GaN devices is used to estimate the relative cost. The single-stage transmitter is a superior candidate for high power density and cost-effective application.

TABLE 4.1 TOPOLOGY HARDWARE COMPARISON

Topology	Rectifier operation	Schematic and operation	Device count	Volume (inch^3)		
				ZVS tanks	L_b	IMN
Single-stage	6.78 MHz DCM		4 switches+2 diodes	2×0.07	0.77	0.51
Two-stage TRFB(C)	70 kHz CCM		6 switches+2 diodes	2×0.07	4.9	0.51
Two-stage TRFB(D)	6.78 MHz DCM		6 switches+2 diodes	3×0.07	0.77	0.51
Two-stage TRHB(C)	70 kHz CCM		4 switches+2 diodes	1×0.07	4.9	0.51
Two-stage TRHB(D)	6.78 MHz DCM		4 switches+2 diodes	2×0.07	0.77	0.51

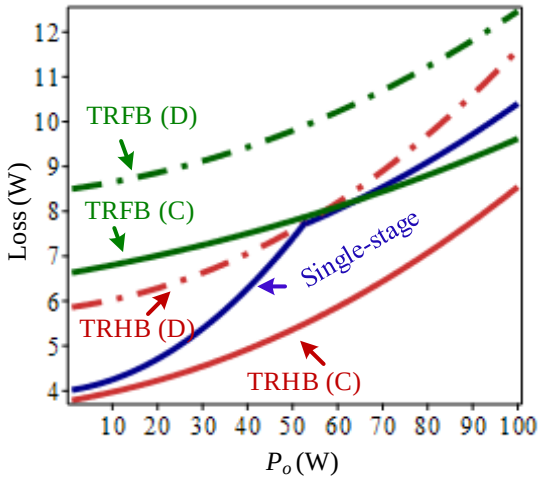


Fig. 4.25. P_{loss} comparison.

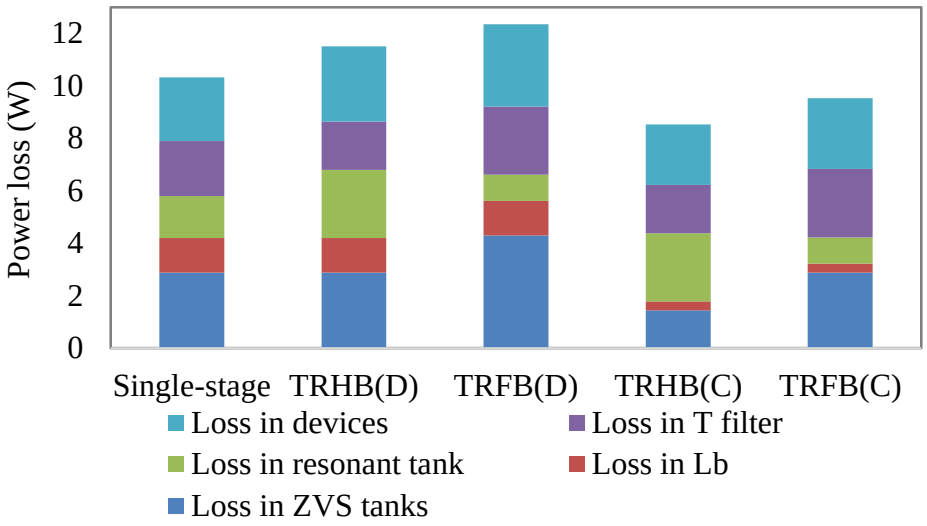


Fig. 4.26. Power loss breakdown at full power (100 W).

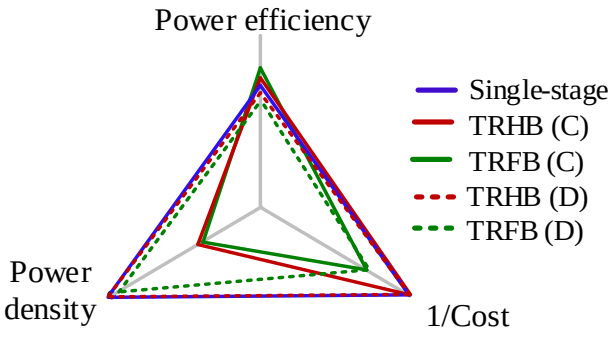


Fig. 4.27. Comparison of three topologies.

4.6 Experimental verification

A GaN-based prototype is built to verify the operation and theoretical analysis of the single-stage transmitter over the full load range. The main design parameters are listed in Table 4.2. The prototype picture is shown in Fig. 4.28.

An open-loop control algorithm is implemented in the Digital Signal Processor (DSP/TMS320F28377S) for the experiments. The input voltage is sampled at a rate of 50 kHz and fed to an ADC channel of the DSP, and an on-board phase-locked loop (PLL) synchronizes the switching to the line cycle. The duty cycle of phase leg A and the phase shift between phase leg A and B are determined according to the control trajectory in Fig. 8.

Fig. 4.29 illustrates the waveforms under full power operation (V_{in}=120V rms/60 Hz, Po=100 W, f_s=6.78 MHz). I_{in} is in phase with V_{in} and shows sinusoidal waveform. V_{bus} has negligible double line frequency ripple. The measured average bus voltage V_{bus}=327 V, while the designed value is 340 V. The 13 V discrepancy between the designed and measured bus voltage is mainly coming from the power loss in the circuit. Closed-loop control will reduce this error. The waveforms of V_a and V_b verify that both phase legs achieve soft switching. I_{inv} exhibits a sinusoidal waveform with some harmonic components while I_p is sinusoidal with low harmonic distortion.

TABLE 4.2 DESIGN PARAMETERS

Parameter	Value	Parameter	Value
V_i	120 V/60 Hz	C_{dc}	120
V_{bus}	340 V	C_{vd1}/ C_{vd2}	70 µF
P_o	0~100 W	L_b	4.5
f_s	6.78 MHz	L_r	19.86
S_1~S_4	GaN FETs	C_r	28 pF
D_1~D_2	SiC Diodes	L_{f1}/L_{f2}	2.87
M_{a1}/ M_{a2}	IPD50R1K4CE	C_f	192

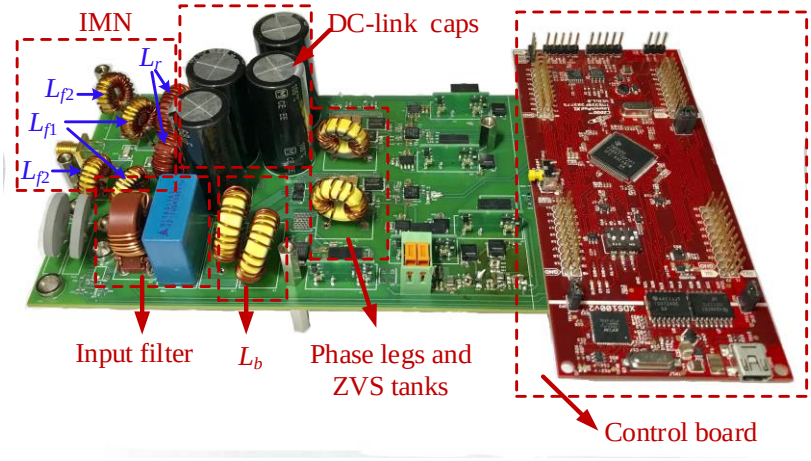
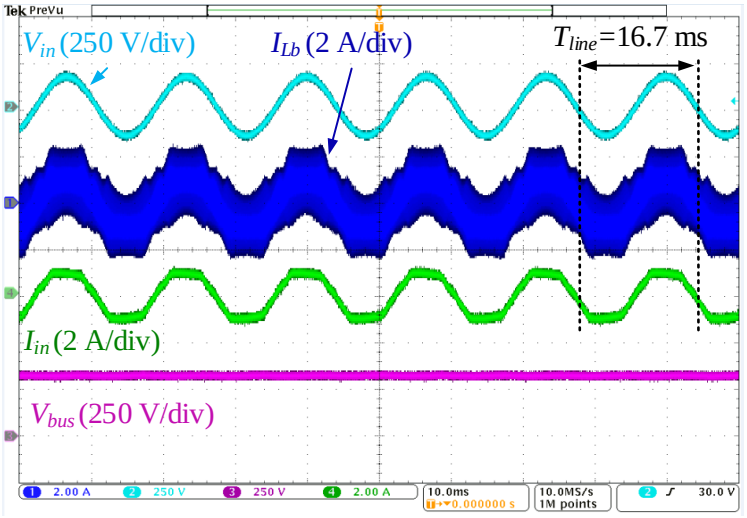
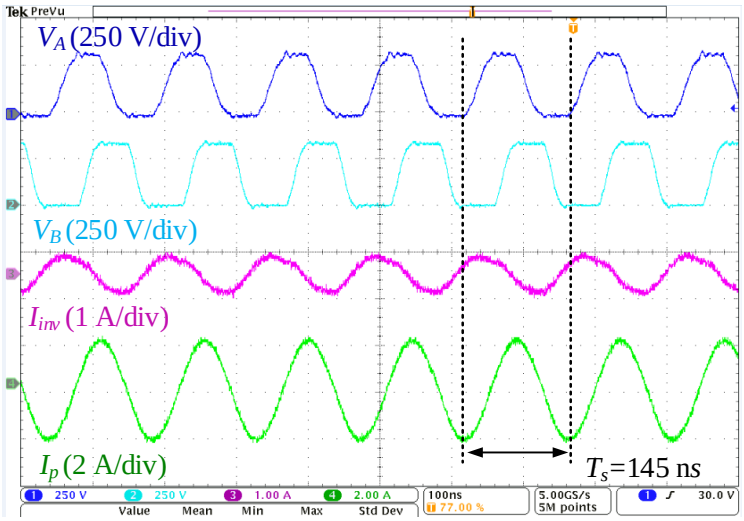


Fig. 4.28. Laboratory prototype.



(a) Rectifier



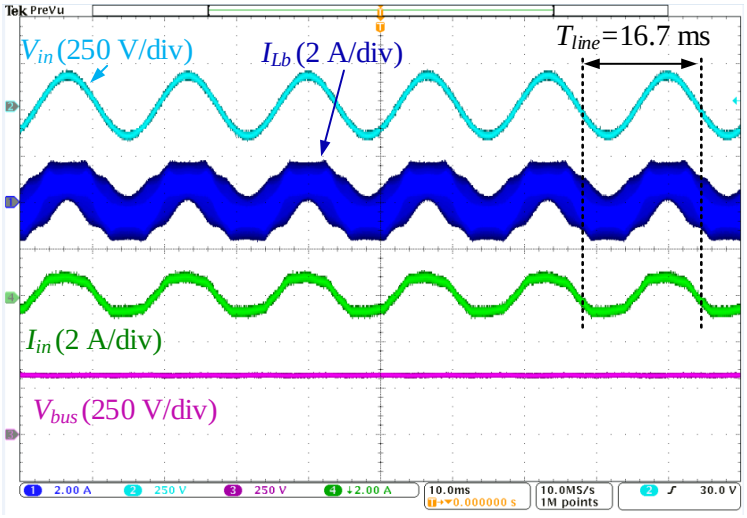
(b) Inverter

Fig. 4.29. Waveforms at full power.

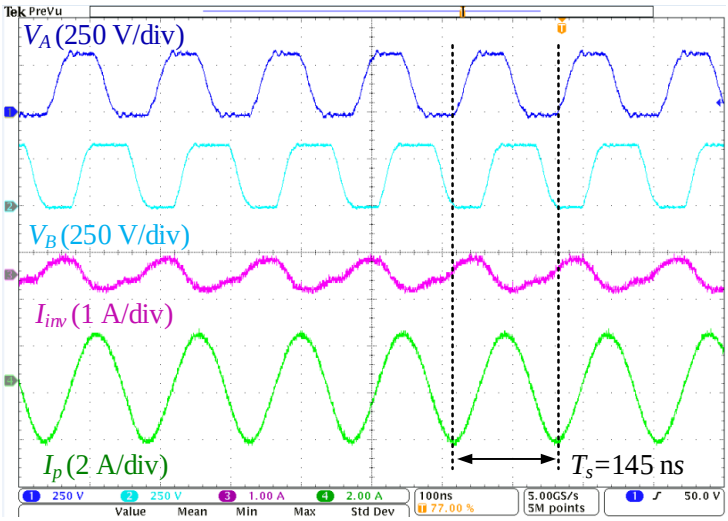
Fig. 4.30 shows waveforms under heavy load operation (V_{in}=120V rms/60 Hz, V_{bus}=323 V, Po=72 W, f_s=6.78 MHz). In Fig. 4.30(a), I_{in} maintains good performance and V_{bus} is regulated to a dc with low ripple. In Fig. 4.30(b), V_a and V_b achieve ZVS. With reduced output power, I_{inv} gets smaller than the corresponding one in Fig. 4.30(b), while I_p remains the same, indicating constant current with varying load.

The experimental waveforms in light load mode (V_{in}=120 V rms/60 Hz, Po=50 W, f_s=6.78 MHz) are illustrated in Fig. 4.31. I_{in} and I_{Lb} have the same waveform under this operation mode, thus only I_{Lb} is given. The waveform of V_d (the voltage on C_{vd2}) show the expected line frequency ripple while V_{bus} has a small double line frequency ripple. The measured V_{bus}=307 V, which matches with the estimated value in Fig. 4.31. V_a is half of V_{bus}. The turn on and turn off transitions of V_b demonstrate ZVS transitions. I_p exhibits low harmonic content.

Fig. 4.32 shows the waveforms during the transition from heavy load mode to light load mode. To achieve a smooth transition, S_1 and S_2 are turned off during their dead time, then M_{a1} and M_{a2} are turned on after 300 ns. According to Fig. 4.32(b), a few switching cycles of resonant behavior occur on switching node A after turning off S_1 and S_2 and before M_{a1} and M_{a2} on. This is caused by the load current charging/discharging the output capacitors of S_1 and S_2. This phenomenon is expected and will not impact operation. I_p has negligible disturbance during this transition.

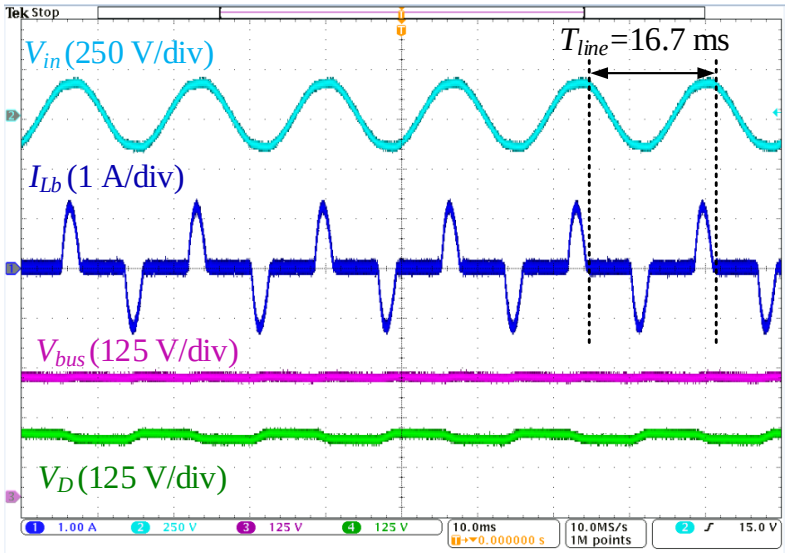


(a)

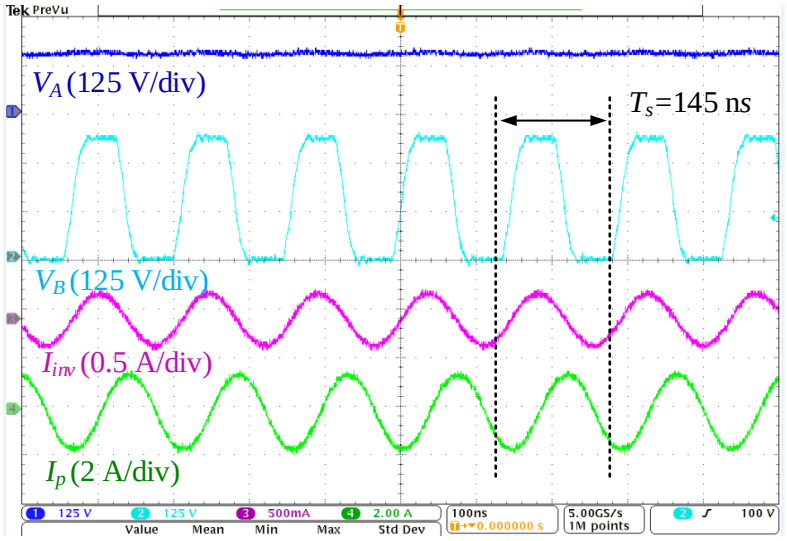


(b)

Fig. 4.30. Waveforms at P_o=72 W.

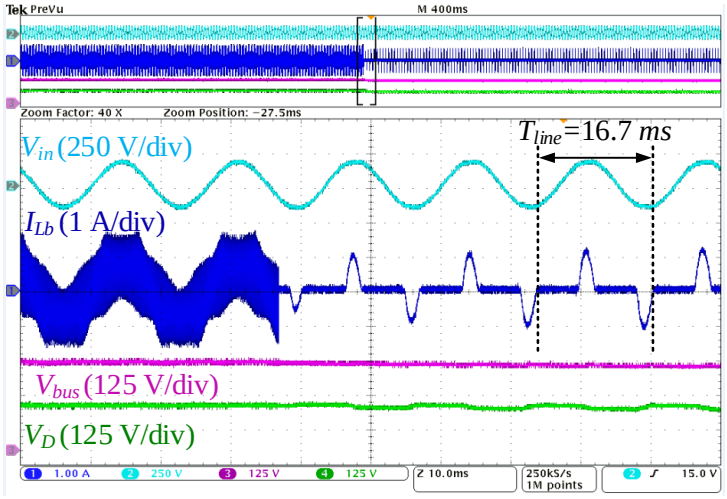


(a)

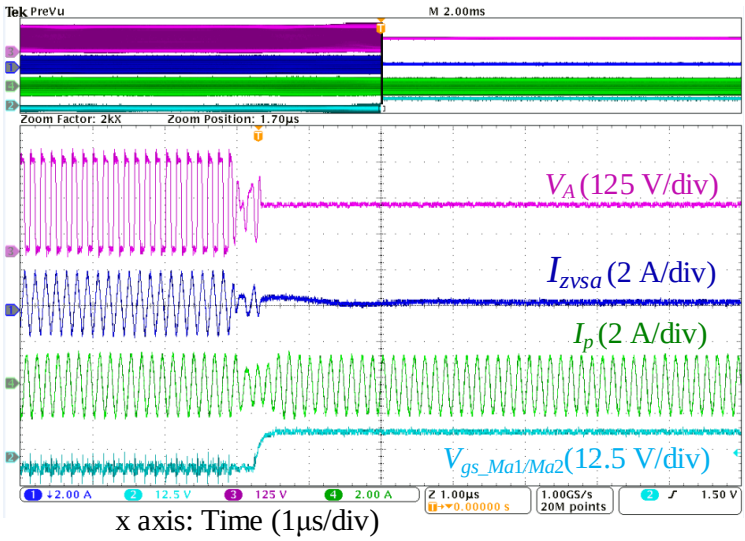


(b)

Fig. 4.31. Waveforms at light load mode (50 W).



(a)

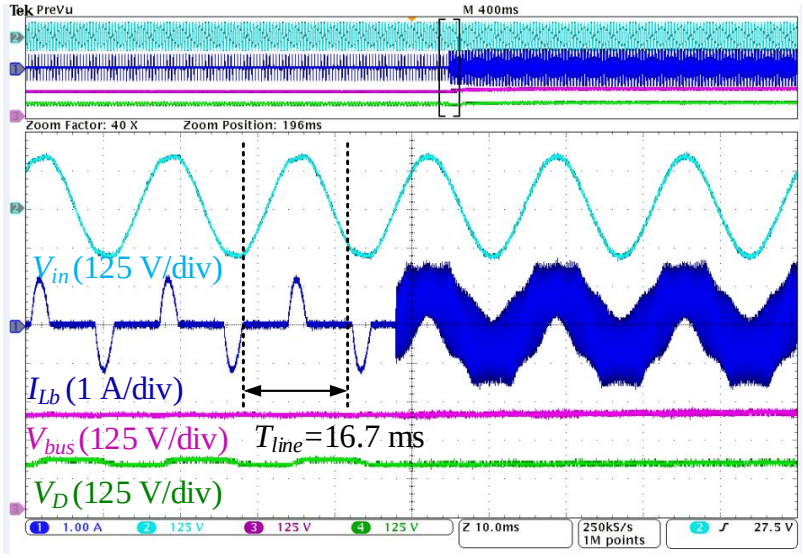


x axis: Time (1µs/div)

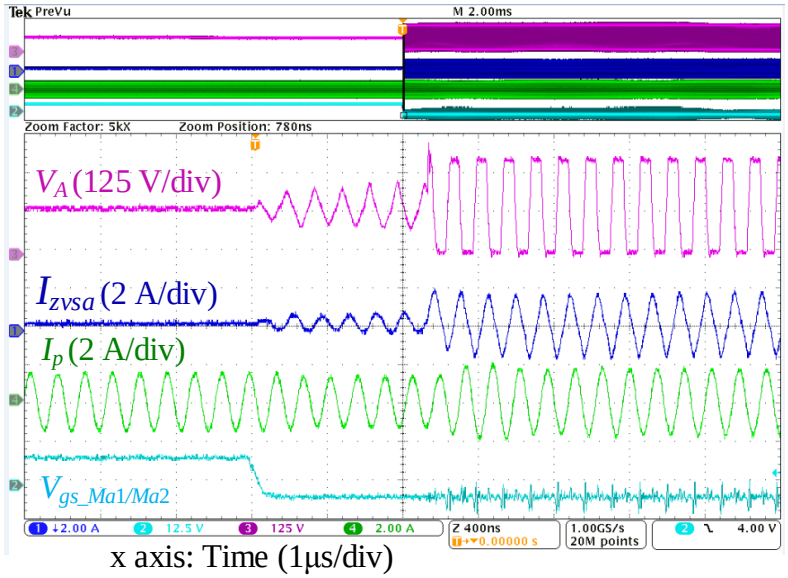
(b)

Fig. 4.32. The transition from heavy load mode to light load mode.

Fig. 4.33 shows the transition from light load mode to heavy load mode. This transit begins with turning off M_{a1} and M_{a2}. To avoid cross-conduction between M_{a1}, $M_{a2,}$ and S_1/ S_2, a delay of 300 ns is implemented before turning on S_1/ S_2. In Fig. 4.33(b), the expected resonant behavior due to charging/discharging output capacitors of S_1 and S_2 is presented during the delay time. Since ZVS tank has a near zero current, there is at least one hard switching event in the first turn-on of either S_1 or S_2. To reduce the chance of hard switching, two methods are adopted. (1) Since I_{inv} periodically charges/discharge output capacitors of S_1 and S_2 in every switching period. It is better to turn on S_1 when V_a resonates to the positive peak value or turn on S_2 when V_a reaches the smallest value. (2) The first turning on pulse for S_1/ S_2 is set to be half of the normal on time. Thus, the ZVS tank current will reach the steady-state after the first PWM pulse. Those two methods are verified by the waveforms in Fig. 4.33(b). S_1 is turned on with small voltage stress. S_1 and S_2 achieve soft switching starting with the second switching period. I_p has negligible disturbance during this transition.



(a)



x axis: Time (1μs/div)

(b)

Fig. 4.33. The transition from light load mode to heavy load mode.

The constant current behavior has been verified at heavy load mode. Fig. 4.34 shows the RMS value of I_p changes less than 6% at a wide output power range.

The measured THD and PF of input current are addressed in TABLE 4.3.High PF and low THD are achieved. The measured harmonic current and the harmonic current limitation from IEC 61000-3-2 Class D as a function of different harmonic orders are given in Fig. 4.35. The results verify that the PFC of single-stage transmitter meets the requirement.

The harmonic distribution of output current I_p under full power is analyzed. Each harmonic component, normalized by the 6.78 MHz fundamental current, is given in Fig. 4.36. As seen, the low harmonic under the wide spectrum is achieved. The total harmonic distortion of I_p at full power is 3%.

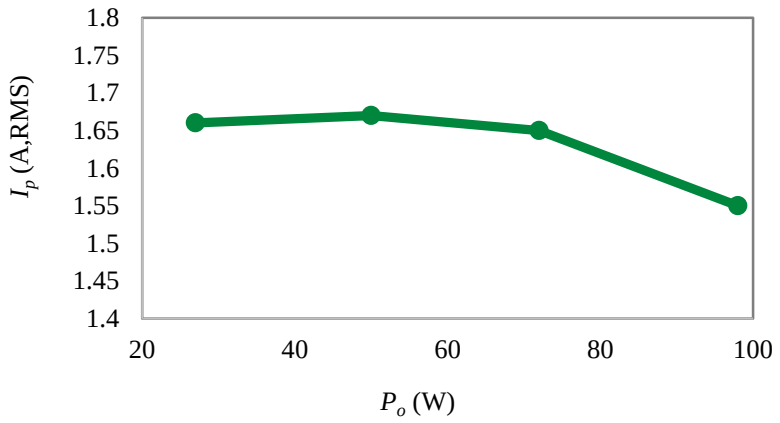


Fig. 4.34. Experimental results for constant transmitter coil in the heavy load mode

TABLE 4.3 MEASURED INPUT CURRENT PERFORMANCE

P_o	PF	THD
98 W	0.99	10.2%
72 W	0.987	12%
50 W	0.98	14.3%

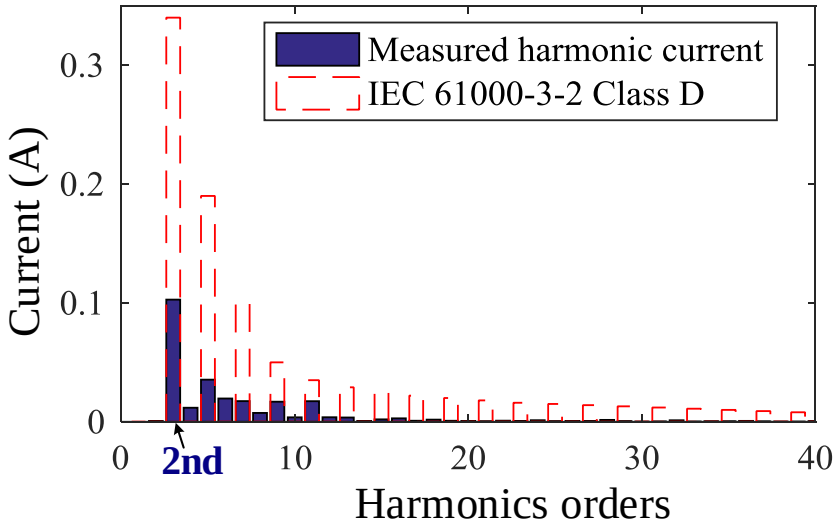


Fig. 4.35. Harmonics analysis of $I_{in.}$

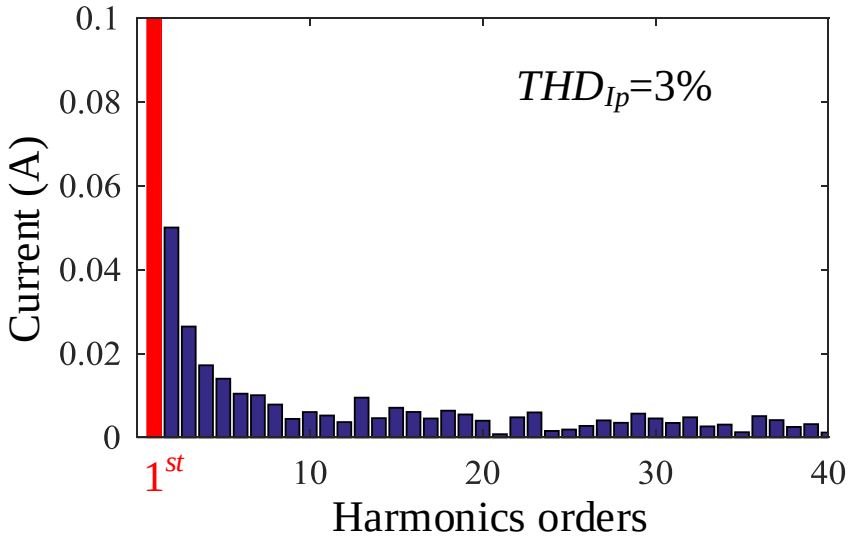


Fig. 4.36. Harmonics analysis of $I_{p.}$

Fig. 4.37 gives the measured and calculated power loss. The DSP power and all auxiliary supplies, including the gate driver supplies, are powered by a separate benchtop voltage source, and not included in the calculations. There is approximately 2.2 W power supplied from the auxiliary source during operation. Experimental power loss matches well with the analytical prediction. To get the maximum efficiency, the single-stage transmitter should operate in heavy load mode when P_o>50 W, and work at light load mode when P_o<50 W, as predicted. Fig. 4.38 shows the power efficiency curve of this proposed single-stage transmitter. The transmitter achieves 90.4% efficiency at 98 W. By employing the light load mode, the efficiency is increased by 5% at 23 W. Light load efficiency may be further improved in the future work by altering the operation to reduce coil current when permissible, which will depend on the number, power level, and coupling of the receivers present.

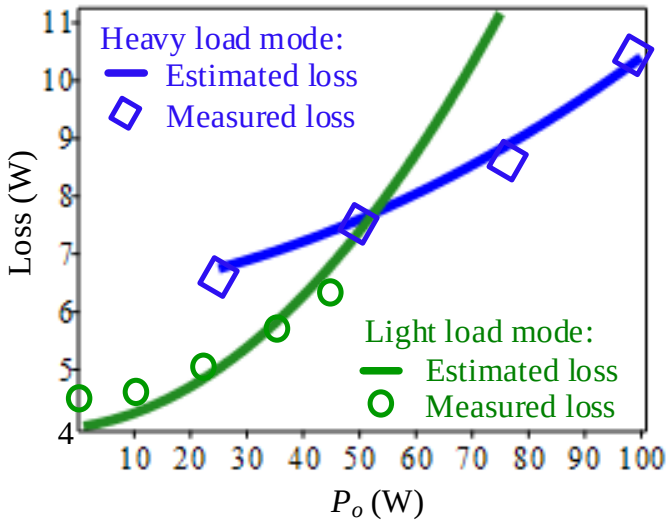


Fig. 4.37. Measured loss.

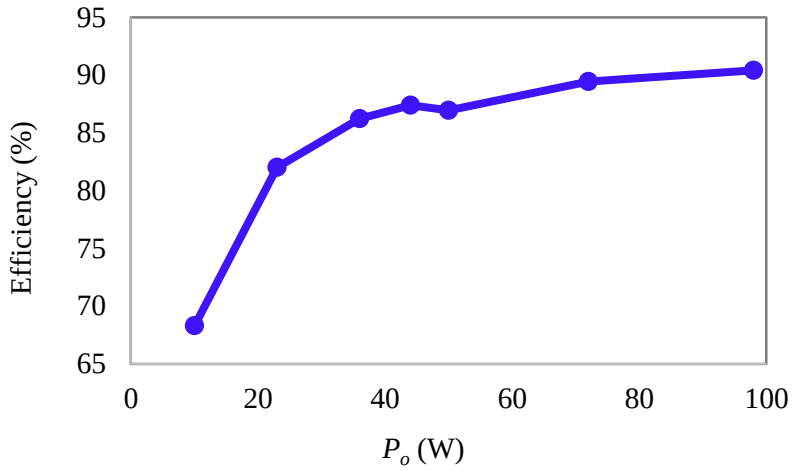


Fig. 4.38. Measured power efficiency.

4.7 Summary

This chapter proposes a single-stage transmitter with high efficiency over a full range of load in WPT application. By integrating a totem-pole rectifier and a full bridge inverter, two fewer GaN FETs are required. Compared with two-stage TRFB and TRHB transmitter, this single-stage transmitter has high power density, high efficiency, and low cost. Constant output current behavior is achieved. This feature enables the fast response to the sudden load change and is beneficial to the multiple receiver application. An auxiliary circuit is added to maintain high efficiency at light load while contributing negligible extra cost and size. The theoretical analysis, operation principle and design considerations of this single-stage transmitter are verified by a laboratory prototype. Experimental results demonstrate 90.4% efficiency at 98 W. Measured THD of the input current is 10.2%, and PF is 0.99 at full power. The output current of the transmitter is a 6.78 MHz sinusoid with 3% THD. Light load mode operation is verified with high efficiency. Smooth transitions between light load mode and heavy load mode are obtained

in the prototype. Future work includes the implementation of close-loop control and verification of the operation with multiple receivers.

5 DYNAMIC OPERATION OF SINGLE-STAGE TRANSMITTER

The transmitter should respond adequately against the receiver position changes or load variation. In addition, it should provide smooth dynamic transition and robust operation over full power range. Therefore, the closed-loop control scheme is investigated in this chapter to achieve this goal. The control targets:

(1) Support to dynamically adjust the delivered power according to the requirement of the receivers.

(2) Allow the transmitter to operate over a wide power range.

(3) Include ZVS detection and protection function.

With this control scheme, the single-stage transmitter is applicable for the multiple receiver application. I_p is provided at the transmitter output. Each receiver employs an autonomous control scheme to draw the required power individually.

5.1 Constant output current regulation in the heavy load mode

As discussed in the previous sections, constant transmitter current helps smooth the dynamic transition. The control goal discussed in this section is to achieve current source behavior for transmitter current I_p.

The proposed control scheme is shown in Fig. 5.1. The constant transmitter coil current is achieved by three steps. First, closed-loop feedback control is used to regulate V_{bus}. Then, the model-based controller is used to achieve constant V_{ab1}. Last, the IMN generates a constant I_p from constant V_{ab1}. A phase-locked loop (PLL) in the control loop detects the phase angle of the input voltage. Due to the bridgeless rectifier operation, the gate signals of the upper device and bottom device are switched in every half-line period.

5.1.1 Constant V_{bus} regulation

Constant I_p is achieved based on constant V_{ab1} and the design of the IMN. Constant V_{ab1} is obtained based on AVC modulation, assuming a constant V_{bus}. Thus, constant V_{bus} has to be ensured. The control diagram used to regulate constant V_{bus} is shown in Fig. 5.2. The transfer function G_{vd} ($V_{bus}(s)/d(s)$) is derived based on the DCM boost rectifier model and a PI controller G_c(s) is developed. By sensing V_{bus} and feeding it back to this PI controller, the duty cycle d_a is updated in every control cycle to regulate V_{bus}.

The impedance of boost inductor L_b at low-frequency is negligible. Therefore, the approximate small signal ac model is used to derive the transfer function G_{vd} of the DCM boost rectifier:

$$G_{vd}(s) = \frac{V_{bus}(s)}{d_a(s)} = \frac{\frac{2V_{bus}(M-1)}{d(2M-1)}}{1 + \frac{(M-1)R_{load} \cdot C_{dc}}{2M-1} \cdot s} \tag{5-1}$$

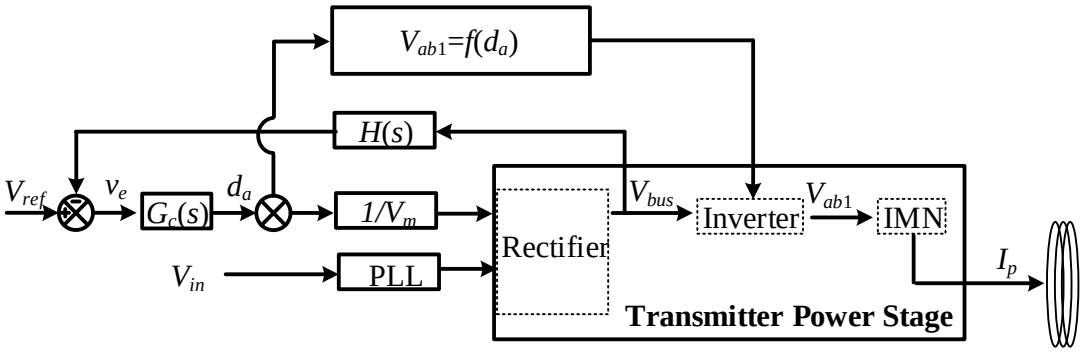


Fig. 5.1. Closed-loop control diagram for constant transmitter coil current.

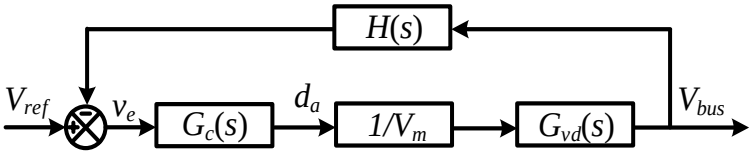


Fig. 5.2. The closed-loop control diagram for V_{bus}.

With the value of the bus voltage, M and load in steady-state operation, the open loop gain is obtained according to (5-1). In this work, the input voltage is 120V/60 Hz, and the bus voltage is 340V. The peak value of the input voltage is considered as the operating point for this model. The system open loop gain is shown in Fig. 5.3. A PI controller $G_c(s)$ is developed to ensure the stability, attenuation at the switching frequency and the accuracy of the system control. The closed-loop gain $G_{vd}(s)\cdot G_c(s)$ is plotted in Fig. 5.3Fig. 5.3. Bode plot of voltage control loop.

5.1.2 Constant V_{ab1} regulation

By sensing V_{bus} and regulating through the feedback PI controller, the duty cycle of phase leg A, d_a is updated to regulate V_{bus}. Then, according to (4-14) and (4-16), for a fixed V_{ab1}, $\alpha_+ = \xi(\beta_a)$ is calculated based on the real-time input parameter d_a. The curve of α_+ with respect to β_a is given in Fig. 5.4. However, $\xi(\beta_a)$ is a complicated equation which requires a large amount of calculation effort in DSP. A simplified equation obtained by curve fitting is used in practice

$$\alpha_+ = 0.038\beta_a^3 - 0.532\beta_a^2 + 2.68\beta_a - 3.078 \qquad (5\text{-}2)$$

The approximation of (5-2) is shown in Fig. 5.4, and matches well with the original curve. The control speed of this model based feedforward controller is elaborate. It directly uses the duty cycle value β_a from the voltage loop controller for the phase shift calculation $phi = \beta_a - \alpha_+$. The constant V_{ab1} is obtained by following this trajectory in Fig. 5.4.

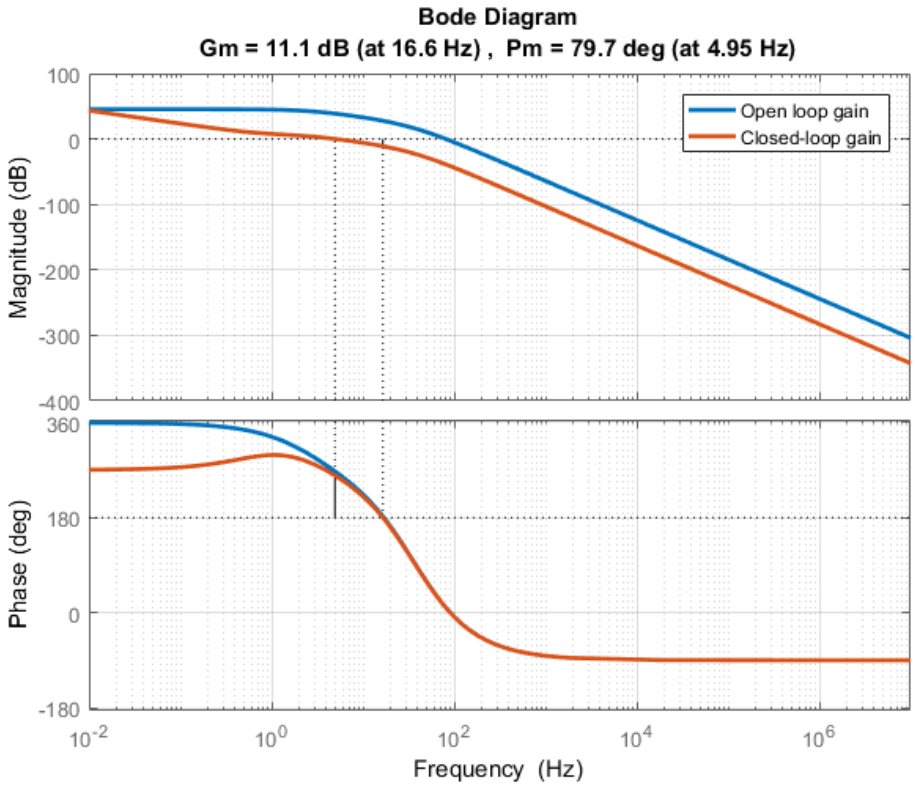


Fig. 5.3. Bode plot of voltage control loop.

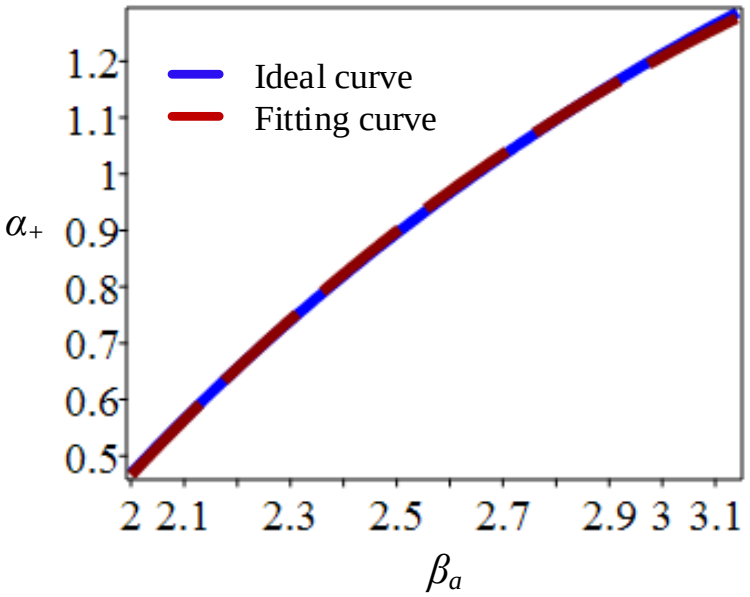


Fig. 5.4. Control trajectory for constant V_{ab1}.

5.1.3 The achievement of Constant I_p

Based on constant V_{ab1}, constant I_p is obtained at the output of IMN in Section 3.4.3.The achievement of constant I_p is verified in the simulation and shown in Fig. 5.5. A 100 W to 60 W resistive load step occurs at t_1. When processing the load step changes at t_1, the bus voltage starts to increase and then drops back to the targeted value quickly. During this transition, the output current of transmitter I_p remains nearly constant.

5.2 Single-stage transmitter dynamic operation over full power range

5.2.1 Dynamic operation in light load mode

The dynamic operation with constant I_p in heavy load mode is achieved via a closed-loop control scheme presented in Section 5.1. In the light load mode, with the independent half-bridge operation, V_{ab1} is naturally closed to a voltage source, so with the IMN, constant I_p can be achieved. Fig. 5.6 shows the simulation results for the verification of constant I_p in light load mode with load step changes. At t_1, the load is changed from 40 W to 20 W.

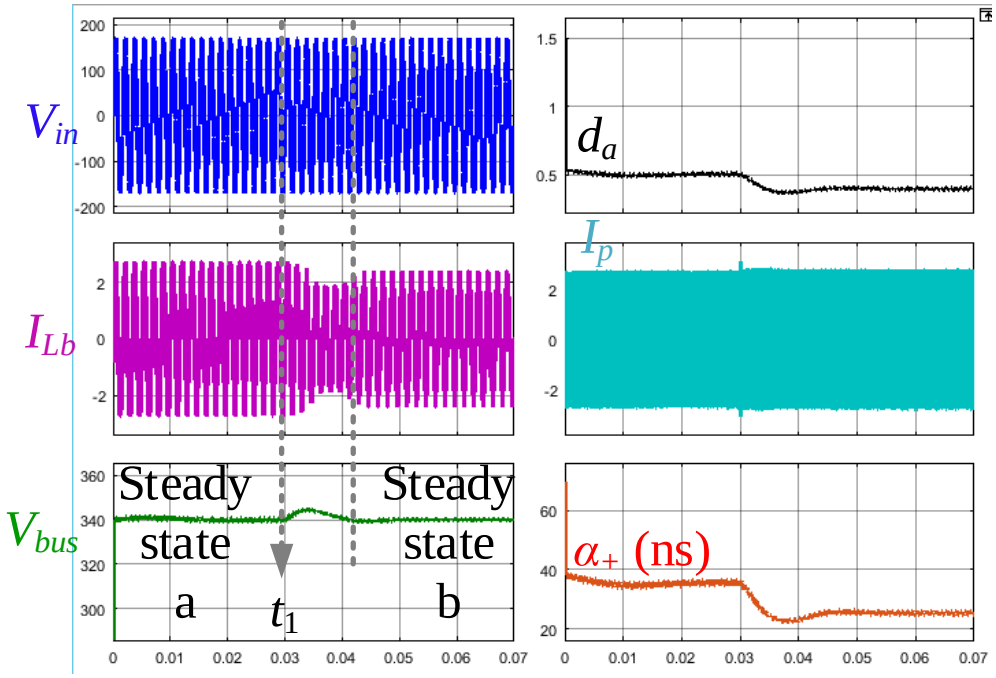


Fig. 5.5. Constant current achievement in heavy load mode in the simulation.

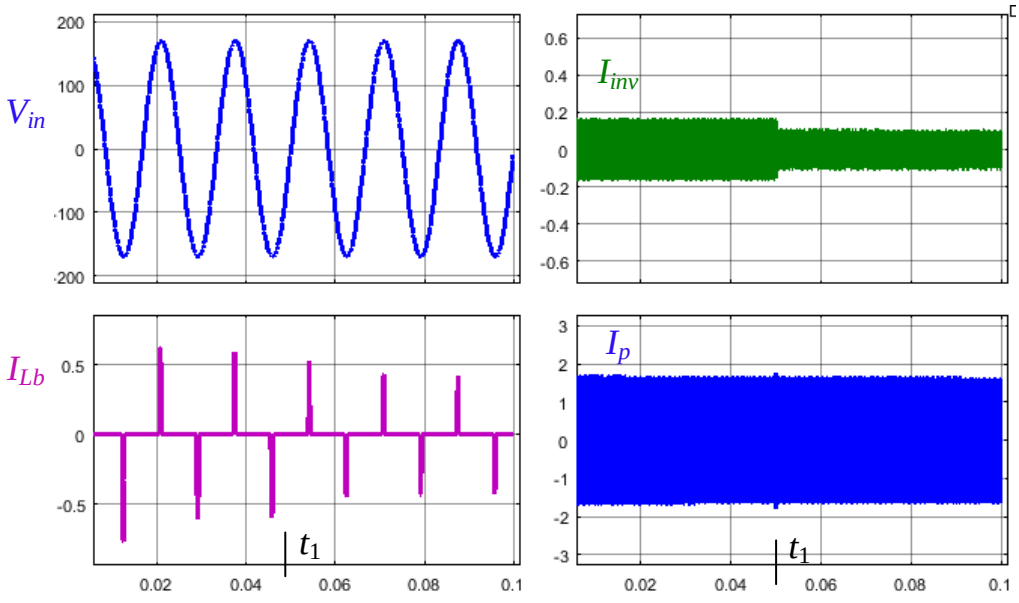


Fig. 5.6. Constant current achievement in light load mode in the simulation.

5.2.2 Operation boundaries

Although I_p can maintain constant within an individual operation mode, it might be different between these two modes. In order to operate across no load to full load, this single-stage transmitter switches between two modes.

Constant I_p is designed to smooth the load transition as discussed previously. However, constant I_p is not always preferred when considering the system operation and efficiency during steady state. In a word, the method and goal of regulating I_p are classified into two causes. During the dynamic period, I_p is controlled to keep constant. After the system is stabilized in the new operating point, it is adjusted to achieve system optimum operation. The details about this motivation and procedure of changing I_p during operation will be discussed in the next chapter. The operating boundary of I_p and the trajectories for dynamic adjustment are addressed in this section.

The value of I_p is determined by the IMN and V_{ab1}. I_{p_max} is defined as the operational maximum transmitter coil current. The value of I_{p_max} is selected according to system design, such as the safety requirement, coil to coil efficiency and the allowed minimum mutual inductance for certain power delivery. In this work, I_{p_max}=2 A. V_{ab1_max} is selected according to the transmitter operation. In this transmitter, V_{ab1_max}=346 V as discussed in Chapter 4. According to I_{p_max} and V_{ab1_max}, the IMN is then designed. With a fixed IMN, different I_p are obtained by changing V_{ab1}. Due to the full bridge inverter topology, V_{ab1} is controlled by d_a, d_b and phase shift *phi* between the two-phase legs. So, V_{ab1} is able to be regulated from V_{ab1_max} to 0. Therefore, the minimum achievable I_p in the heavy load mode is near 0 A.

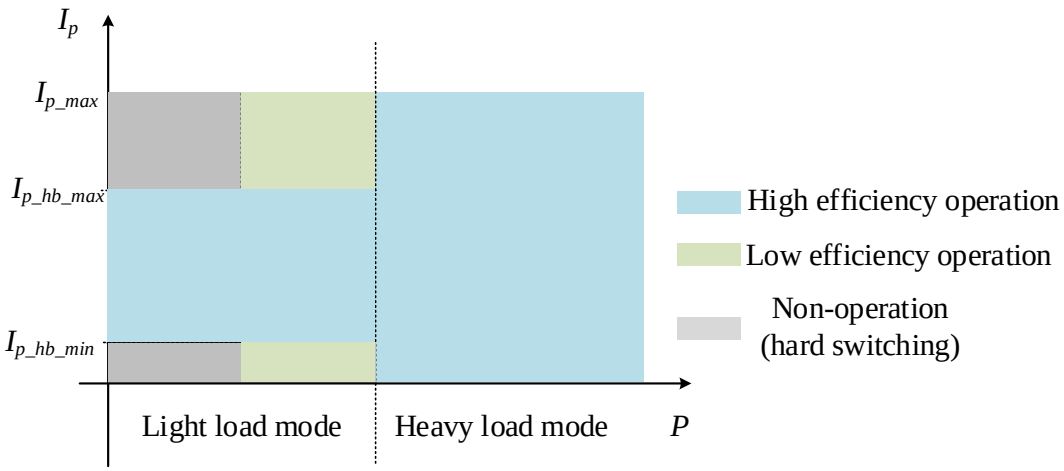
In light load mode, the full bridge inverter is replaced by a half-bridge inverter. The maximum V_{ab1} in this mode is reduced compared with heavy load mode. Based on the V_{bus} and IMN in this design, $V_{ab\_hb\_max}$=216 V, and $I_{p\_hb\_max}$=1.25 A. Since d_b is the variable used to adjust I_p in the light load mode, the minimum I_p is limited by d_b. The duty cycle limit for phase leg A is discussed in Section 4.2 is also applicable to d_b. In order to maintain ZVS operation, d_b should be maintained above 0.25 for the ZVS tank, as designed in Section 4.2. In this case, $I_{p\_hb\_min}$=0.88A.

The boundaries of the operation are summarized in Fig. 5.7(a). The blue area is the preferred operation area. In the heavy load, I_p is able to change from zero to I_{p_max}. In the light load mode, I_p is limited by the half-bridge inverter operation. The green area where 25 W<P_o<50 W is an operational area, but it is not preferred due to low efficiency according to the loss curve shown in Fig. 4.24. Hard switching occurs in the grey area. So, control effort should be made to avoid operation in this area.

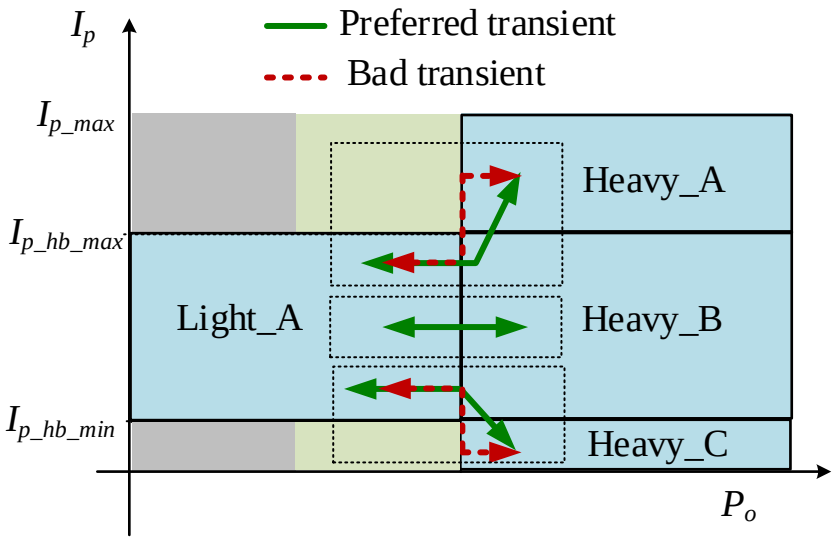
Constant I_p can be maintained in the heavy load mode. A different value of I_p might be obtained after transitioning to light load mode. When the required power changes widely, the transmitter needs to switch between these two modes. During the mode switching transient, I_p changes under some conditions. The transmitter operational area is split into four sub-areas, as shown in Fig. 5.7(b). If the modes are switched between Light_A and Heavy B, I_p is able to maintain constant. However, if the mode switches between Light_A and Heavy_A, or Light_A and Heavy_C, then I_p cannot keep constant. If the receivers do not have active switches (for example, only have a diode rectifier), the power delivered to the receivers will change unexpectedly. However, in practice, receivers typically are actively controlled [24],[139]. A traditional way is to add a subsequent dc-dc converter at

the output of diode rectifier for output voltage/power regulation. Especially in the multiple receiver application, the independent regulation of power flow to each receiver cannot be achieved by a single controller at the transmitter side. Various types of receivers require a different amount of power at different charging stages. So, system operation requires receivers have individual control for output regulation. When I_p changes, receivers still have the capability of regulating power independently with this dc-dc converter. Depending on the implemented dc-dc converter, regulation is limited. The receiver regulation range and system operating range will be discussed in the next chapter.

Assuming the receivers in the system have autonomous control capability. The rectifiers can still obtain the required power or/and constant output voltage with the change of I_p at different operation modes. However, if I_p changes abruptly, it will bring voltage overshoot or undershoot at the receiver side. To improve the dynamic performance, I_p is controlled to be gradually adjusted to the desired value in the current operation mode. Then, transitions between modes occur with constant I_p during the transient. This idea is presented in Fig. 5.7(b). The preferred control trajectory for I_p is shown in the green curve.



(a) Operation boundary.



(b) Consideration of preferred transient trajectory.

Fig. 5.7. Operation boundary over full power range.

5.2.3 Wide power range operation

To obtain high efficiency at wide load range, heavy load mode and light load mode should be enabled at the proper operating range as discussed in section 4.4. The transmitter operates in light load mode for P_o < 50 W, and in heavy load mode for 50 W < P_o < 100 W for low loss according to Fig. 4.24. So, the mode transition occurs at power near 50 W. There are different methods to sense the real-time power, including (1) monitoring the input voltage and input current, then calculating power in the controller, or (2) detecting the output current and voltage. However, considerable effort has to be made to detect output parameters due to high frequency operation. To save the extra sensing effort, known parameters d_a and V_{bus} are proposed to estimate the power. By utilizing this approach, the control diagram considering mode switching is shown in Fig. 5.8.

As discussed above, d_a is adjusted to maintain constant V_{bus} via the voltage loop at different load condition. In other words, d_a indicates the power level when operating in heavy load mode. According to Fig. 4.6, d_a is 0.35 when power is near 50W. Define $d_{a,min}$=0.35. When $d_{a,min}$>0.35, indicating P_o>50 W, the converter operates in heavy load mode. When d_a< $d_{a,min}$, the converter switches to light load mode to maintain high efficiency. During load transitions, the duty cycle might have undershot as shown in Fig. 5.5. To avoid false triggering from overshoot during the transition, a delay time t_{delay} is set in the controller. If d_a maintain below 0.35 for a time longer than t_{delay_htl}, the mode switching process is triggered. In practice, a counter $t_{counter}$ in the controller is used to monitor the time when d_a< $d_{a,min}$ is sensed. So, when both d_a< $d_{a,min}$ and $t_{counter}$ < t_{delay_htl} are satisfied, the process of switching from heavy load mode to light load mode is started. Another constraint is added to avoid hard switching operation. As discussed in Chapter 4,

the transmitter runs into hard switching when d_a <0.25. Thus, d_a is clamped at 0.25 in the controller when the feedback loop asks for a lower value.

When the converter works in light load mode, d_a cannot be used to estimate the power because of VDR operation. But, the average bus voltage changes along with the load during light load mode as shown in Fig. 4.12. Thus, the sensed V_{bus} is used to estimate the power level in light load. Since the converter will not operate in light load mode at power level higher than 50 W, V_{bus,min_light} is defined at P_o=50 W according to Fig. 4.12. The condition for switching from light load mode to heavy load mode is $V_{bus} < V_{bus,min\_light}$. To avoid erroneous switching actions caused by noise in the sensing circuit, a delay time is implemented. Only when V_{bus} is lower than V_{bus,min_light} for a duration of t_{delay_lth}, will mode switching occur.

To avoid overloading of this converter, the allowed maximum power is defined and the method of monitoring this overload is implemented. According to (4-3), the relation between V_{bus} and input current i_{in} is derived based on d_a, for a fixed L_b and f_s

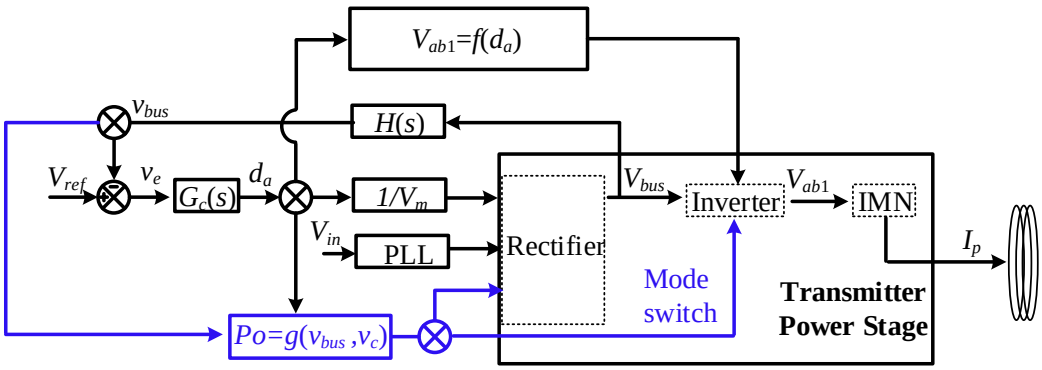


Fig. 5.8. Control diagram with mode switching for a wide power range.

$$V_{bus} = \frac{2 \cdot L_b \cdot f_s \cdot V_m}{2 \cdot L_b \cdot f_s - \frac{d_a^2 \cdot V_m \cdot \sin(2\pi f_{line} \cdot t)}{i_{in}(t)}} \quad (5\text{-}3)$$

The maximum duty cycle d_{a_max} is determined as 0.5 in Chapter 4. At full load, d_a approaches d_{a_max}. If the power is further increased, d_a maintains at d_{a_max}, and the bus voltage starts to drop, as shown in Fig. 5.9. Generally, the allowed maximum power is limited by the rating of hardware components. In this converter, the current rating of the GaN FET is 8A, and the peak current rating of the diode is 4.5A. Considering the derating factor 0.7, the allowed peak current is 3A. Based on this limit, $I_{in\_rms\_max}$=1.05 A, and P_{max}=126 W. According to the plot, d_a=d_{a_max} and V_{bus}<V_{bus,min_heavy}=320 V are utilized to determine the overload condition.

According to the discussion above, the control flowchart for the single-stage transmitter at full power range operation is shown in Fig. 5.10. The transmitter starts at light load mode. During the startup period, VDR charges V_{bus} from 0 to $2V_m$ via diodes. So, soft start is achieved.

In the light load mode, the transmitter monitors power by sensing V_{bus}. If V_{bus}>V_{bus,min_light}, it keeps running in this mode for high efficiency. If V_{bus} maintains higher than V_{bus,min_light} for t_{delay_lth} , the transmitter switches to heavy load mode.

In the heavy load mode, d_a is adjusted by voltage loop controller. If d_a< d_{a_min} for t_{delay_htl}, transmitter switches back to light load mode. If d_{a_min}< d_a <d_{a_max}, it maintains in heavy load mode. If d_a keeps at d_{a_max} and V_{bus,min_heavy} <V_{bus}< V_{bus,min_norm}, the transmitter runs above the rated power level, but is still in the safe range. If V_{bus}<V_{bus,min_heavy}, the transmitter should shut down to prevent component damage from overloading.

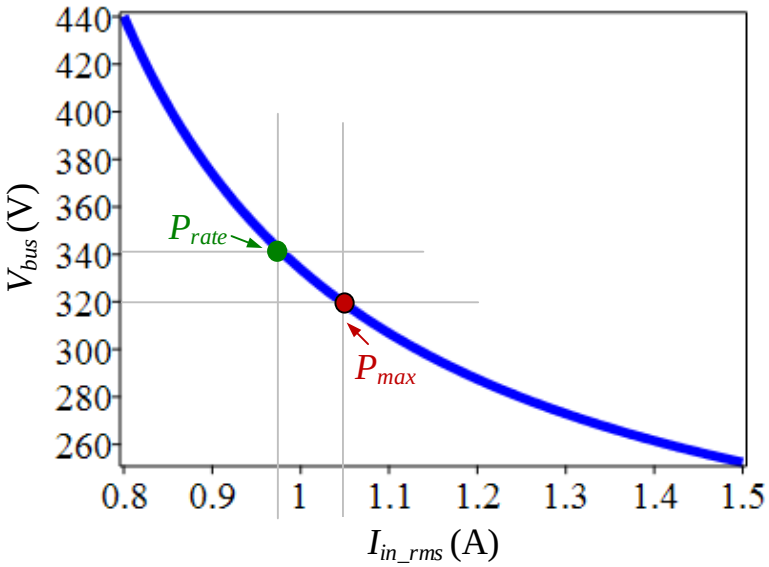


Fig. 5.9. The definition of P_{max}.

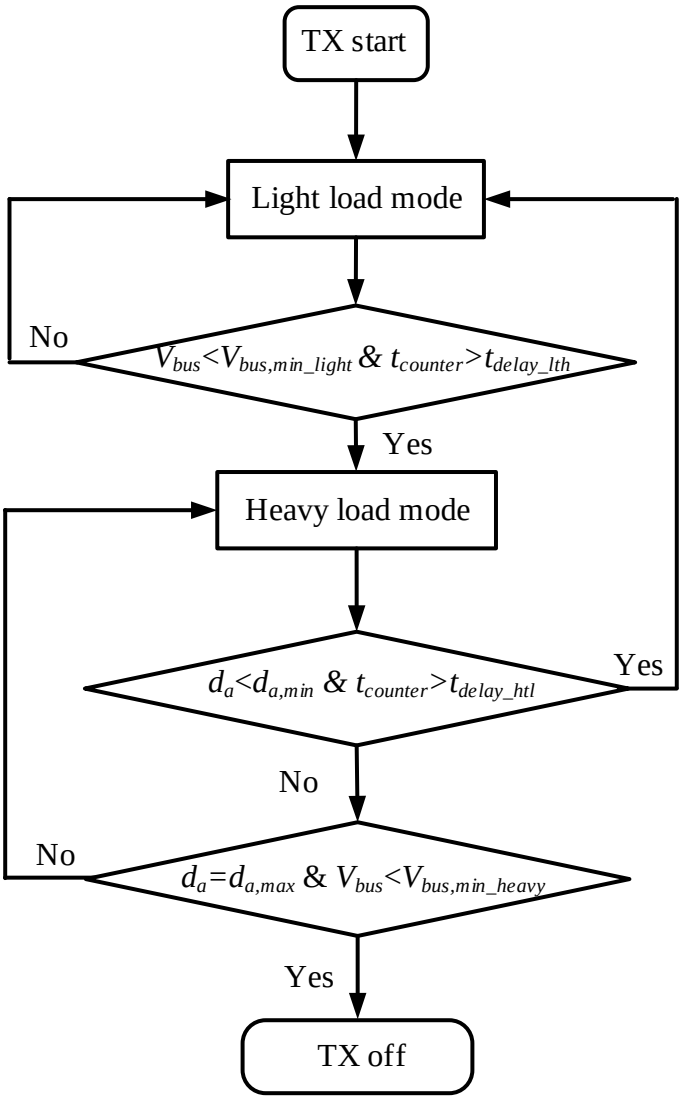


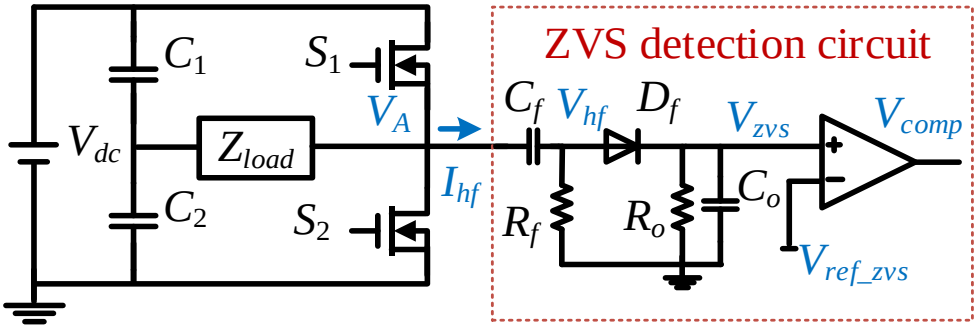
Fig. 5.10. Control flow chart for wide load range operation.

5.3 ZVS detection

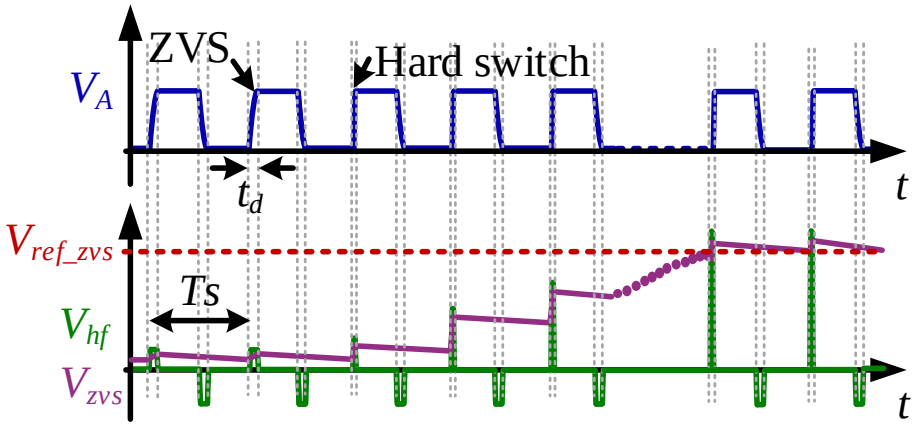
5.3.1 Operation principle

A simple and effective ZVS detection method with negligible power loss is introduced in this section. The voltage slope of the switching node is sensed and converted to a dc voltage. This dc signal is used to detect ZVS status without the assistant of auxiliary switches.

Fig. 5.11(a) shows the schematic of the proposed ZVS detection method. A half-bridge inverter (S_1, S_2, C_1 and C_2) is utilized to demonstrate the ZVS detection principle. This detection circuit consists of a high pass filter and a half-wave rectifier. C_f and R_f form a high pass filter, resulting in a voltage V_{hf} with the magnitude proportional to the switching node dV_A/dt. Since ZVS operation gives low dV_A/dt and hard switching provides high dV_A/dt, the amplitude of V_{hf} indicates ZVS status. In order to sense the magnitude of V_{hf} , a half-wave rectifier (D_f, R_o and C_o) is used to convert pulse-wave V_{hf} to a dc voltage V_{ZVS}. V_{th} is the threshold voltage that is used to distinguish ZVS and hard switching. The output of comparator presents ZVS status by comparing V_{ZVS} to V_{th} . Because of the half-wave rectifier, the only upper device is detected in this detection circuit in Fig. 5.11. A slight modification can be implemented to enable ZVS detection for both upper and bottom devices as shown in Fig. 5.14.



(a) Schematic



(b) Waveforms

Fig. 5.11. ZVS detection method in half-bridge configuration.

5.3.2 Design considerations

C_f is added to the switching node, so small capacitance is preferred in this circuit. In this work, C_f is selected according to the available lowest capacitance. In addition, the voltage rating should be higher than V_{dc}.

There are several considerations for the selection of R_f. To get the voltage slope dV_A/dt, the cutoff frequency of this high pass filter f_o is much higher than switching frequency $f_o >> f_s$, where $f_o = 1/(2\cdot\pi\cdot R_f\cdot C_f)$. In addition, small resistance should be selected to limit the power loss on R_f. The power dissipated in the resistor $P_{dis} \approx (C_f\cdot dV_A/dt)^2\cdot R_f$. Moreover, R_f, R_o and C_o will impact the steady-state value and transient values of V_{ZVS}.

The steady-state value of V_{ZVS} represents the peak magnitude of dV_A/dt. The transient of V_{ZVS} determines the delay time of ZVS detection. The relation between V_{ZVS} and design parameters (R_f, D_f, R_o and C_o) will be discussed next.

The current flows through C_f is $I_{hf} = C_f\cdot dV_A/dt$. Based on the operating point, dV_A/dt is determined, and I_{hf} is considered as a current source. The ZVS detection circuit is simplified as shown in Fig. 5.12(a). During the rising edge of V_A, I_{hf} flows through R_f and the half-wave rectifier. The time duration of this period is t_d. The equivalent circuit is shown in Fig. 5.12(b). The forward voltage of D_f is V_d. A Schottky diode with small V_d is preferred in this circuit. During the rest of the period (T_s-t_d), C_o is discharged through R_o as shown in Fig. 5.12(c). By averaging V_{ZVS} in one switching period

$$C_o \frac{d\langle V_{zvs}\rangle_{T_s}}{dt} + \left(\frac{d}{R_f} + \frac{1}{R_o}\right)\cdot\langle V_{zvs}\rangle_{T_s} - d\left(I_{hf} - \frac{V_d}{R_f}\right) = 0 \qquad (5\text{-}4)$$

where $d = t_d/T_s$. T_s is the switching frequency. Then $\langle V_{ZVS}\rangle_{Ts}$ is

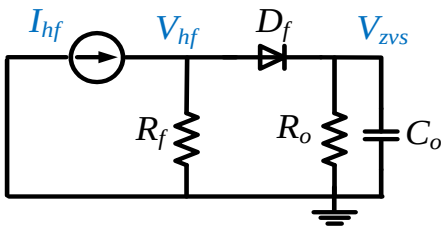
$$\langle V_{zvs}\rangle_{T_s}(t) = \frac{d\cdot\left(I_{hf}-\frac{V_d}{R_f}\right)}{\frac{d}{R_f}+\frac{1}{R_o}}(1-e^{-\frac{t}{\tau}}) + \langle V_{zvs}\rangle_{T_s}(t_-)\cdot e^{-\frac{t}{\tau}} \quad (5\text{-}5)$$

where $\langle V_{ZVS}\rangle_{Ts}(t_-)$ represents initial average V_{ZVS}, and $\tau = C_o/(d/R_f + 1/R_o)$. V_d is small if implementing Schottky diode and R_f is relatively large, so V_d/R_f in (5-5) is negligible. According to (5-5), V_{ZVS} during steady state is approximately

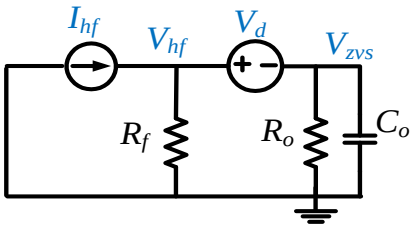
$$\langle V_{zvs}\rangle_{T_s} \approx \frac{d\cdot I_{hf}}{\frac{d}{R_f}+\frac{1}{R_o}} + \langle V_{zvs}\rangle_{T_s}(t_-) \quad (5\text{-}6)$$

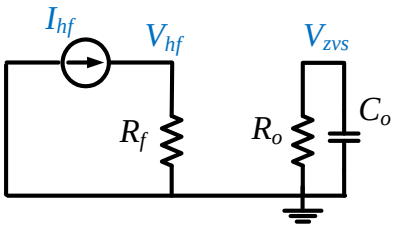
According to (5-6), larger R_o provides larger $\langle V_{ZVS}\rangle_{Ts}$ which will help obtain higher sensing resolution and higher immunity to noise. Meanwhile, according to (5-5), large R_o and C_o will increase the transient time which delays the detection signal. In addition, R_o and C_o will also impact the ripple of V_{ZVS}. Consequently, there is a tradeoff between these aspects for the selection of R_o and C_o.

The maximum allowed dV_A/dt, which indicates the boundary of ZVS and the hard switching operation, is defined based on the converter design. Then the upper limit of I_{hf} (I_{hf_max})and lower limit of d ($d_{\_min}$) are derived from the maximum dV_A/dt. V_{th} is obtained by taking $I_{hf}=I_{hf\_max}$ and $d=d_{\_min}$ into equation (5-6), $V_{th} = \langle V_{ZVS}\rangle_{Ts}$. The detection delay time is determined by τ in equation (5-5).



(a) The equivalent circuit





(b) Equivalent circuit when D_f conducts (c) Equivalent circuit when D_f is off

Fig. 5.12. Simplified ZVS detection circuit.

5.3.3 Discussion of several applications

This ZVS detection method is also applicable in the full bridge inverter as shown inFig. 5.13. The same detection circuit is used for phase leg A and B. V_{ZVS} presents the maximum of the voltage slope of both phase legs. If V_{ZVS} exceeds V_{th}, there are three different possibilities: (1) Only phase leg A loses ZVS; (2) Only phase leg B loses ZVS; (3) Both of them lose ZVS. Turning off all the switches is a simple solution for protection. Alternatively, extending the dead time of one phase leg only can help determine the hard switched phase leg.

The half-wave rectifier detects the rising edge of V_A, and therefore only offers ZVS detection for the upper switches. A full bridge rectifier can be utilized instead of the half-wave rectifier to convert both positive and negative V_{hf} to a dc voltage. Therefore, the rising edge and falling edge of V_A are both sensed, as shown in Fig. 5.14. Consequently, ZVS

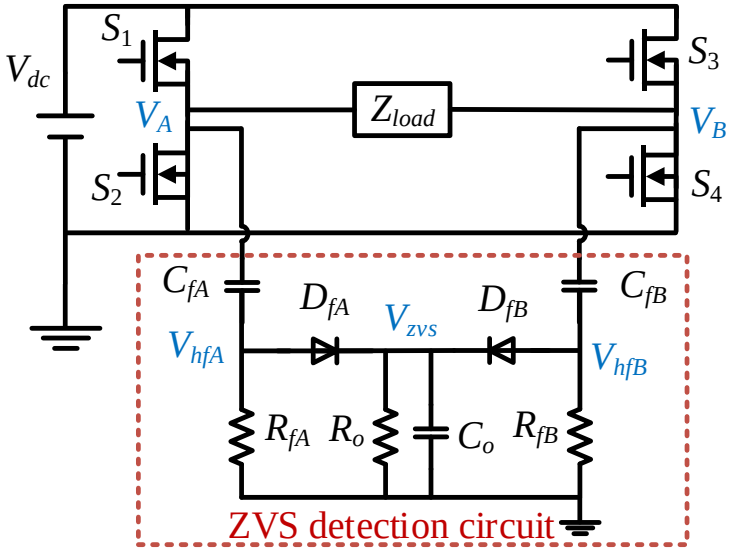


Fig. 5.13. ZVS detection in a full bridge configuration.

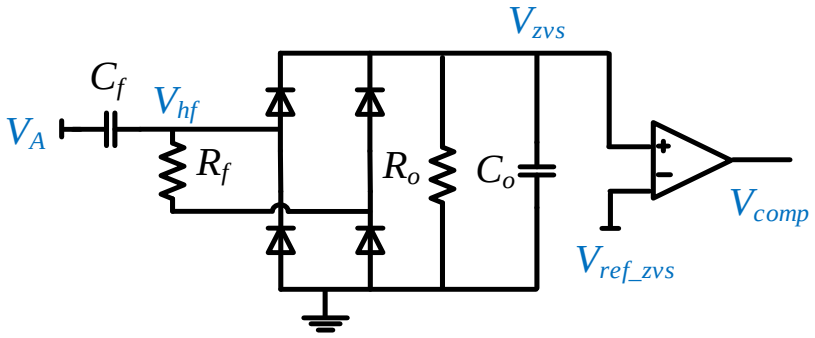


Fig. 5.14. ZVS detection for both upper and bottom devices.

of the upper switch and the bottom switch are detected. The analysis of this circuit is similar to the method for the half-wave rectifier.

If the converter operates symmetrically, only sensing one edge of each phase leg is enough for ZVS detection. The symmetric operation is defined in one phase leg. Before one switch turns on, the resonant current is the same or near the same, in terms of magnitude and direction, as the other one before turning on. For example, the typical resonant converter has a symmetric operation. For this single-stage transmitter, it is approximated to the symmetric operation because ZVS tank current dominates the resonant current before devices turning on. And ZVS tank provides symmetric peak current for devices. Therefore, a simple half-wave rectifier detection circuit is implemented in this work.

5.4 Experimental verification

In order to verify proposed closed-loop control for constant Ip in Section 5.1, the full power operation in Section 5.2, and ZVS detection in Section 5.3, the experimental results are shown in following Section 5.4.1, Section 5.4.2 and Section 5.4.3 respectively.

5.4.1 Single transmitter with multiple receivers in heavy load mode

A. Basic operation with two receivers

To verify the capability of the single-stage transmitter to supply multiple receivers, the prototype is tested with two receivers, as shown in Fig. 5.15. The output current of the transmitter, I_P, drives the transmitter coil L_p. The first receiver (Rx_1) is comprised of a receiving coil L_{s1}, a resonant capacitor C_{s1} and a diode rectifier which converts 6.78 MHz

AC to DC V_{rec} which supplies a resistive load R_1. The second receiver (Rx_2) directly provides 6.78 MHz ac voltage to a resistive load, R_2.

Fig. 5.16 shows the hardware setup of single-transmitter supplying two receivers. The transmitter coil L_p is a 22 cm × 22 cm rectangular coil. The coil of Rx_1, L_{s1} is 11 cm×11 cm. The coil of Rx_2, L_{s2}, is a self-resonant coil with 10 cm outer diameter [39]. L_{s1} and L_{s2} are coupled with L_p. Rx_1 and Rx_2 are placed on top of L_p with negligible distance in the vertical direction. Since the size of L_{s1} and L_{s2} are smaller than L_p, the coupling coefficients are small, k_1=0.08 and k_2=0.06. Rx_1 and Rx_2 are placed side-by-side with negligible cross-coupling.

Fig. 5.17(a) and Fig. 5.17(b) show the measured waveforms with two receivers under different load conditions. The load conditions are detailed in Table 5.1. I_{inv} reduces when the load decreases, but I_p maintains constant as expected. Due to the constant I_p, the output voltage of receivers V_{rec} and V_{R2} keep constant at different load conditions. These results verify the capability of charging multiple receivers with a single-stage transmitter.

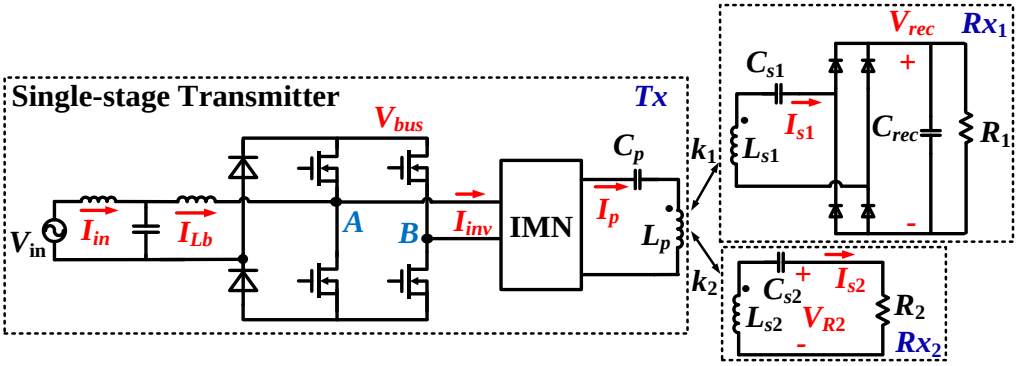


Fig. 5.15. Schematic of two-receiver WPT system.

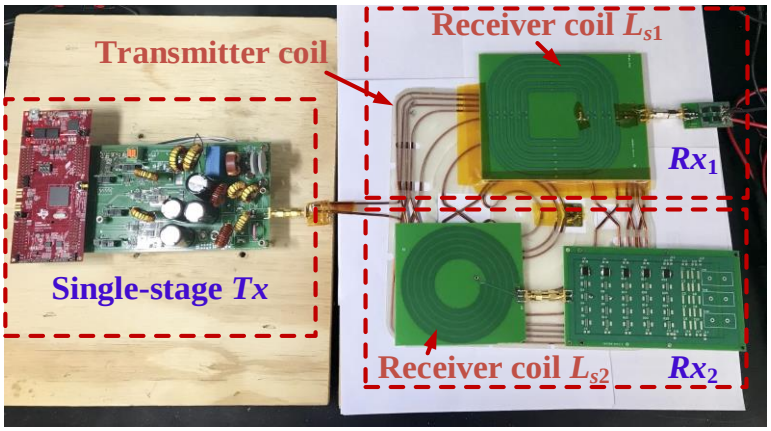
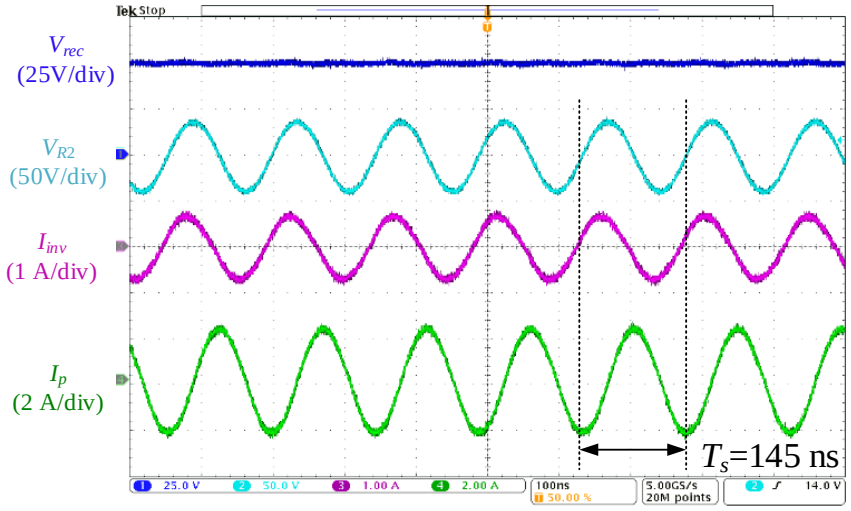
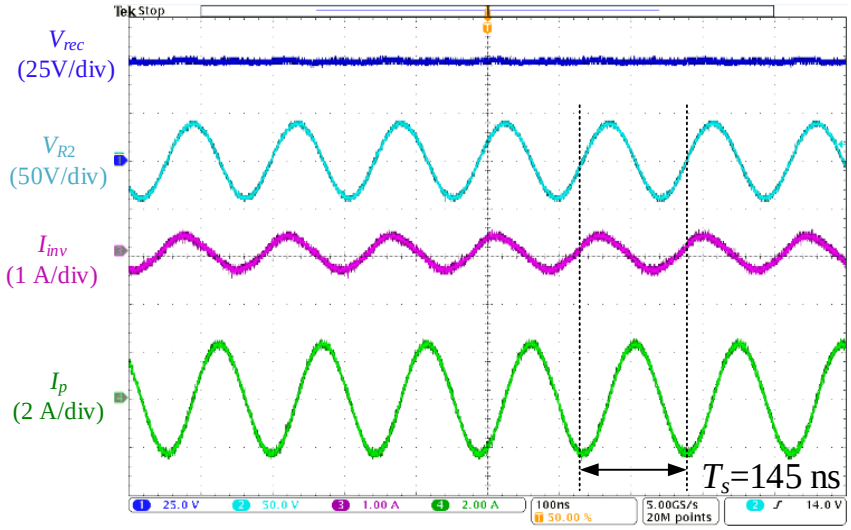


Fig. 5.16. Hardware setup.



(a) Case A at P_o=89 W



(b) Case B at P_o=59 W

Fig. 5.17. Measurement waveform with two receivers.

TABLE 5.1 LOAD CONDITION AND TEST RESULTS FOR TWO-RECEIVER SYSTEM

Case	I_p (A)	R_1(Ω)	V_{rec}(V)	P_{RX1}(W)	R_2(Ω)	V_{R2}(V	P_{RX2}(W	P_o(W)
A	1.6	100	52	27	15	30.5	62	89
B	1.64	200	52	13	20	30.2	46	59

B. Load step change with two receivers

This test is designed to verify dynamic operation during a load step change through the control scheme presented in Section 5.1. The same hardware setup as shown in Fig. 5.16 is used. R_1 is implemented with an electronic load and R_2 is a fixed load resistor. The input parameters and experimental results are shown in Table 5.2. Steady-state A and B are two different load conditions. The change of output power is achieved by adjusting the electronic load R_1. R_1 is 35 Ω (P_{Rx1}=35 W) at steady state A, and changed to 87 Ω (P_{Rx1}=14 W) for state B. P_{Rx2} is 50 W at steady-state A and maintains P_{Rx2}=50 W at state B.

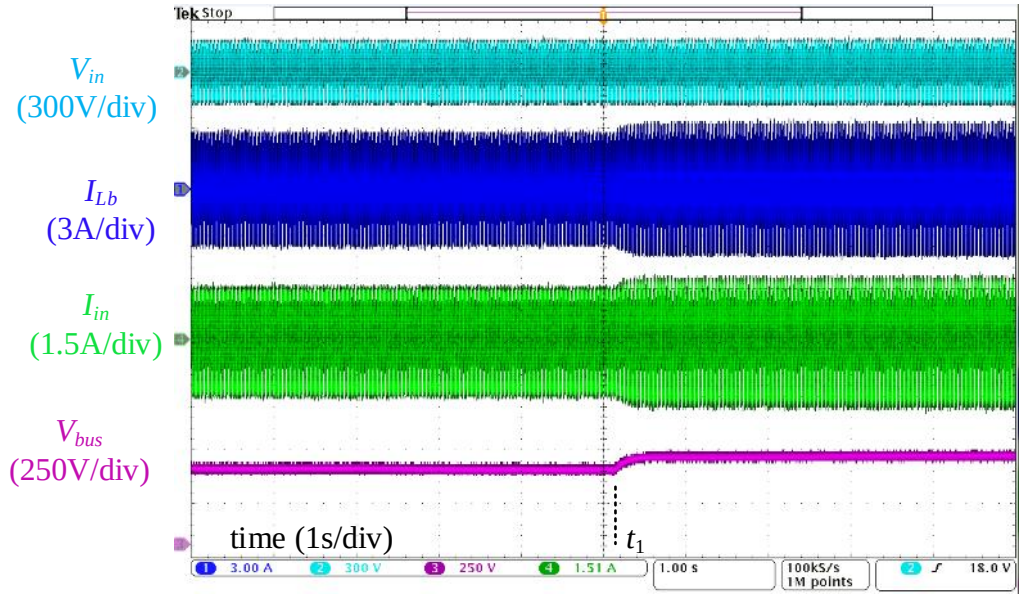
As seen in Table 5.2, the bus voltage follows the reference voltage V_{th}. There are a few volts of discrepancy between the measured bus voltage and the reference voltage. This 1.4% error might come from the accuracy of the sensing circuit of V_{bus} and the controller design. The output current of transmitter I_p remains constant during the load step change. In addition, the output voltage of the diode rectifier V_{rec} maintains constant since the coupling coefficient between the transmitter and receiver coil does not change during the test.

Fig. 5.18 and Fig. 5.19 show the transition during the load step-down change in open loop and closed-loop, respectively. In Fig. 5.18, V_{bus}, V_{rec} and I_p increase significantly after changing the load.

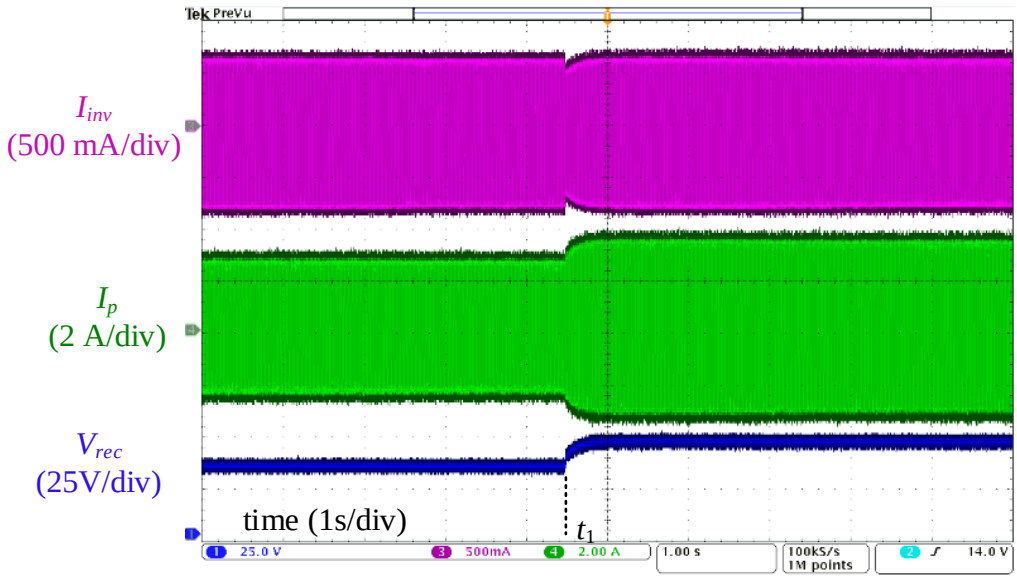
In contrast with the open loop performance, V_{bus} , $V_{rec,}$ and I_p with closed-loop control remain nearly constant before and after load step change, as shown in Fig. 5.19. The zoomed in waveforms show that I_{in} is in phase with V_{in} and exhibits a sinusoidal waveform. V_{rec} is smooth. I_{inv} contains some harmonic components, and I_p achieves sinusoidal waveform with negligible harmonics because of the IMN.

TABLE 5.2 MEASUREMENT RESULTS OF CLOSED-LOOP CONTROL

State	V_{in}/V	V_{ref}/V	V_{bus}/V	I_p/A	V_{rec}/V	P_o/W
A	120	340	335	1.45	35	85
B	120	340	337	1.5	35.6	64

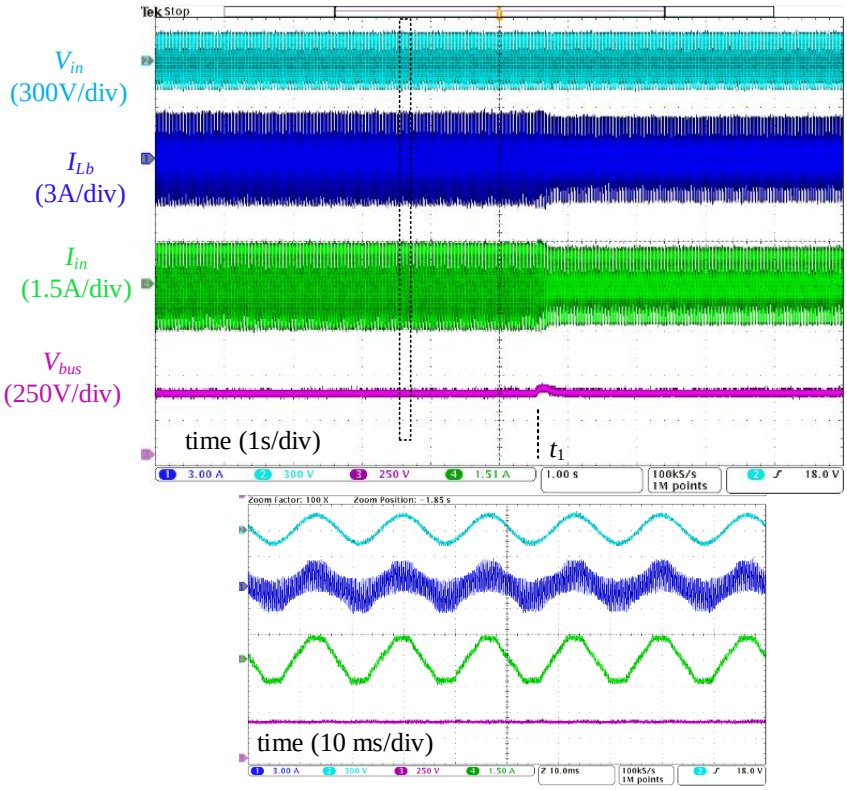


(a) Rectifier waveform

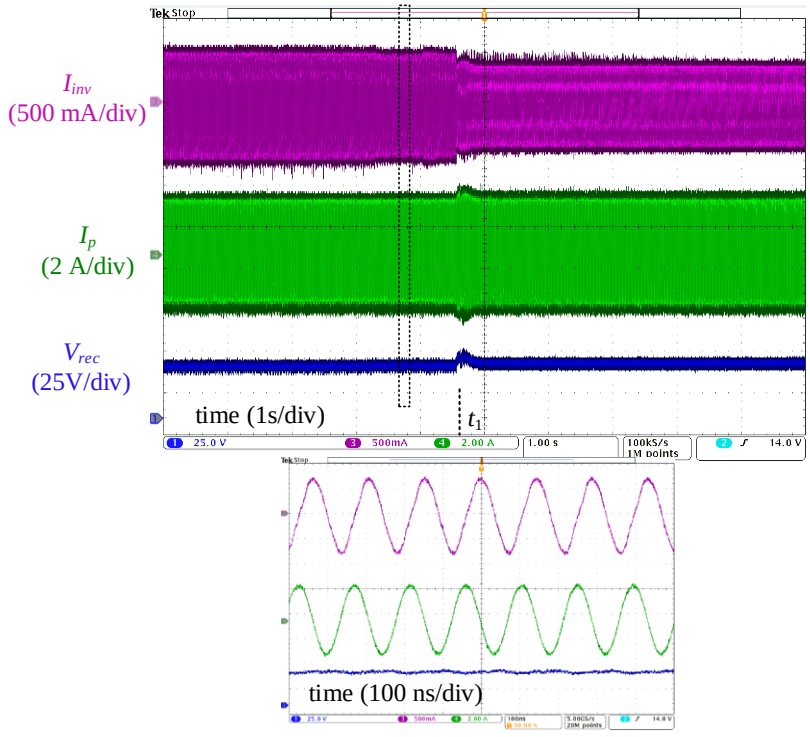


(b) Inverter waveform

Fig. 5.18. Experimental results of load-step change with open loop control.



(a)



(b)

Fig. 5.19. Experimental results of load-step change with the closed-loop controller.

C. Dynamic operation with three receivers

This test is designed to verify the system performance when there is receiver added or removed from the system during operation.

Fig. 5.20 shows the schematic of the transmitter supplying three receivers. All receivers are full bridge diode rectifiers. Fig. 5.21 shows the hardware setup of this configuration. The transmitter coil, receiver coil 1 and receiver coil 2 are the same coils used in Section B. Another receiver, coil 3 is added to the system. Coil 3 is a self-resonant coil with 7 cm outer diameter. Since these three receivers are placed side-by-side with large distance, the cross-coupling effect is negligible.

Fig. 5.22 shows the performance when the additional receiver drops into the charging area is removed from the system in open loop. Initially, from t_1 to t_2, RX_1 and RX_2 are placed on the charging field. At t_2, RX_2 is removed. So, V_{rec2} drops to zero as expected. Meanwhile, I_p increases, therefore V_{rec1} increases. When the load becomes light, V_{bus} increases without feedback control. In addition, V_{ab} is not regulated to maintain constant. Thus, V_{rec1} increases after RX_2 is removed during t_2 to t_3. At t_3, RX_3 is inserted into the system. As shown in the plot, V_{rec3} increases. Since the load becomes heavier, the bus voltage decreases, and the decreased V_{bus} causes a voltage drop on V_{rec1}. At t_4, RX_2 is placed on the edge of the charging system. V_{rec2} becomes smaller than the value at the beginning because of the smaller coupling coefficient on the edge. At the same time, both V_{rec1} and V_{rec3} decrease during the period from t_4 to t_5 due to the reduced V_{bus}. At t_5, when removing RX_3, V_{rec1} and V_{rec2} increase.

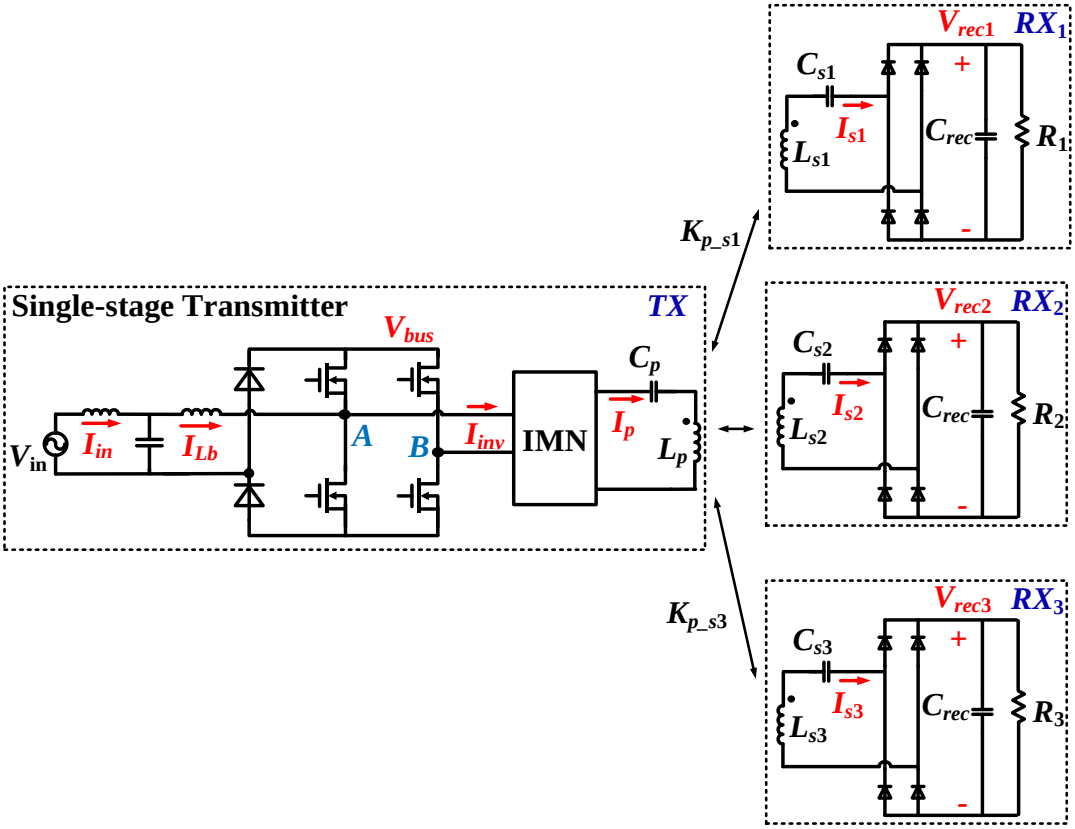


Fig. 5.20. Schematic of WPT system with three receivers.

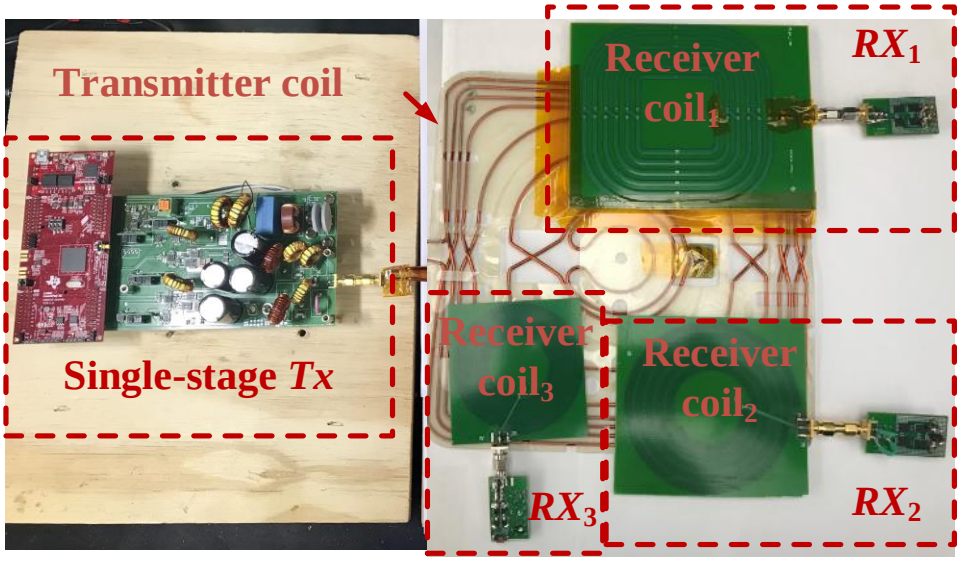


Fig. 5.21. Hardware setup of WPT system with three receivers.

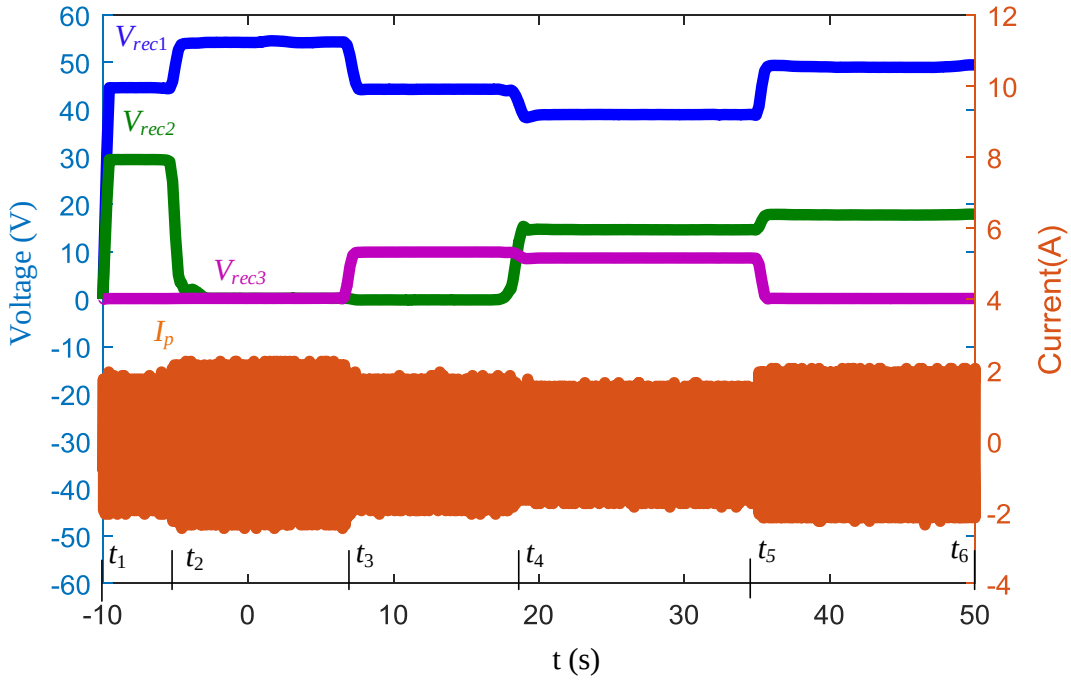


Fig. 5.22. Measurement results with open loop control.

Fig. 5.23 gives the test result with closed-loop control following the similar test procedure as discussed above. According to the results, when adding new receivers into the system or removing them from the system, the output voltage of other receivers remains constant without any additional control effort at the receiver side. Fig. 5.24 shows the power delivered to each receiver. As seen, the power of each individual receiver maintains constant during the whole period of adding and removing the load. This behavior verifies the operation of other receivers is not impacted during dynamic load change.

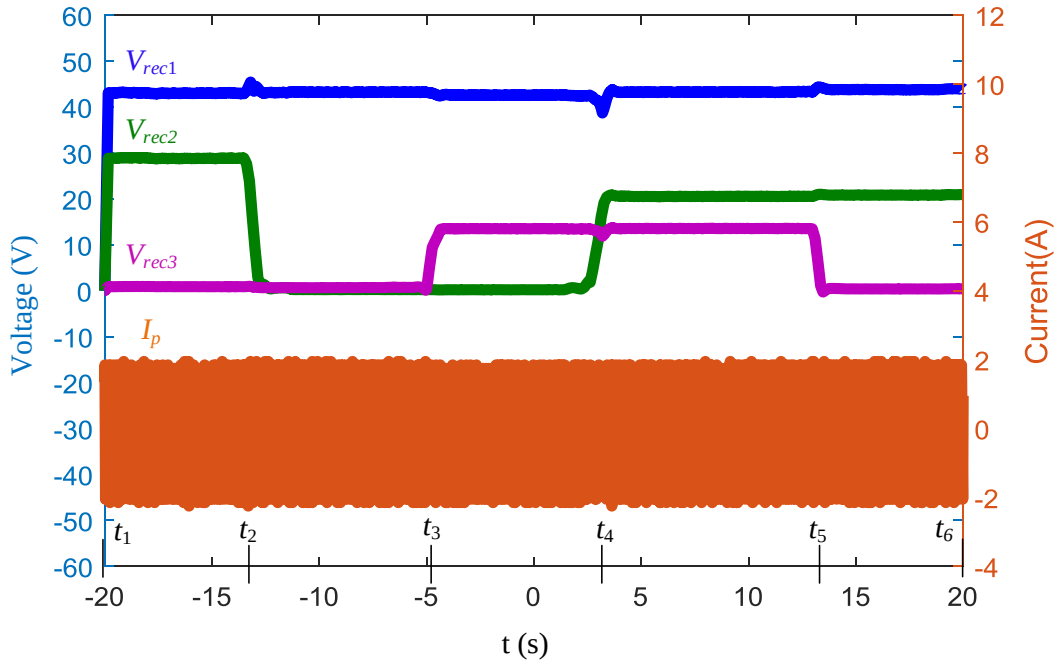


Fig. 5.23. Measurement results with closed-loop control.

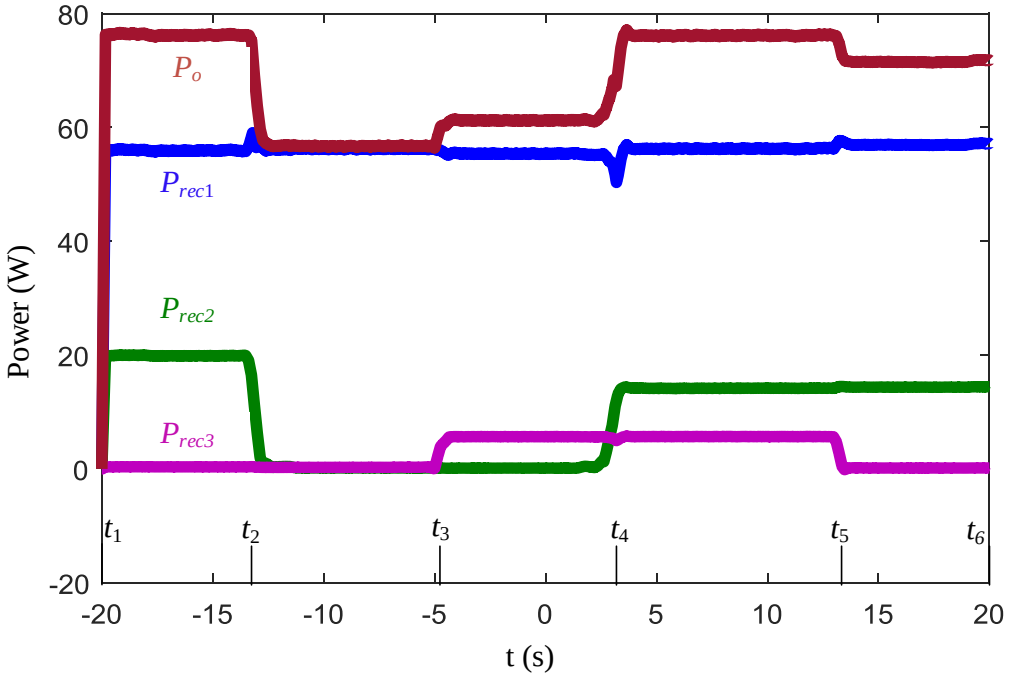


Fig. 5.24. Power change on the three receivers with closed-loop control.

5.4.2 Dynamic operation over a wide power range

The dynamic operation of the transmitter at a wide power range is verified using the test setup shown in Fig. 5.16. The power of RX_1 is changed via adjusting the electronic load R_1. The load of RX_2 maintains constant.

As discussed in Section 5.2.1, there are three cases occur that when processing mode switching. Two of them (between Light_A and Heavy_A, or Light_A and Heavy_C) result in I_p varying between two operation modes. They are named Case 1 in this section. Another situation (between Light_A and Heavy_B) is titled Case 2. Case 2 has the same I_p in two modes. Both of Case 1 and Case 2 are verified experimentally.

Heavy load mode and light load mode are named as HLM and LLM respectively in the experimental waveforms and tables for simplification.

A. Case 1

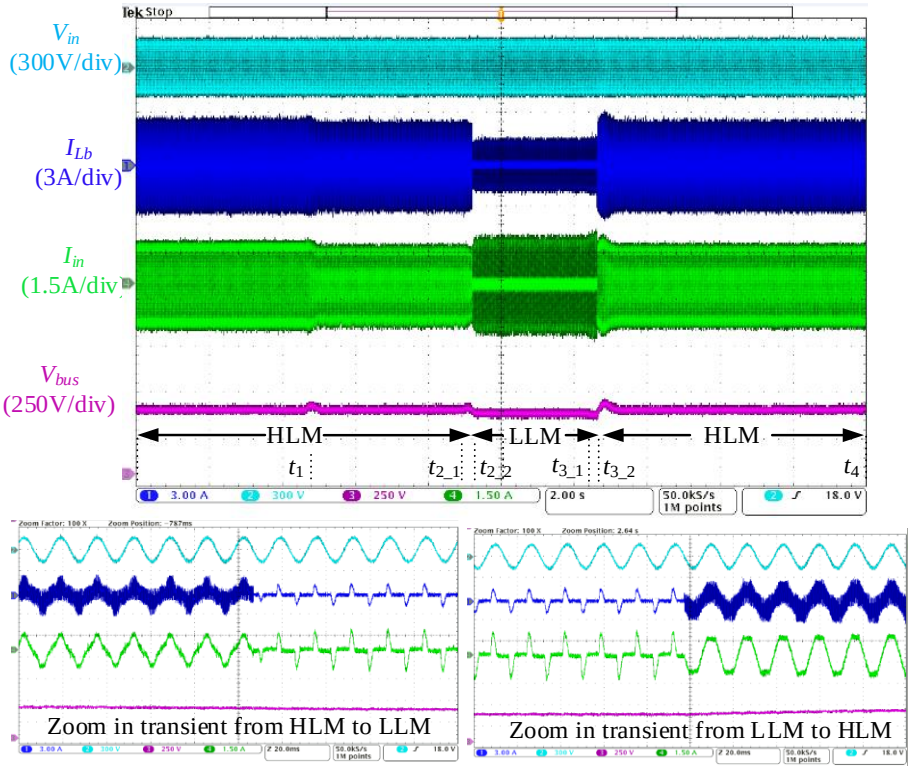
The measured waveforms are shown in Fig. 5.25. Finally, the transmitter works in heavy load mode and supplies 80 W output power. At t_1, the load drops to 62 W. A transient is observed due to voltage loop regulation. Output power maintains at 62 W during t_1 to t_{2_1}. At t_{2_1}, the load is set to 23 W. The PI controller brings d_a lower than $d_{a,min}$. At t_{1_1}, both $d_a < d_{a,min}$ and $t_{counter} < t_{delay}$ are satisfied. So, transmitter switches to light load mode by turning off phase leg A and turning on M_{a1} and M_{a2}. During t_{2_2} to t_{3_1}, the transmitter provides 23 W in light load mode operation. At t_{3_1}, the load increases to 60 W. V_{bus} drops to 310 V with the increased load due to VDR operation. V_{bus} is detected lower than V_{bus,min_light}=315 V at t_{3_2}. According to the control flowchart in Fig. 5.10, the transmitter returns to heavy load mode. The procedure of this test is summarized in Table 5.3.

TABLE 5.3 LOAD SWITCHING TEST

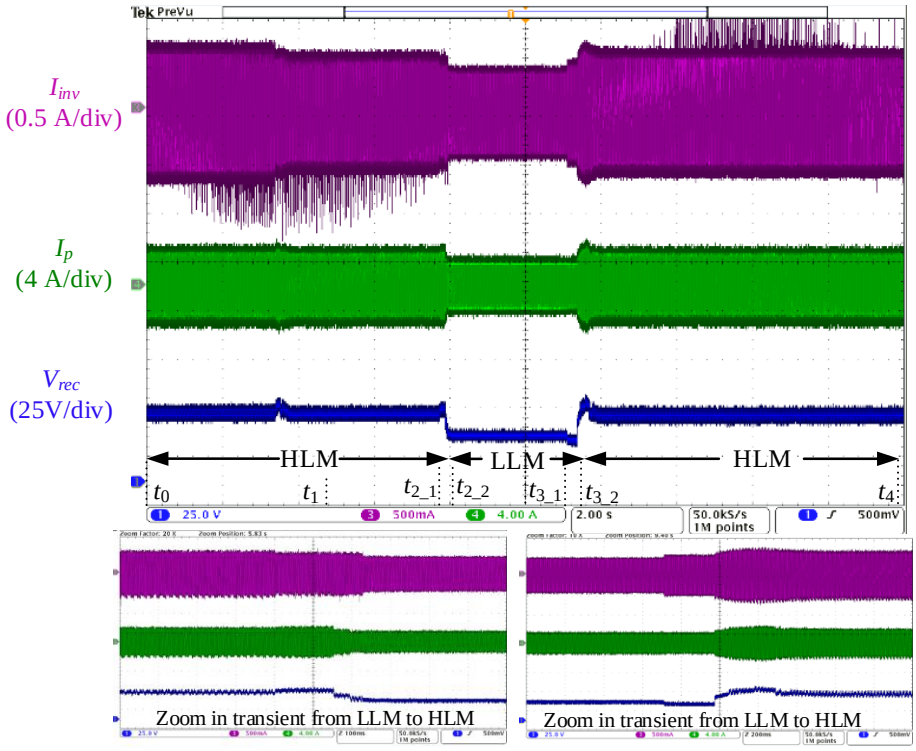
Time	Action	Operation mode	Power Level
t_0	initial state	HLM	76 W
$t_{0\sim}\ t_1$	steady-state	HLM	76 W
t_1	load change	HLM	62 W
$t_{1\sim}\ t_{2\_1}$	steady-state	HLM	62 W
t_{2_1}	load change	HLM	23 W
t_{2_2}	transient	HLM to LLM	-
$t_{2\_1\sim}\ t_{3\_1}$	steady-state	LLM	23 W
t_{3_1}	load change	LLM	60 W
t_{3_2}	transient	LLM to HLM	-
$t_{3\_2\sim}\ t_4$	steady-state	HLM	60 W

The receivers implemented in this experiment don't have power regulation capability. So, when the transmitter switches from heavy load mode to light load mode, the output power changes unexpectedly. For example, when the receiver load is set to 55 Ω, with V_{rec}=35 V and P_{rec}=23 W. But when I_p drops in light load mode, with 55 Ω load, V_{rec} =25 V and the receiver only picks up 12 W. As discussed in 5.2.1, if dc-dc converter is placed at the output of diode rectifier, the output power is able to be controlled at the desired value. This research work mainly focuses on the transmitter design, so, efforts are not made on the receiver design and optimization. Since this test is designed to verify the full power operation of the transmitter, when changing the load at t_{2_1}, 27 Ω instead of 55 Ω is used. After the transmitter enters into light load mode, the desired 23 W power at the output is obtained. The same consideration is applied in the transient from light load mode to heavy load mode.

The experimental waveform is shown in Fig. 5.25. Experimental results of mode switching verify the wide power operation of the transmitter in Case 1. During the load step change in their current operation mode, V_{bus} keeps constant, I_p maintains constant and receiver obtains the required power. When operation mode changes, I_p changes smoothly. This change results in a variation of power due to the lack of active receiver control.



(a) Rectifier waveforms



(b) Inverter waveforms

Fig. 5.25. Experimental results of mode switching in Case 1.

B. Case 2

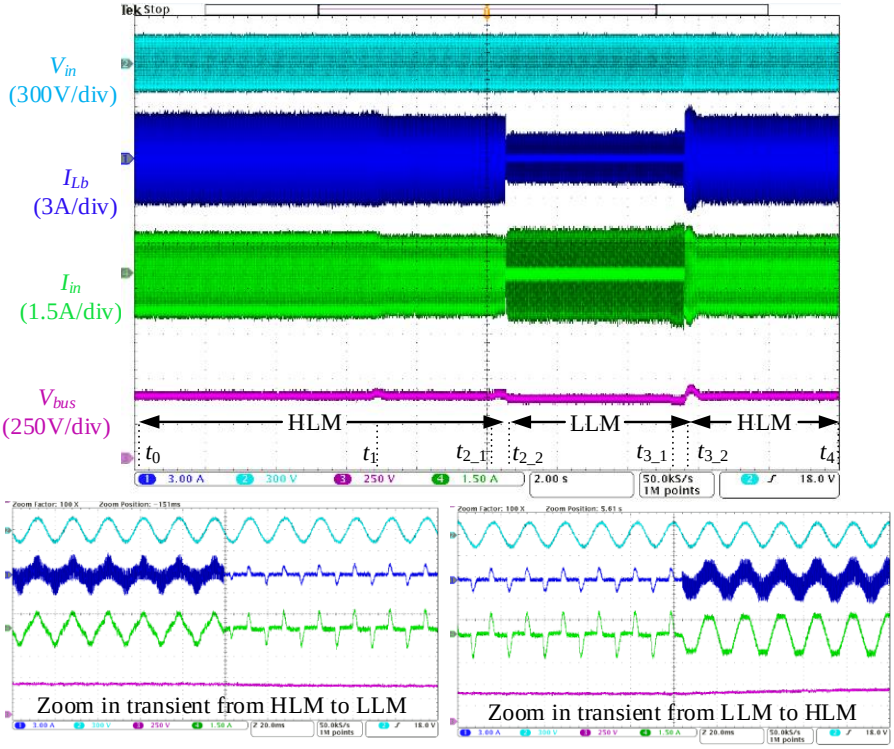
To verify the operation in Case 2, the same test as Case 1 is run, but using an I_p in heavy load mode that is close to I_p in the light load mode I_{p_hb}. So, during the transient, current I_p barely drops as shown in Fig. 5.26. Therefore, V_{rec} keeps nearly constant between these two modes.

5.4.3 ZVS detection

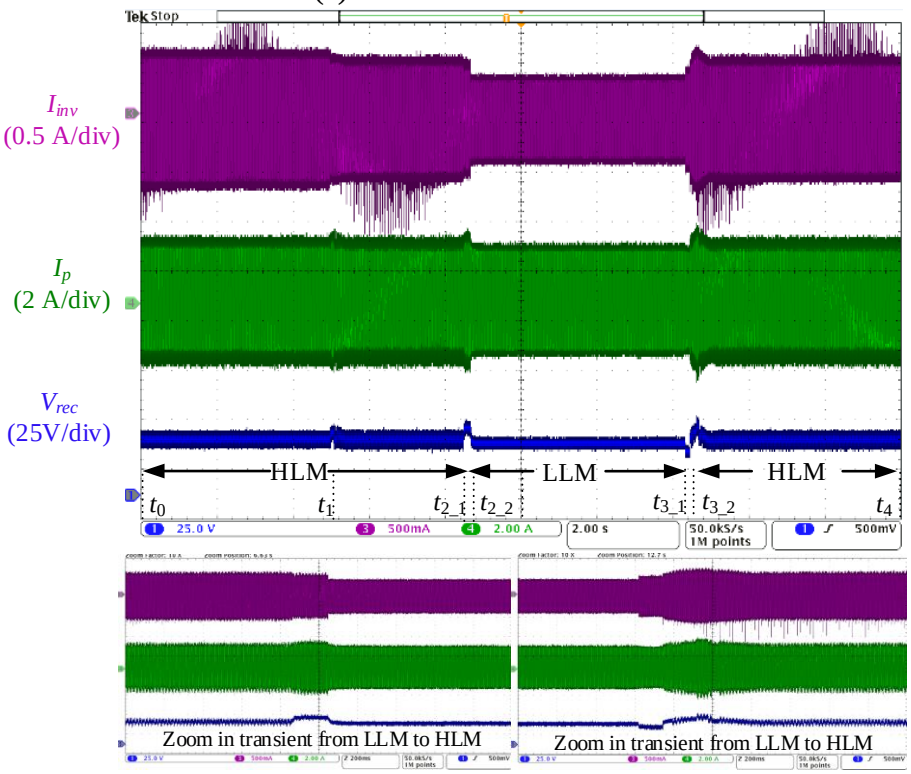
Fig. 5.27 shows the experimental waveforms of ZVS detection. Fig. 5.27(a) and Fig. 5.27(b) verify the simple solution when a loss of ZVS is detected. At t_1, hard switching occurs on both of the two phase legs, so V_{ZVS} increases. At t_2, V_{ZVS} reaches V_{th}, and the output of the comparator becomes high. After sensing the high-level signal, the DSP turns off all the switches to prevent continuous hard switching. There are two delay times shown in this measurement waveform. The delay from t_1 to t_2 is expected and occurs due to charging C_o which is discussed in Section 5.3.1. It can be adjusted by changing R_f, R_o and C_o according to equation (2) with the consideration of the aforementioned tradeoffs. The delay from t_2 to t_3 is caused by the processing time of detection in DSP.

Fig. 5.27(c) and Fig. 5.27(d) show the second solution. When hard switching is detected at t_1, the first attempt is to extend the dead time. If ZVS can be regained by a larger dead time, converter operation is maintained. If not, then all the gate signals of the switches are turned off as in the first solution.

The total loss of this detection circuit is 11 mW which is obtained based on simulation and the parameters from the datasheet.



(a) Rectifier waveforms

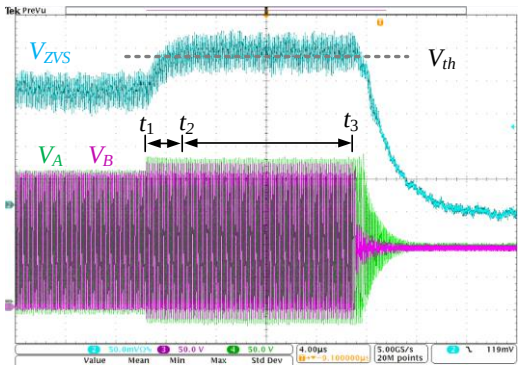


(b) Inverter waveforms

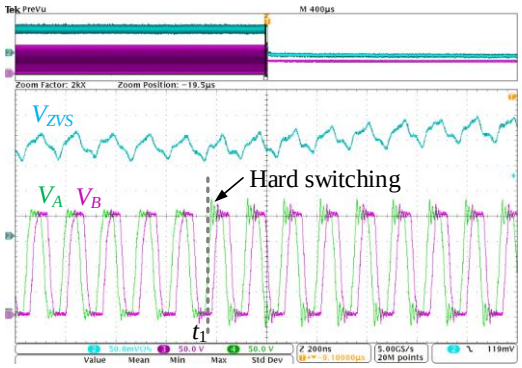
Fig. 5.26. Experimental results of mode switching in Case 2.

TABLE 5.4 DESIGN PARAMETER OF ZVS DETECTION

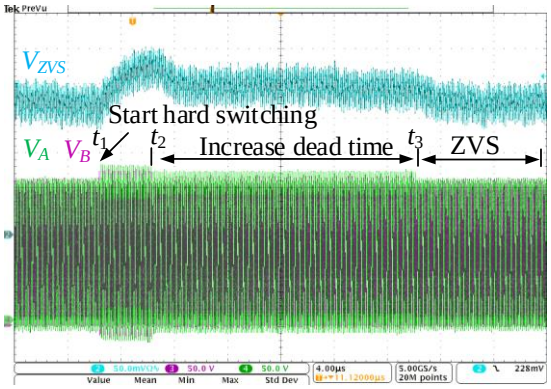
Symbol	Value
V_{bus}	200 V
f_s	6.78 MHz
S_1~S_4	GaN FETs
D_{fA}/D_{fB}	ZHCS400
C_{fA}/C_{fB}	4 pF
R_{fA}/R_{fB}	20 Ω
R_o	200 Ω
C_o	20 nF



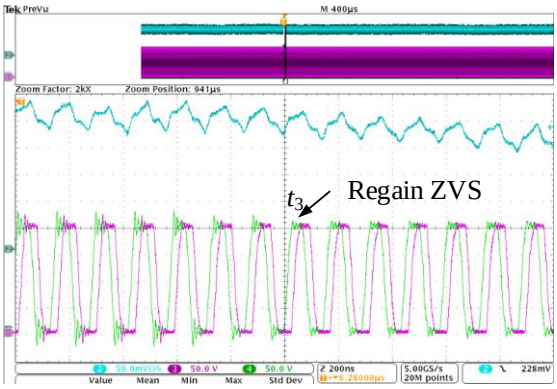
(a) ZVS detection and protection



(b) Zoom in waveform of (a)



(c) Deadtime extension



(d) Zoom in waveform of (c)

Fig. 5.27. Measurement waveforms.

5.5 Summary

This chapter proposes a closed-loop control scheme to achieve current source behavior at the output of the single-stage transmitter, which is the transmitter coil current. This current source behavior enables smooth transient when simultaneously charging multiple receivers with a single transmitter. By controlling the duty cycle and phase shift, and designing a proper IMN, the transmitter coil current is regulated. Based on the provided I_p, the receivers individually receive their required power without disturbing the adjacent loads. The experimental and simulation results agree with the analysis. A constant current is achieved at the output of the transmitter. A well-regulated transition is demonstrated with load step change and load dynamic change in the heavy load mode to verify the functionality and feasibility.

The full load range operation is achieved by the cooperation of heavy load mode and light load mode. Two different cases are discussed. The first case is when the I_p is different in the two modes, and the second case is that two operation modes have the same value of I_p. Both instances are verified in the experiments.

A ZVS detection method effectively detects non-ZVS operation with minimal circuitry, simple control and low loss. This method is applicable for half-bridge and full bridge configurations.

6 WPT SYSTEM OPERATION WITH SINGLE-STAGE TRANSMITTER

Chapter 5 has introduced the operation of the single-stage transmitter under dynamic load changes. In this chapter, the operation and control scheme of the WPT system with the implementation of the single-stage transmitter is discussed.

There is always a limited operating range for the WPT system. A system control scheme is required to help the transmitter and receivers work within this range. Within the operating range of all devices, system efficiency optimization can be used to determine the operating point.

Constant transmitter current helps smooth the transient when the load changes. It is essential for the multiple receiver application where load changes dynamically. However, during the steady state, variable I_p helps provide a large operating range and optimize the system efficiency.

6.1 WPT system configuration

Fig. 6.1 gives a typical WPT system structure. It is comprised of a transmitter unit and receiver unit. The power is delivered from the transmitter to receive through the resonant coupling. The communication between these two units is achieved via 2.4 GHz Bluetooth.

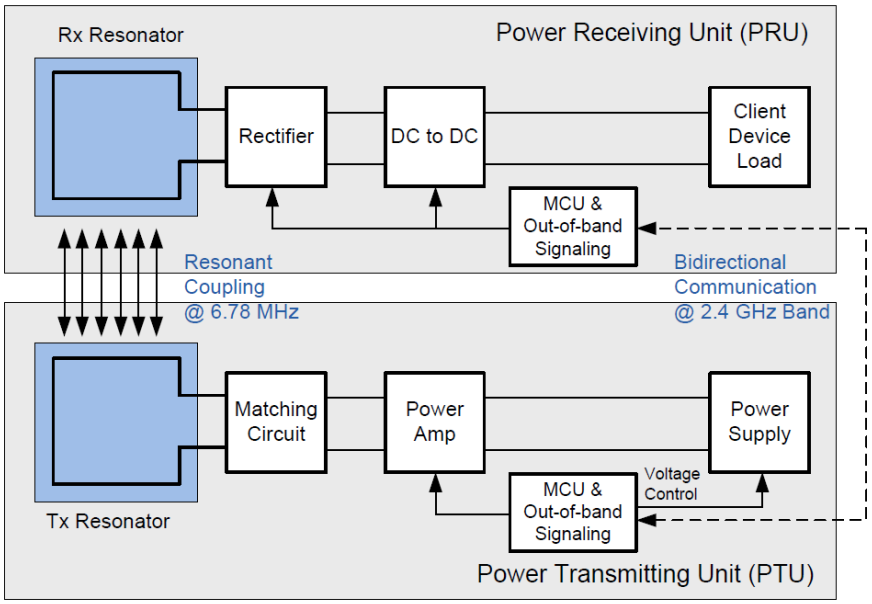


Fig. 6.1. A4WP WPT system baseline system configuration [14].

6.1.1 Transmitter configuration

The structure of the transmitter unit, shown in Fig. 6.1, includes a power supply (rectifier), inverter and an IMN. As discussed previously, this structure is a two-stage transmitter, or multiple stage transmitter depending on the topology of the power supply. In this research work, a single-stage transmitter is introduced to replace the conventional structure for high efficiency and reduced part count. Meanwhile, it is also designed to support system operation with multiple receivers.

Since the details of the transmitter operation have been discussed in the previous chapters, this section focuses on the investigation of the reactive load range for the single-stage transmitter.

The analysis in Chapter 4 assumes the load of transmitter Z_{Pa} is a purely resistive load. However, when considering the practical system operation, Z_{Pa} is determined by the

receivers and the coupling between the transmitter coil and receiver coil. Thus, Z_{Pa} might have a wide reactive range. Large reactive load impacts the transmitter operation. Z_{Pa} is comprised of a real part and imaginary part in Fig. 6.2(a).

$$Z_{Pa} = R_{Pa} + jX_{Pa} \tag{6-1}$$

Then, the output impedance of inverter Z_{inv} is

$$Z_{inv} = R_{inv} + jX_{inv} \tag{6-2}$$

$$R_{inv} = \frac{L_f \cdot R_{Pa}}{C_f \cdot (R_{Pa}^2 + X_{Pa}^2)} \tag{6-3}$$

$$X_{inv} = \frac{-L_f \cdot X_{Pa}}{C_f \cdot (R_{Pa}^2 + X_{Pa}^2)} \tag{6-4}$$

The equivalent circuit after reflecting Z_{Pa} to Z_{inv} is shown in Fig. 6.2(b).According to (6-4), if Z_{Pa} is inductive, Z_{inv} becomes capacitive and vice versa.

Three factors determine the boundary of the reactive load range: (1) ZVS operation condition; (2) Conduction loss from circulating current; and (3) High voltage stress from the reactive load.

Large inductive Z_{Pa} results in a capacitive load on Z_{inv} which eventually causes hard switching. So, the range of inductive load is determined by ZVS operating range. The switching node voltage V_{AB}, ZVS tank current and inverter output current I_{inv} are plotted in Fig. 6.3. The leading phase leg (phase leg A) will lose ZVS first, so, the impact of the load current on this phase leg is used to determine one of the boundaries. At heavy load, there is 0.5 A buffer from ZVS tank design. So, the allowed maximum capacitive inverter current $I_{inv\_capacitive}(t=0)$=0.5 A. As long as this condition is satisfied, soft switching is maintained. Fig. 6.4(a) shows the load range for ZVS operation.

Capacitive Z_{Pa} helps maintain ZVS by providing circulating current of the correct polarity. However, large circulating current increases the loss in the devices and the output filter. Fig. 6.4(b) shows the reactive load boundary for the converter maintaining higher than 80% efficiency at the full power level.

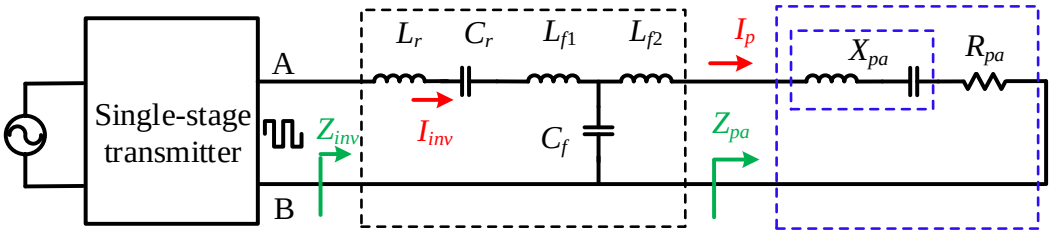
Increased circulating current also increases the voltage stress on the capacitors in IMN. For the MLCC implemented in the IMN, over-voltage will cause failure. The voltage rating of the capacitors in the IMN is 500 V. With 80% voltage derating, the maximum allowed voltage on the capacitors is 400 V. The voltage cross C_r and C_f are

$$V_{Cr} = \frac{V_{ab}}{\sqrt{(R_{inv}^2 + X_{inv}^2)}} \cdot \frac{1}{j\omega C_r} \tag{6-5}$$

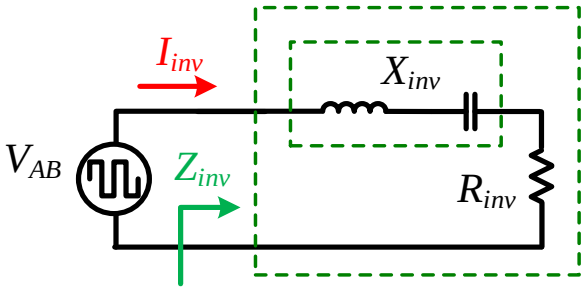
$$V_{Cf} = \frac{V_{ab}}{\sqrt{(R_{inv}^2 + X_{inv}^2)}} \cdot \frac{(R_{pa} + jX_{pa} + j\omega L_f) \cdot \frac{1}{j\omega C_f}}{R_{pa} + jX_{pa} + j\omega L_f + \frac{1}{j\omega C_f}} \tag{6-6}$$

Based on this voltage limitation, the load range is given in Fig. 6.4(c).

By considering the three factors above, the reactive load range is shown in Fig. 6.4(d).



(a)



(b)

Fig. 6.2. Output network of the inverter.

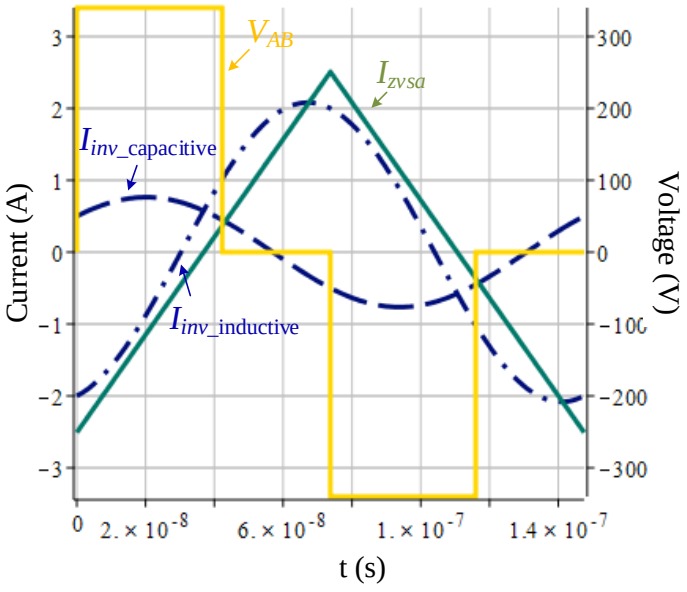
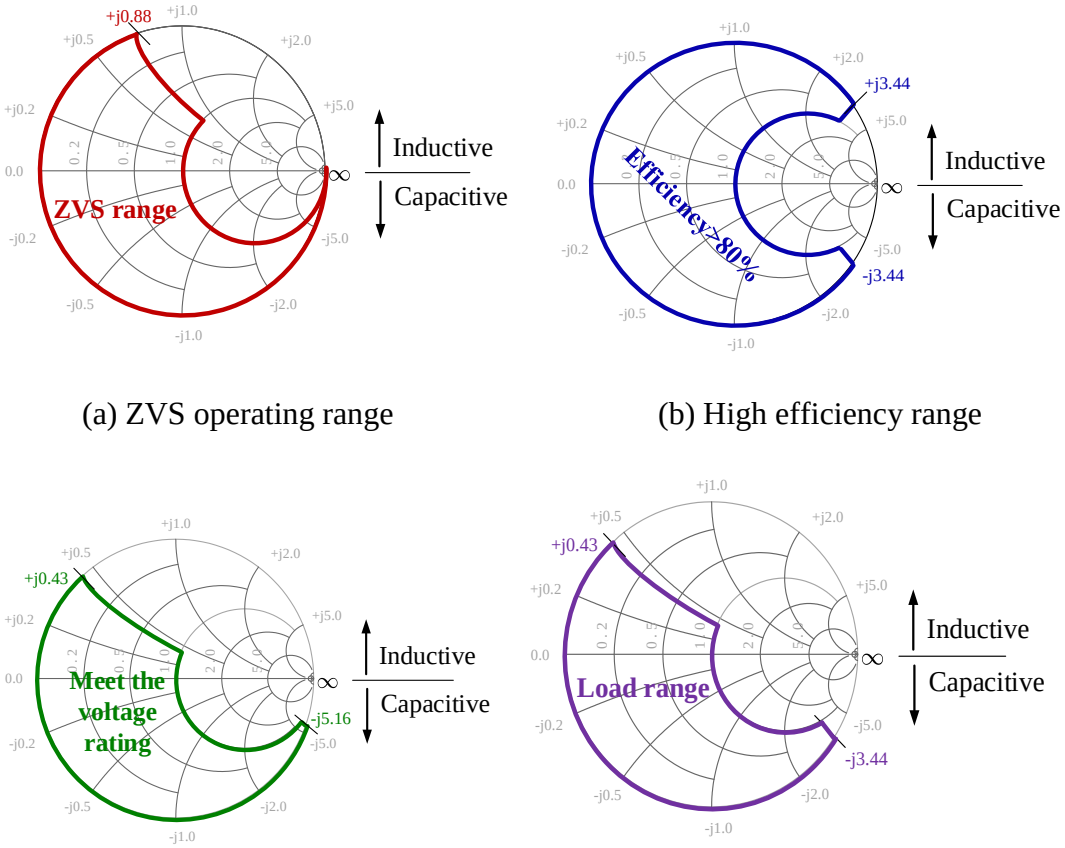


Fig. 6.3. The impact of reactive current on ZVS operation.



(a) ZVS operating range (b) High efficiency range

(c) Load range for limited voltage rating (d) Overall load range

Fig. 6.4. Reactive load range of the transmitter.

6.1.2 Receiver configuration

The configuration of a typical receiver is shown in Fig. 6.5. It is comprised of the resonator (L_s and C_s), a full-bridge diode rectifier, and a dc-dc converter. This resonator is used to filter out other harmonic content. The diode rectifier converts 6.78 MHz ac to a dc voltage. The following dc-dc converter is added for output voltage V_L regulation. Z_{rec} is the equivalent impedance of the receiver, R_{dc} is the input resistance of the dc-dc converter, and R_L is the actual load. In practice, R_L is often a battery. The induced voltage across the receiver coil is $V_{oc}=j\omega M \cdot I_p$. V_{oc} is determined by the mutual inductance M between the transmitter coil and the receiver coil, and I_p. The dc-dc converter implementation is selected according to the system configuration. If V_{rec} is always higher than the required V_L, a buck type converter is preferred. Considering a wide range of V_{rec} for the desired V_L, then the buck-boost type is regulated, Buck converter is used in [24], and buck-boost is utilized in [147]. With this dc-dc converter, the receiver has a control variable R_{dc}. Taking a buck converter as an example.

$$R_{dc} = \frac{R_L}{d^2} = \frac{V_L^2}{P_L \cdot d^2} \tag{6-7}$$

where d is the duty cycle of the buck converter, and P_L is the output power.

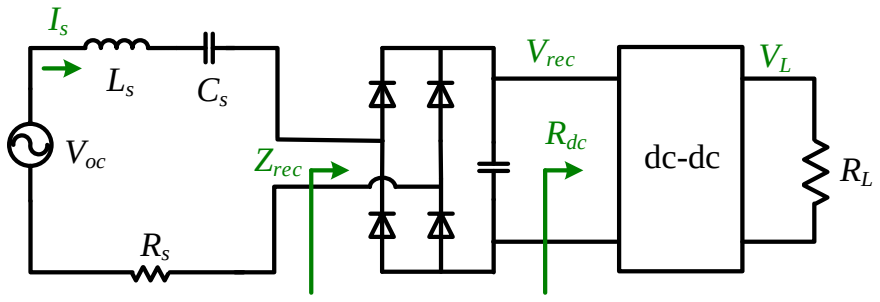


Fig. 6.5. Simplified receiver configuration.

The receiver has limited operating range. The induced voltage V_{oc} on the receiver coil is limited by the standard for a specific application, the voltage rating of devices and efficiency. V_{oc_max} is defined to address this limitation. Similar rules are applicable to the receiver coil current I_{s_max}. The receiver power P_L and I_{s_max} set a limit on the minimum induced voltage V_{oc_min}. When V_{oc} =V_{oc_min}, the desired P_o should be delivered while satisfying I_s <I_{s_max}. So, V_{oc_min} is derived in (6-8). I_{s_min} is obtained by considering P_L and V_{oc_max} in (6-9). V_{oc} is a 6.78 MHz sinusoidal voltage. Ideally, V_{rec} is equal to the peak value of V_{oc}. Since V_{rec} is a dc voltage, it is used to discuss the receiver operating range instead of V_{oc} for simplification in this work. Equation (6-10) and (6-11) address the receiver operating range with V_{rec}.

In addition, when implementing different types of the dc-dc converter at the output of diode rectifier, there is another limit on V_{rec}. Take a buck type converter as an example, V_{rec} should be at least larger than V_L, V_{rec}>V_L. So, the range of V_{rec} with a buck converter is updated in (6-12).

The operating range of the receiver in terms of output power P_L, I_s and V_{rec} is given in Fig. 6.6(a). Fig. 6.6(b) shows the case with a buck type dc-dc converter at the output of diode bridge rectifier.

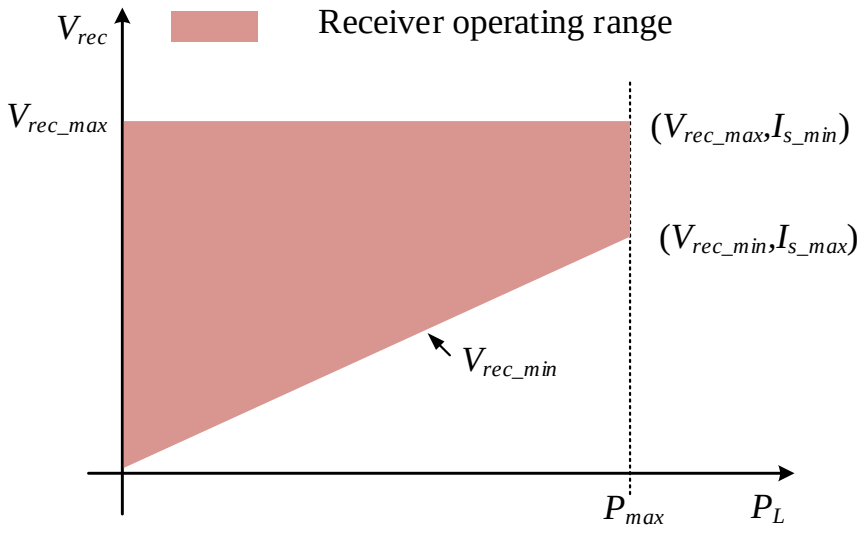
$$V_{oc\_min} = \frac{P_o}{I_{oc\_max}} \tag{6-8}$$

$$I_{s\_min} = \frac{P_o}{V_{oc\_max}} \tag{6-9}$$

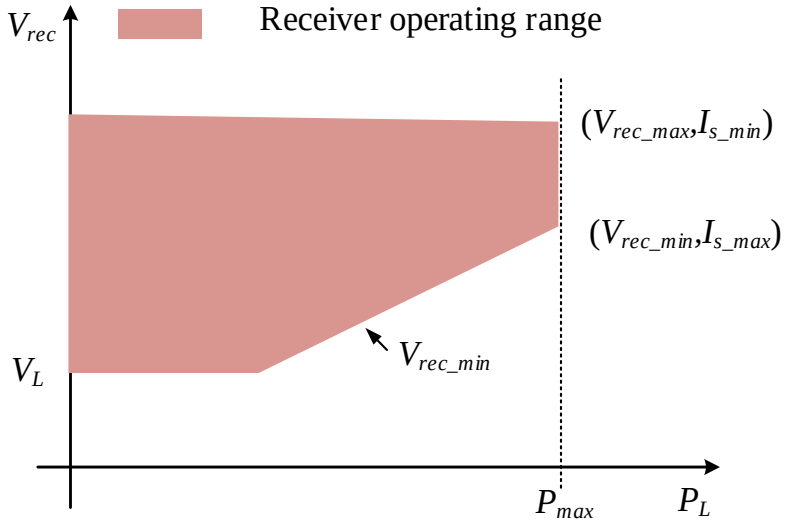
$$V_{rec\_min} = \sqrt{2}V_{oc\_min} = \frac{\sqrt{2}P_o}{I_{s\_max}} \tag{6-10}$$

$$I_{s\_min} = \frac{\sqrt{2}P_o}{V_{rec\_max}} \tag{6-11}$$

$$V_{rec\_\min\_buck} = min\left(\frac{P_L}{I_{s\_max}}, V_L\right) \tag{6-12}$$



(a) Basic operating range



(b) Operating range with a buck type dc-dc converter at the output of the diode rectifier

Fig. 6.6. Receiver operating range.

6.2 System operating range

The system operating range is determined by the transmitter operating range and receiver operating range. By combining the range of these two converters, the overlap area is the system operational range. Fig. 6.7 shows several different cases of system operating range. The X-axis is the power level, and Y-axis is the transmitter current I_p and the output voltage of diode rectifier voltage V_{rec}. Both of I_p and V_{rec} are given by the Y-axis in these plots because they have proportional relation for any given M.

Case 1 shows that transmitter is able to supply this receiver from no load to full load. The maximum V_{rec} in the heavy load mode and in the light load mode is limited by I_{p_max} and $I_{p\_hb\_max}$, respectively.

The receiver in Case 2 also obtains the required power at full range. But, the supplied I_p in the heavy load mode should be controlled to keep V_{rec} below V_{rec_max}.

To supply the full power range for the receiver in Case 3, the transmitter keeps its operation in the light load mode. The maximum transmitter coil current is limited by the half-bridge inverter.

In Case 4, the transmitter is not preferred to supply the receiver in a certain power range that is defined as $P_{invalid}$, because this range causes low efficiency on the transmitter.

There is an invalid power in the middle that cannot be supplied by the transmitter in Case 5. When the receiver requires power in this range, the transmitter has to ask it to reduce the required power or increase the power. If the receiver does not accept power change request, then it must shut down.

Case 6 addresses the situation with three receivers. Each receiver might have different characteristics as introduced in Case 1 to Case 5. So, the system can handle the only

operation at the overlapped area for all of the units. In this case, the transmitter only provides a constant I_p through all the situation, there will be a reduced system operating range. For example, a large value of I_p gives the derived power and V_{rec} for receiver 1, but it causes over-voltage on receiver 2. So, the cooperation between a single transmitter and multiple receivers requires a system level controller and communication.

6.3 The impact of variable I_p on system efficiency

With the control scheme of the single-stage transmitter, I_p is regulated to the desired value by adjusting V_{ab1} according to (3-51). Maintaining I_p constant helps smooth the transient when the load changes. However, implementing the same value of I_p overall a wide power range decreases system efficiency. In order to investigate the impact of various I_p on the system efficiency, the loss from the transmitter, transmitter coil, receiver coil and diode rectifier with respect to I_p is estimated. The sum of these losses is the total loss of the system.

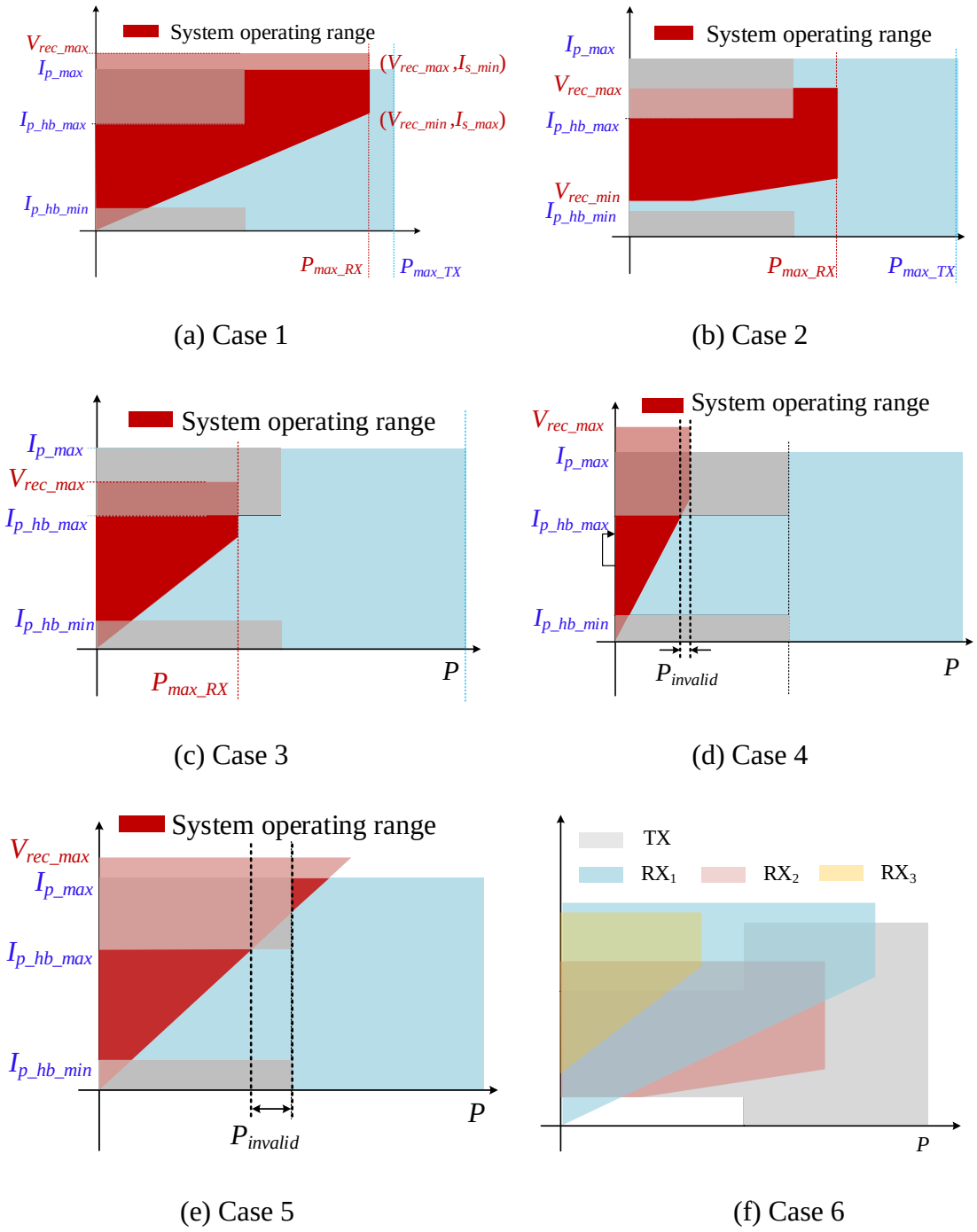
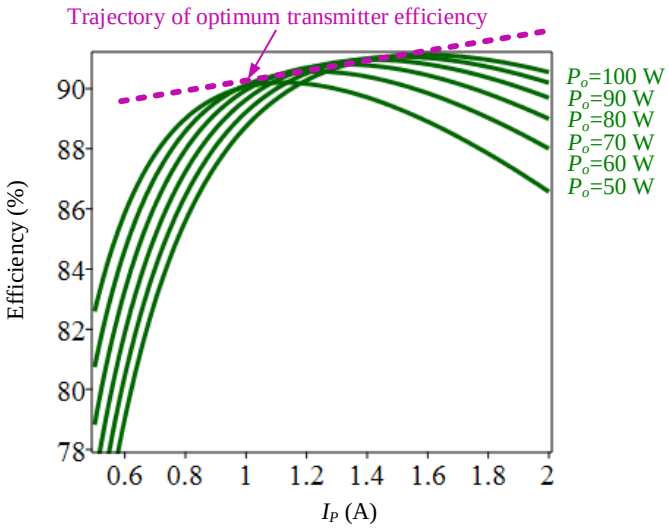


Fig. 6.7. System operating range.

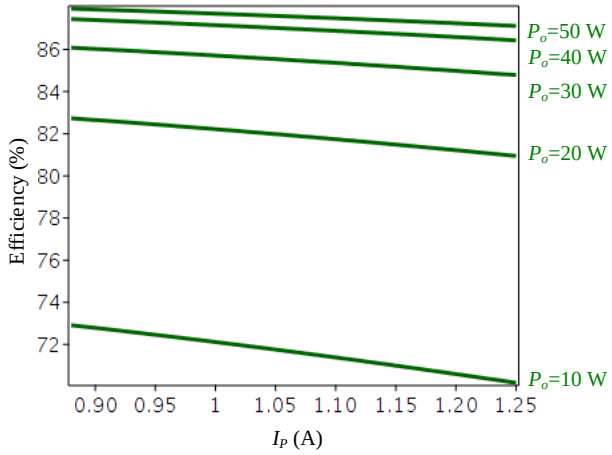
6.3.1 The impact of variable I_p on the transmitter efficiency

Using the loss model developed in Section 4.4, the transmitter efficiency for varying I_p is shown in Fig. 6.8. Fig. 6.8(a) shows the efficiency versus different I_p in heavy load mode. The pure resistive load is assumed in this loss estimation. In this work, the maximum I_p is designed as 2 A as discussed in Chapter 4. In heavy load mode, I_p can be changed from 0 to I_{p_max}=2 A. Since the efficiency drops quickly when I_p <0.6 A, it is ignored in Fig. 6.8(a). Based on a fixed T-type filter, I_p changes proportionally to V_{ab1}. Large I_p requires large V_{ab1}, therefore small I_{inv} at the same power level. If I_p is very large, the loss increase in L_{f2} is significant. However, small I_p needs small V_{ab1}. To get the same power, I_{inv} increases. Large I_{inv} causes high conduction loss in devices and in the resonant tank. Because of these two reasons, the efficiency curves show a non-monotonic shape.

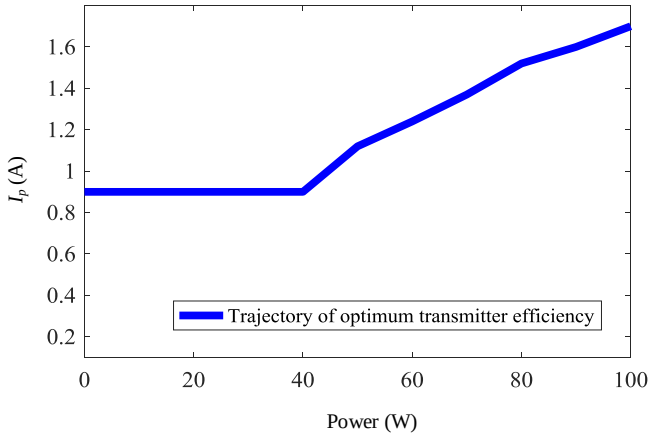
Fig. 6.8(b) shows the efficiency versus I_p in light load mode. In light load mode, due to the limited duty cycle of the half-bridge, the variable range of I_p is reduced as discussed in Section 5.2.1. This plot shows that I_p has a minor impact on the efficiency in light load mode. In addition, the relationship between I_p and the efficiency in this mode is simply monotonic. Lower I_p gives slightly higher efficiency. Fig. 6.8(c) gives the trajectory of optimum transmitter efficiency respects to I_p.



(a) In the heavy load



(b) In the light load



(c) Model-based trajectory of optimum transmitter efficiency

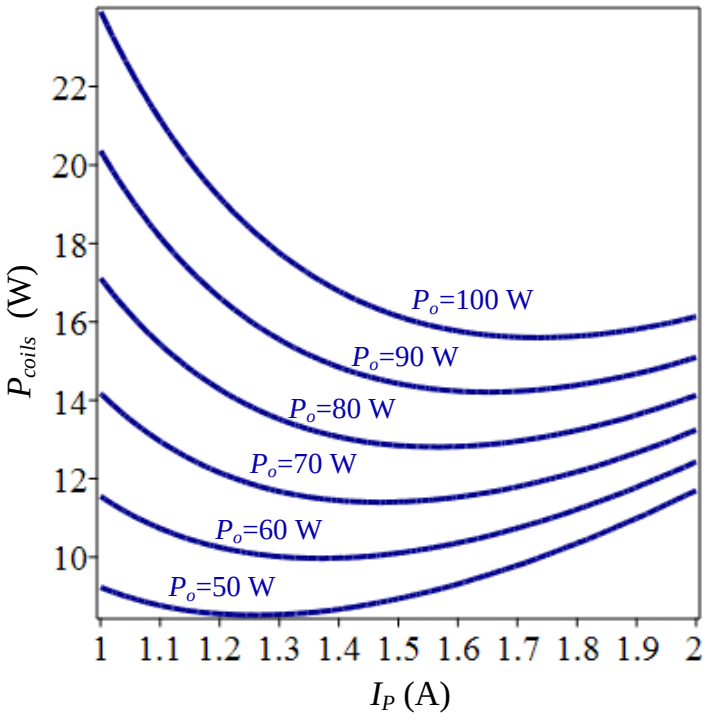
Fig. 6.8. Transmitter efficiency *vs.* I_p.

6.3.2 The impact of variable I_p on the loss of coils and diode rectifier

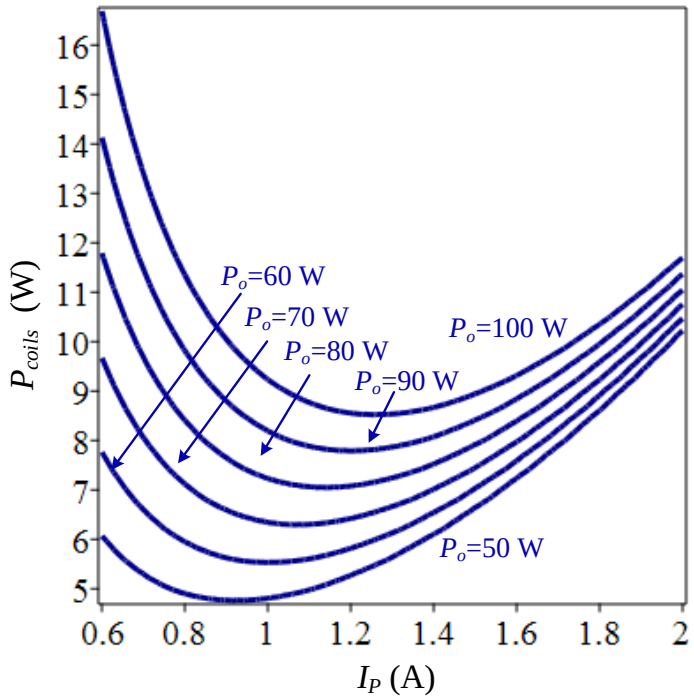
The loss in the transmitter coil is $P_{coil\_TX}=I_p^2 \cdot R_p$. R_p is the ESR of the transmitter coil. It is clear that large I_p causes a significant loss in the transmitter coil. The current through receiver coil is determined by I_p, the mutual inductance of transmitter coil and receiver coil M and output power P_{coil_RX}. When the position of receiver changes, the loss in receiver coil changes. To estimate the impact of I_p on the coils, an example configuration is used. Use a transmitter coil (a 22 cm × 22 cm rectangular shape coil, R_p=2.3 Ω) and a receiver coil (a 12 cm × 12 cm rectangular shape coil, R_s=0.6 Ω) are used to demonstrate the impact of different I_p on the lossThe loss in the diode rectifier is estimated by averaging $Is \cdot V_F$ in a half switching cycle. The Schottky diode V8PMa2 is used in the estimation. The total loss of the coils and diode rectifier based on these given parameters is plotted in Fig. 6.9. Fig. 6.9(a) shows the loss when k=0.06 and Fig. 6.9(b) shows the loss when k=0.12.

Large I_p results in a substantial loss in the transmitter coil and small I_p causes a significant loss on the receiver coil and diode rectifier. The transmitter coil loss is barely impacted by the coupling coefficient. However, I_s is lower with larger coupling coefficient at the same power level. So, the loss of the coils with k=0.12 is lower than the loss when k=0.06.

$$I_s = \frac{P_o}{V_{oc}} = \frac{P_o}{\omega M I_P} \tag{6-13}$$



(a) k=0.06



(b) k=0.12

Fig. 6.9. The loss in the coils and diode rectifier *vs.* I_p.

6.3.3 System efficiency optimization with variable I_p

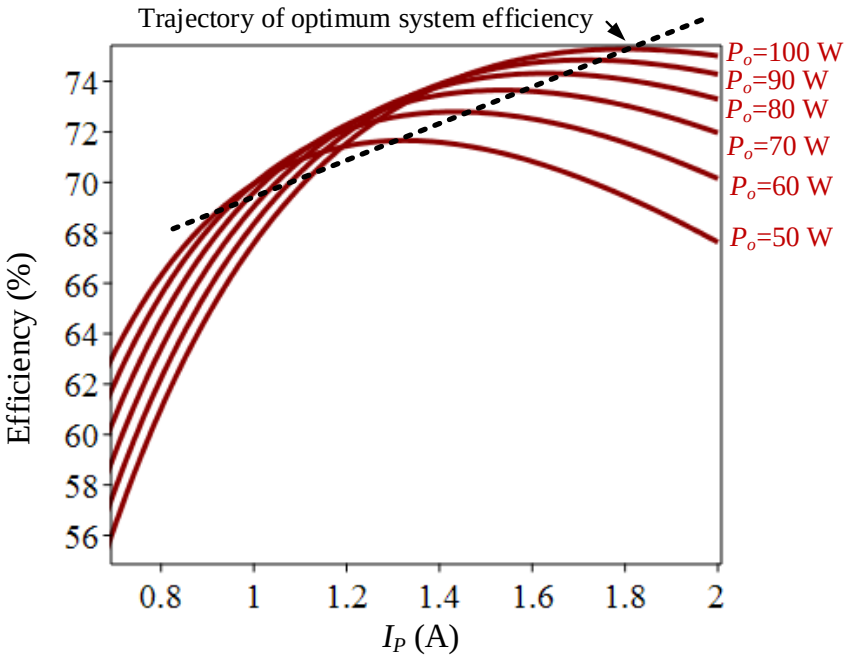
According to the transmitter loss, coils loss and diode rectifier loss, the system efficiency is calculated and shown in Fig. 6.10, based on the conditionn of k=0.08. The black dashed line is the trajectory of optimum system efficiency. According to this plot, reducing I_p at lower power helps maintain high system efficiency.

Note that the system efficiency optimization in practice cannot be achieved without additional control variable in the receiver side. Typically, the dc-dc converter placed at the output of dull bridge diode rectifier provides this control variable (R_{dc}) as discussed in Section 6.1.2. The system efficiency is optimized by I_p. Both of R_{dc} and I_p can be used to control the power delivery. So, with the cooperation of R_{dc} and I_p, the required power and the maximum efficiency can be obtained.

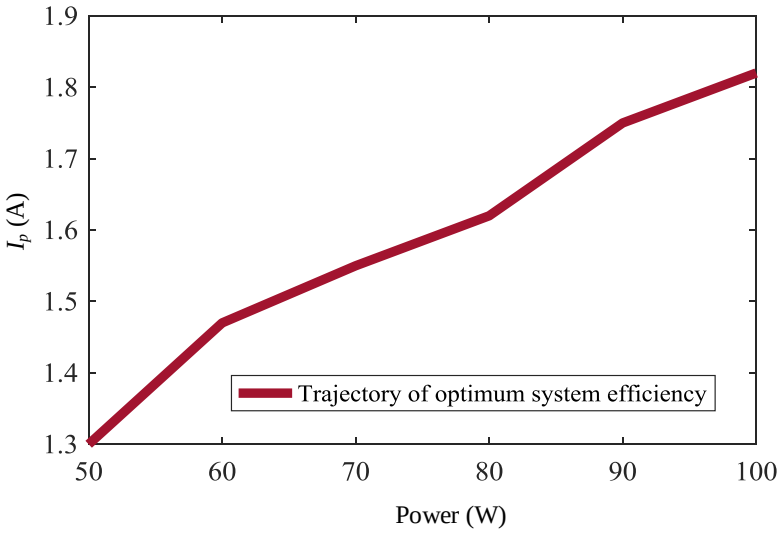
Fig. 6.11 presents the process of achieving optimized system efficiency when the model-based efficiency trajectory is implemented. The utilization of this trajectory is based on several assumptions. First, all the parameters of the receiver are known. Second, the coupling coefficient between the transmitter coil and receiver coil is known and fixed, or real-time measurement of k is implemented. Third, for the system with multiple receivers, the system efficiency optimization becomes more complicated. It is out of the scope of this work. So, the system efficiency optimization is based on a single receiver.

The blue dots represent the normal operation points. The normal operation is the control scheme that maintains I_p the same when the load changes. The green dots show the optimized operation trajectory. The position of dots is just for demonstration. The absolute value doesn't necessarily match with the trajectory shown in Fig. 6.10. Assuming that t_0 is the initial operating point. At t_0, R_{dc} increases which indicate the required output power is

reduced. Since the controller of the transmitter designed in Chapter 5 keeps the I_p constant, P_o reduces automatically. The period between t_0 and t_1 demonstrates this process. But the value of I_p at t_1 is not optimized according to the trajectory. So, the controller starts to change I_p toward the optimized point t_2. When the next load step occurs, this process is repeated.



(b) System efficiency vs I_p



(b) Model-based trajectory of optimum system efficiency

Fig. 6.10. The trajectory of system efficiency optimization.

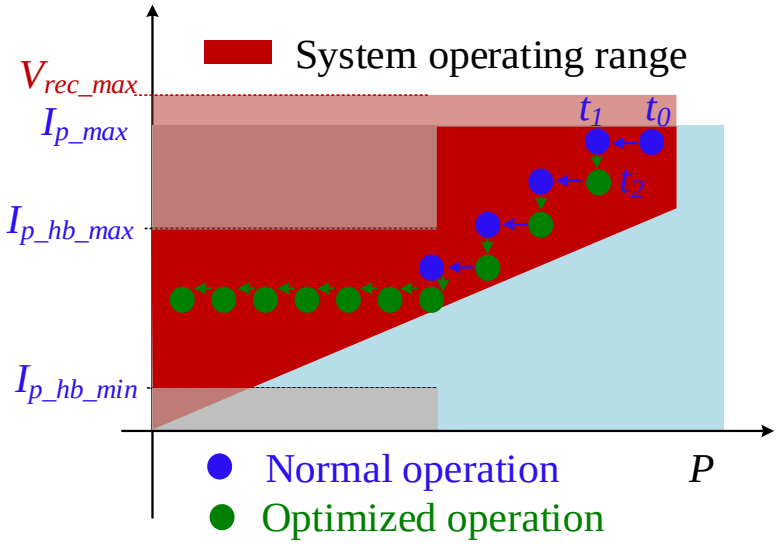


Fig. 6.11. The process of achieving system efficiency optimization.

6.4 The control scheme and procedure of the WPT system

6.4.1 System control scheme

This system implements the autonomous control. The transmitter performs as a master, and receivers are slaves. The transmitter provides I_p through the transmitter coil. All the receivers pick up the required power individually. The benefit of this control method is that the load variation of any receiver will not impact the others. In this system, the control goal of the transmitter is to regulate I_p. I_p is changed to satisfy the system operation requirement in different load conditions.

In this system, I_p is adjusted to achieve several goals. (1) Ensure all the receivers operate within the operating range. The output voltage of each receiver V_{rec} should be lower than the maximum voltage V_{rec_max}. At the same time, V_{rec} should be kept higher than V_{rec_min}. (2) If all the V_{rec} maintain within their operating range, then the system optimization is considered. Multiple receivers might be placed in the system. Two

scenarios can be examined in terms of system optimization. Optimize V_{rec} with the highest percentage utilization of power. The percentage utilization of power is defined as P_{rec}/P_{rec_max}. Or maximize the overall system efficiency. The transmitter needs the parameters from receivers to determine the following actions and operation points.

6.4.2 System control procedure

In order to achieve the system control goal, the control procedure is introduced in this section.

Each receiver reports the dynamic parameter characteristic value (such as V_{rec}, V_L, $I_{L,}$ and etc.) and the signal specifications (such as V_{rec_min}, V_{rec_max}) to the transmitter. With these parameters, the transmitter determines the following control action. There are three states that are defined according to the dynamic parameters from the receiver side.

(1) State 1 addresses the situation that all the receivers operate within the range: $V_{rec\_min}<V_{rec}<V_{rec\_max.}$ Under this situation, the transmitter can choose to optimize the receivers with the highest percentage utilization of power or maximize the system efficiency. The transmitter adjusts I_p to meet the goal. Take Case 6 as an example. State 1 in case 6 is shown in the green box in Fig. 6.12.

(2) State 2 and State 3 present the situation that at least one of the receivers operates out of range. State 2 addresses $V_{rec} > V_{rec\_max}$, while State 3 indicates $V_{rec} < V_{rec\_min}$. If one or more receivers satisfy $V_{rec} > V_{rec\_max}$, I_p should be reduced to the point that V_{rec} is below V_{rec_max}. When I_p is reduced, all the other receivers get smaller V_{rec}. But as long as their value is kept within the specific operating range, the required power is delivered by changing R_{dc} via the controller in the dc-dc converter. But if V_{rec} is lower than V_{rec_min} during the I_p changing, then the one with lower priority will shut down. When the system

works within the range of the blue box in Fig. 6.13, State 2 occurs, because V_{rec} of receiver 2 exceeds the maximum limit.

(3) If all the receivers satisfy $V_{rec} < V_{rec\_max}$, but one or more receivers suffer from $V_{rec} < V_{rec\_min}$ (State 3), then I_p should be gradually increased to let V_{rec} of this receiver meet V_{rec_min}. But if this action causes the other receivers exceeding V_{rec_max}, then transmitter stop increasing I_p to avoid overvoltage. If the system operates in the range of the red box in Fig. 6.13, State 3 occurs because receiver 1 cannot get the large enough V_{rec} for normal operation.

Fig. 6.13 and Fig. 6.14 show the transmitter control scheme with system operation consideration. Compared to the control diagram shown in Chapter 5, the block including communication and system operation decision is added. The communication between transmitter and receiver helps to exchange the dynamic parameters such as V_{rec}, I_{rec}, I_s and V_{oc} from the receiver side. The transmitter judges the system operation status according to this information. Then according to the status, the corresponding I_p command is obtained. Then the controller for transmitter I_p control changes I_p to achieve the required value. To improve system efficiency, two approaches can be adopted. The first approach is based on the predicted loss model. The second method is to sweep I_p and measure the system efficiency. Then, fix I_p at the point with the highest measured efficiency.

The control speed of system optimization should be always slower than the transmitter control loop and the receiver control loop.

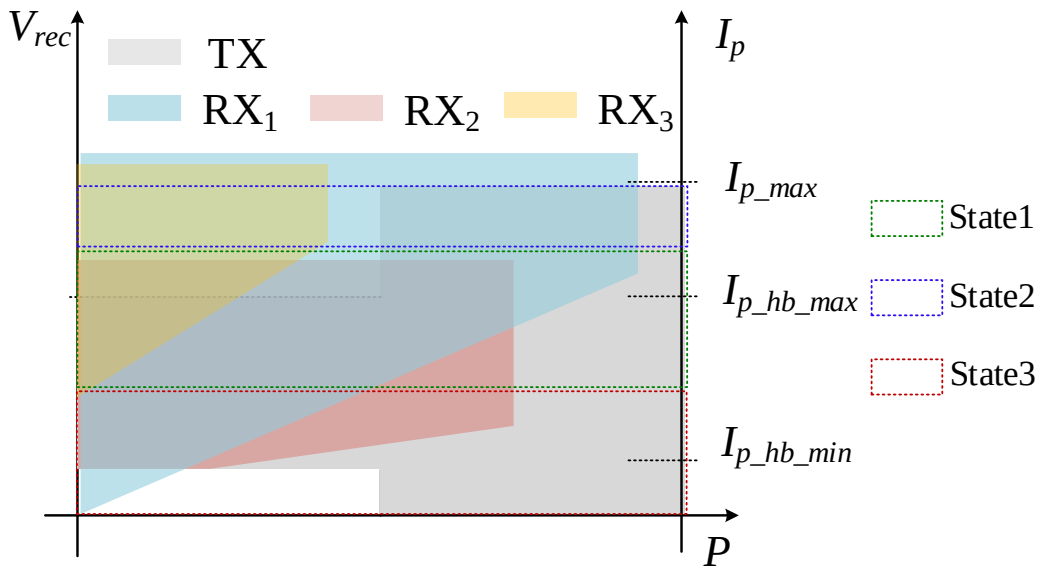


Fig. 6.12. Demonstration of three system operating states.

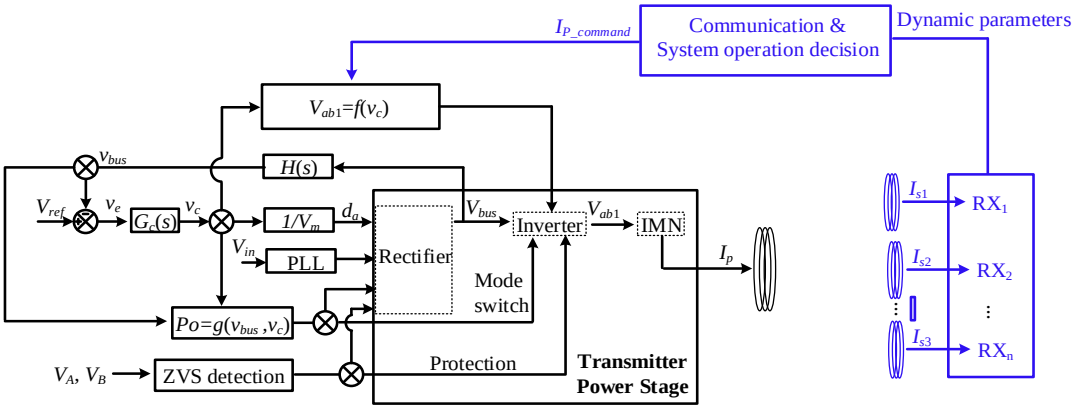


Fig. 6.13. Transmitter control diagram when considering system operation.

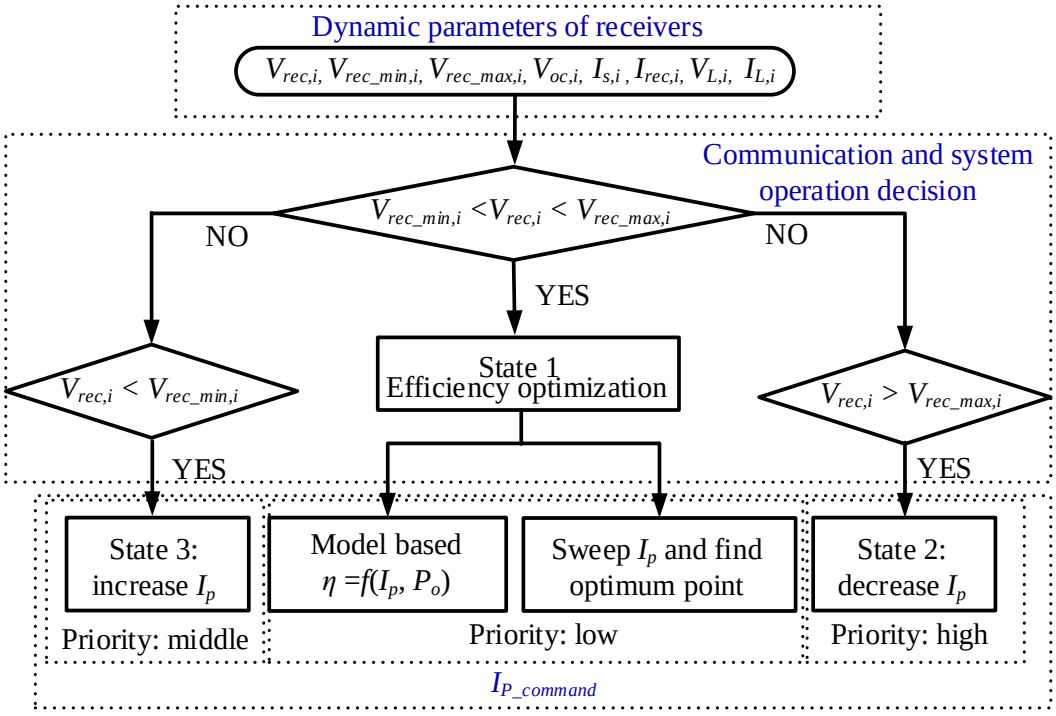


Fig. 6.14. System control flow chart.

6.5 Experimental demonstration

The experiments are designed to demonstrate the capability of the system operation with the single-stage transmitter. The single-stage transmitter is used to supply 6.78 MHz current through the transmitter coil. A full bridge diode rectifier is implemented for the receiver. There is no dc-dc converter for receiver output power regulation. So, the actual power delivered from the transmitter to each receiver fully depends on the value of I_p and the actual load R_L. In addition, there is no actual communication hardware implemented in the system. A button is used to simulate the communication between transmitter and receiver and send the $I_{p\_command}$. This simplified WPT system is considered as valid one for this verification. The main purpose is to demonstrate the capability of the single-stage correctly responding to the different system status and explore the system level control scheme for wide operating range, robust operation and efficiency optimized operation.

6.5.1 Transmitter responses to the system State 2

The experiments in this section and Section 6.5.2 implement the same setup shown in Fig. 5.20. Three receivers are implemented with diode rectifiers. The operating range of all the receivers is based on the assumptions: V_{rec1_min}=1 V, V_{rec1_max}=25 V, V_{rec2_min}=16 V, V_{rec2_min}=32.5 V, V_{rec3_min}=5 V, V_{rec3_max}=15 V. A button is used to simulate the communication.

As introduced above, when one or more receivers incur an overvoltage, the system runs into State 2. In this case, the transmitter should reduce I_p gradually to keep all the receivers within the specified voltage range. Fig. 6.15 shows the system operating range with a single transmitter TX and three receivers RX_1, RX_2, and RX_3. In the beginning, the system operates at the initial operating point as shown in Fig. 6.15. At this time, RX_2 suffers from over-voltage issue due to large I_p. According to the control diagram, when the transmitter has reported the value of the measured V_{rec2}, and it notices that the system is in the State 2, it decides to reduce I_p gradually. The power of each receiver should keep constant during I_p change. This goal can be achieved with the implementation of the dc-dc converter. With the reduced I_p, RX2 moves into the green area where indicates all limitations are met. Also notice that when V_{rec2} decreases, V_{rec1} and V_{rec3} would reduce as well. But they are still in their specified range.

This case is demonstrated in the experimental waveform shown in Fig. 6.16. At t_0 where is the initial operation point, V_{rec2} is 35 V. In order to reduce V_{rec2}, the transmitter decreases I_p step by step. At t_4, V_{rec2} reaches 32.5 V. I_p stops decreasing and keeps this value. During this time, V_{rec1} and V_{rec3} decrease as well. With the smaller I_p, the new system operation point is approached.

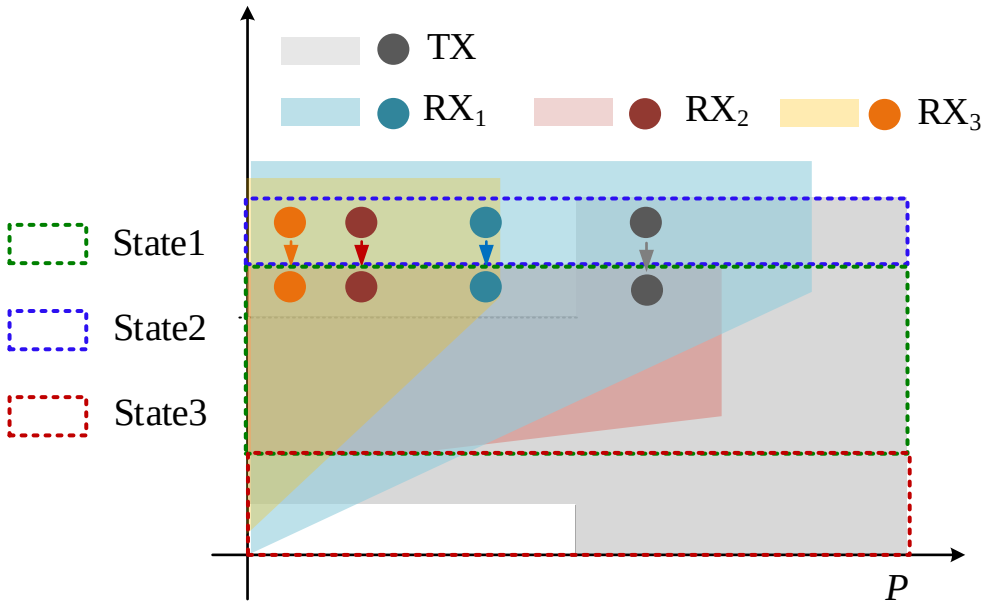


Fig. 6.15. Transmitter responses to State 2.

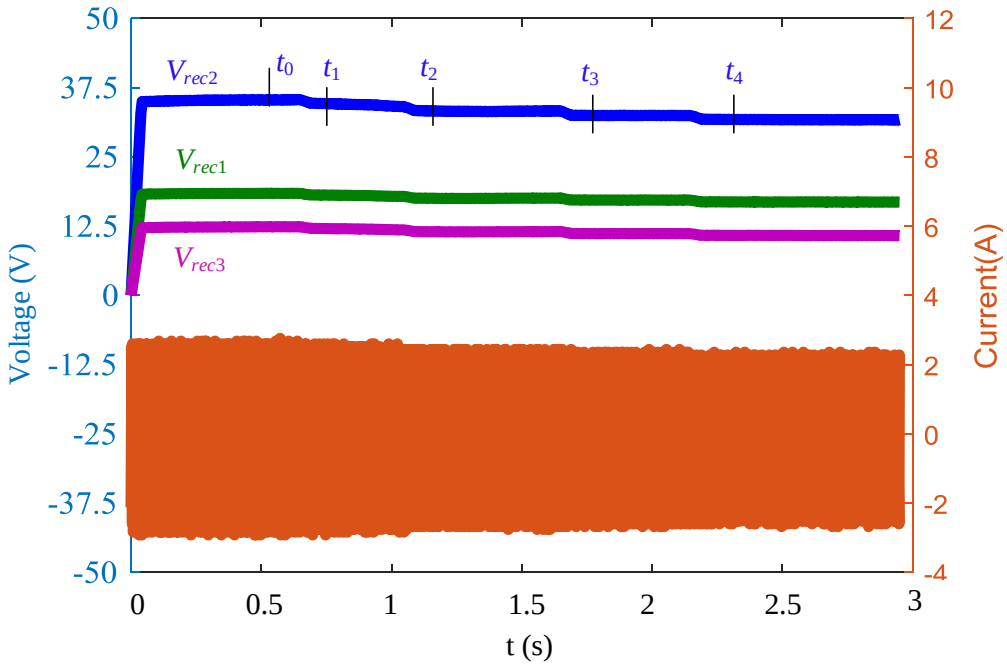


Fig. 6.16. Experimental waveforms of transmitter responses to State 2.

6.5.2 Transmitter responses to the system State 3

A WPT system with a single transmitter TX and three receivers RX_1, RX_2, and RX_3 are set up for this test. Fig. 6.17 and Fig. 6.18 demonstrate the process of the transmitter responding to State 3. At the initial operation point, the output voltage of RX_2 V_{rec2}=15.8 V which is below the specified V_{rec2_min} =16 V. When the transmitter obtains this information, it increases I_p gradually. By t_2, V_{rec_RX2} reaches16.6 V> V_{rec2_min}. With the increased I_p, the new system operation point is obtained.

6.5.3 System efficiency optimization in system State 1

Fig. 6.19 gives the set up for this test. A single receiver is supplied by the transmitter. Fig. 6.20 and Fig. 6.21 demonstrate the process of system efficiency optimization in State 1. As discussed in Section 6.4, when all the receivers work within the specified range, the transmitter starts to optimize V_{rec} of the receiver that has the highest utilization or optimizes the overall system efficiency. In this experiment, assume transmitter chooses to optimize the system efficiency according to the efficiency trajectory in Fig. 6.10 This experiment follows the process discussed in Fig. 6.11. The red curves in Fig. 6.11 show the model-based system efficiency versus I_p at 50 W and 60 W. Assume P_o=60 W at t_0. At the end of t_0, the load changes to decrease the power. First, the controller of the transmitter follows the normal operation and reaches 50 W at t_1 with constant I_p. However,

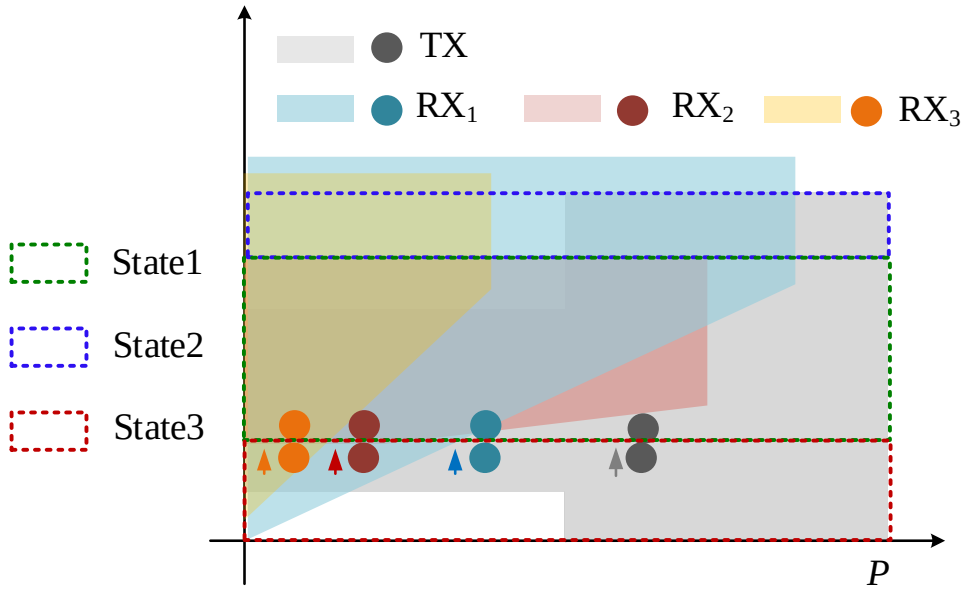


Fig. 6.17. Transmitter responses to State 3.

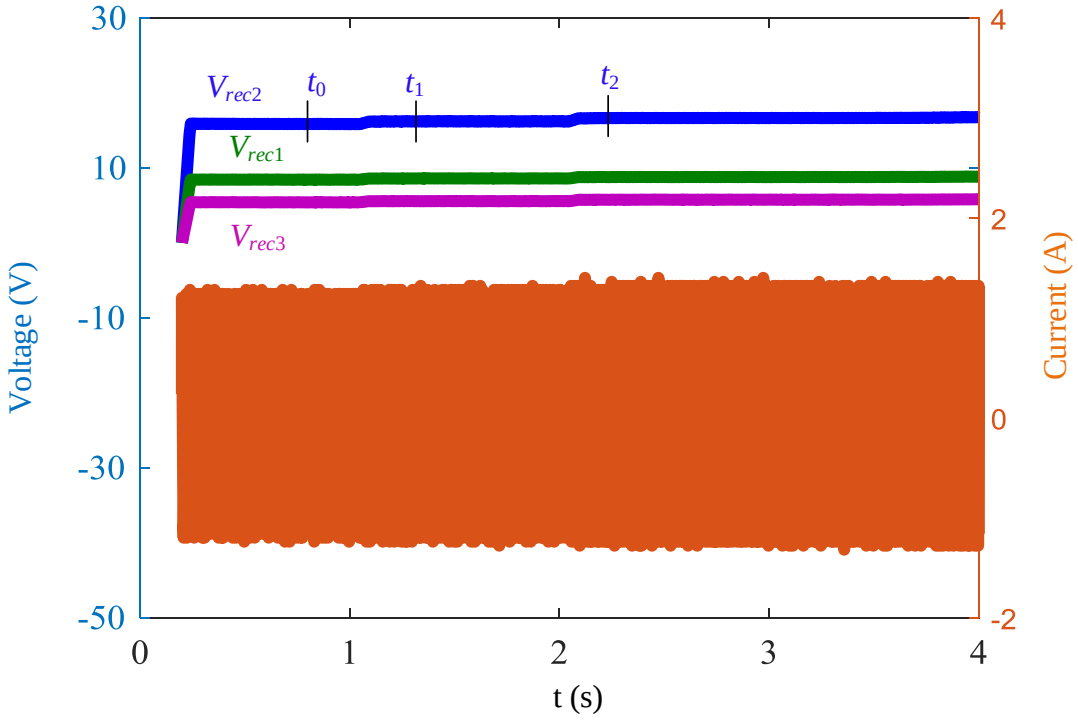


Fig. 6.18. Experimental waveforms of transmitter responses to State 3.

the operation point at t_1 has low efficiency. If follow the 50 W optimized trajectory, I_p should be reduced to get the maximum efficiency operating point at t_2.

The measured waveform demonstrates this optimization process in Fig. 6.21. The receiver used in the experiment only includes the resonator and full bridge diode rectifier. Since there is not control variable in the receiver side, the real system optimization cannot be verified accurately. When I_p changes, V_{rec} changes, the desired output power also changes. The initial operating point is 61 W with I_p =1.8 A at t_0 in this test. At end of t_0, change the load to 52 W. Constant I_p is maintained as shown in the experimental waveform from t_0 to t_1. The measured efficiency during this period is 67.8%. At t_1, the transmitter starts the system efficiency optimizing process to reduce I_p. At t_2, it reaches the new operating point with 70% efficiency. The efficiency is improved by 2.2% via this optimization.

In the future, a dc-dc converter will be added at the output of diode rectifier to better control the output power. The communication block will be added. With a completed WPT system, this method of tracking maximum system efficiency will be further examined.

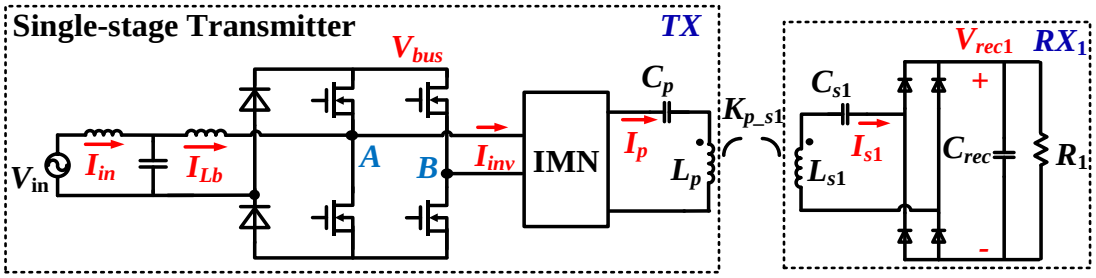


Fig. 6.19. System setup for the demonstration in State 1.

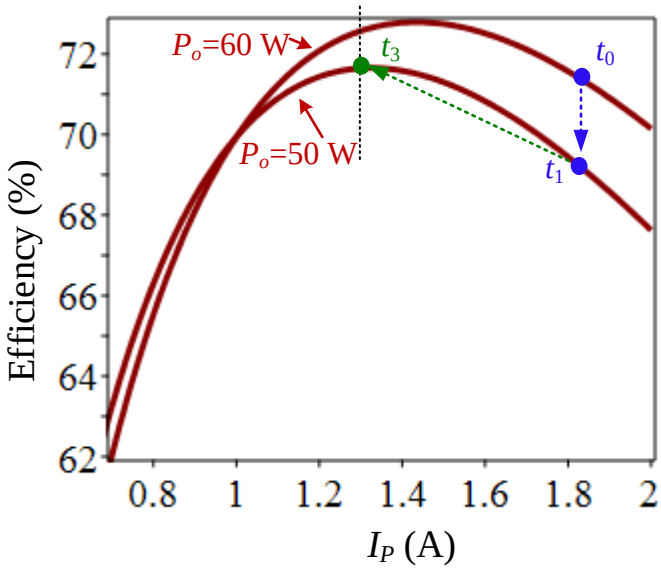


Fig. 6.20. Estimated system efficiency optimization in State 1.

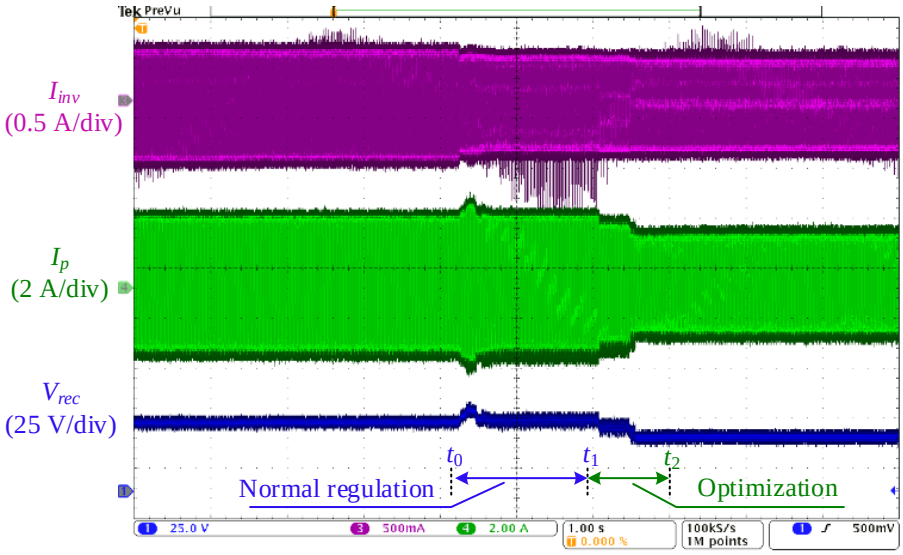


Fig. 6.21. Experimental demonstration of system efficiency optimization.

6.6 Summary

This chapter discusses the operation of a WPT system with the proposed single-stage transmitter. The reactive load range of the transmitter is investigated. Based on this range, the types of receivers that can be charged in this system and the position of receivers can be defined. The method of defining system operating range is introduced. The impact of variable I_p on the system efficiency is studied. Based on this relationship, transmitter current is utilized to track the maximum system efficiency. The system level control scheme for multiple receiver application is discussed. With varied I_p, the transmitter can provide a wide operating range for the receivers. These ideas are demonstrated in the experiments.

7 CONCLUSION AND FUTURE WORK

7.1 Conclusion

7.1.1 Summary of the work

In this thesis, alternative transmitters are proposed to increase the efficiency and to reduce the parts count.

The main research efforts on the low power to medium power range WPT transmitter including transmitter design/optimization, compensation network design and coil design/optimization. Those design and optimization are accomplished separately. So, even if each stage has excellent performance and high efficiency, the overall efficiency might drop significantly. Especially if the commercial ac-dc adapter is used at the front-end stage of the transmitter, an additional dc-dc converter might need to adjust bus voltage for the specific transmitter design. The overall part count is large.

In order to design the transmitter in a more efficient way, achieving high efficiency with fewer components, a two-stage transmitter architecture including the ac-dc PFC rectifier and full bridge high frequency resonant inverter is proposed. The PFC rectifier employs a totem-pole rectifier to get high PF and low THD with the simple regulation scheme. An experimental prototype verifies this idea with measured PF 0.99, THD 4.5%, and efficiency of 91.7%.

To further reduce the part counts, the single-stage ac-ac transmitter is derived by integrating the two-stage transmitter. Two-GaN FETs are saved. Meanwhile, high PF, low THD, and high efficiency are maintained. The measured PF is 0.99, THD is 10.2% and efficiency is 90.4%. In addition, this single-stage converter can achieve higher power

density for two reasons: (1) fewer components; (2) the high frequency ac-ac converter can shrink the size of passive components. The control of the single-stage transmitter is quite challenging because multiple functions have to be achieved within in a single converter.

A closed-loop control scheme is implemented in the single-stage transmitter to supply multiple receivers simultaneously. With a constant current control scheme, smooth dynamic performance is observed during load changes. This method is verified when the single-stage transmitter supplies a single receiver, two receivers, and three receivers in the experiment. The full power range operation of the single-stage transmitter, including the limitations and the procedures, is discussed and verified with experiments. A ZVS detection circuit is implemented to avoid operation with hard switching when out of range loading condition occurs.

The WPT system with the implementation of the single-stage transmitter and single/multiple receivers is investigated. Two advantages are gained from the variable I_p at different load condition. First, it extends the system operating range when multiple receivers are applied. Second, it has the capability of tracking maximum system efficiency. Experiment results demonstrate the WPT system operation.

The control scheme of the single-stage transmitter is concluded: (1) Constant I_p control scheme is implemented during a dynamic load change. (2) After the system is stabilized in the new operation point, examine the dynamic parameters from receivers. Then, according to the current system status, make the decision to achieve the optimum system operation by adjusting I_p.

The comparison of the efficiency and number of power semiconductor among the two-stage transmitter(light green star), the single-stage transmitter (red star) and the ones in the

literature review are summarized in Fig. 7.1. The two-stage transmitter achieves the highest efficiency with eight power semiconductors. The single-stage transmitter achieves the second highest efficiency with six power semiconductors. Compare to the transmitters in the literature review, both of two-stage transmitter and single-stage transmitter achieve the design goal that is obtaining high efficiency with less number of power semiconductors.

7.1.2 Contributions

The contributions of this work are summarized as follows:

(1) A two-stage transmitter architecture is proposed to improve the efficiency and reduce the part counts for the medium range WPT system.

(2) The methods of reducing the THD of CRM operated totem-pole rectifier are investigated and verified. The current spike when the input voltage crosses zero is solved by the proposed method.

(3) The full bridge resonant inverter with an IMN is designed to achieve high efficiency and constant current source behavior.

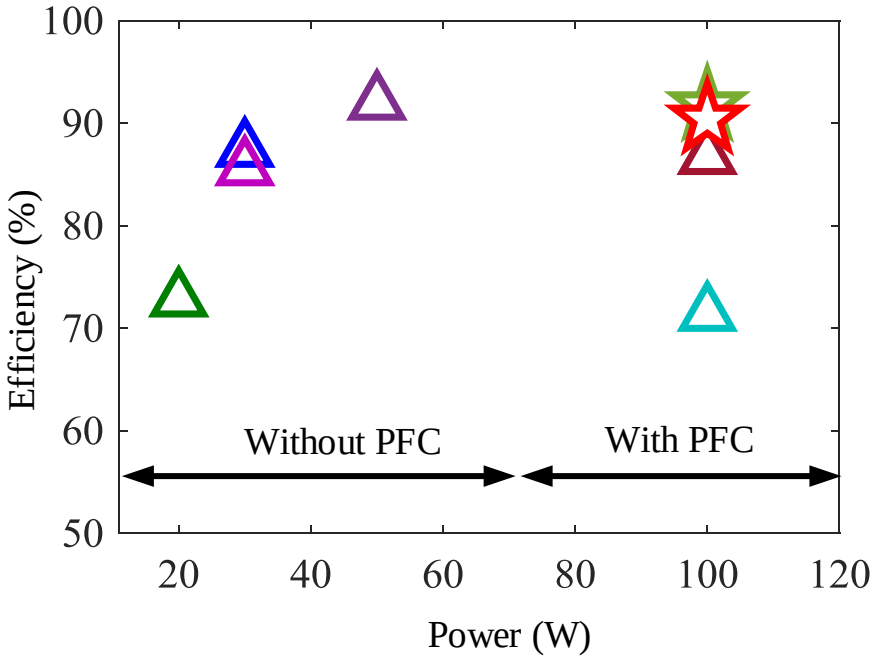
(4) The single-stage transmitter is proposed to reduce the part count and maintain high efficiency.

(5) A control scheme is implemented to regulate the input and output power.

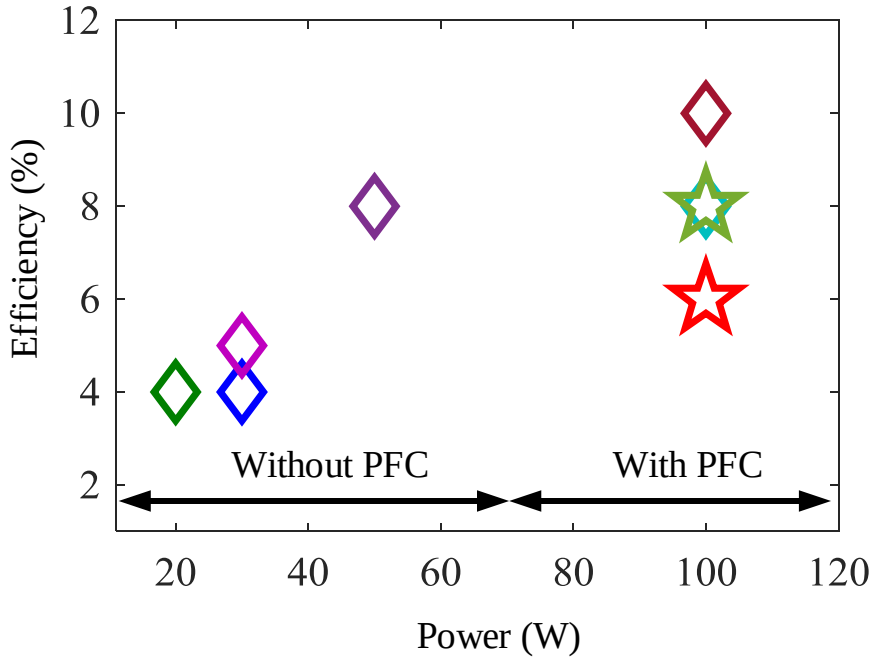
(6) An auxiliary circuit is proposed to improve the light load power efficiency of the single-stage transmitter.

(7) A closed-loop control scheme is introduced to provide constant transmitter coil current I_p which helps smooth the transient performance.

(8) Variable I_p at different load/system condition is considered to extend the system operating range and to track the maximum system efficiency.



(a) The efficiency of the single-stage transmitter



(b) Number of power semiconductors of the single-stage transmitter

Fig. 7.1. The achievement of the single-stage transmitter.

(9) ZVS detection circuit is proposed to monitor the hard switching operation.

7.2 Future work

7.2.1 WPT system optimization

A. Optimized transmitter design

Several design parameters can be optimized to improve the efficiency of the transmitter, such as bus voltage, the range of I_p and IMN.

Several factors can be considered to increase the power density, including integration of boost inductor, ZVS tank inductors and the inductors in the IMN. In addition, the DC capacitor takes a large space of this transmitter, so the method of reducing DC capacitor will be detailed in the next section.

B. Optimized WPT system design

First, the WPT system with the single-stage transmitter will be completed. A dc-dc converter will be added at the receiver side. Bluetooth for the communication between the units will be implemented. The optimum system operation, including wide operating range with multiple different types of receivers, and tracking the maximum system efficiency accurately will be verified with the new designed receivers and with the communication function.

7.2.2 Implementation of feedforward control

The controller of the single-stage transmitter can be improved by adding a feedforward control loop in the model based V_{ab1} calculation. Utilizing the real-time sensed V_{bus} can help improve the performance during a load change. In addition, with this feedforward

control, larger ripple voltage might be allowed on the bus. Therefore, the required DC link capacitance can be reduced. Section 7.2.2 to 7.2.4 discuss these ideas.

As discussed in Section 5.1.2, the constant I_p is achieved via a simplified mathematical model. The benefit of the above-mentioned approach is its simplicity of implementation. This model works well if V_{bus} is always maintained at the desired constant value. However, in some situations, V_{bus} might have temporary fluctuation. For instance, during large load step changing, V_{bus} will overshoot or drop depending on the bandwidth of the voltage loop control. If the mathematical model for I_p is still based on the ideal V_{bus}, the fluctuation on V_{bus} eventually reflects on I_p. To eliminate or reduce the impact of the V_{bus} change on I_p, feedforward control is added into the original control diagram as shown in Fig. 7.2. Both of the sensed V_{bus} and duty cycle is used to determine the proper value of α_+. Since the real-time V_{bus} is included in the loop, and α_+ is adjusted to compensate the increased/decreased bus voltage. Thus V_{ab} is able to maintain constant.

However, considering V_{bus} as a variable increases the complexity of the mathematical model. According to (4-14) and (4-16), α_+ is calculated based on the real-time input parameters d_a and V_{bus}. To distinguish the desired bus voltage V_{bus}, the real-time sensed bus voltage is defined as V_{bus_sense}. Then

$$\alpha_+ = g[\xi(\beta_a), V_{bus\_sense}] \tag{7-1}$$

$\xi(\beta_a)$ is too complicated to implement in the controller. So curve fitting is used to simplify the function as discussed earlier. With the consideration of V_{bus_sense}, α_+ is obtained by surface fitting.The contour plot of V_{bus_sense} with respect to α_+ and β_a is shown in Fig. 7.3(a). By extracting a few points from the contour and processing surface fitting in Fig. 7.3(b), the approximate function is obtained in (7-2).

$$\alpha_+ = f(\beta_a, V_{bus\_sense})$$

$$= -5.02 \cdot 10^{-5} \cdot V_{bus}^2 + 0.04683 \cdot V_{bus} - 0.0015 \cdot V_{bus} \cdot \beta_a \quad (7\text{-}2)$$

$$- 0.21 \cdot \beta_a^2 - 12.38$$

The curve from curve fitting is compared with the original contours and are shown in Fig. 7.3(c). It matches well with the original curve

.

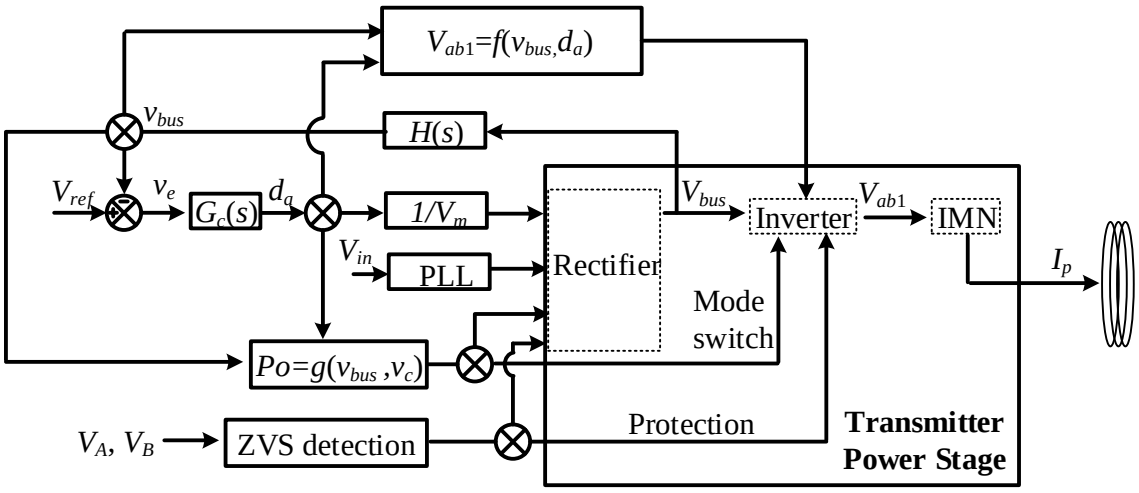
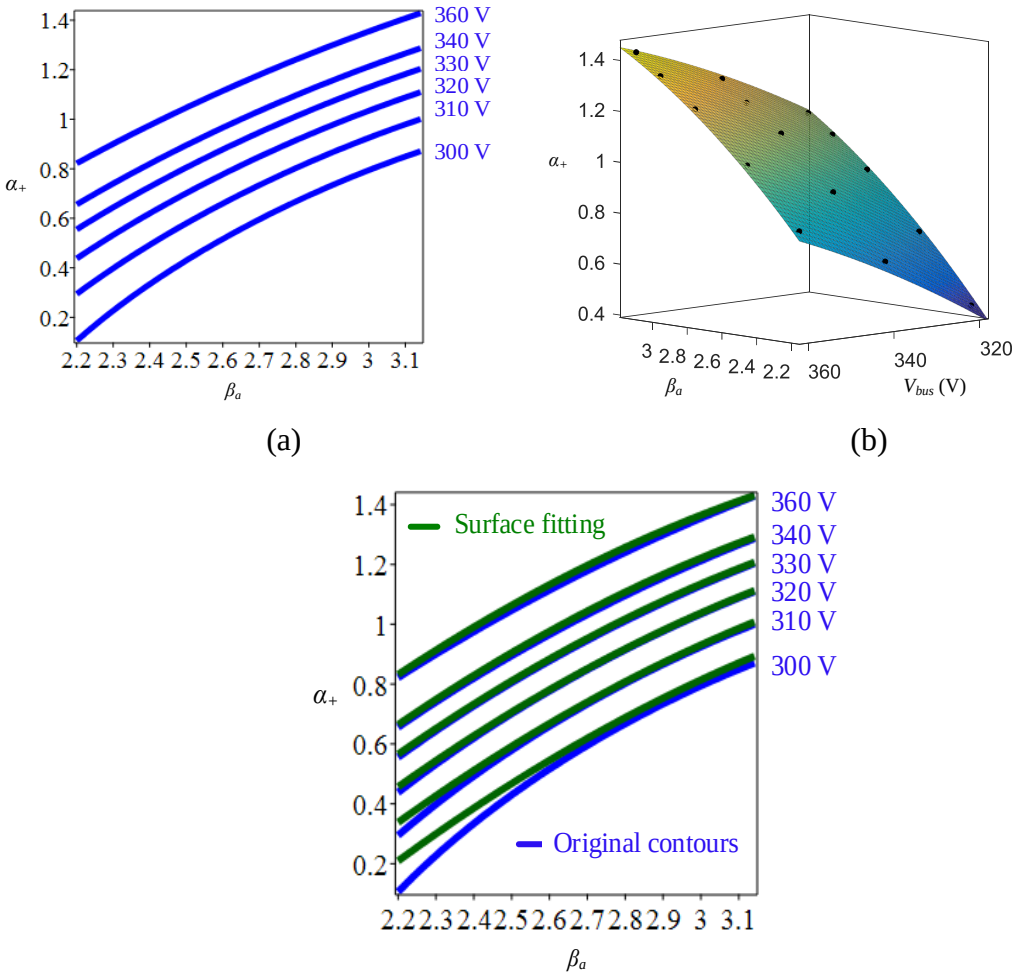


Fig. 7.2. The improved closed-loop control diagram for the single-stage transmitter.



(a) (b)

(c)

Fig. 7.3. Improved mathematical mode via a surface fitting.

7.2.3 Improvement of load change transition by feedforward control

During large load step changes, V_{bus} might have temporary overshoot or undershoot due to the bandwidth of the voltage loop control, as shown in Fig. 7.4. If V_{ab1} is adjusted based on the original model, I_p changes along with V_{bus}.

To improve the transition performance, the feedforward loop is added. This ideal is verified in simulation and shown in Fig. 7.5. With the feedforward control, the overshoot on I_p is reduced by 75%.

7.2.4 Feasibility of reducing DC link capacitor

In the prototype, the volume of DC link capacitors takes 8% of the space of transmitter. If the size of capacitors can be reduced, the power density of the transmitter is increased. According to (4-23), the DC capacitance is determined by the required total energy, the average bus voltage and the allowed ripple voltage on the bus. Since the total energy depends on the power level, it is not changeable. The average bus voltage is selected according to the ac input power quality, the efficiency and control flexibility of the converter. So, it is preferred to keep the desired value. ΔV_{bus} can be changed to reduce the required capacitance. However, large double line frequency ripple is reflected the receiver side and increase the ripple on the output of the receiver. Adding large DC capacitance on the receiver side is typically not preferred, because the size of the receiver is critical.

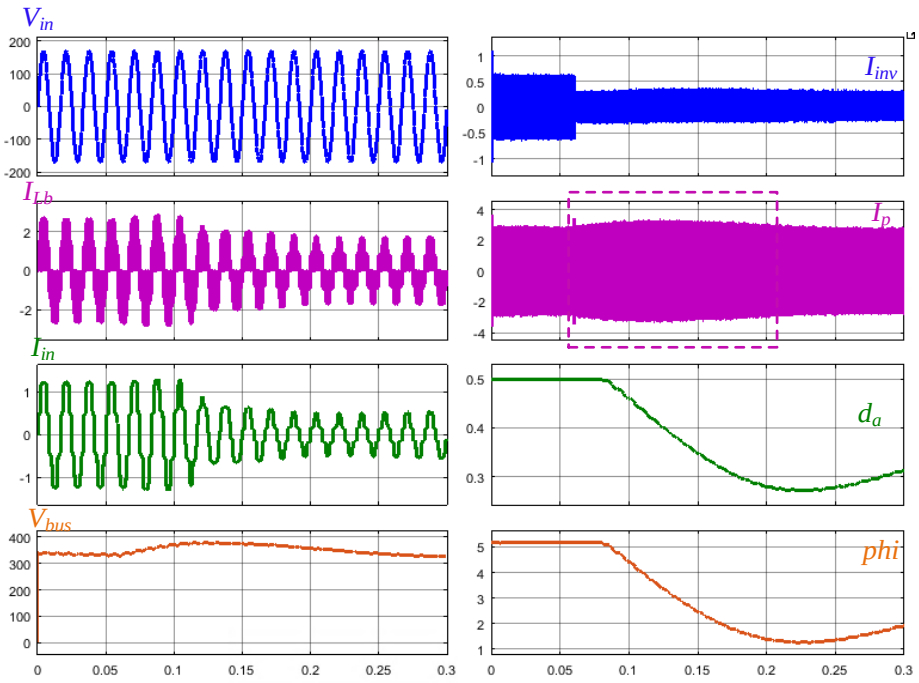


Fig. 7.4. The performance with the original controller during the transition.

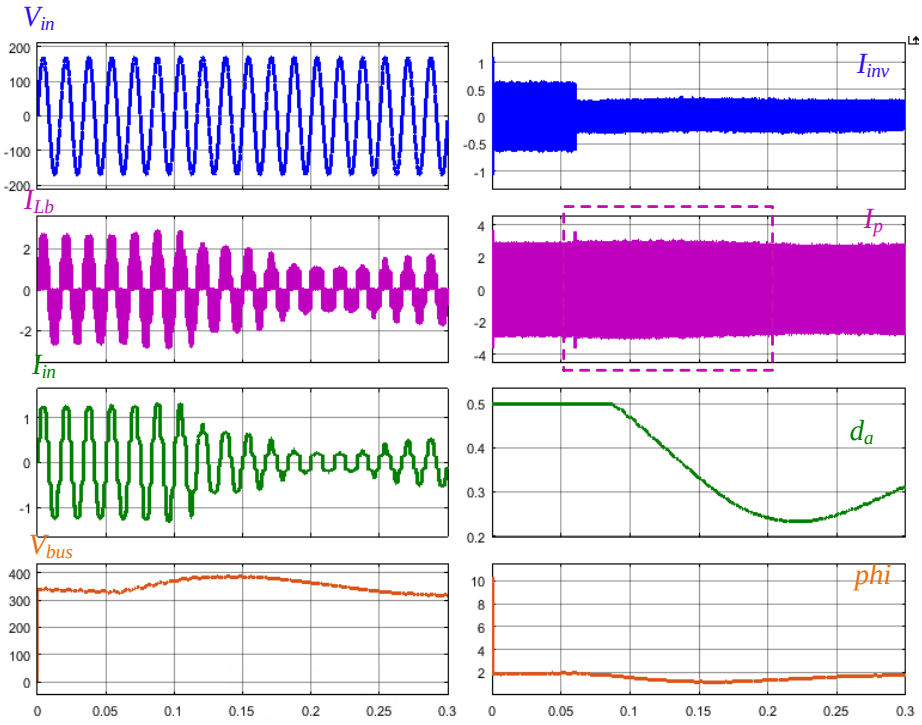
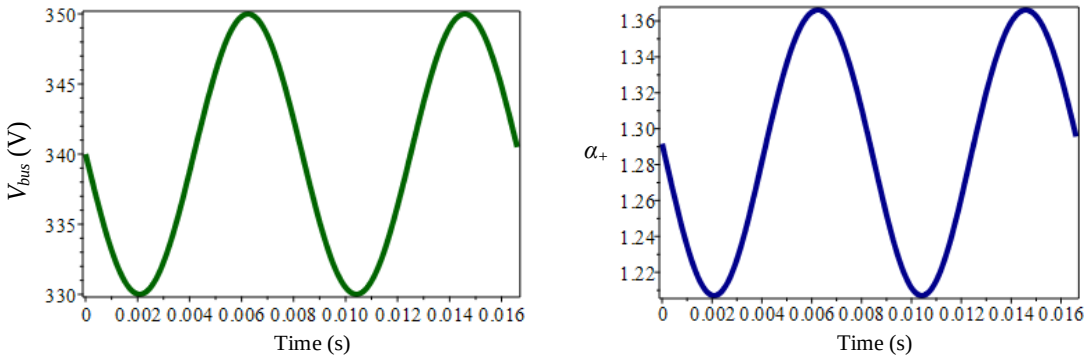


Fig. 7.5. The improved performance with feedforward control during the transition.

The feedforward control is implemented to allow large double line frequency ripple on V_{bus} and suppress this low-frequency ripple at the output of the transmitter, therefore maintaining low ripple on the receiver side. Fig. 7.6(a) shows 20V double line frequency ripple on the bus. Fig. 7.6(b) shows the corresponding α_+ to maintain constant V_{ab1} in the feedforward control loop. In the original transmitter design, 5V ripple voltage is allowed on the bus. When allowing 20 V low-frequency ripple on the V_{bus}, the capacitance can be reduced by 75%.

The feasibility is verified in simulation. Fig. 7.7 shows the performance of transmitter with 40V double line frequency ripple on the bus. In this case, the capacitance is reduced by 87.5%. This low-frequency bus voltage results in low-frequency ripple on I_p. V_{rec}, which is the output voltage of rectifier at the receiver side, also exhibits 120 Hz ripple. With the implementation of feedforward control, the ripple on I_p and V_{rec} are reduced by 60% in Fig. 7.9 compared the one in Fig. 7.7.



(a) Ripple voltage on Bus (b) The trajectory of α_+ for ripple suppression

Fig. 7.6. α_+ changes along with bus voltage.

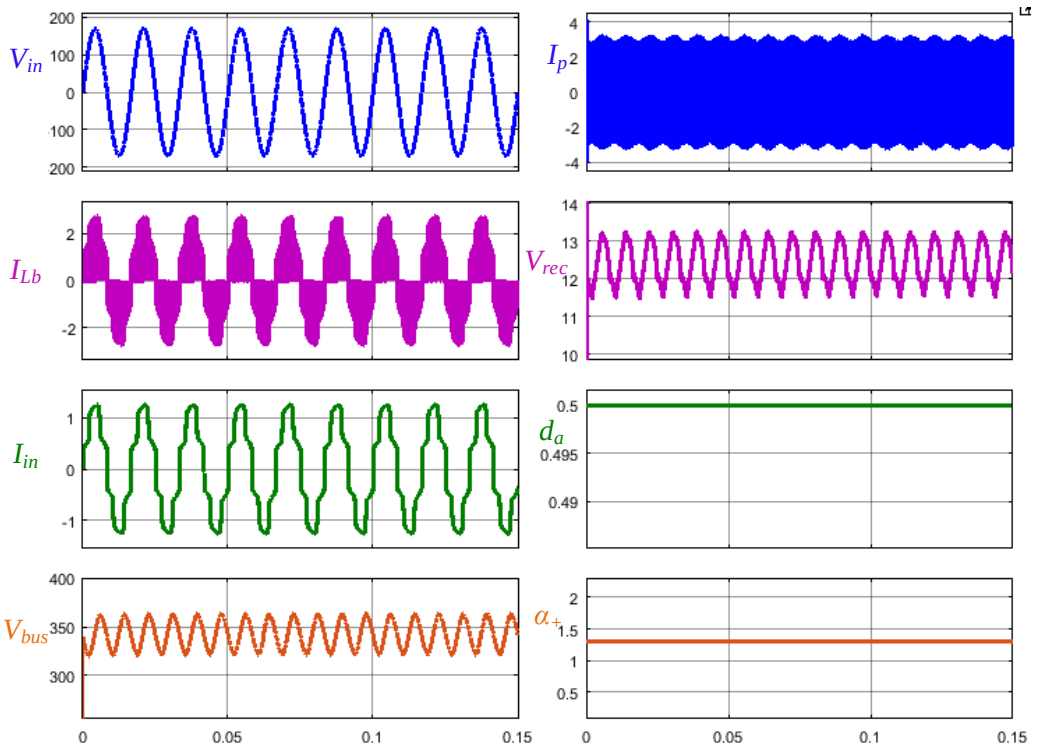


Fig. 7.7. Waveforms with reduced DC link capacitor without feedforward control.

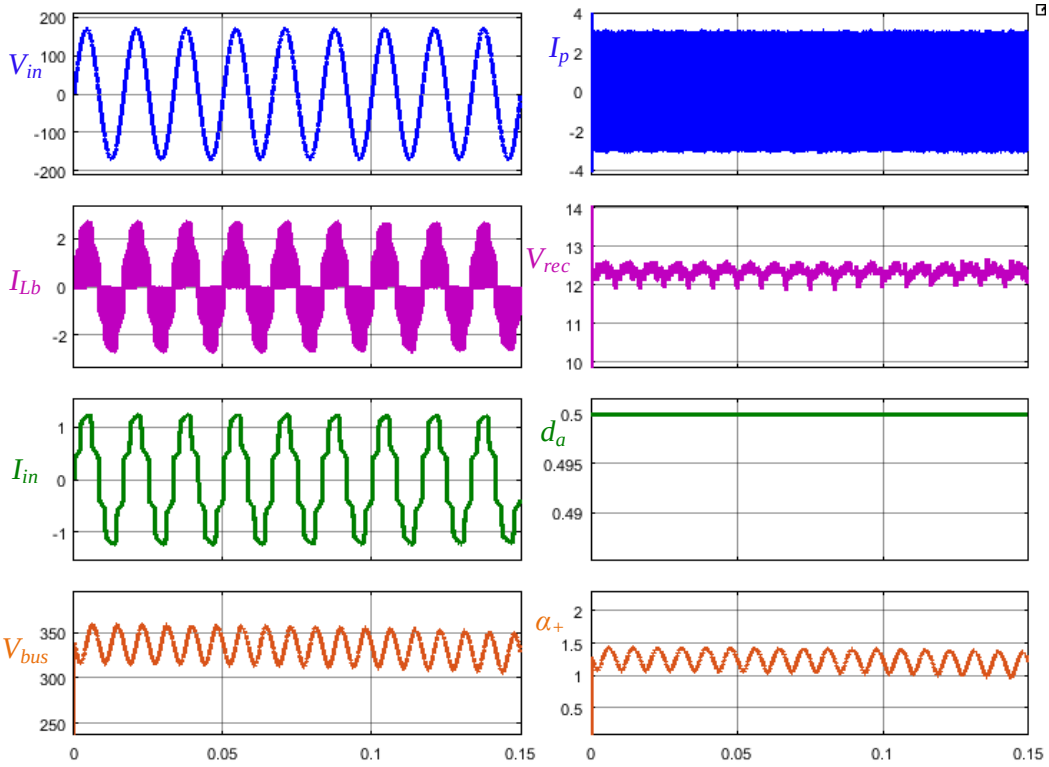


Fig. 7.8. Waveforms with the reduced DC link capacitor with feedforward control.

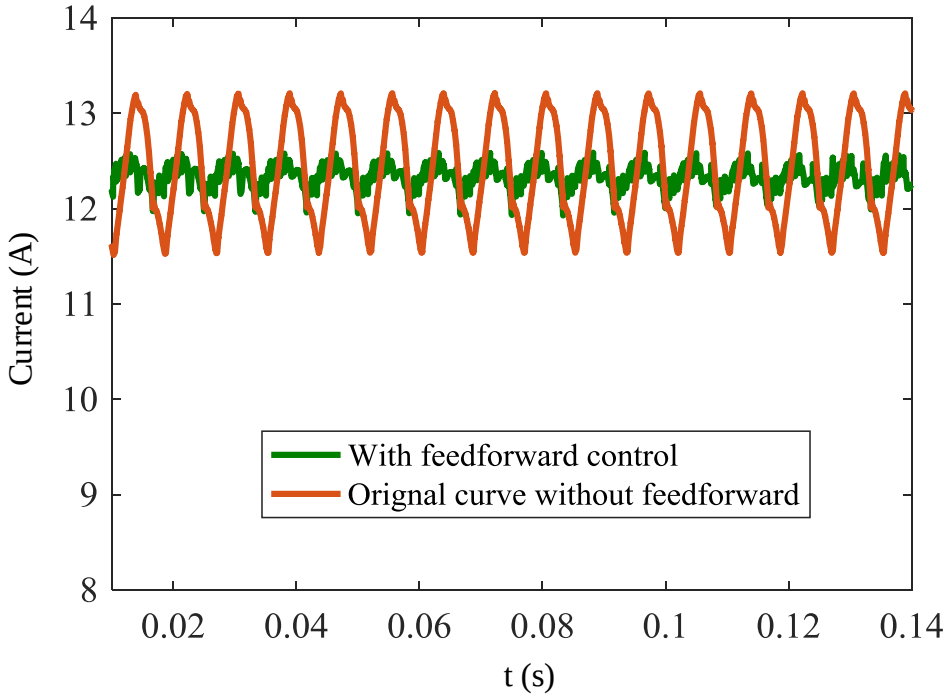


Fig. 7.9. Waveforms with the reduced DC link capacitance with feedforward control.

7.3 Publication list

Journal papers

- **L. Jiang**, D. Costinett, ”A High Efficiency GaN-based Single-Stage 6.78 MHz Transmitter for Wireless Power Transfer Applications”, *IEEE Transactions on Power Electronics*. doi: 10.1109/TPEL.2018.2879958 (early access).
- Chongwen Zhao, Brad Trento, **L. Jiang**, D. Costinett etc., "Design and Implementation of a GaN-Based, 100 kHz, 102 W/in^3 Single-Phase Inverter," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 4, no. 3, pp. 824-840, Sept. 2016.

Conference papers

- **L. Jiang**, D. Costinett, "Voltage Slope-sensing Based Zero Voltage Switching Detection for 6.78 MHz Wireless Power Transfer Application”, Accepted for APEC 2019.
- **L. Jiang** and D. Costinett, "A GaN-Based 6.78 MHz Single-Stage Transmitter with Constant Output Current for Wireless Power Transfer," in *2018 IEEE PELS Workshop on Emerging Technologies: Wireless Power Transfer (Wow)*, 2018, pp. 1-6.
- **L. Jiang**, D. Costinett, "A single-stage 6.78 MHz transmitter with the improved light load efficiency for wireless power transfer applications," in *Proc. IEEE Appl. Power Electron. Conf. Expo*. (APEC), 2018.
- **L. Jiang**, D. Costinett, Aly Fathy, Songnan Yang, "A single stage AC/RF converter for wireless power transfer applications," in *Proc. IEEE Appl. Power Electron. Conf. Expo*. (APEC), 2017.

- **L. Jiang**, Farshid Tamjid, Chongwen Zhao, Daniel Costinett, Aly Fathy, "A GaN-based 100 W Two-Stage Wireless Power Transmitter with Inherent Current Source Output," in *2016 IEEE PELS workshop on emerging technologies: wireless power* (WoW).
- **L. Jiang** and D. Costinett, "A triple active bridge DC-DC converter capable of achieving full-range ZVS," in *Proc. IEEE Appl. Power Electron. Conf. Expo*. (APEC), 2016.

Provisional patent

- **L. Jiang** and D. Costinett, "Single Stage AC/RF Converter in Wireless Power Transfer Application," U.S. Patent PCT/US2017/022 316, Mar. 14, 2017, filed.

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