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Power Electronics Converter Interfaced Power System Emulation Platform Development and Research Demonstration

A Dissertation Presented for the

Doctor of Philosophy

Degree

The University of Tennessee, Knoxville

Shuoting Zhang

May 2019

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Abstract

To provide a more realistic testing environment for power system studies and demonstrations, a hardware test-bed (HTB) platform has been developed by the CURENT at the University of Tennessee, Knoxville, to emulate power systems by programming interconnected three-phase voltage converters (VSCs) to behave like the intended power system components.

In this dissertation, several platforms are developed to extend the HTB emulation capability, including a versatile power electronics converter based transmission line emulator, a hybrid emulation platform with the HTB and the real time digital simulator (RTDS), and a flexible modular multilevel converter (MMC) test-bed for HVDC applications.

For the versatile power electronics converter based transmission line emulator, the algorithms for emulating transmission line lumped model, traveling wave model, transmission line with integrated compensation devices, and faults are proposed and implemented. A combined model is proposed to avoid the switching transients between the normal state and the fault state. Stability analysis is also conducted to locate the boundary conditions of emulating the transmission line stably.

For the hybrid emulation with the HTB and the RTDS, *two* hybrid emulation interfaces are developed to emulate the subsystems of a large system in the HTB and RTDS separately and simultaneously to perform as a whole system. An interface model by combining two complementary ideal transformer model (ITM) interface algorithms are implemented to realize the hybrid emulation stably under different conditions. A time-delay correction method is proposed to compensate the interface time-delay to improve the hybrid emulation accuracy. An analysis of the hybrid emulation stability with two interfaces is also conducted to provide

guidance on the interface algorithm selection.

For the flexible MMC prototype development, a test-bed with 10 full-bridge submodules (SMs) in each arm and flexible topology, switching frequency, and passive component parameters reconfiguration capabilities is developed. A cost-effective method is also proposed and demonstrated to pre-charge the MMC by utilizing a low voltage dc source.

In addition, the potential station transformer saturation issue of line-commutated converter (LCC) HVDC in hybrid ac/dc transmissions is evaluated. The dc fault impact on connected ac system stability is also evaluated by comparing with an equivalent ac fault.

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1 Introduction

1.1 Background and Motivation

Since the "War of currents" between Tesla's alternating current (ac) and Edison's direct current (dc) in the 1880s, the ac scheme has dominated the electric power grid with several advantages over the dc scheme, including the ability to deliver a large amount of electricity over a relatively long distance efficiently through a high voltage alternating current (HVAC) transmission line with the help of ac transformers, cost-effective ac generators and motors, etc. With the development of power electronics technology, delivering electric power through a high voltage direct current (HVDC) transmission line becomes available and provides several distinct advantages over HVAC, including lower cost for bulky electric power delivery over a long distance, faster control capability for ac system support, interconnection between two asynchronous power grids, etc. These advantages make the HVDC scheme a promising solution for integrating remote renewable generation sources.

With the increase of renewable energy penetration, more HVDC projects have been built up and connected to traditional HVAC power grids to deliver a large amount of electricity remotely. The new type of power grid structure and power generation fluctuations of renewable energy sources introduce challenges to operate the mixed ac-dc system stably and safely. In order to provide a more realistic testing environment for power system studies and demonstrations, a hardware test-bed (HTB) platform has been developed by the CURENT at the University of Tennessee, Knoxville, to emulate power systems by programming interconnected three-phase voltage converters (VSCs) to behave like the intended power system components, as shown in Figure 1-1.

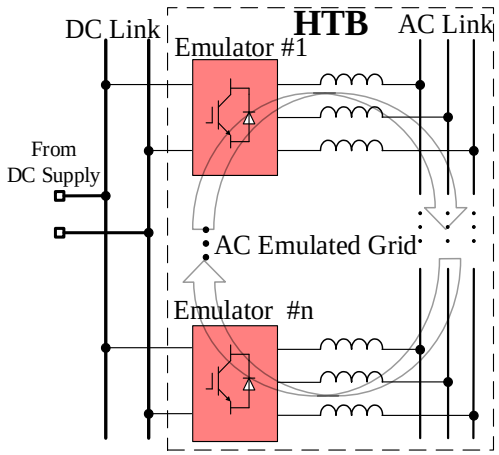


Figure 1-1. System structure of the HTB.

The dc sides of the emulators share a common dc power supply. The ac side of each emulator is controlled to function as a power system component, such as a generator, a load, an energy storage unit, etc. The ac link connection forms the emulated ac grid by connecting each emulated component the same as it is in the original ac grid. Since the emulator VSCs share a common dc link, the active power circulates among the VSCs as indicated by the circulating arrows, and the dc power supply only makes up for the system power loss.

As the bridge of delivering electric power from generators to loads, transmission lines are among the most important components in power grids. Emulating transmission lines is one vital task to build a power system real time emulation platform, like the HTB. Several models can be utilized to represent a transmission line, including lumped models, distributed models, and traveling wave models. The transmission line model selection depends on the transmission line length and power system study requirements. In many cases, transmission lines act as the power delivery bottleneck in power grids and can cause system stability problems. Some compensation

devices have been developed to boost the transmission line power transfer capability, provide power flow controllability, and stabilize the power grid. These compensation devices are connected to the transmission line in series or parallel and include fixed capacitors, thyristor-controlled series compensator, continuously variable series reactor, static synchronous series compensator, thyristor switched capacitors, thyristor controlled reactors, static synchronous compensator, and unified power flow controller. Integrating the compensation devices into the transmission line emulator would be a beneficial way to extend the HTB capabilities. Except for the normal operation conditions, short-circuit faults within transmission lines are the most common disturbances in power grids and are employed for many studies. It is essential for the HTB to have the transmission line short-circuit fault emulation capability.

Comparing with power system digital simulation environments, the HTB is closer to the real system application by allowing real-time system testing and demonstration with real measurement, communication, protection, and control. However, the size of the emulated system is limited by the HTB physical components, and certain phenomena are not easy or not needed to be modeled in the HTB. By emulating the subsystems of a large system in a real-time digital simulator (RTDS) and the HTB separately and simultaneously, the hybrid emulation complements the advantages of the RTDS and the HTB. Similar to the power hardware-in-the-loop (HIL) technique, a hybrid emulation interface with both digital interface and power interface combines the two separate emulation subsystems to perform as a whole system. Different from the purpose of testing a specific device in a regular power HIL setup, this platform is developed mainly for power system studies.

In addition to the traditional power system elements, like generators, loads, and transmission lines, the HVDC emulation is essential to the HTB for the power system studies with a high

penetration of renewable energy. Specifically, the voltage source converter (VSC) based multi-terminal dc technology is the most promising solution for integrating offshore windfarm generation into the power grid. Comparing with other VSCs, such as two-level VSCs and three-level VSCs, modular multilevel converters (MMCs) stand out as a better candidate considering no power switches in series directly and reduced current switching slope (di/dt). Nowadays, researchers are still actively working on different MMC topologies and control algorithms. Building up a MMC test-bed with flexible reconfiguration capabilities of the topology, passive element parameter, and control algorithm is essential for the HTB platform. In addition, MMC submodules (SMs) need to be pre-charged to the rated voltage before normal operations. Pre-charge resistors and bypass breakers are usually utilized to pre-charge the MMC SMs with currents limited by the pre-charge resistors. In HVDC applications, this method needs high voltage high power resistors and breakers, which are bulky and expensive. It is beneficial to develop a small size and cost-effective MMC pre-charge method.

Considering the high cost of building new transmission lines and the social barriers to acquiring the new right-of-way, a hybrid ac/dc transmission concept was proposed to allow ac and dc power delivery through the same transmission line. The hybrid ac/dc transmission can push the power transfer capability of ac transmission lines closer to their thermal limit. The concept and several feasible system topologies of hybrid ac/dc transmission have been verified, and the influence of superimposed dc component on the ac system has been investigated. However, the ac system impact on HVDC has not been studied, such as the potential HVDC converter transformer saturation caused by the dc side fundamental frequency current i_{60}, which exists even in a pure HVDC project.

Though the multiterminal HVDC (MTDC) has been claimed as a promising solution for

integrating remote renewable energy into the power grid, the extreme high rising rate and lack of zero crossing point of the dc fault current are barriers to an economical dc breaker. Usually, short-circuit faults are considered to be more detrimental to dc grids than ac grids. However, the differences between dc and ac grids under fault conditions and their fault impacts on the system stability have not been thoroughly investigated, and different dc fault protection strategies have not been evaluated by considering the ac system transient stability.

The objectives of the research are to develop several platforms to extend the HTB emulation functionality and capability, including a versatile power electronics converter based transmission line emulator, a hybrid emulation platform with the HTB and the real time digital simulator (RTDS), and a flexible modular multilevel converter (MMC) prototype for HVDC applications, to investigate the potential ac system impact on HVDC in a hybrid ac/dc transmission system, and to evaluate the dc fault impact on the interconnected ac system stability.

1.2 Dissertation Organization

The chapters of this dissertation are organized as follows.

Chapter 2 reviews the state of the art research on the transmission line emulator, the power system hybrid emulation, the MMC test-bed, the hybrid ac/dc transmission, and the dc fault impact on ac system stability. According to the reviews, the challenges in these areas and the main objectives of this proposal are identified.

Chapter 3 proposes the transmission line emulation models under normal conditions, including the RL model, T model, traveling wave model, and transmission line with compensation device model. Simulation and experiment results are also presented.

Chapter 4 develops the transmission line emulation models under balanced fault conditions,

and a smooth switching method between the normal state and fault state is proposed. The transmission line emulation stability is also analyzed for both normal states and fault states. Simulation and experiment results are also presented.

Chapter 5 proposes the transmission line emulation models under unbalanced fault conditions, and a negative sequence control method and a time-delay correction method are developed to improve the emulation accuracy. Simulation and experiment results are also presented.

Chapter 6 develops a hybrid emulation platform with the HTB and RTDS. The hybrid emulation stability with two interfaces are analyzed, and a time-delay correction scheme is proposed to improve the interface accuracy. Simulation and experiment results are also presented.

Chapter 7 develops a flexible MMC test-bed. The system structure, control algorithms, and basic functions are presented. A cost-effective method is proposed to pre-charge the MMC by utilizing a low voltage dc source. Simulation and experiment results are also presented.

Chapter 8 investigates the HVDC transformer saturation issue induced by unbalanced transmission lines in the hybrid ac/dc transmission system. Two methods are proposed to solve the problem and simulation results are presented.

Chapter 9 evaluates the dc fault impact on interconnected ac system stability. Simulation results are presented.

Chapter 10 summarizes the work that has been done in this dissertation and provides some recommended future work.

2 Literature Review and Challenges

This chapter reviews the state of the art research on the corresponding areas of the transmission line emulator, the power system hybrid emulation, the MMC test-bed, the hybrid ac/dc transmission, and the dc fault impact on ac system stability. The research challenges are identified and the research objectives are proposed to show the originality of the work.

2.1 Transmission Line Emulator

2.1.1 Transmission Line Models

In power grids, a set of transmission lines consist of several conductive wires, which are constructed side by side for several miles to hundreds of miles. The most accurate way to represent a transmission line would be modeling the self-resistance, inductance, capacitance and the coupling-resistance, inductance, and capacitance with all other transmission lines in every infinitesimal length, as shown in Figure 2-1. However, solving or emulating this complicated model is very difficult and actually not necessary for most power system studies.

Usually, some simplified models are utilized for power system studies, which are divided into three categories, including short line approximation models, medium line approximation models, and long line approximation models. Different transmission line models can be selected for system studies based on the transmission line lengths and the system study objectives.

As shown in Figure 2-2, the lumped RL model, which is a resistor and an inductor connected in series, is utilized to represent a short transmission line since the shunt capacitance is almost negligible [1].

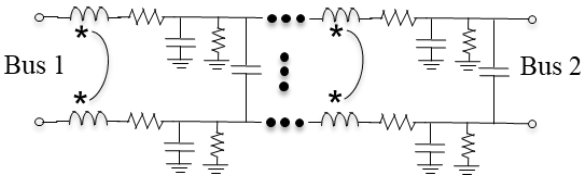


Figure 2-1. Detailed transmission line model.

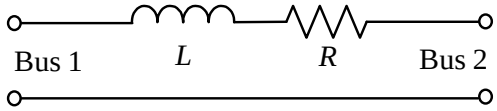


Figure 2-2. Transmission line RL model.

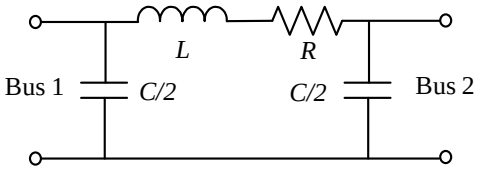


Figure 2-3. Transmission line Π model.

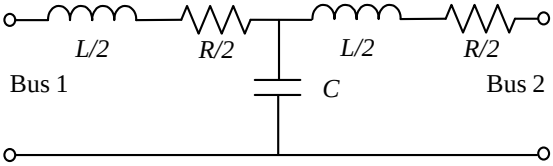


Figure 2-4. Transmission line T model.

For a medium length transmission line, the shunt capacitance is not negligible and can be placed either at the two ends equally as a lumped Π model or at the middle as a lumped T model, as shown in Figure 2-3 and Figure 2-4, respectively [1].

For a long transmission line, the distributed model is preferred instead of a lumped model, as shown in Figure 2-5, where *r*, *L*, and *C* are the resistance, inductance, and capacitance per unit length, *v* and *i* are the voltage and current at location *x*, and *l* is the total length of the transmission line [2]. Assume a lossless transmission line, the traveling wave model can be derived as in Figure 2-6, where the voltage and current relationships are expressed in (2-1) [3].

$$\begin{cases} i_{12}(t) = -\dfrac{1}{Z_0} v_2(t-\tau) + i_2(t-\tau) \\ i_{21}(t) = \dfrac{1}{Z_0} v_1(t-\tau) + i_1(t-\tau) \end{cases} \tag{2-1}$$

where Z_0 and τ are expressed in (2-2).

$$\begin{cases} Z_0 = \sqrt{\dfrac{L}{C}} \\ \tau = l\sqrt{LC} \end{cases} \tag{2-2}$$

By separating a transmission line equally into two sections and adding a lumped *R*/4 at both ends of the two sections, the transmission line with power loss can be approximately represented as a Bergeron model, as shown in Figure 2-7, where *R* is the transmission line total resistance *rl* [3].

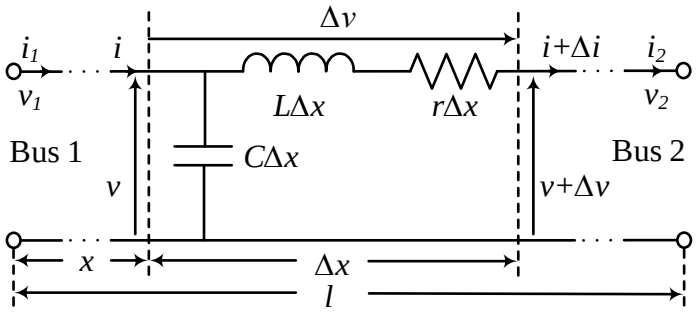


Figure 2-5. Transmission line distributed model.

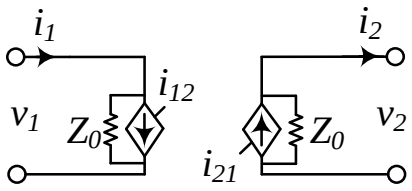


Figure 2-6. Transmission line traveling wave model.

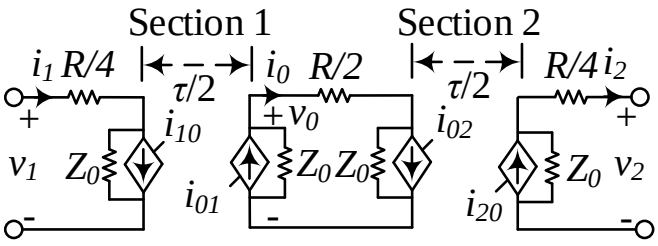


Figure 2-7. Transmission line Bergeron model.

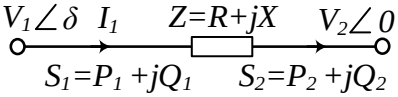


Figure 2-8. Transmission line power delivery diagram.

2.1.2 Transmission Line Compensation Devices

For a simplified transmission line model, as shown in Figure 2-8, the power delivery can be derived as in (2-3).

$$\begin{cases} P_1 = \dfrac{RV_1(V_1\cos 2\delta - V_2\cos\delta) + XV_1(V_1\sin 2\delta - V_2\sin\delta)}{R^2+X^2} \\ Q_1 = \dfrac{RV_1(V_1\sin 2\delta - V_2\sin\delta) + XV_1(V_1\cos\delta - V_2\cos 2\delta)}{R^2+X^2} \\ P_2 = \dfrac{RV_2(V_1\cos\delta - V_2) + XV_1V_2\sin\delta}{R^2+X^2} \\ Q_2 = \dfrac{RV_1V_2\sin\delta + XV_2(V_2 - V_1\cos\delta)}{R^2+X^2} \end{cases} \tag{2-3}$$

Usually, the HVAC transmission line resistance R is much smaller than reactance X, the power delivery in (2-3) can be approximated as in (2-4) [4], [5].

$$\begin{cases} P_1 = \dfrac{V_1(V_1\sin 2\delta - V_2\sin\delta)}{X} \\ Q_1 = \dfrac{RV_1(V_1\cos\delta - V_2\cos 2\delta)}{X} \\ P_2 = \dfrac{V_1V_2\sin\delta}{X} \\ Q_2 = \dfrac{RV_2(V_2 - V_1\cos\delta)}{X} \end{cases} \tag{2-4}$$

Thus, the transmission line power delivery is determined by the line reactance, bus voltages, and power angle difference. To boost the power transfer capacity and gain the power flow

controllability of transmission lines, compensation devices have been proposed and implemented in power grids to realize the flexible alternate current transmission systems (FACTS) by either modifying the equivalent reactance of a transmission line or adjusting the voltages within a transmission line through reactive power injection.

Usually, compensation devices in series with transmission lines are implemented to change the equivalent line reactance. The most straightforward way is to insert a capacitor into the transmission line as a fixed capacitor compensator, as shown in Figure 2-9(a) [6]. The capacitor C can be either inserted into the transmission line to compensate the reactance or bypassed by the bypass switch. This method compensates the line reactance at several discrete values and depends on the number and capacitances of installed fixed capacitor compensators.

To compensate the transmission line reactance continuously, a thyristor-controlled inductor is added to adjust the equivalent reactance smoothly and continuously through the thyristor firing angle, as shown in Figure 2-9(b) [6]. Based on the nonlinear characteristics of magnetic cores, a continuously variable series reactor has been proposed by adjusting the magnetic core saturation point through a dc source, as shown in Figure 2-9(c) [7].

As the development of power electronic technologies, voltage source converters (VSCs) have been introduced to compensate transmission lines, which is named as static synchronous series compensator (SSSC), as shown in Figure 2-9(d) [8]. Because the switching frequencies of VSCs are higher than that of a thyristor, SSSCs can compensate transmission lines with a faster response and lower harmonics than the thyristor-controlled compensators.

Differently, compensation devices connected onto transmission lines in parallel are implemented to inject reactive power. The most straightforward way is to connect a capacitor

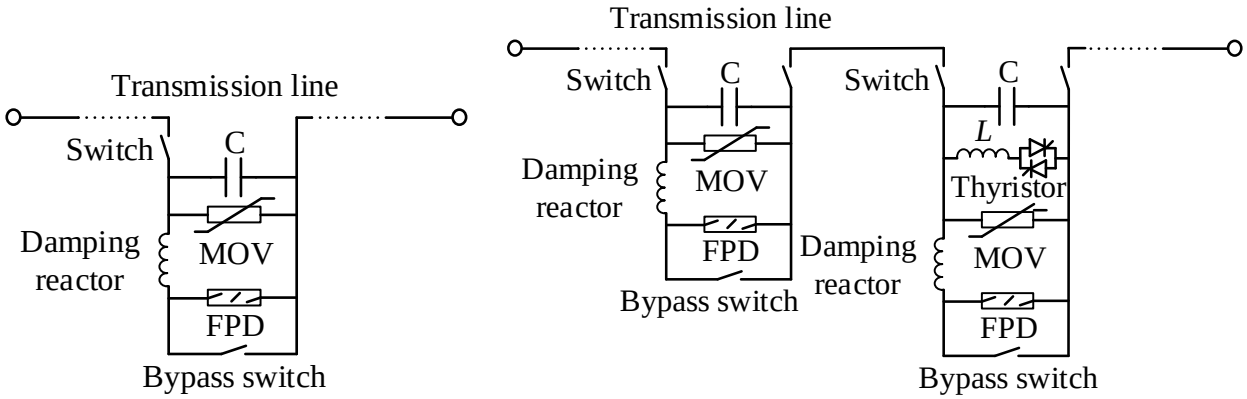
onto the transmission line through a switch as the thyristor switched capacitor parallel compensator, as shown in Figure 2-10(a) [8]. A thyristor-controlled reactor can also be added to adjust the reactive power injection continuously by changing the thyristor firing angle, as shown in Figure 2-10(b) [8]. Similarly, VSCs can be connected to transmission lines in parallel as a static synchronous compensator (STACOM), as shown in Figure 2-10(c) [8].

Combining the SSSC and STATCOM together, a unified power flow controller was proposed to compensate the transmission line in series and parallel coordinately and simultaneously, as shown in Figure 2-11 [8].

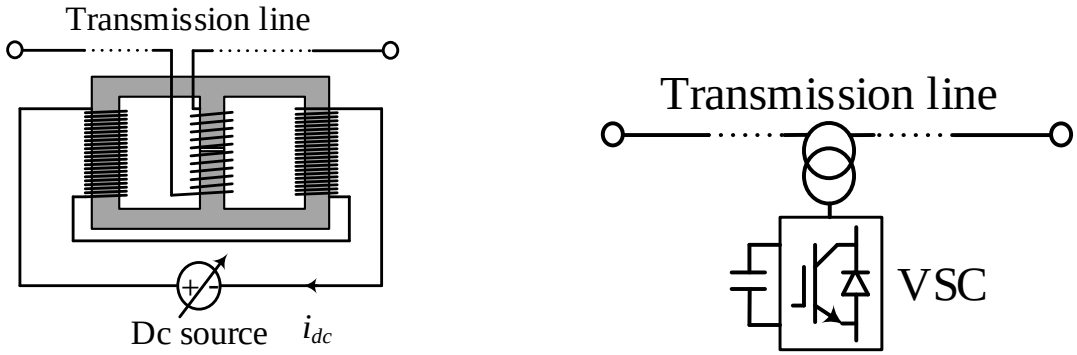
2.1.3 Transmission Line Fault Cases

Being installed in the remote field with lengths of several miles to hundreds of miles, transmission lines are the most vulnerable elements to different types of short-circuit faults in power grids. The faults can be divided into two categories, symmetrical faults and asymmetrical faults.

Symmetrical faults are also called balanced faults, including three-phase faults and three-phase-to-ground faults, as shown in Figure 2-12. As the most severe faults that happen in transmission lines, balanced faults are commonly utilized for power system transient stability studies. Asymmetrical faults are also called unbalanced faults, including line-to-line faults, line-to-ground faults, and line-to-line-to-ground faults, as shown Figure 2-13. As the most frequently occurring faults in transmission lines, unbalanced faults are widely utilized for relay protection studies and unbalanced control investigations of power electronic converters in power grid applications.



(a) (b)



(c) (d)

Figure 2-9. Transmission line series compensation devices: (a) Fixed capacitor series compensator; (b) Thyristor controlled series compensator; (c) Continuously variable series reactor; (d) Static synchronous series compensator (SSSC).

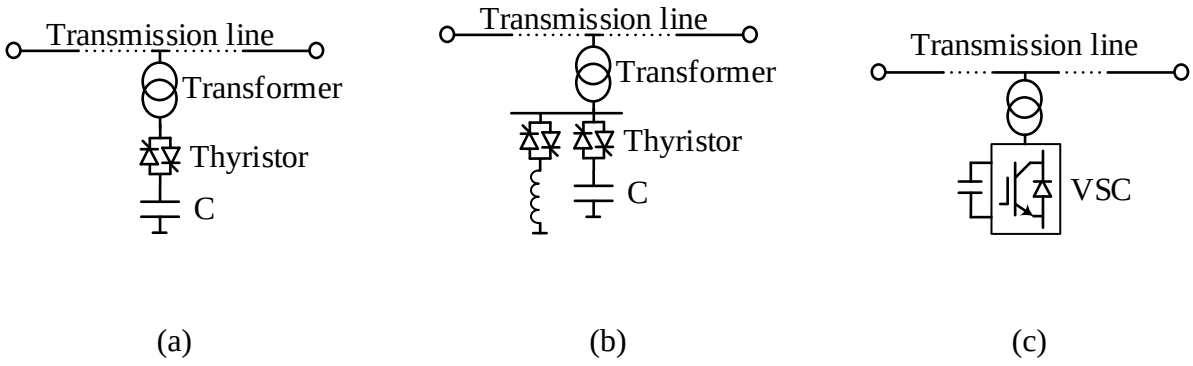


Figure 2-10. Transmission line parallel compensation devices: (a) Thyristor switched capacitor parallel compensator; (b) Thyristor controlled parallel compensator; (c) Static synchronous compensator (STATCOM).

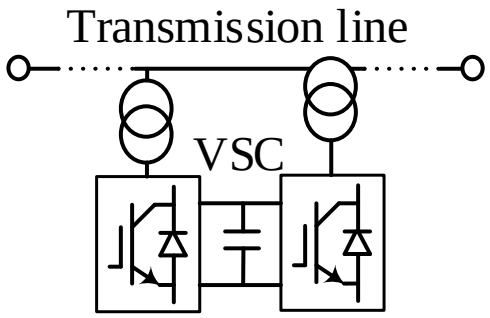
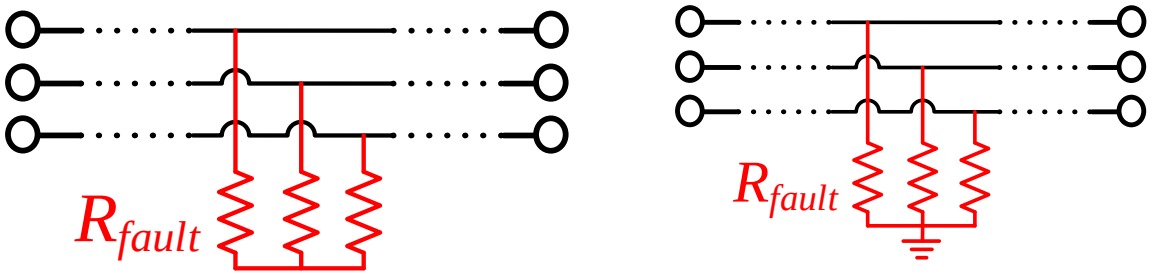
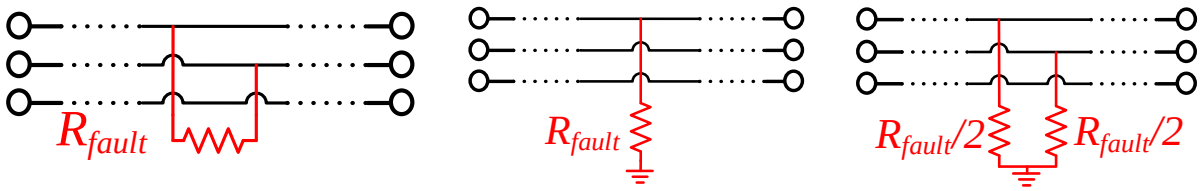


Figure 2-11. Unified power flow controller (UPFC).



(a) (b)

Figure 2-12. Transmission line balanced faults: (a) Three-phase fault; (b) Three-phase-to-ground fault.



(a) (b) (c)

Figure 2-13. Transmission line unbalanced faults: (a) Line-to-line fault; (b) Line-to-ground fault; (c) Line-to-line-to-ground fault.

2.1.4 Transmission Line Emulation Schemes

In 1929, MIT and GE proposed and demonstrated an ac network analyzer by using down-scaled resistors, inductors, and capacitors to represent transmission lines and loads, and emulated synchronous generators with phase-shifting transformers [9], [10]. Nowadays, most power system emulation platforms still rely on physical inductors, capacitors, and resistors to build up lumped RL, Π, and T models for transmission line emulation. In [11], a scaled power system laboratory setup was utilized for EMS testing and validation, where a 4-wire transmission line model was built with inductors, capacitors, and resistors. Power system simulator products with physical inductors, capacitors, and resistors emulating transmission lines are available from a company named TERCO [12]. There are several disadvantages of the transmission line emulation with physical inductors, capacitors, and resistors, including high costs and limited line parameters or reconfiguration capabilities. Also, different types of scaled transmission line compensation devices need to be installed separately for ac system studies with FACTS. Not only the device installations need additional cost and space, but also the utilization flexibility would be limited by the type and parameters of the installed compensation devices. By using several sections of inductors, capacitors and resistors in series to emulate a transmission line, circuit breakers can be implemented at the common point between two sections to emulate a short-circuit fault [13], [14]. However, similar to the other elements in a traditional analog emulation platform, the disadvantages of high cost and less flexibility still exist, and the fault can only happen at several discrete locations, depending on the number of sections. A cost-effective and user-friendly way would be integrating different types of transmission line models, compensation devices, and fault emulation capabilities into one emulator.

In the HTB, a transmission line emulator based on two three-phase VSCs has been

developed to improve the flexibility of changing the emulated line impedance [15]. But only the normal operation and manual line trip open functions with a RL model were implemented [16]. To extend the capabilities of the transmission line emulator, algorithms need to be developed to solve the above-mentioned transmission line models with or without integrated compensation devices under normal or fault conditions.

2.2 Power System Hybrid Emulation

Since the 1990s, with the development of real-time digital simulators, such as real-time-digital-simulator (RTDS), Opal-RT, and the Typhoon HIL, the hybrid simulation environment, which combines a digital simulation and a hardware testing through the hardware-in-the-loop (HIL) technology, has become a new trend for power system studies[17], [18]. With this technology, the simulation capability and flexibility can be improved and also physical devices can get involved in the testing. Except for testing controllers, such as protection relays, generator excitation controllers, and power converter controllers, by using the control HIL technology, the power level facilities can also be tested by using power amplifiers as the interfaces, which is named as power HIL [19]. Power HIL has been used to test different devices, such as photovoltaic inverters and wind generators [20], [21]. A 60 kVA air coil superconducting fault current limiter was evaluated with power HIL technologies in [22]. As one of the critical devices in the power HIL platform, the power amplifier has been developed to be high power and high bandwidth [23], [24]. A multi-physics test-bed with thermal, hydraulic, communication and electrical interfaces was built to test a home energy system in [25]. Reference [26] implements a differential boost converter as the power HIL amplifier to extend the ac output voltage capability. Instead of power system level testing and study, these platforms focus on testing only one device or a small system of no more than a microgrid with a few buses and lines [27]-[29].

For power HIL platforms, the hybrid emulation is stable when the impedance relationship between the digital side and the hardware side fulfills certain conditions [30]-[33]. Tradeoffs need to be considered among the interface stability, bandwidth and accuracy [34]-[38]. As a new type of power system emulation platform, the HTB is full of power electronics switching harmonic components [16]. Appropriate schemes need to be implemented to deal with the potential interface stability and accuracy issues caused by the time delays of filters within the voltage and current measurement loops. Usually, typical power grids with ring or meshed topologies need at least two interfaces to separate them into two subsystems for hybrid emulations. The hybrid emulation stability with two interfaces has not been previously investigated in the literatures.

2.3 MMC Test-bed and Pre-charge Method

2.3.1 MMC Test-bed

A modular multilevel converter (MMC) consists of two arms in each phase, and each arm is built up with submodules (SMs) in series, which are bridge circuits formed by power electronics switches and dc capacitors. Figure 2-14 shows a typical three-phase MMC structure with *N* SMs in each arm. Because of its simplicity and cost effectiveness, the half-bridge SM topology has been widely used in MMC-based HVDC projects, as shown in Figure 2-15(a). However, the half-bridge SM cannot block the dc fault current since it flows through the antiparallel diode of the bottom device T_2. The large and fast rising dc fault current obstructs the application of VSC-based HVDC transmission, especially the most promising multi-terminal direct current (MTDC) system [39]-[41]. Several SM topologies have been proposed that have dc fault current blocking capability, including the full-bridge SM, clamp double SM, cross connected SM, etc. [42]-[45].

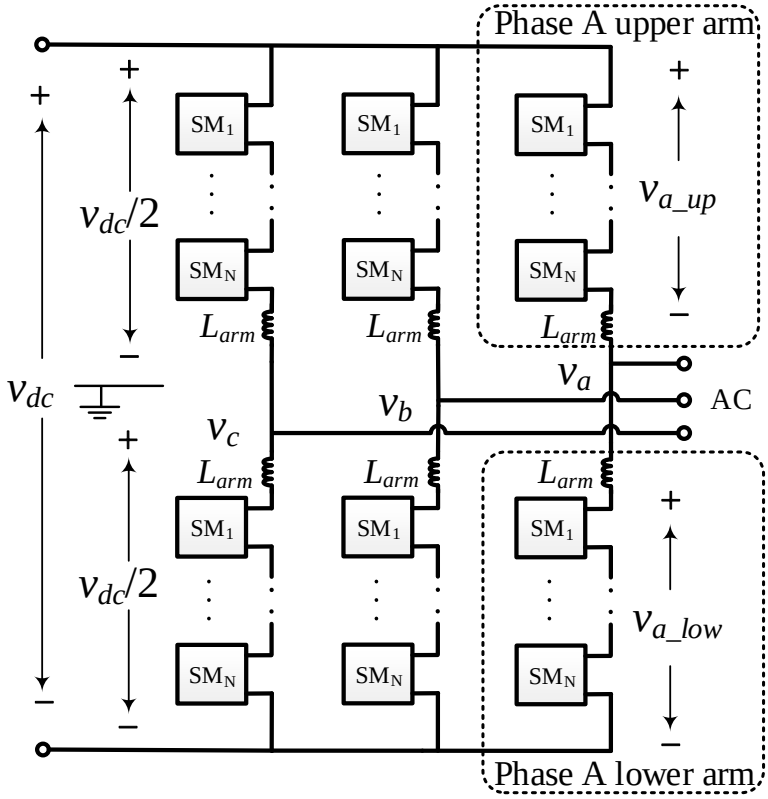


Figure 2-14. MMC basic structure.

(a) (b)

Figure 2-15. MMC SM structure: (a) Half-bridge; (b) Full-bridge.

Figure 2-15(b) shows the full-bridge SM topology, in which the dc fault current is blocked by the SM dc capacitor. Except for that, the full-bridge SM provides other benefits of modulation capability and flexibility since it can output a negative voltage at the SM ac terminal by turning on T_2, T_3 and flexibly select the zero state by either turning on T_1, T_3 or T_2, T_4 [46]. These benefits provide potential ways to further improve the performances and reduce the size of the MMC, such as balancing the SM switch losses, reducing the SM dc voltage ripple, improving the SM dc voltage balancing control, suppressing the circulating current, etc. Recently, a hybrid MMC topology with both half-bridge and full-bridge SMs in one MMC is proposed to block the dc fault current with less switches than the MMC with pure full-bridge SMs [43], [44]. With the development of wide-bandgap devices, researchers have started to investigate the SiC MOSFET application in MMCs considering the benefits of high voltage, high switching frequency, and low conduction loss [47]. However, most of the MMC studies are still limited to digital simulations or rely on hardware demonstrations with a specific setup and limited number of SMs [48]-[54].

2.3.2 MMC Pre-charge Methods

Each phase of a MMC is constructed by multiple series connected SMs, whose dc link capacitor voltages are zero before normal operations. The SM dc link capacitors need to be pre-charged to the rated value to avoid the large inrush current by directly applying the ac or dc voltages on the ac or dc input terminal and be prepared for the MMC normal operation. Four categories of methods have been proposed to pre-charge the SM capacitors in MMCs [55], [56]. The four categories are (1) charging by a separate charging circuit for each SM, (2) charging by the grid-tied ac source, (3) charging by the dc source from the connected dc grid, and (4) charging by an auxiliary dc supply connected on dc side [55], [56].

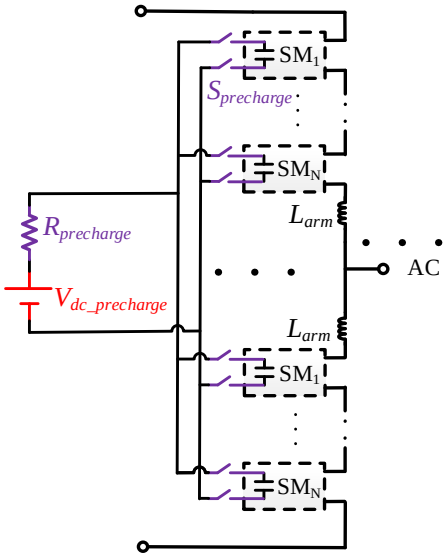


Figure 2-16. MMC pre-charge by a separate charging circuit for each SM.

- MMC pre-charge by a separate charging circuit for each SM [57]

Each MMC SM capacitor can be connected to an auxiliary dc supply and a pre-charge resistor $R_{precharge}$ through separate pre-charge switches $S_{precharge}$ in sequence, as shown in Figure 2-16. The auxiliary dc supply voltage needs to be the same as the MMC SM dc link voltage, which can be a high voltage in HVDC applications. At the same time, several pre-charge switches need to be installed, which increases the cost and complexity.

- Grid-tied MMC pre-charge by the ac grid

A grid-tied MMC SM capacitor can be pre-charged by the ac grid, as shown in Figure 2-17. To avoid large inrush current, the pre-charge resistors $R_{precharge}$ and bypass breakers $BK_{precharge}$ are implemented. The pre-charge resistors $R_{precharge}$ and bypass breakers $BK_{precharge}$ can locate either on ac side in series with the ac grid, as shown in Figure 2-17(a) [58]-[63], or in MMC

arms, as shown in Figure 2-17(b) [64]. Locating the pre-charge resistors and bypass breakers in MMC arms needs more devices but can provide the additional capability of pre-charging from the dc side. In HVDC applications, the ac terminal high voltage leads to high voltage pre-charge resistors and breakers, which would be large size and expensive.

- MMC pre-charge by a dc grid [65]-[67]

For a MMC connected to a dc grid, MMC SM capacitors can be pre-charged by the dc grid through the pre-charge resistor $R_{precharge}$ and bypass breaker $BK_{precharge}$, as shown in Figure 2-18. Though the number of pre-charge resistors and breakers is less than that of pre-charging by the ac grid, the dc terminal high voltage still makes the pre-charge resistors and breakers to be large size and expensive.

- MMC pre-charge by an auxiliary dc supply connected to the dc bus

Except for pre-charging from the connected ac or dc grid, the MMC SM capacitors can also be pre-charged by an auxiliary dc supply connected on the dc side, as shown in Figure 2-19. Each SM can be pre-charged by connecting the SM dc capacitor to the dc supply through the pre-charge diode $D_{precharge}$ and pre-charge resistor $R_{precharge}$ in sequence, as shown in Figure 2-19(a) [68], [69]. In this case, the dc supply voltage needs to be the same as the MMC SM dc link rated voltage, which can be relatively high.

Further, the auxiliary dc supply and pre-charge diode $D_{precharge}$ can cooperate with the MMC switches to operate in a boost converter mode to pre-charge the MMC SMs, as shown in Figure 2-19(b) [56]. Under the boost converter mode, the pre-charge resistor $R_{precharge}$ can be avoided and the dc supply voltage can be lower than the SM dc link rated voltage. However, the pre-charge diode $D_{precharge}$ still needs to withstand the dc terminal high voltage, which makes the

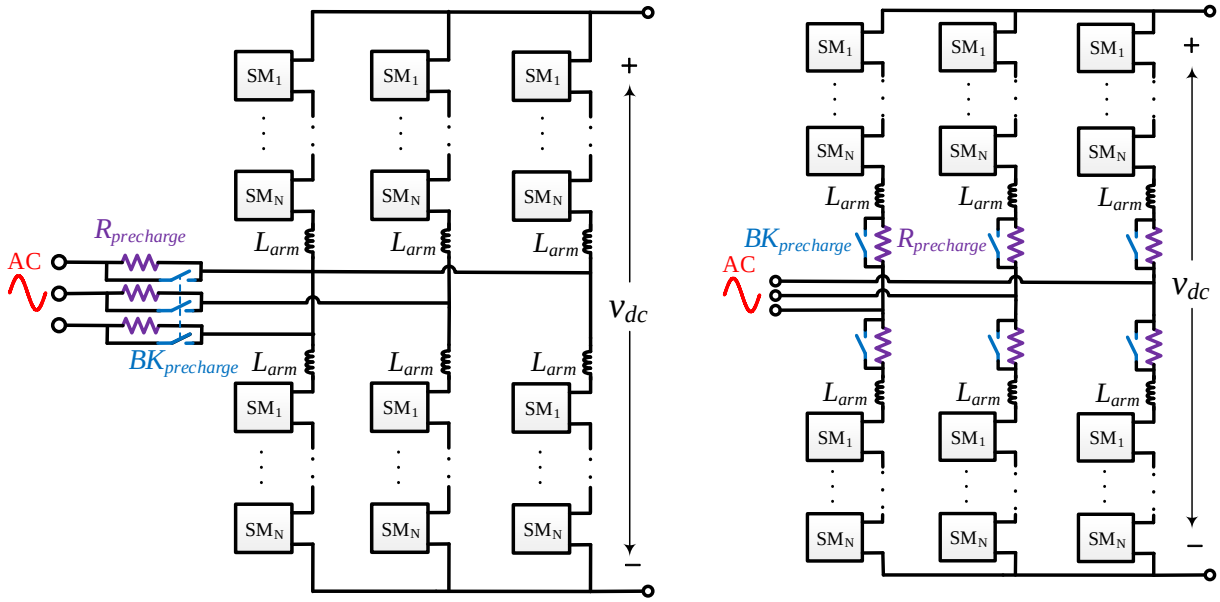


Figure 2-17. Grid-tied MMC pre-charge by the ac grid: (a) Pre-charge resistors and bypass breakers on ac side in series with the ac grid; (b) Pre-charge resistors and bypass breakers in MMC arms.

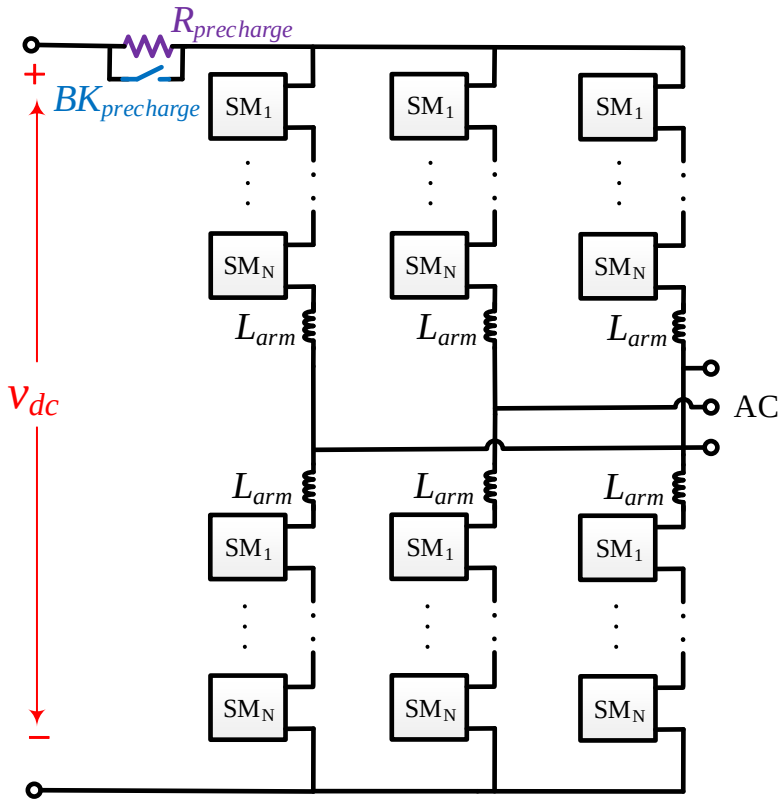


Figure 2-18. Pre-charge resistor $R_{precharge}$ and bypass breaker $BK_{precharge}$ are implemented on the dc side to avoid the large inrush current.

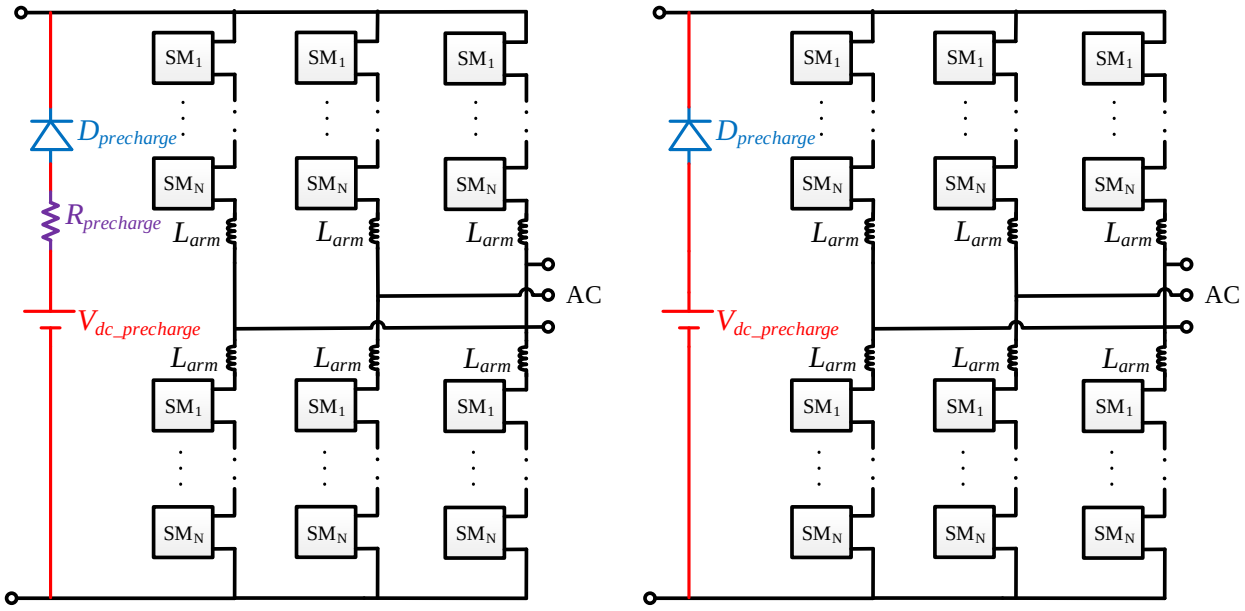


Figure 2-19. MMC pre-charge by an auxiliary dc supply connected on the dc bus: (a) Pre-charge by connecting the dc supply to each SM capacitor through MMC switches in sequence with dc supply voltage equals to the SM rated voltage; (b) Pre-charge by operating as a boost converter with the dc supply voltage lower than the SM rated voltage.

diode a large size and expensive.

All of the above pre-charge methods requires at least one high voltage device for pre-charging the MMC, which makes them expensive and large sizes. It would be beneficial if a pre-charge method can totally avoid high voltage devices by fully utilizing the existing MMC devices.

2.4 Hybrid Ac/dc Transmission

To meet the increasing requirement of electric power delivery, new transmission lines can be built or the power transfer capability of existing transmission lines must be improved. Considering the high cost of building new transmission lines and the social barriers to acquiring the new right-of-way, a hybrid ac/dc transmission concept was proposed to allow ac and dc power delivery through the same transmission line [70]-[73]. The hybrid transmission can push the power transfer capability of ac transmission lines closer to their thermal limit [74]. The concept and several feasible system topologies of hybrid ac/dc transmission have been verified by simulation [75]-[78]. The cost benefit and power delivery improvement of the hybrid ac/dc transmission have been analyzed and evaluated in [78]. In [79], it was mentioned that the zig-zag transformer could be saturated if the three-phase transmission line resistances are unbalanced. A line impedance conditioner based on single-phase converters was proposed to balance the dc currents among the three phases [79]. However, only the influence of the superimposed dc component on the ac system was considered, but not the influence of ac system on HVDC. For HVDC transmission paralleled with ac transmission, a fundamental frequency (60 Hz) current on the dc side of the HVDC converter, referred to as i_{60} with a root mean square (RMS) value I_{60} in this thesis, can be generated due to the coupling effect, and it may lead to potential converter transformer saturation [80]. Considering the ac and dc share the same transmission lines, the

hybrid ac/dc transmission may have worse converter transformer saturation problem, which needs to be fully investigated.

2.5 Dc Fault Impact on Ac System Stability

The fault current characteristics and VSC-HVDC converter performances under dc fault have been investigated in [81], [82]. In [83], a general VSC model was developed for the system stability studies of the power system with the MTDC. Derived from the phasor modeling approach, the model can be used for electromechanical studies, in which the electromagnetic transient process can be neglected. In [84], the interaction between the MTDC and the connected multi-machine ac system was studied. However, the main focus was on the verification of a developed MTDC model for stability analysis. In [85], the system transient stability mechanism based on unbalanced energy theory was discussed. The algorithm was derived by considering directly blocking the HVDC station under the point-to-point HVDC transmission condition. In [86], the ac system transient stability characteristics under dc fault with three different modular multi-level converter (MMC) configurations were discussed. The analysis was based on a point-to-point HVDC overlay transmission. In [87], a four-terminal HVDC system was built to evaluate the impacts of a permanent dc fault on the hybrid ac-dc system. The dc circuit breaker was verified to improve the system stability. However, the study focused only on the active power and dc voltage transient of the HVDC converter under dc fault conditions.

Though short-circuit faults have been claimed to be more detrimental to dc grids than ac grids, the differences between dc and ac grids under fault conditions and their fault impacts on the system stability have not been thoroughly investigated, especially for the MTDC system. Different dc fault protection strategies have not been evaluated by considering the ac system transient stability.

2.6 Research Objectives

Based on the above survey, many algorithms need to be proposed to realize the power electronics converter interfaced power system emulation platforms for extending the HTB capabilities. To realize the development of the emulation platforms, some known or potential issues need to be solved.

The main challenges for transmission line emulator include:

(1) Algorithms and realization of emulating different transmission line models, transmission lines with integrated compensation devices, and transmission lines under fault conditions.

(2) Smooth switching between transmission line normal state and fault state.

(3) Transmission line emulation interface time-delay.

(4) Power converter control under unbalanced faults.

The main challenges for hybrid emulation with the HTB and RTDS include:

(1) Hybrid emulation interface algorithm with high accuracy and stability.

(2) Hybrid emulation interface time-delay correction.

(3) Hybrid emulation stability with two interfaces.

The main challenges for MMC test-bed include:

(1) Flexibility for reconfiguring MMC topology, and modifying passive component values and switching frequency.

(2) Easy to reprogram different control functions and test.

(3) A cost-effective and universal MMC pre-charge method.

The main challenges for hybrid ac/dc transmission and dc fault impact on ac system stability include:

(1) In a hybrid ac/dc transmission system, the impact of ac transmission on HVDC has not been investigated.

(2) For MTDC systems, the dc fault impact on interconnected ac system stability is not clear.

Corresponding to the challenges listed above, the main tasks of this proposal are as follows.

The main tasks for transmission line emulator include:

(1) Propose algorithms to emulate different transmission line models, transmission lines with integrated compensation devices, and transmission lines under fault conditions, and develop the transmission line emulator based on the proposed algorithms.

(2) Propose a method to smoothly switch between transmission line normal state and fault state, and implement it into the transmission line emulator.

(3) Develop an algorithm to compensate the time-delay within the transmission line emulator.

(4) Build up a power converter with unbalanced current tracking capability.

The main tasks for hybrid emulation with the HTB and RTDS include:

(1) Develop a hybrid emulation interface algorithm with high accuracy and stability.

(2) Propose a method to correct the hybrid emulation interface time-delay.

(3) Analyze the hybrid emulation stability with two interfaces.

The main tasks for MMC test-bed include:

(1) Develop a MMC test-bed with the capability of changing topology, passive component value, and switching frequency easily.

(2) Utilize the MMC test-bed to conduct research demonstrations.

(3) Propose and implement a cost-effective and universal MMC pre-charge method.

The main tasks for hybrid ac/dc transmission and dc fault impact on ac system stability include:

(1) Investigate the ac transmission system impact on the HVDC operation and propose corresponding methods to solve the potential issues.

(2) Analyze the differences between a dc fault and an ac fault and evaluate the impact of a dc fault on interconnected ac system stability by implementing different dc fault protection schemes and comparing with an equivalent ac fault.

3 Transmission Line Normal State Emulation

In this chapter, the basic concept and theory of transmission line emulation based on power converters are investigated. The characteristics of different transmission line models are analyzed and corresponding algorithms are proposed to solve the models under the emulation environment. According to this analysis, most transmission line compensation devices can be represented by variable capacitors or inductors connected into transmission lines in series or parallel. Transmission line emulation models with integrated variable capacitors and inductors are developed to emulate transmission lines with compensation devices together. Through Y/Δ transformation, the transmission line model with integrated variable inductors in parallel is developed to avoid the stability issue caused by directly calculating the variable inductor voltages. By analyzing the characteristics of transmission line traveling wave models, a scaling method and an algorithm are proposed to realize the transmission line emulation based on traveling wave models.

3.1 Power Converter Based Transmission Line Emulation Concept

Similar to power HIL concept, the transmission line emulator solves the terminal current references based on the measured terminal voltages and the transmission line model in a digital signal processor and then controls the interface power converters to track the calculated current references. Figure 3-1 shows the basic concept of transmission line emulation with power converters.

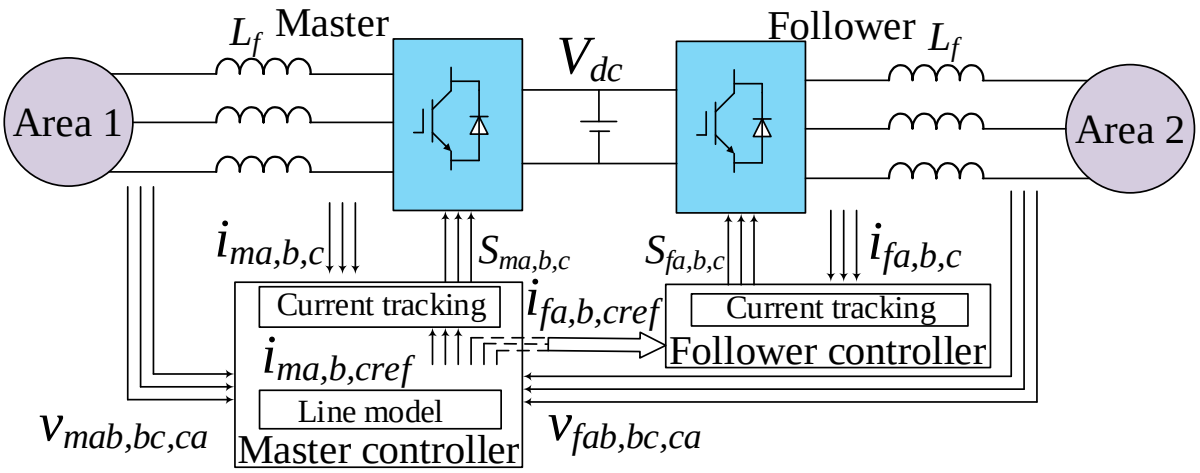
Figure 3-1(a) is the hardware and control structure. Two converters share the dc bus, which are named as Master and Follower, respectively. The inductors with L_f inductance serve as the

converter filters. Both Master and Follower VSCs have their own controllers for current tracking control. Area 1 and Area 2 represent two power system networks, which are connected by the emulated transmission line. The transmission line model, which calculates the current references according to the terminal voltages, is located in the Master controller. The Follower side current references are calculated in the Master controller and sent to the Follower controller through dedicated serial communication.

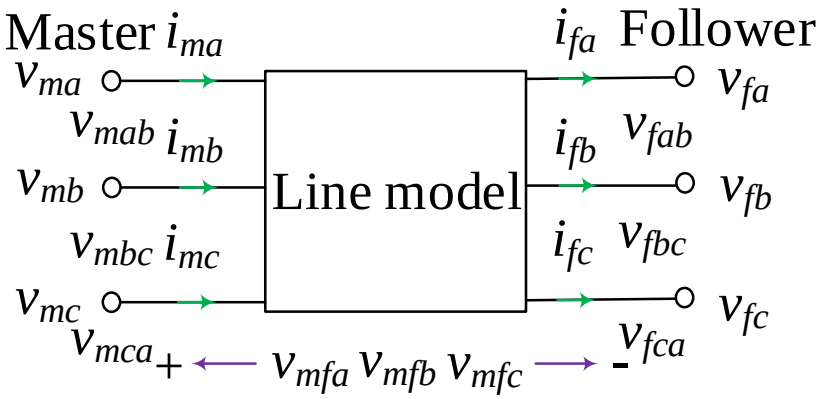
Figure 3-1(b) shows a general three-phase transmission line model, where the two terminals of the transmission line are named as Master and Follower, respectively, corresponding to the emulator structure in Figure 3-1(a). The transmission line inductance and resistance are L and R, respectively. The Master side phase A, B and C to neutral voltages are named as v_{ma}, v_{mb} and v_{mc}, respectively. The Follower side phase A, B and C to neutral voltages are named as v_{fa}, v_{fb} and v_{fc}, respectively.

The Master side phase A to B, phase B to C and phase C to A voltages are named as v_{mab}, v_{mbc} and v_{mca}, respectively. The Follower side phase A to B, phase B to C and phase C to A voltages are named as v_{fab}, v_{fbc} and v_{fca}, respectively.

The Master side phase A, B and C currents are named as i_{ma}, i_{mb} and i_{mc}, respectively, with the corresponding current references i_{maref}, i_{mbref} and i_{mcref} from the transmission line model. The Follower side phase A, B and C currents are named as i_{fa}, i_{fb} and i_{fc}, respectively, with the corresponding current references i_{faref}, i_{fbref} and i_{fcref} from the transmission line model. The phase A, B and C voltages across the transmission line are named as v_{mfa}, v_{mfb} and v_{mfc}, respectively. The voltage and current positive directions are defined in Figure 3-1(b). The voltages and currents in all transmission line emulation cases follow the definitions in Figure 3-1.



(a)



(b)

Figure 3-1. Power converter-based transmission line emulator: (a) Hardware and control structure; (b) A general three-phase transmission line model.

3.2 Transmission Line Emulation with Lumped Models

3.2.1 Transmission Line RL Model and Π model

Figure 3-2 shows the three-phase transmission line RL model, where phase A, B and C currents flowing through the transmission line under normal conditions are named as i_a, i_b and i_c, respectively.

In time domain, the transmission line is expressed as (3-1).

$$v_{mfx} = v_{mx} - v_{fx} = L\frac{di_x}{dt} + Ri_x \ (x = a, b, c) \tag{3-1}$$

By measuring the terminal voltages, the current references can be derived from (3-2).

$$i_{mxref} = i_{fxref} = i_{xref} = \int \frac{v_{mx} - v_{fx} - Ri_x}{L} dt \tag{3-2}$$

Thus, the transmission line RL model emulation algorithm is derived as shown in Figure 3-3.

For the transmission line Π model, the parallel capacitors at both ends can be integrated into the generator or load emulators connected on the same bus. Thus, transmission line RL model emulation can be utilized to emulate the Π model.

3.2.2 Transmission Line T Model

Figure 3-4 shows the three-phase transmission line T model, where phase A, B and C currents flowing into the capacitors are named as i_{Ca}, i_{Cb} and i_{Cc}, respectively and phase A, B and C voltages across the capacitors are named as v_{Ca}, v_{Cb} and v_{Cc}, respectively.

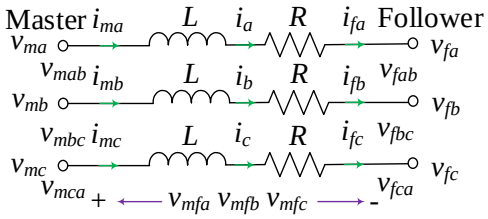


Figure 3-2. Three-phase transmission line RL model.

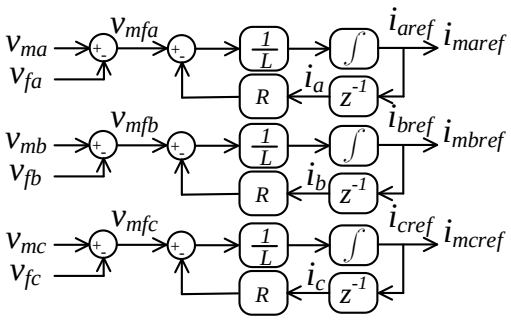


Figure 3-3. Transmission line RL model emulation algorithm.

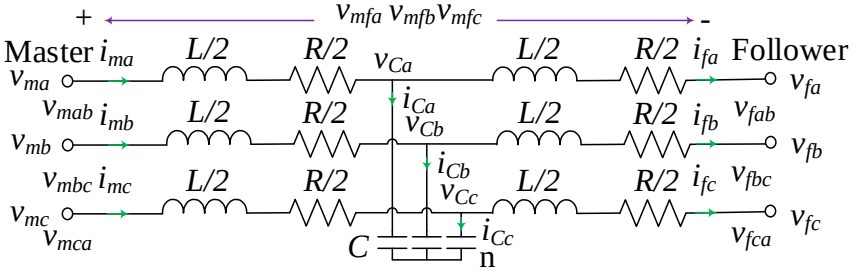


Figure 3-4. Three-phase transmission line T model.

In time domain, the transmission line is expressed as (3-3).

$$\begin{cases} v_{mx} - v_{Cx} = 0.5L\dfrac{di_{mx}}{dt} + 0.5Ri_{mx} \\ v_{Cx} - v_{fx} = 0.5L\dfrac{di_{fx}}{dt} + 0.5Ri_{fx} \quad (x = a, b, c) \\ v_{Cx} = \int \dfrac{i_{Cx}}{C}dt \\ i_{Cx} = i_{mx} - i_{fx} \end{cases} \tag{3-3}$$

By measuring the terminal voltages, the current references can be derived from (3-4).

$$\begin{cases} i_{mxref} = \int \dfrac{v_{mx} - \int \frac{i_{mx} - i_{fx}}{C}dt - 0.5Ri_{mx}}{0.5L}dt \\ i_{fxref} = \int \dfrac{\int \frac{i_{mx} - i_{fx}}{C}dt - v_{fx} - 0.5Ri_{fx}}{0.5L}dt \end{cases} \tag{3-4}$$

Thus, the transmission line T model emulation algorithm is derived as shown in Figure 3-5.

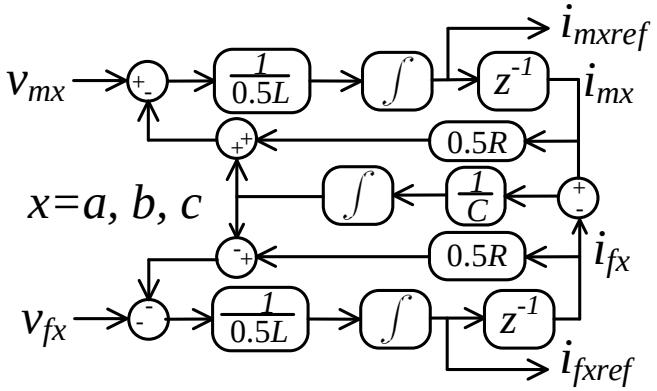


Figure 3-5. Transmission line T model emulation algorithm.

3.3 Transmission Line Emulation with Compensation Devices

According to the discussion in section 2.1.2, the transmission line compensation devices usually operate as variable reactance to either compensate the line impedance in series or inject reactive power in parallel. Thus, the transmission line compensation device functions can be represented by adding variable capacitors or inductor in series or parallel into the transmission line model.

3.3.1 Series Compensation Device Emulation

- Series compensation capacitor

Figure 3-6 shows the three-phase transmission line RL model with variable capacitors representing the series compensation devices working in the capacitive region. The capacitor voltages in phase A, B, and C are named as v_{Ca}, v_{Cb} and v_{Cc}, respectively.

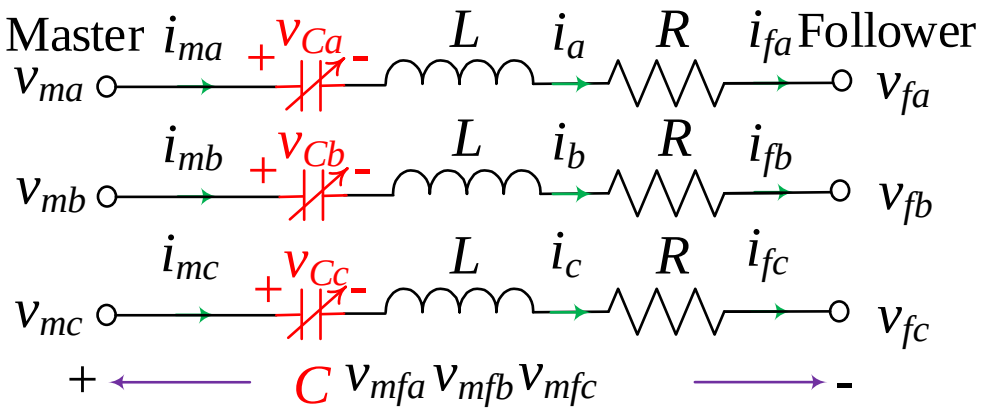


Figure 3-6. Transmission line emulation with series variable capacitors.

In time domain, the transmission line model with series variable capacitors is expressed as (3-5).

$$\begin{cases} v_{mfx} = v_{mx} - v_{fx} = L\dfrac{di_x}{dt} + Ri_x + v_{Cx} \\ v_{Cx} = \int \dfrac{i_x}{C}dt \end{cases} \quad (x = a, b, c) \tag{3-5}$$

By measuring the terminal voltages, the current references can be derived from (3-6).

$$i_{mxref} = i_{fxref} = i_{xref} = \int \frac{v_{mx} - v_{fx} - Ri_x - \int \frac{i_x}{C}dt}{L}dt \tag{3-6}$$

Thus, the emulation algorithm of a transmission line model with series variable compensation capacitors is derived as shown in Figure 3-7.

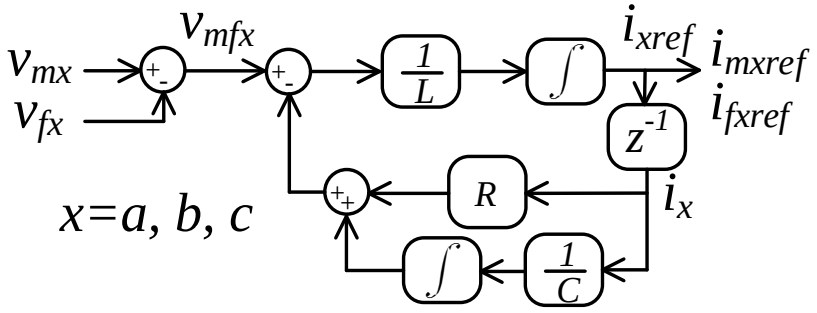


Figure 3-7. Transmission line model with series variable compensation capacitors emulation algorithm.

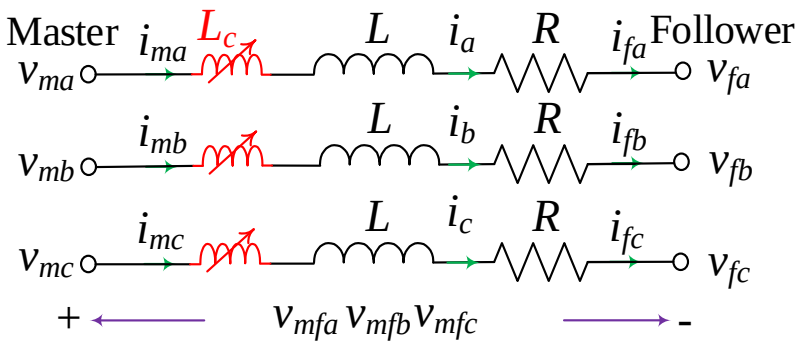


Figure 3-8. Transmission line emulation with series variable inductors.

- Series compensation inductor

Figure 3-8 shows the three-phase transmission line RL model with variable inductors representing the series compensation devices working in the inductive region.

In time domain, the transmission line model with series variable inductors is expressed as (3-7).

$$v_{mfx} = v_{mx} - v_{fx} = L\frac{di_x}{dt} + Ri_x + L_c\frac{di_x}{dt} \quad (x = a, b, c) \tag{3-7}$$

By measuring the terminal voltages, the current references can be derived from (3-8).

$$i_{mxref} = i_{fxref} = i_{xref} = \int \frac{v_{mx} - v_{fx} - Ri_x}{L + L_c}dt \tag{3-8}$$

Thus, the emulation algorithm of a transmission line model with series variable compensation inductors is derived as shown in Figure 3-9.

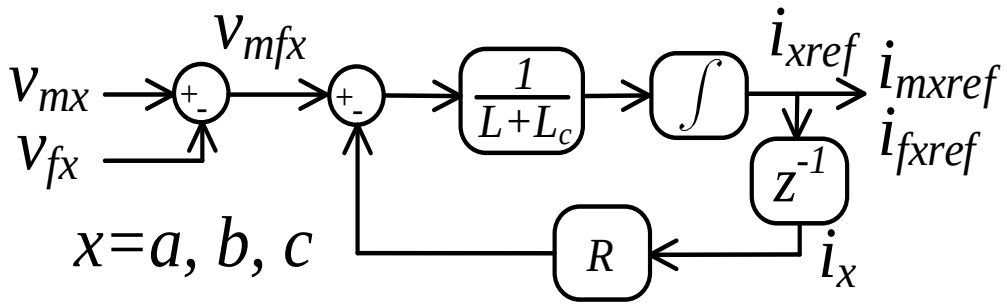


Figure 3-9. Transmission line model with series variable compensation inductors emulation algorithm.

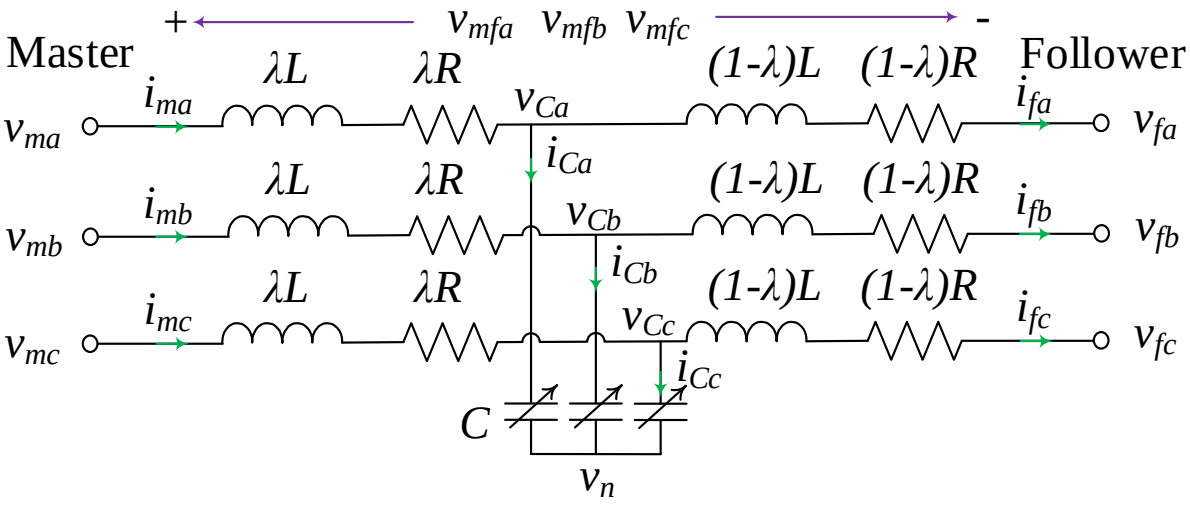


Figure 3-10. Transmission line emulation with parallel variable capacitors.

3.3.2 Parallel Compensation Device Emulation

- Parallel compensation capacitor

Figure 3-10 shows the three-phase transmission line RL model with variable capacitors representing the parallel compensation devices working in the capacitive region, where the parameter λ ($0 < \lambda < 1$) is the percentage of the distance from the compensation device location to the master side terminal with regard to the total line length. The capacitor voltages and currents in phase A, B, and C are named as v_{Ca}, v_{Cb}, v_{Cc}, i_{Ca}, i_{Cb}, and i_{Cc}, respectively.

Since the capacitor common connection point voltage referring to the imaginary neutral point is zero in the balanced three-phase system, the transmission line model with parallel variable capacitors is expressed as (3-9).

$$\begin{cases} v_{mx} - v_{Cx} = \lambda L \dfrac{di_{mx}}{dt} + \lambda R i_{mx} \\ v_{Cx} - v_{fx} = (1-\lambda) L \dfrac{di_{fx}}{dt} + (1-\lambda) R i_{fx} \quad (x = a, b, c) \\ v_{Cx} = \displaystyle\int \frac{i_{Cx}}{C} dt \\ i_{Cx} = i_{mx} - i_{fx} \end{cases} \tag{3-9}$$

By measuring the terminal voltages, the current references can be derived from (3-10).

$$\begin{cases} i_{mxref} = \displaystyle\int \frac{v_{mx} - \int \frac{i_{mx} - i_{fx}}{C} dt - \lambda R i_{mx}}{\lambda L} dt \\ i_{fxref} = \displaystyle\int \frac{\int \frac{i_{mx} - i_{fx}}{C} dt - v_{fx} - (1-\lambda) R i_{fx}}{(1-\lambda) L} dt \end{cases} \tag{3-10}$$

Thus, the emulation algorithm of a transmission line model with parallel variable compensation capacitors is derived as shown in Figure 3-11.

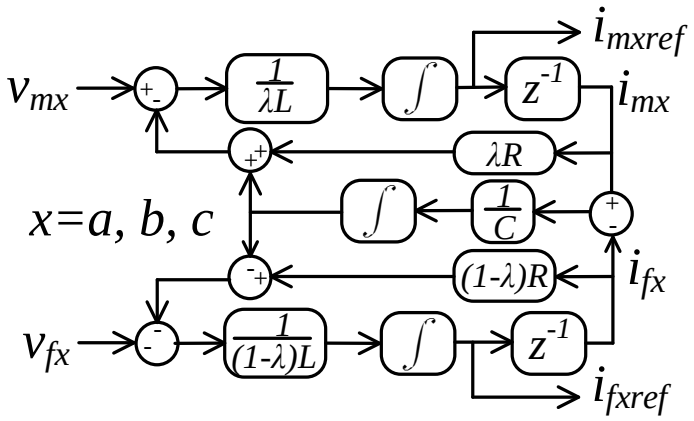


Figure 3-11. Transmission line model with parallel variable compensation capacitors emulation algorithm.

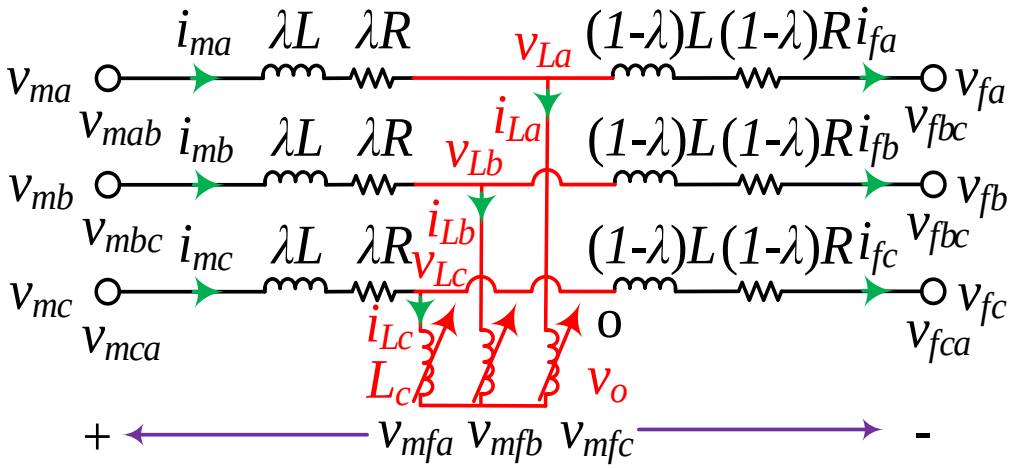


Figure 3-12. Transmission line emulation with parallel variable inductors.

- Parallel compensation inductor

Figure 3-12 shows the three-phase transmission line RL model with variable inductors representing the parallel compensation devices working in the inductive region, where the parameter λ ($0 < \lambda < 1$) is the percentage of the distance from the compensation device location to the master side terminal with regard to the total line length. The inductor voltages in phase A, B, and C are named as v_{La}, v_{Lb} and v_{Lc}, respectively. The inductor currents in phase A, B, and C are named as i_{La}, i_{Lb} and i_{Lc}, respectively.

A straightforward way would be replacing the capacitor voltage in (3-10) to the inductor voltage, as expressed in (3-11). However, the inductor voltage is not a state variable and needs to calculate the current derivation, which is very sensitive to harmonics and errors.

$$\begin{cases} i_{mxref} = \int \dfrac{v_{mx} - L_c \dfrac{d\left(i_{mx} - i_{fx}\right)}{dt} - \lambda R i_{mx}}{\lambda L} dt \\ i_{fxref} = \int \dfrac{L_c \dfrac{d\left(i_{mx} - i_{fx}\right)}{dt} - v_{fx} - (1-\lambda) R i_{fx}}{(1-\lambda) L} dt \end{cases} \tag{3-11}$$

To avoid the inductor voltage calculation by solving the current derivation equation, the Y/Δ transformation is implemented to reshape the transmission line model with parallel variable inductors. Since the inductor common connection point voltage referring to the imaginary neutral point is zero in the balanced three-phase system, the transmission line model can be analyzed by a single-phase circuit. Figure 3-13 shows the Y/Δ transformation of the transmission line model under a single-phase circuit.

Figure 3-13(a) is the Y/Δ transformation in s-domain. According to Y/Δ transformation, the impedances in the Δ connection are expressed in (3-12).

$$\begin{cases} Z_{mf}(s) = \dfrac{\lambda(1-\lambda)Z(s)^2 + \lambda Z(s)Z_c(s) + (1-\lambda)Z(s)Z_c(s)}{Z_c(s)} \\ Z_{mn}(s) = \dfrac{\lambda(1-\lambda)Z(s)^2 + \lambda Z(s)Z_c(s) + (1-\lambda)Z(s)Z_c(s)}{(1-\lambda)Z(s)} \\ Z_{fn}(s) = \dfrac{\lambda(1-\lambda)Z(s)^2 + \lambda Z(s)Z_c(s) + (1-\lambda)Z(s)Z_c(s)}{\lambda Z(s)} \end{cases} \tag{3-12}$$

where the impedances in Y connection are expressed in (3-13).

$$\begin{cases} Z(s) = R + sL \\ Z_c(s) = sL_c \end{cases} \tag{3-13}$$

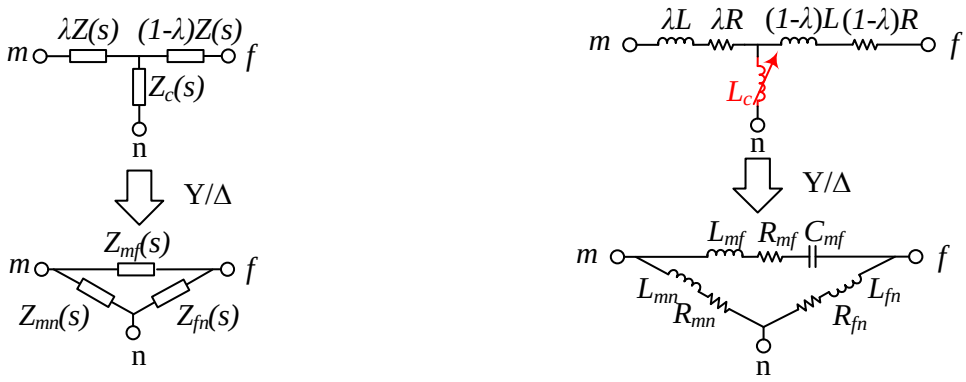
Substitute (3-13) into (3-12), to obtain (3-14).

$$\begin{cases} Z_{mf}(s) = \left(L + \dfrac{\lambda(1-\lambda)L^2}{L_c}\right)s + R + \dfrac{2\lambda(1-\lambda)RL}{L_c} + \dfrac{\lambda(1-\lambda)R^2}{L_c}\dfrac{1}{s} \\ Z_{mn}(s) = \left(\lambda L + \dfrac{L_c}{1-\lambda}\right)s + \lambda R \\ Z_{fn}(s) = \left((1-\lambda)L + \dfrac{L_c}{\lambda}\right)s + (1-\lambda)R \end{cases} \tag{3-14}$$

Based on (3-14), the equivalent R, L, C circuit after the Y/Δ transformation is shown in Figure 3-13(b), where the corresponding element parameters are expressed in (3-15).

$$\begin{cases} L_{mf} = L + \dfrac{\gamma(1-\gamma)L^2}{L_c}, R_{mf} = R + \dfrac{2\gamma(1-\gamma)RL}{L_c}, C_{mf} = \dfrac{\gamma(1-\gamma)R^2}{L_c} \\ L_{mn} = \left(\gamma L + \dfrac{L_c}{1-\gamma}\right), R_{mn} = \gamma R \\ L_{fn} = (1-\gamma)L + \dfrac{L_c}{\gamma}, R_{fn} = (1-\gamma)R \end{cases} \tag{3-15}$$

Thus, the three-phase transmission line model with parallel variable inductors after Y/Δ transformation is shown in Figure 3-14.



(a) (b)

Figure 3-13. Y/Δ transformation of the transmission line model with parallel variable inductors: (a) Circuit diagram in s-domain; (b) Equivalent R, L, C circuit.

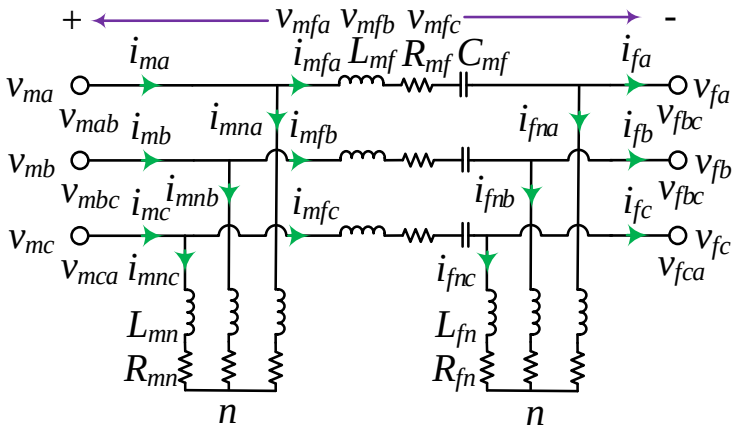


Figure 3-14. Transmission line model with parallel variable compensation inductors after Y/Δ transformation.

In time domain, the model is expressed as (3-16).

$$\begin{cases} v_{mx} = L_{mn}\dfrac{di_{mnx}}{dt} + R_{mn}i_{mnx} \\ v_{mfx} = L_{mf}\dfrac{di_{mfx}}{dt} + R_{mf}i_{mfx} + \displaystyle\int \frac{i_{mfx}}{C_{mf}}dt \\ v_{fx} = L_{fn}\dfrac{di_{fnx}}{dt} + R_{fn}i_{fnx} \\ i_{mx} = i_{mnx} + i_{mfx} \\ i_{fx} = i_{mfx} - i_{fnx} \end{cases} \quad (x = a, b, c) \tag{3-16}$$

By measuring the terminal voltages, the current references can be derived from (3-17) and (3-18).

$$\begin{cases} i_{mfxref} = \displaystyle\int \frac{v_{mfx} - R_{mf}i_{mfx} - \int \frac{i_{mfx}}{C_{mf}}dt}{L_{mf}}dt \\ i_{mnxref} = \displaystyle\int \frac{v_{mx} - R_{mn}i_{mnx}}{L_{mn}}dt \\ i_{mfxref} = \displaystyle\int \frac{v_{mfx} - R_{mf}i_{mfx} - \int \frac{i_{mfx}}{C_{mf}}dt}{L_{mf}}dt \\ i_{fnxref} = \displaystyle\int \frac{v_{fx} - R_{fn}i_{fnx}}{L_{fn}}dt \end{cases} \tag{3-17}$$

$$\begin{cases} i_{mxref} = i_{mnxref} + i_{mfxref} \\ i_{fxref} = i_{mfxref} - i_{fnxref} \end{cases} \tag{3-18}$$

Substitute (3-17) into (3-18), to obtain (3-19).

$$\begin{cases} i_{mxref} = \displaystyle\int \frac{v_{mx} - R_{mn}i_{mnx}}{L_{mn}}dt + \int \frac{v_{mfx} - R_{mf}i_{mfx} - \int \frac{i_{mfx}}{C_{mf}}dt}{L_{mf}}dt \\ i_{fxref} = \displaystyle\int \frac{v_{mfx} - R_{mf}i_{mfx} - \int \frac{i_{mfx}}{C_{mf}}dt}{L_{mf}}dt - \int \frac{v_{fx} - R_{fn}i_{fnx}}{L_{fn}}dt \end{cases} \tag{3-19}$$

Thus, the emulation algorithm of a transmission line model with parallel variable compensation inductors after Y/Δ transformation is derived as shown in Figure 3-15.

3.4 Transmission Line Emulation with Traveling Wave Model

3.4.1 Transmission Line Emulation Based on Traveling Wave Model

According to Figure 2-6, Figure 2-7, (2-1), and (2-2) in the transmission line traveling wave model discussion, the two section transmission line traveling wave model with lumped resistors representing the power losses are expressed in (3-20) corresponding to the diagram in Figure 3-16, where $Z_0 = \sqrt{L/C}$, $\tau = l\sqrt{LC}$, L and C are the inductance and capacitance per unit length, R is the total resistance, and l is the line length.

$$\begin{cases} i_{mhx}(t) = -\dfrac{1}{Z_0} v_{mmx}\left(t - \dfrac{\tau}{2}\right) + i_{mmx}\left(t - \dfrac{\tau}{2}\right) \\ i_{mmhx}(t) = \dfrac{1}{Z_0}\left(v_{mx}\left(t - \dfrac{\tau}{2}\right) - \dfrac{R}{4} i_{mx}\left(t - \dfrac{\tau}{2}\right)\right) + i_{mx}\left(t - \dfrac{\tau}{2}\right) \end{cases} \tag{3-20}$$

The voltage and current relationships of transmission line section 1 and section 2 are expressed in (3-21) and (3-22), respectively.

$$\begin{cases} i_{mhx}(t) = -\dfrac{1}{Z_0} v_{mmx}\left(t - \dfrac{\tau}{2}\right) + i_{mmx}\left(t - \dfrac{\tau}{2}\right) \\ i_{mmhx}(t) = \dfrac{1}{Z_0}\left(v_{mx}\left(t - \dfrac{\tau}{2}\right) - \dfrac{R}{4} i_{mx}\left(t - \dfrac{\tau}{2}\right)\right) + i_{mx}\left(t - \dfrac{\tau}{2}\right) \end{cases} \tag{3-21}$$

$$\begin{cases} i_{fmhx}(t) = -\dfrac{1}{Z_0}\left(v_{fx}\left(t - \dfrac{\tau}{2}\right) + \dfrac{R}{4} i_{fx}\left(t - \dfrac{\tau}{2}\right)\right) + i_{fx}\left(t - \dfrac{\tau}{2}\right) \\ i_{fhx}(t) = \dfrac{1}{Z_0}\left(v_{mmx}\left(t - \dfrac{\tau}{2}\right) - \dfrac{R}{2} i_{mmx}\left(t - \dfrac{\tau}{2}\right)\right) + i_{mmx}\left(t - \dfrac{\tau}{2}\right) \end{cases} \tag{3-22}$$

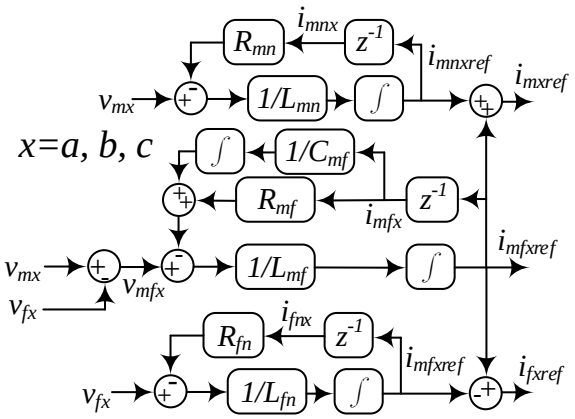


Figure 3-15. Transmission line model with parallel variable compensation inductors after Y/Δ transformation.

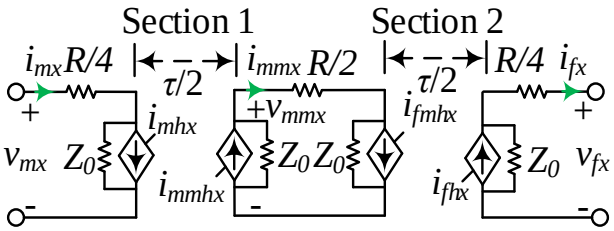


Figure 3-16. Two section transmission line traveling wave model with lumped resistors.

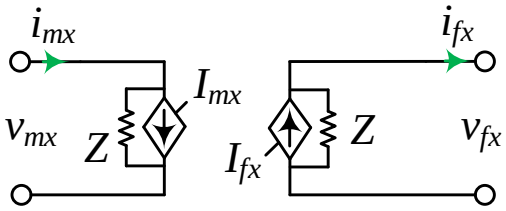


Figure 3-17. Simplified transmission line traveling wave model with lumped resistors.

The circuit between section 1 and section 2 is expressed in (3-23).

$$\begin{cases} i_{mmx}(t) = i_{mmhx}(t) - \dfrac{v_{mmx}(t)}{Z_0} \\ v_{mmx}(t) - \dfrac{R}{2} i_{mmx}(t) = Z_0 \left(i_{mmx}(t) - i_{fmhx}(t) \right) \end{cases} \tag{3-23}$$

Solve (3-23), to obtain (3-24).

$$\begin{cases} v_{mmx}(t) = \dfrac{2{Z_0}^2 + Z_0 R}{4Z_0 + R} i_{mmhx}(t) - \dfrac{2{Z_0}^2}{4Z_0 + R} i_{fmhx}(t) \\ i_{mmx}(t) = \dfrac{2Z_0}{4Z_0 + R} \left(i_{mmhx}(t) + i_{fmhx}(t) \right) \end{cases} \tag{3-24}$$

Substitute (3-21) and (3-22) into (3-24), to obtain (3-25).

$$\begin{cases} v_{mmx}(t) = \dfrac{2Z_0 + R}{4Z_0 + R} v_{mx}\left(t - \dfrac{\tau}{2}\right) + \dfrac{(2Z_0 + R)\left(Z_0 - \dfrac{R}{4}\right)}{4Z_0 + R} i_{mx}\left(t - \dfrac{\tau}{2}\right) + \\ \qquad \dfrac{2Z_0}{4Z_0 + R} v_{fx}\left(t - \dfrac{\tau}{2}\right) - \dfrac{Z_0(4Z_0 - R)}{2(4Z_0 + R)} i_{fx}\left(t - \dfrac{\tau}{2}\right) \\ i_{mmx}(t) = \dfrac{2}{4Z_0 + R} v_{mx}\left(t - \dfrac{\tau}{2}\right) + \dfrac{(4Z_0 - R)}{2(4Z_0 + R)} i_{mx}\left(t - \dfrac{\tau}{2}\right) - \\ \qquad \dfrac{2}{4Z_0 + R} v_{fx}\left(t - \dfrac{\tau}{2}\right) + \dfrac{4Z_0 - R}{2(4Z_0 + R)} i_{fx}\left(t - \dfrac{\tau}{2}\right) \end{cases} \tag{3-25}$$

Substitute (3-25) into (3-21) and (3-22), to obtain (3-26).

According to (3-26), the two terminal currents and voltages are directly related to each other without the variables between section 1 and section 2.

Assume the model in Figure 3-16 can be simplified as in Figure 3-17, then the two terminal voltages should be equivalent, as expressed in (3-27).

$$\begin{cases} i_{mhx}(t) = \dfrac{4Z_0}{4Z_0+R}\left(-\dfrac{1}{Z_0}v_{fx}(t-\tau)+\dfrac{4Z_0-R}{4Z_0}i_{fx}(t-\tau)\right)+ \\ \qquad \dfrac{R}{4Z_0+R}\left(-\dfrac{1}{Z_0}v_{mx}(t-\tau)-\dfrac{4Z_0-R}{4Z_0}i_{mx}(t-\tau)\right) \\ i_{fhx}(t) = \dfrac{4Z_0}{4Z_0+R}\left(\dfrac{1}{Z_0}v_{mx}(t-\tau)+\dfrac{4Z_0-R}{4Z_0}i_{mx}(t-\tau)\right)+ \\ \qquad \dfrac{R}{4Z_0+R}\left(\dfrac{1}{Z_0}v_{fx}(t-\tau)-\dfrac{4Z_0-R}{4Z_0}i_{fx}(t-\tau)\right) \end{cases} \tag{3-26}$$

$$\begin{cases} v_{mx}(t) = Z\big(i_{mx}(t)-I_{mx}(t)\big) = \dfrac{R}{4}i_{mx}(t)+Z_0\big(i_{mx}(t)-i_{mhx}(t)\big) \\ v_{fx}(t) = Z\left(I_{fx}(t)-i_{fx}(t)\right) = Z_0\left(i_{fhx}(t)-i_{fx}(t)\right)-\dfrac{R}{4}i_{fx}(t) \end{cases} \tag{3-27}$$

Solve (3-27), to obtain (3-28).

$$\begin{cases} I_{mx}(t) = \dfrac{Z-(Z_0+\frac{R}{4})}{Z}i_{mx}(t)+\dfrac{Z_0}{Z}i_{mhx}(t) \\ I_{fx}(t) = \dfrac{Z-(Z_0+\frac{R}{4})}{Z}i_{fx}(t)+\dfrac{Z_0}{Z}i_{fhx}(t) \end{cases} \tag{3-28}$$

Substitute (3-26) into (3-28), to obtain (3-29).

$$\begin{cases} I_{mx}(t) = \dfrac{1+H}{2}\left(-\dfrac{1}{Z}v_{fx}(t-\tau)+Hi_{fx}(t-\tau)\right)+\dfrac{1-H}{2}\left(-\dfrac{1}{Z}v_{mx}(t-\tau)-Hi_{mx}(t-\tau)\right) \\ I_{fx}(t) = \dfrac{1+H}{2}\left(\dfrac{1}{Z}v_{mx}(t-\tau)+Hi_{mx}(t-\tau)\right)+\dfrac{1-H}{2}\left(\dfrac{1}{Z}v_{fx}(t-\tau)-Hi_{fx}(t-\tau)\right) \end{cases} \tag{3-29}$$

where Z and H are defined in (3-30). However, the references of terminal currents i_{mx}, i_{fx} instead of controlled current sources I_{mx}, I_{fx} are required for the transmission line emulation.

$$\begin{cases} Z = Z_0 + \dfrac{R}{4} \\ H = \dfrac{Z_0 - \dfrac{R}{4}}{Z_0 + \dfrac{R}{4}} \end{cases} \tag{3-30}$$

By adding up the current flowing through the parallel resistor and the corresponding controlled current source together, the terminal current references for transmission line emulation can be derived in (3-31).

$$\begin{cases} i_{mxref}(t) = \dfrac{1+H}{2}\left(-\dfrac{1}{Z}v_{fx}(t-\tau) + Hi_{fx}(t-\tau)\right) + \\ \quad \dfrac{1-H}{2}\left(-\dfrac{1}{Z}v_{mx}(t-\tau) - Hi_{mx}(t-\tau)\right) + \dfrac{v_{mx}(t)}{Z} \\ i_{fxref}(t) = \dfrac{1+H}{2}\left(\dfrac{1}{Z}v_{mx}(t-\tau) + Hi_{mx}(t-\tau)\right) + \\ \quad \dfrac{1-H}{2}\left(\dfrac{1}{Z}v_{fx}(t-\tau) - Hi_{fx}(t-\tau)\right) - \dfrac{v_{fx}(t)}{Z} \end{cases} \tag{3-31}$$

3.4.2 Scaling Method of Transmission Line Traveling Wave Model

Usually, a high voltage and high power grid is scaled down to an equivalent and relatively low voltage and low power grid to be emulated for system studies. In this thesis, the frequency is not scaled, and there are mainly four variables need to be scaled, including voltage, current, power, and impedance. Define the impedance scaling ratio Z_{ratio} in (3-32).

$$Z_{ratio} = \frac{Z_{original}}{Z_{scaled}} \tag{3-32}$$

where Z_{scaled} is the equivalent impedance in the scaled system corresponding to the impedance $Z_{original}$ in the original system. Thus, the inductance scaling ratio L_{ratio}, capacitance scaling ratio

C_{ratio}, and resistance scaling ration R_{ratio} can be derived as in (3-33).

$$\begin{cases} L_{ratio} = \dfrac{L_{original}}{L_{scaled}} = \dfrac{Z_{original}/w}{Z_{scaled}/w} = Z_{ratio} \\ C_{ratio} = \dfrac{C_{original}}{C_{scaled}} = \dfrac{1/wZ_{original}}{1/wZ_{scaled}} = \dfrac{1}{Z_{ratio}} \\ R_{ratio} = \dfrac{R_{original}}{R_{scaled}} = Z_{ratio} \end{cases} \tag{3-33}$$

where L_{scaled} and C_{scaled} are the equivalent inductance and capacitance in the scaled system corresponding to the inductance $L_{original}$ and capacitance $C_{original}$ in the original system, respectively. Since the transmission line traveling wave model is derived from the distributed inductance and capacitance model, the scaled transmission line traveling wave model is determined by the scaled distributed inductance and capacitance. The scaled traveling wave model characteristic impedance $Z_{0scaled}$ and time constant τ_{scaled} are expressed in (3-34).

$$\begin{cases} Z_{0scaled} = \sqrt{\dfrac{L_{scaled}}{C_{scaled}}} = \dfrac{1}{Z_{ratio}}\sqrt{\dfrac{L_{original}}{C_{original}}} = \dfrac{Z_{0original}}{Z_{ratio}} \\ \tau_{scaled} = l\sqrt{L_{scaled}C_{scaled}} = l\sqrt{L_{original}C_{original}} = \tau_{original} \end{cases} \tag{3-34}$$

where $Z_{0scaled}$ and τ_{scaled} are the equivalent characteristic impedance and time constant in the scaled system corresponding to the characteristic impedance $Z_{0original}$ and time constant $\tau_{original}$ in the original system, respectively.

Substitute (3-34) into (3-30), to obtain (3-35). According to (3-34) and (3-35), the transmission line Norton interface impedance Z is scaled based on the impedance ratio, while the travel time τ and coefficient H keep the same as the original system.

$$\begin{cases} Z_{scaled} = Z_{0scaled} + \dfrac{R_{scaled}}{4} = \dfrac{Z_{0original}}{Z_{ratio}} + \dfrac{R_{original}}{4Z_{ratio}} = \dfrac{Z_{original}}{Z_{ratio}} \\ H_{scaled} = \dfrac{Z_{0scaled} - \dfrac{R_{scaled}}{4}}{Z_{0scaled} + \dfrac{R_{scaled}}{4}} = \dfrac{\dfrac{Z_{0original}}{Z_{ratio}} - \dfrac{R_{original}}{4Z_{ratio}}}{\dfrac{Z_{0original}}{Z_{ratio}} + \dfrac{R_{original}}{4Z_{ratio}}} = H_{original} \end{cases} \quad (3\text{-}35)$$

3.5 Simulation and Experiment Results

By highlighting a transmission line emulator in Figure 1-1, the system configuration of the HTB grid emulator is shown in Figure 3-18. The transmission line emulator is composed of two VSCs, which are named as Master and Follower, respectively, in this dissertation. The Master and Follower VSCs also share the same dc link with the other HTB emulator VSCs so that the power loss of Master and Follower VSCs does not affect the power loss performance of emulated transmission line. Figure 3-19 shows the HTB grid emulation platform. The VSC parameters are listed in Table 1.

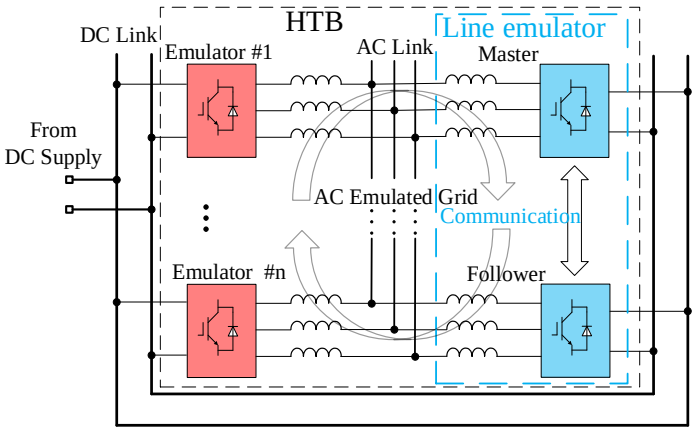


Figure 3-18. System configuration of HTB with a transmission line emulator.

Figure 3-19. HTB grid emulation platform.

Table 1. Parameters of the VSC

Parameters	**Values**
Filter inductance L_f	0.575 mH
Dc-link voltage V_{dc}	200 V
Switching frequency f_s	10 kHz

A simplified two area system is selected to verify the transmission line emulation under normal conditions, as shown in Figure 3-20. The transmission line is connected to two voltage sources with the line-to-line voltage RMS value V_{LL} = 43 V: (1) an ideal voltage source V_1 with the source impedance L_1 = 5.97 mH, R_1 = 0.65 Ω and (2) an ideal voltage source V_2 with the source impedance L_2 = 2.4 mH, R_2 = 0.07 Ω, respectively.

Both the simulation and experiment are conducted to verify the proposed transmission line model with compensation devices. Figure 3-21 is the simulation verification setup in MATLAB/SIMULINK environment by representing the transmission line with controlled current sources, whose current references come from the transmission line model. Figure 3-22 and Figure 3-23 are the experimental verification setup and hardware platform, respectively, and the two VSCs, named as VSC1 and VSC2, are controlled to function as the voltage source V_1 and V_2, respectively. The pure MATLAB/SIMULINK digital simulation with the system in Figure 3-20 is conducted to be the original simulation for comparison verification.

3.5.1 Transmission Line Emulation with Lumped Models

- RL model

A system diagram with two identical transmission lines, named as Line 1 and Line 2, is built to verify the transmission line RL model, as shown in Figure 3-24. The transmission line parameters are L = 5 mH and R = 0.5 Ω. Line 2 is connected in parallel with Line 1 through the switches S_1 and S_2 at 0.1 s when the phase angle of V_{1ab} is 218°. The angle difference between the two voltage sources is $\theta = \theta_{V1} - \theta_{V2}$ = 225°. Figure 3-25(a) and Figure 3-25(b) show I_a and I_b comparisons, respectively, of the experimental and the original simulation results. The results indicate that the experimental waveforms match with the original simulation results.

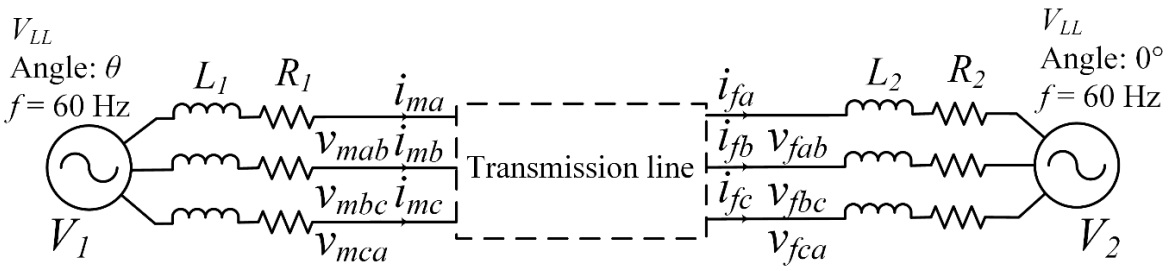


Figure 3-20. Original transmission line simulation for transmission line emulation verification.

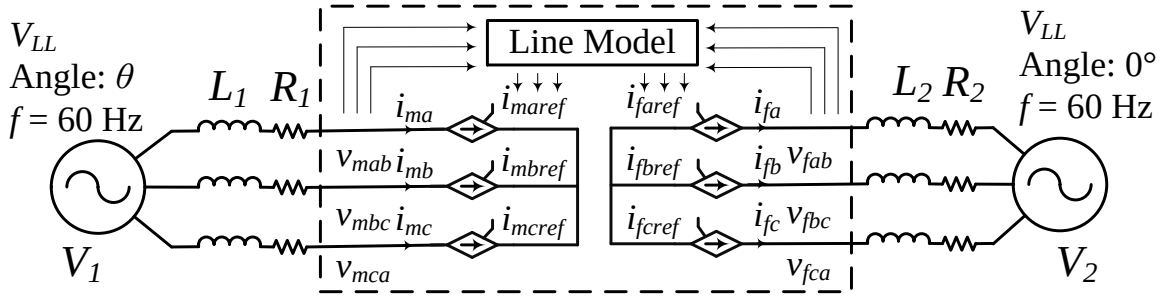


Figure 3-21. Transmission line model simulated in MATLAB/SIMULINK with controlled current sources for transmission line emulation verification.

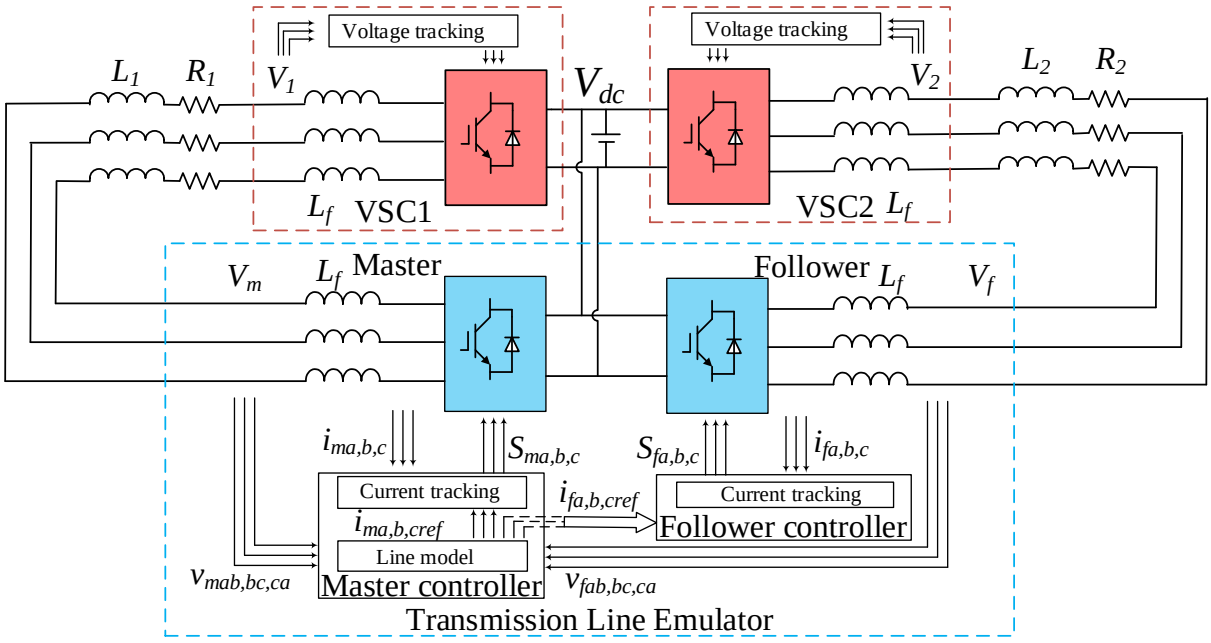


Figure 3-22. Experimental diagram for transmission line emulation verification.

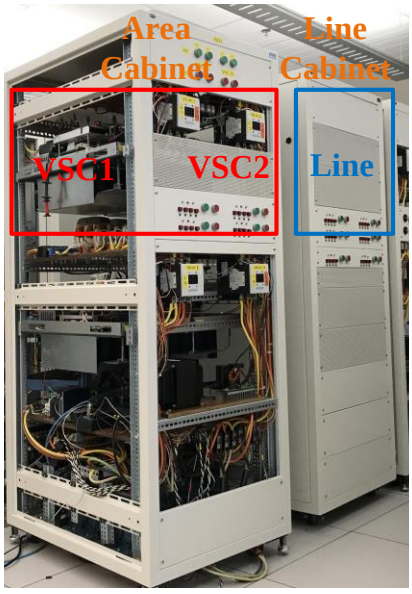


Figure 3-23. Experiment hardware platform for transmission line emulation verification.

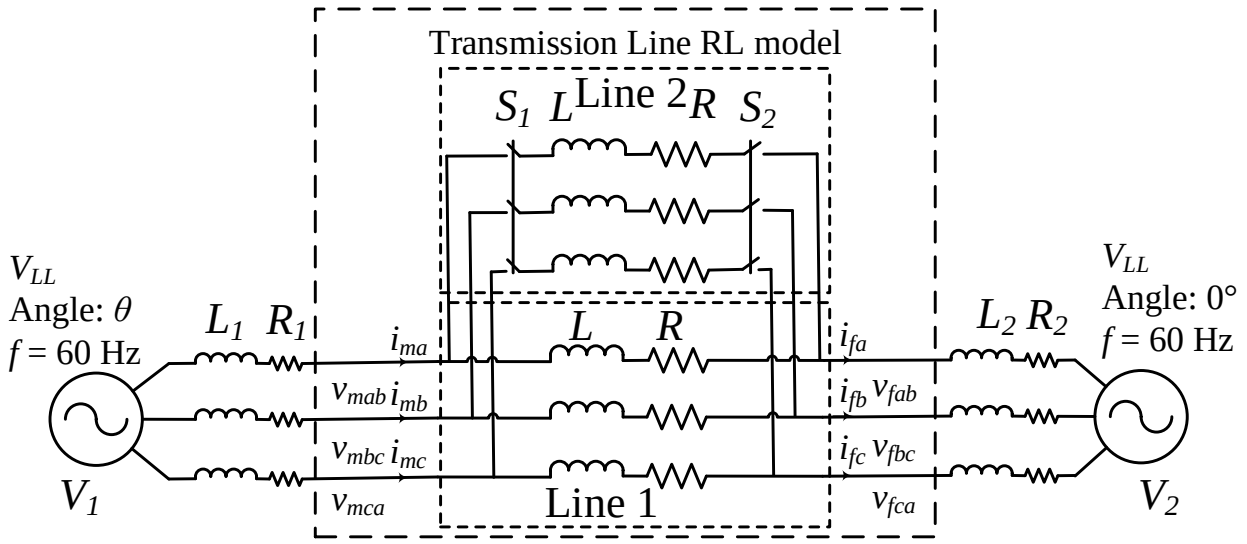
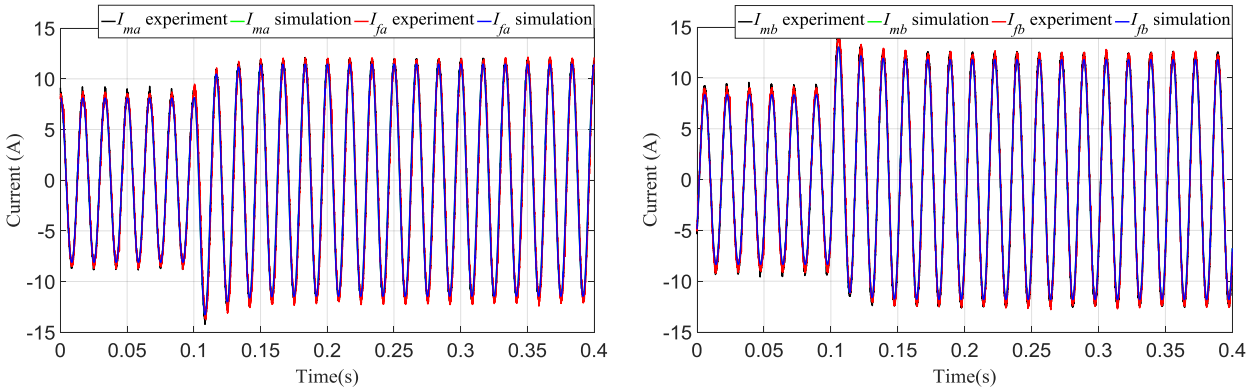


Figure 3-24. System diagram for transmission line RL model verification.



(a) (b)

Figure 3-25. Experiment and simualtion comparisons with the transmission line RL model when Line 2 is connected into the system: (a) I_a; (b) I_b.

- T model

A system diagram with two identical transmission lines, named as Line 1 and Line 2, is built to verify the transmission line T model, as shown in Figure 3-26. The emulated transmission line parameters are L = 12 mH, R = 0.65 Ω, and C = 0.4 mF. Line 2 is connected in parallel with Line 1 through the switches S_1 and S_2 at 0.1 s when the phase angle of V_{1ab} is 9°. The angle difference between the two voltage sources is $\theta = \theta_{V1} - \theta_{V2}$ = -194°. Figure 3-27(a) and Figure 3-27(b) show the I_a and I_b comparisons, respectively, of the experimental and the original simulation results. The results indicate that the experimental waveforms match with the original simulation results.

3.5.2 Transmission Line Emulation with Compensation Devices

- Series compensation capacitor

The system diagram for transmission line RL model with series compensation capacitors verification is shown in Figure 3-28. The emulated transmission line parameters are L = 12 mH, R = 0.65 Ω. The series compensation capacitors are changed from C = 3 mF to C = 0.6 mF at 0.1 s when the phase angle of V_{1ab} is 190°. The angle difference between the two voltage sources is $\theta = \theta_{V1} - \theta_{V2}$ = -63°. Figure 3-29(a) shows the I_a comparison of the transmission line model based simulation and the original simulation results and Figure 3-29(b) shows the I_a comparison of the experimental and the original simulation results. The results indicate that both the transmission line model based simulation and the experimental waveforms match well with the original simulation results.

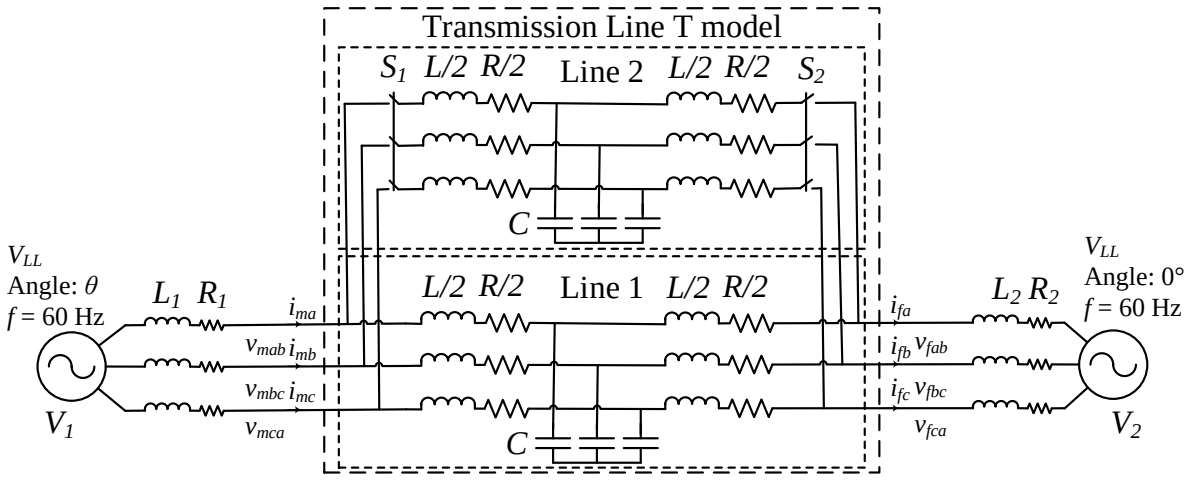
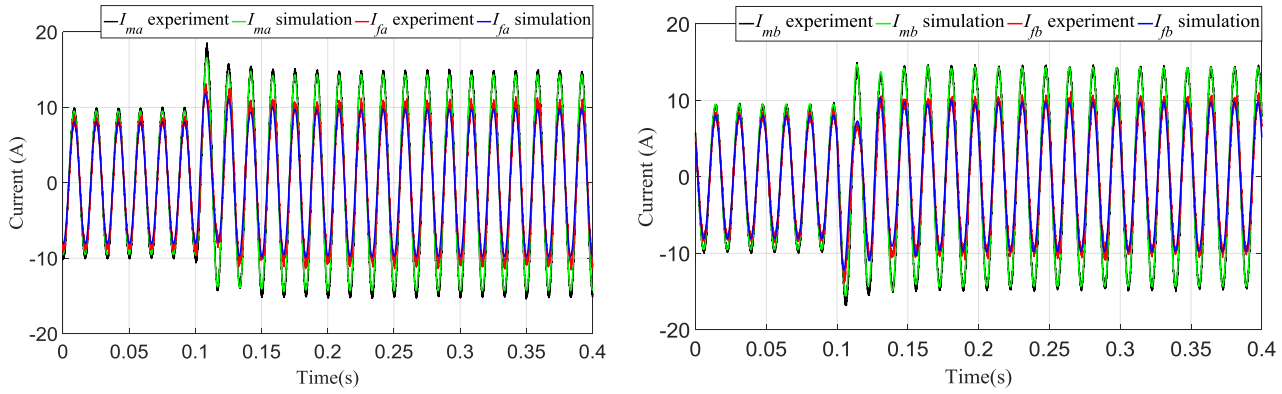


Figure 3-26. System diagram for transmission line T model verification.



(a) (b)

Figure 3-27. Experiment and simualtion comparisons with the transmission line T model when Line 2 is connected into the system: (a) I_a; (b) I_b.

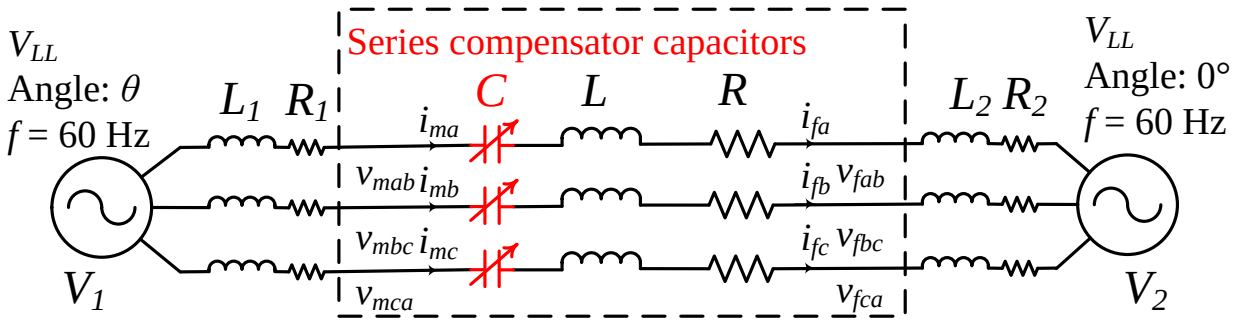
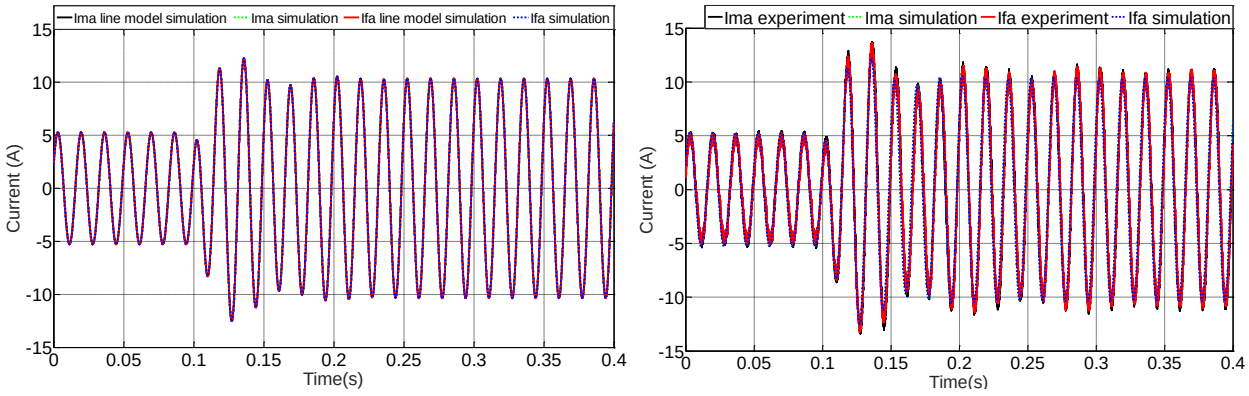


Figure 3-28. System diagram for a transmission line with series compensation capacitors verification.



(a) (b)

Figure 3-29. I_a comparisons with the original simulation for the case of the transmission line with series compensation capacitors: (a) Transmission line model based simulation results; (b) Experimental results.

- Series compensation inductor

The system diagram for transmission line RL model with series compensation inductors verification is shown in Figure 3-30. The emulated transmission line parameters are L = 12 mH, R = 0.65 Ω. The series compensation inductors are changed from L_c = 15 mH to L_c = 0.5 mH at 0.1 s when the phase angle of V_{1ab} is 29°. The angle difference between the two voltage sources is $\theta = \theta_{V1} - \theta_{V2} = 215°$. Figure 3-31(a) shows the I_a comparison of the transmission line model based simulation and the original simulation results, and Figure 3-31(b) shows the I_a comparison of the experimental and the original simulation results. The results indicate that both the transmission line model based simulation and the experimental waveforms match well with the original simulation results.

- Parallel compensation capacitor

The system diagram for transmission line RL model with parallel compensation capacitors verification is shown in Figure 3-32. The emulated transmission line parameters are L = 12 mH, R = 0.65 Ω. The parallel compensation capacitors are changed from C = 1 mF to C = 0.5 mF at 0.1 s when the phase angle of V_{1ab} is 227° and the compensation location parameter λ = 0.5. The angle difference between the two voltage sources is $\theta = \theta_{V1} - \theta_{V2} = 166°$. Figure 3-33(a) shows the I_a comparison of the transmission line model based simulation and the original simulation results, and Figure 3-33(b) shows the I_a comparison of the experimental and the original simulation results. The results indicate that both the transmission line model based simulation and the experimental waveforms match well with the original simulation results.

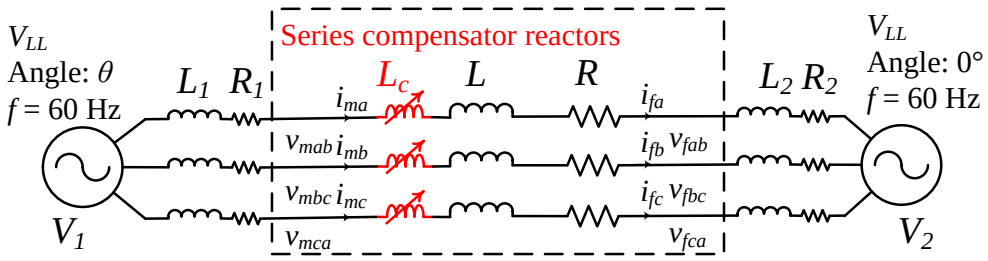
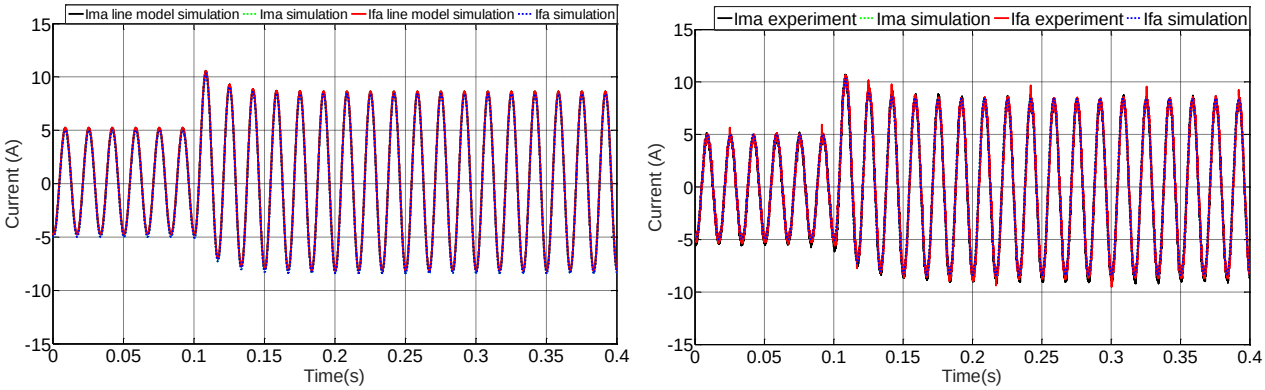


Figure 3-30. System diagram for a transmission line with series compensation inductors verification.



(a) (b)

Figure 3-31. I_a comparisons with the original simulation for the case of the transmission line with series compensation inductors: (a) Transmission line model based simulation results; (b) Experimental results.

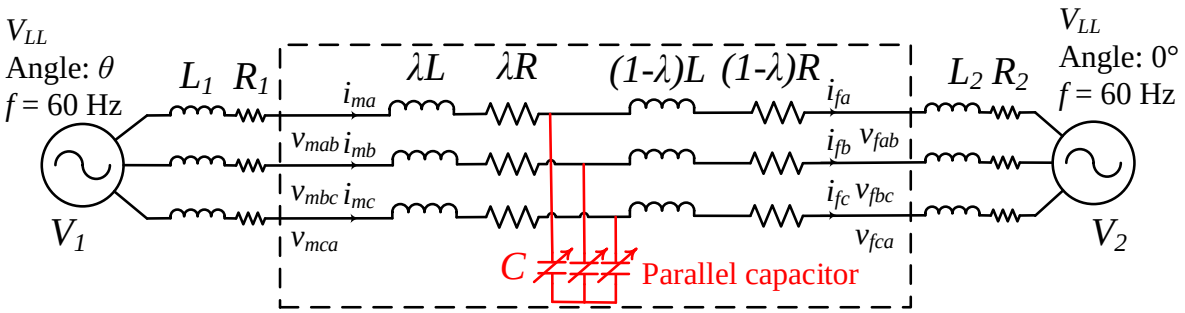
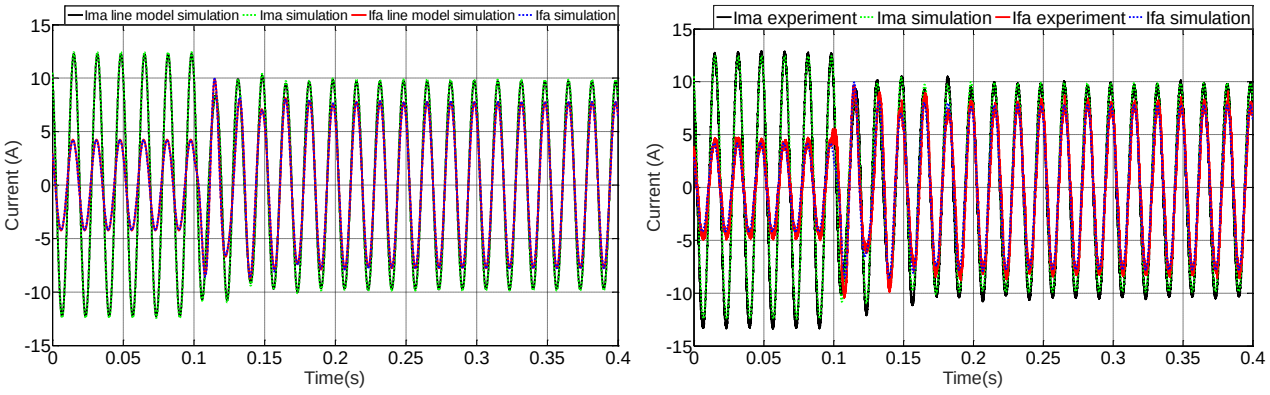


Figure 3-32. System diagram for a transmission line with parallel compensation capacitors verification.



(a) (b)

Figure 3-33. I_a comparisons with the original simulation for the case of the transmission line with parallel compensation capacitors: (a) Transmission line model based simulation results; (b) Experimental results.

- Parallel compensation inductor

The system diagram for transmission line RL model with parallel compensation inductors verification is shown in Figure 3-34. The emulated transmission line parameters are L = 5 mH, R = 0.65 Ω. The parallel compensation inductors are changed from L_c = 12 mH to L_c = 3 mH at 0.1 s when the phase angle of V_{1ab} is 178.2° and the compensation location parameter λ = 0.5. The angle difference between the two voltage sources is $\theta = \theta_{V1} - \theta_{V2}$ = -47.52°. Figure 3-35(a) and Figure 3-35(b) show the I_a and I_b comparisons, respectively, of the experimental and the original simulation results. The results indicate that the experimental waveforms match well with the original simulation results.

3.5.3 Transmission Line Emulation with Traveling Wave Model

A system diagram with two identical transmission lines, named as Line 1 and Line 2, is built to verify the transmission line traveling wave model, as shown in Figure 3-36. The emulated transmission line parameters are Z = 16 Ω and H = 0.9865, and Line 2 is connected in parallel with Line 1 through switches S_1 and S_2 at 0.1 s.

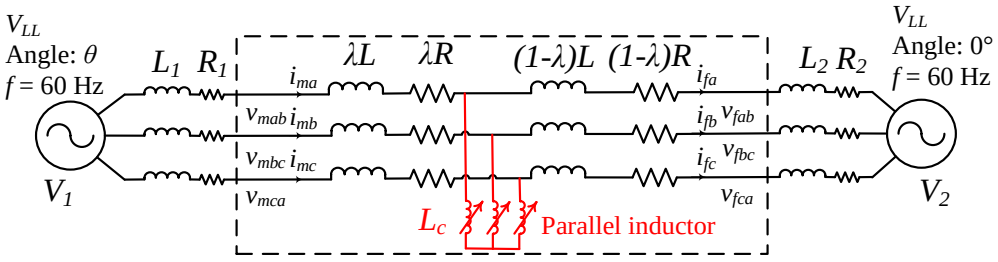
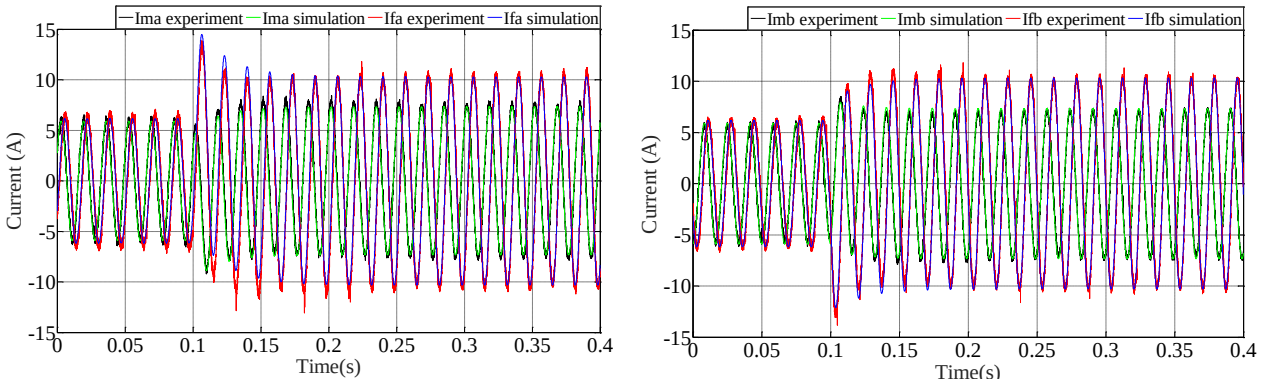


Figure 3-34. System diagram for a transmission line with parallel compensation inductors.



(a) (b)

Figure 3-35. I_a experiment comparisons with the original simulation for the case of the transmission line with parallel compensation inductors: (a) Phase A current; (b) Phase B current.

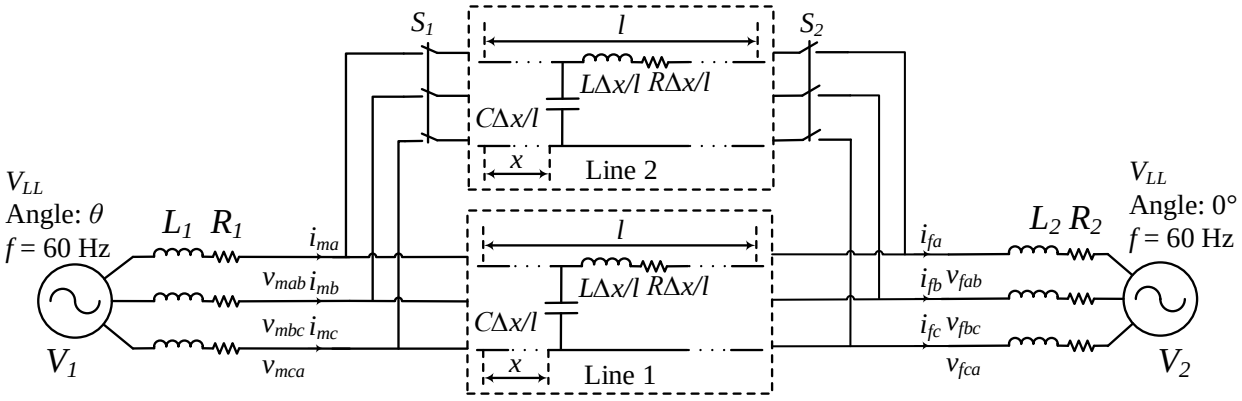


Figure 3-36. System diagram for a transmission line traveling wave model verification.

a) Transmission line traveling time $\tau = 0.5$ ms

For the transmission line traveling time τ equals to 0.5 ms, Line 2 is switched into the system at 0.1 s when the phase angle of V_{1ab} is 6.5° and the angle difference between the two voltage sources is $\theta = \theta_{V1} - \theta_{V2} = -107°$. Figure 3-37(a) and Figure 3-37(b) show the I_a and I_b comparisons, respectively, of the experimental and the original simulation results. The results indicate that the experimental waveforms match with the original simulation results.

b) Transmission line traveling time $\tau = 1$ ms

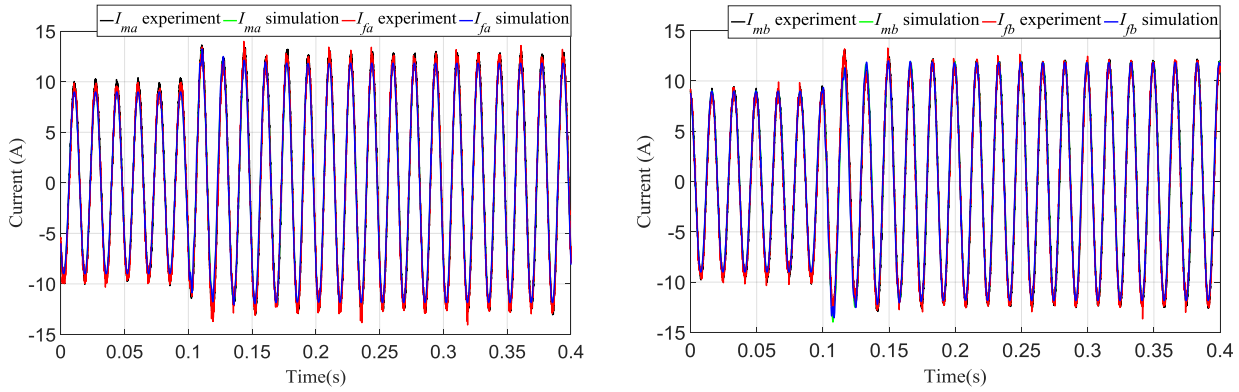
For the transmission line traveling time τ equals to 1 ms, Line 2 is switched into the system at 0.1 s when the phase angle of V_{1ab} is 6.5° and the angle difference between the two voltage sources is $\theta = \theta_{V1} - \theta_{V2} = -125°$. Figure 3-38(a) and Figure 3-38(b) show the I_a and I_b comparisons, respectively, of the experimental and the original simulation results.

c) Transmission line traveling time $\tau = 1.5$ ms

For the transmission line traveling time τ equals to 1.5 ms, Line 2 is switched into the system at 0.1 s when the phase angle of V_{1ab} is 25° and the angle difference between the two voltage sources is $\theta = \theta_{V1} - \theta_{V2} = -130°$. Figure 3-39(a) and Figure 3-39(b) show the I_a and I_b comparisons, respectively, of the experimental and the original simulation results. The results indicate that the experimental waveforms match with the original simulation results.

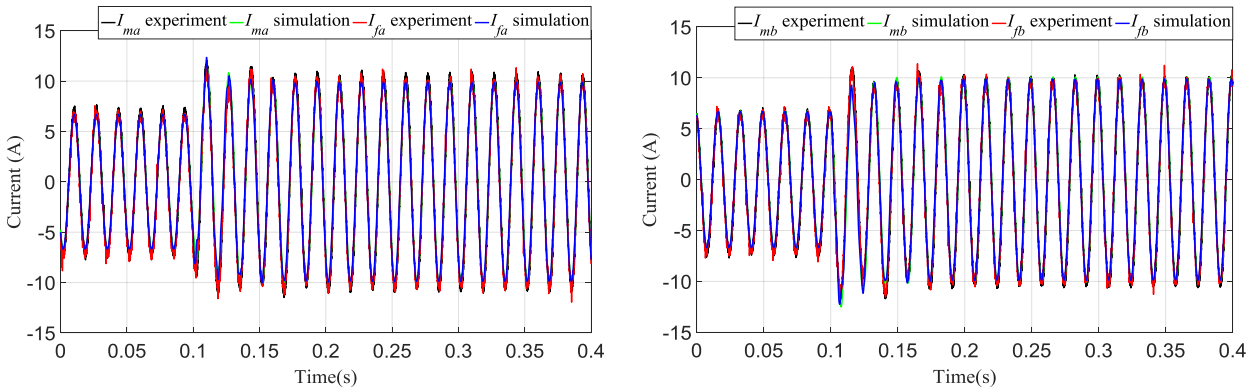
d) Transmission line traveling time $\tau = 2$ ms

For the transmission line traveling time τ equals to 2 ms, Line 2 is switched into the system at 0.1 s when the phase angle of V_{1ab} is -1° and the angle difference between the two voltage sources is $\theta = \theta_{V1} - \theta_{V2} = -141°$. Figure 3-40(a) and Figure 3-40(b) show the I_a and I_b comparisons, respectively, of the experimental and the original simulation results.



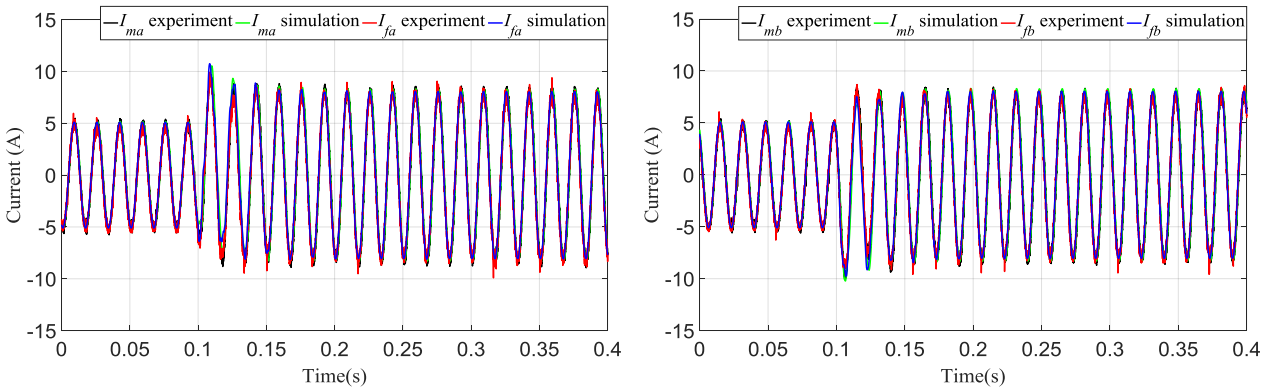
(a) (b)

Figure 3-37. Experiment and simualtion comparisons with the transmission line traveling wave model when the traveling time τ equals to 0.5 ms: (a) I_a; (b) I_b.



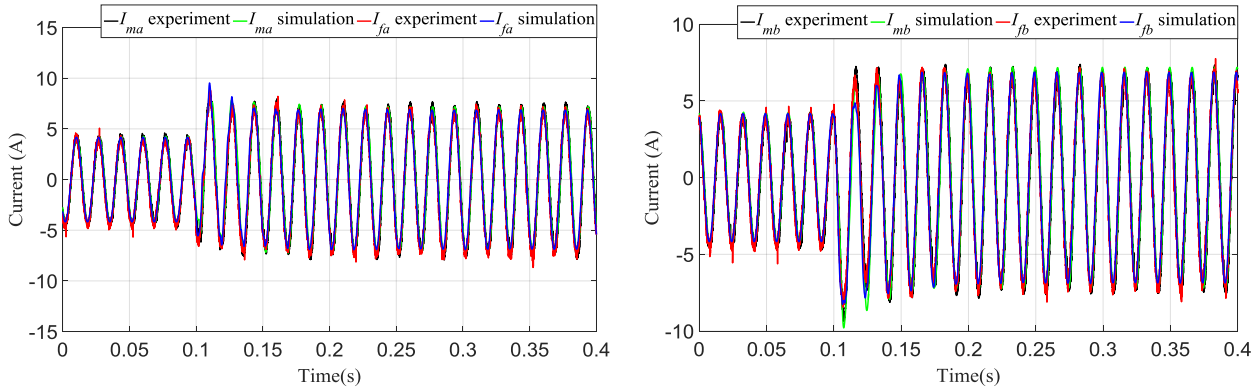
(a) (b)

Figure 3-38. Experiment and simualtion comparisons with the transmission line traveling wave model when the traveling time τ equals to 1 ms: (a) I_a; (b) I_b.



(a) (b)

Figure 3-39. Experiment and simualtion comparisons with the transmission line traveling wave model when the traveling time τ equals to 1.5 ms: (a) I_a; (b) I_b.



(a) (b)

Figure 3-40. Experiment and simualtion comparisons with the transmission line traveling wave model when the traveling time τ equals to 2 ms: (a) I_a; (b) I_b.

3.5.4 Transmission Line Emulation Accuracy

By zooming in the waveform comparisons in section 3.5.1, section 3.5.2, and section 3.5.3, the phase A current I_{ma} and I_{fa} amplitudes and phase angle differences between the emulation experiments and the original system simulations are identified as shown in Table 2. According to Table 2, the current I_{ma} and I_{fa} amplitudes differences between the transmission line emulation experiments and the original system simulations are smaller than 0.3 A, which is less than 4% of all original system simulation results. The current I_{ma} and I_{fa} phase angle differences between the transmission line emulation experiments and the original system simulations are not larger than 3°, which is less than 150 us time difference for the 60 Hz waveforms.

3.6 Conclusion

The emulation algorithms of transmission line RL, Π, T and traveling wave models have been proposed according to the characteristics of the circuit diagrams. The transmission line emulations with integrated series or parallel variable capacitors or inductors have been developed to emulate the transmission line together with series or parallel compensation devices. By comparing with the system simulation with the original transmission line and compensation devices, the proposed algorithms have been verified to emulate the transmission line together with the compensation devices well through both simulations in MATLAB/SIMULINK environment and experiments in the HTB.

Table 2. Phase A current I_{ma} and I_{fa} amplitudes and phase angles differences between the emulation experiments and the original system simulations

Emulation case	I_{ma} amplitude		I_{ma} phase angle difference (°)	I_{fa} amplitude		I_{fa} phase angle difference (°)
	Original (A)	Difference (%)		Original (A)	Difference (%)	
RL model	8.3	3.6	1	8.2	3.7	2
T model	9.5	2.1	3	8.1	2.5	3
Series compensation capacitor	5.3	3.8	2	5.3	3.8	2
Series compensation inductor	5.0	2.0	2	5	2.0	2
Parallel compensation capacitor	12.4	1.6	3	4.2	2.4	3
Parallel compensation inductor	5.9	1.7	1	6.2	1.6	2
Traveling wave time 1 ms	6.8	1.5	1	6.7	3.0	2
Traveling wave time 1.5 ms	5.2	1.9	1	5.1	2.0	1
Traveling wave time 2 ms	4.3	1.2	1	4.2	1.2	1

4 Transmission Line Emulation with a Balanced Fault

In this chapter, the algorithm of transmission line emulation with a balanced fault is proposed. For lumped RL and T models, the current references calculated for the transmission line emulation correspond to the line inductor currents. If the current references of the transmission line normal and fault models are solved separately, a small current reference mismatch between the normal and fault models would cause a current step change of an inductor during the switching between the normal and fault states, which would induce a large voltage spike or even instability. A smooth switching algorithm is proposed by combining the normal state model and fault state model together. To locate the boundary of emulating transmission line stably, the emulation stability under both normal states and fault states is analyzed. Experiment results verified the effectiveness of the proposed model and smooth switching algorithm.

4.1 Transmission Line with a Balance Fault Model

In a balanced system, the transmission line three-phase-to-ground fault is equivalent to a three-phase fault since the neutral to ground voltage is zero. The transmission line RL model with a balanced fault is shown in Figure 4-1 where R_F is the fault resistance. The parameter γ ($0 < \gamma < 1$) is the percentage of the distance from the fault location "o" to the Master side terminal with regard to the total line length.

The transmission line model with a balanced fault is expressed in (4-1).

$$\begin{cases} v_{mx} - v_{ox} = \gamma L \dfrac{di_{mx}}{dt} + \gamma R i_{mx} \\ v_{ox} - v_{fx} = (1-\gamma) L \dfrac{di_{fx}}{dt} + (1-\gamma) R i_{fx} \quad (x = a, b, c) \\ v_{ox} = R_F\left(i_{mx} - i_{fx}\right) \end{cases} \tag{4-1}$$

By measuring the terminal voltages, the current references can be derived from (4-2).

$$\begin{cases} i_{mxref} = \int \dfrac{v_{mx} - R_F(i_{mx} - i_{fx}) - \gamma R i_{mx}}{\gamma L} dt \\ i_{fxref} = \int \dfrac{R_F(i_{mx} - i_{fx}) - v_{fx} - (1-\gamma) R i_{fx}}{(1-\gamma) L} dt \end{cases} \tag{4-2}$$

Thus, the emulation algorithm of a transmission line with a balanced fault is derived as shown in Figure 4-2.

The emulation algorithm of a transmission line under a balanced fault with a zero fault resistance is derived by setting R_F to zero, as shown in Figure 4-3. The balanced fault with a zero fault resistance is the most severe fault within a transmission line, which is commonly utilized for power system transient stability studies.

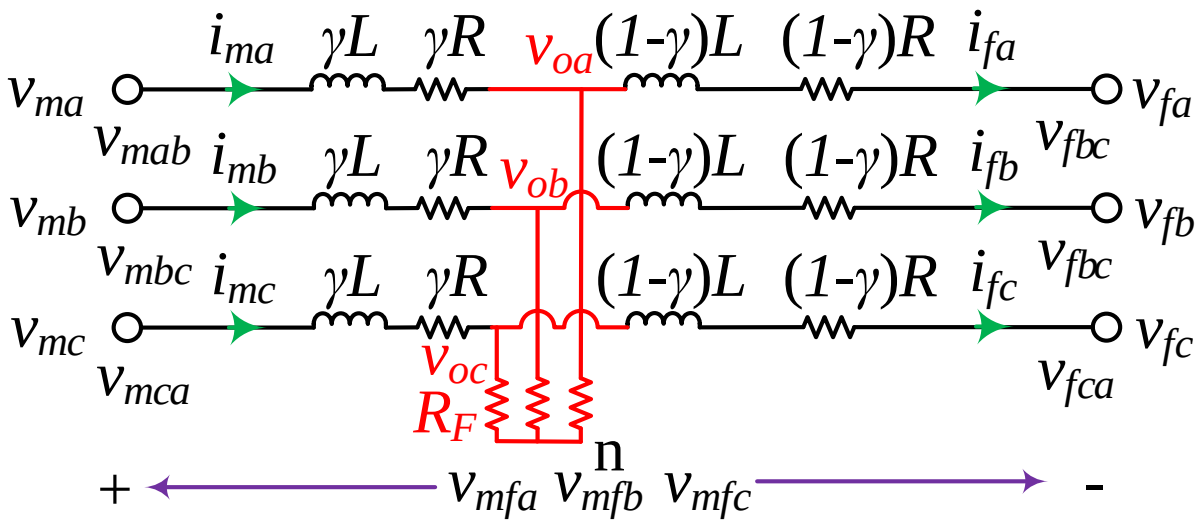


Figure 4-1. Transmission line with a balanced three-phase fault.

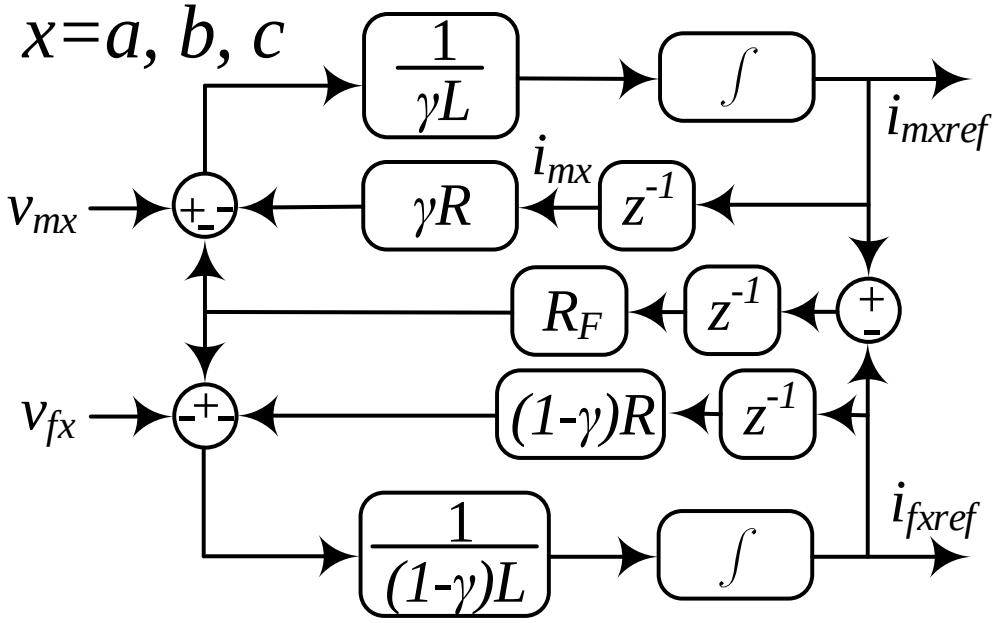


Figure 4-2. Transmission line with a balanced fault emulation algorithm.

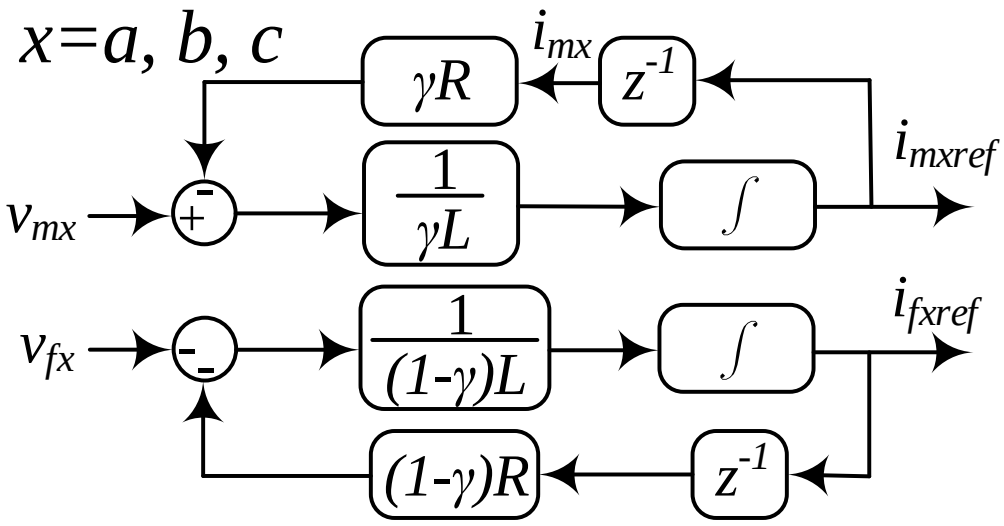


Figure 4-3. Transmission line with a balanced zero resistance fault emulation algorithm.

4.2 Smooth Switching Algorithm between Normal State and Fault State

Considering the ideal current tracking performance, the transmission line emulator main circuit can be simplified and represented as controlled current sources, as shown in Figure 4-4.

By switching the controlled current source input references between the model under the normal state and the model under the fault state, the transmission line emulator can realize the emulations of both normal state and fault state. However, at the switching moment, there can be current reference errors between the normal state and the fault state if the two models are calculated separately. The error introduces undesired transients, especially when the transmission line is in series with inductors, which cannot tolerate current step changes.

In this thesis, a combined model is proposed to avoid the switching transients between the normal state and the fault state. Instead of switching the controlled current source input references, the inputs of the integral units for the current reference calculations are switched, as shown in Figure 4-5, which combines the normal and fault states in one model. Figure 4-5(a) and (b) are the transmission line emulation model with non-zero fault resistance and zero fault resistance, respectively. The single-pole double-throw switches are implemented to switch between the normal state and the short-circuit fault state. The emulated transmission line operates at the normal state when the switches are at position “1”; otherwise, it operates at the short-circuit fault state if the switches are at position “2”.

4.3 Parallel-connected Transmission Lines

Parallel-connected transmission lines are commonly utilized in power grids for power delivery reliability and full utilization of corridors. Figure 4-6 shows a diagram with *k* parallel-connected lines.

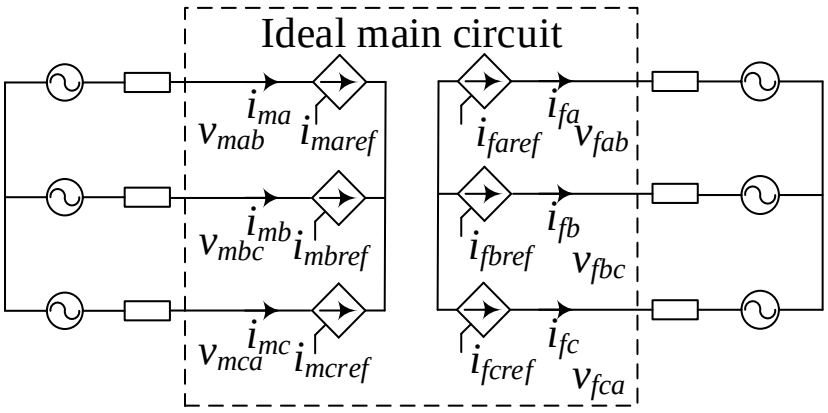
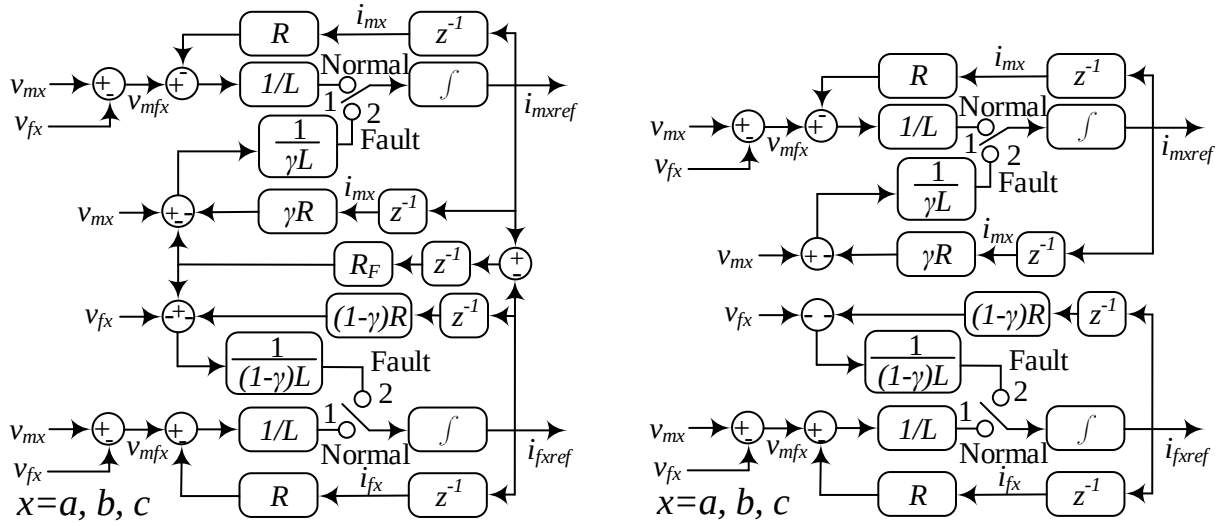


Figure 4-4. Transmission line emulator ideal main circuit model.



(a) (b)

Figure 4-5. Transmission line emulation model under balanced fault: (a) Non-zero resistive fault; (b) Zero resistive fault.

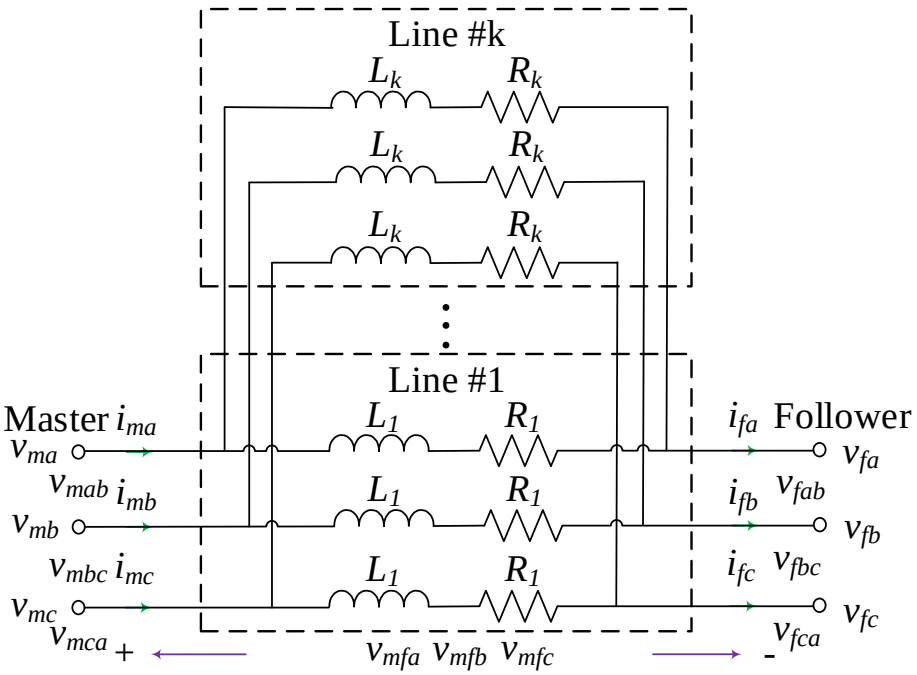


Figure 4-6. Diagram of parallel-connected transmission lines.

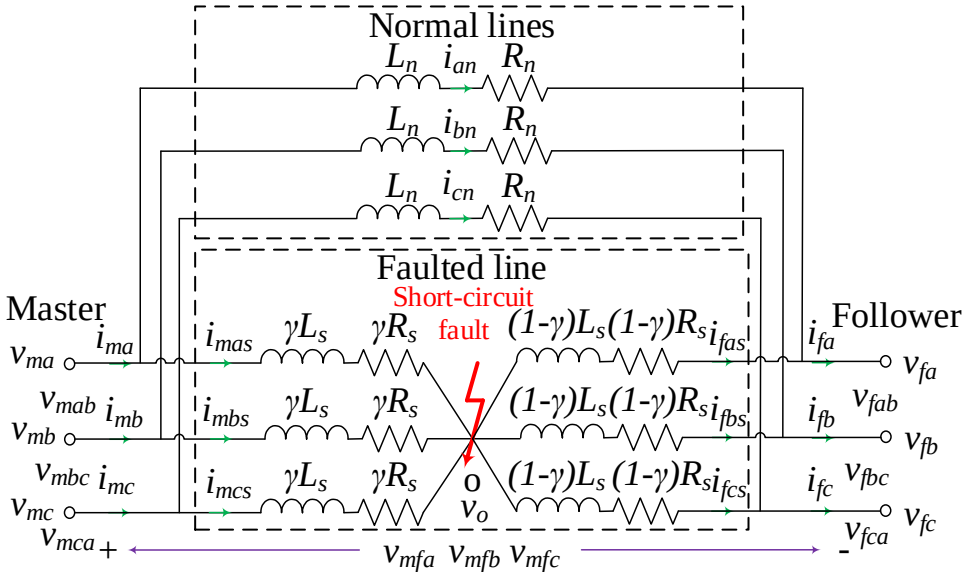


Figure 4-7. Parallel-connected lines with a three-phase short-circuit fault.

When a three-phase short-circuit fault happens within one of the parallel-connected transmission lines, the parallel-connected transmission lines can be separated into two parts, which are the normal lines and the faulted line, as shown in Figure 4-7. The normal lines can be integrated into a single transmission line with equivalent inductance L_n and resistance R_n of all normal lines in parallel. The faulted line inductance and resistance are named as L_s and R_s, respectively.

The phase A, B and C currents of the normal lines are named as i_{an}, i_{bn} and i_{cn}, respectively, with the corresponding current references i_{anref}, i_{bnref} and i_{cnref} from the transmission line model. The Master side phase A, B and C currents of the faulted line are named as i_{mas}, i_{mbs} and i_{mcs}, respectively, with the corresponding current references i_{masref}, i_{mbsref} and i_{mcsref} from the transmission line model. The Follower side phase A, B and C currents of the faulted line are named as i_{fas}, i_{fbs} and i_{fcs}, respectively, with the corresponding current references i_{fasref}, i_{fbsref} and i_{fcsref} from the line model.

Figure 4-8 shows the combined model of parallel-connected transmission lines with a three-phase short-circuit fault happens within one of the transmission lines. The normal line model and the line model with a three-phase short-circuit fault are solved separately. The total current reference of the parallel-connected transmission lines is derived by adding up the current references of the normal line model and the line model with a three-phase short-circuit fault. The single-pole double-throw switches are implemented to switch between the normal state and the short-circuit fault state of the predetermined transmission line for the three-phase short-circuit fault emulation. The predetermined transmission line operates at the normal state when the switches are at position “1”; otherwise, it operates at the short-circuit fault state if the switches are at position “2”.

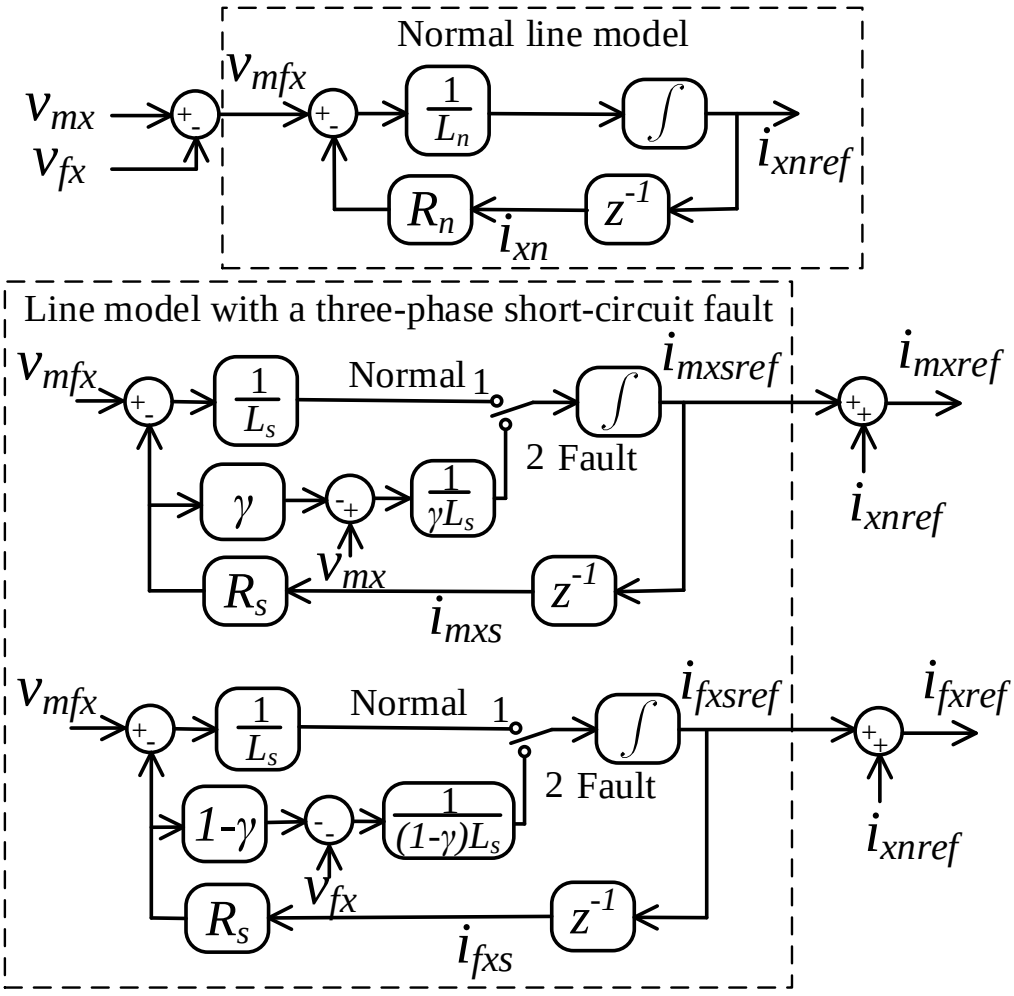


Figure 4-8. Combined model of parallel-connected transmission lines.

4.4 Transmission Line Emulation Stability Analysis

4.4.1 Single Transmission Line Stability Analysis

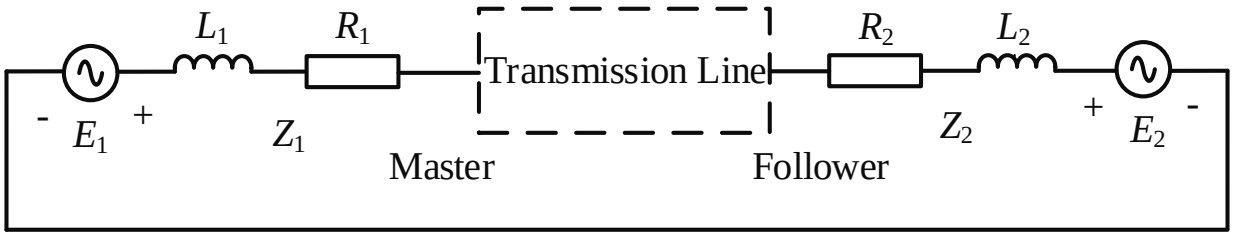
Similar to the power HIL interface algorithms, there is a potential emulation stability issue induced by the time delay within the transmission line emulator. It is essential to locate the boundary conditions of emulating the transmission line stably [88]. A balanced three-phase circuit can be separated into three identical single-phase circuits for analysis.

Assume the single-phase diagram of a power system where the transmission line can be simplified as in Figure 4-9(a). E_1 and Z_1 are the equivalent voltage source and impedance at the Master side. E_2 and Z_2 are the equivalent voltage source and impedance at the Follower side. Theoretically, the models of the two VSCs, which are programmed to emulate the transmission line, should also be considered in the stability analysis.

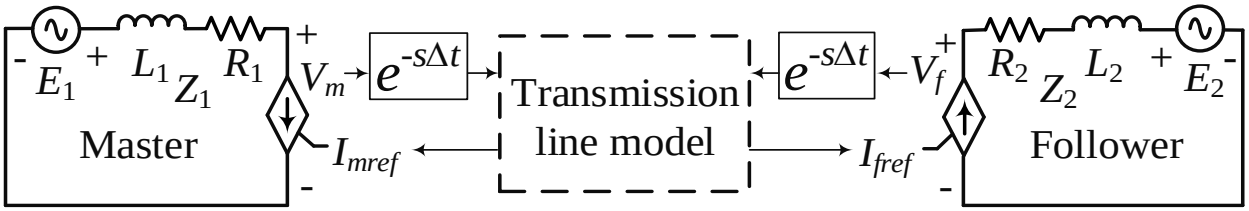
In this thesis, in order to focus on the stability analysis of the transmission line emulation algorithm itself and derive a more generalized stability condition guidance, the VSC current tracking performance is assumed to be ideal. Figure 4-9 (b) shows the single-phase diagram with the transmission line emulator considering ideal current tracking performance. Similar to the power HIL interface algorithm analysis in [89]-[92], assuming the total time delay within the transmission line emulator is Δt, and the time delay is applied on the voltage measurements to simplify the analysis. For the stability analysis, only balanced zero resistive faults are considered.

In s-domain, the circuit at the Master side and the circuit at the Follower side can be expressed in (4-3).

$$\begin{cases} E_1(s) = Z_1(s)I_{mref}(s) + V_m(s) \\ E_2(s) = -Z_2(s)I_{fref}(s) + V_f(s) \end{cases} \tag{4-3}$$



(a)



(b)

Figure 4-9. Simplified single-phase diagram: (a) Original system; (b) System with transmission line emulator.

Under the normal condition, the transmission line model can be expressed as in (4-4), where Z_L is the transmission line impedance.

$$I_{mref}(s) = I_{fref}(s) = \left(V_m(s) - V_f(s)\right) e^{-s\Delta t}/Z_L(s) \tag{4-4}$$

Substitute (4-4) into (4-3), the current references can be solved as in (4-5).

$$I_{mref}(s) = I_{fref}(s) = \frac{\left(E_1(s) - E_2(s)\right)/Z_L(s)e^{-s\Delta t}}{\left(\left(Z_1(s) + Z_2(s)\right)/Z_L(s)e^{-s\Delta t}\right) + 1} \tag{4-5}$$

According to (4-5), taking E_1 or E_2 as the input and I_{mref} or I_{fref} as the output, the denominator of the closed-loop transfer function is the denominator in (4-5). Thus, the open-loop transfer function can be obtained as the expression inside of the absolute value sign in (4-6). If the magnitude of the open-loop transfer function is smaller than 1, there is no 0 dB crossing point in the amplitude-frequency curve, which means that the phase margin is infinite. Thus, the system is assured to be stable when (4-6) is satisfied.

$$I_{mref}(s) = I_{fref}(s) = \frac{\left(E_1(s) - E_2(s)\right)/Z_L(s)e^{-s\Delta t}}{\left(\left(Z_1(s) + Z_2(s)\right)/Z_L(s)e^{-s\Delta t}\right) + 1} \tag{4-6}$$

The stability requirement is expressed in (4-7) based on (4-6).

$$|Z_1 + Z_2| < |Z_L| \tag{4-7}$$

According to (4-7), under normal conditions, the transmission line emulation is assured to be stable if the line impedance is larger than the sum of the equivalent source impedances at both sides of the transmission line.

Under a short-circuit fault with zero fault resistance condition, the transmission line model can be expressed as in (4-8), where Z_L is the transmission line impedance and γ is the percentage of the distance from the fault location to the Master side terminal with regard to the total line length.

$$\begin{cases} I_{mref}(s) = V_m(s)e^{-s\Delta t}/(\gamma Z_L(s)) \\ I_{fref}(s) = V_f(s)e^{-s\Delta t}/\big((1-\gamma)Z_L(s)\big) \end{cases} \tag{4-8}$$

Substitute (4-8) into (4-3), the current references can be solved as in (4-9).

$$\begin{cases} I_{mref}(s) = \dfrac{E_1(s)/(\gamma Z_L(s))e^{-s\Delta t}}{(Z_1(s)/(\gamma Z_L(s))e^{-s\Delta t}) + 1} \\ I_{fref}(s) = \dfrac{E_2(s)/((1-\gamma)Z_L(s))e^{-s\Delta t}}{(Z_2(s)/((1-\gamma)Z_L(s))e^{-s\Delta t}) + 1} \end{cases} \tag{4-9}$$

Similarly, the system is assured to be stable when (4-10) is satisfied.

$$\begin{cases} \left|Z_1(s)/(\gamma Z_L(s))e^{-s\Delta t}\right| < 1 \\ \left|Z_2(s)/((1-\gamma)Z_L(s))e^{-s\Delta t}\right| < 1 \end{cases} \tag{4-10}$$

The stability requirement is expressed in (4-11) based on (4-10), and the line model is more likely to be unstable if the fault is at one end of the transmission line (γ is close to 0 or 1).

$$\begin{cases} |Z_1| < |\gamma Z_L| \\ |Z_2| < |(1-\gamma)Z_L| \end{cases} \tag{4-11}$$

4.4.2 Parallel-connected Transmission Line Stability Analysis

Under normal conditions, the parallel-connected transmission line model is the same as the single transmission line, thus the transmission line emulation is stable if the equivalent impedance of the parallel-connected transmission lines is larger than the sum of the equivalent

source impedances at both sides of the transmission line.

Under a short-circuit fault with zero fault resistance condition, the transmission line can be separated into the normal lines and the faulted line. The emulation stability of normal lines can be evaluated by assuming the short-circuited line operates stably, as shown in Figure 4-10. According to Thevenin-Norton theorem, the Master side and Follower side equivalent impedances are $Z_1 \parallel (\gamma Z_s)$ and $Z_2 \parallel ((1-\gamma)\, Z_s)$, respectively, where Z_s is the faulted transmission line impedance. Similar as the single transmission line analysis, the stability requirement is expressed in (4-12), where Z_n is the normal transmission line impedance.

$$|(Z_1 \,||\, (\gamma Z_s)) + (Z_2 \,||\, ((1-\gamma) Z_s))| < |Z_n| \tag{4-12}$$

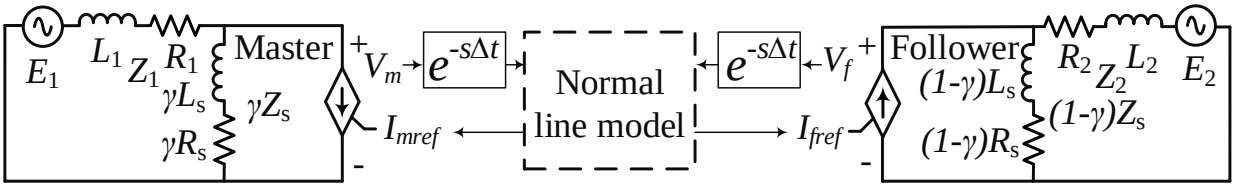
The Master side emulation stability of the faulted line can be evaluated by assuming the normal lines and the faulted line Follower side operate stably, as shown in Fig. 14 (b). According to Thevenin-Norton theorem, the equivalent impedance at the Master terminal is $((Z_2 \parallel ((1-\gamma)\, Z_s)) + Z_n) \parallel Z_1$. The stability requirement is expressed in (4-13).

$$|((Z_2 \,||\, ((1-\gamma) Z_s)) + Z_n)||Z_1| < |\gamma Z_s| \tag{4-13}$$

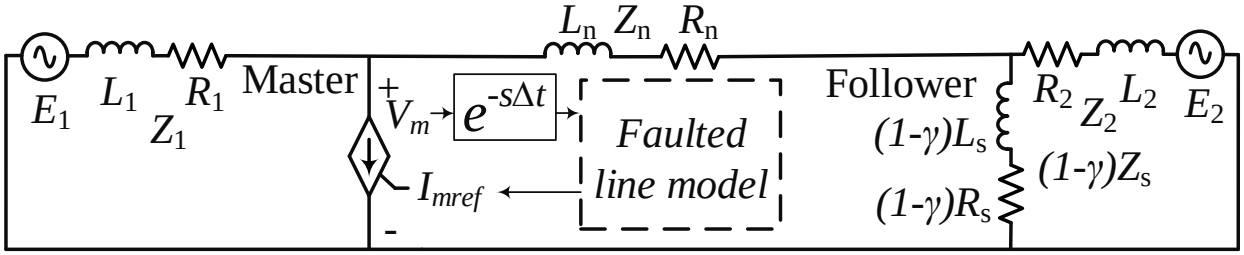
Similarly, the Follower side emulation stability of the faulted line can be evaluated by assuming the normal lines and the faulted line Master side operate stably, as shown in Fig. 14 (c), and the Follower side stability requirement is expressed in (4-14).

$$|((Z_1 \,||\, (\gamma Z_s)) + Z_n)||Z_2| < |(1-\gamma) Z_s| \tag{4-14}$$

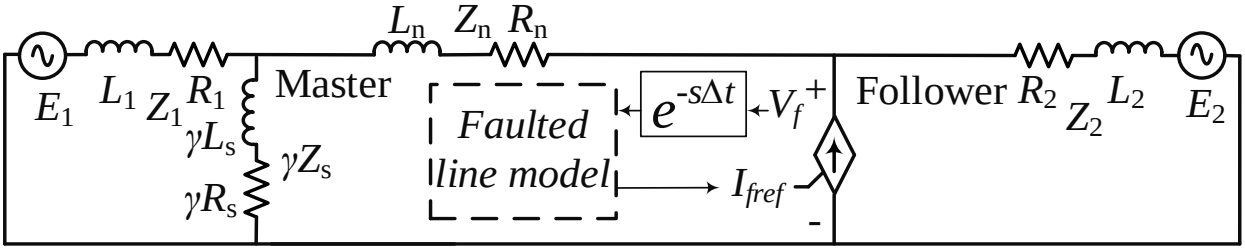
Thus, the emulation of parallel-connected transmission lines with a three-phase short-circuit within one transmission line is assured to be stable when (4-12), (4-13) and (4-14) are satisfied.



(a)



(b)



(c)

Figure 4-10. Stability analysis diagram of the parallel-connected transmission line with a three-phase short-circuit at one of the transmission lines: (a) Normal line stability analysis model; (b) Faulted line Master side stability analysis model; (c) Faulted line Follower side stability analysis model.

4.5 Simulation and Experiment Results

The same as the transmission line emulation verification under normal conditions, a system diagram of a transmission line connected between two voltage sources is set up to verify the transmission line fault emulation, as shown in Figure 3-23. In the HTB, the ideal voltage sources V_1 and V_2 are realized by voltage source converters through maintaining the voltage magnitude with closed-loop control.

The ideal voltage source frequency is kept at 60 Hz, but the angle can be modified manually through the Human Machine Interface (HMI) to change the power flow between the two sources. The voltage source internal impedances are realized by physical inductors, which are L_1, R_1 and L_2, R_2, respectively. The transmission line can be set to connect between two ideal voltage sources by using zero internal impedances (Set L_1, R_1, L_2, and R_2 to zero) for the voltage sources.

4.5.1 Zero Resistive Fault Emulation of a Single Transmission Line

The system diagram of the single transmission line experiment verification is shown in Figure 4-11. The transmission line inductance and resistance are L and R, respectively. The three-phase short-circuit fault happens at the location γ ($0<\gamma<1$), which is the ratio of the distance from the fault location to the Master side terminal with regard to the total line length.

- A single transmission line connected with two ideal voltage sources scenario

To verify the transmission line emulation performance by connecting to two ideal voltage sources, the voltage source impedances are set to zero (L_1, R_1, L_2, and R_2 equal to zero). The transmission line inductance and resistance are selected as 12 mH and 0.3 Ω, respectively. Three fault scenarios with γ equals to 1/3, 1/2, and 2/3, respectively, are conducted to verify the three-phase short-circuit fault emulation at different locations within the emulated transmission line.

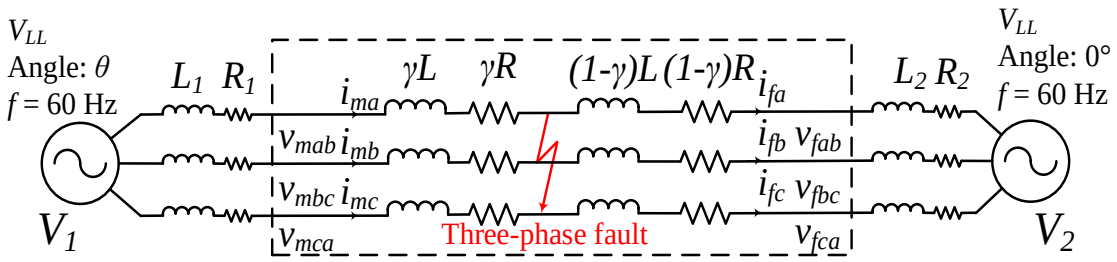


Figure 4-11. System topology for single line experimental verification.

a) Three-phase short-circuit fault with γ = 1/3

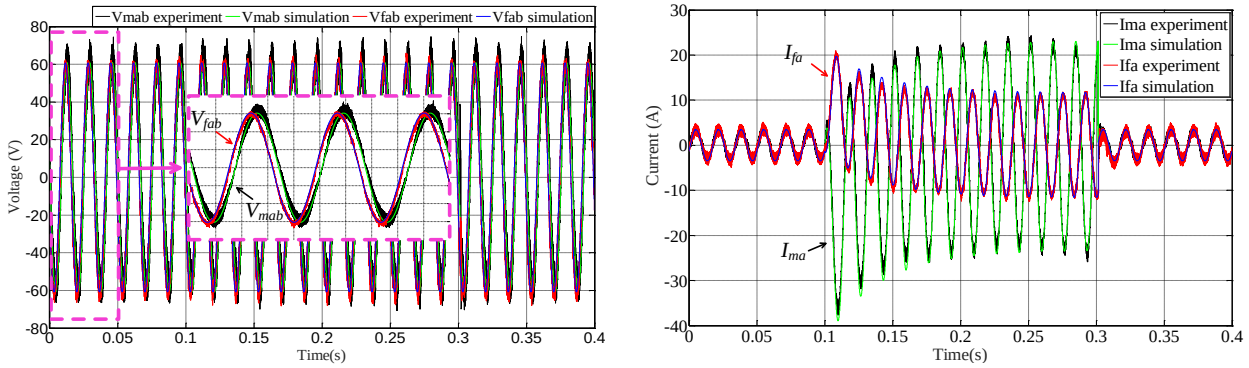
A three-phase short-circuit fault happens at 0.1 s and cleared at 0.3 s at the location γ = 1/3 when the phase angle of V_{mab} is 170°. The angle difference between the two voltage sources is $\theta = \theta_{V1} - \theta_{V2}$ = -26°. Figure 4-12(a) and Figure 4-12(b) show the experiment and simulation result comparisons of V_{ab} and I_a, respectively, which indicate that the experimental waveforms match with the simulation results.

b) Three-phase short-circuit fault with γ = 1/2

A three-phase fault happens at 0.1 s and cleared at 0.3 s at the location γ = 1/2 when the phase angle of V_{mab} is 130°. The angle difference between the two sources is θ = -30°. Figure 4-13(a) and Figure 4-13(b) show the experiment and simulation comparisons of V_{ab} and I_a, respectively.

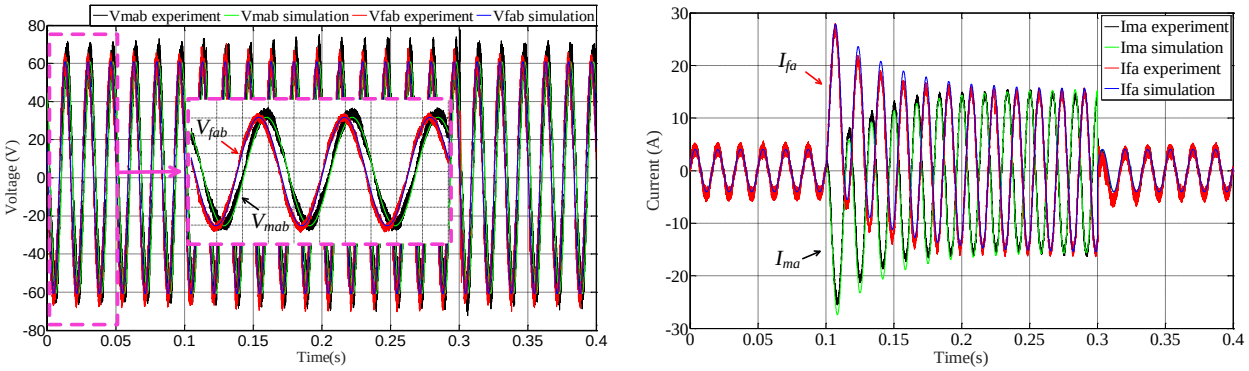
c) Three-phase short-circuit fault with γ = 2/3

A three-phase fault happens at 0.1 s and cleared at 0.3 s at the location γ = 2/3 when the phase angle of V_{mab} is 150°. The angle difference between the two voltage sources is $\theta = \theta_{V1} - \theta_{V2}$ = -22°. Figure 4-14(a) and Figure 4-14(b) show the experiment and simulation result comparisons of V_{ab} and I_a, respectively.



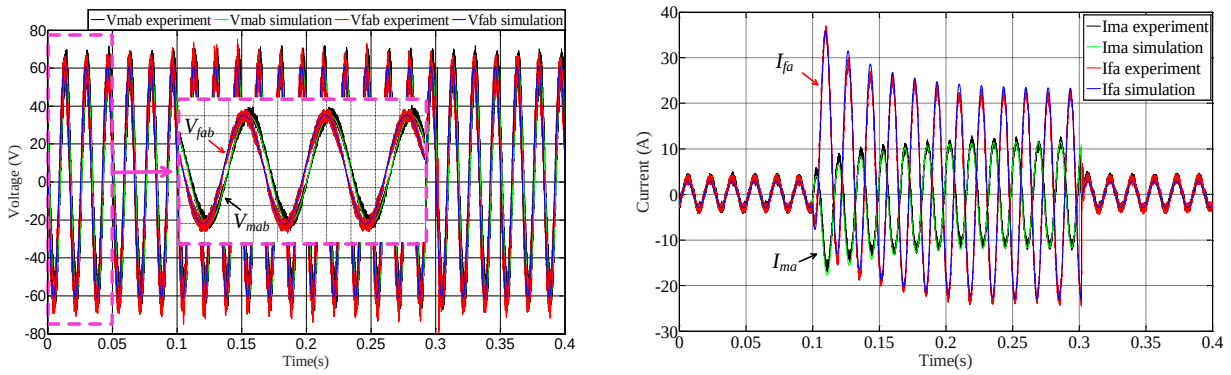
(a) (b)

Figure 4-12. Single transmission line experiment and simulation comparison with γ = 1/3: (a) V_{ab}; (b) I_a.



(a) (b)

Figure 4-13. Single transmission line experiment and simulation comparison with γ = 1/2: (a) V_{ab}; (b) I_a.



(a) (b)

Figure 4-14. Single transmission line experiment and simulation comparison with γ = 2/3: (a) V_{ab}; (b) I_a.

- A single transmission line connected with two non-ideal voltage sources scenario

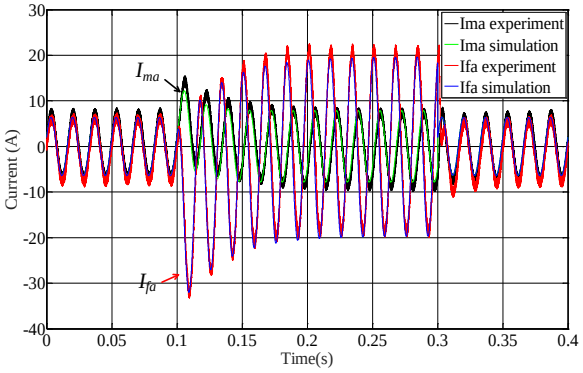
In order to verify the single transmission line emulation stability, two non-ideal voltage sources are connected with the transmission line by setting the voltage source impedances L_1 to 5.97 mH, R_1 to 0.65 Ω, L_2 to 2.4 mH, and R_2 to 0.07 Ω. Similar to the power HIL interface algorithm, the transmission line emulation instability usually happens at the frequency range higher than the fundamental frequency. In order to simplify the analysis, the inductance is employed to judge the transmission line emulation stability since the resistance is negligible compared to the reactance in the high frequency range. According to (4-7), the transmission line emulation is assured to be stable under normal conditions if the transmission line inductance L is larger than 5.97 mH + 2.4 mH = 8.37 mH. According to (4-11), the transmission line emulation is assured to be stable under fault conditions if the inductance between the fault location and the Master terminal γL is larger than 5.97 mH and the inductance between the fault location and the

Follower terminal ((1-γ) L) is larger than 2.4 mH.

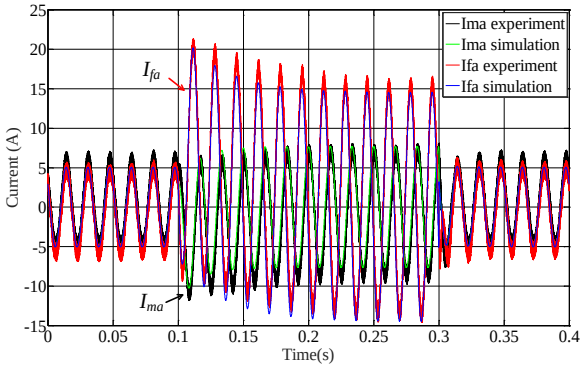
Figure 4-15(a) shows the experiment and simulation result comparison of I_a when the transmission line inductance and resistance are L = 8.5 mH (> 8.37 mH) and R = 0.25 Ω, respectively. The three-phase short-circuit fault happens at 0.1 s at the location γ = 0.71 (0.71 × 8.5 mH = 6.035 mH > 5.97 mH and 8.5 mH - 6.035 mH = 2.465 mH > 2.4 mH) when the phase angle of V_{mab} is 73°. Figure 4-15(b) and Figure 4-15(c) show the experiment and simulation result comparisons of I_a when the transmission line inductance and resistance are L = 10 mH (> 8.37 mH) and R = 0.3 Ω, respectively. Figure 4-15(b) is the case when a three-phase short-circuit fault happens at 0.1 s at the location γ = 0.6 (0.6 × 10 mH = 6 mH > 5.97 mH and 10 mH - 6 mH = 4 mH > 2.4 mH) when the phase angle of V_{mab} is 197°. Figure 4-15(c) is the case when a three-phase short-circuit fault happens at 0.1 s at the location γ = 0.75 (0.75 × 10 mH = 7.5 mH > 5.97 mH and 10 mH – 7.5 mH = 2.5 mH > 2.4 mH) when the phase angle of V_{mab} is 177°. The transmission line emulation is stable when (4-7) and (4-11) are satisfied.

4.5.2 Zero Resistive Fault Emulation of Parallel-connected Transmission Lines

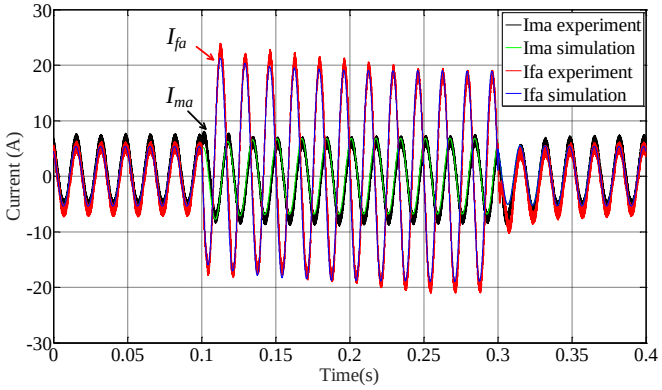
The system diagram for the parallel-connected transmission line experiment verification is shown in Figure 4-16. The equivalent inductance and resistance of all parallel-connected transmission lines are L and R, respectively. The equivalent inductance and resistance of the normal transmission lines are L_n and R_n, respectively, and the equivalent inductance and resistance of the faulted transmission lines are L_s and R_s, respectively, as shown in Figure 4-16. The three-phase short-circuit fault happens at the location γ ($0<\gamma<1$), which is the ratio of the distance from the fault location to the Master side terminal with regard to the total line length.



(a)



(b)



(c)

Figure 4-15. Single transmission line experiment and simulation comparison under non-ideal voltage sources condition: (a) L = 8.5 mH and γ = 0.71; (b) L = 10 mH and γ = 0.6; (c) L = 10 mH and γ = 0.75.

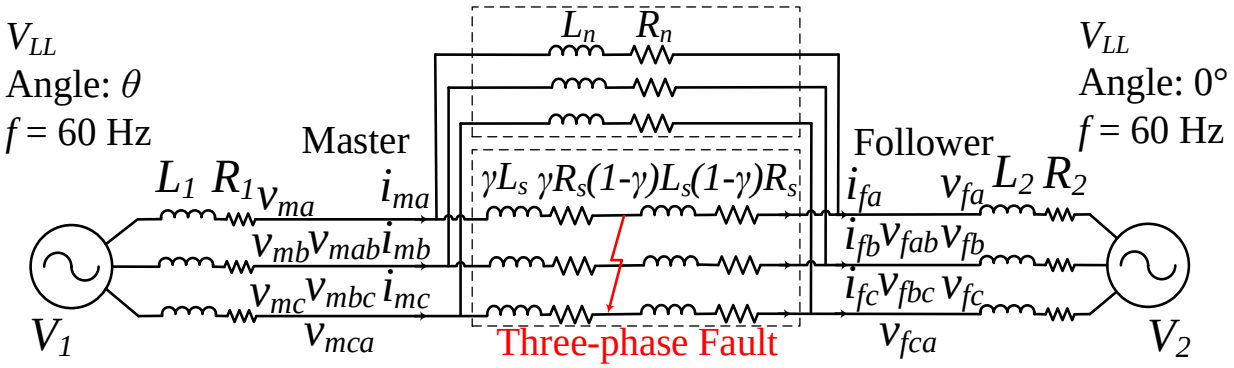


Figure 4-16. System topology for parallel-connected transmission lines experimental verification.

- Parallel-connected transmission lines connected with two ideal voltage sources scenario

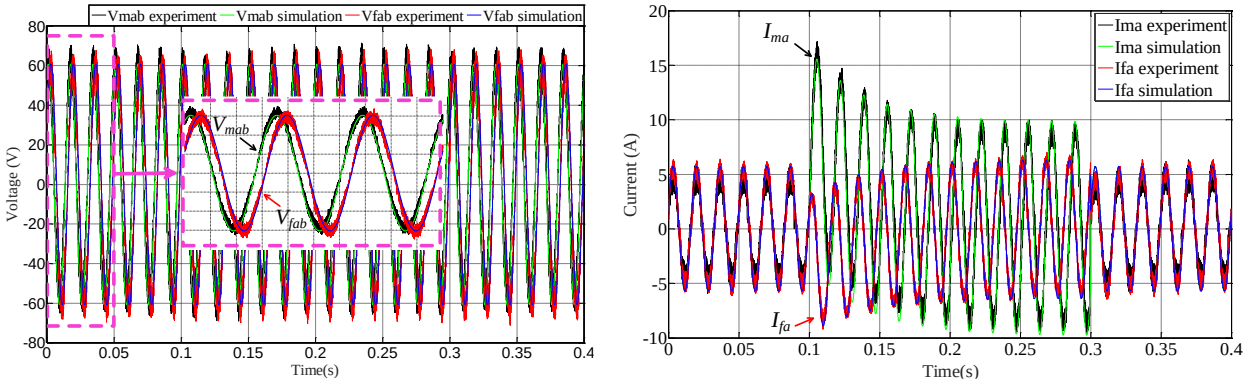
In order to verify the transmission line emulation performance by connecting to two ideal voltage sources, the voltage source impedances are set to zero (L_1, R_1, L_2, and R_2 equal to zero). A transmission line diagram with three parallel-connected transmission lines is selected to verify the fault emulation of parallel-connected transmission lines. The total inductance and resistance of three parallel–connected transmission lines are L = 12 mH and R = 0.3 Ω, respectively. The inductance and resistance of each transmission line are 36 mH and 0.9 Ω, respectively. Two of the transmission lines are normal and the three-phase short-circuit fault happens within one of the transmission lines. Thus, the normal line inductance and resistance are L_n = 18 mH and R_n = 0.45 Ω, respectively. Three fault scenarios with γ equals to 1/3, 1/2, and 2/3, respectively are tested to verify the three-phase short-circuit fault emulation capability at different locations within the emulated transmission line.

e) Three-phase short-circuit fault with γ = 1/3

A three-phase short-circuit fault happens at 0.1 s and cleared at 0.3 s at the location γ = 1/3 when the phase angle of V_{mab} is 65°. The angle difference between the two voltage sources is $\theta = \theta_{V1} - \theta_{V2}$ = 43°. Figure 4-17(a) and Figure 4-17(b) show the experiment and simulation result comparisons of V_{ab} and I_a, respectively, which indicate that the experimental waveforms match well with the simulation results.

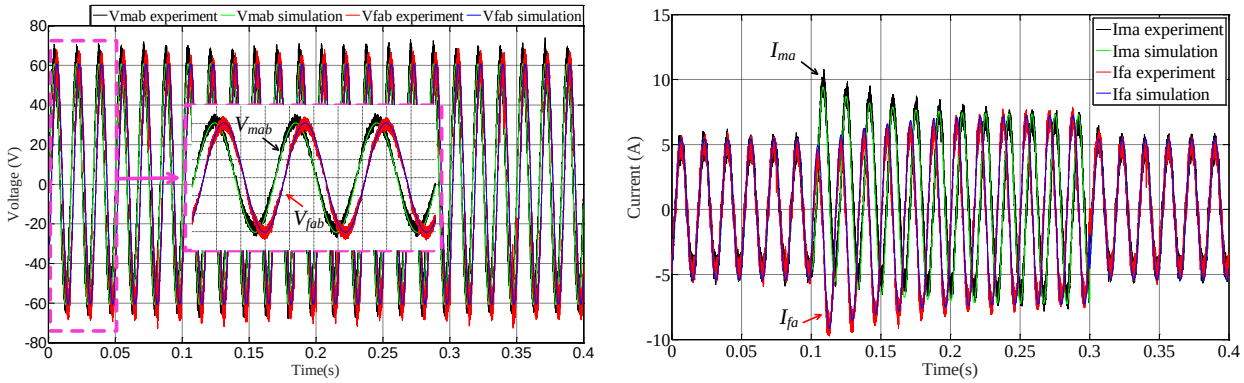
f) Three-phase short-circuit fault with γ = 1/2

A three-phase fault happens at 0.1 s and cleared at 0.3 s at the location γ = 1/2 when the phase angle of V_{mab} is 350°. The angle difference between the two voltage sources is $\theta = \theta_{V1} - \theta_{V2}$ = 41°. Figure 4-18(a) and Figure 4-18(b) show the experiment and simulation comparisons of V_{ab} and I_a, respectively, which indicate that the experimental results match well with the simulation results.



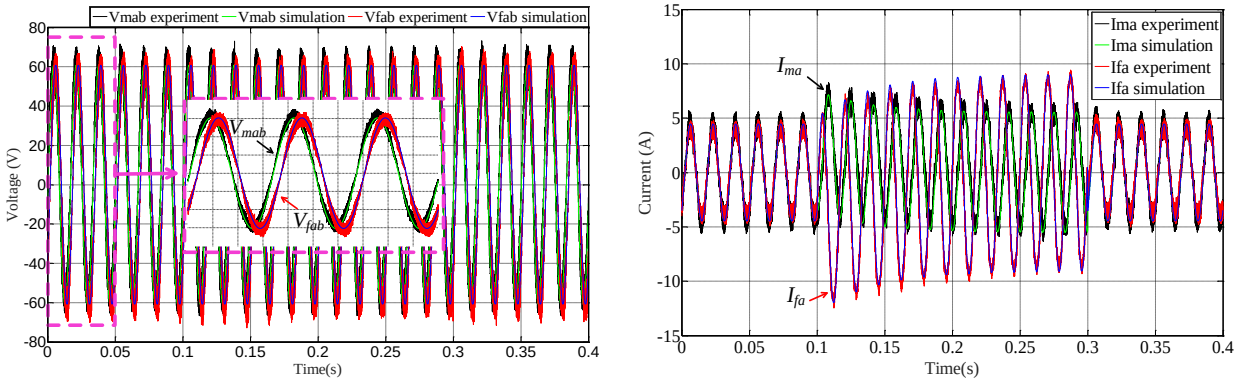
(a) (b)

Figure 4-17. Parallel-connected lines experiment results with γ = 1/3: (a) V_{ab}; (b) I_a.



(a) (b)

Figure 4-18. Parallel-connected lines experiment results with γ = 1/2: (a) V_{ab}; (b) I_a.



(a) (b)

Figure 4-19. Parallel-connected lines experiment results with γ = 2/3: (a) V_{ab}; (b) I_a.

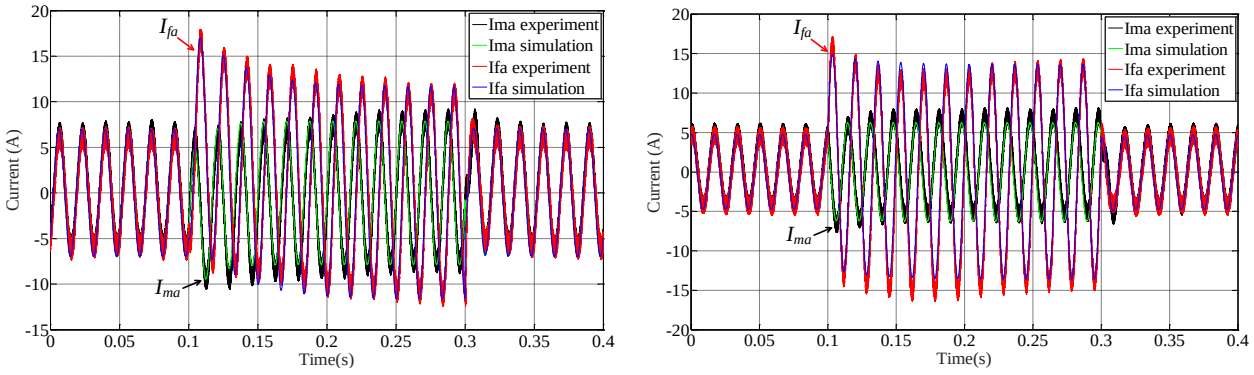
g) Three-phase short-circuit fault with $\gamma = 2/3$

A three-phase short-circuit fault happens at 0.1 s at the location $\gamma = 2/3$ when the phase angle of V_{mab} is 350°. The angle difference between the two voltage sources is $\theta = \theta_{V1} - \theta_{V2} = 33°$. The fault is cleared at 0.3 s. Figure 4-19(a) and Figure 4-19(b) show the experiment and simulation result comparisons of V_{ab} and I_a, respectively, which indicate that the experimental waveforms match with the simulation results.

- Parallel-connected transmission lines connected with two non-ideal voltage sources scenario

To verify the parallel-connected transmission line emulation stability, two non-ideal voltage sources are connected with the transmission line by setting the voltage source impedances L_1 to 5.97 mH, R_1 to 0.65 Ω, L_2 to 2.4 mH, and R_2 to 0.07 Ω. The whole transmission line equivalent inductance and resistance are L = 8.5 mH and R = 0.25 Ω, respectively. The normal transmission line equivalent inductance and resistance are L_n = 17 mH and R_n = 0.5 Ω, respectively. The faulted line equivalent inductance and resistance are L_n = 17 mH and R_n = 0.5 Ω, respectively.

Figure 4-20(a) and Figure 4-20(b) show the experiment and simulation result comparisons of I_a when a three-phase short-circuit fault happens at 0.1 s with the fault location γ equals to 0.5 and 0.7, respectively. Similarly, the inductance is employed to judge the transmission line emulation stability. When γ equals to 0.5, $(L_1 \parallel \gamma L_s) + (L_2 \parallel (1-\gamma) L_s) = 5.38$ mH < L_n = 17 mH satisfies (4-12), $((L_2 \parallel (1-\gamma) L_s + L_n) \parallel L_1 = 4.54$ mH < γL_s = 8.5 mH satisfies (4-13), and $((L_1 \parallel \gamma L_s) + L_n) \parallel L_2 = 2.15$ mH < $(1-\gamma)L_s$ = 8.5 mH satisfies (4-14). When γ equals to 0.7, $(L_1 \parallel \gamma L_s) + (L_2 \parallel (1-\gamma) L_s) = 5.61$ mH < L_n = 17 mH satisfies (4-12), $((L_2 \parallel (1-\gamma)L_s + L_n) \parallel L_1 = 4.52$ mH < γL_s = 11.90 mH satisfies (4-13), and $((L_1 \parallel \gamma L_s) + L_n) \parallel L_2 = 2.15$ mH < $(1-\gamma)L_s$ = 5.1 mH satisfies (4-14). The transmission line emulation is stable when (4-12), (4-13), and (4-14) are satisfied.

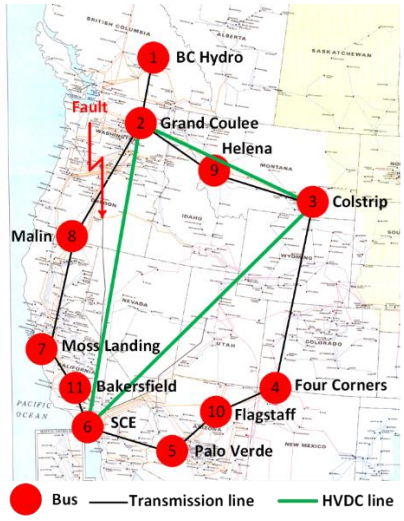


(a) (b)

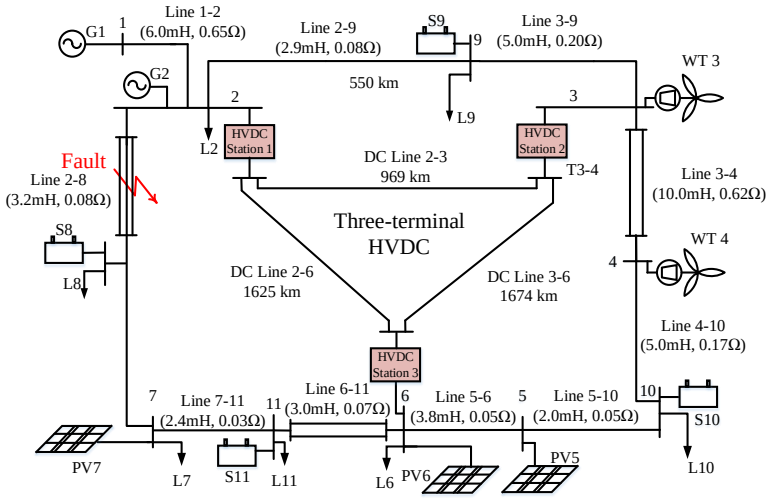
Figure 4-20. Parallel-connected transmission line experiment and simulation comparison under non-ideal voltage sources condition: (a) L = 8.5 mH and γ = 0.5; (b) L = 8.5 mH and γ = 0.7.

4.5.3 Transmission Line Fault Emulation Application in Real System Scenario

The simplified future Western Electricity Coordinating Council (WECC) system with a hypothetical three-terminal HVDC overlay in Figure 4-21 is scaled and emulated in the HTB for system studies. The transmission line between Bus 2 and Bus 8, named as Line 2-8, is emulated by the transmission line emulator. Line 2-8 is composed of three parallel-connected transmission lines, and the scaled total equivalent inductance and resistance are 3.2 mH and 0.08 Ω, respectively. The transmission line emulator Master side and Follower side are connected to Bus 2 and Bus 8, respectively. The fault location γ represents the ratio of the distance from the fault location to Bus 2 with regard to the total line length. The transmission line emulator is employed to study the impacts of the fault location and the number of faulted lines on the system behaviors.



(a)



(b)

Figure 4-21. WECC system with a hypothetical three-terminal HVDC overlay: (a) One-line diagram with the corresponding map; (b) One-line diagram with generators, loads, and transmission line parameters shown.

- Fault location impact study

A three-phase short-circuit fault happens at the location γ in one of the three parallel-connected transmission lines. Figure 4-22 shows the transmission line terminal voltages and currents. The channel "F1" and "F2" are V_{ab} and V_{bc} at the terminal of Bus 2. The channel "F3" and "F4" are V_{ab} and V_{bc} at the terminal of Bus 8. The channel "F5" and "F7" are I_a and I_b at the terminal of Bus 2. The channel "F6" and "F8" are I_a and I_b at the terminal of Bus 8. Fig. 30(a) and (b) are the waveforms with the fault location γ = 0.33 and γ = 0.67, respectively. According to the waveforms, the fault currents at the terminal of Bus 2 decreases as the fault location γ increases, and the fault currents at the terminal of Bus 8 increases as the fault location γ increases. The Bus 8 voltage decreases as the fault location γ increases. The Bus 2 voltage does not change much during the fault as the increase of the fault location γ. This is because Bus 2 is supported by a generator G_2, which maintains the terminal voltage by the excitation control.

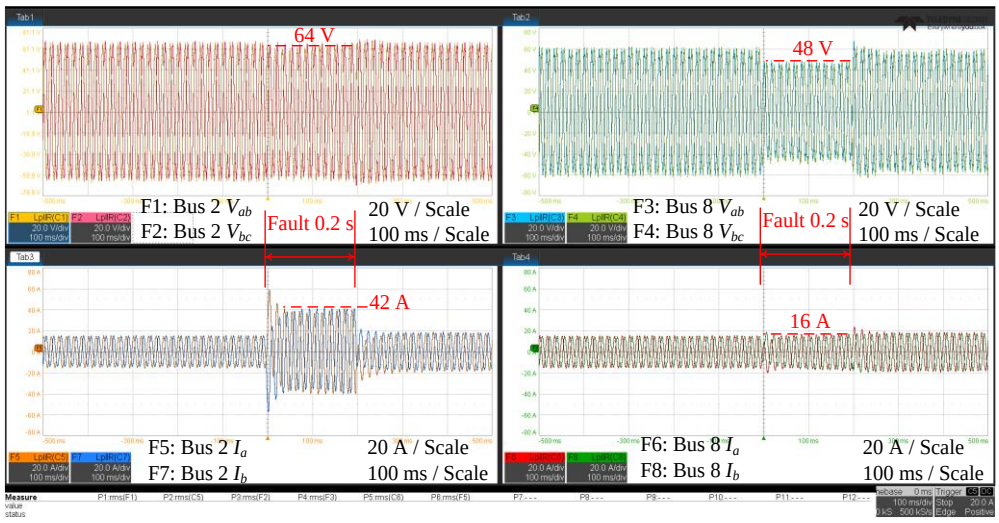
- System impact study with different number of faulted lines

Two cases are conducted where a three-phase short-circuit fault happens at the middle (γ = 0.5) of the transmission line for 0.4 s fault duration.

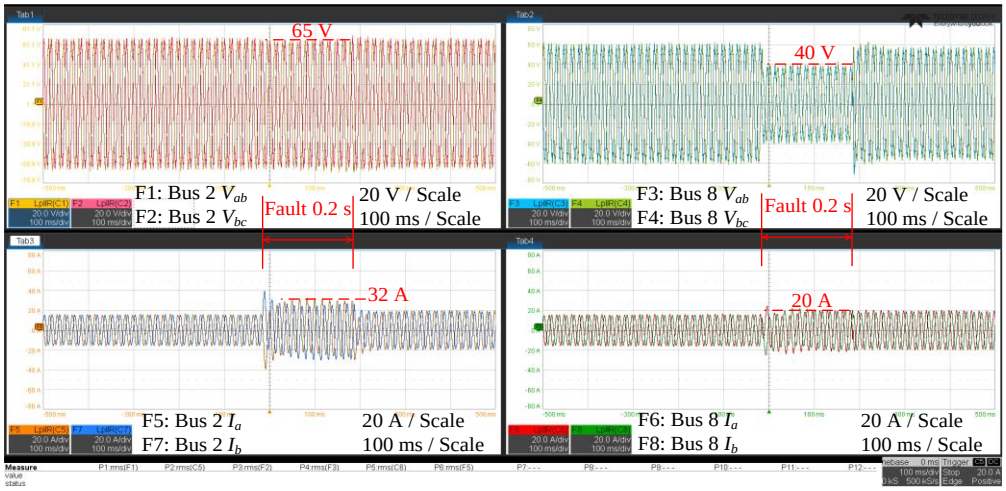
Case 1 (One line fault): the fault happens in one of the three parallel-connected transmission lines.

Case 2 (two lines fault): the fault happens in two of the three parallel-connected transmission lines.

Figure 4-23(a) and (b) show system frequency and Bus 8 voltage comparisons between one line and two lines fault cases, and the fault happens at 2 s. The two lines fault creates larger impact on the system since the frequency and voltage deviations during the transient are large.

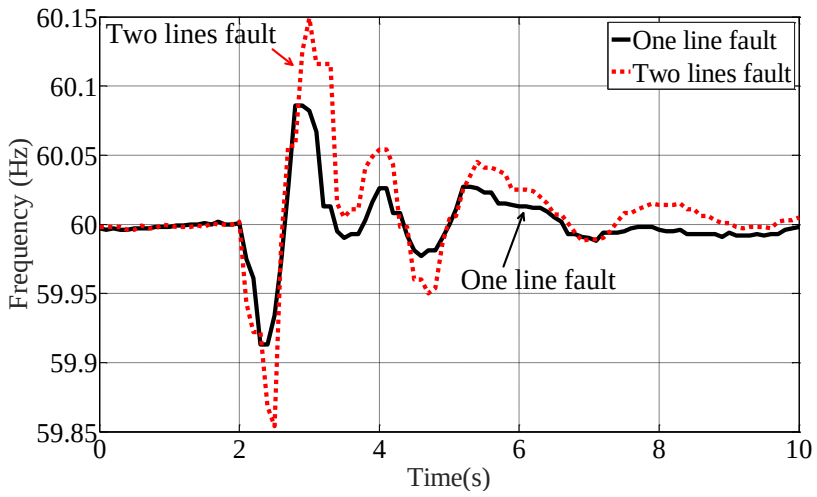


(a)

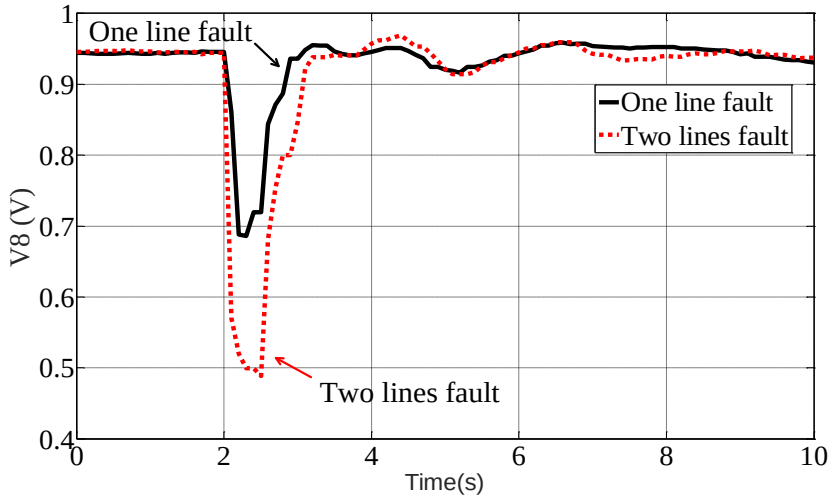


(b)

Figure 4-22. Transmission line terminal voltage and current waveforms under a three-phase short-circuit fault at different locations within one of the three parallel-connected transmission lines: (a) γ = 0.33; (b) γ = 0.67.



(a)



(b)

Figure 4-23. System performance comparisons between one line fault and two lines fault of the three parallel-connected transmission lines: (a) System frequency comparison; (b) Bus 8 voltage comparison

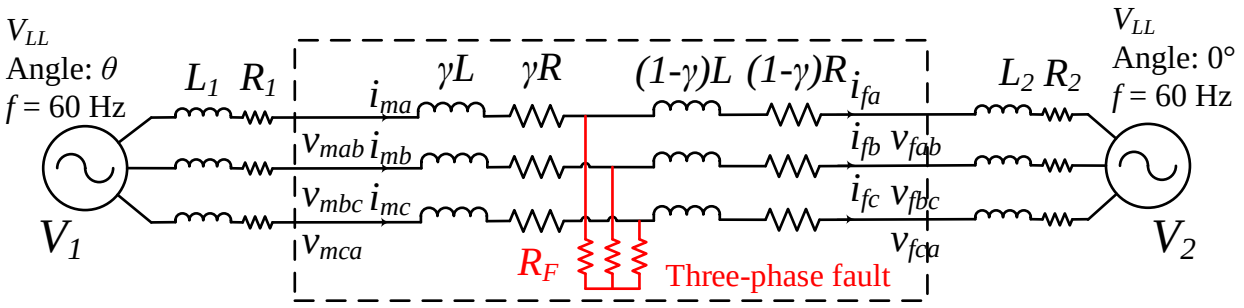


Figure 4-24. System topology for single line experimental verification.

4.5.4 Non-zero Resistive Fault Emulation of a Single Transmission Line

The experiment verification system diagram of a single transmission line with a non-zero resistive three-phase fault is shown in Figure 4-24. The transmission line inductance and resistance are L and R, respectively.

The three-phase short-circuit fault with fault resistance R_F happens at the location γ ($0<\gamma<1$), which is the ratio of the distance from the fault location to the Master side terminal with regard to the total line length.

In order to verify the single transmission line emulation with a non-zero resistive three-phase fault, two non-ideal voltage sources are connected with the transmission line by setting the voltage source impedances L_1 to 5.97 mH, R_1 to 0.65 Ω, L_2 to 2.4 mH, and R_2 to 0.07 Ω. The transmission line inductance and resistance are selected as 5 mH and 0.5 Ω, respectively.

a) Three-phase short-circuit fault with γ = 0.3 and R_F = 1 Ω

A three-phase short-circuit fault with R_F = 1 Ω happens at 0.1 s at the location γ = 0.3 when the phase angle of V_{mab} is 358°. The angle difference between the two voltage sources is $\theta = \theta_{V1}$

– θ_{V2} = 304°. The fault is cleared at 0.3 s. Figure 4-25(a) and (b) show the experiment and simulation result comparisons of I_a and I_b, respectively, which indicate that the experimental waveforms match well with the simulation results.

b) Three-phase short-circuit fault with γ = 0.3 and R_F = 2 Ω

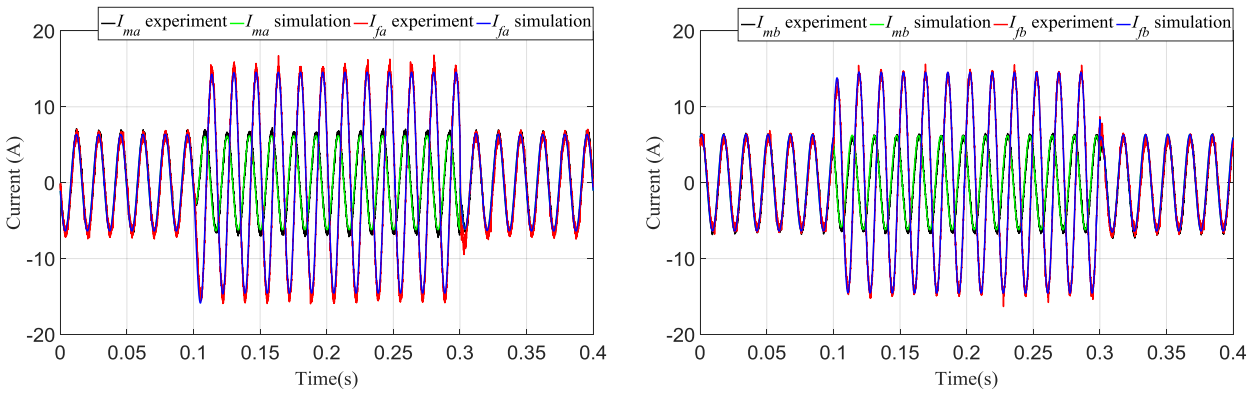
A three-phase short-circuit fault with R_F = 2 Ω happens at 0.1 s at the location γ = 0.3 when the phase angle of V_{mab} is 118°. The angle difference between the two voltage sources is $\theta = \theta_{V1} - \theta_{V2}$ = 75°. The fault is cleared at 0.3 s. Figure 4-26(a) and Figure 4-26(b) show the experiment and simulation result comparisons of V_{ab} and I_a, respectively, which indicate that the experimental waveforms match well with the simulation results.

c) Three-phase short-circuit fault with γ = 0.4 and R_F = 1 Ω

A three-phase short-circuit fault with R_F = 1 Ω happens at 0.1 s at the location γ = 0.4 when the phase angle of V_{mab} is 65°. The angle difference between the two voltage sources is $\theta = \theta_{V1} - \theta_{V2}$ = -307°. The fault is cleared at 0.3 s. Figure 4-27(a) and Figure 4-27(b) show the experiment and simulation result comparisons of V_{ab} and I_a, respectively, which indicate that the experimental waveforms match well with the simulation results.

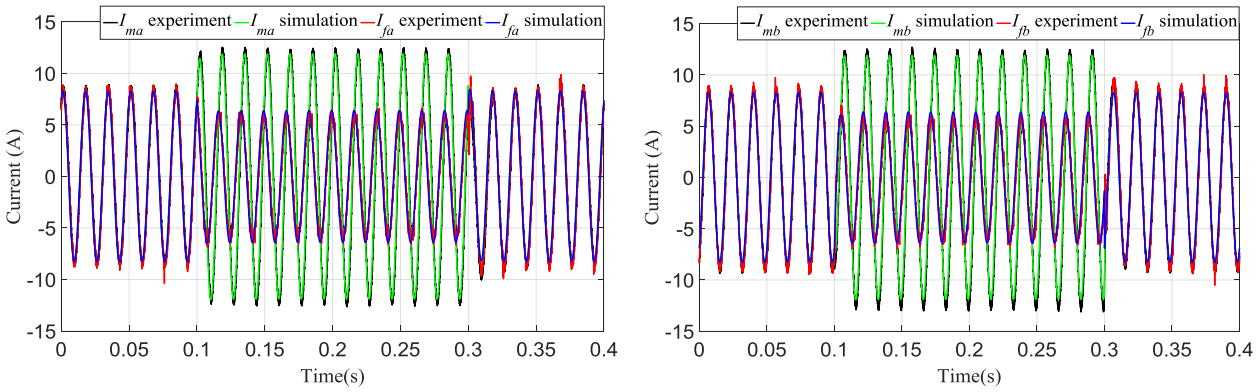
d) Three-phase short-circuit fault with γ = 0.4 and R_F = 2 Ω

A three-phase short-circuit fault with R_F = 2 Ω happens at 0.1 s at the location γ = 0.4 when the phase angle of V_{mab} is -57°. The angle difference between the two voltage sources is $\theta = \theta_{V1} - \theta_{V2}$ = 156°. The fault is cleared at 0.3 s. Figure 4-28(a) and Figure 4-28(b) show the experiment and simulation result comparisons of V_{ab} and I_a, respectively, which indicate that the experimental waveforms match well with the simulation results.



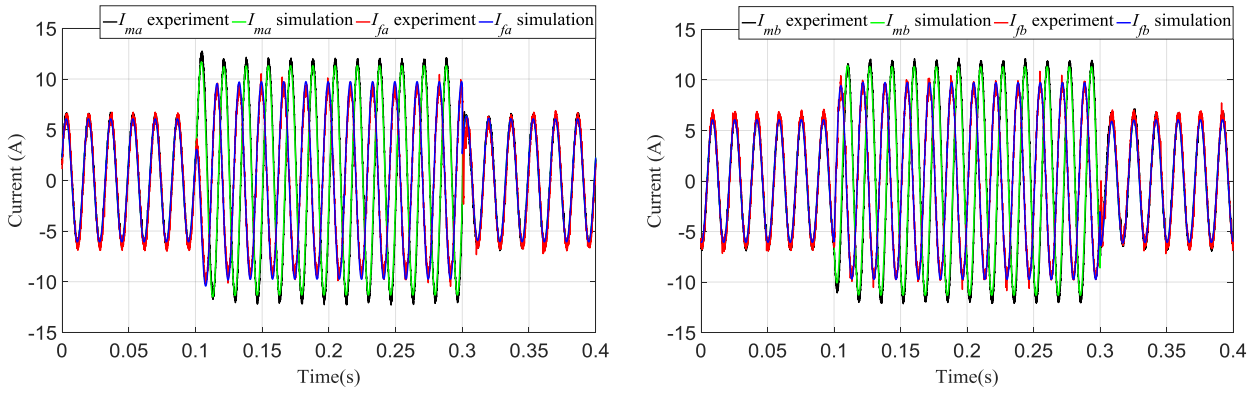
(a) (b)

Figure 4-25. Single transmission line experiment and simulation comparison with γ = 0.3 and R_F = 1 Ω: (a) I_a; (b) I_b.



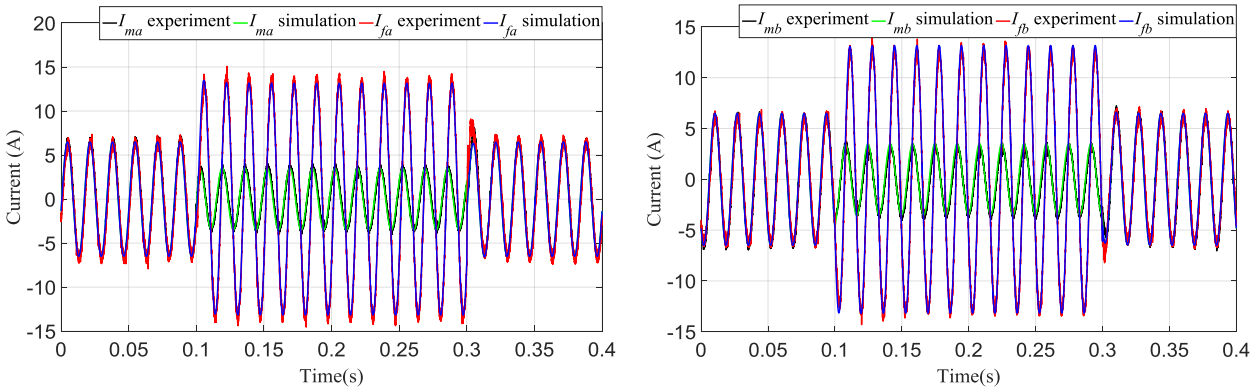
(a) (b)

Figure 4-26. Single transmission line experiment and simulation comparison with γ = 0.3 and R_F = 2 Ω: (a) V_{ab}; (b) I_a.



(a) (b)

Figure 4-27. Single transmission line experiment and simulation comparison with γ = 0.4 and R_F = 1 Ω: (a) V_{ab}; (b) I_a.



(a) (b)

Figure 4-28. Single transmission line experiment and simulation comparison with γ = 0.4 and R_F = 2 Ω: (a) V_{ab}; (b) I_a.

4.6 Conclusion

The fault model of a single transmission line has been proposed to realize three-phase short-circuit fault emulation at different locations along the emulated transmission line. By switching the input of the integrator for current reference calculation, a combined transmission line model is proposed to avoid the switching transient between the normal and fault conditions. Furthermore, the fault model of parallel-connected transmission lines has also been proposed and implemented in the transmission line emulator to emulate a three-phase short-circuit fault within one of the parallel-connected transmission lines. In addition, the transmission line emulation stability is also analyzed for both single and parallel connected transmission lines. Experiment results verified the proposed transmission line model and the effectiveness of the developed transmission line emulator with three-phase short-circuit fault emulation capability.

5 Transmission Line Emulation with an Unbalanced Fault

In this chapter, the algorithm of transmission line emulation with an unbalanced fault is proposed based on the circuit analysis. A negative sequence current control method is proposed and implemented to track the negative component of the current references under an unbalanced fault condition.

A time delay correction method is also developed to compensate the interface time delay within the transmission line emulation, which creates an angle shift on the current negative sequence component under *dq0* domain and influences the emulation accuracy. Simulation and experiment results verified the effectiveness of the proposed model, negative sequence control method, and time-delay correction scheme.

5.1 Line-to-Line Fault Model

The transmission line RL model with a line-to-line fault is shown in Figure 5-1 where R_F is the fault resistance. The parameter γ ($0 < \gamma < 1$) is the percentage of the distance from the fault location "o" to the Master side terminal with regard to the total line length.

The transmission line model with a line-to-line fault is expressed in (5-1).

$$\begin{cases} v_{mfa} = v_{ma} - v_{fa} = L\dfrac{di_a}{dt} + Ri_a \\ v_{mb} - v_{ob} = \gamma L\dfrac{di_{mb}}{dt} + \gamma Ri_{mb} \\ v_{fb} - v_{ob} = -(1-\gamma)L\dfrac{di_{fb}}{dt} - (1-\gamma)Ri_{fb} \\ v_{mc} - v_{ob} + R_F(i_{mb} - i_{fb}) = \gamma L\dfrac{di_{mc}}{dt} + \gamma Ri_{mc} \\ v_{fc} - v_{ob} + R_F(i_{mb} - i_{fb}) = -(1-\gamma)L\dfrac{di_{fc}}{dt} - (1-\gamma)Ri_{fc} \end{cases} \tag{5-1}$$

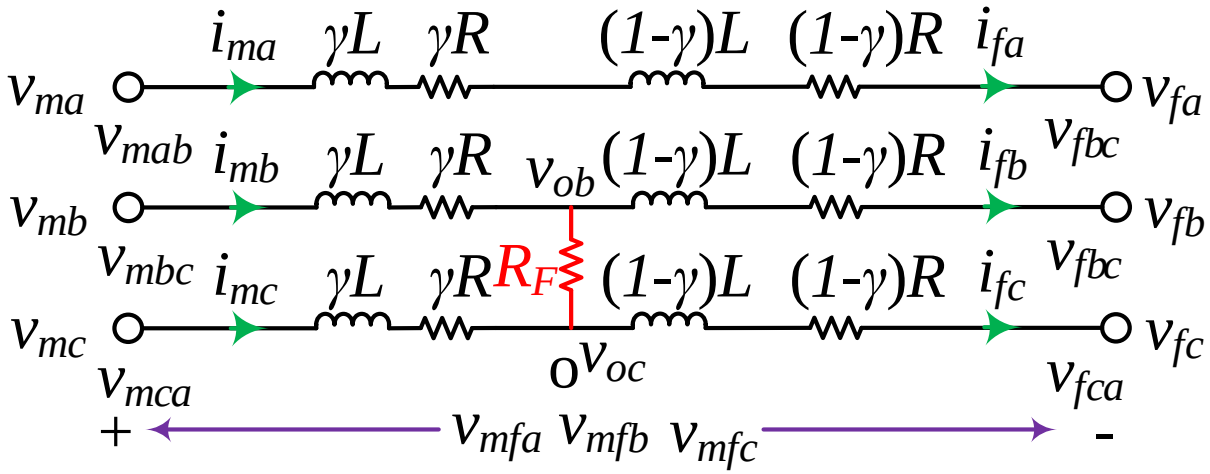


Figure 5-1. Transmission line with a line-to-line fault.

Solve (5-1), get (5-2).

$$\begin{cases} v_a = v_{ma} - v_{fa} = L\dfrac{di_a}{dt} + Ri_a \\ v_{mbc} = v_{mb} - v_{mc} = \gamma L\dfrac{d(i_{mb} - i_{mc})}{dt} + \gamma R(i_{mb} - i_{mc}) + R_F(i_{mb} - i_{fb}) \\ v_{fbc} = v_{fb} - v_{fc} = -(1-\gamma)L\dfrac{d(i_{fb} - i_{fc})}{dt} - (1-\gamma)R(i_{fb} - i_{fc}) + R_F(i_{mb} - i_{fb}) \end{cases} \tag{5-2}$$

By measuring the terminal voltages, the current references can be derived from (5-3).

$$\begin{cases} i_{maref} = i_{faref} = i_{aref} = \displaystyle\int \frac{v_{ma} - v_{fa} - Ri_a}{L}dt \\ i_{mbcref} = i_{mbref} - i_{mcref} = \displaystyle\int \frac{v_{mbc} - \gamma Ri_{mbc} - R_F(i_{mb} - i_{fb})}{\gamma L}dt \\ i_{fbcref} = i_{fbref} - i_{fcref} = \displaystyle\int \frac{-v_{fbc} - (1-\gamma)Ri_{fbc} + R_F(i_{mb} - i_{fb})}{(1-\gamma)L}dt \end{cases} \tag{5-3}$$

For a three-phase three-wire system, the current relationship is expressed in (5-4).

$$i_{maref} + i_{mbref} + i_{mcref} = i_{faref} + i_{fbref} + i_{fcref} = 0 \tag{5-4}$$

Submit (5-4) into (5-3), get (5-5).

$$\begin{cases} i_{maref} = i_{faref} = i_{aref} = \int \dfrac{v_{ma} - v_{fa} - Ri_a}{L} dt \\ i_{mbref} = \dfrac{\int \dfrac{v_{mbc} - \gamma R i_{mbc} - R_F(i_{mb} - i_{fb})}{\gamma L} dt - \int \dfrac{v_{ma} - v_{fa} - Ri_a}{L} dt}{2} \\ i_{fbref} = \dfrac{\int \dfrac{-v_{fbc} - (1-\gamma) R i_{fbc} + R_F(i_{mb} - i_{fb})}{(1-\gamma)L} dt - \int \dfrac{v_{ma} - v_{fa} - Ri_a}{L} dt}{2} \\ i_{mcref} = \dfrac{-\int \dfrac{v_{mbc} - \gamma R i_{mbc} - R_F(i_{mb} - i_{fb})}{\gamma L} dt - \int \dfrac{v_{ma} - v_{fa} - Ri_a}{L} dt}{2} \\ i_{fcref} = \dfrac{\int \dfrac{v_{fbc} + (1-\gamma) R i_{fbc} - R_F(i_{mb} - i_{fb})}{(1-\gamma)L} dt - \int \dfrac{v_{ma} - v_{fa} - Ri_a}{L} dt}{2} \end{cases} \tag{5-5}$$

Simplify (5-5), get (5-6).

$$\begin{cases} i_{maref} = i_{faref} = i_{aref} = \int \dfrac{v_{ma} - v_{fa} - Ri_a}{L} dt \\ i_{mbref} = \int \dfrac{v_{mbc} - \gamma R i_{mbc} - \gamma(v_{ma} - v_{fa}) + \gamma R i_a - R_F(i_{mb} - i_{fb})}{2\gamma L} dt \\ i_{fbref} = \int \dfrac{-v_{fbc} - (1-\gamma) R i_{fbc} - (1-\gamma)(v_{ma} - v_{fa}) + (1-\gamma) R i_a + R_F(i_{mb} - i_{fb})}{2(1-\gamma)L} dt \\ i_{mcref} = \int \dfrac{-v_{mbc} + \gamma R i_{mbc} - \gamma(v_{ma} - v_{fa}) + \gamma R i_a + R_F(i_{mb} - i_{fb})}{2\gamma L} dt \\ i_{fcref} = \int \dfrac{v_{fbc} + (1-\gamma) R i_{fbc} - (1-\gamma)(v_{ma} - v_{fa}) + (1-\gamma) R i_a + R_F(i_{mb} - i_{fb})}{2(1-\gamma)L} dt \end{cases} \tag{5-6}$$

Thus, the emulation algorithm of a transmission line with a line-to-line fault is derived as shown in Figure 5-2.

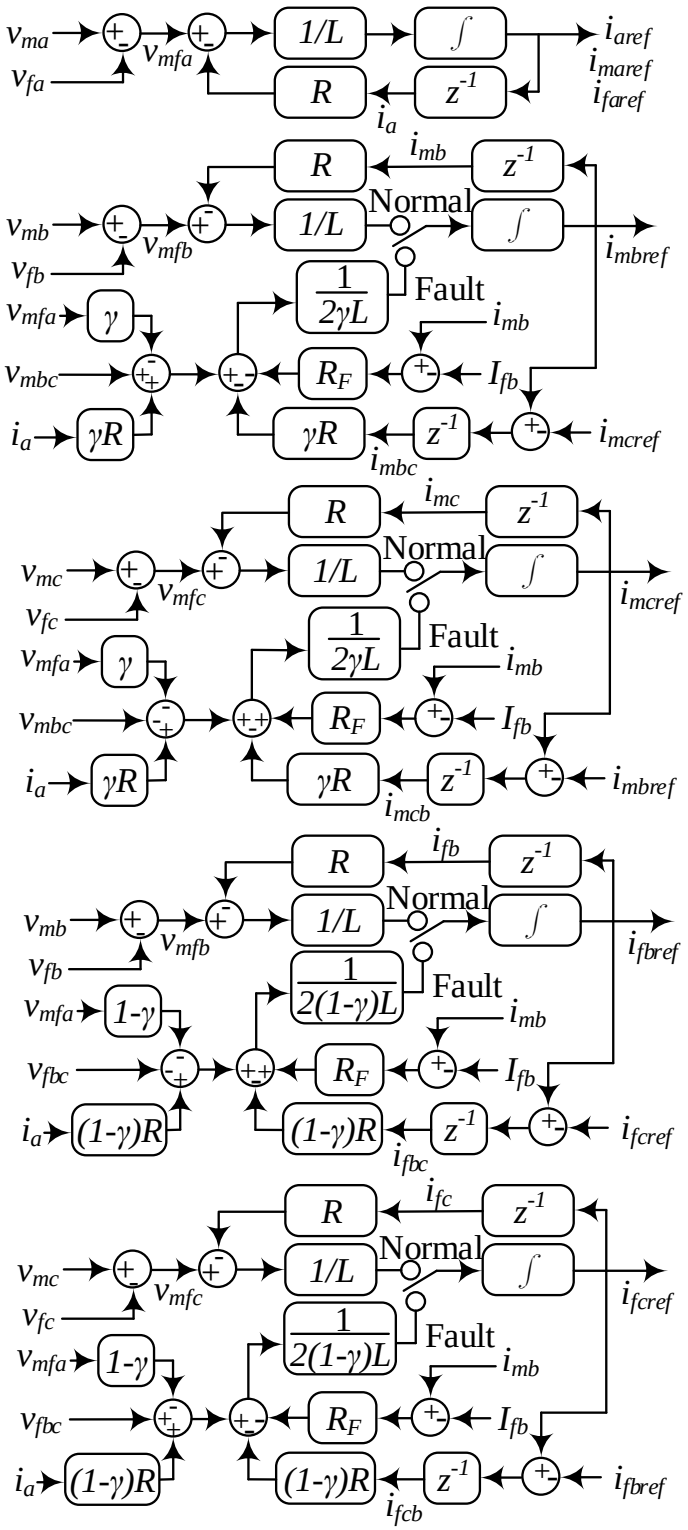


Figure 5-2. Transmission line with a line-to-line fault emulation algorithm.

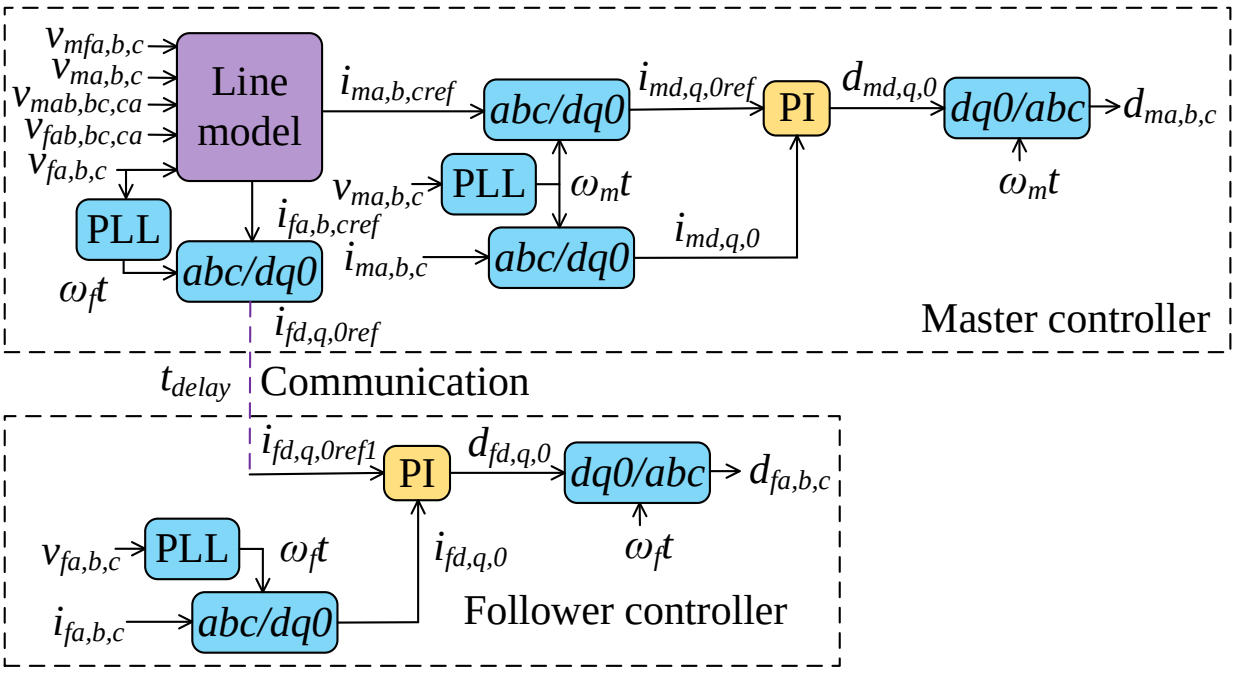


Figure 5-3. Transmission line emulator control structure.

5.2 Negative Sequence Control and Time-delay Correction

The transmission line emulator detailed control structure corresponding to Figure 3-1(a) is shown in Figure 5-3. The Master and Follower current references $i_{ma,b,c,ref}$ and $i_{fa,b,c,ref}$ are derived in the Master controller from the transmission line model based on the measured Master and Follower side voltages $v_{mfa,b,c}$, $v_{ma,b,c}$, $v_{mab,bc,ca}$, $v_{fab,bc,ca}$, and $v_{fa,b,c}$.

Proportional-integral (PI) controllers under *dq0* coordinate are implemented to track the current references. The Master and Follower side voltages $v_{ma,b,c}$ and $v_{fa,b,c}$ are utilized to acquire the phase angle $w_m t$ and $w_f t$ for Master and Follower sides' Park's transformations (*abc*/*dq0* and *dq0*/*abc*), respectively. The Follower side current references $i_{fa,b,cref}$ are transferred to $i_{fd,q,0ref}$ in the Master controller through the *abc*/*dq0* transformation, and then transmitted to the Follower controller through communication.

Under balanced conditions, the current references $i_{md,q,0ref}$ and $i_{fd,q,0ref}$ are pure dc components, which can be tracked with PI controllers without errors. Thus, transmission lines can be emulated accurately under balanced conditions by using PI controllers in *dq0* domain. However, negative sequence components in the current references $i_{ma,b,cref}$ and $i_{fa,b,cref}$ would be induced by a transmission line line-to-line fault. These negative sequence components are transferred to a second order harmonic in the *dq0* domain references $i_{md,q,0ref}$ and $i_{fd,q,0ref}$, which cannot be tracked without errors by purely using PI controllers.

In this dissertation, a negative sequence control algorithm is proposed to eliminate the current tracking errors for both Master and Follower side controllers caused by negative sequence components, as shown in Figure 5-4.

The phase B and phase C of current references $i_{ma,b,cref}$, $i_{fa,b,cref}$ and feedbacks $i_{ma,b,c}$, $i_{fa,b,c}$ are switched so as the negative sequence components become positive sequence components in the restructured current references $i_{ma,c,bref}$, $i_{fa,c,bref}$ and feedbacks $i_{ma,c,b}$, $i_{fa,c,b}$. Then, the original negative sequence components are transferred to dc components in the *dq0* domain, which can be tracked without errors by using PI controllers. The *dq0* domain modulation indexes are transferred back to the *abc* domain. The phase B and phase C modulation indexes from the negative sequence control block are switched back and added into the original control outputs.

Except for the negative sequence component tracking control, the second order harmonic phase-shift of the Follower side current references $i_{fd,q,0ref}$ caused by the communication time-delay between the Master controller and Follower controller can also influence the emulation accuracy.

Under balanced conditions, the communication time-delay would not influence the steady-

state performances since the current references $i_{fd,q,0ref}$ are dc components. However, the time-delay performs as a phase-shift on the second order harmonic of $i_{fd,q,0ref}$ induced by a line-to-line fault.

The Park's *abc*/*dq0* and *dq0*/*abc* transformation matrixes are expressed in (5-7) and (5-8), respectively.

$$P = \frac{2}{3}\begin{bmatrix} \cos(\omega_f t) & \cos\left(\omega_f t - \frac{2\pi}{3}\right) & \cos\left(\omega_f t + \frac{2\pi}{3}\right) \\ \sin(\omega_f t) & \sin\left(\omega_f t - \frac{2\pi}{3}\right) & \sin\left(\omega_f t + \frac{2\pi}{3}\right) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \tag{5-7}$$

$$P^{-1} = \begin{bmatrix} \cos\left(\omega_f (t-\Delta T)\right) & \sin\left(\omega_f (t-\Delta T)\right) & 1 \\ \cos\left(\omega_f (t-\Delta T) - \frac{2\pi}{3}\right) & \sin\left(\omega_f (t-\Delta T) - \frac{2\pi}{3}\right) & 1 \\ \cos\left(\omega_f (t-\Delta T) + \frac{2\pi}{3}\right) & \sin\left(\omega_f (t-\Delta T) + \frac{2\pi}{3}\right) & 1 \end{bmatrix} \tag{5-8}$$

Under balanced conditions, the Follower side current reference is a positive sequence component expressed in (5-9).

$$I_{fa,b,crefpos} = I_{pos}\left[\cos(\omega_f t - \theta_{pos}) \quad \cos(\omega_f t - \theta_{pos} - \frac{2\pi}{3}) \quad \cos(\omega_f t - \theta_{pos} + \frac{2\pi}{3})\right]^T \tag{5-9}$$

where I_{pos} and θ_{pos} are the positive sequence component magnitude and phase angle, respectively.

The current reference positive component after *dq0* transformation are expressed in (5-10).

$$I_{fd,q,0refpos} = PI_{fa,b,crefpos} = I_{pos}[\cos\theta_{pos} \quad \sin\theta_{pos} \quad 0]^T \tag{5-10}$$

The current reference positive component after the communication delay t_{delay} keeps the

same, as expressed in (5-11).

$$I_{fd,q,0ref1pos} = I_{pos}[\cos\theta_{pos} \quad \sin\theta_{pos} \quad 0]^T \tag{5-11}$$

Transfer the current reference positive component after communication back to *abc* domain, as expressed in (5-12), which is the same as the original current reference positive component.

$$I_{fa,b,cref1pos} = P^{-1} I_{fd,q,0ref1pos} = I_{fa,b,crefpos} \tag{5-12}$$

Under line-to-line fault conditions, the Follower side current references contain a negative sequence component, as expressed in (5-13).

$$I_{fa,b,crefneg} = I_{neg}\left[\cos(\omega_f t - \theta_{neg}) \quad \cos(\omega_f t - \theta_{neg} + \frac{2\pi}{3}) \quad \cos(\omega_f t - \theta_{neg} - \frac{2\pi}{3})\right]^T \tag{5-13}$$

where I_{neg} and θ_{neg} are the negative sequence component magnitude and phase angle, respectively.

The current reference negative component after *dq0* transformation is expressed in (5-14).

$$I_{fd,q,0refneg} = PI_{fa,b,crefneg} = I_{neg}[\cos(2\omega_f t - \theta_{neg}) \quad \sin(2\omega_f t - \theta_{neg}) \quad 0]^T \tag{5-14}$$

The current reference negative components after the communication time-delay t_{delay} is expressed in (5-15).

$$I_{fd,q,0ref1neg} = I_{neg}\left[\cos\left(2\omega_f t - 2\omega_f t_{delay} - \theta_{neg}\right) \quad \sin\left(2\omega_f t - 2\omega_f t_{delay} - \theta_{neg}\right) \quad 0\right]^T \tag{5-15}$$

Transfer the current reference negative component after communication back to *abc* domain, as expressed in (5-16), which indicates that the communication time-delay induces $2\omega_f t_{delay}$ phase

angle delay on the current reference negative sequence component.

$$I_{fa,b,cref1neg} = P^{-1} I_{fd,q,0ref1neg} = I_{neg} \begin{bmatrix} \cos(\omega_f t - \theta_{neg} - 2\omega_f t_{delay}) \\ \cos\left(\omega_f t - \theta_{neg} + \frac{2\pi}{3} - 2\omega_f t_{delay}\right) \\ \cos\left(\omega_f t - \theta_{neg} - \frac{2\pi}{3} - 2\omega_f t_{delay}\right) \end{bmatrix} \tag{5-16}$$

To eliminate the negative sequence component phase-shift caused by the communication time-delay, a time-delay compensation method is proposed and implemented in the Follower controller, as shown in Figure 5-4.

According to the above analysis, the positive sequence component has no phase-shift if the received Follower side current reference $i_{fd,q,0ref1}$ is transferred to *abc* domain through a regular *dq0*/*abc* transformation. Thus, only the negative sequence component is introduced into the time-delay compensation block by using a bandpass filter (BPF) with a center frequency $2\omega_f$.

For the time-delay compensation block, the compensation phase angle $\omega_f t_{comp}$ and magnitude ratio σ are applied on the *dq0* to *abc* transformation, which is expressed in (5-17).

$$P_{comp}^{-1} = \sigma \begin{bmatrix} \cos\left(\omega_f(t - t_{comp})\right) & \sin\left(\omega_f(t - t_{comp})\right) & 1 \\ \cos\left(\omega_f(t - t_{comp}) - \frac{2\pi}{3}\right) & \sin\left(\omega_f(t - t_{comp}) - \frac{2\pi}{3}\right) & 1 \\ \cos\left(\omega_f(t - t_{comp}) + \frac{2\pi}{3}\right) & \sin\left(\omega_f(t - t_{comp}) + \frac{2\pi}{3}\right) & 1 \end{bmatrix} \tag{5-17}$$

The current reference compensation component is expressed in (5-18).

$$I_{fa,b,ccomp} = P_{comp}^{-1} I_{fd,q,0ref1neg} = \sigma I_{neg} \begin{bmatrix} \cos(\omega_f t - \theta_{neg} + \omega_f t_{comp}) \\ \cos\left(\omega_f t - \theta_{neg} + \frac{2\pi}{3} + \omega_f t_{comp}\right) \\ \cos\left(\omega_f t - \theta_{neg} - \frac{2\pi}{3} + \omega_f t_{comp}\right) \end{bmatrix} \tag{5-18}$$

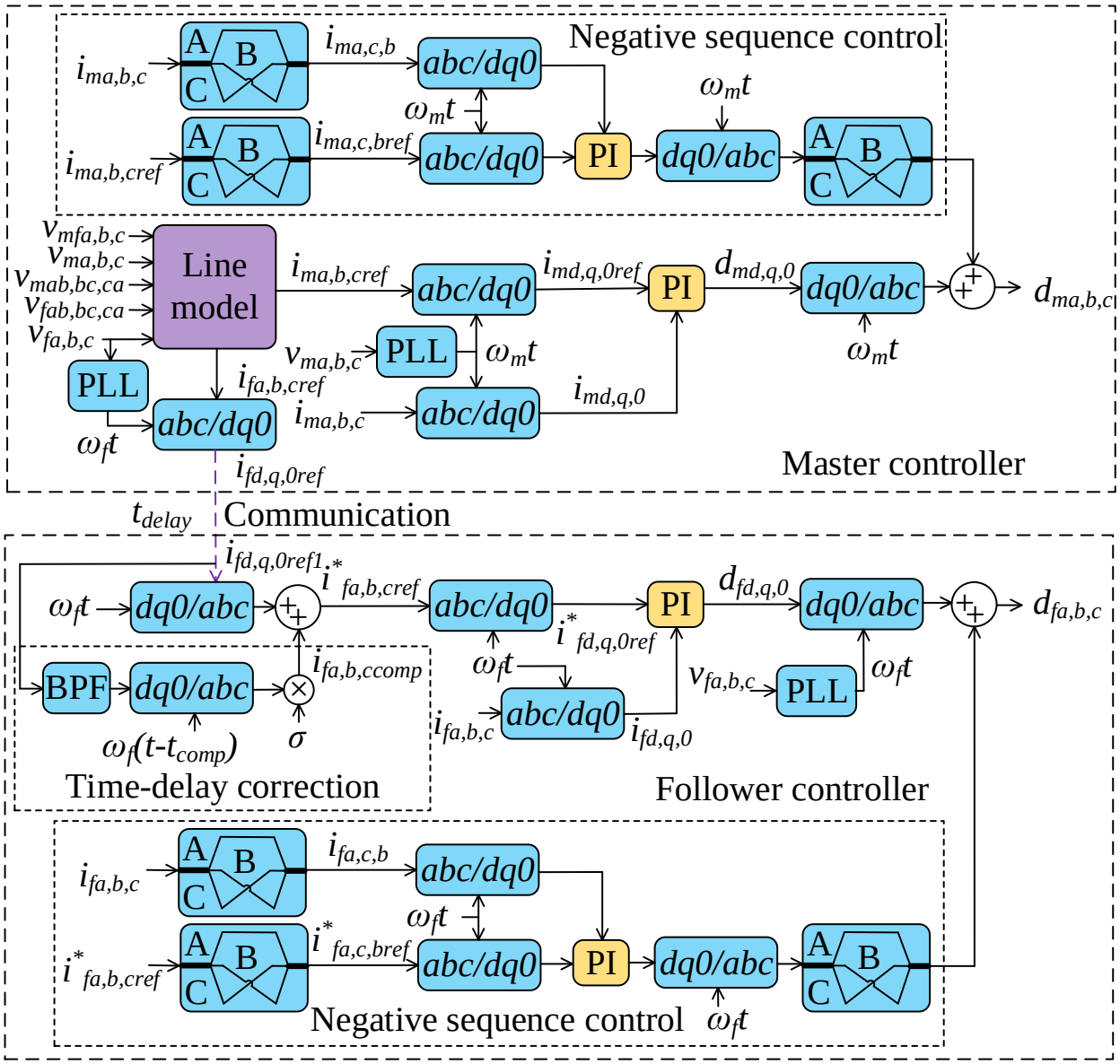


Figure 5-4. Current tracking control with negative sequence current control and time-delay correction.

To fully compensate the negative sequence component, (5-19) should be satisfied.

$$I_{fa,b,crefneg} = I_{fa,b,cref1neg} + I_{fa,b,ccomp} \tag{5-19}$$

Submit (5-13), (5-16), and (5-18) into (5-19), get (5-20).

$$\begin{bmatrix} \cos(\omega_f t - \theta_{neg})\left(\sigma\cos(\omega_f t_{comp}) + \cos(2\omega_f t_{delay}) - 1\right) + \\ \sin(\omega_f t - \theta_{neg})\left(\sin(2\omega_f t_{delay}) - \sigma\sin(\omega_f t_{comp})\right) \\ \cos\left(\omega_f t - \theta_{neg} + \frac{2\pi}{3}\right)\left(\sigma\cos(\omega_f t_{comp}) + \cos(2\omega_f t_{delay}) - 1\right) + \\ \sin\left(\omega_f t - \theta_{neg} + \frac{2\pi}{3}\right)\left(\sin(2\omega_f t_{delay}) - \sigma\sin(\omega_f t_{comp})\right) \\ \cos\left(\omega_f t - \theta_{neg} - \frac{2\pi}{3}\right)\left(\sigma\cos(\omega_f t_{comp}) + \cos(2\omega_f t_{delay}) - 1\right) + \\ \sin\left(\omega_f t - \theta_{neg} - \frac{2\pi}{3}\right)\left(\sin(2\omega_f t_{delay}) - \sigma\sin(\omega_f t_{comp})\right) \end{bmatrix} = \begin{bmatrix} 0 \\ 0 \\ 0 \end{bmatrix} \tag{5-20}$$

If condition is expressed as in (5-21) for satisfying (5-20).

$$\begin{cases} \sigma\cos(\omega_f t_{comp}) + \cos(2\omega_f t_{delay}) - 1 = 0 \\ \sin(2\omega_f t_{delay}) - \sigma\sin(\omega_f t_{comp}) = 0 \end{cases} \tag{5-21}$$

Solve (5-21), get (5-22).

$$\begin{cases} t_{comp} = \dfrac{1}{\omega_f}\tan^{-1}\dfrac{\sin(2\omega_f t_{delay})}{1 - \cos(2\omega_f t_{delay})} \\ \sigma = \sqrt{\left(\sin(2\omega_f t_{delay})\right)^2 + \left(1 - \cos(2\omega_f t_{delay})\right)^2} \end{cases} \tag{5-22}$$

For the transmission line emulator, the communication time delay t_{delay} is around 200us. According to (5-22), the time delay compensation parameters are t_{comp} = 4ms and σ = 0.1507.

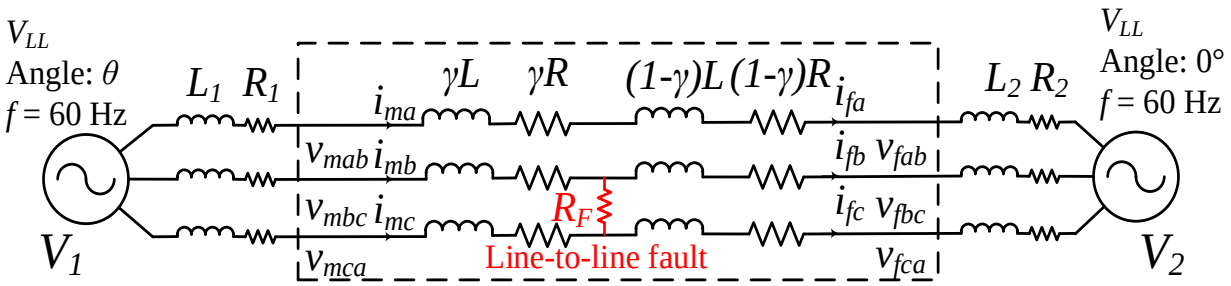


Figure 5-5. System topology for single line experimental verification.

5.3 Simulation and Experiment Results

The same as the transmission line emulation verification under normal conditions, a system diagram of a transmission line connected between two voltage sources is set up to verify the transmission line fault emulation, as shown in Figure 3-20. The ideal voltage source frequency is kept at 60 Hz, and the voltage source internal impedances are realized by physical inductors, which are L_1, R_1 and L_2, R_2, respectively.

The system diagram of the single transmission line experiment verification is shown in Figure 5-5. The transmission line inductance and resistance are L and R, respectively. The line-to-line short-circuit fault happens at the location γ ($0<\gamma<1$), which is the ratio of the distance from the fault location to the Master side terminal with regard to the total line length. The resistance R_F is the fault resistance.

In order to verify the transmission line emulation performance, two non-ideal voltage sources are connected with the transmission line by setting the voltage source impedances L_1 to 5.97 mH, R_1 to 0.65 Ω, L_2 to 2.4 mH, and R_2 to 0.07 Ω. The transmission line inductance and resistance are selected as 5 mH and 0.65 Ω, respectively. Three fault scenarios with γ equals to

0.3 and 0.5, respectively are conducted to verify the line-to-line short-circuit fault emulation capability at different locations within the emulated transmission line.

- Negative sequence control and time delay correction performances

a) Line-to-line fault emulation without negative sequence control and time delay correction

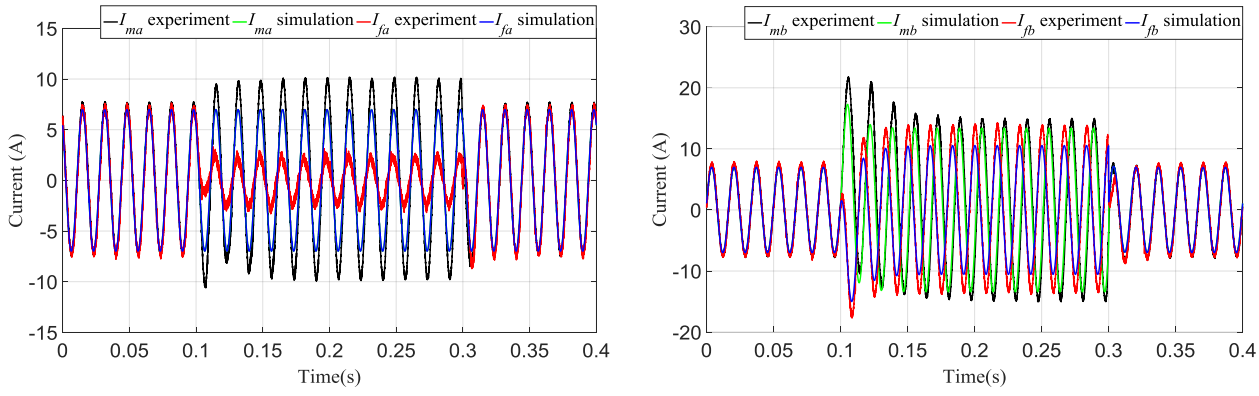
A line-to-line short-circuit fault with a fault resistance R_F = 0 Ω happens at 0.1 s at the location γ = 0.3 and when the phase angle of V_{mab} is 63°. The angle difference between the two voltage sources is $\theta = \theta_{V1} - \theta_{V2}$ = 175°. The fault is cleared at 0.3 s. Figure 5-6(a) and Figure 5-6(b) show the experiment and simulation result comparisons of I_a and I_b, respectively, which indicate that the experimental waveforms do not match with the simulation results.

b) Line-to-line short-circuit fault emulation without negative sequence control

A line-to-line short-circuit fault with a fault resistance R_F = 0 Ω happens at 0.1 s at the location γ = 0.3 and when the phase angle of V_{mab} is 280°. The angle difference between the two voltage sources is $\theta = \theta_{V1} - \theta_{V2}$ = 64°. The fault is cleared at 0.3 s. Figure 5-7(a) and Figure 5-7(b) show the experiment and simulation result comparisons of I_a and I_b, respectively, which indicate that the experimental waveforms do not match with the simulation results.

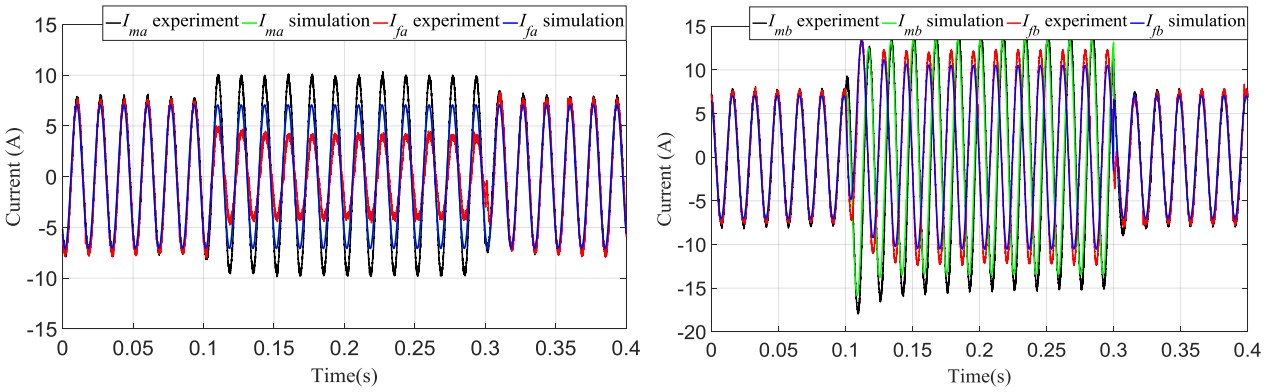
c) Line-to-line short-circuit fault emulation without time delay correction

A line-to-line short-circuit fault with a fault resistance R_F = 0 Ω happens at 0.1 s at the location γ = 0.3 and when the phase angle of V_{mab} is 234°. The angle difference between the two voltage sources is $\theta = \theta_{V1} - \theta_{V2}$ = 55°. The fault is cleared at 0.3 s. Figure 5-8(a) and Figure 5-8(b) show the experiment and simulation result comparisons of I_a and I_b, respectively, which indicate that the experimental waveforms do not match with the simulation results but the differences are smaller than the experiment without negative sequence control.



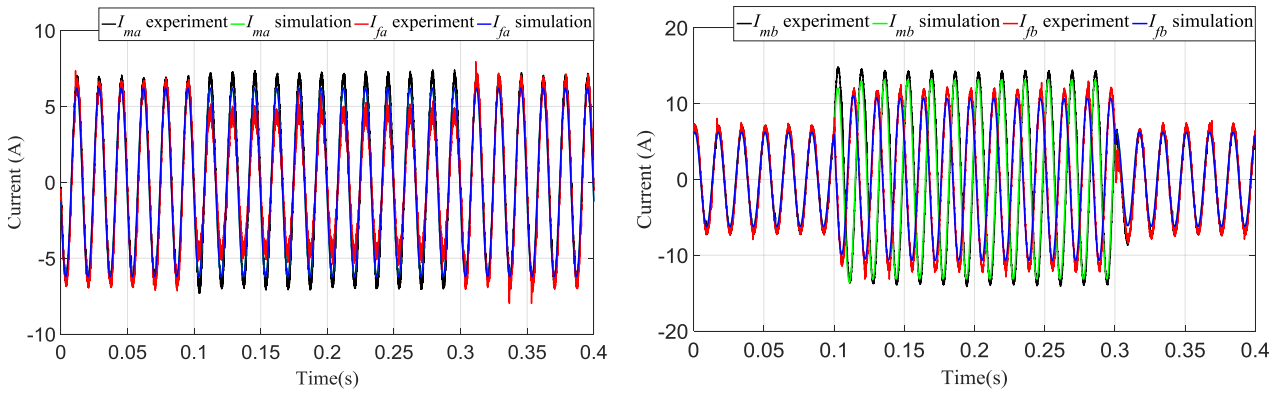
(a) (b)

Figure 5-6. Single transmission line experiment and simulation comparison without negative sequence control and time delay correction when $\gamma = 0.3$ and $R_F = 0\ \Omega$: (a) I_a; (b) I_b.



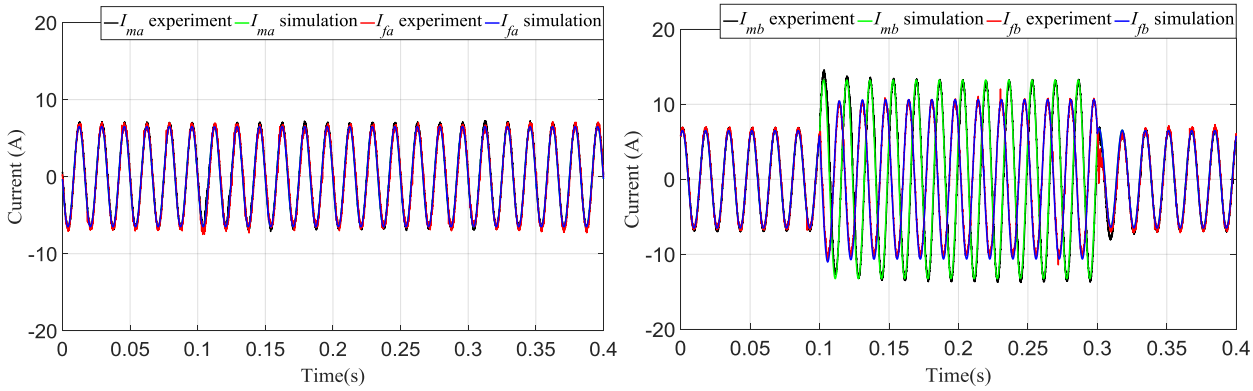
(a) (b)

Figure 5-7. Single transmission line experiment and simulation comparison without negative sequence control when $\gamma = 0.3$ and $R_F = 0\ \Omega$: (a) I_a; (b) I_b.



(a) (b)

Figure 5-8. Single transmission line experiment and simulation comparison without time delay correction when $\gamma = 0.3$ and $R_F = 0\ \Omega$: (a) I_a; (b) I_b.



(a) (b)

Figure 5-9. Single transmission line experiment and simulation comparison with $\gamma = 0.3$ and $R_F = 0\ \Omega$: (a) I_a; (b) I_b.

d) Line-to-line short-circuit fault emulation with proposed negative sequence control and time delay correction

A line-to-line short-circuit fault with a fault resistance R_F = 0 Ω happens at 0.1 s at the location γ = 0.3 and when the phase angle of V_{mab} is 58°. The angle difference between the two voltage sources is $\theta = \theta_{V1} - \theta_{V2}$ = 226°. The fault is cleared at 0.3 s. Figure 5-9(a) and Figure 5-9(b) show the experiment and simulation result comparisons of I_a and I_b, respectively, which indicate that the experimental waveforms match well with the simulation results.

- Line-to-line fault emulation results

a) Line-to-line short-circuit fault with γ = 0.5 and R_F = 0 Ω

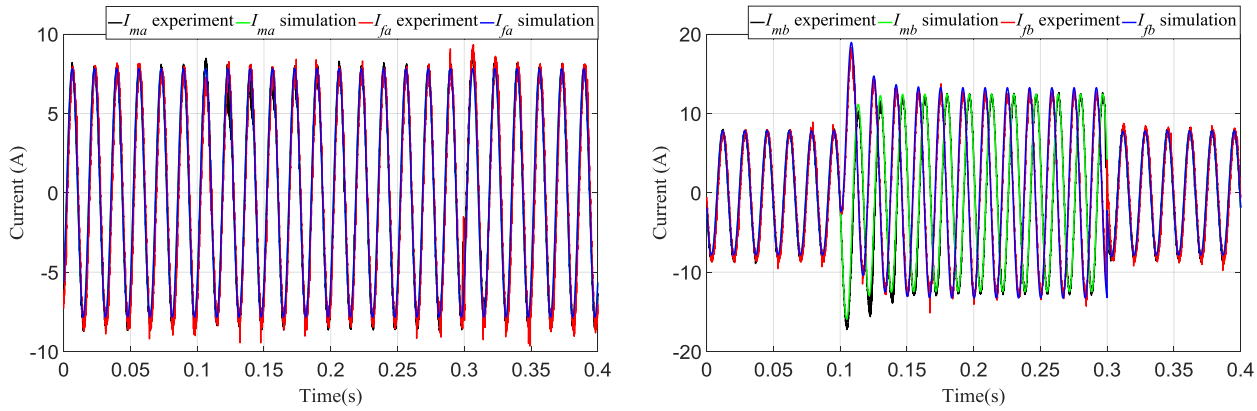
A line-to-line short-circuit fault with a fault resistance R_F = 0 Ω happens at 0.1 s at the location γ = 0.5 and when the phase angle of V_{mab} is 72.36°. The angle difference between the two voltage sources is $\theta = \theta_{V1} - \theta_{V2}$ = 4.32°. The fault is cleared at 0.3 s.

Figure 5-10(a) and Figure 5-10(b) show the experiment and simulation result comparisons of I_a and I_b, respectively, which indicate that the experimental waveforms match well with the simulation results.

b) Line-to-line short-circuit fault with γ = 0.5 and R_F = 1 Ω

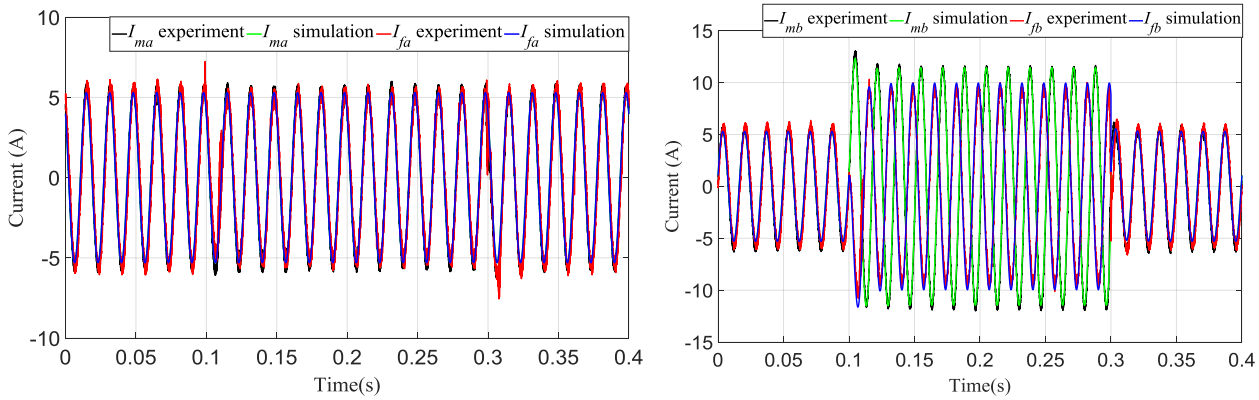
A line-to-line short-circuit fault with a fault resistance R_F = 1 Ω happens at 0.1 s at the location γ = 0.5 and when the phase angle of V_{mab} is 46.44°. The angle difference between the two voltage sources is $\theta = \theta_{V1} - \theta_{V2}$ = 169.56°. The fault is cleared at 0.3 s.

Figure 5-11(a) and Figure 5-11(b) show the experiment and simulation result comparisons of I_a and I_b, respectively, which indicate that the experimental waveforms match well with the simulation results.



(a) (b)

Figure 5-10. Single transmission line experiment and simulation comparison with γ = 0.5 and R_F = 0 Ω: (a) I_a; (b) I_b.



(a) (b)

Figure 5-11. Single transmission line experiment and simulation comparison with γ = 0.5 and R_F = 1 Ω: (a) I_a; (b) I_b.

c) Line-to-line short-circuit fault with $\gamma = 0.5$ and $R_F = 2\ \Omega$

A line-to-line short-circuit fault with a fault resistance $R_F = 2\ \Omega$ happens at 0.1 s at the location $\gamma = 0.5$ and when the phase angle of V_{mab} is 59.83°. The angle difference between the two voltage sources is $\theta = \theta_{V1} - \theta_{V2} = 88.56°$. The fault is cleared at 0.3 s.

Figure 5-12(a) and Figure 5-12(b) show the experiment and simulation result comparisons ofs I_a and I_b, respectively, which indicate that the experimental waveforms match well with the simulation results.

d) Line-to-line short-circuit fault with $\gamma = 0.3$ and $R_F = 1\ \Omega$

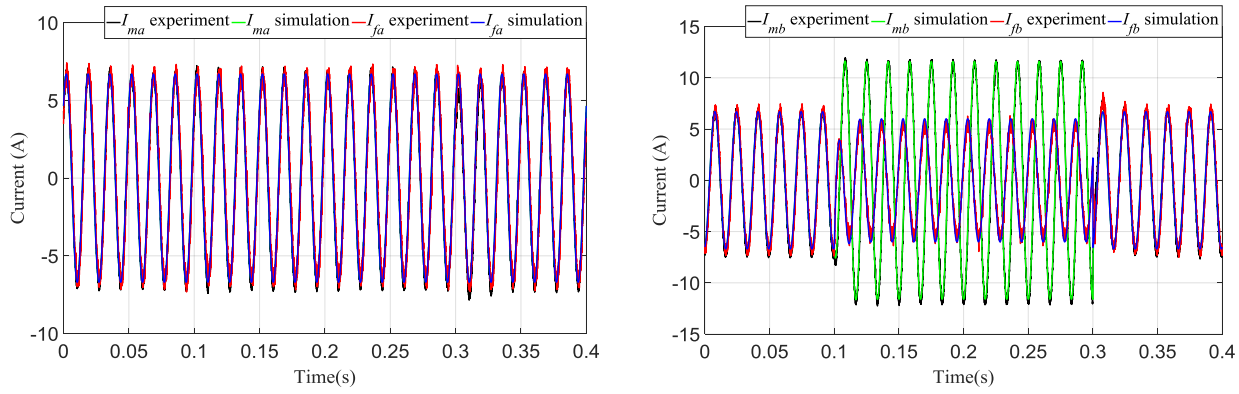
A line-to-line short-circuit fault with a fault resistance $R_F = 1\ \Omega$ happens at 0.1 s at the location $\gamma = 0.3$ and when the phase angle of V_{mab} is 70°. The angle difference between the two voltage sources is $\theta = \theta_{V1} - \theta_{V2} = -307°$. The fault is cleared at 0.3 s.

Figure 5-13(a) and Figure 5-13(b) show the experiment and simulation result comparisons of I_a and I_b, respectively, which indicate that the experimental waveforms match well with the simulation results.

e) Line-to-line short-circuit fault with $\gamma = 0.3$ and $R_F = 2\ \Omega$

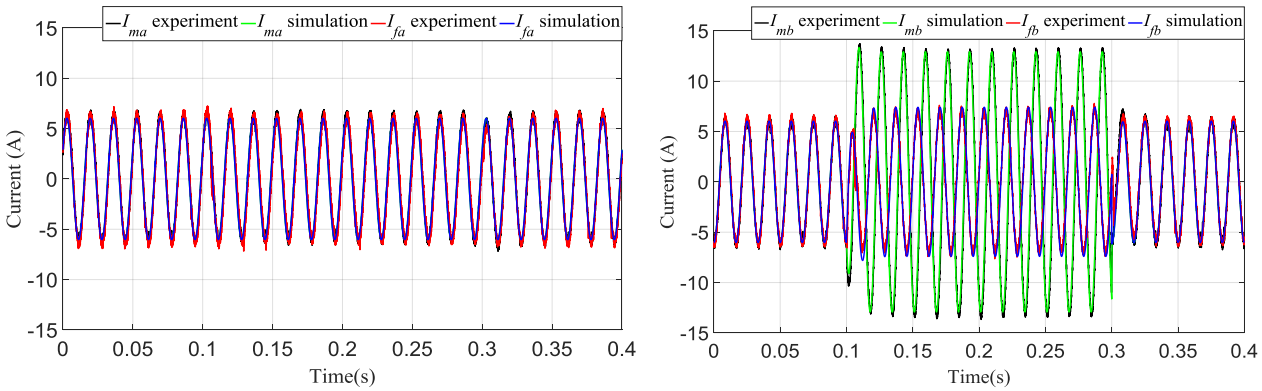
A line-to-line short-circuit fault with a fault resistance $R_F = 2\ \Omega$ happens at 0.1 s at the location $\gamma = 0.3$ and when the phase angle of V_{mab} is 355°. The angle difference between the two voltage sources is $\theta = \theta_{V1} - \theta_{V2} = 50°$. The fault is cleared at 0.3 s.

Figure 5-14(a) and Figure 5-14(b) show the experiment and simulation result comparisons of I_a and I_b, respectively, which indicate that the experimental waveforms match well with the simulation results.



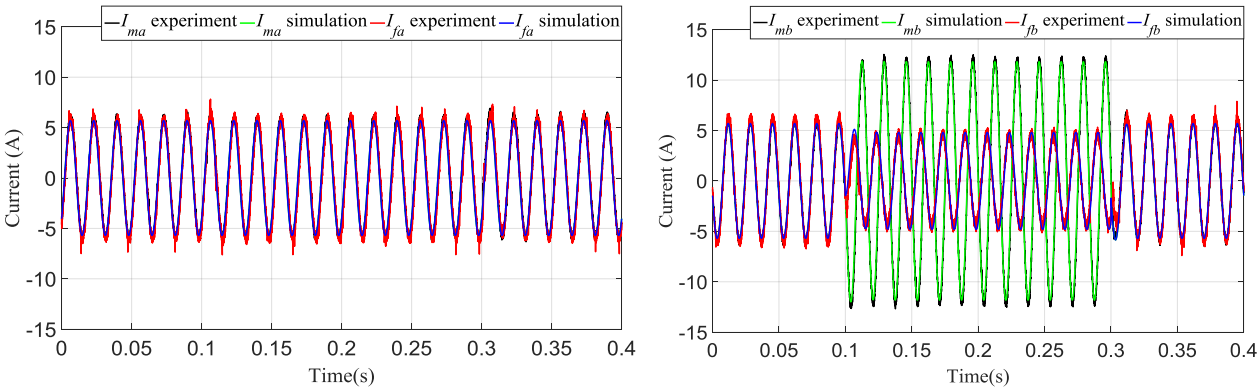
(a) (b)

Figure 5-12. Single transmission line experiment and simulation comparison with $\gamma = 0.5$ and $R_F = 2\ \Omega$: (a) I_a; (b) I_b.



(a) (b)

Figure 5-13. Single transmission line experiment and simulation comparison with $\gamma = 0.3$ and $R_F = 1\ \Omega$: (a) I_a; (b) I_b.



(a) (b)

Figure 5-14. Single transmission line experiment and simulation comparison with γ = 0.3 and R_F = 2 Ω: (a) I_a; (b) I_b.

5.4 Conclusion

The fault model of a single transmission line has been developed to realize line-to-line short-circuit fault emulation at different locations along the emulated transmission line. A negative sequence control method has been proposed to track the negative sequence current induced by the line-to-line fault. A time-delay correction method based on Park's transformation has also been proposed and implemented to compensate the communication time-delay between the Master and Follower controller, which influence the transmission line emulation accuracy during a line-to-line fault. Experiment results verified the proposed transmission line model and the effectiveness of the developed transmission line emulator with line-to-line short-circuit fault emulation capability.

6 Hybrid Emulation Platform with RTDS and HTB

In this chapter, the basic concept and theory of power system hybrid emulation are introduced. A combined interface algorithm is developed to assure the hybrid emulation stability under different system configurations based on the stability analysis of the state of the art interface algorithms. A new time-delay correction method is proposed to improve the hybrid emulation accuracy by compensating the interface time-delay. Two hybrid emulation interfaces are built up to makes the platform suitable for more general power grid topologies, and the emulation stability with two interfaces are analyzed. Simulation and experiment results are presented to verify the developed platform.

6.1 Hybrid Emulation Interface Algorithm

The theoretical basis of hybrid emulation is the substitution theorem in electric circuit theory. Within an electrical network, if a subsystem is replaced by a voltage source, whose voltage equals to the subsystem terminal voltage in the original network at any instant of time, the performance of the remainder of the subsystem in the network keeps the same as it is in the original network. Alternately, if a subsystem is replaced by a current source, whose instantaneous current equals to the subsystem terminal current in the original network, the performance of the remainder of the subsystem keeps the same as it is in the original network.

By using the substitution theorem directly, the Ideal Transformer Model (ITM) algorithm was proposed to realize the hybrid emulation of a real-time digital simulator and a hardware platform [93]. In this dissertation, the ITM algorithms are separately named as voltage source ITM and current source ITM based on the type of controlled source implemented at the hardware side.

The voltage source ITM is represented by a controlled voltage source at the hardware side, as shown in Figure 6-1(a). The current source ITM is represented by a controlled current source at the hardware side, as shown in Figure 6-1(b).

For the voltage source ITM in Figure 6-1(a), the voltage and current relationship is expressed in (6-1).

$$\begin{cases} E_1(s) = Z_1(s)i^*(s) + u(s) \\ E_2(s) = -Z_2(s)i(s) + u^*(s) \end{cases} \tag{6-1}$$

Assume the total interface time delay is Δt, and the time delay is applied on the voltage reference to simplify the analysis, as expressed in (6-2).

$$\begin{cases} i^*(s) = i(s) \\ u^*(s) = u(s)e^{-s\Delta t} \end{cases} \tag{6-2}$$

Substituting (6-2) into (6-1) results in (6-3).

$$\{E_2(s) = -Z_2(s)i(s) + u(s)e^{-s\Delta t} \tag{6-3}$$

Substituting (6-1) and (6-2) into (6-3) results in (6-4).

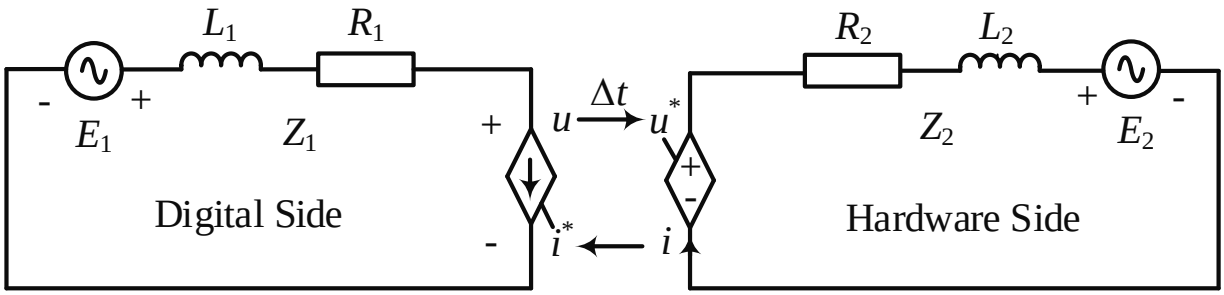
$$E_2(s) = -Z_2(s)i(s) + E_1(s)e^{-s\Delta t} - Z_1(s)i(s)e^{-s\Delta t} \tag{6-4}$$

Solving for *i(s)* from (6-4) results in (6-5).

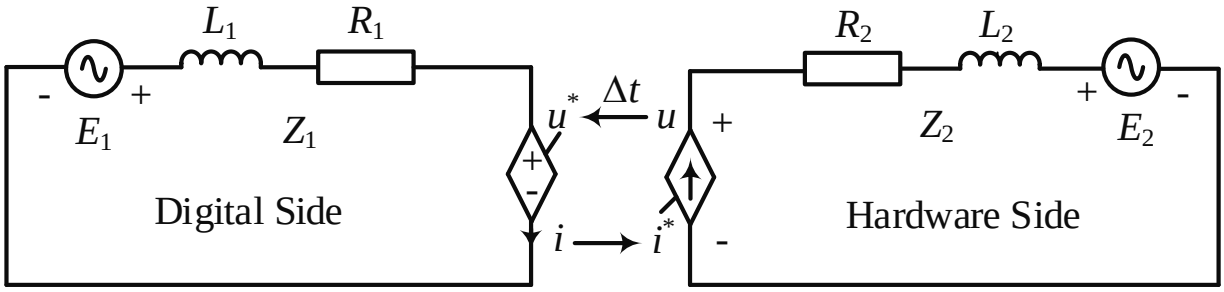
$$i(s) = [E_1(s)e^{-s\Delta t}/Z_2(s) - E_2(s)/Z_2(s)]\ /[1 + Z_1(s)e^{-s\Delta t}/Z_2(s)] \tag{6-5}$$

According to the Nyquist stability, the system is assured to be stable when (6-6) is satisfied.

$$\left|Z_1(s)e^{-s\Delta t}/Z_2(s)\right| < 1 \tag{6-6}$$



(a)



(b)

Figure 6-1. Hybrid emulation interface algorithms: (a) Voltage source ITM; (b) Current source ITM.

The stability requirement is expressed in (6-7) based on (6-6).

$$|Z_1(s)| < |Z_2(s)| \tag{6-7}$$

With the same assumption for the current source ITM, the relationship is expressed in (6-8).

$$E_1(s) = Z_1(s)i(s) + E_2(s)e^{-s\Delta t} + Z_2(s)i(s)e^{-s\Delta t} \tag{6-8}$$

Solving *i(s)* from (6-8) results in (6-9).

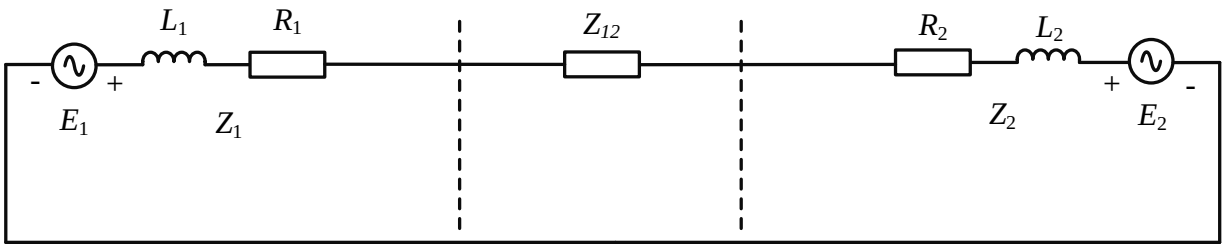
$$i(s) = [E_1(s) - E_2(s)e^{-s\Delta t}] / [Z_1(s) + Z_2(s)e^{-s\Delta t}] \tag{6-9}$$

Similarly, the stability requirement is expressed in (6-10) based on (6-9).

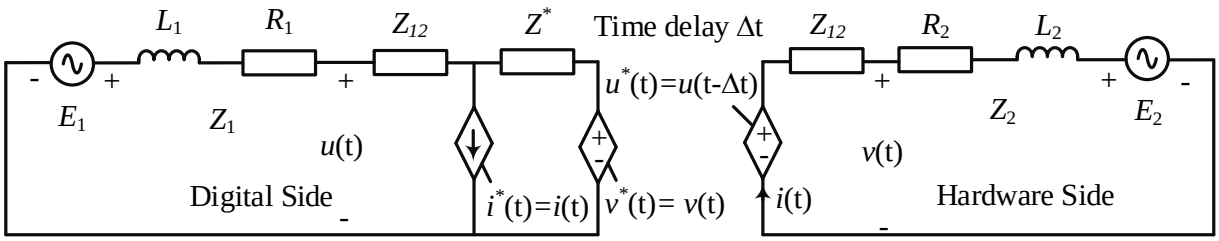
$$|Z_1(s)| > |Z_2(s)| \tag{6-10}$$

According to (6-7), the voltage source ITM algorithm is stable if the equivalent impedance of the digital side is smaller than the hardware side; on the contrary, the current source ITM is stable if the equivalent impedance of digital side is larger than hardware side, as shown in (6-10).

Since the hybrid emulation is unstable under some impedance relationship conditions with one type of ITM algorithm, some interface algorithms have been proposed to improve the stability. Figure 6-2 shows the Damping Impedance Model (DIM) algorithm, in which the impedance Z_{12} between the digital side and the hardware side is used repeatedly and an additional impedance Z^* is applied at the digital side to improve the hybrid emulation stability [32], [92]. The stability region is larger than that of the pure voltage source ITM [32]. However, the interface accuracy can be affected by the repeated use of Z_{12} and the additional impedance Z^*, and an actual resistor needs to be installed in the hardware side. The physical resistor introduces losses in the hardware setup and influences the emulation flexibility. The Partial Circuit Duplication (PCD) algorithm is a special case of DIM when $R_d = 0$ [32].

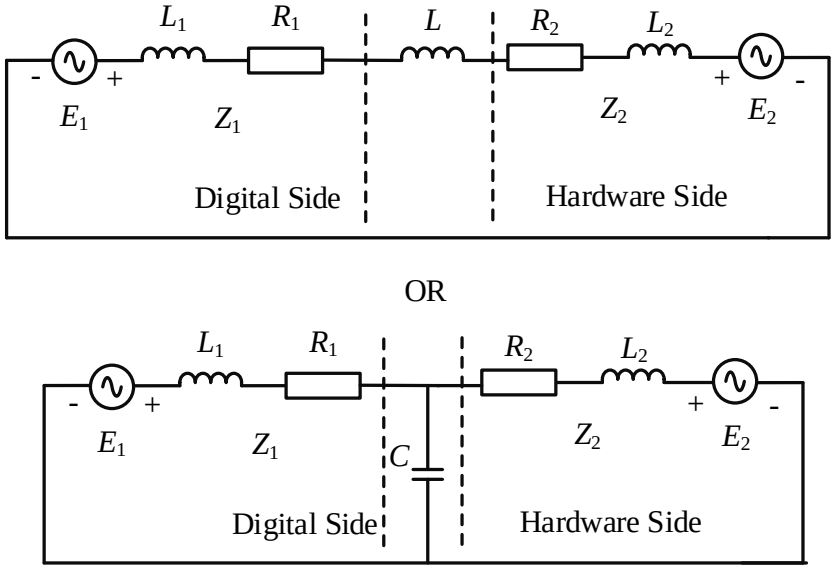


(a)

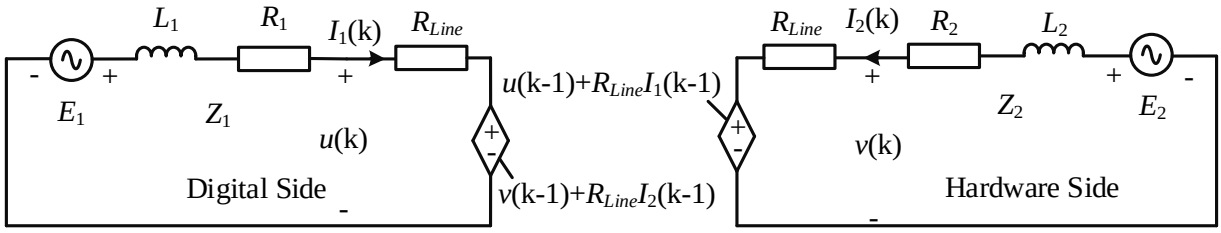


(b)

Figure 6-2. DIM algorithm: (a) System topology to be emulated; (b) Hybrid emulation diagram with DIM algorithm.



(a)



(b)

Figure 6-3. TLM algorithm: (a) System topology to be emulated; (b) Hybrid emulation diagram with TLM algorithm.

By using the decoupling characteristic and natural time-delay of Bergeron equivalent circuit, the Transmission Line Model (TLM) algorithm was proposed to improve the hybrid emulation stability, as shown in Figure 6-3 [32]. The TLM algorithm utilizes a linking inductor or capacitor equivalently as the Bergeron line model.

The resistance R_{Line} in the model equals to L / Δt and Δt / C for the linking inductor L case and the linking capacitor C case, respectively, where Δt is the transmission line propagation time. The TLM algorithm is highly stable since it is numerically based on the trapezoidal approximation. However, an actual resistor also needs to be installed in the hardware side, and the resistance must be modified when the emulated system changes.

Although the DIM, PCB, and TLM algorithms have a larger stability region than a pure voltage source or current source ITM algorithm, the interface accuracy and system flexibility are affected by implementing these algorithms.

Considering the stability conditions of voltage source ITM and current source ITM are complementary, an interface, which is composed of these two ITM algorithms, is implemented to realize the hybrid emulation stably under different conditions in this paper. When the equivalent impedance in the digital side is smaller than the hardware side, the voltage source ITM is used; when the equivalent impedance in the digital side is larger than the hardware side, the current source ITM is selected.

6.2 Time-delay Correction Method

In the hybrid emulation system, the interface time-delay not only causes stability problems but also influences the hybrid emulation accuracy [35]. A time-delay compensation method based on FFT was proposed in [36] to improve the power interface accuracy, as shown in Figure

6-4. The voltage reference is first transformed to the frequency domain with the FFT algorithm. In the frequency domain, the time-delay is equivalent to a phase-shift for each frequency component, so a phase-advance can be implemented to compensate for the corresponding phase-shift. A portion of the harmonic components can be processed with this method by implementing multiple FFTs. However, the number of harmonic components that can be processed is limited considering the FFT calculation time.

In this thesis, a time-delay compensation method in *dq0* domain is proposed to improve the hybrid emulation accuracy, as shown in Figure 6-5. In the *dq0* domain, the time-delay is equivalent to a phase-shift for the fundamental frequency phase angle θ_1, so a phase compensation angle $\Delta\theta_1$ can be added into the phase angle θ_1 to correct the time-delay. The $\Delta\theta_1$ can be acquired by testing and preset as the delay correction angle. Since the angle correction is implemented to adjust the *abc* to *dq0* Park's transformation phase angle, all harmonic components are maintained.

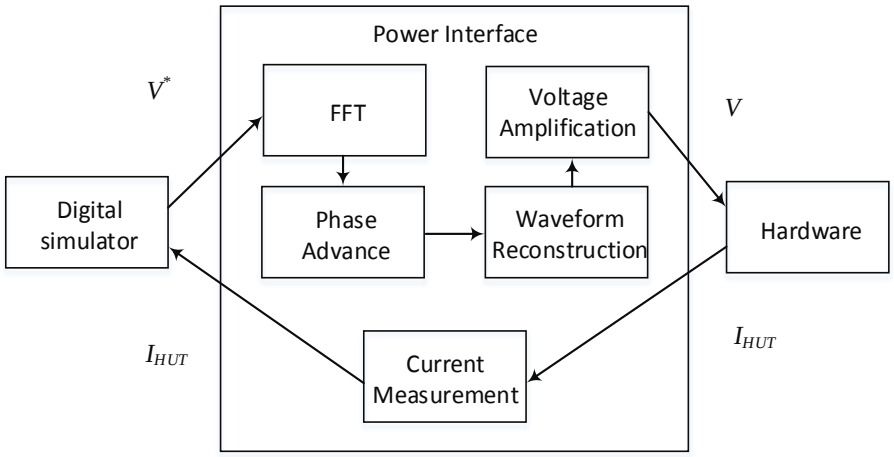


Figure 6-4. Time delay compensation method based on FFT.

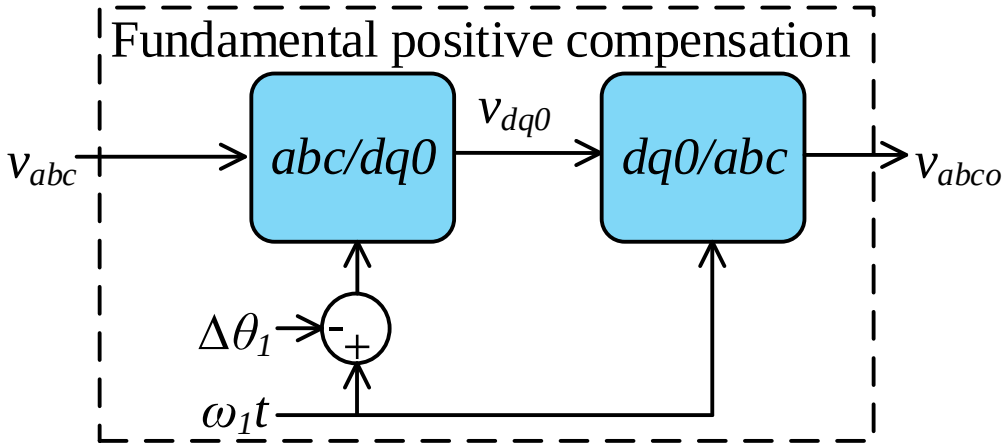


Figure 6-5. Time-delay compensation method based on Park's transformation .

The Park's transformation (*abc*/*dq0*) matrix with a phase angle delay $\Delta\theta_1$ and Park's inverse transformation (*dq0*/*abc*) matrix are expressed in (6-11) and (6-12), respectively.

$$P_{-\Delta\theta_1} = \frac{2}{3}\begin{bmatrix} \cos(\omega_1 t - \Delta\theta_1) & \cos(\omega_1 t - \frac{2\pi}{3} - \Delta\theta_1) & \cos(\omega_1 t + \frac{2\pi}{3} - \Delta\theta_1) \\ \sin(\omega_1 t - \Delta\theta_1) & \sin(\omega_1 t - \frac{2\pi}{3} - \Delta\theta_1) & \sin(\omega_1 t + \frac{2\pi}{3} - \Delta\theta_1) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \tag{6-11}$$

$$P^{-1} = \begin{bmatrix} \cos(\omega_1 t) & \sin(\omega_1 t) & 1 \\ \cos(\omega_1 t - \frac{2\pi}{3}) & \sin(\omega_1 t - \frac{2\pi}{3}) & 1 \\ \cos(\omega_1 t + \frac{2\pi}{3}) & \sin(\omega_1 t + \frac{2\pi}{3}) & 1 \end{bmatrix} \tag{6-12}$$

Assume the original three-phase voltages are v_a, v_b, and v_c, the output voltages after the delay correction are expressed in (6-13).

$$\begin{bmatrix} v_{ao} \\ v_{bo} \\ v_{co} \end{bmatrix} = P^{-1}P_{-\Delta\theta_1}\begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} =$$

$$\frac{2}{3}\begin{bmatrix} \frac{1}{2}+\cos(\Delta\theta_1) & \frac{1}{2}+\cos(\frac{2\pi}{3}+\Delta\theta_1) & \frac{1}{2}+\cos(-\frac{2\pi}{3}+\Delta\theta_1) \\ \frac{1}{2}+\cos(\Delta\theta_1-\frac{2\pi}{3}) & \frac{1}{2}+\cos(\Delta\theta_1) & \frac{1}{2}+\cos(-\frac{4\pi}{3}+\Delta\theta_1) \\ \frac{1}{2}+\cos(\frac{2\pi}{3}+\Delta\theta_1) & \frac{1}{2}+\cos(\frac{4\pi}{3}+\Delta\theta_1) & \frac{1}{2}+\cos(\Delta\theta_1) \end{bmatrix}\begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} \quad (6\text{-}13)$$

Assume v_a, v_b, and v_c are positive sequence three-phase voltages with an angular frequency ω, as expressed in (6-14). Submit (6-14) into (6-13), get (6-15).

$$[v_a \quad v_b \quad v_c]^T = \left[V\cos(\omega_1 t) \quad V\cos(\omega_1 t-\frac{2\pi}{3}) \quad V\cos(\omega_1 t+\frac{2\pi}{3})\right]^T \quad (6\text{-}14)$$

$$\begin{bmatrix} v_{ao} \\ v_{bo} \\ v_{co} \end{bmatrix} = P^{-1}P_{-\Delta\theta_1}\begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} = \begin{bmatrix} V\cos(\omega t+\Delta\theta_1) \\ V\cos(\omega t-\frac{2\pi}{3}+\Delta\theta_1) \\ V\cos(\omega t+\frac{2\pi}{3}+\Delta\theta_1) \end{bmatrix} \quad (6\text{-}15)$$

According to (6-15), three-phase positive sequence voltages under any frequency get a $\Delta\theta_1$ phase-lead and maintain the magnitude by implementing the delay correction angle $\Delta\theta_1$ in the Park's *abc*/*dq0* transformation. The fundamental frequency positive sequence component angle-delay can be completely compensated by setting $\Delta\theta_1$ equals to the pre-tested angle-delay.

Assume v_a, v_b, and v_c are negative sequence three-phase voltages with an angular frequency ω, as expressed in (6-16). Submit (6-16) into (6-13), get (6-17).

$$[v_a \quad v_b \quad v_c]^T = \left[V\cos(\omega t) \quad V\cos(\omega t+\frac{2\pi}{3}) \quad V\cos(\omega t-\frac{2\pi}{3})\right]^T \quad (6\text{-}16)$$

$$\begin{bmatrix} v_{ao} \\ v_{bo} \\ v_{co} \end{bmatrix} = P^{-1}P_{-\Delta\theta_1}\begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} = \begin{bmatrix} V\cos(\omega t - \Delta\theta_1) \\ V\cos(\omega t - \frac{2\pi}{3} - \Delta\theta_1) \\ V\cos(\omega t + \frac{2\pi}{3} - \Delta\theta_1) \end{bmatrix} \tag{6-17}$$

According to (6-17), three-phase negative sequence voltages under any frequency get a $\Delta\theta_1$ phase-delay and maintain the magnitude by implementing the delay correction angle $\Delta\theta_1$ in the Park's *abc*/*dq0* transformation.

Assume v_a, v_b, and v_c are zero sequence three-phase voltages with an angular frequency ω, as expressed in (6-18). Submit (6-18) into (6-13), get (6-19).

$$[v_a \quad v_b \quad v_c]^T = [V\cos(\omega t) \quad V\cos(\omega t) \quad V\cos(\omega t)]^T \tag{6-18}$$

$$\begin{bmatrix} v_{ao} \\ v_{bo} \\ v_{co} \end{bmatrix} = P^{-1}P_{-\Delta\theta_1}\begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} = \begin{bmatrix} V\cos(\omega t) \\ V\cos(\omega t) \\ V\cos(\omega t) \end{bmatrix} \tag{6-19}$$

According to (6-19), three-phase zero sequence voltages under any frequency keeps the same by implementing the delay correction angle $\Delta\theta_1$ in the Park's *abc*/*dq0* transformation.

Assume the required negative sequence phase angle delay correction is $\Delta\theta_n$, an additional compensation voltage can be added to fully compensate the negative sequence component, as expressed in (6-20).

$$\begin{bmatrix} v_{anc} \\ v_{bnc} \\ v_{cnc} \end{bmatrix} = \begin{bmatrix} V\cos(\omega t + \Delta\theta_n) \\ V\cos(\omega t + \frac{2\pi}{3} + \Delta\theta_n) \\ V\cos(\omega t - \frac{2\pi}{3} + \Delta\theta_n) \end{bmatrix} - \begin{bmatrix} V\cos(\omega t - \Delta\theta_1) \\ V\cos\left(\omega t + \frac{2\pi}{3} - \Delta\theta_1\right) \\ V\cos\left(\omega t - \frac{2\pi}{3} - \Delta\theta_1\right) \end{bmatrix} \tag{6-20}$$

Solve (6-20), get (6-21), and A_n and B_n are expressed in (6-22).

$$\begin{bmatrix} v_{anc} \\ v_{bnc} \\ v_{cnc} \end{bmatrix} = V \begin{bmatrix} \mathrm{A}_n\cos(\omega t) - \mathrm{B}_n\sin(\omega t) \\ \mathrm{A}_n\cos\left(\omega t + \frac{2\pi}{3}\right) - \mathrm{B}_n\sin\left(\omega t + \frac{2\pi}{3}\right) \\ \mathrm{A}_n\cos\left(\omega t - \frac{2\pi}{3}\right) - \mathrm{B}_n\sin\left(\omega t - \frac{2\pi}{3}\right) \end{bmatrix} \tag{6-21}$$

$$\begin{cases} A_n = \cos(\Delta\theta_n) - \cos(\Delta\theta_1) \\ B_n = \sin(\Delta\theta_n) + \sin(\Delta\theta_1) \end{cases} \tag{6-22}$$

Solve (6-21), get (6-23), and λ_n and $\Delta\theta_{nc}$ are expressed in (6-24).

$$\begin{bmatrix} v_{anc} \\ v_{bnc} \\ v_{chc} \end{bmatrix} = \lambda_n V \begin{bmatrix} \cos(\omega t + \Delta\theta_{nc}) \\ \cos(\omega t + \frac{2\pi}{3} + \Delta\theta_{nc}) \\ \cos(\omega t - \frac{2\pi}{3} + \Delta\theta_{nc}) \end{bmatrix} \tag{6-23}$$

$$\begin{cases} \lambda_n = \sqrt{{A_n}^2 + {B_n}^2} = \sqrt{(\cos(\Delta\theta_n) - \cos(\Delta\theta_1))^2 + (\sin(\Delta\theta_n) + \sin(\Delta\theta_1))^2} \\ \Delta\theta_{nc} = \arctan\left(\frac{B_n}{A_n}\right) = \arctan\left(\frac{\sin(\Delta\theta_n) + \sin(\Delta\theta_1)}{\cos(\Delta\theta_n) - \cos(\Delta\theta_1)}\right) \end{cases} \tag{6-24}$$

An additional function block can be added to fully compensate the angle-delay of the negative sequence component, as shown in Figure 6-6. By switching phase B and C, the negative sequence component is transferred to positive sequence component, and the negative sequence component with a frequency ω is transferred to a dc component through the *abc*/*dq0* transformation. The low-pass filter filters out all the other components except for the negative sequence component under the frequency ω. By adding the angle $\Delta\theta_{nc}$, multiplying a coefficient λ_n, and switching phase B and C back, the required correction voltage in (6-23) for the negative sequence component can be acquired.

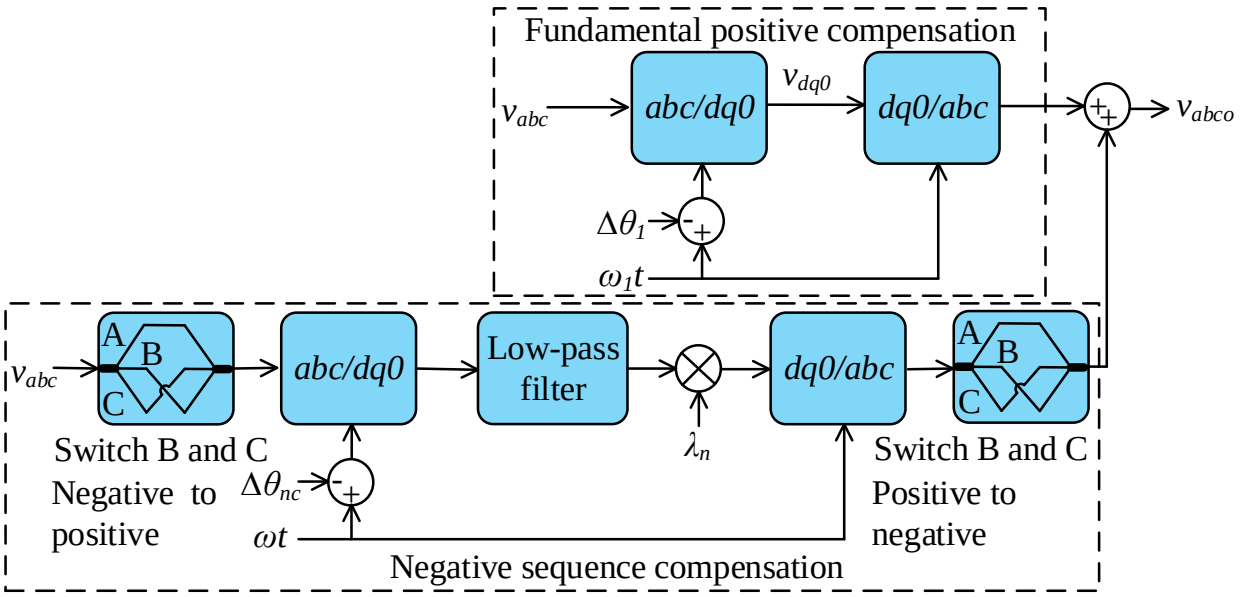


Figure 6-6. Time-delay compensation with an added negative sequence correction block.

Assume the required zero sequence phase angle delay correction is $\Delta\theta_0$, an additional compensation voltage can be added to fully compensate the zero sequence component, as expressed in (6-25).

$$\begin{bmatrix} v_{a0c} \\ v_{b0c} \\ v_{c0c} \end{bmatrix} = \begin{bmatrix} V\cos(\omega t + \Delta\theta_0) \\ V\cos(\omega t + \Delta\theta_0) \\ V\cos(\omega t + \Delta\theta_0) \end{bmatrix} - \begin{bmatrix} V\cos(\omega t) \\ V\cos(\omega t) \\ V\cos(\omega t) \end{bmatrix} \tag{6-25}$$

Solve (6-25), get (6-26).

$$\begin{bmatrix} v_{a0c} \\ v_{b0c} \\ v_{c0c} \end{bmatrix} = V \begin{bmatrix} \mathrm{A}_0\cos(\omega t) - \mathrm{B}_n\sin(\omega t) \\ \mathrm{A}_0\cos(\omega t) - \mathrm{B}_n\sin(\omega t) \\ \mathrm{A}_0\cos(\omega t) - \mathrm{B}_n\sin(\omega t) \end{bmatrix} \tag{6-26}$$

where A_0 and B_0 are expressed in (6-27).

$$\begin{cases} A_0 = \cos(\Delta\theta_0) - 1 \\ B_0 = \sin(\Delta\theta_0) \end{cases} \tag{6-27}$$

Solve (6-26), get (6-28).

$$\begin{bmatrix} v_{a0c} \\ v_{b0c} \\ v_{c0c} \end{bmatrix} = \lambda_0 V \begin{bmatrix} \cos(\omega t + \Delta\theta_{0c}) \\ \cos(\omega t + \Delta\theta_{0c}) \\ \cos(\omega t + \Delta\theta_{0c}) \end{bmatrix} \tag{6-28}$$

where λ_0 and $\Delta\theta_{0c}$ are expressed in (6-29).

$$\begin{cases} \lambda_0 = \sqrt{{A_0}^2 + {B_0}^2} = \sqrt{(\cos(\Delta\theta_0) - 1)^2 + (\sin(\Delta\theta_0))^2} \\ \Delta\theta_{0c} = \arctan\left(\dfrac{B_0}{A_0}\right) + \pi = \arctan\left(\dfrac{\sin(\Delta\theta_0)}{\cos(\Delta\theta_0) - 1}\right) + \pi \end{cases} \tag{6-29}$$

An additional function block can be added to fully compensate the angle-delay of the zero sequence component, as shown in Figure 6-7. By adding $2\pi/(3\omega)$ and $4\pi/(3\omega)$ time delay on phase B and Phase C, respectively, the zero sequence component under the frequency ω is transferred to positive sequence component, and then it is transferred to a dc component through the *abc*/*dq0* transformation. The low-pass filter filters out all the other components except for the zero sequence component under the frequency ω. By adding the angle $\Delta\theta_{0c}$, multiplying a coefficient λ_0, and using the phase A voltage for all three phases, the required correction voltage in (6-28) for the zero sequence component can be acquired.

Usually, the higher order harmonic component angle delay is larger than the fundamental frequency component for the same time delay. Thus, for the positive components of higher order harmonics, the compensation method maintains the magnitudes and partially compensates the angle-delay.

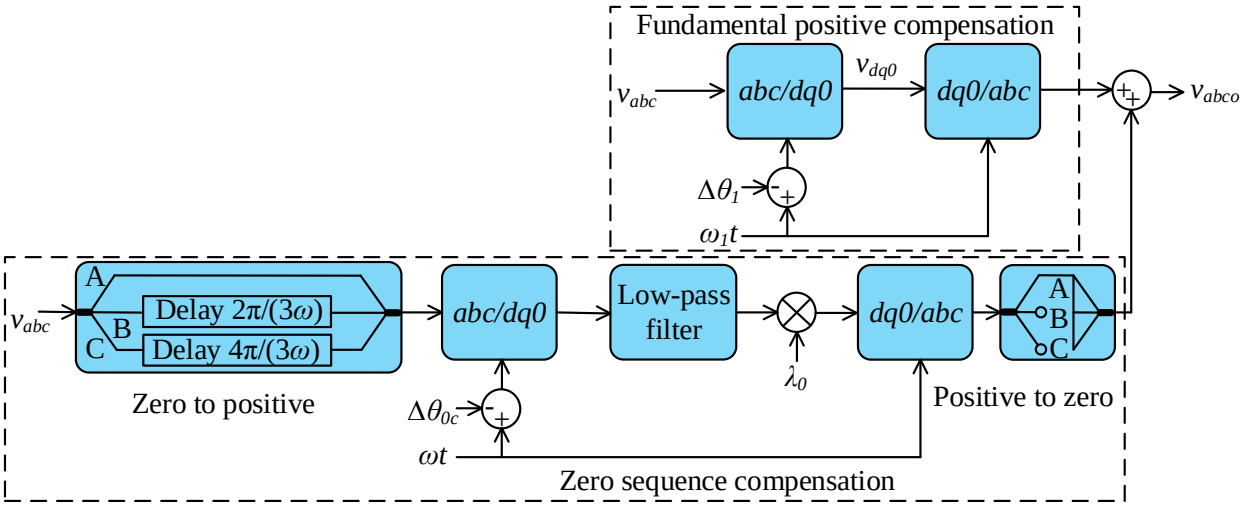


Figure 6-7. Time delay compensation with an added zero sequence correction block.

Assume the required harmonic positive sequence phase angle delay correction is $\Delta\theta_h$, an additional compensation voltage can be added to fully compensate the harmonic positive sequence component, as expressed in (6-30).

$$\begin{bmatrix} v_{ahc} \\ v_{bhc} \\ v_{chc} \end{bmatrix} = \begin{bmatrix} V\cos(\omega t + \Delta\theta_h) \\ V\cos(\omega t - \frac{2\pi}{3} + \Delta\theta_h) \\ V\cos(\omega t + \frac{2\pi}{3} + \Delta\theta_h) \end{bmatrix} - \begin{bmatrix} V\cos(\omega t + \Delta\theta_1) \\ V\cos\left(\omega t - \frac{2\pi}{3} + \Delta\theta_1\right) \\ V\cos\left(\omega t + \frac{2\pi}{3} + \Delta\theta_1\right) \end{bmatrix} \tag{6-30}$$

Solve (6-30), get (6-31), and A_n and B_n are expressed in (6-32).

$$\begin{bmatrix} v_{ahc} \\ v_{bhc} \\ v_{chc} \end{bmatrix} = V \begin{bmatrix} \mathrm{A}_h\cos(\omega t) - \mathrm{B}_h\sin(\omega t) \\ \mathrm{A}_h\cos\left(\omega t - \frac{2\pi}{3}\right) - \mathrm{B}_h\sin\left(\omega t - \frac{2\pi}{3}\right) \\ \mathrm{A}_h\cos\left(\omega t + \frac{2\pi}{3}\right) - \mathrm{B}_h\sin\left(\omega t + \frac{2\pi}{3}\right) \end{bmatrix} \tag{6-31}$$

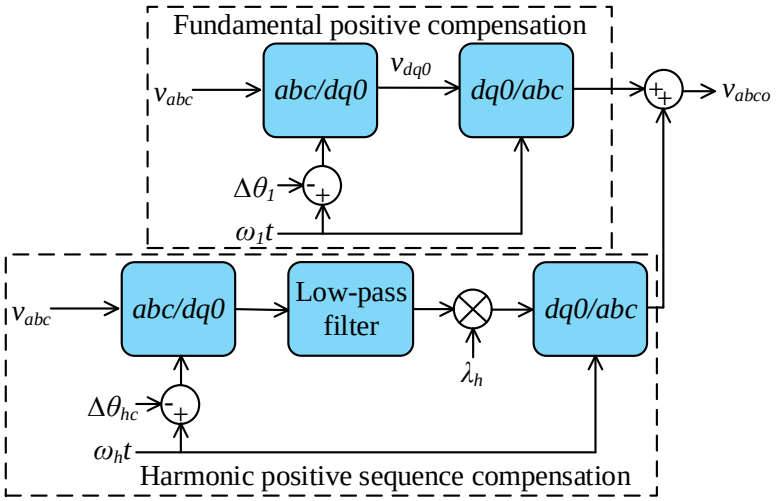


Figure 6-8. Time-delay compensation with added harmonic positive sequence correction blocks.

$$\begin{cases} A_h = \cos(\Delta\theta_h) - \cos(\Delta\theta_1) \\ B_h = \sin(\Delta\theta_h) - \sin(\Delta\theta_1) \end{cases} \tag{6-32}$$

Solve (6-32), get (6-33), and λ_h and $\Delta\theta_{hc}$ are expressed in (6-34).

$$\begin{bmatrix} v_{ahc} \\ v_{bhc} \\ v_{chc} \end{bmatrix} = \lambda_h V \begin{bmatrix} \cos(\omega t + \Delta\theta_{hc}) \\ \cos(\omega t - \frac{2\pi}{3} + \Delta\theta_{hc}) \\ \cos(\omega t + \frac{2\pi}{3} + \Delta\theta_{hc}) \end{bmatrix} \tag{6-33}$$

$$\begin{cases} \lambda_h = \sqrt{{A_h}^2 + {B_h}^2} = \sqrt{(\cos(\Delta\theta_h) - \cos(\Delta\theta_1))^2 + (\sin(\Delta\theta_h) - \sin(\Delta\theta_1))^2} \\ \Delta\theta_{hc} = \arctan\left(\frac{B_h}{A_h}\right) + \pi = \arctan\left(\frac{\sin(\Delta\theta_h) - \sin(\Delta\theta_1)}{\cos(\Delta\theta_h) - \cos(\Delta\theta_1)}\right) + \pi \end{cases} \tag{6-34}$$

An additional function block can be added to fully compensate the angle-delay of the harmonic positive sequence component, as shown in Figure 6-8.

The positive sequence component with a frequency ω is transferred to a dc component through the *abc*/*dq0* transformation. The low-pass filter filters out all the other components except for the positive sequence component under the frequency ω. By adding the angle $\Delta\theta_{hc}$ and multiplying a coefficient λ_h, the required correction voltage in (6-33) for the harmonic positive sequence component can be acquired.

6.3 Hybrid Emulation Stability Analysis with Two Interfaces

To separate a meshed network into two subsystems for hybrid emulation, at least two interfaces need to be developed. To simplify the stability analysis and get a more general conclusion, a hybrid emulation system with two interfaces based on ITM algorithms, named as "interface 1" and "interface 2" in this dissertation, respectively, is simplified as in Figure 6-9. The original system is separated into two subsystems, named as "subsystem 1" and "subsystem 2", by the two interfaces.

The separation "interface 1" is located at the line connection between node N_{11} and node N_{12}. The separation "interface 2" is located at the line connection between node N_{21} and node N_{22}. The time-delays in "interface 1" and "interface 2" are Δt_1 and Δt_2, respectively.

The equivalent voltage source and impedance connected on node N_{11}, node N_{12}, node N_{21}, and node N_{22} are identified as E_{11} and Z_{11}, E_{12} and Z_{12}, E_{21} and Z_{21}, and E_{22} and Z_{22}, respectively. The equivalent impedance between node N_{11} and node N_{21} is identified as Z_{51}. The equivalent impedance between node N_{12} and node N_{22} is identified as Z_{52}.

The node N_{11}, node N_{12}, node N_{21}, and node N_{22} voltage and current equations are expressed in (6-35) and (6-36), respectively.

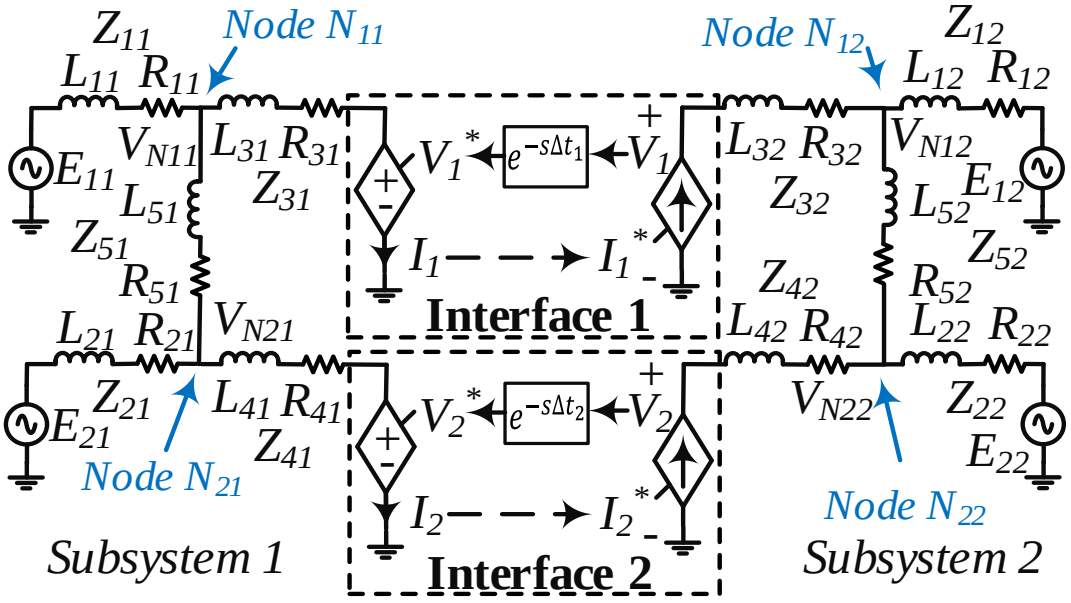


Figure 6-9. Hybrid emulation system with two interfaces based on ITM algorithms.

$$\begin{cases} V_{N11}(s) = V_1(s)e^{-s\Delta t_1} + I_1(s)Z_{31}(s) \\ V_{N21}(s) = V_2(s)e^{-s\Delta t_2} + I_2(s)Z_{41}(s) \\ V_{N12}(s) = V_1(s) - I_1(s)Z_{32}(s) \\ V_{N22}(s) = V_2(s) - I_2(s)Z_{42}(s) \end{cases} \tag{6-35}$$

$$\begin{cases} \dfrac{V_{N11}(s) - V_{N21}(s)}{Z_{51}(s)} = \dfrac{E_{11}(s) - V_{N11}(s)}{Z_{11}(s)} - I_1(s) = I_2(s) - \dfrac{E_{21}(s) - V_{N21}(s)}{Z_{21}(s)} \\ \dfrac{V_{N12}(s) - V_{N22}(s)}{Z_{52}(s)} = \dfrac{E_{12}(s) - V_{N12}(s)}{Z_{12}(s)} + I_1(s) = -I_2(s) - \dfrac{E_{22}(s) - V_{N22}(s)}{Z_{22}(s)} \end{cases} \tag{6-36}$$

Submit (6-35) into (6-36), get (6-37), (6-38), (6-39), and (6-40).

$$\begin{aligned} &Z_{21}(s)\big(Z_{11}(s) + Z_{31}(s)\big)I_1(s) + Z_{11}(s)\big(Z_{21}(s) + Z_{41}(s)\big)I_2(s) + \\ &Z_{21}(s)e^{-s\Delta t_1}V_1(s) + Z_{11}(s)e^{-s\Delta t_2}V_2(s) = Z_{21}(s)E_{11}(s) + Z_{11}(s)E_{21}(s) \end{aligned} \tag{6-37}$$

$$\big(Z_{11}(s)Z_{31}(s)+Z_{11}(s)Z_{51}(s)+Z_{31}(s)Z_{51}(s)\big)I_1(s)-Z_{11}(s)Z_{41}(s)I_2(s)+\big(Z_{11}(s)+Z_{51}(s)\big)e^{-s\Delta t_1}V_1(s)-Z_{11}(s)e^{-s\Delta t_2}V_2(s)=Z_{51}(s)E_{11}(s) \tag{6-38}$$

$$Z_{22}(s)\big(Z_{12}(s)+Z_{32}(s)\big)I_1(s)+Z_{12}(s)\big(Z_{22}(s)+Z_{42}(s)\big)I_2(s)-Z_{22}(s)V_1(s)-Z_{12}(s)V_2(s)=-Z_{22}(s)E_{12}(s)-Z_{12}(s)E_{22}(s) \tag{6-39}$$

$$\big(Z_{12}(s)Z_{32}(s)+Z_{12}(s)Z_{52}(s)+Z_{32}(s)Z_{52}(s)\big)I_1(s)-Z_{12}(s)Z_{42}(s)I_2(s)-\big(Z_{12}(s)+Z_{52}(s)\big)V_1(s)+Z_{12}(s)V_2(s)=-Z_{52}(s)E_{12}(s) \tag{6-40}$$

Eliminate $V_1(s)$ and $V_2(s)$ from (6-37), (6-38), (6-39), and (6-40), results in (6-41) and (6-42).

$$\begin{aligned}&\big(-Z_{11}(s)^2Z_{12}(s)Z_{21}(s)e^{-s\Delta t_1}-Z_{11}(s)Z_{22}(s)\big(Z_{11}(s)Z_{21}(s)+Z_{21}(s)Z_{31}(s)+\\&Z_{11}(s)Z_{31}(s)+Z_{11}(s)Z_{51}(s)+Z_{31}(s)Z_{51}(s)\big)e^{-s\Delta t_2}-Z_{11}(s)Z_{22}(s)\big(Z_{12}(s)+\\&Z_{32}(s)\big)\big(Z_{11}(s)+Z_{21}(s)+Z_{51}(s)\big)e^{-s(\Delta t_1+\Delta t_2)}\big)I_1(s)+\\&\Big(-Z_{11}(s)Z_{12}(s)\Big(Z_{21}(s)Z_{41}(s)+\big(Z_{21}(s)+Z_{41}(s)\big)\big(Z_{11}(s)+Z_{51}(s)\big)\Big)e^{-s\Delta t_1}-\\&Z_{11}(s)^2Z_{21}(s)Z_{22}(s)e^{-s\Delta t_2}-Z_{11}(s)Z_{12}(s)\big(Z_{22}(s)+Z_{42}(s)\big)\big(Z_{11}(s)+Z_{21}(s)+\\&Z_{51}(s)\big)e^{-s(\Delta t_1+\Delta t_2)}\Big)I_2(s)=-Z_{11}(s)Z_{12}(s)\Big(Z_{21}(s)E_{11}(s)+\big(Z_{11}(s)+\\&Z_{51}(s)\big)E_{21}(s)\Big)e^{-s\Delta t_1}-Z_{11}(s)Z_{22}(s)\Big(\big(Z_{21}(s)+Z_{51}(s)\big)E_{11}(s)+\\&Z_{11}(s)E_{21}(s)\Big)e^{-s\Delta t_2}+Z_{11}(s)\big(Z_{11}(s)+Z_{21}(s)+Z_{51}(s)\big)\big(Z_{22}(s)E_{12}(s)+\\&Z_{12}(s)E_{22}(s)\big)e^{-s(\Delta t_1+\Delta t_2)}\end{aligned} \tag{6-41}$$

$$\Big(\big(Z_{12}(s)+Z_{22}(s)+Z_{52}(s)\big)\big(Z_{11}(s)Z_{21}(s)+Z_{21}(s)Z_{31}(s)+Z_{11}(s)Z_{31}(s)+$$
$$Z_{11}(s)Z_{51}(s)+Z_{31}(s)Z_{51}(s)\big)+\big(Z_{11}(s)+Z_{21}(s)+Z_{51}(s)\big)\big(Z_{12}(s)Z_{22}(s)+$$
$$Z_{22}(s)Z_{32}(s)+Z_{12}(s)Z_{32}(s)+Z_{12}(s)Z_{52}(s)+Z_{32}(s)Z_{52}(s)\big)e^{-s\Delta t_1}\Big)I_1(s)+$$
$$\big(Z_{11}(s)Z_{21}(s)\big(Z_{12}(s)+Z_{22}(s)+Z_{52}(s)\big)+Z_{12}(s)Z_{22}(s)\big(Z_{11}(s)+Z_{21}(s)+ \quad (6\text{-}42)$$
$$Z_{51}(s)\big)e^{-s\Delta t_1}\big)I_2(s)=\big(Z_{12}(s)+Z_{22}(s)+Z_{52}(s)\big)\Big(\big(Z_{21}(s)+Z_{51}(s)\big)E_{11}(s)+$$
$$Z_{11}(s)E_{21}(s)\Big)-\big(Z_{11}(s)+Z_{21}(s)+Z_{51}(s)\big)\Big(\big(Z_{22}(s)+Z_{52}(s)\big)E_{12}(s)+$$
$$Z_{12}(s)E_{22}(s)\Big)e^{-s\Delta t_1}$$

Solving I_1 and I_2 from (6-41) and (6-42), results in (6-43).

$$\begin{cases} I_1=\dfrac{\frac{T_5}{T_1}+\frac{T_6}{T_1}e^{-s\Delta t_1}+\frac{T_7}{T_1}e^{-s\Delta t_2}+\frac{T_8}{T_1}e^{-s(\Delta t_1+\Delta t_2)}}{1+\frac{T_2}{T_1}e^{-s\Delta t_1}+\frac{T_3}{T_1}e^{-s\Delta t_2}+\frac{T_4}{T_1}e^{-s(\Delta t_1+\Delta t_2)}} \\ I_2=\dfrac{\frac{T_9}{T_1}+\frac{T_{10}}{T_1}e^{-s\Delta t_1}+\frac{T_{11}}{T_1}e^{-s\Delta t_2}+\frac{T_{12}}{T_1}e^{-s(\Delta t_1+\Delta t_2)}}{1+\frac{T_2}{T_1}e^{-s\Delta t_1}+\frac{T_3}{T_1}e^{-s\Delta t_2}+\frac{T_4}{T_1}e^{-s(\Delta t_1+\Delta t_2)}} \end{cases} \quad (6\text{-}43)$$

where the symbol T_1, T_2, T_3, T_4, T_5, T_6, T_7, T_8, T_9, T_{10}, T_{11}, and T_{12} represent the expressions in (6-44), (6-45), (6-46), (6-47), (6-48), (6-49), (6-50), (6-51), (6-52), (6-53), (6-54), and (6-55), respectively.

$$T_1=\big(Z_{12}(s)+Z_{22}(s)+Z_{52}(s)\big)\big(Z_{11}(s)Z_{21}(s)Z_{31}(s)+Z_{11}(s)Z_{21}(s)Z_{41}(s)+$$
$$Z_{11}(s)Z_{21}(s)Z_{51}(s)+Z_{11}(s)Z_{31}(s)Z_{41}(s)+Z_{11}(s)Z_{41}(s)Z_{51}(s)+ \quad (6\text{-}44)$$
$$Z_{21}(s)Z_{31}(s)Z_{41}(s)+Z_{21}(s)Z_{31}(s)Z_{51}(s)+Z_{31}(s)Z_{41}(s)Z_{51}(s)\big)$$

$$T_2 = \Big(Z_{12}(s)Z_{22}(s) + Z_{12}(s)Z_{52}(s) + Z_{32}(s)\big(Z_{12}(s) + Z_{22}(s) + Z_{52}(s)\big)\Big)\Big(Z_{11}(s)Z_{21}(s) + Z_{21}(s)Z_{51}(s) + Z_{41}(s)\big(Z_{11}(s) + Z_{21}(s) + Z_{51}(s)\big)\Big) - Z_{11}(s)Z_{12}(s)Z_{21}(s)Z_{22}(s) \tag{6-45}$$

$$T_3 = \Big(Z_{11}(s)Z_{21}(s) + Z_{11}(s)Z_{51}(s) + Z_{31}(s)\big(Z_{11}(s) + Z_{21}(s) + Z_{51}(s)\big)\Big)\Big(Z_{12}(s)Z_{22}(s) + Z_{22}(s)Z_{52}(s) + Z_{42}(s)\big(Z_{12}(s) + Z_{22}(s) + Z_{52}(s)\big)\Big) - Z_{11}(s)Z_{12}(s)Z_{21}(s)Z_{22}(s) \tag{6-46}$$

$$T_4 = \big(Z_{11}(s) + Z_{21}(s) + Z_{51}(s)\big)\big(Z_{12}(s)Z_{22}(s)Z_{32}(s) + Z_{12}(s)Z_{22}(s)Z_{42}(s) + Z_{12}(s)Z_{22}(s)Z_{52}(s) + Z_{12}(s)Z_{32}(s)Z_{42}(s) + Z_{12}(s)Z_{42}(s)Z_{52}(s) + Z_{22}(s)Z_{32}(s)Z_{42}(s) + Z_{22}(s)Z_{32}(s)Z_{52}(s) + Z_{32}(s)Z_{42}(s)Z_{52}(s)\big) \tag{6-47}$$

$$T_5 = \big(Z_{12}(s) + Z_{22}(s) + Z_{52}(s)\big)\Big(\big(Z_{21}(s)Z_{41}(s) + Z_{21}(s)Z_{51}(s) + Z_{41}(s)Z_{51}(s)\big)E_{11}(s) + Z_{11}(s)Z_{41}(s)E_{21}(s)\Big) \tag{6-48}$$

$$T_6 = -\Big(\Big(Z_{21}(s)Z_{41}(s) + \big(Z_{21}(s) + Z_{41}(s)\big)\big(Z_{11}(s) + Z_{51}(s)\big)\Big)\Big(\big(Z_{22}(s) + Z_{52}(s)\big)E_{12}(s) + Z_{12}(s)E_{22}(s)\Big) + Z_{12}(s)Z_{22}(s)\Big(Z_{21}(s)E_{11}(s) + \big(Z_{11}(s) + Z_{51}(s)\big)E_{21}(s)\Big)\Big) \tag{6-49}$$

$$T_7 = \Big(\big(Z_{12}(s) + Z_{52}(s)\big)\big(Z_{22}(s) + Z_{42}(s)\big) + Z_{22}(s)Z_{42}(s)\Big)\Big(\big(Z_{21}(s) + Z_{51}(s)\big)E_{11}(s) + Z_{11}(s)E_{21}(s)\Big) + Z_{11}(s)Z_{21}(s)\Big(Z_{22}(s)E_{12}(s) + \big(Z_{12}(s) + Z_{52}(s)\big)E_{22}(s)\Big) \tag{6-50}$$

$$T_8 = -\big(Z_{11}(s) + Z_{21}(s) + Z_{51}(s)\big)\Big(\big(Z_{22}(s)Z_{42}(s) + Z_{22}(s)Z_{52}(s) + Z_{42}(s)Z_{52}(s)\big)E_{12}(s) + Z_{12}(s)Z_{42}E_{22}(s)\Big) \tag{6-51}$$

$$T_9 = \big(Z_{12}(s) + Z_{22}(s) + Z_{52}(s)\big)\Big(\big(Z_{11}(s)Z_{31}(s) + Z_{11}(s)Z_{51}(s) + Z_{31}(s)Z_{51}(s)\big)E_{21}(s) + Z_{21}(s)Z_{31}(s)E_{11}(s)\Big) \tag{6-52}$$

$$T_{10} = \Big(\big(Z_{22}(s) + Z_{52}(s)\big)\big(Z_{12}(s) + Z_{32}(s)\big) + Z_{12}(s)Z_{32}(s)\Big)\Big(\big(Z_{11}(s) + Z_{51}(s)\big)E_{21}(s) + Z_{21}(s)E_{11}(s)\Big) + Z_{21}(s)Z_{11}(s)\Big(Z_{12}(s)E_{22}(s) + \big(Z_{22}(s) + Z_{52}(s)\big)E_{12}(s)\Big) \tag{6-53}$$

$$T_{11} = -\Big(\big(Z_{11}(s)Z_{31}(s) + \big(Z_{11}(s) + Z_{31}(s)\big)\big(Z_{21}(s) + Z_{51}(s)\big)\big)\Big)\Big(\big(Z_{12}(s) + Z_{52}(s)\big)E_{22}(s) + Z_{22}(s)E_{12}(s)\Big) + Z_{22}(s)Z_{12}(s)\Big(Z_{11}(s)E_{21}(s) + \big(Z_{21}(s) + Z_{51}(s)\big)E_{11}(s)\big)\Big)\Big) \tag{6-54}$$

$$T_{12} = -\big(Z_{11}(s) + Z_{21}(s) + Z_{51}(s)\big)\Big(\big(Z_{12}(s)Z_{32}(s) + Z_{12}(s)Z_{52}(s) + Z_{32}(s)Z_{52}(s)\big)E_{22}(s) + Z_{22}(s)Z_{32}E_{12}(s)\Big) \tag{6-55}$$

For a special case, if breaking the connections between node N_{11} and node N_{21} and between node N_{12} and node N_{22} by setting Z_{51} and Z_{52} to infinite, the original ring network is divided into two individual two-area systems, which are the top one with E_{11}, Z_{11}, Z_{31}, Z_{32}, Z_{12}, and E_{12} and the bottom two-area system with E_{21}, Z_{21}, Z_{41}, Z_{42}, Z_{22}, and E_{22}, and the currents I_1 and I_2 are derived as in (6-56).

$$\begin{cases} I_1 = \dfrac{\left(\dfrac{E_{11}}{Z_{11}(s)+Z_{31}(s)} - \dfrac{E_{12}}{Z_{11}(s)+Z_{31}(s)} e^{-s\Delta t_1}\right)}{\left(1 + \dfrac{Z_{12}(s)+Z_{32}(s)}{Z_{11}(s)+Z_{31}(s)} e^{-s\Delta t_1}\right)} \\ I_2 = \dfrac{\left(\dfrac{E_{21}}{Z_{21}(s)+Z_{41}(s)} - \dfrac{E_{22}}{Z_{21}(s)+Z_{41}(s)} e^{-s\Delta t_2}\right)}{\left(1 + \dfrac{Z_{22}(s)+Z_{42}(s)}{Z_{21}(s)+Z_{41}(s)} e^{-s\Delta t_2}\right)} \end{cases} \tag{6-56}$$

which match with the result in (6-9).

According to (6-43), taking E_{11}, E_{12}, E_{21}, or E_{22} as the input and I_1 or I_2 as the output, the denominator of the closed-loop transfer function is the denominator in (6-43). Thus, the open-loop transfer function $G_o(s)$ can be obtained as in (6-57).

$$G_o(s) = \frac{T_2}{T_1} e^{-s\Delta t_1} + \frac{T_3}{T_1} e^{-s\Delta t_2} + \frac{T_4}{T_1} e^{-s(\Delta t_1 + \Delta t_2)} \tag{6-57}$$

The system stability can be evaluated by the open-loop transfer function $G_o(s)$ with corresponding parameters of the targeted emulation system. Specifically, in order to provide a general guidance for the system separation considering stability, if the magnitude of the open-loop transfer function is smaller than 1, there is no 0 dB crossing point in the amplitude-frequency curve, which means that the phase margin is infinite. Thus, the system is assured to be stable when (6-58) is satisfied.

$$|G_o(s)| = \left|\frac{T_2}{T_1} e^{-s\Delta t_1} + \frac{T_3}{T_1} e^{-s\Delta t_2} + \frac{T_4}{T_1} e^{-s(\Delta t_1 + \Delta t_2)}\right| < 1 \tag{6-58}$$

To be more conservative on (6-58), the system is assured to be stable if (6-59) is satisfied.

$$\frac{|T_2| + |T_3| + |T_4|}{|T_1|} < 1 \tag{6-59}$$

According to (6-44), (6-45), (6-46), and (6-47), the majority of variables in T_1 and T_4 are from "subsystem 1" and "subsystem 2", respectively, and the variables in T_2 and T_3 are distributed evenly in "subsystem 1" and "subsystem 2". Larger impedances at the controlled voltage side (Z_{11}, Z_{21}, Z_{31}, Z_{41}, Z_{51}) than the controlled current side (Z_{12}, Z_{22}, Z_{32}, Z_{42}, Z_{52}) helps to stabilize the hybrid emulation with two interfaces. Especially, allocating all impedances of the two separation lines (between node N_{11} and N_{12} and between node N_{21} and N_{22}) to the controlled voltage side, which means Z_{32} and Z_{42} are set to zero, makes the emulation system more stable.

6.4 Hardware Configuration and Software Implementation

6.4.1 Hardware Configuration

The developed hybrid emulation platform is composed of the RTDS, HTB and hybrid emulation interfaces, as shown in Figure 6-10. In the RTDS, G_i (i = 1, 2, ⋯ n) represents generator i and LD_j (j = 1, 2, ⋯ m) represents load j. In the HTB, each converter serves as an emulating unit by programming the DSP based converter controller. Two hybrid emulation interfaces, which are interface 1 and interface 2, are built to extend the capability and flexibility of the hybrid emulation platform. Each hybrid emulation interface has a digital interface at the RTDS side and a power interface at the HTB side.

The power interface, which is connected to the HTB emulation subsystem, is controlled as a voltage or current source, depending on the selected interface algorithm. The power interface voltage and current references come from the RTDS. The digital interface, which is connected to the RTDS subsystem, resides in the RTDS and is composed of controlled current source and controlled voltage source models. The digital interface voltage and current references come from the output voltage and current measurements of the power interface.

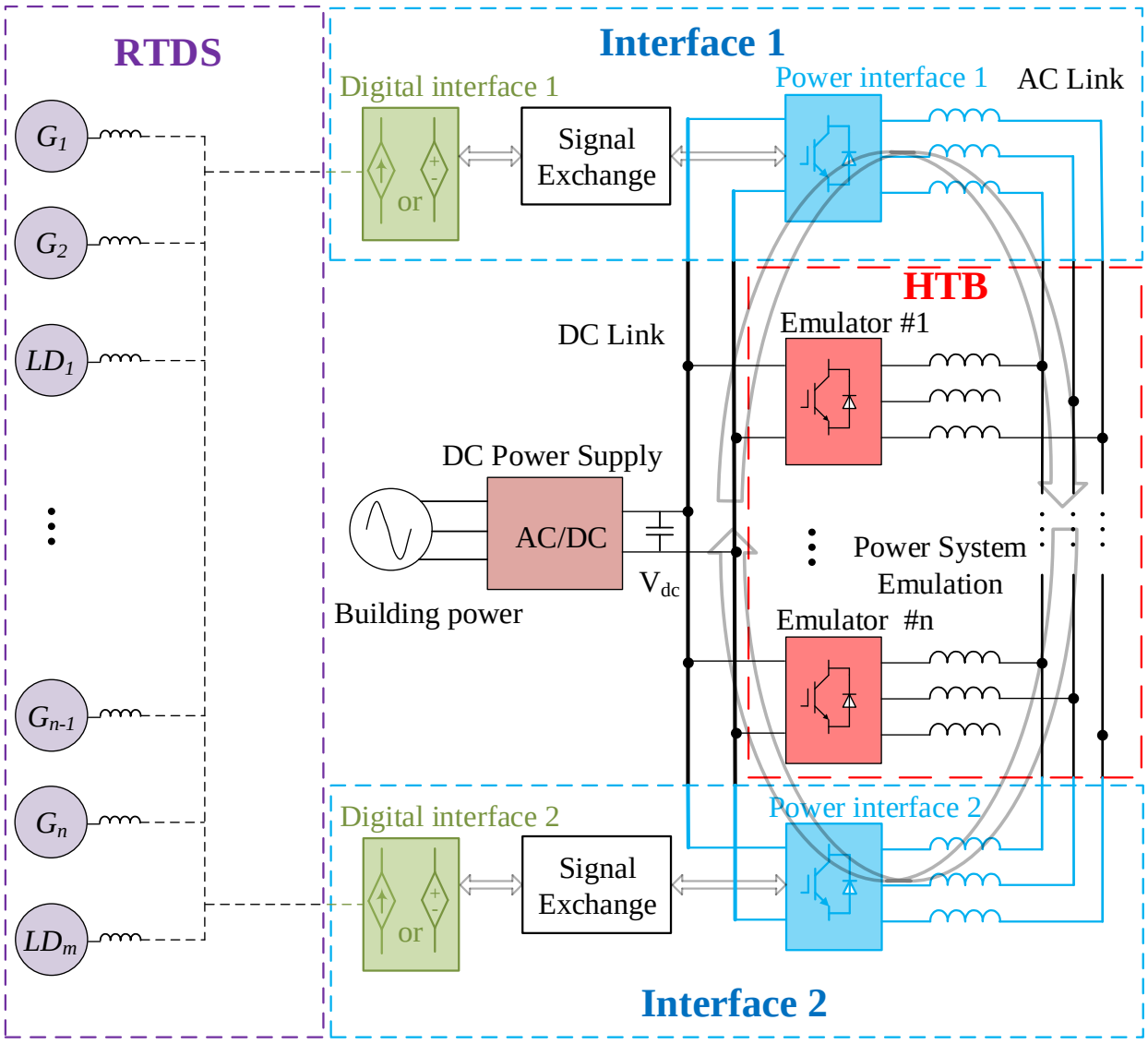


Figure 6-10. RTDS and HTB hybrid emulation configuration.

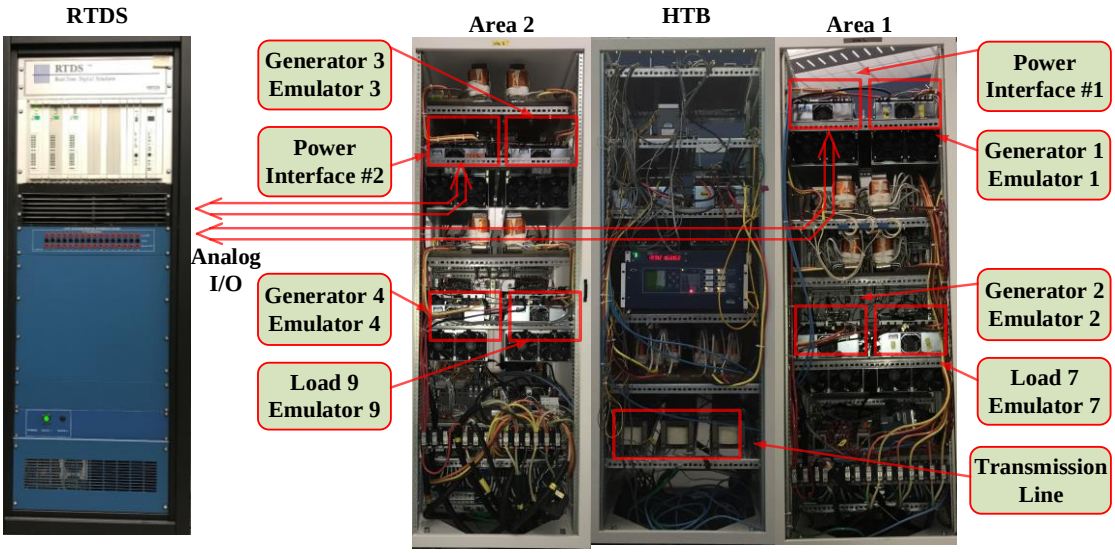


Figure 6-11. Hybrid emulation converter cluster and RTDS.

The converter cluster of the HTB and power interfaces has a paralleled construction, as shown in Figure 6-10. The converters share the same dc link, which has a dc power supply to maintain a constant dc voltage. The ac link connection of the converters can be configured as an emulated power system. Although each converter is controlled to export or absorb certain active power by the emulation requirements, the dc power supply only needs to compensate the converter power loss because of the power circulation through the dc link.

In this dissertation, one RTDS Rack and two area cabinets with converters rated at 600 V and 75 kW are built as the hybrid emulation platform, as shown in Figure 6-11. In each area cabinet, three of the four converters are programmed as HTB emulators, and the other converter serves as the power interface of the hybrid emulation. The output voltage and current measurement signals of the power interface are sent to the RTDS through the RTDS Giga-

Transceiver Analogue Input (GTAI) card. The power interface voltage and current references are sent to the power interface controller through the RTDS Giga-Transceiver Analogue Output (GTAO) card.

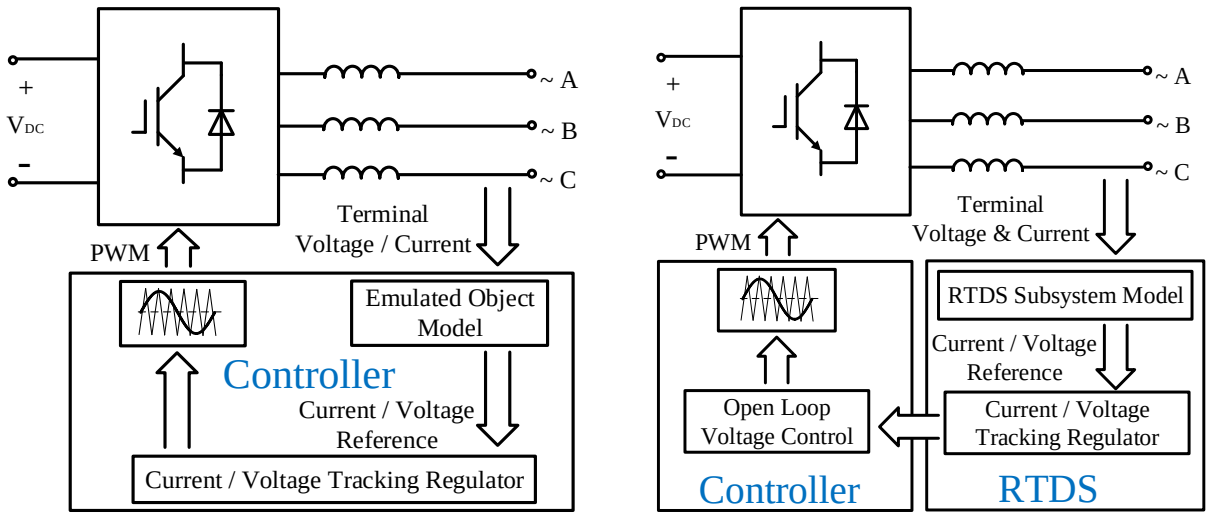
The rated power and voltage of the emulated power system are usually too large to be directly emulated in the HTB, thus scaled-down parameters are implemented in the HTB to keep the same performance as the original power system by maintaining the same per-unit values. Different from the HTB, the subsystem in the RTDS is calculated digitally without the restriction of actual power and voltage, so the original subsystem can be implemented in the RTDS directly.

6.4.2 Converter Control

Within the HTB, each converter is controlled to have the same steady state and dynamic characteristics as the emulated component by tracking the voltage reference based on the terminal current or tracking the current reference based on the terminal voltage, as shown in Figure 6-12(a).

For example, if a synchronous generator is emulated, the Digital Signal Processor (DSP)-based controller calculates the terminal voltage reference by solving the synchronous generator model, which corresponds to the "Emulated Object Model" block in Figure 6-12(a), with the terminal current measurement, and then the controller "Current/Voltage Tracking Regulator" block regulates the terminal voltage to track the derived voltage reference through a closed-loop control with the terminal voltage feedback.

The power interface converter is controlled to behave at the A, B, C terminals the same as the subsystem simulated in the RTDS by tracking the voltage or current reference, which comes from the digital interface terminal of the RTDS subsystem, as shown in Figure 6-12(b).



(a) (b)

Figure 6-12. Basic converter control in RTDS and HTB hybrid emulation: (a) HTB emulator converter control; (b) Power interface converter control.

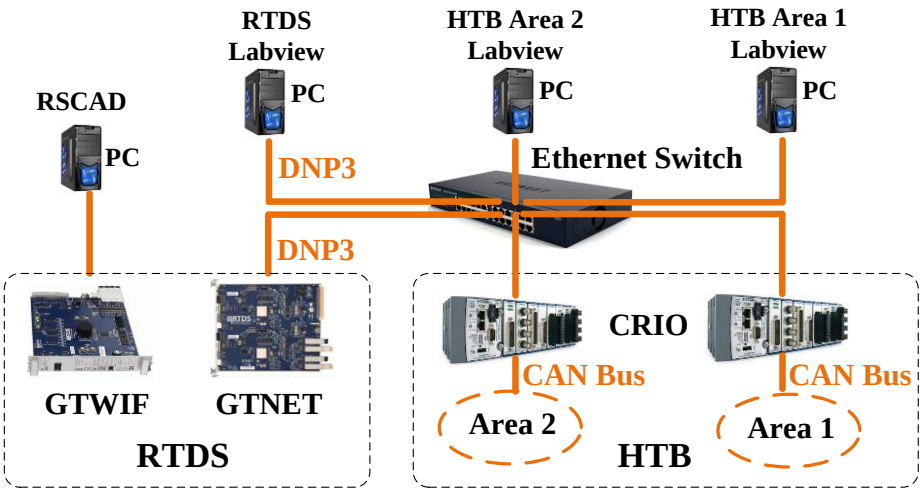


Figure 6-13. Hybrid emulation communication and HMI structure.

The voltage reference is tracked if the voltage source ITM interface algorithm is selected, otherwise, the current reference is tracked under the current source ITM interface algorithm. Instead of in the DSP-based power interface converter controller, the current or voltage closed-loop tracking control function is realized in the RTDS by the "Current/Voltage Tracking Regulator" block with the converter terminal current or voltage feedback. The power interface controller operates under an open-loop condition by directly generating the switching signal with the received modulation signal from the RTDS "Current/Voltage Tracking Regulator" block.

6.4.3 Hybrid Emulation Platform Communication System

Figure 6-13 shows the communication system of the hybrid emulation platform. A CompactRIO (CRIO), which is a real-time embedded industrial controller from National Instruments (NI), is implemented in each area cabinet to serve as the local controller by communicating with the controller of each emulator through a CAN bus. A personal computer (PC) running Labview serves as the control center for each area by communicating with the CRIO through an Ethernet switch. The DNP3 protocol is implemented in both the RTDS GTNET card and the PC Labview to realize the communication between the RTDS and the control center. A PC running RSCAD software operates the RTDS through the GTWIF card.

In this dissertation, the Labview and RTDS DNP3 models are defined as master station and follower station, respectively. The master station exchanges data with the follower station by polling the follower station periodically. The DNP3 master station model running in Labview is shown in Figure 6-14. The follower station IP address, internet port number and baud rate are defined in the DNP3 master station settings. The analog input, analog output and binary output are implemented in this application.

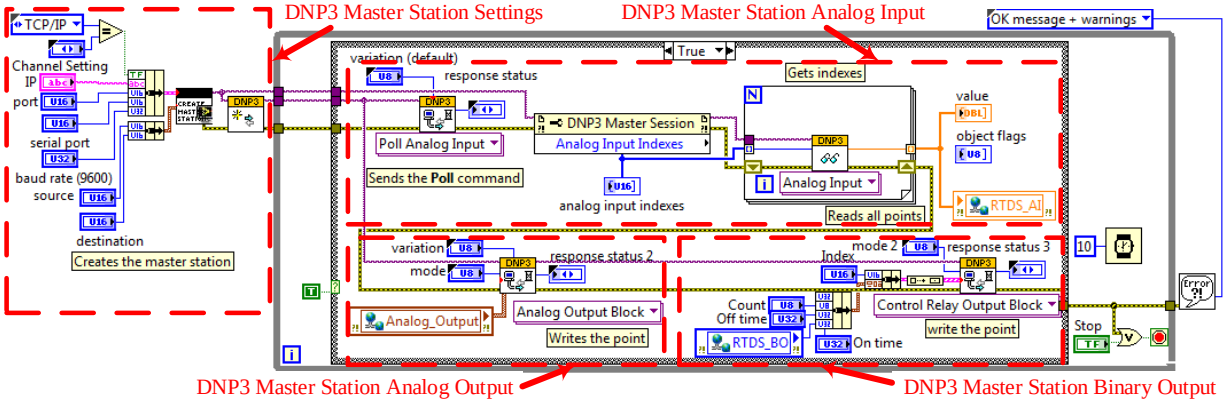
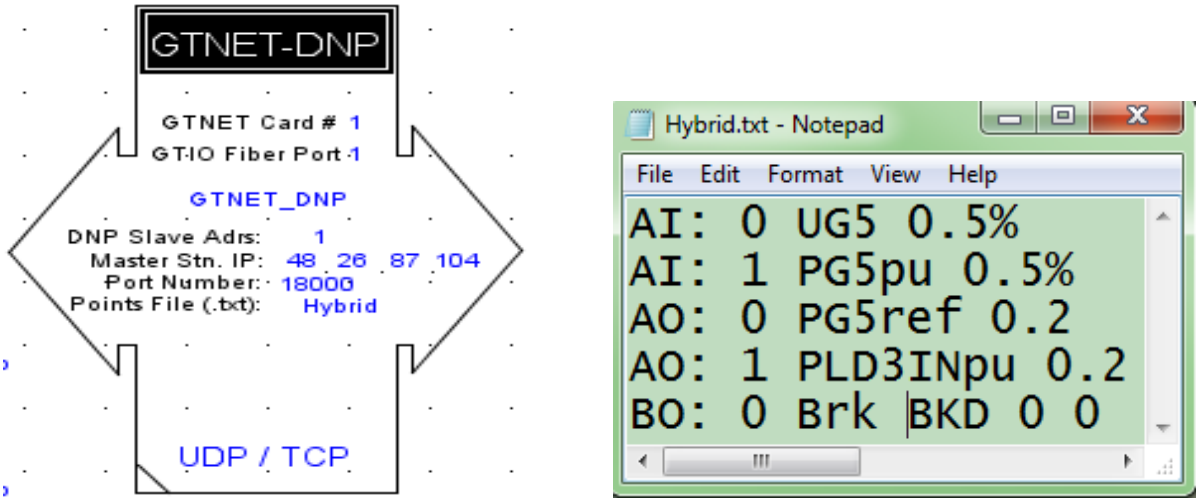


Figure 6-14. Labview DNP3 communication model.



(a) (b)

Figure 6-15. Example of the RTDS DNP3 communication model: (a) DNP3 follower station model; (b) Data exchange file.

The DNP3 follower station model running in the RTDS is shown in Figure 6-15(a). The DNP3 follower address, master station IP address and internet port number are defined. The points file (.txt) named as "Hybrid" defines the data exchanged, as shown in Figure 6-15(b).

6.5 Simulation and Experiment Results

6.5.1 Hybrid Emulation Results with One Interface

Although the hybrid emulation platform with the RTDS and HTB is developed to realize relatively large-scale system emulations, a typical two-area system is employed to verify the effectiveness of the developed hybrid emulation platform with one interface. The scaled-down two-area system with the given parameters of the generators and loads is shown in Figure 6-16. G_i (i = 1, 2, 3, 4) is a synchronous generator with a mechanical power input P_{Gi} and a terminal voltage reference V_{Gi}. LD_j (j = 7, 9) is a load with an active power reference P_{LDj} and a reactive power reference Q_{LDj}. The pure HTB emulation and pure digital simulation based on the same system as the hybrid emulation are conducted to verify the hybrid emulation performance.

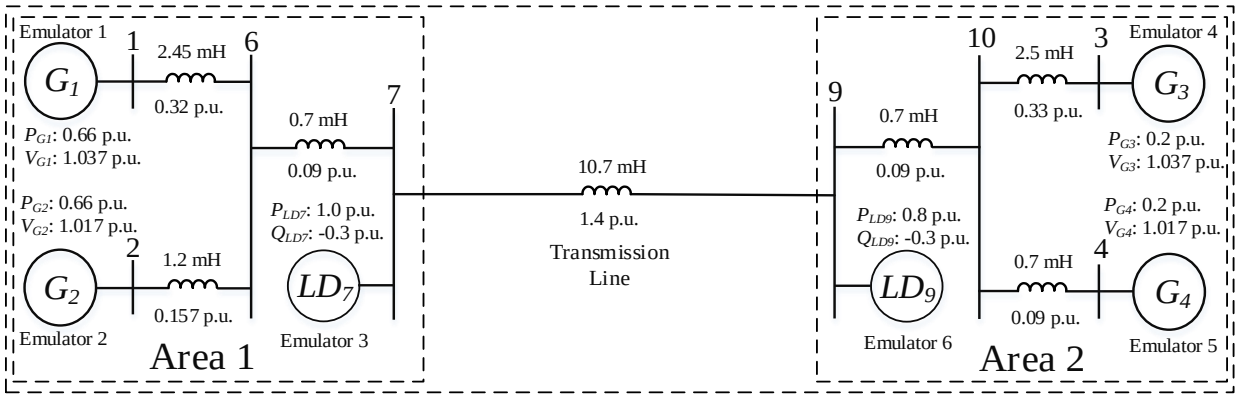
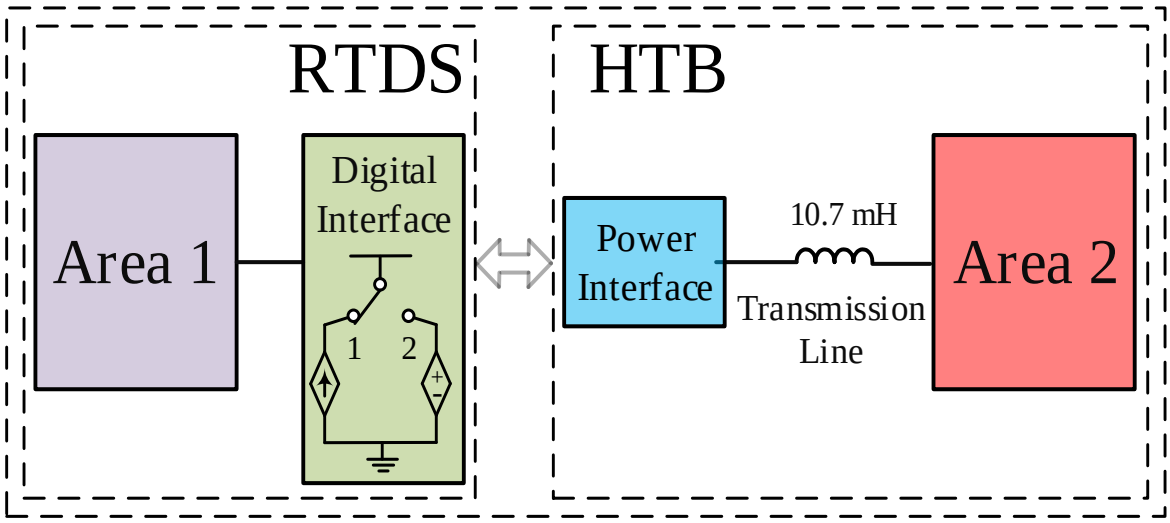
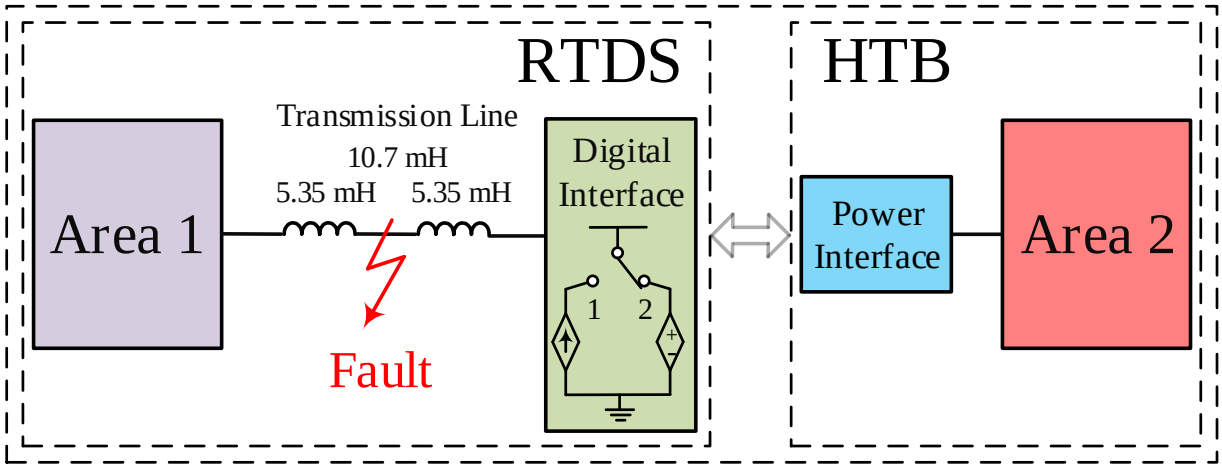


Figure 6-16. Scaled-down two-area system.



(a)



(b)

Figure 6-17. Hybrid emulation of two-area system: (a) Transmission line in HTB; (b) Transmission line in RTDS.

In this thesis, two complementary cases of the two-area system are emulated in the hybrid emulation platform separately to verify the implemented voltage source and current source ITM algorithms. When the transmission line between Area 1 and Area 2 is emulated in the HTB, the equivalent impedance in the digital side is smaller than the hardware side, then the voltage source ITM algorithm is implemented by selecting the single-pole double-throw switch to position "1", as shown in Figure 6-17(a). On the contrary, the current source ITM algorithm is utilized by selecting the single-pole double-throw switch to position "2" if the transmission line between Area 1 and Area 2 is simulated in the RTDS, as shown in Figure 6-17(b).

- Case I: Load step change scenario

Figure 6-18, Figure 6-19, and Figure 6-20 show the G_3 frequency, G_3 active power, and LD_9 active power comparisons, respectively, between the hybrid emulation and the pure HTB emulation when there is a step change of LD_9 from 0.8 p.u. to 0.4 p.u. at 2.5s. The hybrid emulation matches with the pure HTB emulation since the hybrid emulation waveforms are similar to that of the pure HTB emulation.

- Case II: Transmission line fault scenario

Figure 6-21 and Figure 6-22 show the waveform comparisons between the hybrid emulation and the pure digital simulation based on MATLAB/Simulink when a three-phase short-circuit fault happens at the middle point of the transmission line between the two areas. The three-phase short-circuit fault happens at 6 s with 0.15 s duration. The system returns to the original operation point gradually with damped oscillations after the short-circuit fault disappears at 6.15 s. Figure 6-21 and Figure 6-22 show the G_3 frequency and G_3 active power comparisons, respectively. The hybrid emulation matches well with the pure digital simulation.

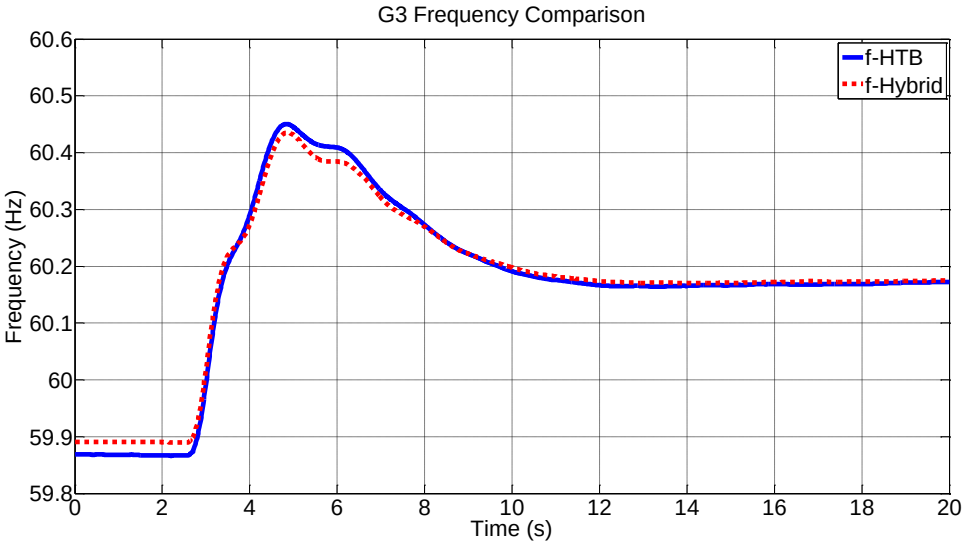


Figure 6-18. G_3 frequency comparison between the hybrid emulation and the pure HTB emulation during the load step change.

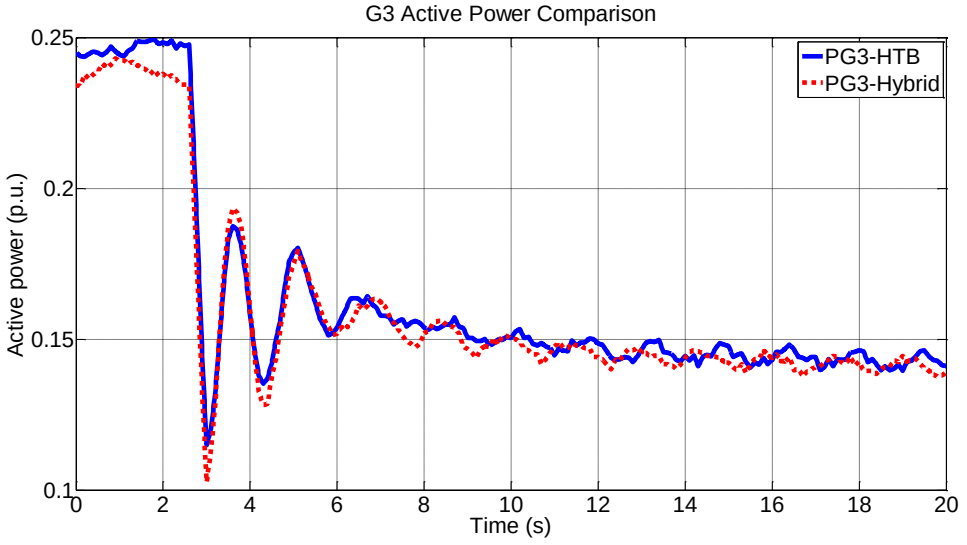


Figure 6-19. G_3 active power comparison between the hybrid emulation and the pure HTB emulation during the load step change.

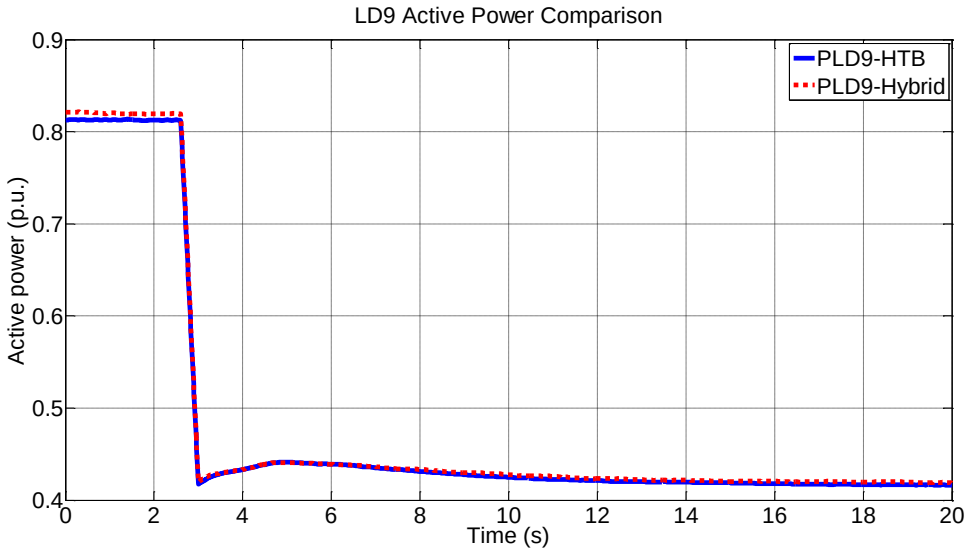


Figure 6-20. *LD9* active power comparison between the hybrid emulation and the pure HTB emulation during the load step change.

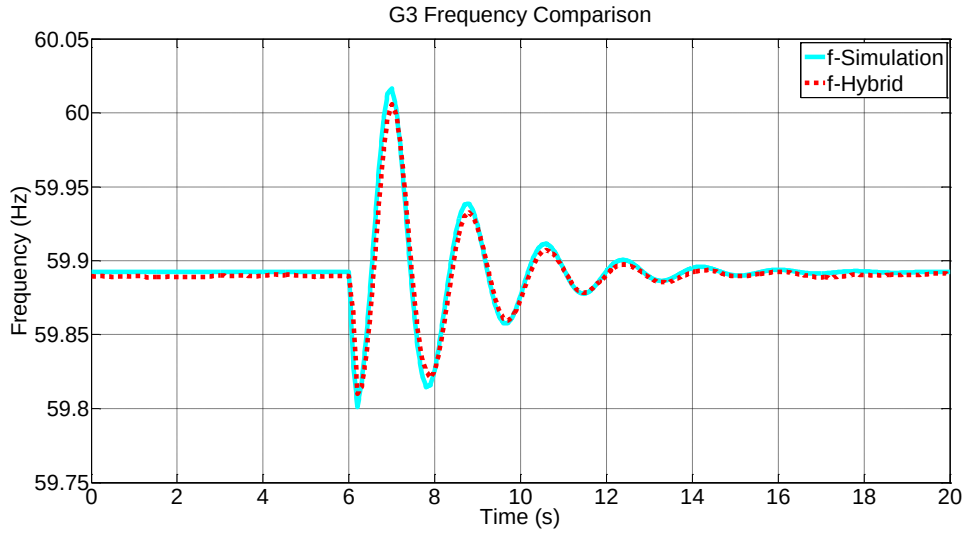


Figure 6-21. *G3* active power comparison between the hybrid emulation and the pure HTB emulation during the transmission line fault.

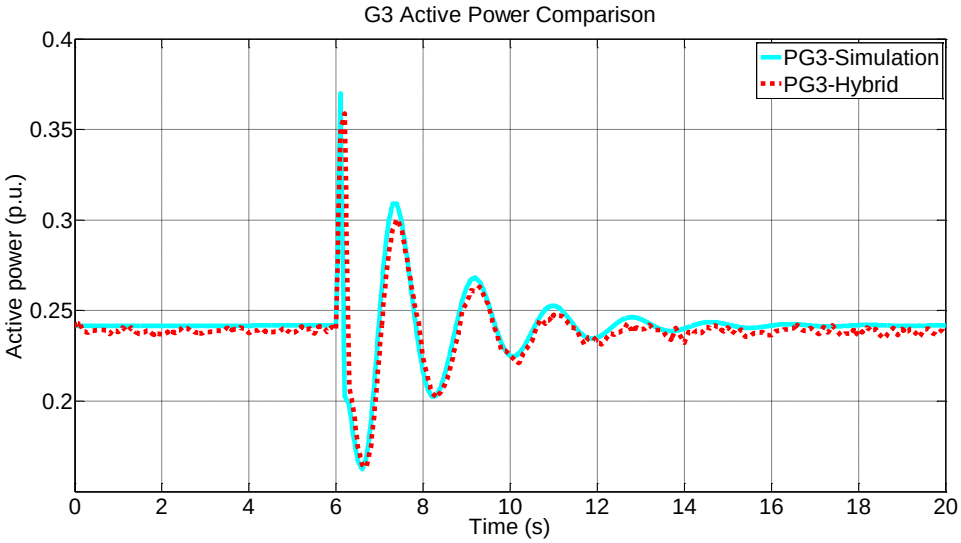


Figure 6-22. G_3 frequency comparison between the hybrid emulation and the pure HTB emulation during the transmission line fault.

Figure 6-23. Northeast Power Coordinating Council (NPCC) system with hypothetical Cape Wind Project system.

6.5.2 Hybrid Emulation Results with Two Interfaces

The hybrid emulation platform with two interfaces is applied to demonstrate the Northeast Power Coordinating Council (NPCC) system with hypothetical Cape Wind Project system, as shown in Figure 6-23. The hypothetical Cape Wind Project system delivers the power of two offshore wind farms to the onshore load center with a multi-terminal dc grid (MTDC).

The NPCC system is reduced and scaled down to be a three-area system for the hybrid emulation system demonstration, as shown in Figure 6-24. G_i (i = 1, 2, 3, 4, 5) is a synchronous generator with a mechanical power input P_{Gi} and a terminal voltage reference V_{Gi}. LD_j (j = 7, 9, 12, 13) is a load with an active reference P_{LDj} and a reactive power reference Q_{LDj}. WF_k (k = 1, 2) is a wind power generator with a mechanical power input P_{WFk}. VSC_l (l = 1, 2, 3, 4) is the MTDC station voltage source converter. VSC_1 and VSC_2 deliver the active power of WF_1 and WF_2 into the MTDC network, respectively. VSC_3 works in the constant dc voltage (V_{dc} = 1.0 p.u.) and constant reactive power (Q_{VSC3} = 0.3 p.u.) mode. VSC4 works in the constant active power (P_{VSC4} = 0.3 p.u.) and constant reactive power (Q_{VSC4} = 0.3 p.u.) mode.

Based on the existing HTB hardware of a two-area system (Area 1, Area 2, and a transmission line between Area 1 and Area 2) and with the help of the hybrid emulation stability analysis with two interfaces in Section 6.3, the current source ITM algorithm is implemented in both hybrid emulation interfaces with the entire line impedances from Area 1 to Area 3 and from Area 2 to Area 3 allocated at the digital side. The scaled-down three-area system is emulated in the hybrid emulation platform with two interfaces, as shown in Figure 6-25. Area 1, Area 2, and the transmission line between them are emulated in the HTB. Area 3, the transmission line between Area 1 and Area 3, and the transmission line between Area 2 and Area 3 are simulated in the RTDS.

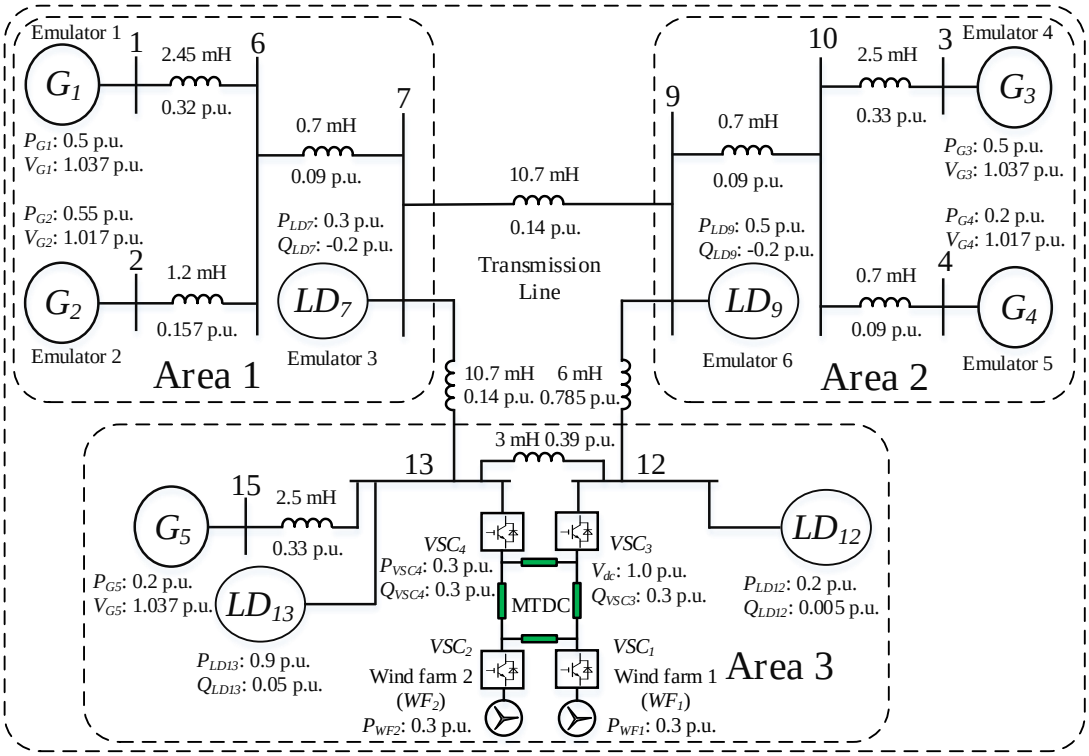


Figure 6-24. Three-area system with offshore wind farm.

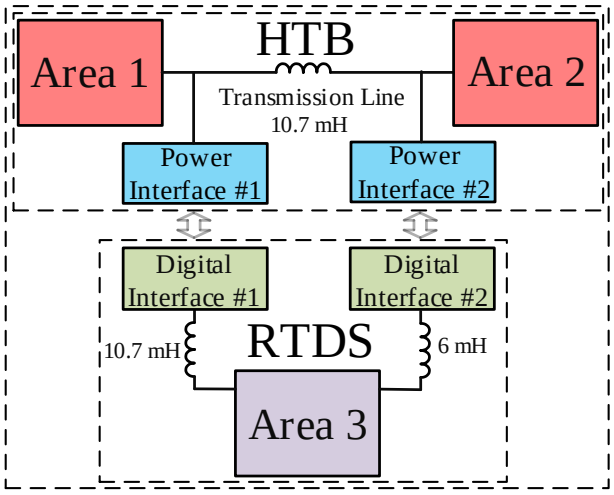


Figure 6-25. Hybrid emulation of the scaled-down three-area system.

The current source ITM algorithm is implemented in both hybrid emulation interfaces since the equivalent impedance in the digital side is larger than the hardware side. The scaled-down three-area system is simulated in the pure MATLAB/Simulink environment and the pure RTDS platform separately to compare with the hybrid emulation.

- Case I: Steady state comparison of three-area system

The comparison of the bus voltages and the system frequency under steady state condition is shown in Table 3. The voltage deviations among the hybrid emulation, the pure MATLAB simulation and the pure RTDS simulation are smaller than 0.006 p.u. The frequency deviation among the hybrid emulation, the pure MATLAB simulation and the pure RTDS simulation are smaller than 0.0004 p.u. The comparison indicates that the hybrid emulation matches with the pure digital simulations well since the per-unit values of the deviations are small, which verifies the validity of hybrid emulation with two interfaces during the steady state condition.

- Case II: Power generation trip in three-area system

A power generation trip is emulated by dropping the active power of wind farm 2 from 0.3 p.u. to 0.0 p.u. The system frequency response of the hybrid emulation matches well with that of the pure MATLAB simulation and the pure RTDS simulation, as shown in Figure 6-26. The system frequency drops because of losing a power generation source.

- Case III: Voltage collapse scenario in three-area system

As a heavy load center, Area 3 has voltage stability issues caused by the long transmission lines from Area 1 and Area 2. The voltage collapse scenario is demonstrated by ramping the LD_{13} active power with a slope of 0.018 p.u. / s.

Table 3. Three-area system steady state comparison among hybrid emulation, pure MATLAB and pure RTDS simulations

Parameters	**Hybrid (p. u.)**	**MATLAB (p. u.)**	**RTDS (p. u.)**
V_1	1.030	1.031	1.031
V_2	1.011	1.011	1.011
V_3	1.031	1.031	1.031
V_4	1.012	1.013	1.013
V_7	1.035	1.036	1.039
V_9	1.035	1.036	1.041
V_{12}	1.137	1.141	1.141
V_{13}	1.085	1.088	1.089
V_{15}	1.035	1.034	1.033
f	1.0044	1.0045	1.0040

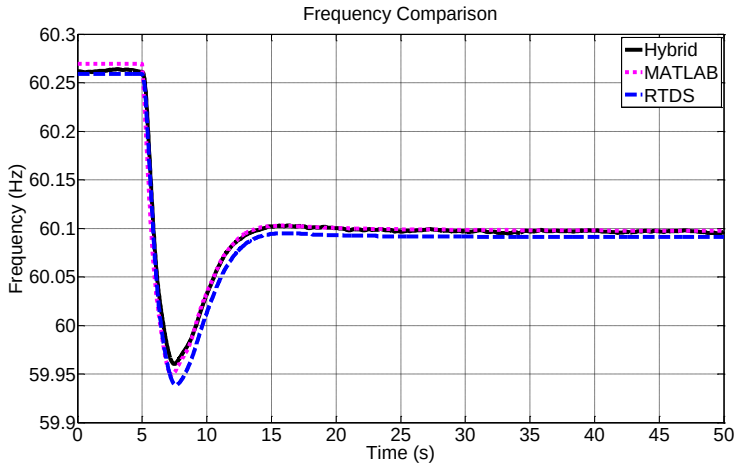


Figure 6-26. Frequency response comparison under a wind farm outage condition.

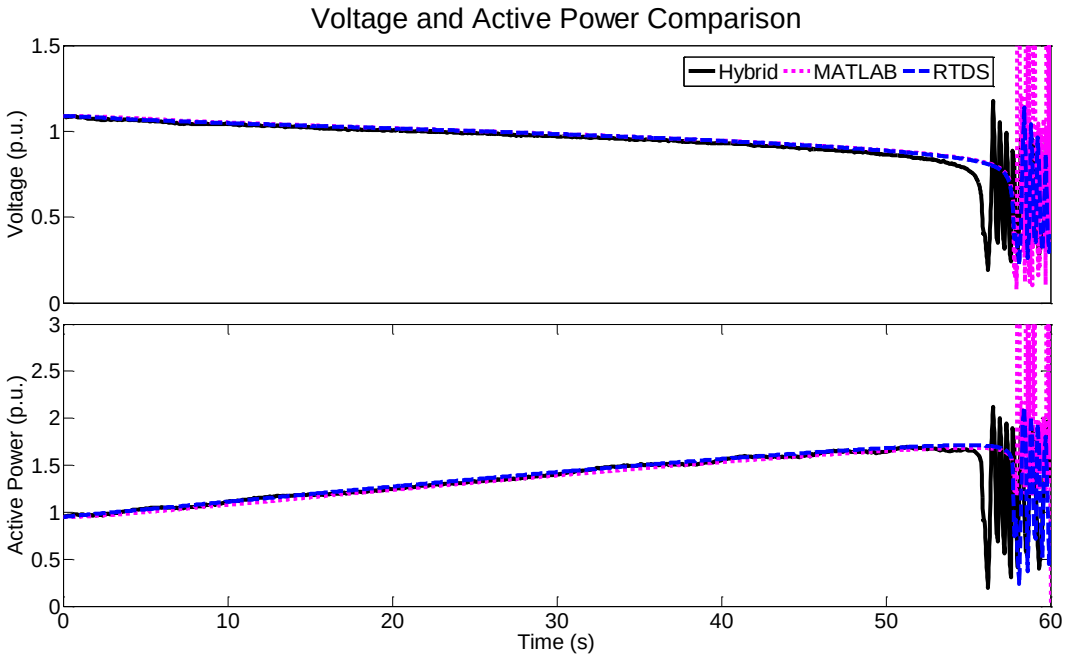


Figure 6-27. Bus 13 voltage and LD_{13} active power comparisons during the LD_{13} active power ramping period.

Figure 6-27 shows the bus 13 voltage and LD_{13} active power during the LD_{13} active power ramping period. The voltage collapse happens at the time around 57 s for the three cases of hybrid emulation, pure MATLAB simulation and pure RTDS simulation, which indicates that the hybrid emulation matches with the pure MATLAB simulation and the pure RTDS simulation well.

6.6 Conclusion

A hybrid emulation platform based on RTDS and HTB is developed to extend the size of an emulated system limited by the number of HTB physical components available. Considering the complementary stability criterion of the voltage source ITM algorithm and current source ITM algorithm, both algorithms are implemented in a hybrid emulation interface to guarantee the interface stability under different system conditions by selecting the appropriate algorithm based on the relationship between the equivalent impedance at the digital side and the equivalent impedance at the hardware side.

A time-delay correction method is also proposed and implemented in the hybrid emulation interface to enhance the emulation accuracy. To further extend the emulation capability and flexibility, two identical interfaces are implemented in the developed hybrid emulation platform. The emulation stability is analyzed for a hybrid emulation system with two interfaces. The validity of the hybrid emulation platform is verified since the hybrid emulation performance is similar to the pure HTB emulation, pure MATLAB simulation and pure RTDS simulation.

7 MMC Test-bed Development and Demonstration

In this chapter, a flexible MMC test-bed with 10 full-bridge submodules (SMs) in each arm and flexible reconfiguration capabilities of MMC topologies, switching frequencies, and passive component parameters, is developed for MMC studies. The SM dc voltage balance control based on a sorting algorithm and a second order circulating current suppressing algorithm based on proportional resonance (PR) controller are implemented. A cost-effective and universal per-charging method is also proposed to pre-charge the MMC to be prepared for normal operations.

7.1 System Structure and Hardware Design

Figure 7-1 shows the main circuit diagram of the developed MMC test-bed. Each arm has 10 full-bridge SMs, which can be easily configured as half-bridge SMs by keeping T_4 "on" and T_3 "off" and operating T_1 and T_2. Thus, the MMC test-bed can conduct the half-bridge, full-bridge, and hybrid MMC tests.

The dc input has a dc breaker and two series connected dc capacitors C_1, C_2. An Y_g/Δ transformer is installed on the ac side. Two ac contactors and three current limiting resistors are installed to pre-charge the MMC through the ac side if the traditional pre-charging method is evaluated. Two dc voltages v_{dcp}, v_{dcn}, two dc currents i_{dcp}, i_{dcn}, six arm currents i_{a_up}, i_{a_low}, i_{b_up}, i_{b_low}, i_{c_up}, i_{c_low}, six ac currents i_a, i_b, i_c, i_{ao}, i_{bo}, i_{co}, six ac voltages v_a, v_b, v_c, v_{ao}, v_{bo}, v_{co}, and all of the SM dc voltages are measured for flexible tests of different control algorithms.

As a scaled MMC testing platform, the maximum dc voltage, ac voltage, and apparent power of the MMC test-bed are designed to be V_{dc} = 400V, V_{ac} = 208V, and S_N = 15 kVA, respectively.

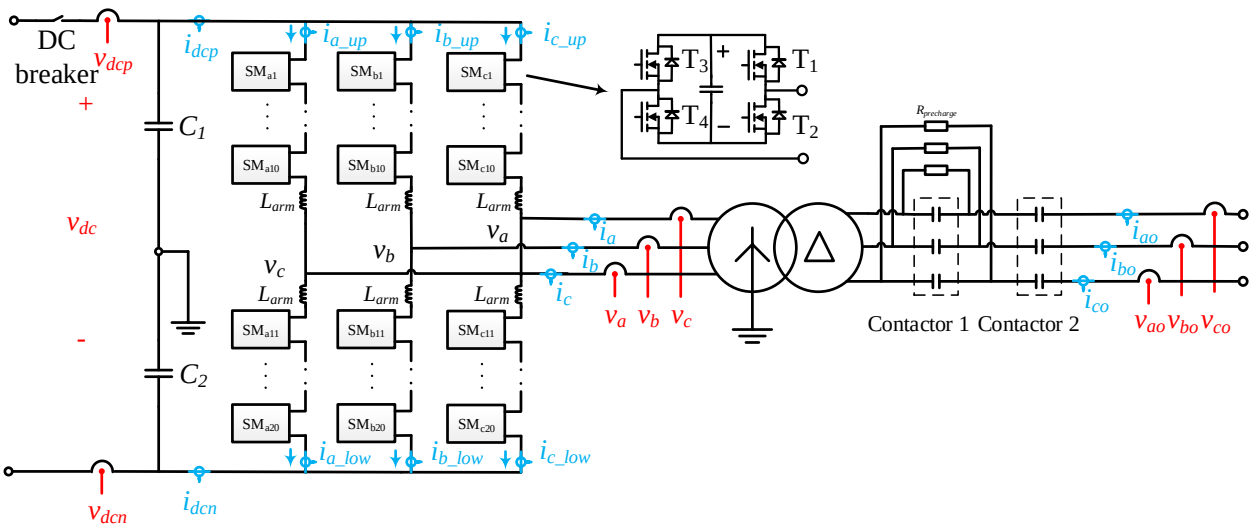


Figure 7-1. MMC test-bed main circuit diagram.

Figure 7-2 shows the control system diagram of the developed MMC test-bed. The Labview running in a Personal Computer (PC) functions as the station level controller and Human Machine Interface (HMI) by exchanging information with the main controller DSP through CAN bus communication based on a CompactRIO, which is a real-time embedded industrial controller made by National Instruments (NI).

The major control functions are implemented in the main controller DSP to generate the modulation index based on the operation mode from the HMI and the voltage and current feedback from the main controller FPGA. The main controller FPGA samples the voltages and currents with dedicated analog to digital (A/D) chips, communicates with six arm controllers through optical fibers, and exchanges information with the main controller DSP through a data bus.

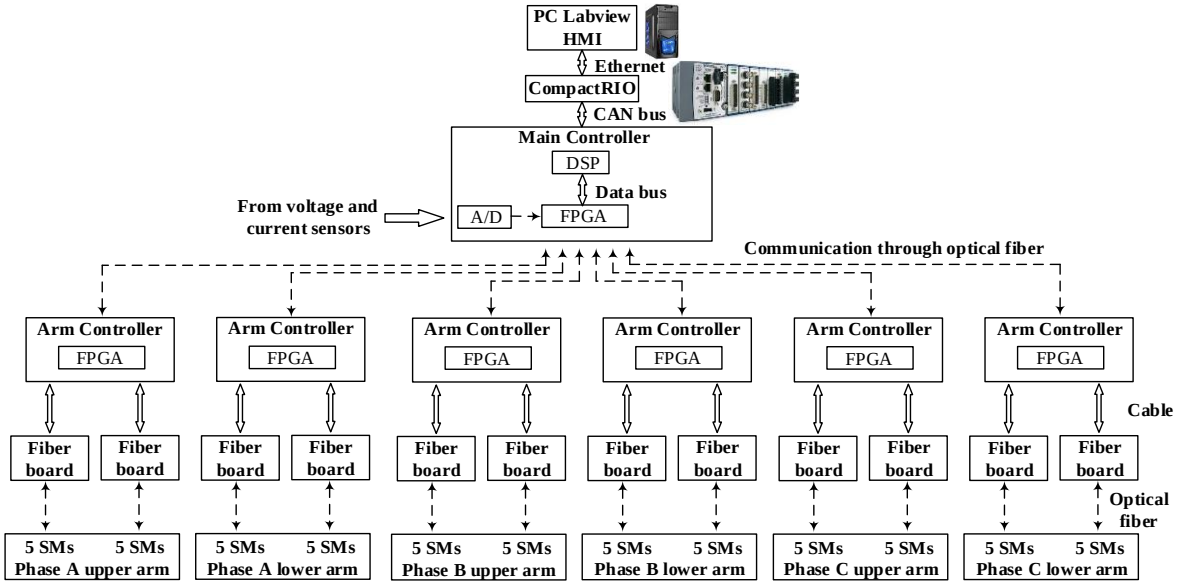


Figure 7-2. MMC test-bed control system diagram.

Each FPGA-based arm controller receives the modulation index and arm current measurement from the main controller FPGA, measures the dc voltage feedback from the 10 SMs through the two fiber boards, and generates the switching signals to control the 10 SMs in each arm through the two fiber boards.

Figure 7-3 shows the designed PCB boards for the MMC test-bed. Figure 7-3(a), (b), (c), and (d) are the main controller, the arm controller, the fiber board, and the SM board, respectively. Each dc capacitor in the SM board is connected to the SM dc bus through a manual switch in series so that the total SM dc capacitance can be easily modified by changing the status of the manual switches, as shown in Figure 7-3(d). The SM board can operate at a switching frequency higher than 10 kHz by using the MOSFET devices (V_{DS} = 200V, I_D = 88A) for the potential high-voltage high-frequency SiC device application studies.

(a) (b)

(c) (d)

Figure 7-3. PCB boards for the MMC test-bed: (a) Main controller; (b) Arm controller; (c) Fiber board; (d) SM board.

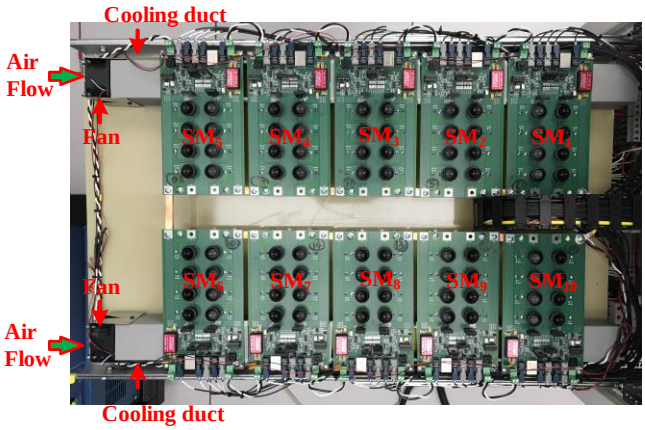


Figure 7-4. SM installation of each arm for MMC test-bed hardware.

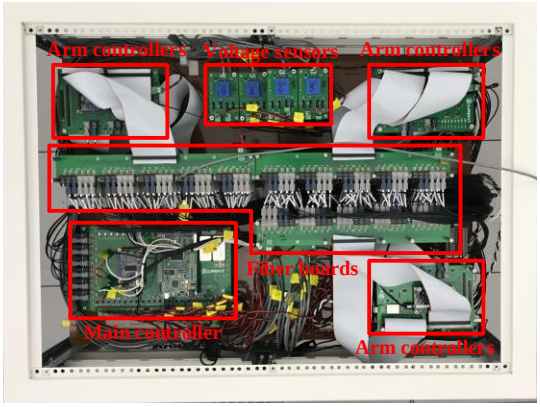


Figure 7-5. Control board installation from the cabinet top view for MMC test-bed hardware.

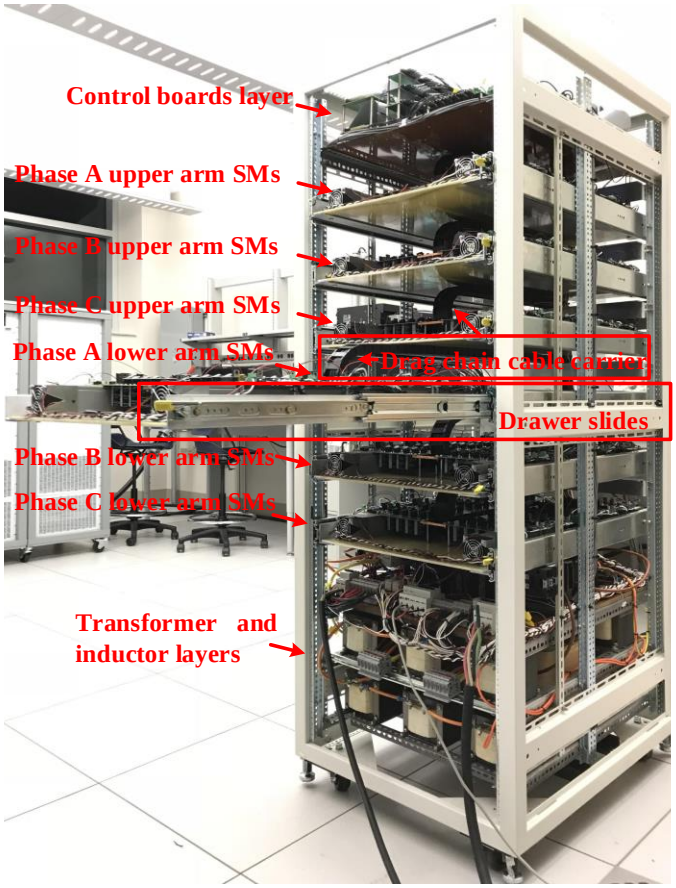


Figure 7-6. Cabinet installation for MMC test-bed hardware.

Figure 7-4, Figure 7-5, and Figure 7-6 show the MMC test-bed hardware installations. Figure 7-4 is the SM installation of each arm where five SMs share a cooling duct with a fan blowing the air. Figure 7-5 is the control board installation from the cabinet top view. Figure 7-6 is the cabinet installation, which has a control board layer, six arm SM layers, and two transformer and inductor layers.

The arm SM layer is mounted to the cabinet frame with a pair of drawer slides. By installing the optical fibers and cables connected to the arm SM layer in a drag chain cable carrier, the SM arm layer can be extended out on the drawer slides to test the MMC and modify the SM capacitance easily, as shown in Figure 7-6.

7.2 Control Algorithm Implementation

For a MMC, there are mainly three control function blocks, including the overall converter function control, the circulating current suppressing control, and the SM dc voltage balance control, as shown in Figure 7-7.

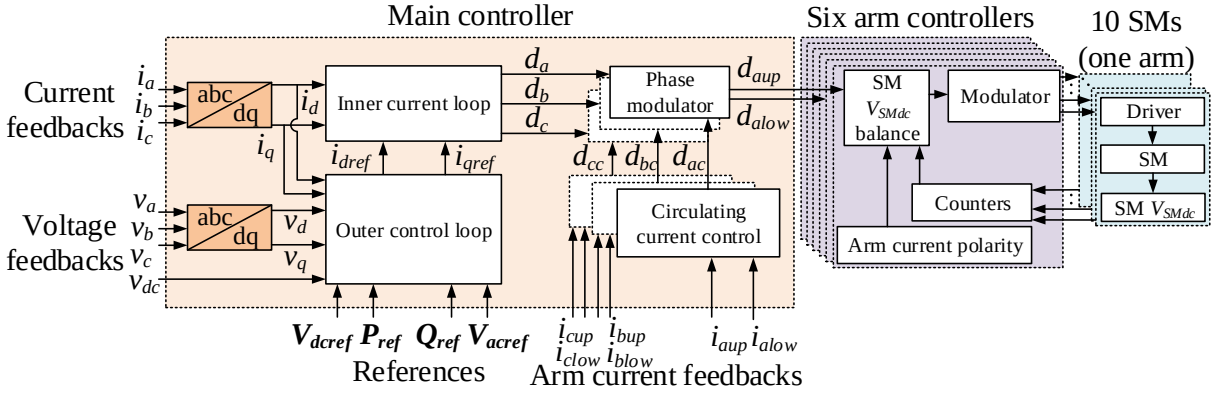


Figure 7-7. MMC test-bed control system diagram.

7.2.1 Converter Function Control

The converter function is realized by a double-loop control structure, as shown in Figure 7-8. The outer *d* axis control loop controls either the dc voltage or active power by generating the *d* axis current reference I_{dref}. The outer *q* axis control loop controls either the ac bus voltage or the reactive power by generating the *q* axis current reference I_{qref}. The inner *dq* control loops control the I_d and I_q, respectively, with PI controllers and *dq* decoupling terms.

7.2.2 Circulating Current Suppression Control

A proportional resonant (PR) controller is implemented to suppress the second order circulating current, as shown in Figure 7-9. The circulating current reference is zero and the feedback is $i_{acir} = (i_{aup}+i_{alow})/2$. The circulating current suppression control duty ratio d_{acir} is derived with a PR controller according to the circulating current error Δi_{acir}. The circulating current suppression control duty ratio d_{acir} is subtracted by the duty ratio from the inner current loop to acquire the upper arm duty ratio d_{aup} and low arm duty ratio d_{alow}.

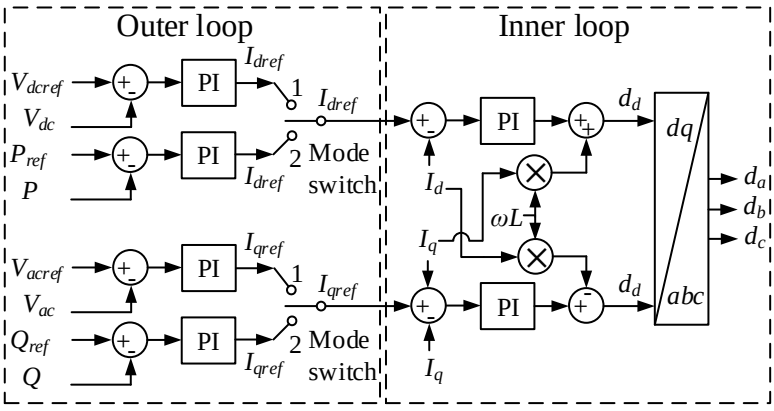


Figure 7-8. Converter function double-loop control algorithm.

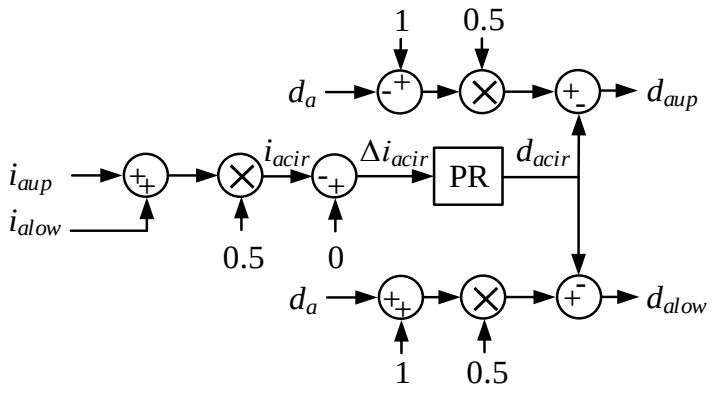


Figure 7-9. MMC second order circulating current suppression control.

7.2.3 SM Dc Voltage Balance Control

A sorting method is implemented to balance the SM dc voltages. Figure 7-10 shows the phase A upper arm SM dc voltage balance control diagram. The fully inserted SM number k ($1 \leq k \leq N$-1, N is the total SM number) and the modulation index D ($0 \leq D \leq 1$) of one more SM are calculated by using the phase A upper arm duty ratio d_{aup}. The voltage ranking index(1) to index(N)) store the SM sequence numbers according to the SM dc voltage from high to low. The SM selection block decides the fully inserted k SMs and another SM operating under duty ration D according to the arm current direction and voltage ranking indexes. In this dissertation, the arm current positive direction is defined as in Figure 7-1. If $I_{aup} \geq 0$, the SMs with sequence numbers stored in the voltage ranking index(1) to index(k) are fully inserted (duty ratio $D_i = 1$) and the SM with sequence number stored in the voltage ranking index(k+1) operates with duty ratio D. On the contrary, if $I_{aup} < 0$, the SMs with sequence numbers stored in the voltage ranking index(N-k+1) to index(N) are fully inserted (duty ratio $D_i = 1$) and the SM with sequence number stored in the voltage ranking index(N-k) operates with duty ratio D.

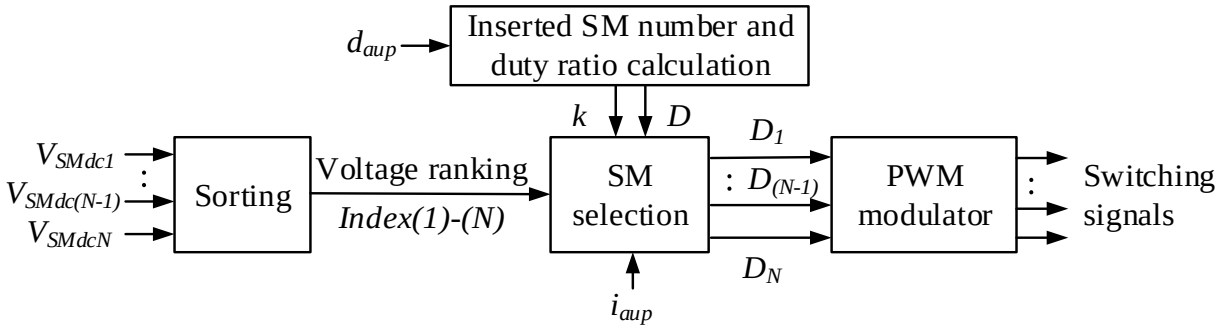


Figure 7-10. MMC SM dc voltage balance control.

7.3 MMC Pre-charge

A cost-effective and universal pre-charge method is proposed to pre-charge the MMC SM dc voltages to the rated value to be ready for normal operation, as shown in Figure 7-11. A low voltage pre-charge dc supply is connected to the three-phase bottom SM dc links through a low voltage pre-charge diode.

In this dissertation, the SMs in each phase from the positive dc bus to the negative dc bus in Figure 7-11 are named as SM_{xn} (x is a, b, or c representing the phase; n is 1, 2, $\cdots$ or 20 representing the SM number).

During the pre-charge process, the MMC operates in a half-bridge mode. The upper power electronic switch and lower power electronic switch in each SM are named as S_{up_xn} and S_{low_xn}, respectively.

To pre-charge the SMs in one phase except for the SM_{x20} (x is a, b, or c representing the phase), the targeted pre-charge phase, the pre-charge dc supply, and the pre-charge diode cooperate with another phase to operate in a boost converter mode.

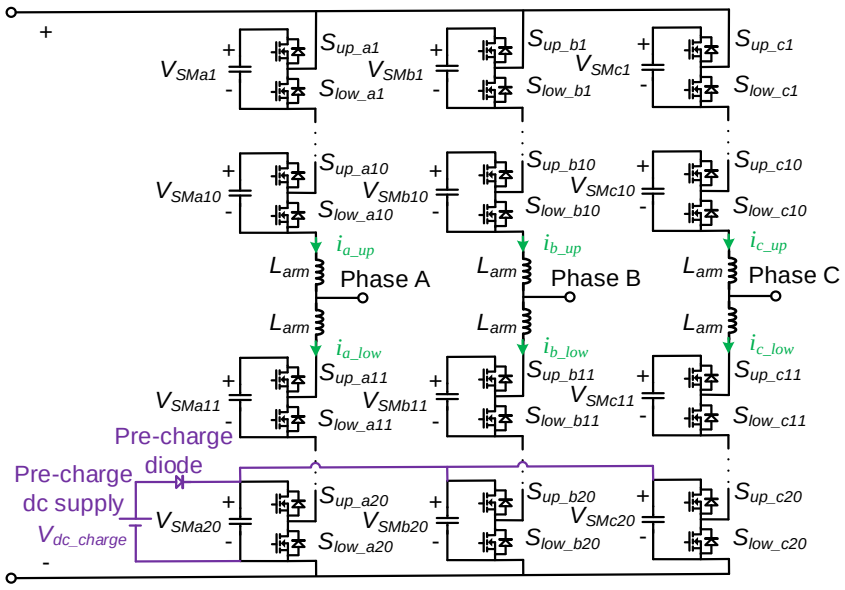


Figure 7-11. Proposed MMC pre-charge method with a low voltage dc supply.

Figure 7-12 and Figure 7-13 show the two operating statuses in sequence to pre-charge the SM_{am} (m is *1*, *2*, ⋯ or *19*) with the pre-charge dc supply. First, the pre-charge dc supply energy is delivered to phase A and phase B arm inductors by increasing the current i_{charge} through turning on the phase B bottom SM upper switch S_{up_b20} and the lower switches of all the other SMs in phase A and phase B, as shown in Figure 7-12. Second, after the i_{charge} reaches a pre-set upper bound value, the energy stored in phase A and phase B arm inductors is delivered to phase A SM capacitor except for the SM_{a20} by turning on all phase A upper switches except for the bottom SM and turning on all phase B lower switches, as shown in Figure 7-13. After the i_{charge} decreases to a pre-set lower bound value, repeat the above two steps until all SM_{am} (m is *1*, *2*, ⋯ or *19*) are pre-charged to a pre-set value. By using the same method, phase B and phase C SMs except for the SM_{b20} and SM_{c20} can also be pre-charged to the pre-set value.

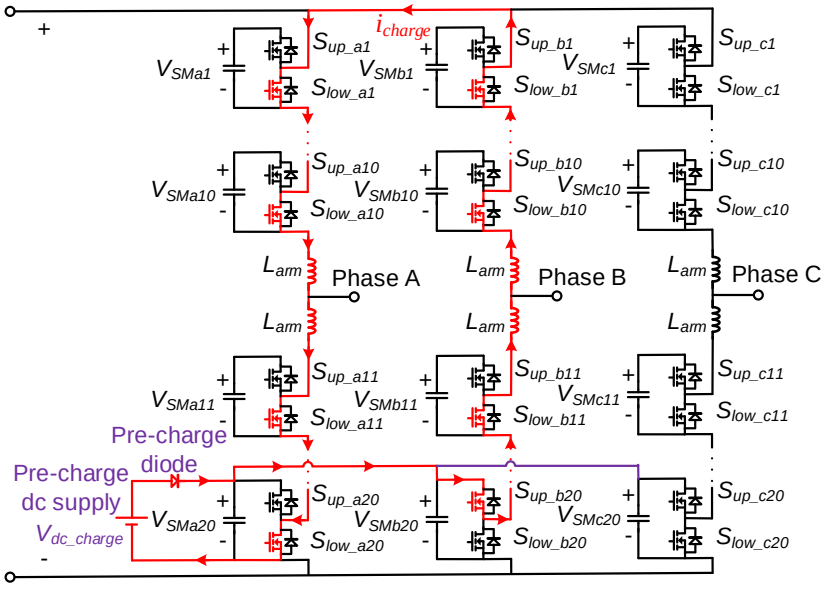


Figure 7-12. Deliver energy from pre-charge dc supply to phase A and B arm inductors by increasing current.

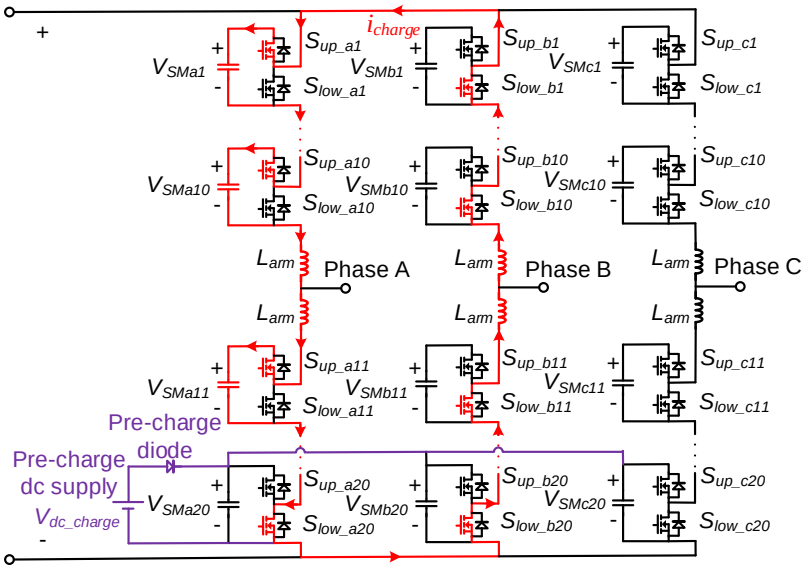


Figure 7-13. Deliver energy from phase A and phase B arm inductors to phase A SM capacitor.

Because the SM_{a20}, SM_{b20} and SM_{c20} dc links are directly connect to the pre-charge dc supply through the pre-charge diode, they are not able to be pre-charged by the pre-charge dc supply. Instead, a part of the energy pre-charged and stored in the SM_{xm} (x is a, b, or c representing the phase; m is 1, 2, ⋯ or 19 representing the SM number) is utilized to pre-charge the SM_{a20}, SM_{b20} and SM_{c20}.

In the previous pre-charging process, the SM_{xm} is pre-charged to a pre-set value slightly higher than the rated voltage to reserve energy for pre-charging the SM_{a20}, SM_{b20} and SM_{c20}. Any two phases cooperate to operate in a buck converter mode to pre-charge the SM_{a20}, SM_{b20}, and SM_{c20} with the SM_{xm}. Figure 7-14 and Figure 7-15 show the two operating statuses in sequence to pre-charge the SM_{b20} with the energy stored in SM_{am} (m is 1, 2, ⋯ or 19).

First, the energy in SM_{am} (m is 1, 2, ⋯ or 19) is delivered to phase A and phase B arm inductors by increasing the current i_{charge} through turning on the S_{up_am} (m is 1, 2, ⋯ or 19), S_{low_a20}, and S_{low_bn} (n is 1, 2, ⋯ or 20), as shown in Figure 7-14. Second, after the i_{charge} reaches a pre-set upper bound value, the energy stored in phase A and phase B arm inductors is delivered to SM_{b20} by turning on S_{up_bm} and all lower switches of the other SMs in phase A and phase B, as shown in Figure 7-15. After the i_{charge} decreases to a pre-set lower bound value, repeat the above two steps until either all SM_{am} (m is 1, 2, ⋯ or 19) or SM_{b20} reaches the rated value. By using the same method, the SM_{c20} can be pre-charged by the SM_{bm} (m is 1, 2, ⋯ or 19) and the SM_{a20} can be pre-charged by the SM_{cm} (m is 1, 2, ⋯ or 19) successively.

The detailed pre-charge program diagram is shown in Figure 7-16. There are two pre-charge sections in sequence, which are pre-charge SM_{xm} and pre-charge SM_{x20} (x is a, b, or c representing the phase and m is 1, 2, ⋯ or 19), respectively.

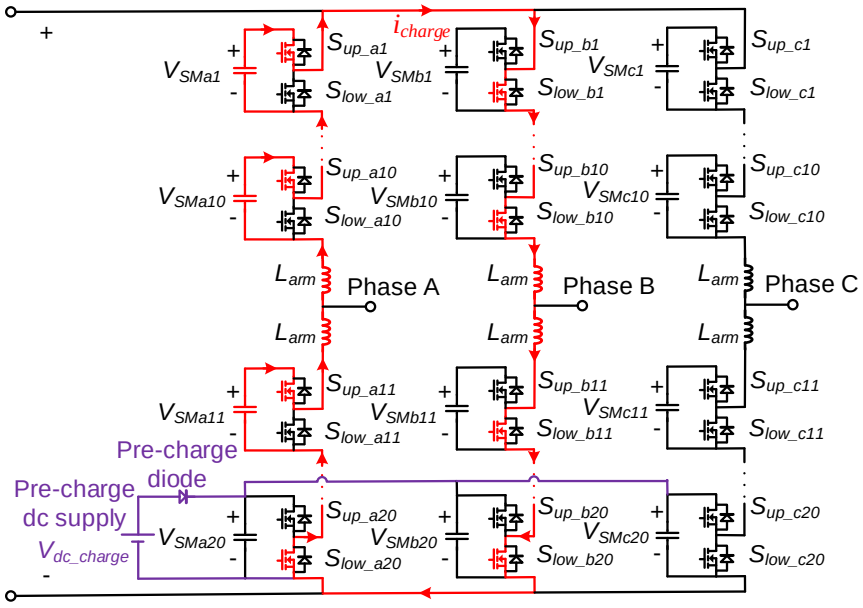


Figure 7-14. Deliver energy from phase A SM_{am} (m is *1*, *2*, ⋯ or *19*) to phase A and phase B arm inductors by increasing current.

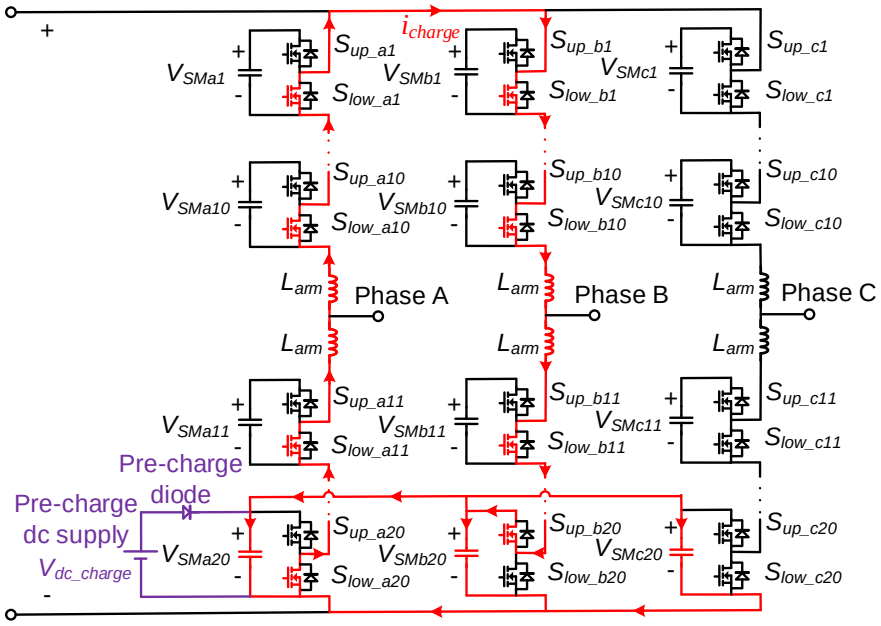


Figure 7-15. Deliver energy from phase A and phase B arm inductors to the SM_{b20}.

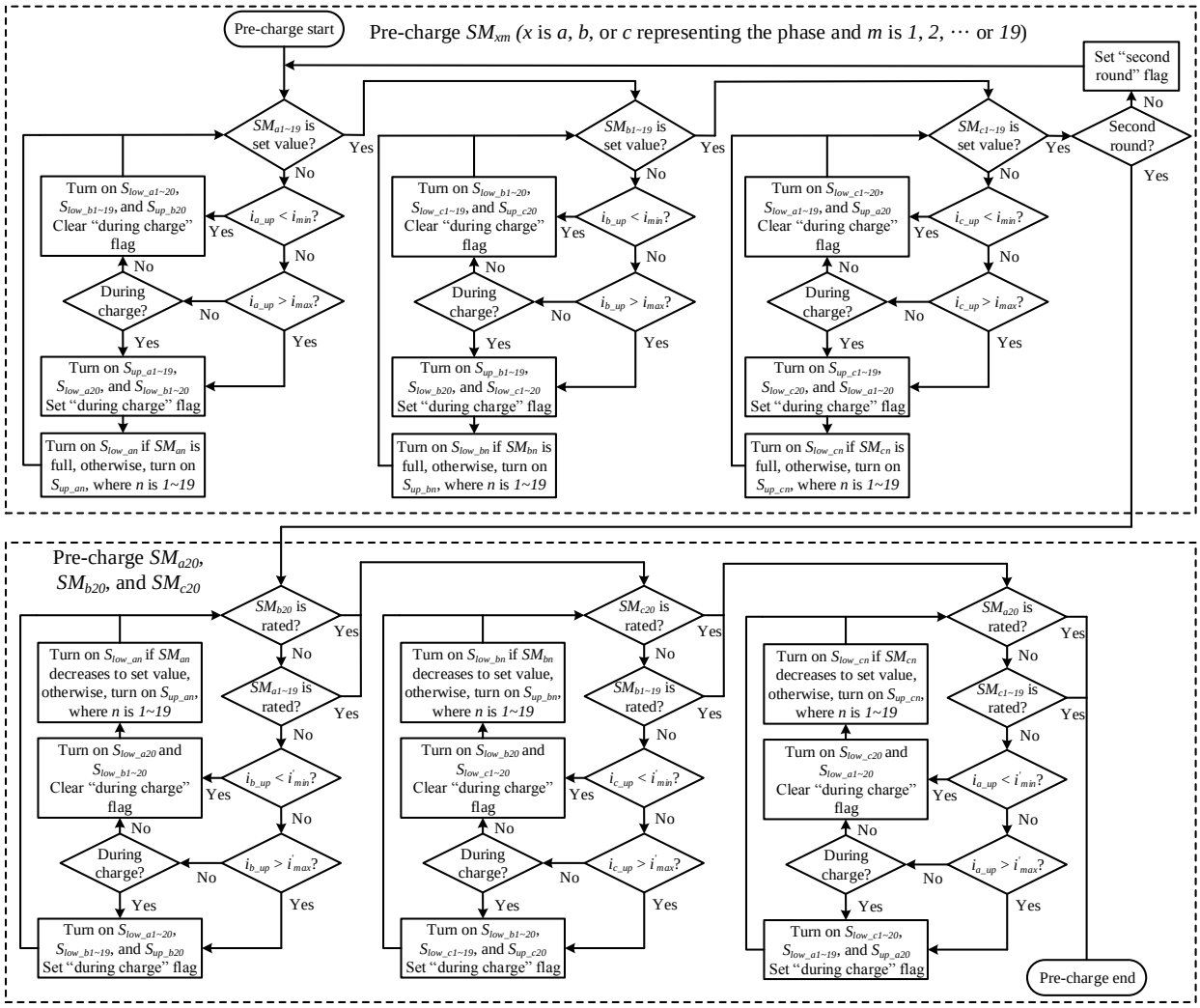


Figure 7-16. MMC pre-charge operation sequence.

- Pre-charge SM_{xm}

In the pre-charge SM_{xm} section, the phase A, B, and C are pre-charged in sequence. The pre-charge for each phase is finished when all of the SM_{xm} in this phase reaches the pre-set value. To compensate the natural discharge on the phase A and B SMs after finishing pre-charging phase C in the first round, a quick second round pre-charge is designed to bring the three phase SMs back to the pre-set value.

For each phase pre-charge part, in this dissertation, the phase A and B, B and C, and C and A cooperate to pre-charge the phase A, B, and C, respectively. The two phases cooperate to start to increase the inductor current and clear the "during charge" flag when the inductor current is smaller than the pre-set lower bound i_{min}.

The two phases cooperated to start to decrease the inductor current by charging the SMs and set the "during charge" flag when the inductor current is larger than the pre-set higher bound i_{max}. If the inductor current is between the lower bound i_{min} and the higher bound i_{max}, the two phases keep the switching status according to the "during charge" flag, which means that the two phases keep charging the SMs if it is during the charge status, otherwise, increasing the inductor current if it is not during the charge status.

- Pre-charge SM_{x20}

In the pre-charge SM_{x20} section, the SM_{b20}, SM_{c20}, and SM_{a20} are pre-charged by the phase A and B with a part of energy in the $SM_{a1\sim19}$, the phase B and C with a part of energy in $SM_{b1\sim19}$, and the phase C and A with a part of energy in $SM_{c1\sim19}$, respectively.

The pre-charge for the SM_{b20} ends when either all of the $SM_{a1\sim19}$ or the SM_{b20} reaches the rated value. Similarly, the pre-charge for the SM_{c20} ends when either all of the $SM_{b1\sim19}$ or the

SM_{c20} reaches the rated value, and the pre-charge for the SM_{a20} ends when either all of the $SM_{c1\sim19}$ or the SM_{a20} reaches the rated value.

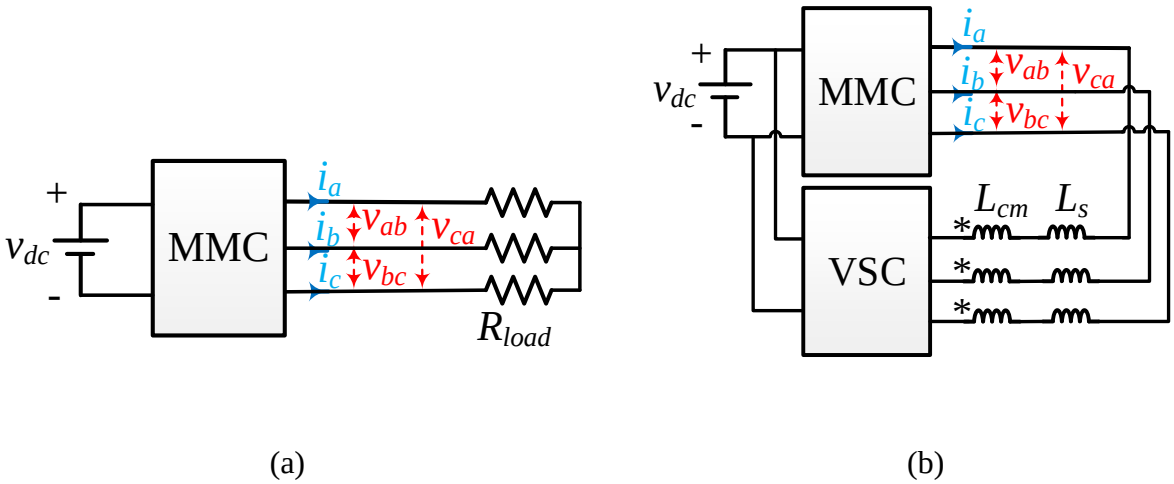
Similarly, for each phase pre-charge part, the two phases cooperate to start to increase the inductor current and clear the "during charge" flag when the inductor current is smaller than the pre-set lower bound i'_{min}. The two phases cooperated to start to decrease the inductor current by charging the SMs and set the "during charge" flag when the inductor current is larger than the pre-set upper bound i'_{max}.

If the inductor current is between the lower bound i'_{min} and the upper bound i'_{max}, the two phases keep the switching status according to the "during charge" flag, which means that the two phases keep charging the SMs if it is during the charge status, otherwise, increasing the inductor current if it is not during the charge status.

7.4 Experiment Results

The scenario of a half-bridge MMC working as an inverter is conducted to verify the functions of the developed MMC test-bed. Two operation modes, which are resistive load mode and grid-tied mode, are conducted with the MMC test-bed, as shown in Figure 7-17(a) and Figure 7-17(b), respectively.

In Figure 7-17(a), the ac resistor R_{load} serves as the load. In Figure 7-17(b), the two-level voltage source converter (VSC) is controlled as a constant voltage source to emulate the grid. The ac inductor L_s serves as the ac filter of the two-level VSC. A three-phase common mode choke is implemented to block the common mode circulating current between the two-level VSC and the MMC since they share the dc bus. The MMC dc bus voltage, arm inductance, and switching frequency are V_{dc} = 400 V, L_{arm} = 3 mH, and f_{sw} = 10 kHz, respectively.



(a) (b)

Figure 7-17. MMC test-bed experiment setup: (a) Resistive load mode; (b) Grid-tied mode.

7.4.1 MMC Test-bed with Resistive Load Scenario

Figure 7-18 shows the experimental results with resistive load $R_{load} \approx 2.3\ \Omega$. Figure 7-18(a) and (b) are the load terminal line-to-line voltages and phase currents with the RMS values $V_{LL} \approx 60$ V and $I \approx 15$ A, respectively, and $V_{LL} \approx \sqrt{3} I R_{load}$.

Figure 7-18(c) shows the phase A upper and lower arm currents whose sum equals to the output current. Figure 7-18(d) shows the dc bus voltage $V_{dc} = 400$ V and one SM dc link voltage v_{SM} from each phase with the average value $V_{SM} \approx 40\ \text{V} = V_{dc} / 10$.

Figure 7-18(e) and (f) are the phase C upper arm v_{SM1}, v_{SM2} and lower arm v_{SM1}, v_{SM2} with the SM capacitance equal to 17.6 mF and 4.4 mF, respectively. The average SM dc voltage equals to 40 V for both SM capacitance cases, and the SM dc voltage ripple is larger for the smaller capacitance case.

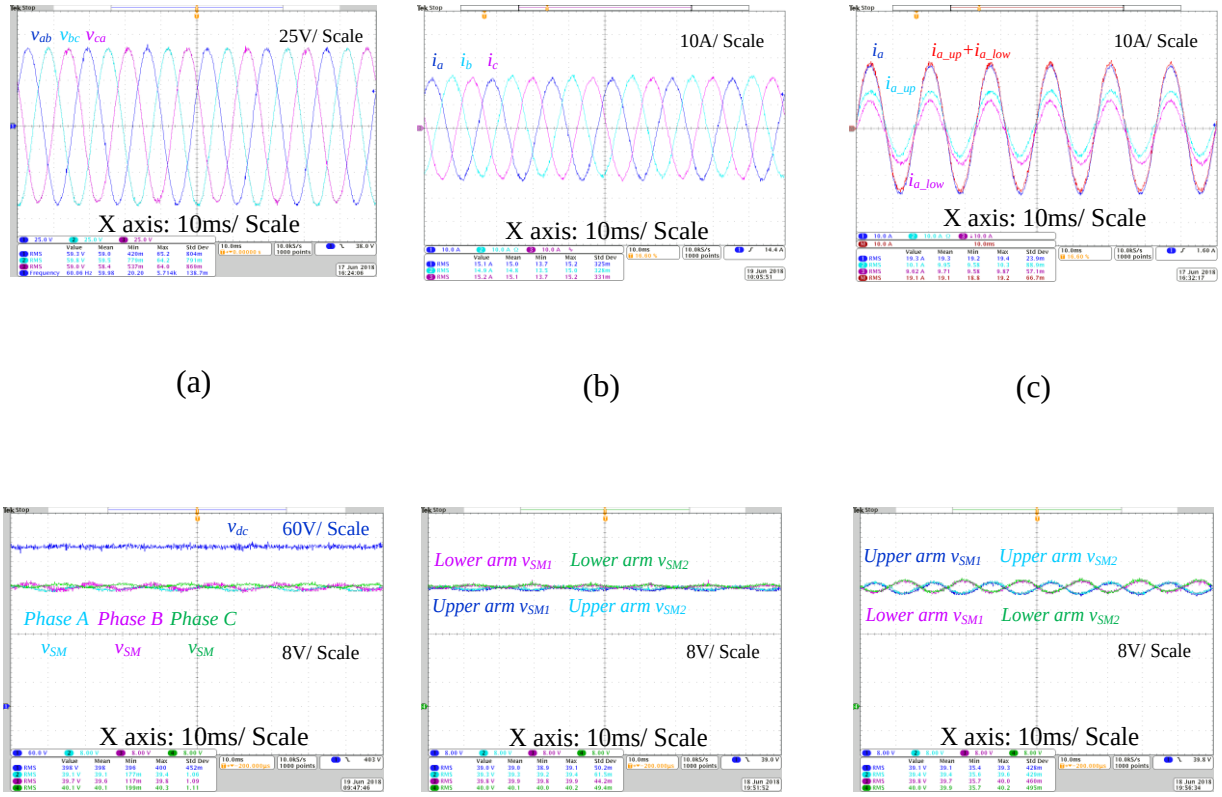


Figure 7-18. MMC test-bed experiment results with resistive load: (a) Load terminal voltages v_{ab}, v_{bc}, v_{ca}; (b) Load terminal currents i_a, i_b, i_c; (c) Phase A arm currents i_{a_up}, i_{a_low}, output current i_a, and the sum of the arm currents $i_{a\_up}+i_{a\_low}$; (d) Dc bus voltage v_{dc}, phase A SM voltage, phase B SM voltage, and phase C SM voltage; (e) Phase C upper arm v_{SM1}, v_{SM2}, and phase C lower arm v_{SM1}, v_{SM2} with SM capacitance C_{SM} = 17.6 mF; (f) Phase C upper arm v_{SM1}, v_{SM2}, and phase C low arm v_{SM1}, v_{SM2} with SM capacitance C_{SM} = 4.4 mF.

Figure 7-19 shows the ac side voltage and current waveforms during the transient of increasing the active power command with a step change from 800 W to 2000 W.

7.4.2 MMC Test-bed Grid-tied Mode

Figure 7-20 shows the experimental results with grid-tied mode. Figure 7-20(a) and Figure 7-20(b) are the MMC terminal line-to-line voltages and current, respectively, under a steady state condition. Figure 7-20(c) shows the terminal voltages and currents under the transient of increasing the active power demand with a step change from 2 kW to 4 kW.

7.4.3 MMC Pre-charge

A pre-charge dc supply with V_{dc_charge} = 36 V is implemented to pre-charge the MMC to the rated dc voltage 400 V, which corresponds to 40 V in each SM. The current upper and lower bounds for pre-charging $SM_{x1\sim19}$ (x is a, b, or c representing the phase) are set to be i_{max} = 13 A and i_{min} = 5 A, respectively. The current upper and lower bounds for pre-charging SM_{x20} (x is a, b, or c representing the phase) are set to be i'_{max} = 6 A and i'_{min} = 3 A, respectively.

Figure 7-21 shows the phase A, B, and C SMs voltages during the pre-charge in the HMI. First, the phase A, B, and C SMs except for the ones connected to pre-charge dc supply are pre-charged to the pre-set value in sequence. During the phase B and C pre-charging, the phase A SM voltages decrease slightly due to the natural discharge. Because the same reason, the phase B SM voltages decrease slightly during the phase C pre-charge. Second, a quick second round pre-charge is applied to bring the phase A and B SM voltages to the pre-set value. Last, the SMs connected to the pre-charge dc supply is pre-charged to the rated value.

Figure 7-22 shows the SM_{a1} (Channel 1), SM_{b1} (Channel 2), SM_{c1} (Channel 2), and SM_{a20} (Channel 4) voltages in the scope during the pre-charging, which are the same as in the HMI.

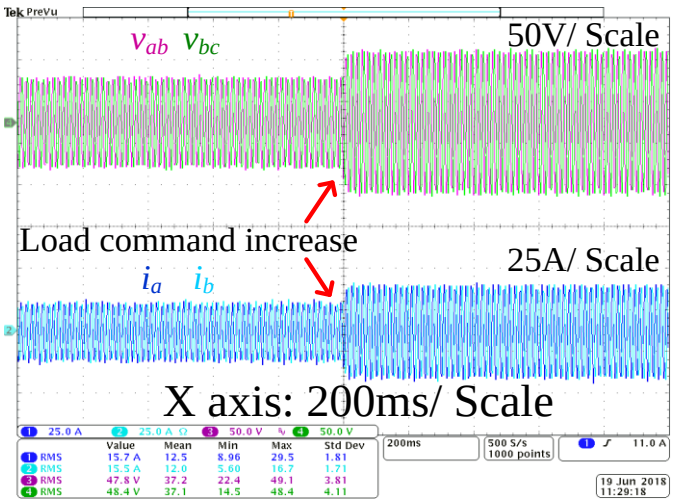
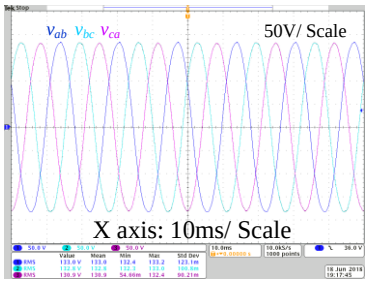
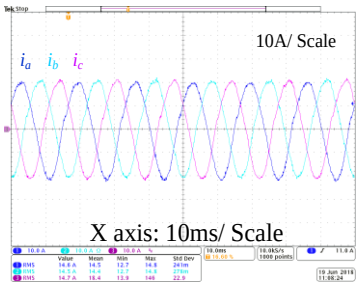


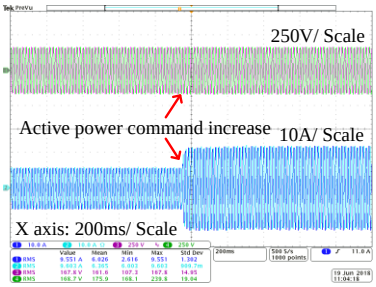
Figure 7-19. MMC test-bed experiment results with resistive load step increase from 800 W to 2000 W.



(a)



(b)



(c)

Figure 7-20. MMC test-bed experiment results with grid-tied mode: (a) MMC terminal voltages v_{ab}, v_{bc}, v_{ca}; (b) MMC terminal currents i_a, i_b, i_c; (c) MMC terminal voltages and currents during the transient of increasing active power command from 2 kW to 4 kW.

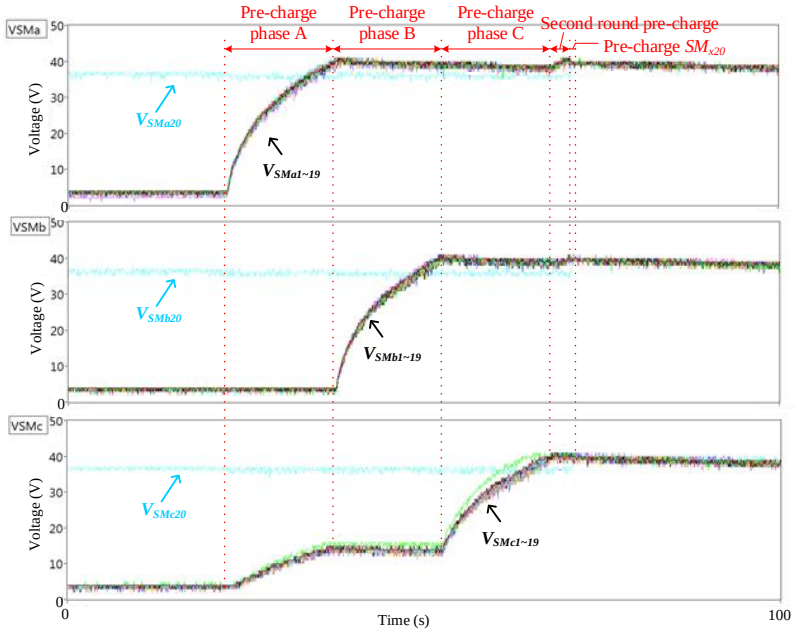


Figure 7-21. MMC all SMs voltages during pre-charge: (a) Phase A; (b) Phase B; (c) Phase C.

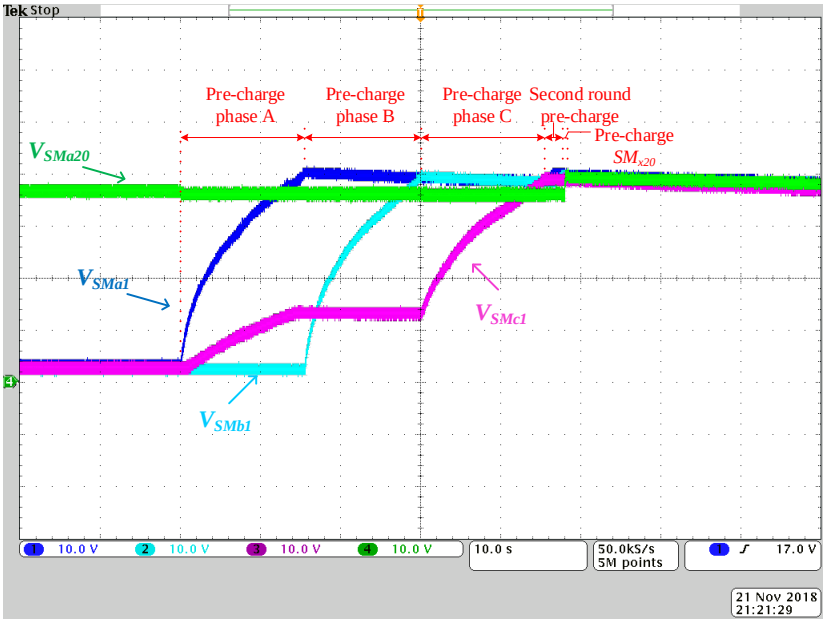


Figure 7-22. MMC SM_{a1}, SM_{b1}, SM_{c1}, SM_{a20} voltages during pre-charging.

Figure 7-23 shows the i_{a_up} (Channel 1), i_{b_up} (Channel 2), i_{c_up} (Channel 3), and V_{SMa2} (Channel 4) during pre-charging. The phase A and B cooperate to pre-charge the phase A SMs with mainly positive i_{a_up} and negative i_{b_up}. Similarly, the phase B and C SMs are pre-charged with i_{b_up}, i_{c_up} and i_{c_up}, i_{a_up}, respectively. The current peak is limited to around the upper bound i_{max} = 13 A. As the phase A SM voltages increase, the phase A current i_{a_up} decreases to be smaller than the lower bound i_{min} = 5 A or even negative values during the charging process.

Figure 7-24 shows the zoom in waveforms when the phase A SM voltages are close to the pre-set value, in which the minimum i_{a_up} reaches -4 A. This is because the control action is at least one step time delayed refer to the actual current. The higher the phase A SM voltages, the larger the current decrease would be within a fixed time-delay, then the more the current can potentially exceed the hysteresis bound. The current decrease slope is sharper than the rise slope since the applied voltage to decrease the current is the sum of the $SM_{a1\sim19}$ voltages, which is larger than the SM_{b20} voltage that is applied to increase the current.

Figure 7-25 shows the zoom in waveforms during the second round pre-charge process, which repeats the first pre-charge process with a shorter duration since all SM voltages are already close to the pre-set value.

Figure 7-26 shows the zoom in waveforms during the pre-charge SM_{x20} process. The SM_{b20} is pre-charged with the energy stored in $SM_{a1\sim19}$ with mainly negative i_{a_up} and positive i_{b_up}. Similarly, the SM_{c20} and SM_{a20} are pre-charged with i_{b_up}, i_{c_up} and i_{c_up}, i_{a_up}, respectively. The current peak values exceed the upper bound i'_{max} = 6 A and lower bound i'_{min} = 3 A for the same reason of control delay. Differently, the current rise slope is sharper than the decrease slope since the applied voltage to increase the current is the sum of the $SM_{a1\sim19}$, $SM_{b1\sim19}$, or $SM_{c1\sim19}$ voltages, which is larger than the SM_{b20}, SM_{a20}, or SM_{c20} voltage that is applied to decrease the current.

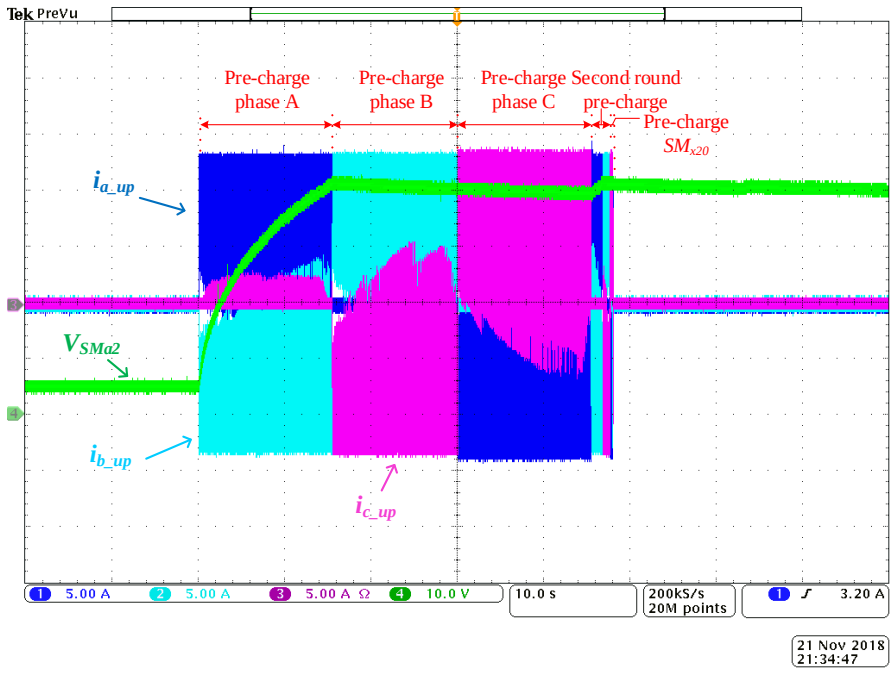


Figure 7-23. MMC i_{a_up}, i_{b_up}, i_{c_up}, and V_{SMa2} during pre-charging.

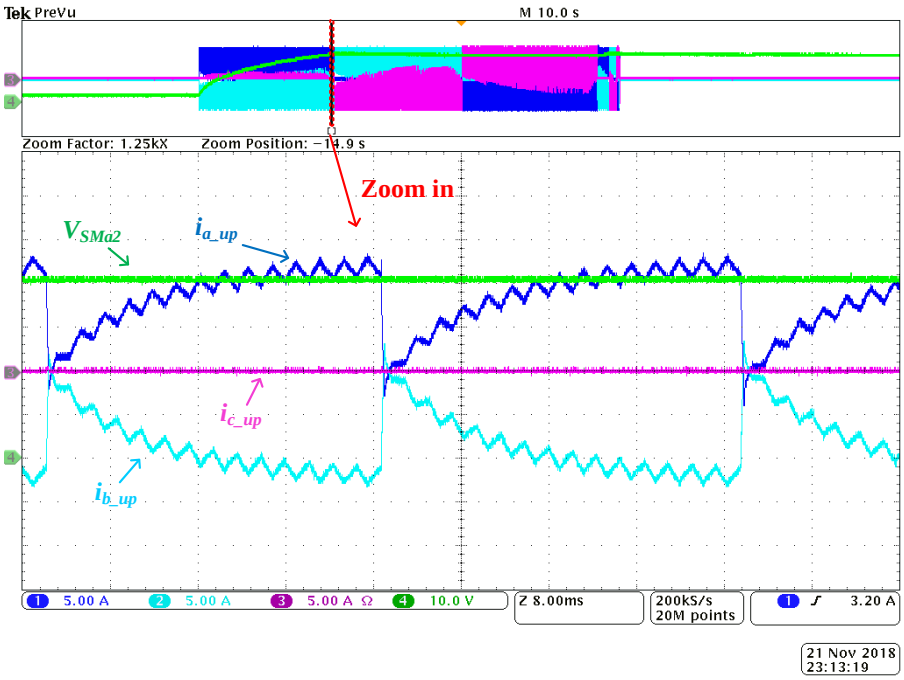


Figure 7-24. MMC i_{a_up}, i_{b_up}, i_{c_up}, and V_{SMa2} when the phase A SM voltages are high.

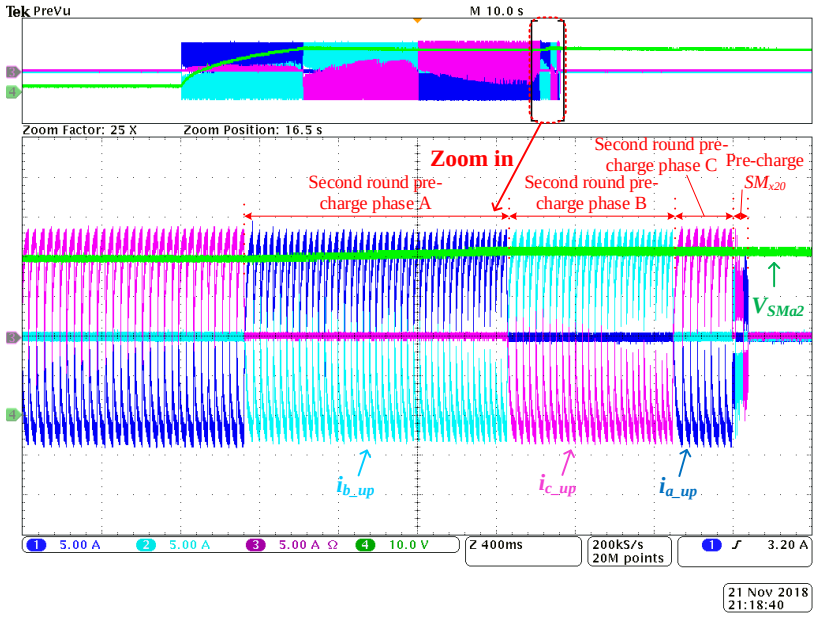


Figure 7-25. Zoom in MMC i_{a_up}, i_{b_up}, i_{c_up}, and V_{SMa2} for the second round pre-charge process.

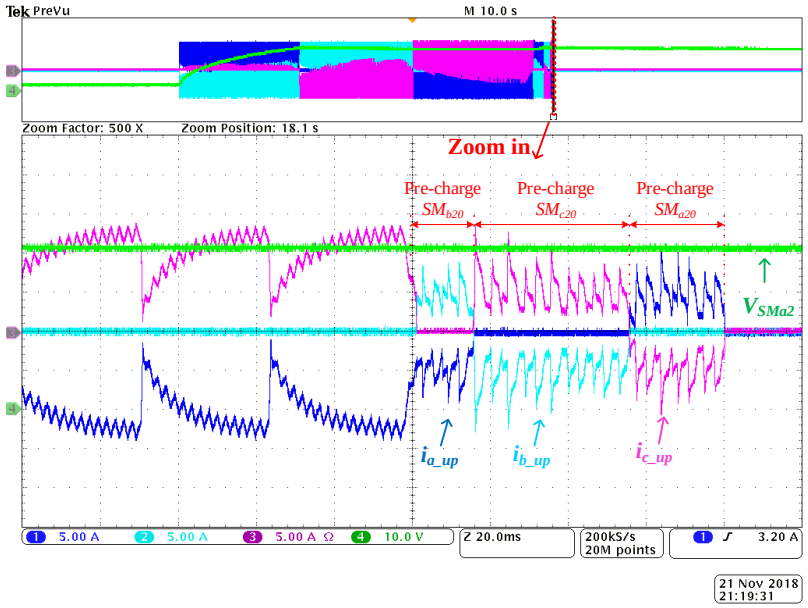


Figure 7-26. Zoom in MMC i_{a_up}, i_{b_up}, i_{c_up}, and V_{SMa2} for the pre-charge SM_{x20} process.

7.5 Conclusions

A flexible MMC test-bed with 10 SMs in each arm has been developed to conduct MMC studies with different topologies, switching frequencies, and passive component parameters. The SM dc capacitance can be modified easily by changing the status of the manual switch in series with each SM capacitor. Each layer of the arm SMs can be extended out from the cabinet to test the MMC and operate the manual switches easily. The function has been verified by running the developed MMC test-bed as an inverter under the half-bridge MMC configuration with different SM dc capacitances.

A cost-effective and universal pre-charge method by utilizing the MMC circuit and a low voltage dc supply is proposed to pre-charge the MMC. The proposed method has been implemented in the MMC test-bed. The function has been demonstrated by pre-charging all SMs in the MMC test-bed to the rated value.

8 Hybrid Ac/dc Transmission

In this chapter, the system structure and principle of hybrid ac/dc transmission is introduced. The fundamental frequency current on the dc side i_{60} induced by the non-transposed double circuit transmission line is investigated. The i_{60} influence on the HVDC station transformer saturation is evaluated and two methods are proposed to solve the issues caused by the i_{60}.

8.1 System Structure and Basic Principle

The hybrid ac/dc transmission system is shown in Figure 8-1. The 12-pulse line-commutated converter (LCC)-based bipolar HVDC is used to inject the dc current into the double ac circuits through zig-zag transformers. Each HVDC station contains an ac station transformer with three windings and two thyristor based rectifiers in series.

The zig-zag transformer has two windings from different magnetic pillars connected in reversed polarities, as shown in Figure 8-2. With magnetic flux cancellation characteristic for each magnetic pillar, balanced three-phase dc current injection will not cause a zig-zag transformer saturation problem, and the zero sequence impedance of the zig-zag transformer will be small. The positive sequence impedance of the zig-zag transformer is three times of the winding impedance, which is large [78]. Thus, the injected dc current can flow through the zig-zag transformer with a low impedance. At the same time, the zig-zag transformer blocks the positive sequence current.

The non-transposed transmission lines are used since it is commonly implemented in the high voltage ac systems. The tower structure and line sag of a typical 345 kV double circuit transmission line are shown in Figure 8-3.

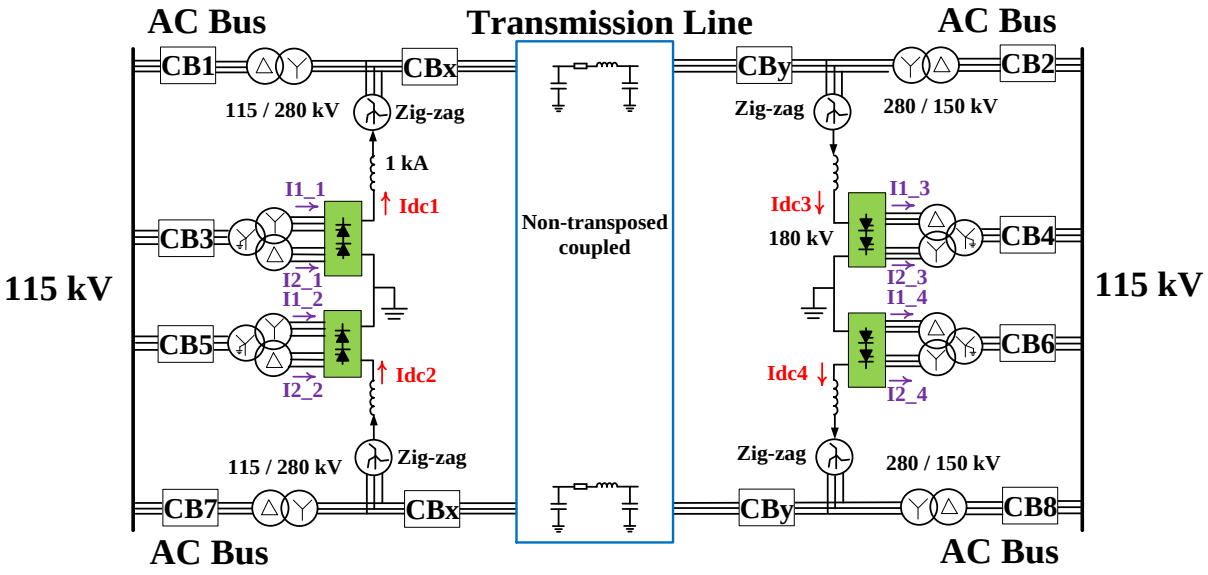


Figure 8-1. System configuration of hybrid ac/dc transmission.

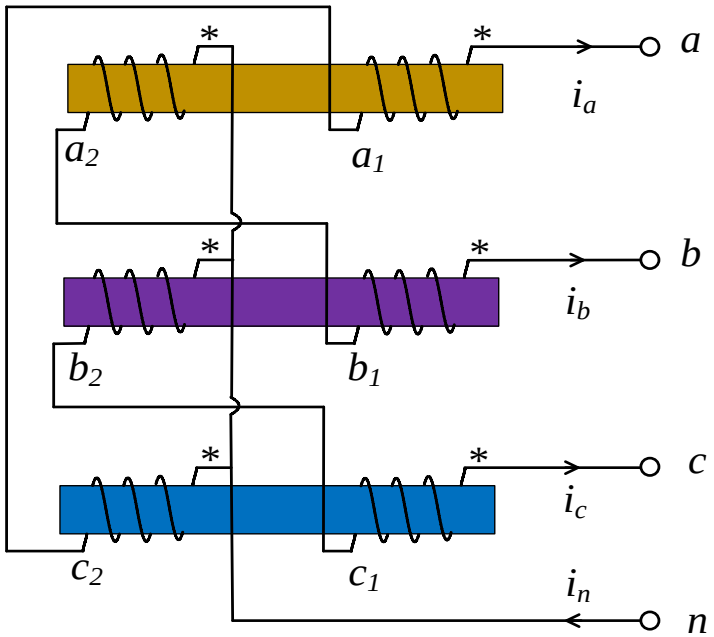


Figure 8-2. Zig-zag transformer.

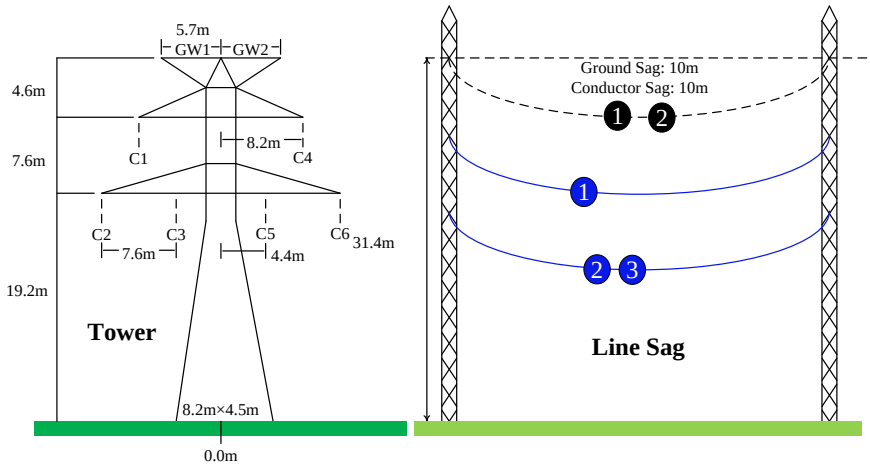


Figure 8-3. Transmission line tower structure.

8.2 HVDC Transformer Saturation Induced by Unbalanced Transmission Line

8.2.1 I_{60} Induced by Non-transposed Lines

A typical 345 kV non-transposed double circuit transmission line is used to investigate the influence of ac transmission on an HVDC station in hybrid ac/dc transmission system. The detailed line parameters are shown in Table 4.

In order to evaluate the induced zero-sequence current, a simulation model without HVDC stations is built, as shown in Figure 8-4.

Table 5 gives the simulation results of zero-sequence currents and ground currents. According to the results, the zero-sequence current increases with the line length. It is because the unbalanced capacitances, which are the main contributor to the zero-sequence current, increase with the line length.

Table 4. Transmission line RLC matrix

Series R matrix (Ω/km)						
Line	**A1**	**B1**	**C1**	**A2**	**B2**	**C2**
A1	0.1249	0.1004	0.1026	0.1070	0.1025	0.1006
B1	0.1004	0.1118	0.0963	0.1001	0.0962	0.0946
C1	0.1026	0.0963	0.1157	0.1025	0.0983	0.0966
A2	0.1070	0.1001	0.1025	0.1249	0.1026	0.1009
B2	0.1025	0.0962	0.0983	0.1026	0.1157	0.0967
C2	0.1006	0.0946	0.0966	0.1009	0.0967	0.1125
Series L matrix (mH/km)						
Line	**A1**	**B1**	**C1**	**A2**	**B2**	**C2**
A1	1.7880	0.8120	0.8170	0.6710	0.6890	0.6290
B1	0.8120	1.8100	0.8670	0.6270	0.6780	0.6150
C1	0.8170	0.8670	1.8020	0.6890	0.7720	0.6770
A2	0.6710	0.6270	0.6890	1.7880	0.8170	0.8310
B2	0.6890	0.6780	0.7720	0.8170	1.8020	0.8650
C2	0.6290	0.6150	0.6770	0.8310	0.8650	1.8090
Parallel C matrix (nF/km)						
Line	**A1**	**B1**	**C1**	**A2**	**B2**	**C2**
A1	10.0480	-1.4852	-1.4525	-0.6046	-0.4867	-0.2287
B1	-1.4852	10.5530	-1.6621	-0.2107	-0.2488	-0.0954
C1	-1.4525	-1.6621	10.7420	-0.4834	-0.8856	-0.2565
A2	-0.6046	-0.2107	-0.4834	10.1050	-1.4230	-1.6725
B2	-0.4867	-0.2488	-0.8856	-1.4230	10.7410	-1.6568
C2	-0.2287	-0.0954	-0.2565	-1.6725	-1.6568	10.4980

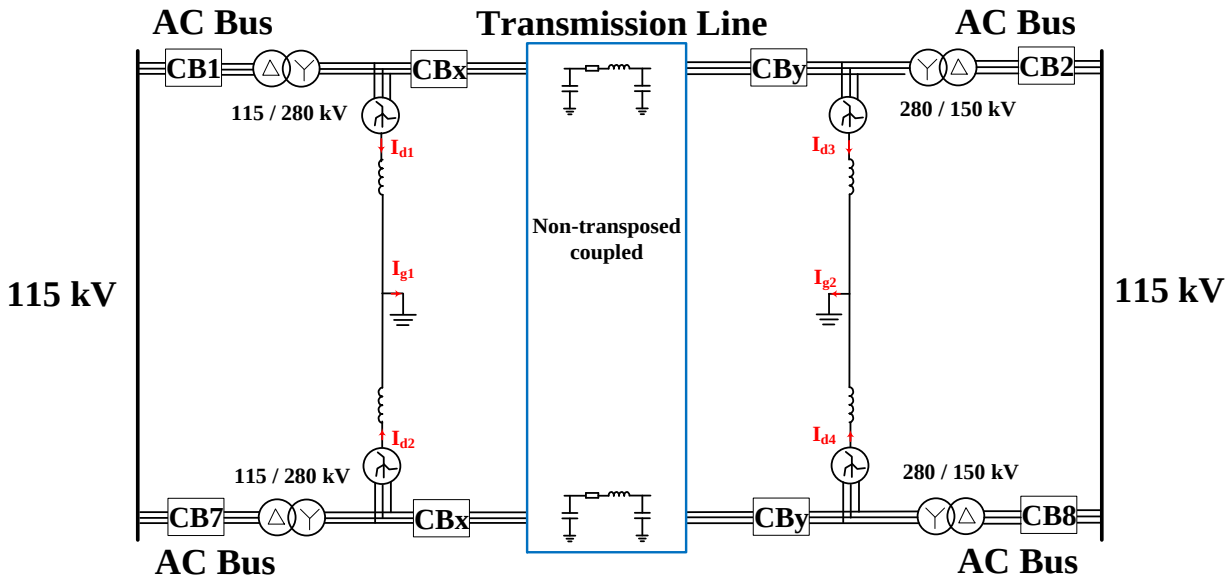


Figure 8-4. Zero sequence current evaluation.

Table 5. Zero sequence current induced by non-transposed transmission lines

Transmission line length	Zero sequence current rms				Ground current rms	
	I_{d1} (A)	I_{d2} (A)	I_{d3} (A)	I_{d4} (A)	I_{g1} (A)	I_{g2} (A)
100 miles (161 km)	4.67	10.40	8.10	5.70	9.20	5.30
200 miles (322 km)	13.52	22.73	18.82	15.40	20.34	15.38
300 miles (483 km)	31.00	42.00	37.00	33.00	39.00	34.00

The zero-sequence current induced by non-transposed double circuit transmission lines can have two flow paths. One is from the neutral point of the zig-zag transformer to ground, and the other path is from the neutral point of one zig-zag transformer to the neutral point of another zig-zag transformer. In the hybrid ac/dc transmission system, the circulating current shows as three phase zero-sequence current on the transmission line, i_{60} on the dc side, and dc components between the HVDC converter and transformer.

The i_{60} circulating loop caused by unbalanced line-to-ground capacitors is shown in Figure 8-5. Assuming balanced three phase voltages are applied to the line-to-ground capacitors and considering the unbalanced capacitances, the currents flowing through the capacitors are unbalanced and contain the zero-sequence component. Because the currents flow into the ground through the capacitors, the i_{60} circulating loop contains the ground and can be separated into two independent loops by the ground.

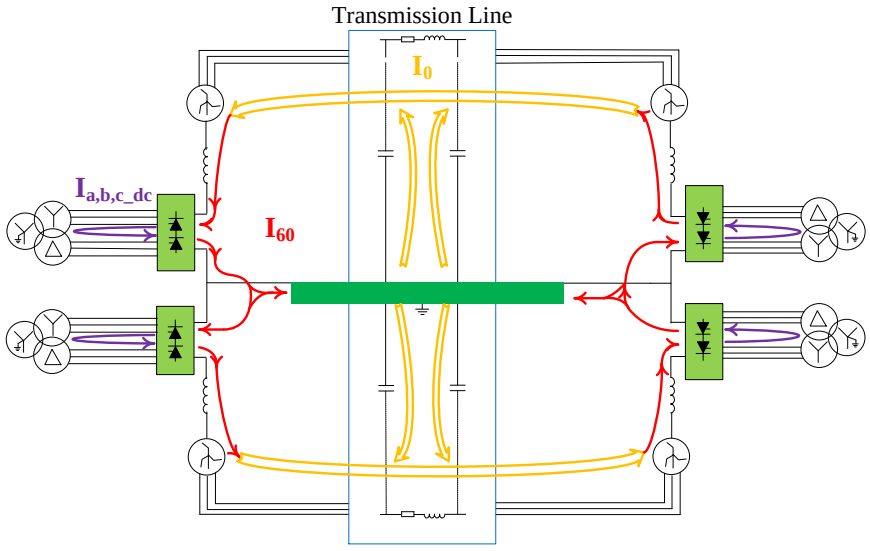


Figure 8-5. I_{60} circulating loop caused by line-to-ground capacitors.

In the i_{60} circulating loop, the impedances between HVDC converter and transformer can be ignored because the currents are dc components and the resistances are small. Two smoothing inductors on dc side and the three-phase line impedance are the main contributor to the impedance of the i_{60} circulating loop.

The i_{60} circulating loop caused by unbalanced line-to-line capacitors is shown in Figure 8-6. Assuming balanced three-phase voltages are applied to the line-to-line capacitors and considering the unbalanced capacitances, the currents flowing through the capacitors are unbalanced and contain zero-sequence current. Because the currents flow from one three-phase line to the other through the capacitance, the i_{60} circulating loop does not include the ground and circulates among the double circuit transmission lines. Four smoothing inductors on dc side and two three-phase line impedances are the main contributor to the impedance of the i_{60} circulating loop.

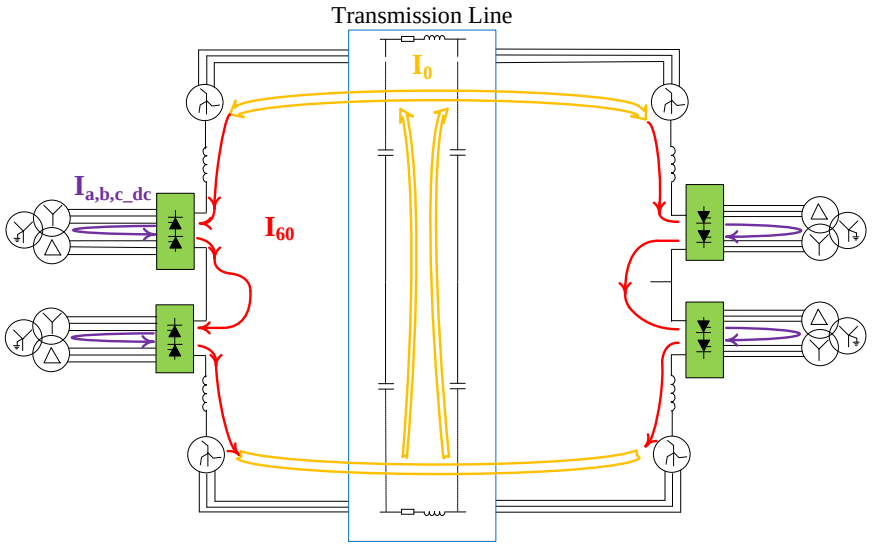


Figure 8-6. I_{60} circulating loop caused by line-to-line capacitors.

8.2.2 I_{60} Influence on Transformer Saturation

According to [80], there is little influence on the converter transformer if I_{60} is less than 0.1% of the rated dc current. But, if I_{60} is larger than 1%, it will cause noticeable impact, including loss of life, audible noise, harmonic generation, etc. Thus, the zero-sequence current induced by non-transposed transmission lines is calculated to evaluate the influence on converter transformer saturation. For the LCC HVDC converter, phase *a* voltage can be assumed as in (8-1).

$$v_{an} = \sqrt{2}V_a \sin\theta \ (\theta = \omega t = 120\pi t) \tag{8-1}$$

Dc side current I'_{dc} includes dc component I_{dc} and fundamental frequency component i_{60} is expressed in (8-2) where β is the angle difference of i_{60} to v_{an} and α is the firing angle.

$$I'_{dc} = I_{dc} + \sqrt{2}I_{60}\sin(\theta - \beta) \tag{8-2}$$

Figure 8-7 shows the waveforms of dc side current and phase A voltage and current. The phase A current can be expressed as in (8-3).

$$I_a = \begin{cases} 0 & 0 \le \theta \le \alpha \\ I_{dc} + \sqrt{2}I_{60}\sin\theta & \alpha < \theta < \alpha + \dfrac{2\pi}{3} \\ 0 & \alpha + \dfrac{2\pi}{3} \le \theta \le \alpha + \pi \\ -I_{dc} - \sqrt{2}I_{60}\sin\theta & \alpha + \pi < \theta < \alpha + \dfrac{5\pi}{3} \\ 0 & \alpha + \dfrac{5\pi}{3} \le \theta < 2\pi \end{cases} \tag{8-3}$$

The dc component of phase A current is obtained as in (8-4).

$$I_{a_{dc}} = \frac{1}{2\pi}\int_0^{2\pi} I_a \, d\theta \tag{8-4}$$

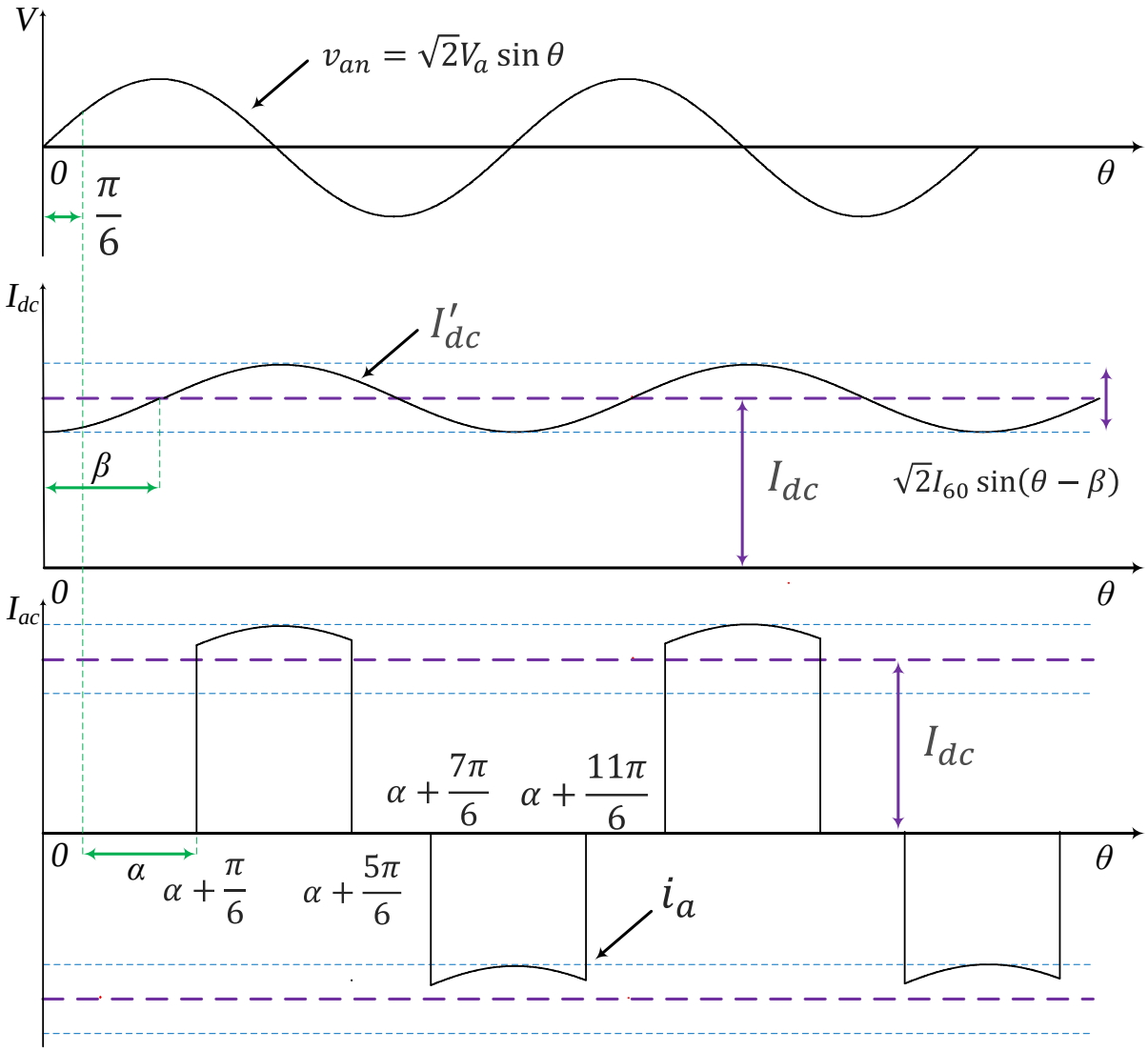


Figure 8-7. Waveforms of LCC HVDC converter.

Submit (8-3) into (8-4), get (8-5).

$$I_{a_{dc}} = \frac{1}{2\pi}\int_{\alpha+\frac{\pi}{6}}^{\alpha+\frac{5\pi}{6}} \left(I_{dc} + \sqrt{2}I_{60}\sin(\theta-\beta)\right) d\theta + \frac{1}{2\pi}\int_{\alpha+\frac{7\pi}{6}}^{\alpha+\frac{11\pi}{6}} \left(-I_{dc} - \sqrt{2}I_{60}\sin(\theta-\beta)\right) d\theta \tag{8-5}$$

Solve (8-5), get (8-6).

$$I_{a_{dc}} = \frac{\sqrt{6}}{\pi} I_{60}\cos(\alpha-\beta) \tag{8-6}$$

Similarly, the dc components of other two phases can be obtained. Therefore, the dc components of three-phase ac currents can be expressed as in (8-7).

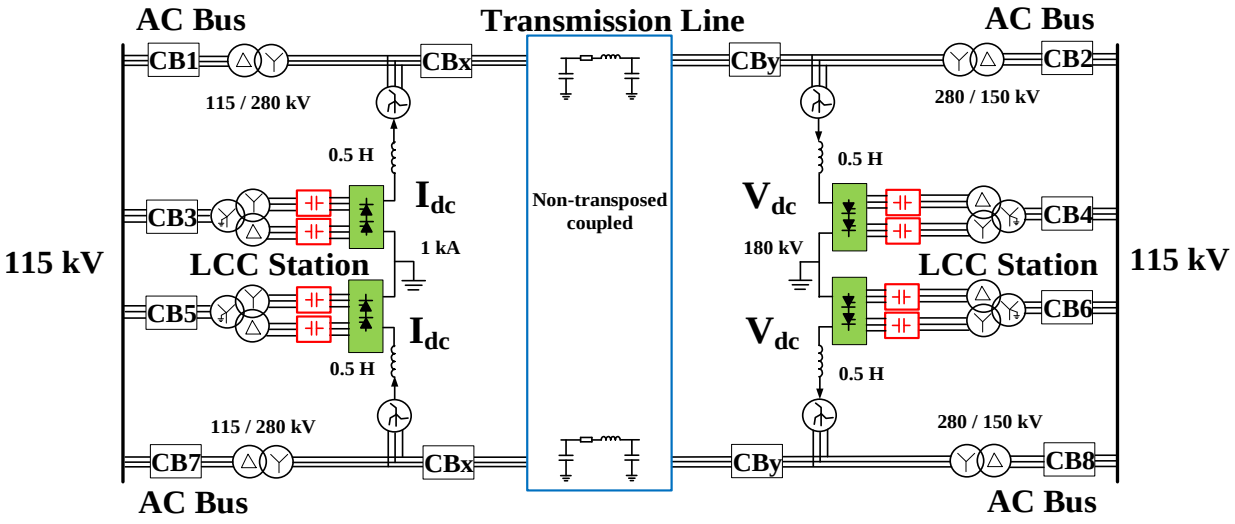


Figure 8-8. CCC HVDC.

$$\begin{cases} I_{a\_dc} = \dfrac{\sqrt{6}}{\pi} I_{60} \cos(\alpha - \beta) \\ I_{b\_dc} = \dfrac{\sqrt{6}}{\pi} I_{60} \cos\left(\alpha - \beta - \dfrac{2\pi}{3}\right) \\ I_{c\_dc} = \dfrac{\sqrt{6}}{\pi} I_{60} \cos\left(\alpha - \beta + \dfrac{2\pi}{3}\right) \end{cases} \tag{8-7}$$

According to (8-7), the three-phase dc current components are linearly proportional to the I_{60}, which means large I_{60} may cause converter transformer saturation.

8.3 Proposed I_{60} Suppression Method

Since the circulating current is a dc component between the HVDC converter and transformer, series capacitors can be used to block the current. The capacitor commutated converter (CCC) HVDC, which is mostly used for weak ac system connection, is implemented to block the circulating current, as shown in Figure 8-8.

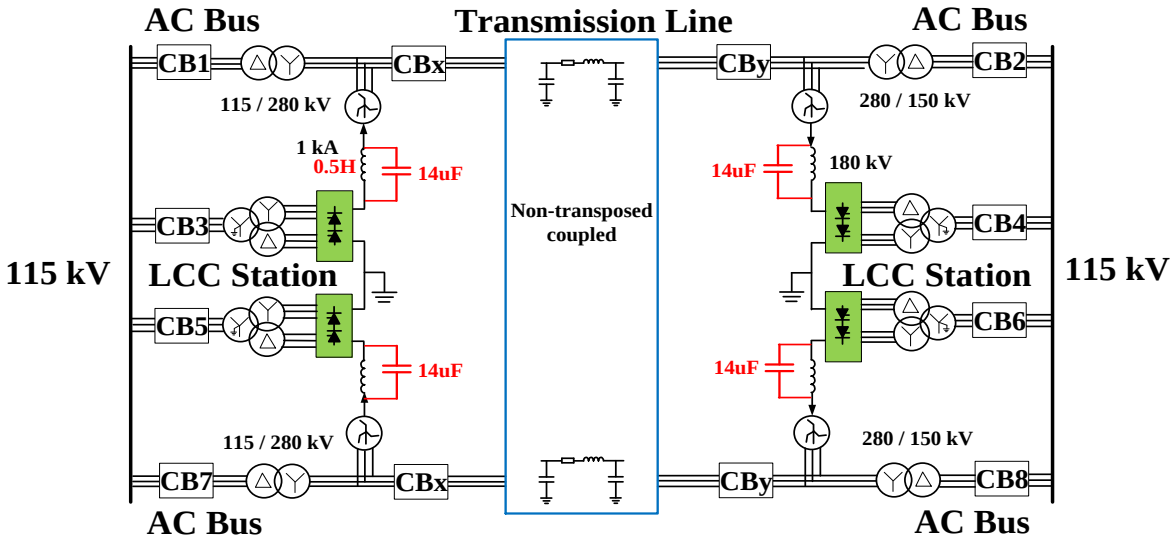


Figure 8-9. Band-stop LC filter.

An alternative method is to use a band-stop LC filter as shown in Figure 8-9, because the circulating current on dc side is at the fundamental frequency. The capabilities to limit the dc current in the converter transformer windings for both methods have been verified in simulation.

8.4 Simulation Results

A simulation platform of the hybrid ac/dc transmission simulation system is built with parameters given in Table 6 and the topology is the same as in Figure 8-1. The dc side current waveforms are shown in Figure 8-10. The dc side current waveforms of using method 1 (CCC HVDC) and method 2 (band-stop LC filter) are shown as in Figure 8-11 and Figure 8-12, respectively. The I_{60} and converter transformer dc current component values under original, CCC HVDC and band-stop LC filter cases are given in Table 7. The simulation results show that the I_{60} is higher than 1% of the rated dc current and the dc current components exist in converter transformer windings if no limiting method is implemented, and both proposed methods can suppress the i_{60} and block the dc current components in transformer windings.

Table 6. Hybrid ac/dc system parameters

Parameters	Values
Line length	200 miles
Line voltage	AC: 280 kV DC:180 kV
Line current	AC: 612 A DC:1000 A
Transmission power	729 MW (AC: 189 MW DC: 540 MW)
Transformer	115 kV / 280 kV

Table 7. I_{60} and dc component values

Variables	Original Case	CCC-HVDC	Band-stop LC Filter
I_{60} in I_{dc1} (A)	18	0	0
I_{60} in I_{dc2} (A)	27	0	0
I_{60} in I_{dc3} (A)	18	0	0
I_{60} in I_{dc4} (A)	15	0	0
I_{dc} in I_{1_1} (A)	A: -10 B: 18 C: -8	A: 0 B: 0 C: 0	A: 0 B: 0 C: 0
I_{dc} in I_{2_1} (A)	A: -2 B: 18 C: -16	A: 0 B: 0 C: 0	A: 0 B: 0 C: 0
I_{dc} in I_{1_2} (A)	A: -28 B: 12 C: 16	A: 0 B: 0 C: 0	A: 0 B: 0 C: 0
I_{dc} in I_{2_2} (A)	A: -25 B: 22 C: 3	A: 0 B: 0 C: 0	A: 0 B: 0 C: 0
I_{dc} in I_{1_3} (A)	A: 8 B: 2 C: -10	A: 0 B: 0 C: 0	A: 0 B: 0 C: 0
I_{dc} in I_{2_3} (A)	A: 10 B: -3 C: -7	A: 0 B: 0 C: 0	A: 0 B: 0 C: 0
I_{dc} in I_{1_4} (A)	A: -4 B: 10 C: -6	A: 0 B: 0 C: 0	A: 0 B: 0 C: 0
I_{dc} in I_{2_4} (A)	A: 2 B: 7 C: -9	A: 0 B: 0 C: 0	A: 0 B: 0 C: 0

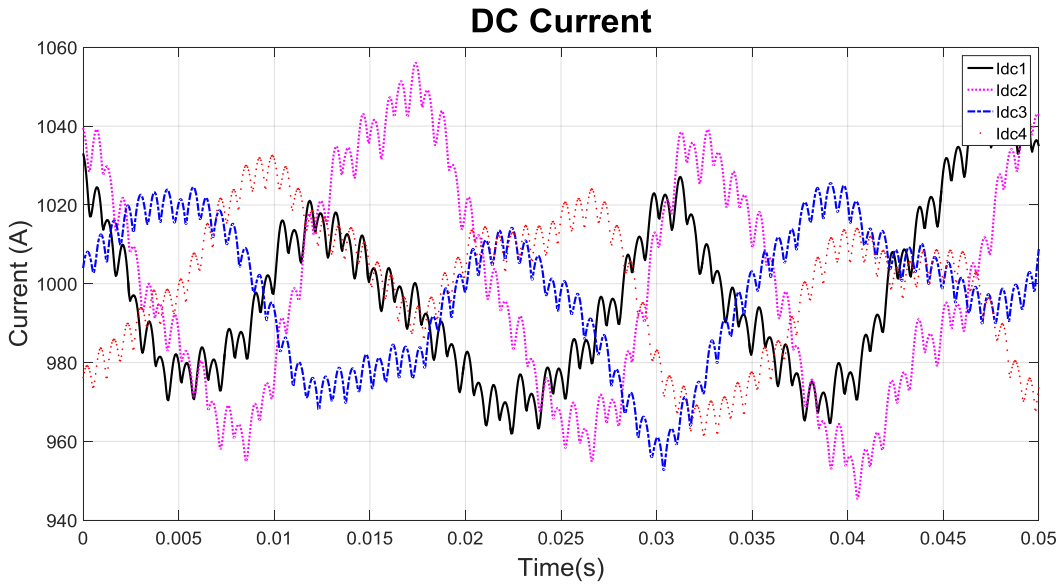


Figure 8-10. Original case dc side waveforms.

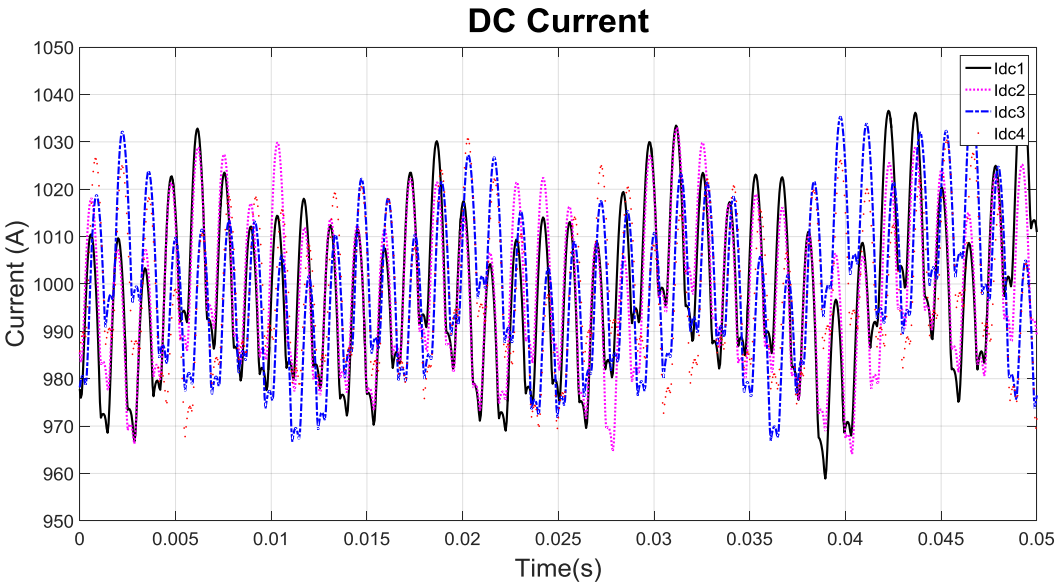


Figure 8-11. CCC HVDC dc side waveforms.

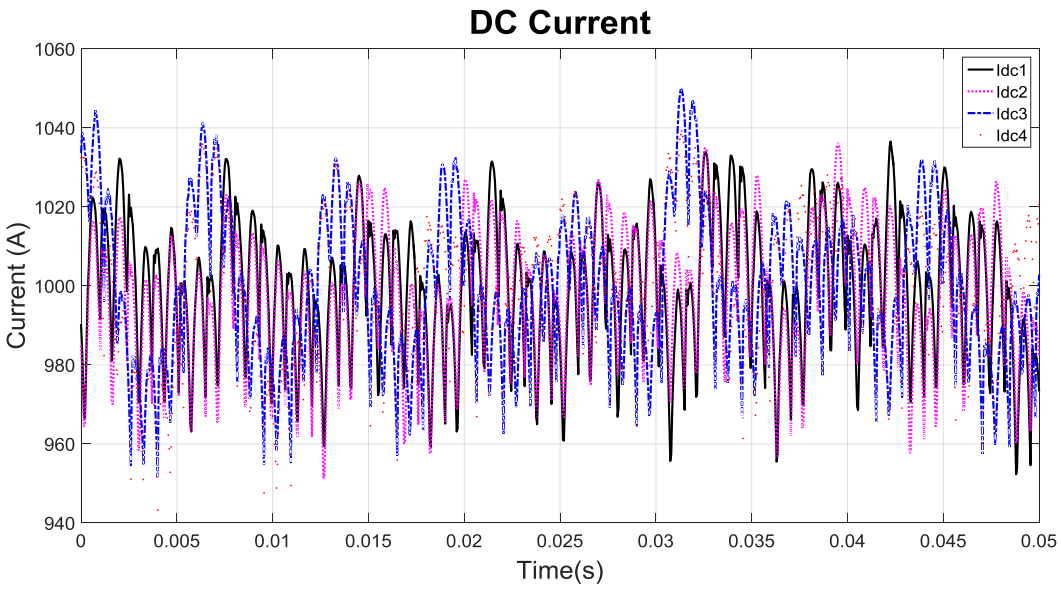


Figure 8-12. Band-stop LC filter dc side waveforms.

8.5 Conclusion

The zero-sequence current induced by non-transposed coupled transmission lines has been investigated through a typical 345 kV double circuit transmission line, and the influence of i_{60} on the HVDC converter transformer has been analyzed and simulated. The CCC HVDC and band-stop LC filter methods are proposed and verified to limit the i_{60} and avoid converter transformer saturation. Compared with the conventional HVDC, the CCC HVDC is cost-effective for weak ac system connection. The band-stop LC filter method will add extra cost for the filter capacitor and inductor, but it is possible to share a part of the smoothing inductor as the filter inductance.

9 Dc Fault Impact on Ac System Stability

This chapter introduces the voltage source converters (VSCs) for high voltage dc (HVDC) applications and analysis their performances under dc fault conditions. The characteristics of dc and ac grids under fault conditions are investigated for both the point-to-point and multi-terminal grid configurations. The dc fault impact on interconnected ac system stability by using different protection schemes is evaluated by comparing with an equivalent ac fault.

9.1 HVDC Converter Dc Fault Analysis

The state-of-the-art VSC HVDC topology is the MMC, as shown in Figure 9-1. The submodules in MMC can be either half-bridge or full-bridge, as shown in Figure 9-2(a) and Figure 9-2(b), respectively. The red lines and blue arrows indicate the possible fault current contribution loop from ac side to dc side under dc fault conditions. The half-bridge MMC cannot block the dc fault current by turning off the switches, as the fault current can still flow through the anti-parallel diodes. By inserting the submodule capacitors into the fault current loop, the full-bridge MMC can block the dc fault current. As a simple type of three-phase VSC, the two-level VSC is also used in the VSC-HVDC system. Figure 9-3 shows the fault current loop in a two-level VSC. During a dc fault, the fault current is contributed from both the ac side and dc capacitor. Considering the large dc fault current and low damping resistance, the dc fault current with both half-bridge MMC and two-level VSC will circulate through the anti-parallel diodes in each branch, as shown in Figure 9-4. Neglecting the small voltage drops of the anti-parallel diodes, the H-bridge ac terminal voltage is zero. Thus, the dc fault equivalently creates a three-phase fault on the converter ac side. The fault impedance is the ac filter impedance.

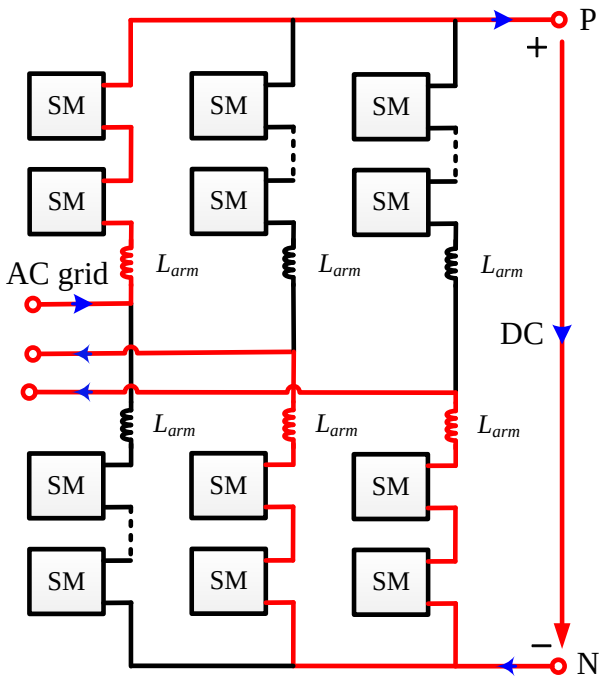
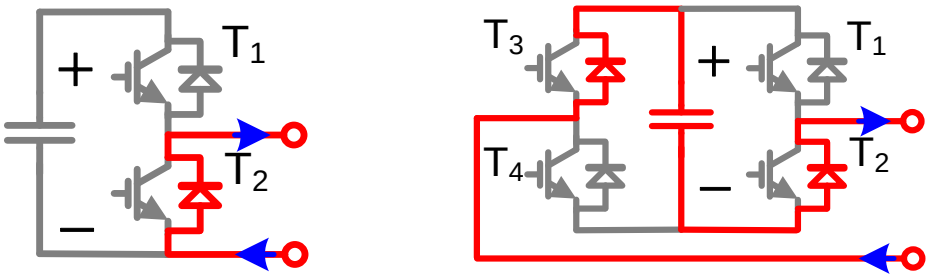


Figure 9-1. MMC topology.



(a) (b)

Figure 9-2. MMC submodule fault current loop: (a) Half-bridge; (b) Full-bridge.

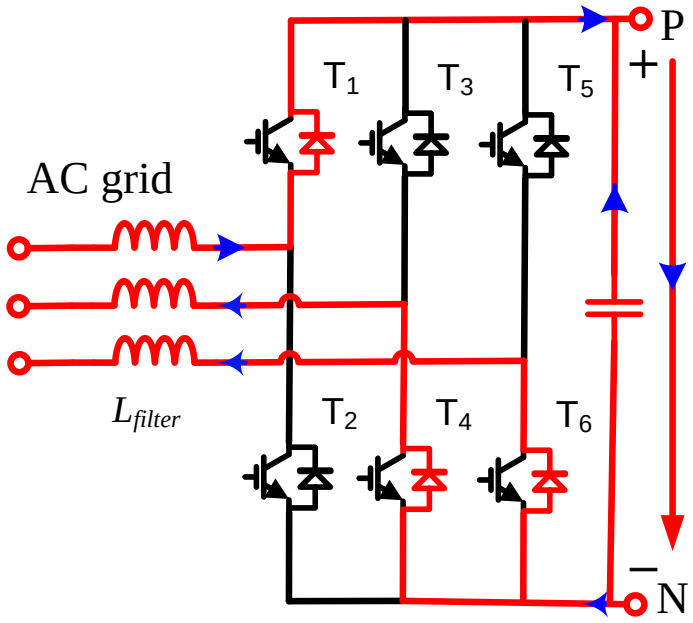


Figure 9-3. Two-level VSC topology.

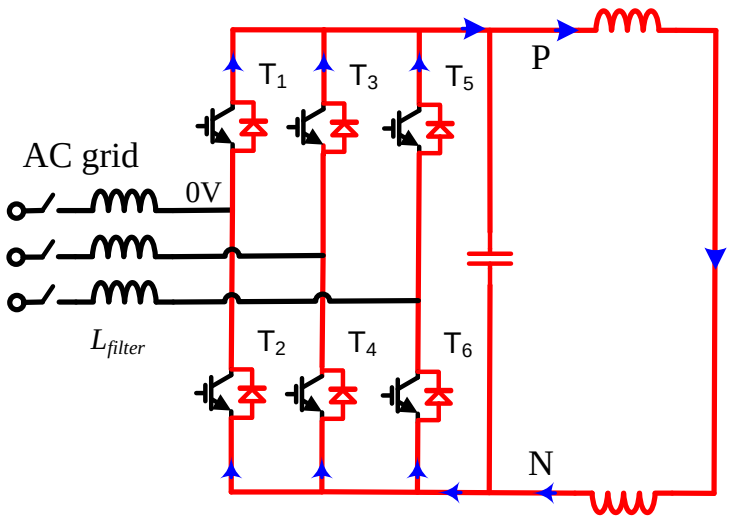


Figure 9-4. Diode freewheel.

9.2 Dc Fault Impact on Dc Grid and Interconnected Ac System Stability

As the most severe short-circuit fault in ac system, the three-phase short-circuit causes the fault location voltage to be zero, and the voltage rises as the distance to the fault location increases. Thus, the fault has less impact on buses far away from the fault location due to the less voltage drop. However, a dc pole-to-pole fault pulls the whole dc grid voltage down to zero since the voltage drop across the line resistance is negligible.

9.2.1 Point-to-point Configuration

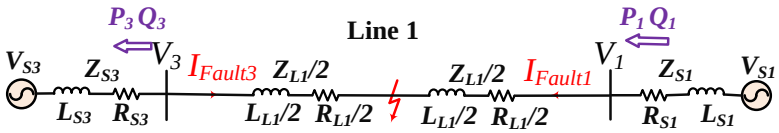
Figure 9-5(a) shows the point-to-point ac transmission with a three-phase short-circuit fault. The voltage at the fault location is zero and the ac bus voltages can be expressed in (9-1).

$$\begin{cases} V_1 = \dfrac{I_{Fault1} Z_{L1}}{2} = \dfrac{\frac{Z_{L1}}{2}}{\left(\frac{Z_{L1}}{2} + Z_{S1}\right)} V_{S1} \\ V_3 = \dfrac{I_{Fault3} Z_{L1}}{2} = \dfrac{\frac{Z_{L1}}{2}}{\left(\frac{Z_{L1}}{2} + Z_{S3}\right)} V_{S3} \end{cases} \tag{9-1}$$

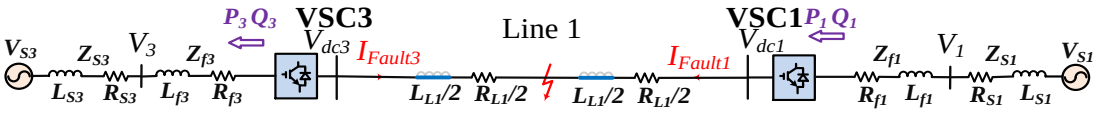
The point-to-point dc transmission with a pole-to-pole short-circuit fault is shown in Figure 9-5(b). The dc side voltage is zero and the HVDC converter ac bus voltages are expressed in (9-2).

$$\begin{cases} V_1 = Z_{f1}/(Z_{f1} + Z_{S1}) V_{S1} \\ V_3 = Z_{f3}/(Z_{f3} + Z_{S3}) V_{S3} \end{cases} \tag{9-2}$$

Though the fault does not pull the two terminal ac voltages down to zero, both ac and dc transmissions lose the power transfer capability.



(a)



(b)

Figure 9-5. Point-to-point transmission: (a) Ac transmission case; (b) Dc transmission case.

9.2.2 Multi-terminal Configuration

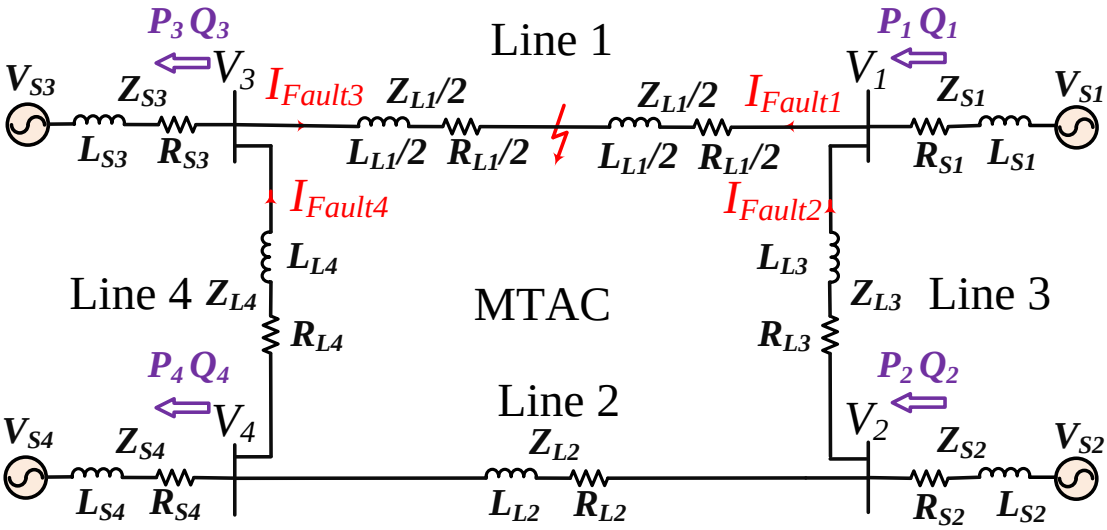
Figure 9-6(a) shows a 4-terminal ac transmission with a three-phase short-circuit fault. Bus 1 and 3 voltages are determined by the total fault current, as expressed in (9-3).

$$\begin{cases} V_1 = I_{Fault1} Z_{L1}/2 \\ V_3 = I_{Fault3} Z_{L1}/2 \end{cases} \tag{9-3}$$

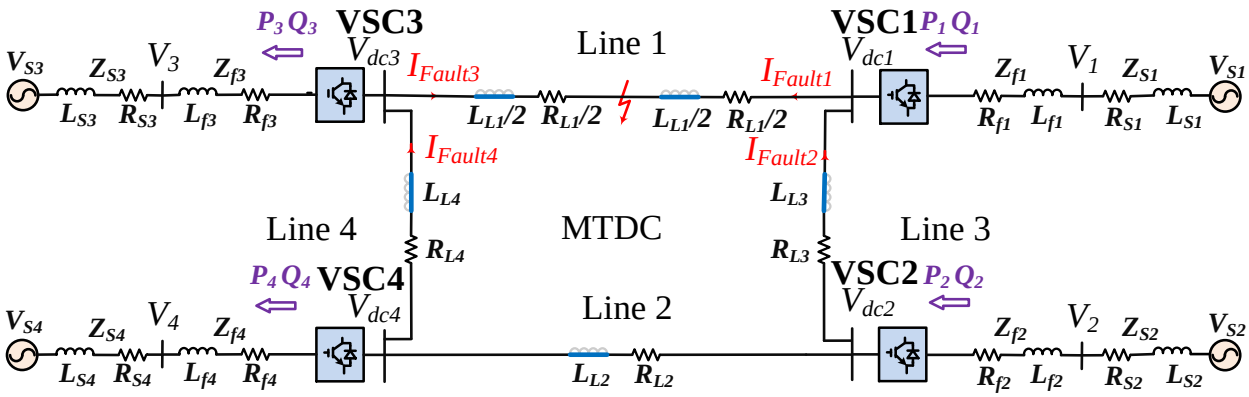
Considering the voltages across line 3 and 4, bus 2 and 4 voltages are expressed in (9-4).

$$\begin{cases} V_2 = V_1 + I_{Fault2} Z_{L3} \\ V_4 = V_3 + I_{Fault4} Z_{L4} \end{cases} \tag{9-4}$$

Since bus 2 and 4 voltages may not drop too much, the transmission line between bus 2 and 4 can maintain certain power transfer capability.



(a)



(b)

Figure 9-6. Multi-terminal transmission: (a) Ac grid case; (b) Dc grid case.

The MTDC with a pole-to-pole short-circuit fault is shown in Figure 9-6(b). The dc grid loses the power transfer capability since the dc side voltage drops to around zero. The ac bus voltages of the HVDC converters are determined by the ac system and filter impedances, as expressed in (9-5).

$$\begin{cases} V_1 = Z_{f1}/(Z_{f1} + Z_{S1})V_{S1} \\ V_2 = Z_{f2}/(Z_{f2} + Z_{S2})V_{S2} \\ V_3 = Z_{f3}/(Z_{f3} + Z_{S3})V_{S3} \\ V_4 = Z_{f4}/(Z_{f4} + Z_{S4})V_{S4} \end{cases} \tag{9-5}$$

9.2.3 Dc Fault Impact on Connected Ac System Stability

The dc fault impact on the connected ac system includes the MTDC power transfer capability loss and an equivalent three-phase short-circuit fault on the ac side of each HVDC converter, as shown in Figure 9-7. The power transfer capability loss impact on ac system depends on the percentage of the power delivered through MTDC. The equivalent ac fault impact on ac system depends on the HVDC converter ac filter impedance and the number of HVDC converters.

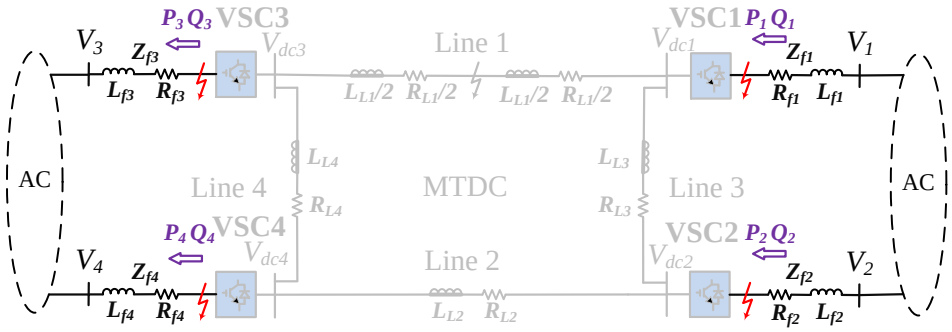


Figure 9-7. Equivalent ac faults caused by dc fault.

9.3 Simulation Results and Analysis

The dc and ac simulation platforms are built in MATLAB to verify the dc and ac grid characteristics under fault conditions and the fault impact on ac system. The point-to-point transmission and multi-terminal system topologies are shown in Figure 9-5 and Figure 9-6, respectively. The simulation platform can correspond to the hypothetical MTDC system transferring power form two windfarms in Cape Cod Bay area to two onshore load centers in Massachusetts (U.S.) and Connecticut (U.S.), as shown in Figure 9-8 [94].

The per unit values of system parameters are shown in Table 8. Figure 9-9 shows the HVDC station control diagram. The HVDC station VSC3 operates at constant dc voltage and constant reactive power mode. The other three VSC stations operate at constant active power and constant reactive power mode.

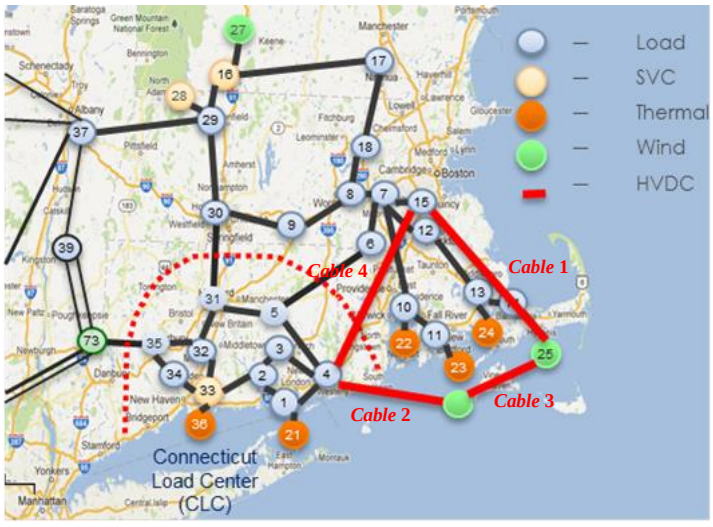


Figure 9-8. Cape Wind Project hypothetical system in Northeast Power Coordinating Council (NPCC) system.

Table 8. System parameters for ac and dc fault simulation

Source 1		**Source 2**		**Source 3**		**Source 4**	
V_{S1}	θ_1	V_{S2}	θ_2	V_{S3}	θ_3	V_{S4}	θ_4
1 p.u.	35°	1 p.u.	35°	1 p.u.	0°	1 p.u.	0°
Z_{S1} (p.u.)		**Z_{S2} (p.u.)**		**Z_{S3} (p.u.)**		**Z_{S4} (p.u.)**	
L_{S1}	R_{S1}	L_{S2}	R_{S2}	L_{S3}	R_{S3}	L_{S4}	R_{S4}
0.2300	0.0068	0.2300	0.0068	0.2300	0.0068	0.2300	0.0068
Z_{L1} (p.u.)		**Z_{L2} (p.u.)**		**Z_{L3} (p.u.)**		**Z_{L4} (p.u.)**	
L_{L1}	R_{L1}	L_{L2}	R_{L2}	L_{L3}	R_{L3}	L_{L4}	R_{L4}
0.1120	0.0120	0.0930	0.0080	0.0900	0.0020	0.1270	0.0350
Z_{f1} (p.u.)		**Z_{f2} (p.u.)**		**Z_{f3} (p.u.)**		**Z_{f4} (p.u.)**	
L_{f1}	R_{f1}	L_{f2}	R_{f2}	L_{f3}	R_{f3}	L_{f4}	R_{f4}
0.1500	0.0015	0.1900	0.0019	0.1500	0.0015	0.1900	0.0019

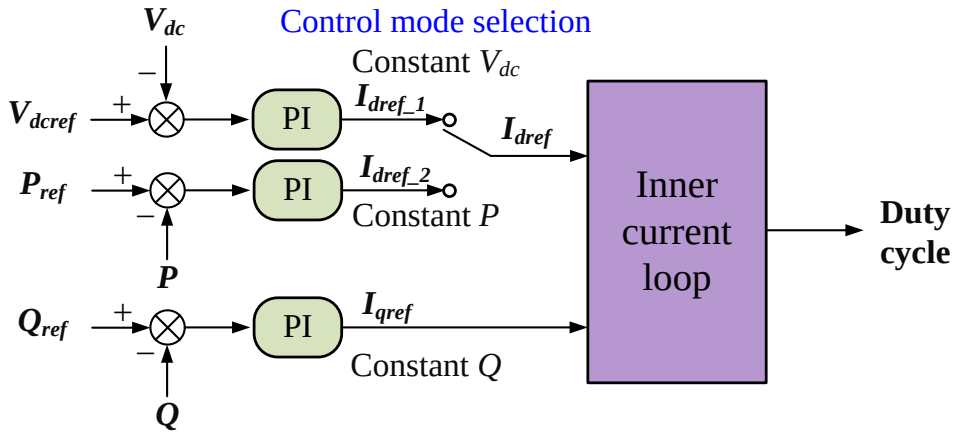


Figure 9-9. HVDC station control diagram.

9.3.1 Point-to-point Ac and Dc Transmission Comparison

The simulation results for the point-to-point transmission case are shown in Table 9. The steady state values before the fault happens are shown in the "Normal" column. The steady state values after the fault happens are shown in the "Fault" column. For the ac transmission during fault, the bus voltages and active powers drop to around 0.2 p.u. and 0 p.u., respectively. For the dc transmission, the ac bus voltages, dc voltages and active powers drop to around 0.4 p.u., 0 p.u. and 0 p.u., respectively. Both ac and dc transmissions lose the power transfer capability and the results match with (9-1) and (9-2).

9.3.2 Multi-terminal Ac and Dc Transmission Comparison

The simulation results for the multi-terminal case are shown in Table 10. The steady state values before the fault happens are shown in the "Normal" column. The steady state values after the fault happens are shown in the "Fault" column. For the multi-terminal ac (MTAC) during fault, the voltage drop and active power loss of bus 1 and bus 3 is larger than that of bus 2 and bus 4, which are located further away from the fault location.

The positive value of P_4 indicates that the bus 2 and bus 4 remain certain power transfer capability. For the MTDC system during fault, the ac and dc voltages drop to around 0.4 p.u. and 0 p.u., respectively. The positive values of P_1 and P_2 and negative values of P_3 and P_4 indicate that all active powers flow into the MTDC grid for the grid power loss. The MTDC loses the power transfer capability. Based on the results, the ac fault impact decreases as the distance from the fault location increases, but the dc fault impact is significant within the whole MTDC grid. At the same time, there is an equivalent three-phase short-circuit fault on the ac side of each HVDC converter since dc voltages almost drop to zero.

Table 9. Point-to-point ac and dc transmission comparison

Grid type	V_1 (p.u.)		V_3 (p.u.)		P_1 (p.u.)		P_3 (p.u.)	
	Normal	Fault	Normal	Fault	Normal	Fault	Normal	Fault
AC	0.974	0.196	0.966	0.196	0.890	0.068	0.880	-0.068
DC	1.000	0.393	0.940	0.393	0.870	0.060	0.850	-0.060
Grid type	Q_1 (p.u.)		Q_3 (p.u.)		V_{dc1} (p.u.)		V_{dc3} (p.u.)	
	Normal	Fault	Normal	Fault	Normal	Fault	Normal	Fault
AC	-0.041	0.589	-0.043	-0.589	Not available			
DC	-0.130	0.890	-0.130	-0.890	1.008	0.015	1.000	0.015

Table 10. Multi-terminal ac and dc comparison

Grid type	V_1 (p.u.)		V_2 (p.u.)		V_3 (p.u.)		V_4 (p.u.)	
	Normal	Fault	Normal	Fault	Normal	Fault	Normal	Fault
AC	0.978	**0.283**	0.976	**0.461**	0.972	**0.265**	0.972	**0.479**
DC	0.998	**0.382**	0.998	**0.390**	0.936	**0.381**	0.930	**0.393**
Grid type	P_1 (p.u.)		P_2 (p.u.)		P_3 (p.u.)		P_4 (p.u.)	
	Normal	Fault	Normal	Fault	Normal	Fault	Normal	Fault
AC	0.910	0.190	0.780	0.430	0.890	0.030	0.780	**0.160**
DC	0.865	0.100	0.740	0.210	0.837	-0.100	0.738	-0.210
Grid type	Q_1 (p.u.)		Q_2 (p.u.)		Q_3 (p.u.)		Q_4 (p.u.)	
	Normal	Fault	Normal	Fault	Normal	Fault	Normal	Fault
AC	-0.064	0.744	-0.050	0.711	-0.019	-0.732	-0.005	-0.778
DC	-0.140	0.870	-0.100	0.700	-0.130	-0.870	-0.120	-0.700
Grid type	V_{dc1} (p.u.)		V_{dc2} (p.u.)		V_{dc3} (p.u.)		V_{dc4} (p.u.)	
	Normal	Fault	Normal	Fault	Normal	Fault	Normal	Fault
DC	1.007	0.030	1.006	0.072	1.000	0.020	1.001	0.078

9.3.3 Dc Fault Impact on Ac System Evaluation

A scale-down three-area system, which represents a reduced NPCC region, is built in MATLAB to evaluate the dc fault impact on connected ac system, as shown in Figure 9-10. Area 1, 2, and 3 represent the New York area, New England area, and the Connecticut area, respectively. The offshore wind is connected to the ac system through a MTDC. An equivalent MTAC is built to replace the MTDC for comparison, as shown in Figure 9-6 and Table 8.

Three dc fault protection schemes are implemented separately in the MTDC to evaluate the dc fault impact on ac system with different protection schemes. Figure 9-11 shows the detailed protection strategy, including the ac fault protection. The three dc fault protection schemes are: 1) dc breakers, 2) full-bridge MMCs with dc contactors, 3) ac breakers with dc contactors.

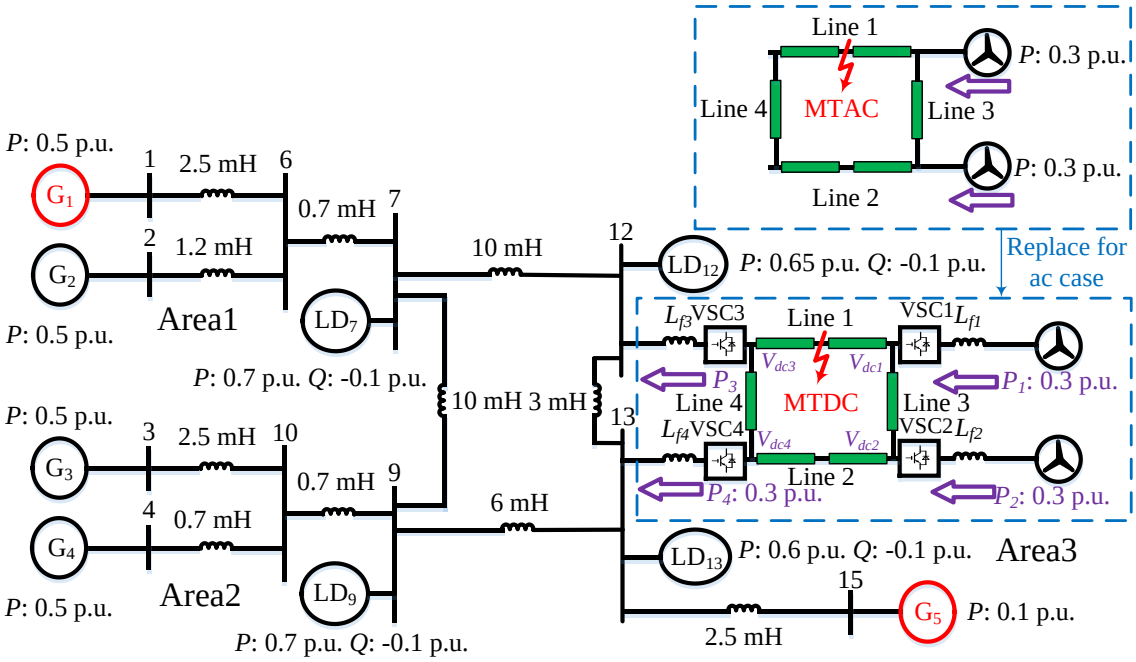


Figure 9-10. Three-area system with offshore wind farm.

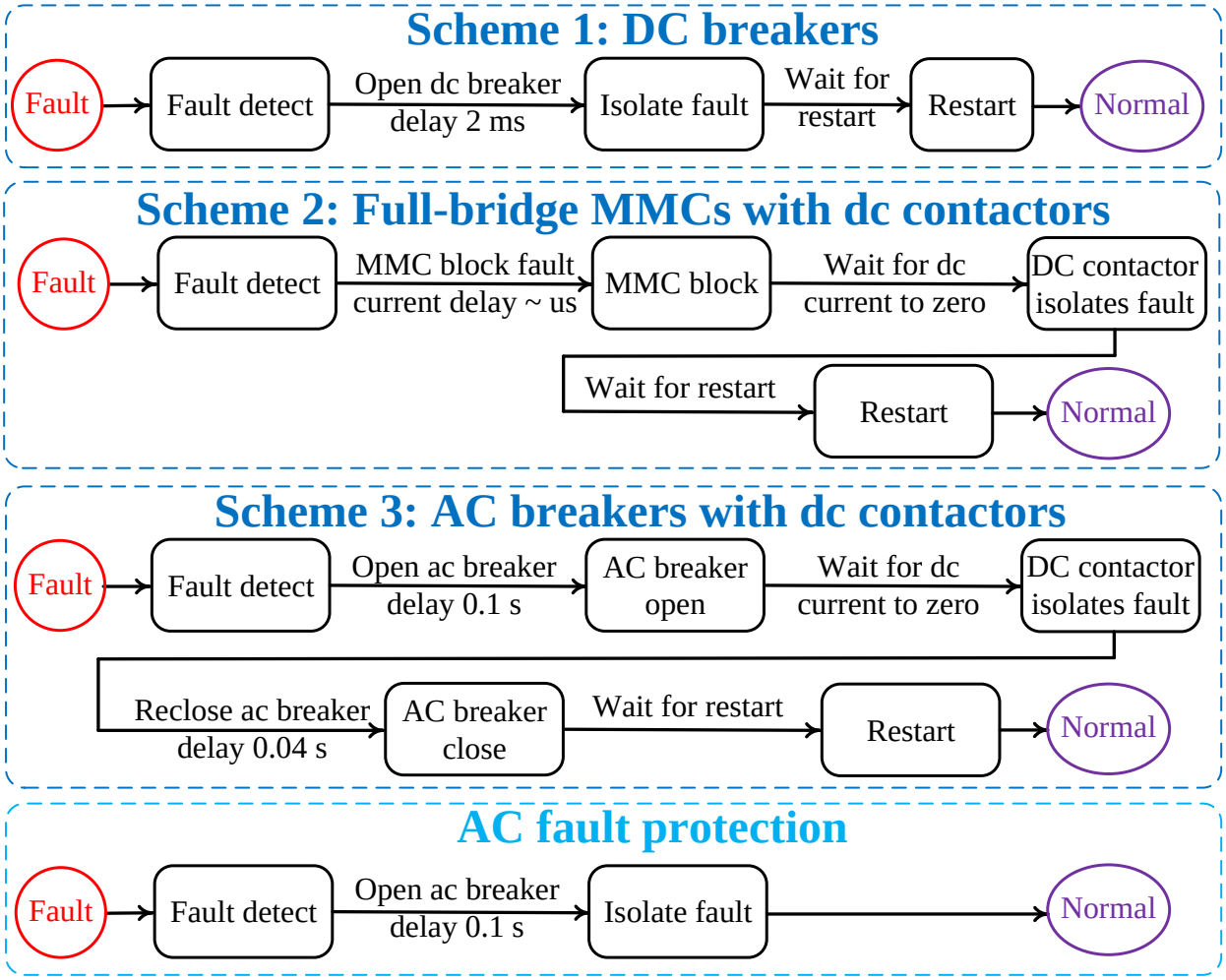


Figure 9-11. Dc and ac fault protection schemes.

A permanent pole-to-pole dc short circuit happens at 0.1s. The VSC dc side voltages and ac side active powers are shown in Figure 9-12, Figure 9-13, and Figure 9-14 with the dc fault protection scheme 1, scheme 2, and scheme 3, respectively.

1) Scheme 1: The equivalent ac fault duration is around zero since dc voltages are further above zero, as shown in Figure 9-12(a). The power transfer capability loss duration is around 0.05 s considering the active power recovery, as shown in Figure 9-12(b).

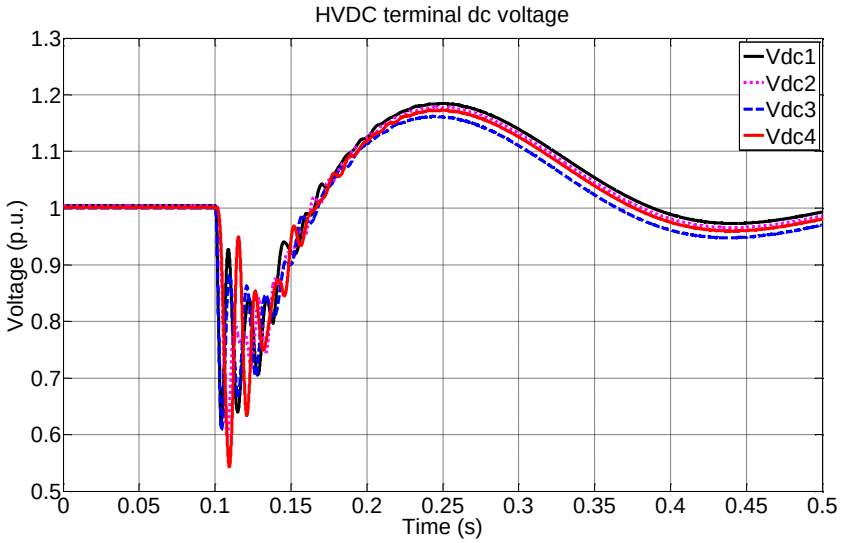
2) Scheme 2: The equivalent ac fault duration is around 0.02 s since dc voltages drop to around zero, as shown in Figure 9-13(a). The negative dc voltages indicate that the dc fault currents are blocked by the full-bridge MMCs. The power transfer capability loss duration is around 0.15 s considering the active power recovery, as shown in Figure 9-13(b).

3) Scheme 3: The equivalent ac fault duration is around 0.1 s since dc voltages maintain around zero until 0.2 s, as shown in Figure 9-14(a). The power transfer capability loss duration is around 0.4 s considering the active power recovery, as shown in Figure 9-14(b).

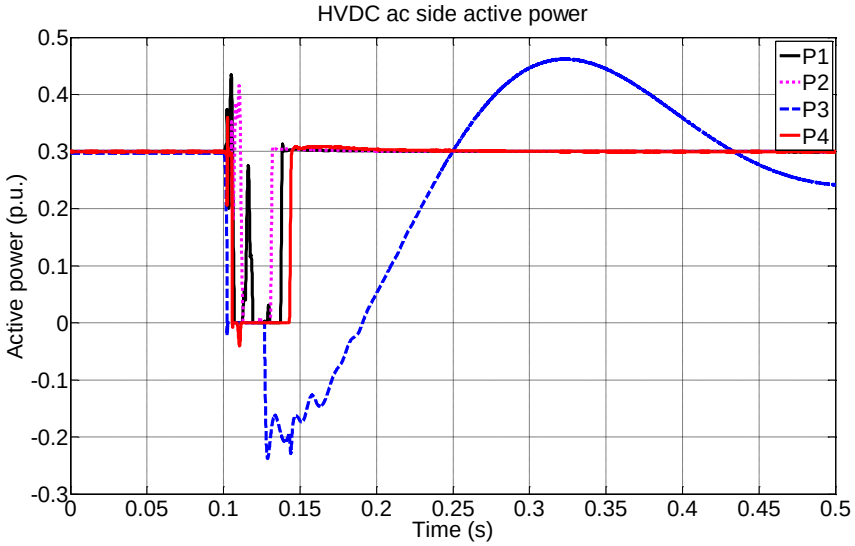
Table 11 summaries the equivalent ac fault duration time and power transfer capability loss duration time for the three dc fault protection schemes.

Table 11. Equivalent ac fault and power transfer capability loss duration time with three different dc fault protection schemes

Duration time	**Scheme 1**	**Scheme 2**	**Scheme 3**
Power transfer loss	0.05s	0.15s	0.4s
Equivalent ac fault	0.0s	0.02s	0.1s

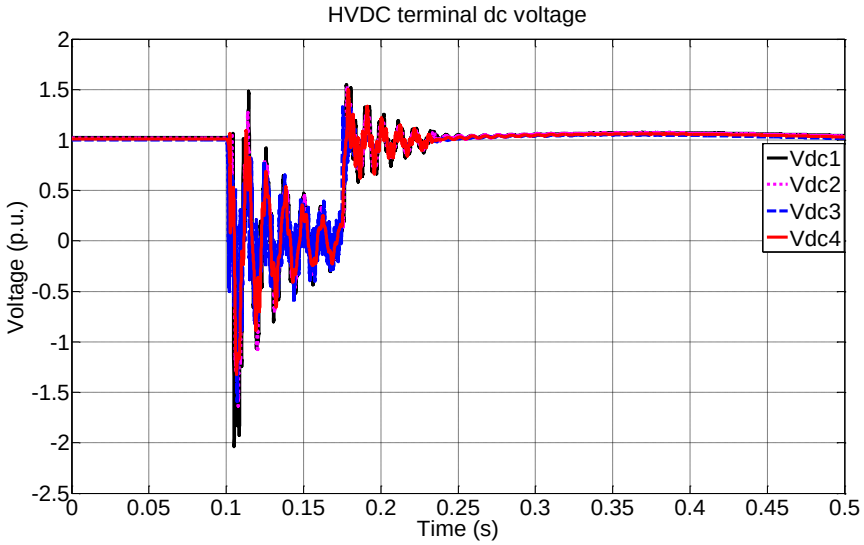


(a)

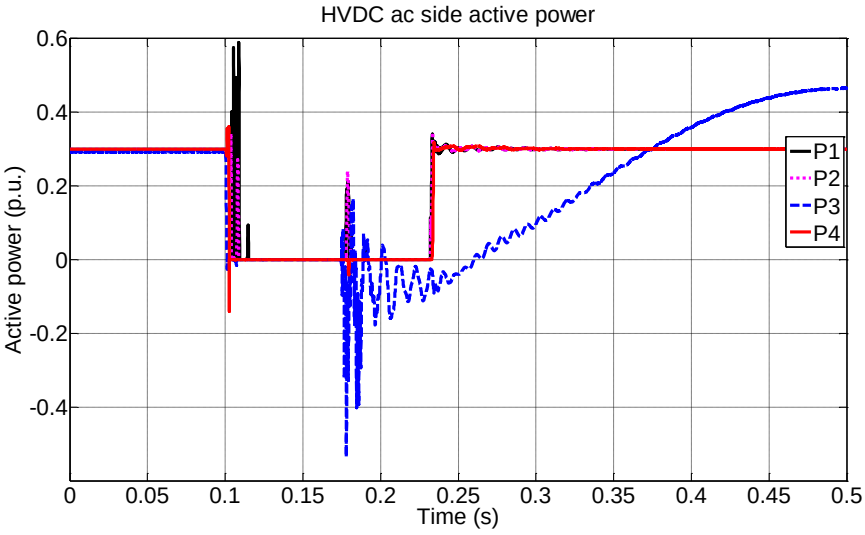


(b)

Figure 9-12. Waveforms with dc fault protection scheme 1: (a) VSC dc side voltages; (b) VSC ac side active powers.

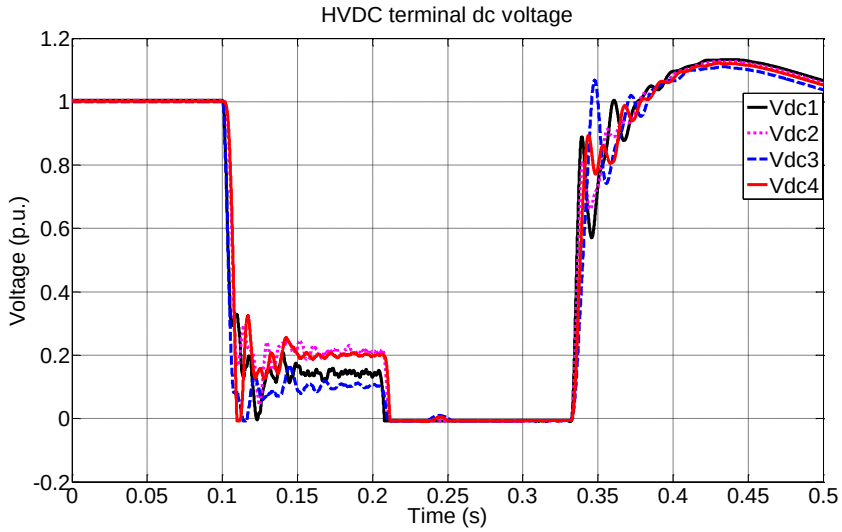


(a)

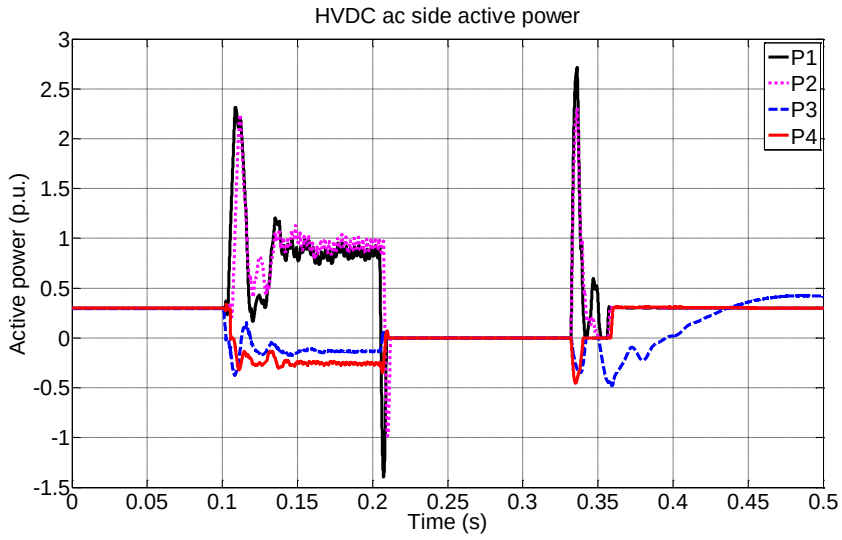


(b)

Figure 9-13. Waveforms with dc fault protection scheme 2: (a) VSC dc side voltages; (b) VSC ac side active powers.



(a)



(b)

Figure 9-14. Waveforms with dc fault protection scheme 3: (a) VSC dc side voltages; (b) VSC ac side active powers.

Since the power angle difference between generators G5 and G1 is the largest one, it is chosen to evaluate the fault impact on the ac system transient stability. Figure 9-15 shows the angle variations with three dc fault protection schemes. According to the first peak angle value, the dc fault impact on ac system is small with the dc protection scheme 1. The dc fault protection scheme 2 has similar performance as the ac fault case. The dc fault impact on ac system is larger with the dc protection scheme 3. The system is transient stable under all protection schemes since the angle is within -180°.

According to the simulation results, the dc fault impact on ac system can be small if fast dc breakers or full-bridge MMCs are implemented. The fast dc breaker can even make the impact smaller than the equivalent MTAC case. Though the dc fault impact on ac system is large if ac breakers are employed to deal with the dc fault, the system is still transient stable.

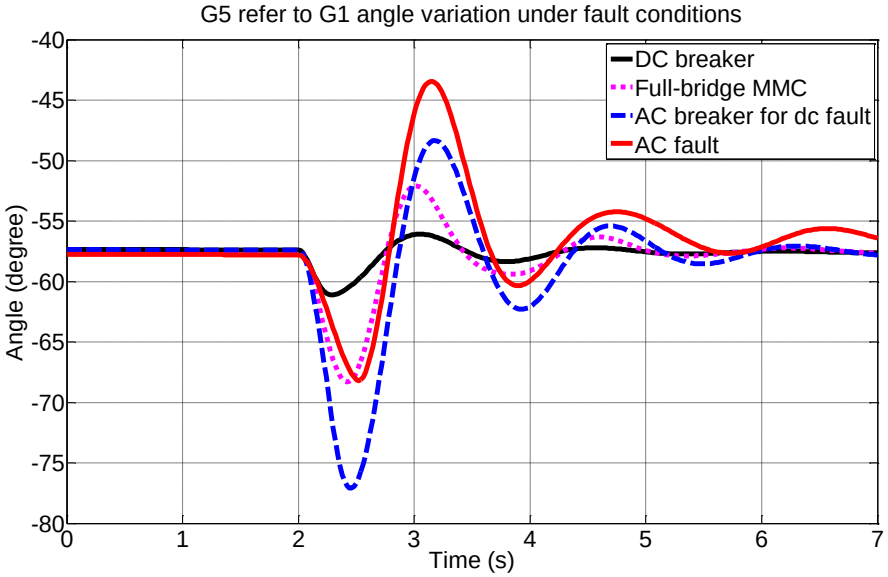


Figure 9-15. Power angle variations between G5 and G1 under fault conditions.

Shown in Figure 9-16 is the model built in MATLAB Simulink to emulate the power transfer capability loss and equivalent ac fault, named as PFE in this dissertation. The power source model can output the demand active and reactive powers by changing the output currents based on the terminal voltages. The power transfer loss can be emulated by changing the power source references to zero. The equivalent ac fault can be emulated by closing the breaker.

The PFEs are connected into the three-area system by replacing the original HVDC stations with PFEs, as shown in Figure 9-17. By using PFEs, the impacts of power transfer capability loss and equivalent ac faults on the connected ac system can be evaluated separately.

Figure 9-18 shows the power angle comparison of the dc fault protection scheme 1 and equivalent PFE cases. The 0.05 s power transfer loss and 0 s equivalent ac fault are implemented in the PFEs. The difference of the two power-angle peak values is smaller than 0.5°, which indicates that the PFE model can emulate the dc fault impact on ac system with protection scheme 1.

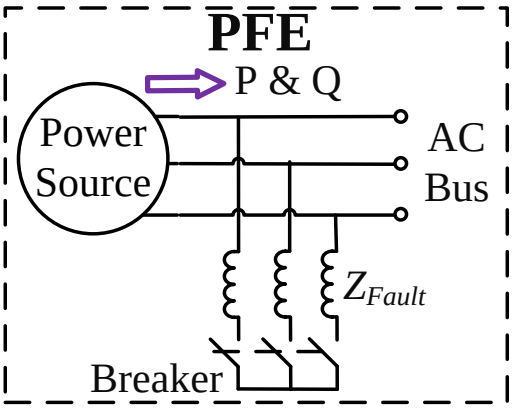


Figure 9-16. Power transfer capability loss and equivalent fault emulator.

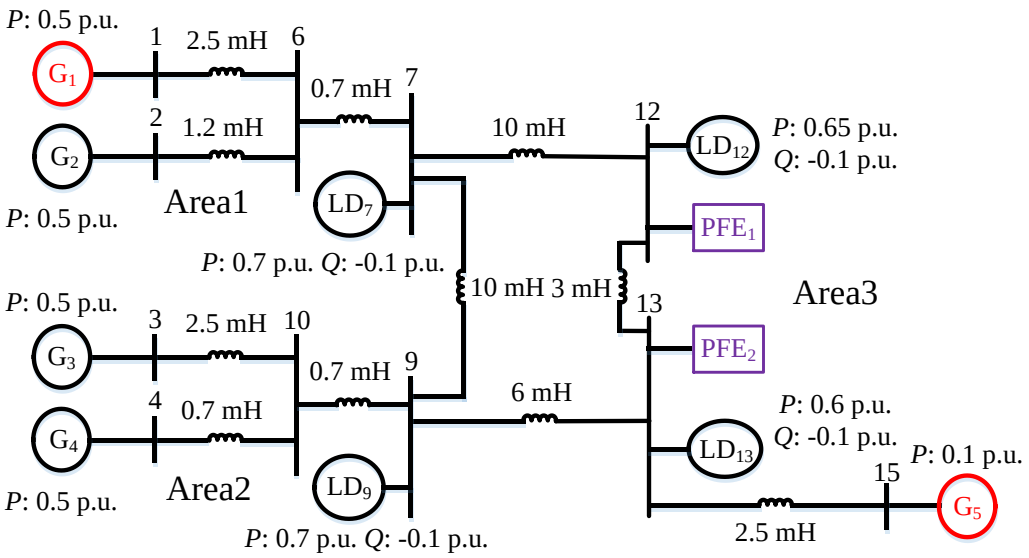


Figure 9-17. Three-area system with PFEs emulating the power transfer capability losses and equivalent ac faults.

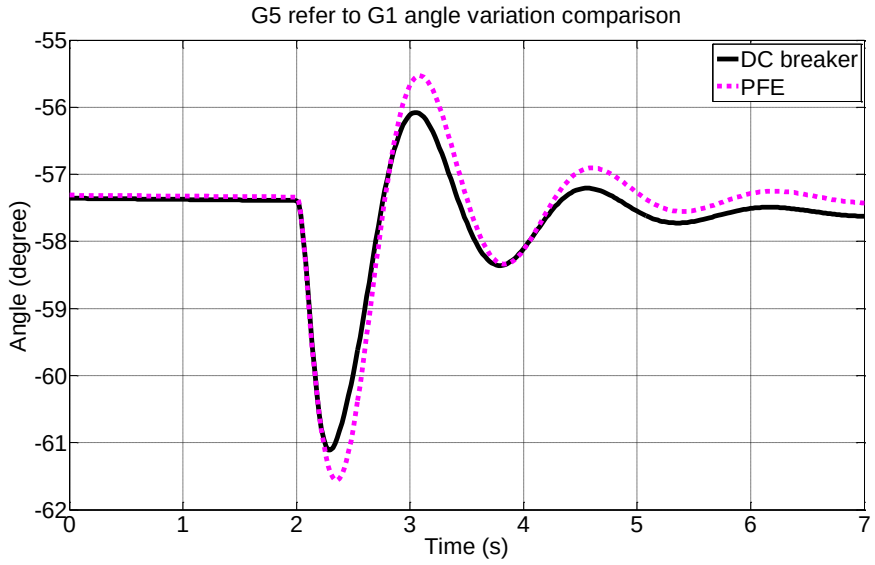


Figure 9-18. Power angle comparison of 2ms dc breaker and equivalent PFE cases.

Figure 9-19 shows the power angle comparison of the dc fault protection scheme 2 and equivalent PFE cases. The 0.15 s power transfer loss and 0.02 s equivalent ac fault are implemented in the PFEs. The difference of the two power-angle peak values is smaller than 0.5°, which indicates that the PFE model can emulate the dc fault impact on ac system with protection scheme 2. The power transfer capability loss and equivalent ac faults are also implemented individually to evaluate their impacts on the ac system transient stability separately, as shown in Figure 9-19. The impact of power transfer capability loss on the power angle variation is close to that of the equivalent PFE case. The equivalent ac fault impact on the power angle variation is small.

Figure 9-20 shows the power angle comparison of the dc fault protection scheme 3 and equivalent PFE cases. The 0.4 s power transfer loss and 0.1 s equivalent ac fault are implemented in the PFEs. The difference of the two power-angle peak values is small, which indicates that the PFE model can emulate the dc fault impact on ac system with protection scheme 3. The power transfer capability loss and equivalent ac faults are also implemented individually to evaluate their impacts on the ac system transient stability separately, as shown in Figure 9-20. The impact of power transfer capability loss on the power angle variation is close to that of the equivalent PFE case. The equivalent ac fault impact on the power angle variation is small.

Figure 9-21 shows the power angle comparison of the equivalent ac fault and zero impedance ac fault related to the dc fault protection scheme 3. The power angle variation is several times larger if the fault impedance is not implemented. However, according to the comparison of equivalent PFE and zero impedance PFE, the ac fault still contributes little to the angle variation even if the fault impedance is not implemented.

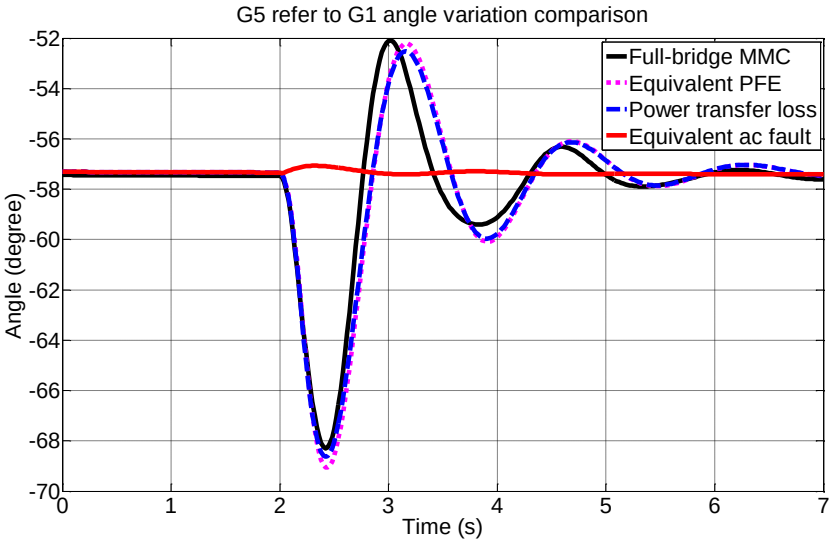


Figure 9-19. Power angle comparison of full-bridge MMC, equivalent PFE, power transfer loss, and equivalent ac fault cases.

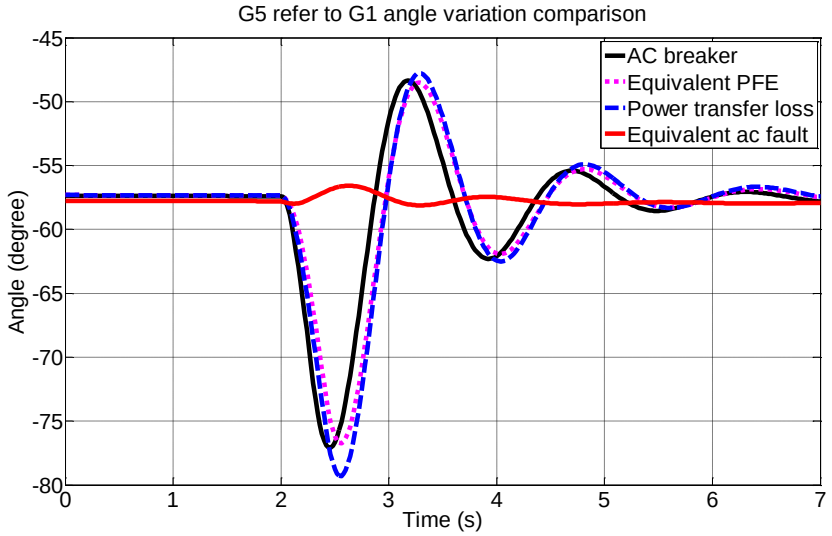


Figure 9-20. Power angle comparison of 0.1s ac breaker, equivalent PFE, power transfer loss, and equivalent ac fault cases.

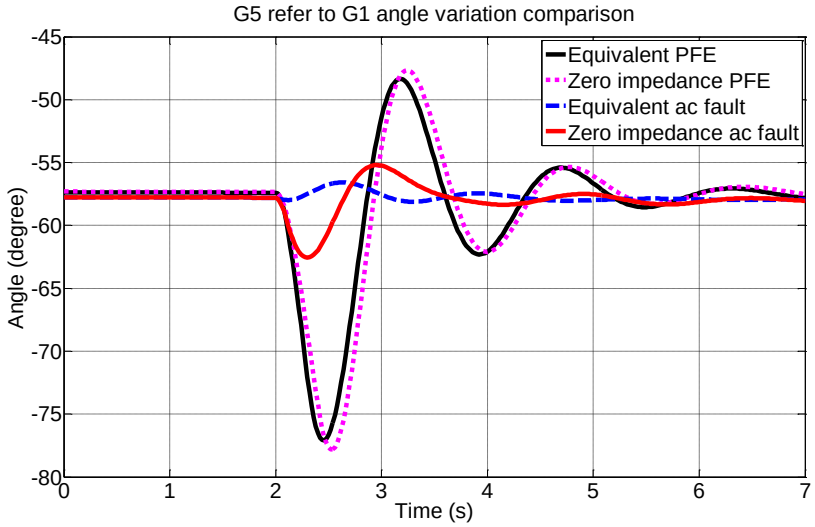


Figure 9-21. Power angle comparison of equivalent PFE, zero impedance PFE, equivalent ac fault, and zero impedance ac fault cases related to 0.1s ac breaker protection.

According to the simulation results, the PFE model is verified to emulate the dc fault impact on ac system with the three protection schemes. The dc fault impact on ac system stability mainly comes from the power transfer capability loss. The impact of equivalent ac faults on ac system stability is insignificant. The VSC filter impedance weakens the equivalent ac fault impact on ac system stability, but the influence is not significant in the defined system scenarios.

9.4 Conclusion

Based on the analysis of the dc fault performances under different HVDC converter topologies, this paper investigates the dc and ac grid characteristics under fault conditions and the dc fault impact on connected ac system. From the simulation results, the following conclusions can be drawn:

1) For point-to-point transmission case, both ac and dc transmissions lose the power transfer capability under zero impedance three-phase short-circuit fault and zero resistance dc fault conditions.

2) For multi-terminal transmission case, the ac fault impact decreases as the distance from the fault location increases, but the dc fault impact is significant within the whole dc grid. Under the zero impedance three-phase short-circuit fault condition, the ac grid can still maintain certain power transfer capability for the buses far away from the fault. However, the dc grid completely loses the power transfer capability under a zero resistance short-circuit fault. A dc fault also creates an equivalent three-phase short-circuit fault on the ac side of each HVDC converter.

3) During dc fault, the connected ac system suffers both the MTDC power transfer capability loss and the equivalent ac faults. The impact of equivalent ac faults depends on the HVDC converter filter impedances.

4) The dc fault impact on connected ac system can be small if fast dc breakers or full-bridge MMCs are implemented. The fast dc breaker can even make the impact smaller than the equivalent ac case. Though the dc fault impact on ac system is large if ac breakers are employed to deal with the dc fault, the system is still transient stable for the evaluated system in this dissertation. The HVDC converter filters weaken the equivalent multiple ac faults impact on ac system, and the impact of equivalent multiple ac faults on the connected ac system is small under the defined system scenarios.

Though the results are based on the defined system scenarios, the conclusion can be a reference for the ac grid and dc grid evaluation by considering fault conditions.

10 Conclusion and Recommended Future Work

This chapter summarizes the work that has been done in this dissertation and provides some recommendations for future work in this area.

10.1 Conclusion

A power electronics converter interfaced power system emulation platform has been developed in this dissertation. The key issues involving transmission line emulation, hybrid emulation with the HTB and RTDS, and flexible MMC test-bed have been investigated. The conclusions can be drawn as follows:

- Transmission line emulation

  (1) Algorithms to solve different transmission line models, transmission lines with integrated compensation devices, and transmission lines under fault conditions are proposed respectively to emulate the corresponding transmission line performances by calculating the terminal current references with the terminal voltage feedbacks. The proposed algorithms have been implemented in a transmission line emulator based on two VSCs and are verified by comparing experiment results with the corresponding digital simulations.

  (2) Combined transmission line models are developed to avoid the switching transient between the normal and fault states by switching the input of the integrator for current reference calculation instead of switching the current references from two different integrators.

  (3) A time-delay compensation method based on Park's transformation is proposed to

correct the follower side current reference negative sequence component phase angle shift caused by the communication time delay. Experiment results verify the effectiveness of the proposed compensation method.

(4) A negative sequence current control method is proposed and implemented in the transmission line emulator to track the negative sequence current references under unbalanced conditions. Experiment results verify the effectiveness of the proposed negative sequence control methods.

- Hybrid emulation with the HTB and RTDS

(1) A hybrid emulation interface with both voltage source ITM and current source ITM algorithms is established to guarantee the interface stability under different system conditions by selecting the appropriate algorithm based on the relationship between the equivalent impedance at the digital side and the equivalent impedance at the hardware side.

(2) A time-delay correction method based on Park's transformation is proposed and implemented in the hybrid emulation interface to enhance the emulation accuracy.

(3) Two identical interfaces are implemented in the developed hybrid emulation platform to further extend the emulation capability and flexibility. The hybrid emulation stability with two interfaces is analyzed, and the analysis result is utilized for selecting appropriate interface algorithms to ensure the hybrid emulation stability. Experiment results verify the effectiveness of developed hybrid emulation platform.

- Flexible MMC test-bed

(1) A MMC test-bed with 10 full-bridge SMs in each arm is developed with flexible

reconfiguration capabilities of topologies, switching frequencies, and passive component parameters.

(2) A cost-effective and universal pre-charge method by utilizing the MMC circuit and a low voltage dc supply is proposed to pre-charge the MMC, which has been implemented and demonstrated in the MMC test-bed.

- Hybrid ac/dc transmission and dc fault impact on ac system stability

(1) In hybrid ac/dc transmission system, the zero-sequence current induced by non-transposed coupled transmission lines flows into the dc side as a fundamental frequency current i_{60}, which can induce saturation issues on the LLC-HVDC converter transformer. Two methods, including the capacitor-commutated converter (CCC)-HVDC and band-stop LC filters, are proposed to solve the potential HVDC converter transformer saturation.

(2) Under a dc fault, the connected ac system suffers both the MTDC power transfer capability loss and the equivalent ac faults, whose impact depends on the HVDC converter filter impedances. The dc fault impact on ac system is large if ac breakers are employed to deal with the dc fault. On the contrary, a dc fault impact on connected ac system can be small if fast dc breakers or full-bridge MMCs are implemented. The fast dc breaker can even make the impact smaller than the equivalent ac case.

10.2 Recommended Future Work

As the further extension of the work in this dissertation, the following future works are recommended:

(1) Transmission line emulation

Even though the commonly utilized transmission line models have been emulated with the transmission line emulator, more complicated transmission line models can be potentially emulated in the future, like the multiple ∏ sections transmission line model, transmission line model considering phase coupling effects, unbalanced transmission line models, etc.

For transmission line emulation with combined compensation devices, variable capacitors and inductors are utilized to represent different compensation devices. In the future, high level control functions can be implemented to adjust the variable capacitors and inductors online to perform the same as FACTs, like STATCOM, SSSC, UPFC, etc.

(2) Hybrid emulation between RTDS and HTB

This dissertation implemented a switched hybrid emulation interface between the voltage source ITM and current source ITM algorithms in the hybrid emulation platform. Because the two ITM algorithms have complementary stability conditions, the hybrid emulation system maintains stability by selecting the corresponding stable interface algorithm under different scenarios. Even though the demonstrated scenarios in this dissertation are always stable by keeping the selected interface algorithm, it is potentially beneficial to switch the interface algorithm online under some extreme cases that the impedance relationship between the HTB and RTDS subsystems changes in real time.

(3) MMC test-bed

The basic functions have been implemented in the MMC test-bed, and it has been utilized to study and demonstrate the proposed pre-charge method. Because the reconfiguration flexibility and as many as 10 SMs in each arm, this platform can be used to conduct various MMC research

scenarios, like the MMC fault tolerant study, dc fault current block and fast restart with full-bridge or hybrid MMC setup, MMC modeling and stability study, etc.

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