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# A new Version of High Stability Output 12-Bit Tracking Analog to Digital Converter

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## Abstract

In this paper a 12-bit tracking analog-to-digital converter (ADC) is designed and its performance is verified. It continuously tests the analog input signal and makes correction when necessary. The resulting digital equivalent of the analog input signal is continuously updated. The least significant bit (LSB) of this converter jumps up and down to track the analog input and this causes the final output to be unstable. To overcome the problem of instability in the digital output the 12-bit tracking ADC is modified by introducing the test bit B0. The test bit is designed to have a voltage equals to that of the LSB. It always sets or resets in tracking the analog value. Using this technique the digital output B1 to B12 of the converter is maintained stable. Test and measurements are performed in the converter circuit to demonstrate the practicality of this version.

## INTRODUCTION

ADCs convert continuous physical quantities such as voltage and current, into a digital form. Closed loop ADCs such as successive approximation, dual ramp, etc use different algorithms to perform the conversion. The conversion procedure of these ADCs is periodically repeated from the beginning each time conversion done. i.e. the counter need to reset at the end of each cycle [1, 2]. On the other hand tracking ADC continuously tests the analog input signal and makes correction when necessary in such a way the history of the measurement is taken into account. The conversion is therefore

## *EDITORIAL*

faster. The counter has never to reset. The resulting digital equivalent of the analog input signal is continuously updated. One major problem is that the LSB of this converter is never stable; it always jumps up and down by one bit in tracking the analog value. The digital output permanently oscillates between two subsequent bits Bn and Bn+1 [1, 2].

In this study continuous oscillation and instability of tracking ADC output is eliminated by introducing the test bit.

### 1. EXPERIMENTAL Setup

In this paper a 12- bit tracking ADC is designed and tested. The block diagram of the converter is shown in Fig 1. The analog input Ux is compared to $U_B$. The Up/Down counter output B0 to B11 is converted to current equivalent using digital to analog converter (DAC).The resulting current is converted to voltage ($U_B$) using an operational amplifier [3, 4].

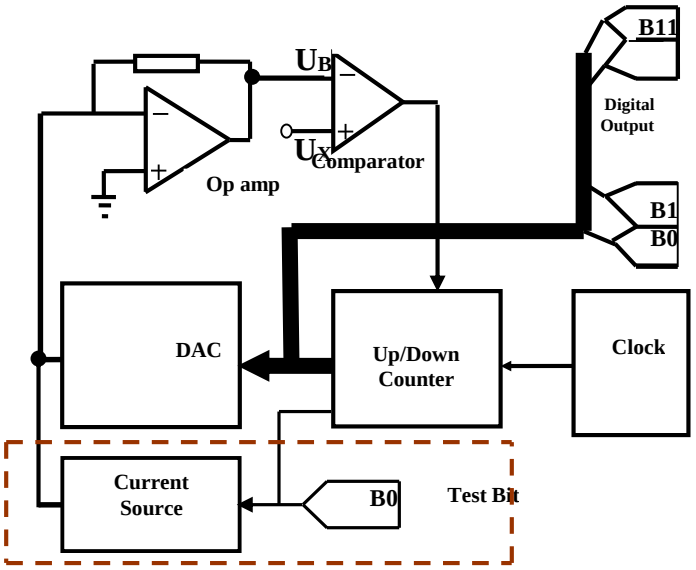
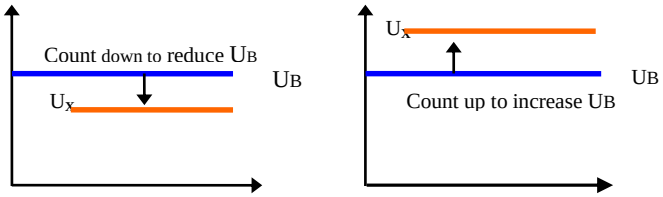



Fig.1. Block diagram of 12-bit tracking

$U_X$ is applied to the non inverting input of the comparator. If $U_B$ is smaller than $U_X$, then the U/D control input advances the counter to count up. The digital output value B0 to B11 goes higher. This value is converted to its analog equivalent $U_B$ and compared to $U_X$.

## *EDITORIAL*

Counting up proceeds as long as $U_B$ is smaller than $U_X$. Finally $U_B$ exceeds $U_X$. Then the comparator output reverses its state and the bi-directional control input advances the counters to change the counting direction from up to down. The counters output is converted to its analog equivalent $U_B$ and compared with $U_X$. The following figure shows the counting procedure of the tracking ADC [5, 6].




**(a)** **(b)**

Fig.2. Counting procedure of the tracking ADC. (a) $U_x<U_B$, (b) $U_x>U_B$.

Fig.3 represents the output behavior of the converter when the analog input signal Ux is applied. The LSB to MSB continuously updating until the final result reaches the analog input signal Ux. Then the LSB continuously changes its state in tracking the analog input.

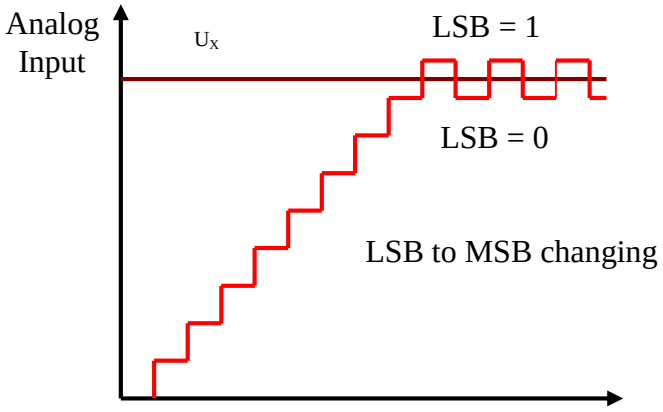



Fig.3. Behavior of LSB in Tracking ADC

### 2.1 New version of tracking ADC

In this study continuous oscillation and instability of tracking ADC output is eliminated by introducing the test bit. The modified version of tracking ADC is similar to

## *EDITORIAL*

the old type converter with some elements added to its circuitry [note the elements in doted area of Fig. 1].

Let us suppose that $U_B$ is smaller than $U_X$. This means that the binary number represented by $U_B$ is too small. It should be increased. In the first step we intend to increase it for 1 only, i.e. from N to N+1. However, the value N+1 might be too high. In order to avoid wrong decision; B1 to B12 is left unchanged for the time being. The decision to increase the number is checked by setting the test bit B0 (which brings the same voltage as that of B1; the LSB of the result).

- **Two cases can follow**

[a] If the result of conversion of the increased digital value is still too low then the least bit B0 is reset and the digital output B1 to B12 is increased for 1 by making on step more in the up direction of bi-directional counter.

[b] If the result is too big then the test bit B0 is removed and the present digital output remains.

These conditions are achieved if the DAC (AD7541) used in the converter circuit follows the weighting sequence 1, 1, 2, 4, 8,… instead of the usual 1,2,4,8,... sequence. Fig. 4 represents the waveforms of the converter upon applying the input $U_X$.

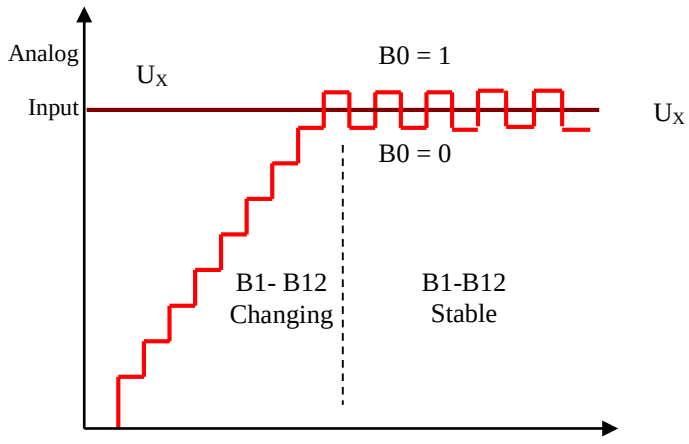



Fig.4. Waveform of Modified Tracking

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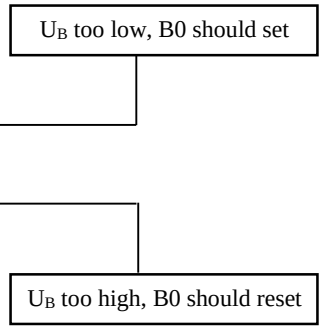
### 2.2 Stabilizing converter output using the test bit

At the start of conversion, the LSB to MSB are changing because the analog input signal Ux exceeds the initial estimate UB. At the point where the analog equivalent of the digital result reaches Ux, the test bit B0 jumps up and down to track Ux while B1 to B12 remain stable.

The test bit behavior is explained with reference to Table 1. The analog value of the test bit is assumed to be 1 V. Let us suppose Ux equals 3.2V and the analog equivalent UB of the binary number B1 to B12 is zero. Therefore UB should be increased. The bi-directional counter starts to count up.

. The behavior of the test bitTable 1

| Step | $U_B$ (V) | $B_3$ | $B_2$ | $B_1$ | $B_0$ |
|---|---|---|---|---|---|
| 1 | 0 | 0 | 0 | 0 | 0 |
| 2 | 1 | 0 | 0 | 0 | 1 |
| 3 | 1 | 0 | 0 | 1 | 0 |
| 4 | 2 | 0 | 0 | 1 | 1 |
| 5 | 2 | 0 | 1 | 0 | 0 |
| 6 | 3 | 0 | 1 | 0 | 1 |
| 7 | 3 | 0 | 1 | 1 | 0 |
| 8 | 4 | 0 | 1 | 1 | 1 |
| 9 | 4 | 1 | 0 | 0 | 0 |
| 10 | 5 | 1 | 0 | 0 | 1 |




To avoid wrong decision the test bit is set. This is shown in step 2. The corresponding analog equivalent UB (1V) is too small. In step3 B0 is reset and B1 to B12 is increased for one step up. In this case UB becomes 1V. It is too small and should be increased.

## *EDITORIAL*

Following this counting sequence it becomes clear that in step7 UB equals 3V. It should be increased. In step8 B0 is set and the corresponding UB is 4V. i.e. the result is too big therefore B0 should be removed and the binary number B1 to B12 remains. The test bit B0 jumps up and down by one bit in tracking the analog input Ux while the binary patterns B1 to B12 are stable.

The test bit B0 shown in Fig.5 controls the current source. Current source circuit provides the constant current I. This current flows either through the transistor Q1 when B0 is higher than $U_{REF}$ or through the transistor $Q_2$ when $B_0$ is smaller than $U_{REF}$. The current I flows through the small value resistor $R_1$. The resistor $R_2$ is much bigger than $R_1$ and has no influence on the current. The voltage drop $U_0$ appears at the collector of the transistor $Q_1$ when it conducts. When the test bit $B_0$ is set the voltage $U_0$ should cause the current which equivalent to one bit through $R_2$ into the summing point at the inverting input of the operational amplifier.

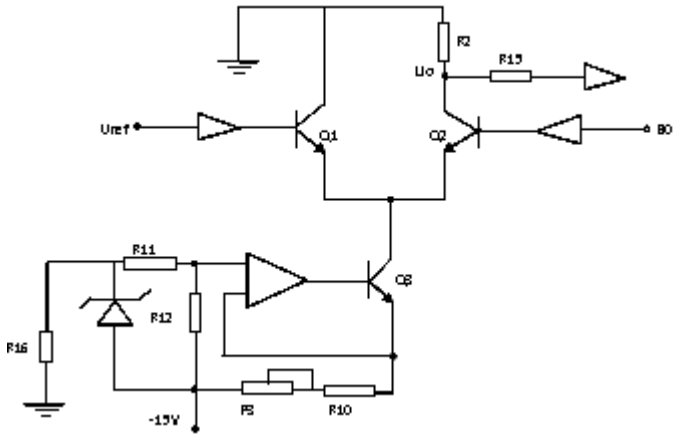



Fig.5. The test bit circuitry

**2. MEA**

A preliminary test is carried out in the converter circuit. The test bit circuitry is disconnected from the modified 12-bit tracking circuit by removing the elements in doted area of Fig. 1. The DAC output that ramps up to whatever level the analog input signal is at, output the binary number corresponding to that level, and starts over again.

## *EDITORIAL*

Plotted over time, it looks like the ramp signal shown in Fig.6. This indicates that, the converter circuit functioned properly [7, 8].

A high resolution adjustable voltage source is used for selecting the analog input signal $U_X$. At the beginning of measurement, $U_X$ is adjusted to it is minimum value. The voltage level is slightly increased until the code word at LSB changed. This indicates the transition occurrence between adjacent quantizing intervals.

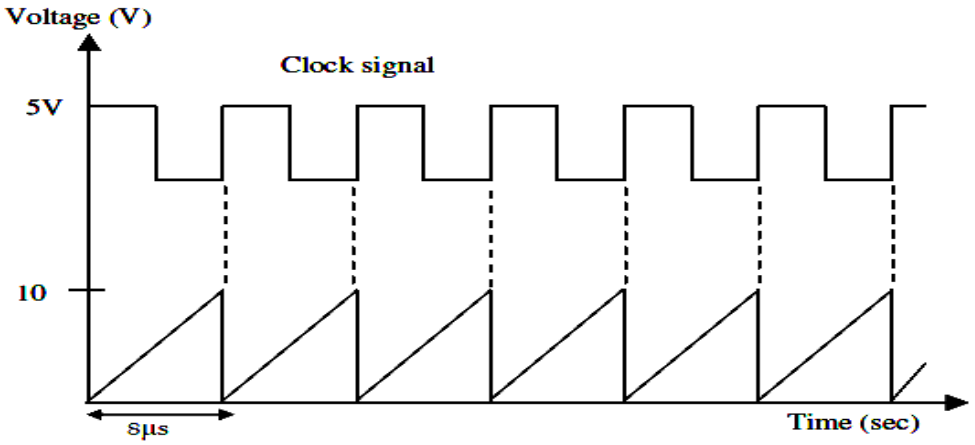



Fig.6. Ramp signal observed at DAC output

The lea jumps as long as Ux changed. The waveforms observed are shown in Fig. 7. Other converter bits follow the same sequence.. This indicates that the circuit truly behaves as the original version of tracking converter.

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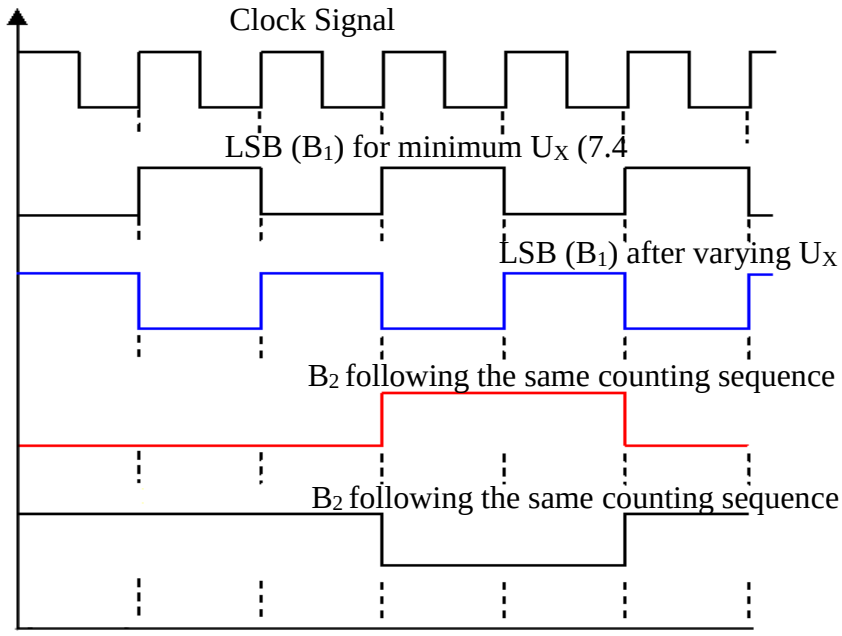


Fig.7. Schematic diagram of A 12-bit modified tracking

Permanent oscillation on the output of the tracking ADC is eliminated by connecting the test bit circuitry (Fig. 1). It adds the current from the current source to the summing point of the operational amplifier. The test bit $B_0$ jumps permanently when Ux is varied. The LSB to MSB remained stable. Figure 8 represents the LSB behavior of modified tracking converter when Ux varies. The LSB changed its state whenever the analog input Ux crosses the threshold voltage, i.e. from 1 to 0 or vice versa.

The LSB B1 of the modified converter is used to recover the conversion of the analog input signal Ux to its digital equivalent. This is done by slightly increasing Ux until LSB changes its state. The corresponding digital output $B_1$ to $B_{12}$ are obtained. The test is repeated for 4096 steps. The transfer characteristic of the converter is obtained by plotting the analog input versus the digital output.Table1 represents a sample of the data obtained and Fig. 8 shows the corresponding input output relationship.

## *EDITORIAL*

Table1. A sample of analog in Ux versus the binary output

| Ux (V) | B1 | B2 | B3 | B4 | B5 | B6 | B7 | B8 | B9 | B10 | B11 | B12 | Decimal Equivalent | Residues (V) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0.0074 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 6 | -0.0003 |
| 0.0154 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 42 | 0.0005 |
| 0.0988 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 82 | 0.0001 |
| 0.1975 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 164 | 0.0002 |
| 0.3911 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 326 | 0.0006 |
| 0.7810 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 656 | 0.0005 |
| 1.4785 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 1232 | -0.0004 |
| 2.7609 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 2300 | 0.0004 |
| 3.6003 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 3000 | -0.0002 |
| 4.8008 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 4000 | 0.0003 |
| 4.9081 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 4090 | 0.0004 |

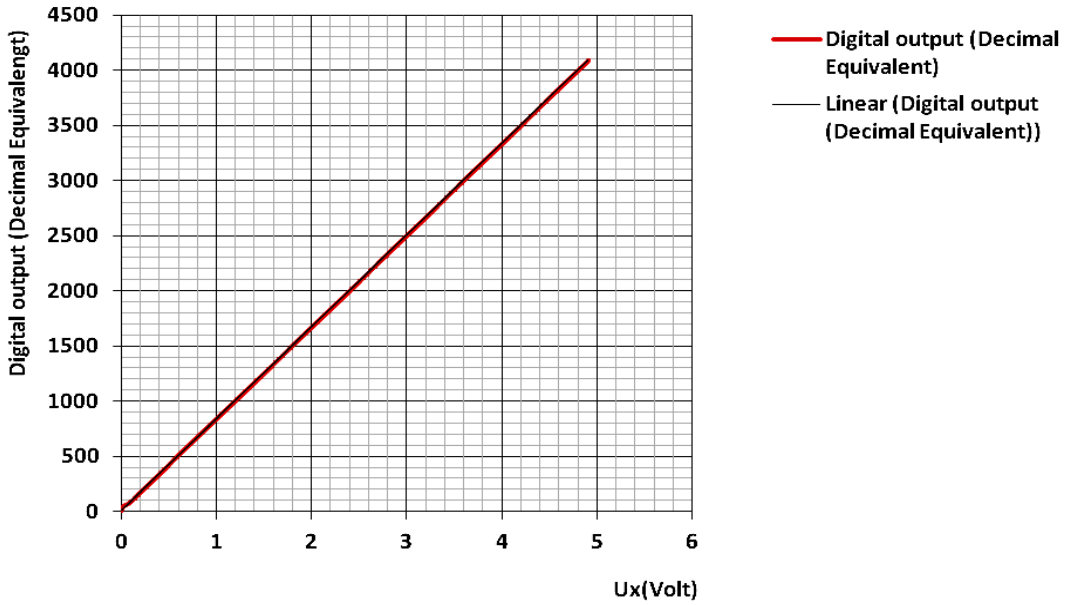


Fig. 8. A Sample result of the input output relationship of the modified converter

The deviation of the measured results from the ideal values represents a straight line. Therefore the residuals are obtained using the best linear fit. The deviations are shown in Table 1 and the relationship between the residue and the binary outputs is shown in Fig. 9.

*EDITORIAL*

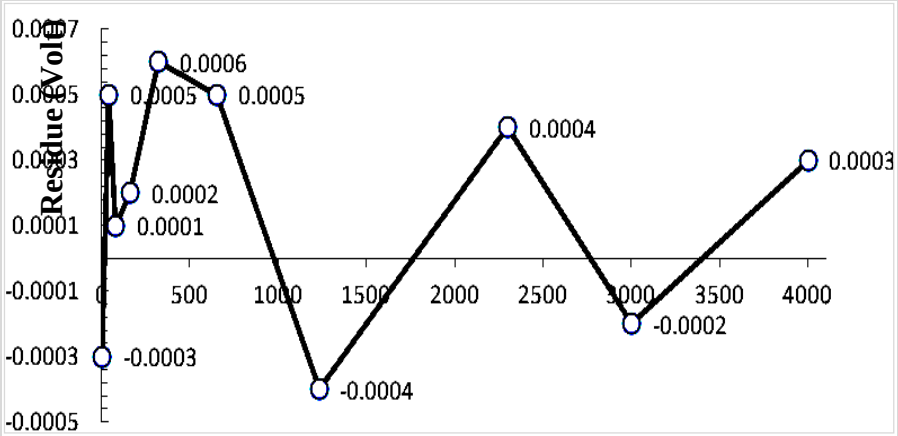


Fig. 9. A sample plot of residue against the converter output

## CONCLUSION

This paper presents the principle of the tracking analog to digital converter. The problem of permanent oscillation in LSB of this converter is solved by introducing the test bit. A modification in the convertor circuit is introduced. The DAC output pattern of the new converter circuit is modified to follow the sequence 1, 1, 2, 4, 8,…. instead of the usual sequence 1, 2,4,8,….. .The converter resolution can be enhanced by further use of U/D counters. Converter speed could be improved by using high speed operational amplifiers. The input /output relationships of the converter represent a straight line, therefore the best linear fit is made to determine the deviation of the measured results from the ideal values. One difficulty associated with the qualitative testing of the converter is the large number of samples handled. The input samples required to be converted to digital output ranges from 0 to $2^{12}$. The converter has a wide range of measuring frequencies. The optimum measuring frequency is found as 125 k Hz. The conversion time of the modified converter is 16.3 µSec which is in good agreement with those cited in the state of art

*EDITORIAL*

## REFERENCES

N. Balabanian, B. Carlson, Digital logic Design Principles, 2001.

P. Saul, J. Jenkins, 10-bit Monolithic Tracking ADC. IEEE International, Solid State Conference, Digest of Technical Papers, Volume XXI, 1978.

L. Thomas, F. Loyel, Digital Fundamentals, 2005.

Horowitz and Hill. The Art of Electronics, JUL 1999.

Y. Han and B. Jalali, Continuous Time-Stretched ADC Array Implemented Using Virtual Time Gating. IEEE, Fundamental Theory and Applications, Volume52, Issue 8, AUG 2005.

S.B. Kaplan, S.V. Rylov, P. D. Bradley, Real Time Digital Error correction for Flash ADC, Application Superconductivity, IEEE Transaction on; Volume 1, Issue 2, Part3, JUN 1997.

S. Cha and et al, Digitally Controlled Phase Locked Loop with Tracking Analog to Digital

Converter, IEEE, Asian Solid - State Circuits Conference, 2005.

T. H. Tsai, P. J. Hurst, S. H. Lewis, Band Width Mismatch and Its

Correction in Time Interleaved ADCs IEEE Circuits and Systems

II, Volume3, Issue 10, Oct 2006.

# *EDITORIAL*


## الملخص

في هذا البحث تم تصميم دائرة المبدل التماثلي الرقمي التابع ذو البتات الاثنتي عشر للقيام بعملية تبديل الاشارات التماثلية إلى قيم رقمية . ونسبة للذبذبة التي تحث في القيم الرقمية عند أوجه خروج هذا المبدل تمت تعديل دائرته بإضافة دائرة إلكترونية مبسطة . سميت هذه الدائرة بدائرة اختبار البت. تقوم هذه الدائرة بإضافة التيار المناسب إلى التيار المكافئ للقيم الرقمية الناتجة عند أوجه خروج المبدل لجعل قراءتهم في حالة ثبات دائم . أمكن الحصول على التيار المكافئ للقيم للمبدل الرقمي التماثلي و المستفاد منه في عمل التغذية الخلفية.

أجريت عدة تجارب في دائرة المبدل ثم قورنت النتائج مع عدد من المبدلات المتواجدة في الاسواق فكانت متقاربة لنسبة كبيرة. ولقد امتازت دائرة المبدل التماثلي الرقمي التابع عن بقية المبدلات بسرعة التبديل ويرجع ذلك لمتابعة القيم التماثلية المراد تبديلها على الدوام دون الإبتداء من الصفر عند لحظة الإنتهاء من عملية التبديل الأولي كما هو الحال في حالة المبدلات الأخرى .