A Modified X-Torus Topology for Interconnection Network

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***Abstract*—The interconnection network is the key components for the communication. The X-Torus topology has been designed in the past. It has been found in the previous design, that the router is not being utilized to their maximum and still there is the scope for adding more links in the topology. In this paper, a new topology has been introduced, based on X-Torus topology by adding extra links with a limited degree of the 6. The performance of the topology has been analyzed using the five traffic patterns that are random, neighbor, bit complements, and hot spot traffic over the factors end to end delay, sink bandwidth and average hop count. An improvement of 62% in terms of latency and 15% in terms of throughput has been observed in the proposed topology. This modified X-Torus topology proves to be a better substitute for X-Torus topology.**

***Index Terms*— Average Hop Count; Average Latency; Average Throughput; Interconnection Networks; Traffic Patterns.**

I. INTRODUCTION

The Interconnection Networks (INs) plays an important role in the digital system. The INs are used in a wide variety of application router fabrics, massively parallel computers, Input-output connections and in designing the on-chip networks [1]. The Interconnection networks the performance depends upon 3 parameters topology, routing algorithm and flow control mechanism used [2], [3]. The interconnection networks are generally classified into regular and irregular networks. In a regular network, every node can behave as the routing element and processing element. The simplest approach of designing a regular network is to place every processing element along with the routing element and place the links between them. This will make a simple one-dimensional topology [14]. When the extreme nodes (a pair of routing element and processing element) are connected then it will form a ring topology [3]. The Two-dimensional topology is designed by placing the nodes in the forms of tiles [4]. The placement of the nodes in the form of tiles is also referred as a mesh. The main advantage of the mesh topology is the simplicity in its design [15]. The common properties associated with any regular topology are:

1. Degree: It is the total number of nodes incident on a particular node. In general, we can have two types of degrees in degree and out degree, but in our discussion, all the nodes are bidirectional we are counting the degree based on the in degree. [2], [3]
2. Diameter: It is the shortest distance between any two farthest points in the topology under consideration. [2], [3]
3. Bisection Width: It is the minimal number of links that should be removed from the graph such that the graph gets divided into two equal halves. [2], [3]
4. Edge length: It is the most desirable to have the constant edge length. The idea behind the constant edge length is that if we have long edges the time required for the traversal of the packet from the source and destination will not be the same even though they might be at the same hop distance. [2], [3]

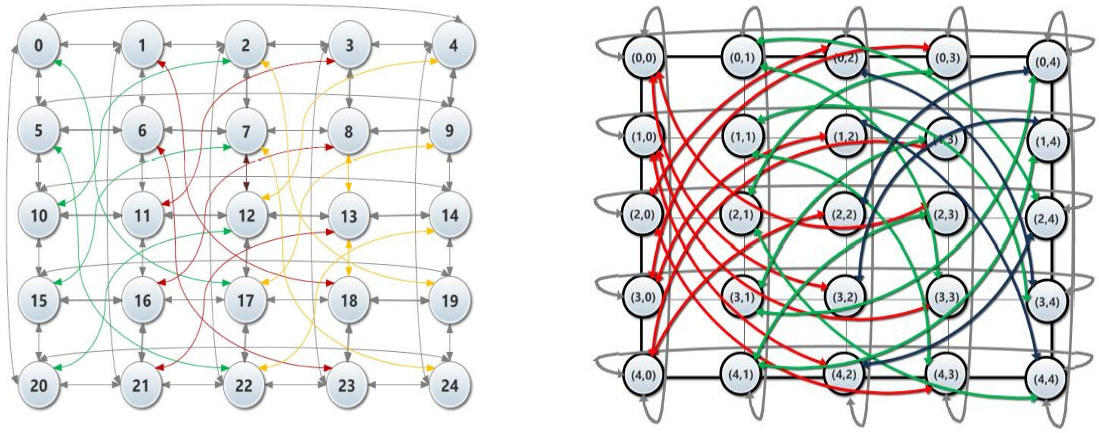
The degree of the topology described the cost of the router required for designing the topology. So, in the case of mesh if we join the extreme corners of the nodes the degree is will be 4 for all nodes. The diameter will be reduced to half and the bisection with will be doubled such type of topology is referred as the torus topology. The topology has been widely used in It has a wide area of applications in practical systems like Cray T3D, Cray T3E [1], [5], [8], Fujitsu AP3000, Ametak 2010 [1,6,8], and Intel Touchstone [1], [7], [8].

To further exploit the performance of the system a topology named X-Torus has been implemented in [1], [9]. The X-Torus topology has been described in Figure 1(a). From the figure, we can see that we have increased the degree of any node in the topology which means all the nodes will be designed using a 6-degree router but in most of the cases, this will not be used at all. The detailed mathematical formulation of the X-Torus topology has described in the [1], [9].

In this paper, our objective is to design a topology that can have a uniform degree by introducing the more extra links without increasing the degree of the router, the details of the same has been described in Section II. In Section III, we have described the test bed and experimental setup. In Section IV, detailed discussions of the results have been done and finally, the paper has been concluded in Section V.

II. MODIFIED X-TORUS TOPOLOGY

Like the X-Torus topology, the different mathematical formulation the odd number of nodes and even number of nodes will be used. The equations for the odd parity have been described by the Equation 1, 2 and 3.



(a) (b)

Figure 1: (a) X-Torus Topology, (b) Modified X-Torus Topology

$$C_x=\left\{\left\langle\left(u_a,u_b\right),\left(v_a,v_b\right)\right\rangle\middle|\left(\left(u_a=v_a\cap u_b=\left[v_b\pm1\right]_{k_x}\right)\cup\left(u_a=\left[v_a+\left\lceil\frac{k_x}{2}\right\rceil\right]_{k_x}\cap u_b=v_b+\left\lfloor\frac{k_x}{2}\right\rfloor_{k_x}\right)\right)\cap\left(\left(u_a,u_b\right),\left(v_a,v_b\right)\right)\in N_x\right\} \quad (1)$$

$$C_y=\left\{\left\langle\left(u_a,u_b\right),\left(v_a,v_b\right)\right\rangle\middle|\left(\left(u_b=v_b\cap u_a=\left[v_a\pm1\right]_{k_y}\right)\cup\left(u_b=\left[v_b+\left\lceil\frac{k_y}{2}\right\rceil\right]_{k_y}\cap u_a=v_a+\left\lfloor\frac{k_y}{2}\right\rfloor_{k_y}\right)\right)\cap\left(\left(u_a,u_b\right),\left(v_a,v_b\right)\right)\in N_y\right\} \quad (2)$$

$$C=C_x\cup C_y \quad (3)$$

Similarly, the Even parity links can be described by the equation 4, 5 and 6.

$$C_x=\left\{\left\langle\left(u_a,u_b\right),\left(v_a,v_b\right)\right\rangle\middle|\left(\left(u_a=v_a\cap u_b=\left[v_b\pm1\right]_{k_x}\right)\cup\left(u_a=\left[v_a+\left\lceil\frac{k_x}{2}\right\rceil\right]_{k_x}\cap u_b=v_b+\left\lfloor\frac{k_x}{2}\right\rfloor_{k_x}\right)\right)\cap\left(\left(u_a,u_b\right),\left(v_a,v_b\right)\right)\in N_x\right\} \quad (4)$$

$$C_y=\left\{\left\langle\left(u_a,u_b\right),\left(v_a,v_b\right)\right\rangle\middle|\left(\left(u_b=v_b\cap u_a=\left[v_a\pm1\right]_{k_y}\right)\cup\left(u_b=\left[v_b+\left\lceil\frac{k_y}{2}\right\rceil\right]_{k_y}\cap u_a=v_a+\left\lfloor\frac{k_y}{2}\right\rfloor_{k_y}\right)\right)\cap\left(\left(u_a,u_b\right),\left(v_a,v_b\right)\right)\in N_y\right\} \quad (5)$$

$$C=C_x\cup C_y \quad (6)$$

In the above equations, the v_a and v_b are the source coordinates from which the coordinates X links are to draw u_a and u_b are the coordinates of the links that are adjacent the source node in the torus topology. The Kx and Ky are the number of nodes in the *x* dimension and number of nodes in y dimension or simply we can say the number of rows and columns the existing topology. The topology generated can be described below in Figure 1 (b). The figure describes the 5X5 Mesh topology with a Modified X-Torus links that mean k_x and k_y are five. To understand the in detail, let us consider a Figure 1 (b), with the coordinate representation. Now considering:

$$(v_a,v_b)=(0,0)$$
$$u_a=0$$
$$u_b=(0\pm1)_5$$
$$=(1,-1)$$
$$=\{1,4\}$$
$$u_a=(0+3)=3$$
$$u_a=(0+2)=2$$
$$C_x=\{(0,1),(0,4),(3,2)\}$$
$$u_b=0$$
$$u_b=(0\pm1)_5$$
$$=\{1,4\}$$
$$u_a=(0+3)=3$$
$$u_a=(0+2)=2$$
$$C_y=\{(0,1),(0,4),(3,2)\}$$
$$C=C_x\cup C_y$$
$$=\{(0,1),(0,4),(3,2),(1,0),(4,0),(2,3)\}$$

A node with coordinate (0,0) connected with:

$$\{(0,1),(0,4),(3,2),(1,0),(4,0),(2,3)\}$$

III. Test Bed and Experimental Setup

To test the performance of the designed topology the simulation was performed on the Windows 10 on the OMNET++ simulator, a component-based C++ simulation library and framework which is both extensible and modular and is primarily used for building network simulator based on

the Eclipse IDE [10], [11]. The System was equipped with intel® Core™ i3 CPU M330@2.13 GHZ with 4.00 GB and 2.99GB usable. The various parameters used for the testing the mesh, torus, X-Torus and Modified X-Torus is provided in Table 1 below.

Table 1
Describing the Various Parameters Used for Simulation

Sno.	Parameter Name	Value
1	Row	5
2	Columns	5
3	Routing Algorithm	Table based Shortest Path (Static)
4	Simulation Time	0.5 s
5	Channel Data Rate	1 Gbps
6	Link Delay	0.1 ms
7	Traffic patterns	Random, Neighbor, tornado, bit complements and Hot Spot

The Traffic patterns used can be defined by the in terms of the mathematical equations based on the source id [12].

1. Random Uniform Traffic: It is the randomly distributed uniform traffic generated by the Equation 7.

$$Dstid = \text{int}\, uniform(0, N-1) \tag{7}$$

Intuniform is the function, predefined in omnet and N is the total number of nodes.[12]

2. Bit Complement Traffic: The Bit complement traffic is described by Equation 8.

$$Dstid = (N-1) - Myaddress \tag{8}$$

Here N is the number of nodes and myaddress is the address of the source node.[12]

3. Neighbor address: It is a traffic which sends the traffic to the adjacent nodes. The simplest representation can be described by the Equation 9.

$$Dstid = (Myaddress + 1)\%N \tag{9}$$

Here N is the number of nodes in a row or columns.

4. Tornado Traffic: This traffic is designed to send the traffic to half of the distance this can be described by the Equation 10.

$$Dstid = \left(\frac{N}{2} + (Myaddress\%N) \right)\%N \tag{10}$$

Here N is the number of rows or columns.

5. Hot Spot traffic: In hot spot traffic, the fixed percent of nodes are sending to specific nodes the by creating a hot spot effect.

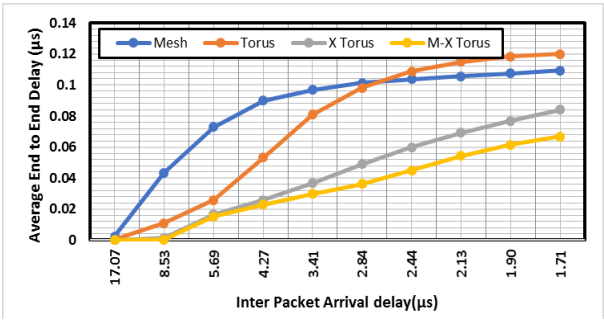
IV. Results and Discussion

The performance evaluation of the topology is done on the basis of an average end to end latency, average throughput, and average hop count.

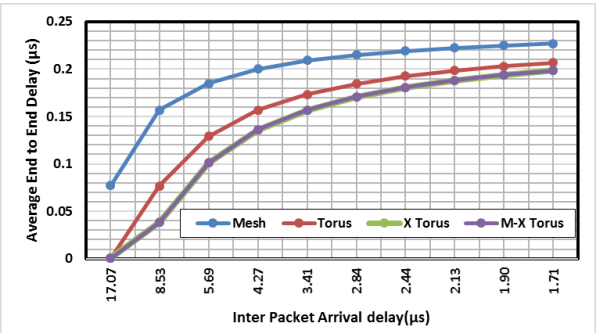
A. Average End to End latency

The latency is defined as the total time taken by the packet from the source to sink. [13] The End to End latency is recorded by using the timestamps mentioned on the packet when it is generated at the source. When the packet reaches the destination the timestamp of packet arrival at the sink is recorded. The difference between the two timestamps is recorded. The same process is recorded for each packet that reaches the destination and finally, the average value is calculated. The graphs for the end to end latency for various traffics are described in Figure 2.

From the graph, it is clear that the MX-Torus is having lowest latency. The MX-Torus gave performance improvement of 20% at the inter-packet arrival delay of 1.71µs. In the graph described in Figure 2(b), we can see that the trend shown by both the X-Torus topology and MX-Torus topology is almost the same. So we can the extra links in the MX-Torus could not exploit the advantage. In the case of neighbor traffic, all the topologies are giving the same latency as all sink nodes are in single hop distance. In the case of tornado traffic, MX-Torus traffic has given the best performance, this performance was better at lower loads than on higher loads. This improvement was about 62%. Again, in the case of hotspot traffic the MX-Torus topology has shown the improvement and this improvement increases as the load increases, this has identified that the most improvement is found at the 17.1 inter-packet arrival delay and improvement was about 20%.



(a)



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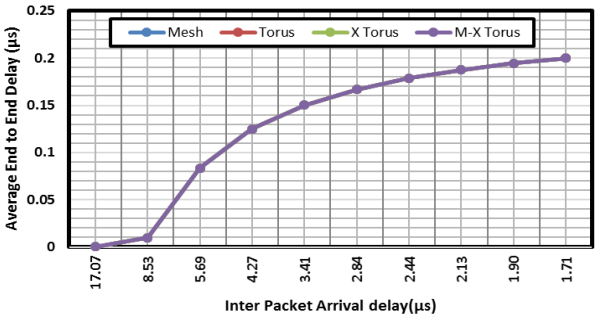

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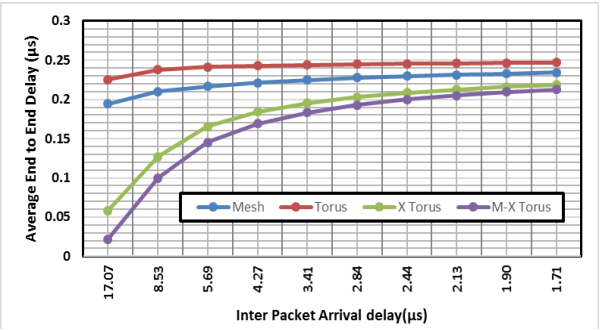

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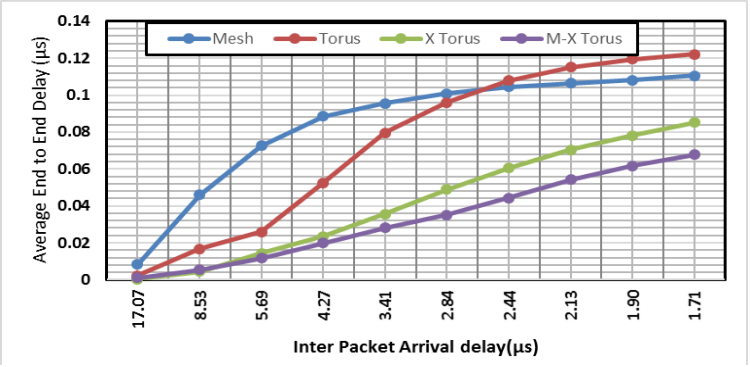


(e)

Figure 2: End to End Latency on (a) Uniform Traffic, (b) Bit Complement Traffic, (c) Neighbor Traffic, (d) Tornado Traffic, (e) Hot Spot Traffic

B. Average Throughput

Throughput is defined as the maximum data transferred per unit of time. The packets received by the particular node are recorded for the mentioned simulation time. This will give us the estimate of a total number of bytes per second received at the particular node. Then we take the average of a total number of bytes per second received by each node. The comparison of the throughput is done on the various traffic patterns and has been presented in Figure 3.

In the case of the uniform traffic, MX-Torus has given maximum throughput in comparison to the other topologies under consideration as shown in Figure 3(a). The MX-Torus topology has given an improvement of 15% over the X-Torus topology at the inter-packet arrival delay of 1.71 µs. In the case of Bit complement traffic, the MX-Torus and the X-Torus have given the same throughput so that the links provided in MX-Torus cannot exploit the needs of the bit complement traffic. But still is competitive with the X-Torus topology. The same has been described in Figure 3(b).

In the case of the Neighbor traffic, all the topologies are giving the same performance this is due to the fact that the neighbor is at the distance of single hop so the graph seems to be similar for each of the topology. The throughput of the MX-Torus topology is better in comparison to the other topologies. The throughput was almost same at a lower value of loads, but significantly increases with the increase in the load it has been found that performance was having the improvement of 13%.

C. Average Hop Count

The average hop count is defined as the average number of links packet has to traverse to reach from the source to destination. Ideally, the average hop count is the minimum average shortest path between all pairs of nodes as the source and destination. But here in the analysis, traffic has given different average hop counts this is due to the fact a particular traffic will exploit specific source and destinations.

From the Figure 4(a), we can see that the average hop count of the MX-Torus topology is having lowest average hop count at lower load factor. From the Figure 4(b), it can be observed the average hop count of the MX-Torus is slightly less than that it competitor X-Torus topology. Average hop count in case of neighbor traffic is the almost the same for the torus, X-Torus, and MX-Torus topology, but from the Figure 4(c), the average hop count of the mesh is slightly higher than that of a torus-based topologies this is due to the effect of the equation used for the neighbor traffic. From the Figure 4(d) and (e) we can see that the average hop count of the M-X topology is better in comparison to other topologies.

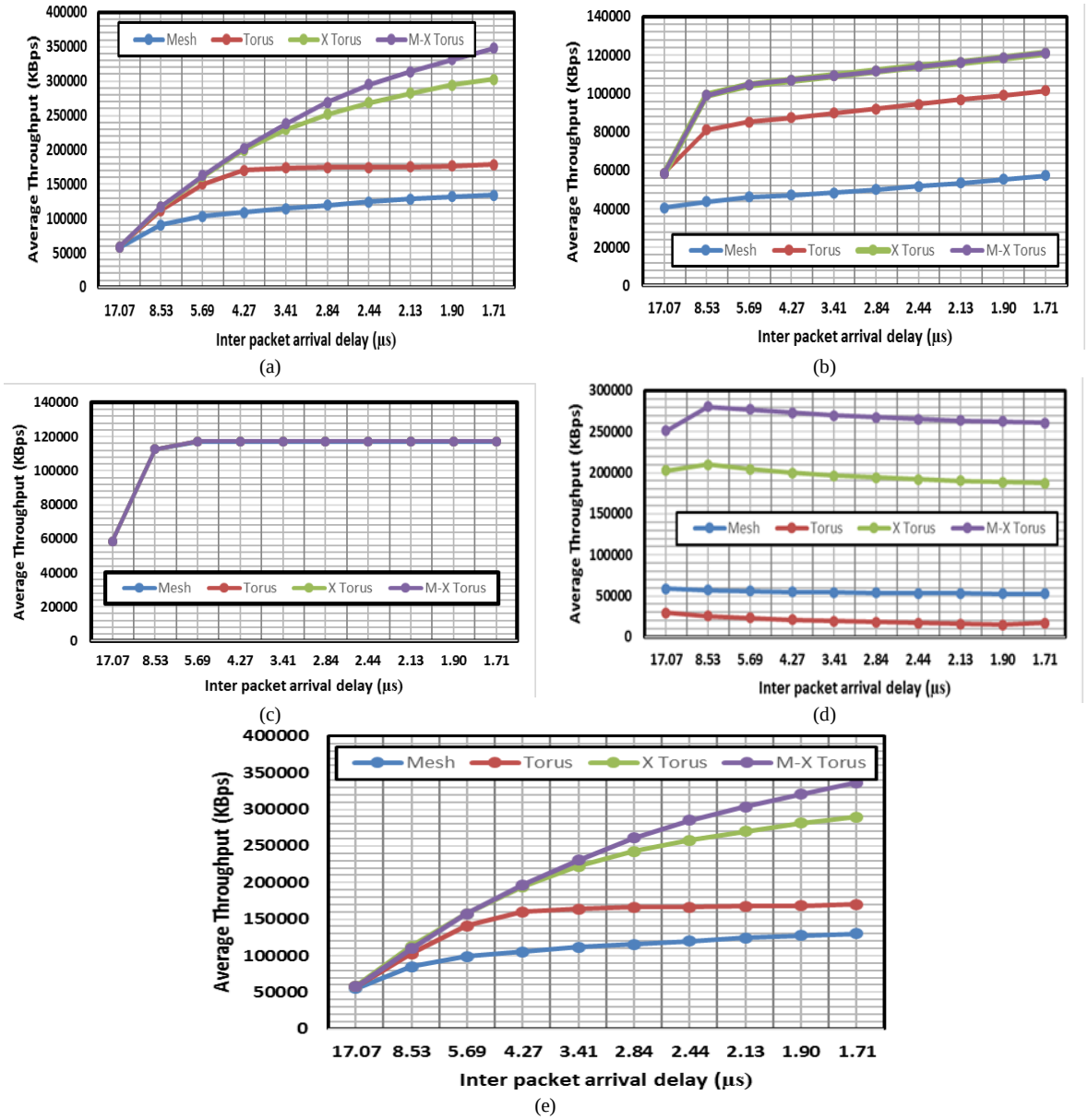
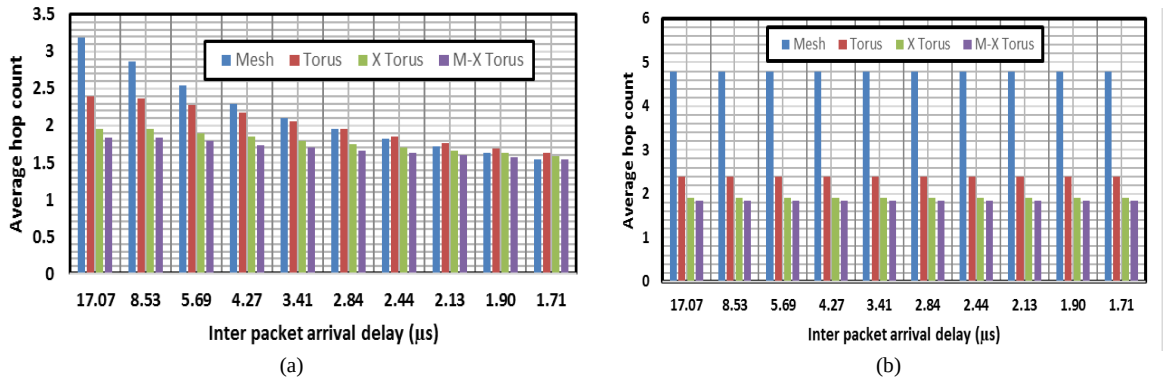


Figure 3: Average Throughput on (a) Uniform Traffic, (b) Bit Complement Traffic, (c) Neighbor Traffic, (d) Tornado Traffic, (e) Hot Spot Traffic



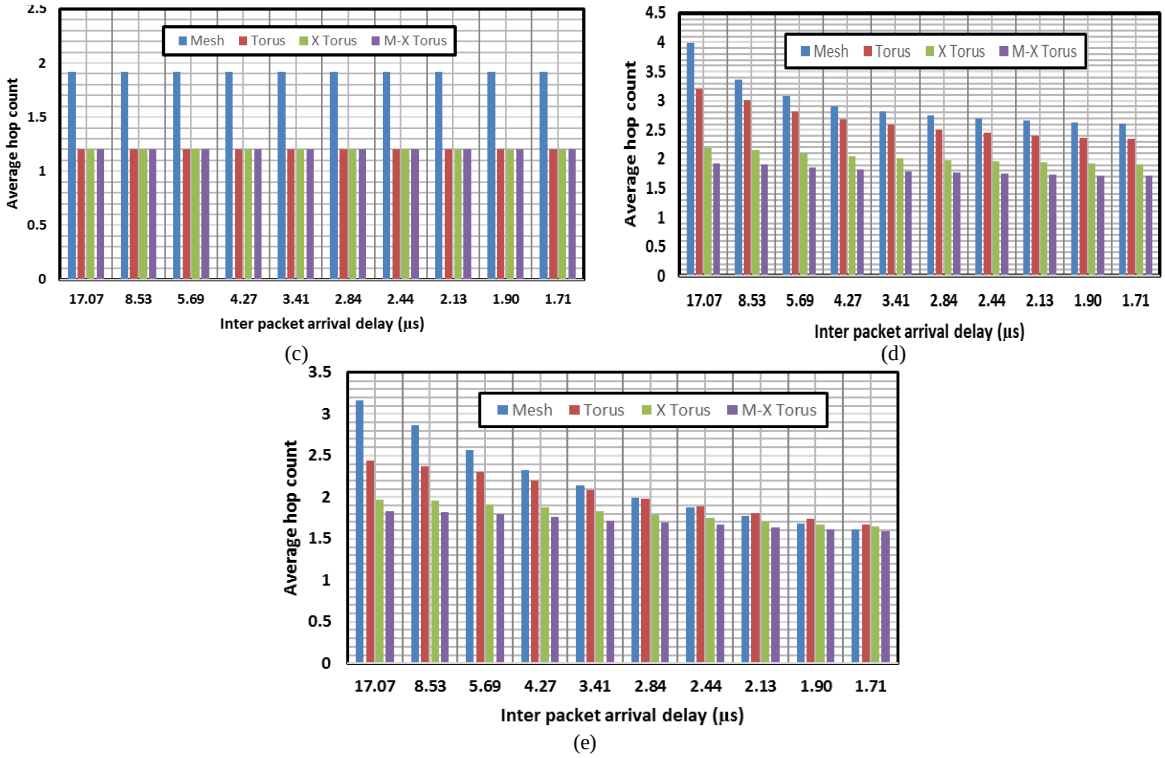


Figure 4: Average Hop Count on (a) Uniform Traffic, (b) Bit Complement Traffic, (c) Neighbor Traffic, (d) Tornado Traffic, (e) Hot Spot Traffic

V. CONCLUSION

From the analysis of the results, it can be understood that the performance of the MX-Torus topology is either better or equivalent to the X-Torus topology. This can also be concluded that the topology is best suited for the applications which have the traffic of the type uniform, tornado or hotspots. For the other traffic also the performance was same, so we can say that the MX-Torus topology is a better substitute in comparison X-Torus topology when performance is the top priority. The MX-Torus has gained the maximum improvement of 62% in the terms of latency and 15% in terms of throughput.

REFERENCES

[1] Vaish, R. and Shrivastava, U., 2012. On a deadlock and performance analysis of ALBR and DAR algorithm on X-Torus topology by optimal utilization of Cross Links and minimal lookups. The Journal of Supercomputing, 59(3), pp.1252-1288.

[2] Duato, J., Yalamanchili, S. and Ni, L.M., 2003. Interconnection networks: an engineering approach. Morgan Kaufmann.

[3] Dally, W.J. and Towles, B.P., 2004. Principles and practices of interconnection networks. Elsevier.

[4] Dally, W.J. and Towles, B., 2001. Route packets, not wires: On-chip interconnection networks. In Design Automation Conference, 2001. Proceedings (pp. 684-689). IEEE.

[5] Anderson, E., Brooks, J., Grassl, C. and Scott, S., 1997, November. Performance of the Cray T3E multiprocessor. In Proceedings of the 1997 ACM/IEEE conference on Supercomputing (pp. 1-17). ACM.

[6] Seitz, C.L., Athas, W.C., Flaig, C.M., Martin, A.J., Seizovic, J., Steele, C.S. and Su, W.K., 1988, January. The architecture and programming of the Ametek series 2010 multicomputer. In Proceedings of the third conference on Hypercube concurrent computers and applications: Architecture, software, computer systems, and general issues-Volume 1 (pp. 33-37). ACM.

[7] Lillevik, S.L., 1991, April. The Touchstone 30 gigaflop DELTA prototype. In Distributed Memory Computing Conference, 1991. Proceedings., The Sixth (pp. 671-677). IEEE.

[8] Bhuyan, L.N., 1987. Special issue of interconnection networks. IEEE Computer, 20(6).

[9] Gu, H., Xie, Q., Wang, K., Zhang, J. and Li, Y., 2006, May. X-Torus: a variation of Torus topology with lower diameter and larger bisection width. In International Conference on Computational Science and Its Applications (pp. 149-157). Springer Berlin Heidelberg.

[10] Varga, A., 2001. Discrete event simulation system. In Proc. of the European Simulation Multiconference (ESM'2001).

[11] Varga, A., & Hornig, R. (2008, March). An overview of the OMNeT++ simulation environment. In Proceedings of the 1st international conference on Simulation tools and techniques for communications, networks and systems & workshops (p. 60). ICST (Institute for Computer Sciences, Social-Informatics and Telecommunications Engineering).

[12] Chauhan, D.S., 2012. Comparative analysis of Traffic Patterns on k-ary n-tree using adaptive algorithms based on Burton Normal Form. The Journal of Supercomputing, 59(2), pp.569-588.

[13] Kim, K., Lee, S.J., Lee, K. and Yoo, H.J., 2005, May. An arbitration look-ahead scheme for reducing end-to-end latency in networks on chip. In Circuits and Systems, 2005. ISCAS 2005. IEEE International Symposium on (pp. 2357-2360). IEEE.

[14] Peñaranda, R., Gómez, M.E., López, P., Gunnar Gran, E. and Skeie, T., 2017. A fault-tolerant routing strategy for k-ary n-direct s-indirect topologies based on intermediate nodes. Concurrency and Computation: Practice and Experience.

[15] MdYunus, N.A., Othman, M., MohdHanapi, Z. and Lun, K.Y., 2016. Reliability review of interconnection networks. IETE Technical Review, 33(6), pp.596-606.