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Designing Framework For The Computer Aided Design Of Silicon Carbide Jfet Circuits In Bleo Environments

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DESIGNING FRAMEWORK FOR THE COMPUTER AIDED DESIGN OF SILICON CARBIDE JFET CIRCUITS IN BLEO ENVIRONMENTS

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By

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ABSTRACT

Circuit Design and testing are two essential processes to synthesis of an efficient and reliable circuit. Real-time testing of a circuit through circuit fabrication and development is an expensive and a risky procedure whereas testing the circuit by modelling and simulating is more efficient and inexpensive.

Silicon-based semiconductors are the basic components of any modern day electronic devices, and their usage has dominated the marketplace. But these conventional CMOS devices cannot exist in an environment consisting of harsh radiation, high temperature and many other environmental conditions, such as Venus or Mars. However, 6H-SiC JFETs, which are basic logic gate integrated circuits, have significantly potential for persistent operation in these environmental conditions. On the basis of the temperature effects of 6H-SiC JFET's compared to conventional CMOS JFET's, we choose to develop the framework for a computer aided design of Silicon Carbide JFET circuits in Beyond Low Earth Orbit (BLEO) environments. Our framework will help test the modern and emerging nanotechnologies for the temperature dependence of SiC electronics and sensors in harsh environments.

Framework along with the Integrated circuit design and the simulations for the SiC electronic circuit are the desired results for this project.

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INTRODUCTION

Beyond Low Earth Orbit (BLEO) environments are very harsh environments consisting of extreme temperatures, such as Venus, which consists of high temperatures of 500˚C, and Mars consisting of temperatures -150˚C. Additionally, BLEO environments exhibit high degree of radiation, pressure and chemical reactions, making the environment extremely difficult for the proper functioning of the conventional CMOS devices.

Conventional CMOS devices in low earth orbit environments work exhibit semiconductor properties without any variations, but the similar devices in BLEO environments exhibit thermal overstress, variation in propagation delay, increase in the leakage power, dynamic power and short circuit power. Additionally, there is an increase in the device temperature, which contribute to the breaking of the die, as well as melting the material by making the CMOS device unsuitable to operate at the high temperatures. Conventional CMOS devices have been demonstrated to fail after 127 minutes of operation at 480ºC, making those devices poor candidates for long-term BLEO operations. Silicon Carbide devices, which are potentially capable for use in circuits which require to operate in the BLEO environments having high temperatures, radiations, pressure and chemical reactions. However, there only currently exists fabrication of Silicon Carbide JFETS at the

transistor level. In order for these devices to be rapidly fabricates in VLSI circuits, a computer-aided design and test framework using the device models must be developed.

In this thesis, we developed a Computer Aided design flow for Silicon Carbide JFETS, and developed and simulated a Full Adder using the Silicon Carbide Junction Field effect transistor models provided by NASA. The device was tested for temperature variations by varying the parameters of the Junction Field effect transistor which are effected by the change in temperature. The Computer Aided design flow will aid future engineers in the determination of the effect on the JFET circuit when it is subjected to the temperature variation, along with the change in parameters of oxide thickness, sheet resistance, length and the width of the JFET device.

Due to the difficulty in creating a BLEO environment on Earth, we used the Computer Aided Design tools of Virtuoso for the designing of the Full Adder circuit schematic consisting of the Silicon Carbide JFET's, Spectre for simulating the schematic by subjected the schematic to the change in the temperature, as well as the change in the temperature dependent parameters using the Spectre simulation code. Computer Aided design tool Viva is used to obtain the plots related to the simulation.

In order to demonstrate the effective of the design produced by the synthesis flow, we checked the variation in the properties of the Silicon Carbide junction field effect transistor device when subjected to the change in the temperature. Additionally, we present results from variations on changes in the parameters effected by the change in temperature, as well as other parameters, like sheet resistance, oxide thickness, length and width. We obtained the ideal operating temperatures and other operating parameters for the Silicon Carbide JFET device for each device model using the results obtained from the simulations.

SECTION 2

LITERATURE REVIEW

Since the invention of the semiconductor, there has been a significant increase in the use of semiconductors on several industrial systems like aerospace, electrical and automotive fields due to the improvement of the performance of the semiconductor device [1]. Usage of semiconductors was largely influenced by the presence of highly capable microelectronics along with the need of improving the performance of the integrated system which requires the system being operated at a temperature up to 200˚C and any frequency range [1]. The performance of the semiconductors was gradually increased by the introduction of the MOS technology as these MOS devices could produce scalability along with less power consumption. But there are some limitations of these conventional CMOS devices which are illustrated as follows: Operation of circuits based on these devices at temperatures higher than 200˚C is very difficult as these devices express self-heating when subjected to a high-power environment, which leads to power leakages in the internal components of the device since the device also possesses high temperatures at their internal junctions [1]:

a) Bandgap is the measured criteria for the devices to be operated at different temperatures. It is described as the energy difference between the valence band and the conduction band of the semiconductor. Lower the bandgap will insure lesser temperature of operation.

b) High losses due to heat dissipation and having less dielectric materials are one of the major concern for the lower temperature operation of the conventional CMOS devices.
c) The usage of cooling systems when the device is exposed to high temperatures also create an additional overhead, thereby reducing the performance of the Conventional CMOS devices.

Moreover, having additional overhead in form of long wires and more connectors is also a concern as they increase the size, weight, and complexity of these Conventional CMOS devices there by increasing possibility of failure to operate in these high temperatures [1]. The Conventional CMOS devices can be used in these high temperatures but with additional cost and weight and require thermal protection systems and shielding systems for protecting them from the high radiation, temperature, and pressures [2]. The Circuits designed for these high temperatures and pressures are more complex when compared to the normally designed circuitry to work normally. However, these complex circuits could allow conventional CMOS devices to survive for only 127 minutes on the surface of Venus at temperature of 480˚C, which is 4 times higher than the military specification for temperature of 125 ˚C, limiting the purpose of planetary mission to the surface of Venus and other planets [2]. Although Conventional CMOS devices are used in the modern-day space technology and other high radiation technology fields, the efficiency is very low along with the rate of failures increasingly high in these high temperatures and pressure when compared to the efficiency and rate of failure in the specified operating temperature and pressure [2].

Due to the limitations of conventional CMOS devices, there have been many experiments conducted on wide-bandgap semiconductors for operating at high temperatures and in a harsh environment consisting of high operating frequencies along with high operating power and high radiation [6]. These environments are experienced in many of engineering devices like aerospace

propulsion system and in planets like Venus and Mars [6]. Silicon Carbide (SiC) is one of the Semiconductors which can operate in an environment consisting of high temperatures up-to 600˚C and in the harsh environments [6]. Other materials apart from the Silicon Carbide, which are capable of functioning at the temperatures of 500 ˚C, do not exhibit the complexity of the Silicon Carbide in the form of structure and the atomic placement of the Silicon and Carbon atoms. The properties of Silicon Carbide are discussed below [2-3, 7]:

a) Silicon Carbide the higher critical electrical field than that of Si and it is made relatively thinner than any semiconductor with element of higher dielectric strength.
b) Silicon Carbide exhibits lower losses when compared to conventional CMOS devices due to its conductivity and higher doping level than the Conventional CMOS devices.
c) Operating at a higher temperature can be obtained using Silicon Carbide Semiconductor devices as they can operate at temperatures up to 600˚C.
d) SiC Devices doesn't require any cooling devices when exposed to high temperatures as in the case of Silicon. Due to which the overhead of Cooling systems can be reduced in the systems consisting of SiC Devices.
e) Silicon Carbide has a wider bandgap when compared to the conventional CMOS devices making them suitable to use in harsh environments consisting of high-power along with high-radiation and high frequency.
f) Data is accurate as there is less signal to noise interference ratio which is due to the placing of interface electronics close to the sensors (Used in aerospace propulsion system).

Due to these above properties of Silicon Carbide of having Wide bandgap, operating at higher temperature it is used in the systems exposed to the harsh environments and it helps in the reduction of cost as cooling systems used to reduce internal junction temperature can be optimized

and there is no requirement of having long wires and more connectors, thereby improving the reliability.

There are different polytypes in Silicon Carbide which are given as follows 6H-SiC, 4H-SiC, 2H-SiC, 15R-SiC, 3C-SiC, 8H-SiC and 10H-SiC [8]. Among all the polytypes 4H-SiC and 6H-SiC have higher thermal conductivity, high breakdown strength and high conductivity when compared with Silicon. Other polytypes also exhibits the similar properties but 4H-SiC and 6H-SiC are available in a bulk wafer form which makes these polytypes suitable for generating the semiconductor devices which are used in high temperature, high radiation and high frequency environments [5,6].

This presence of many polytypes for the Silicon Carbide is due the structure of the Silicon Carbide (SiC) which is formed by 4 covalently bonded carbon atoms each being at an angle of 109.4˚ with the Silicon Atom forming a tetrahedron shape [6]. The axis parallel to the normal axis (for instance y-axis) acts as the plane of rotation and forms another tetrahedron, which are the two structures a Silicon Carbide exists [9]. Coming to the formation of the structure of the silicon carbide, it can be explained by the stacking sequences called as A, B and C as shown in Figure 1 [9].

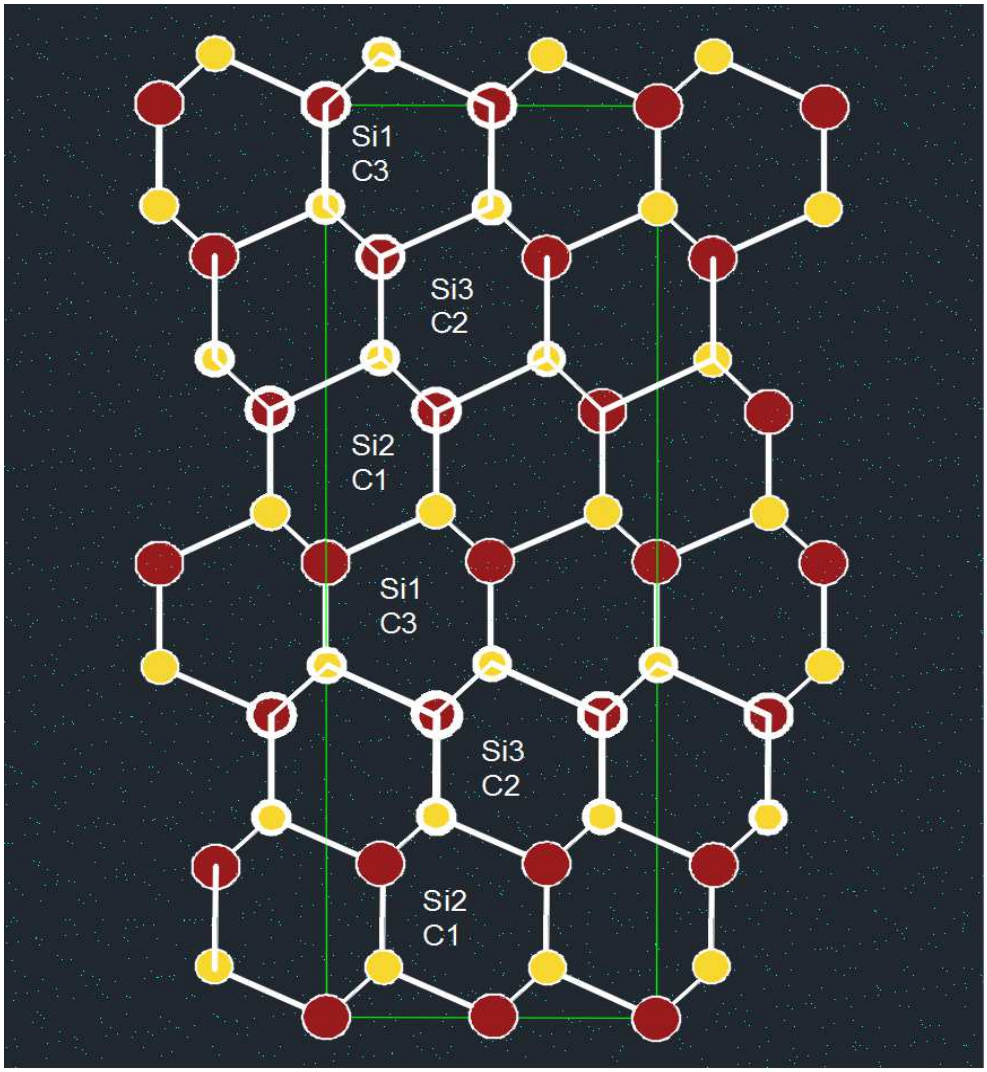

Figure 1: Structure of 6H-SiC [16].

In Table 1 both theoretical and experimental values of bandgap (the energy difference between the valence band and the conduction band) for the most occurring polytypes of Silicon carbide along with the details of μ_n (mobility of electron) and μ_p (mobility of holes) which are given by the following formula

$$\mu_{n,p} = qT_c / 2m_{n,p} \qquad 1$$

where T_c is the collision time, q is the charge of electron or hole and $m_{n,p}$ is the mass of electron or hole [10].

Polytype	Sequence	E_g (eV) (Experimental)	E_g (eV) (Theoretical)	μ_n	μ_p	Thermal Conductivity (W cm^{-1} K^{-1})
6H-SiC	ABCACB	3.023	3.05	370^a 50^c	70	4.9
4H-SiC	ABCB	3.263	3.28	720^a 650^c	90	3.7
3C-SiC	ABC	2.390	2.40	900	40	3.6
2H-SiC	AB	3.330	4.04	-	-	-
15R-SiC	ABCACBCABACABCB	2.986	3.03	400	-	-

Table 1: Sequence and Electrical Properties of several Silicon Carbide polytypes [7-11].

Electrical conductivity is defined as the measure of the conductivity that is flow of electrons in the material when the material is exposed to current. It is reciprocal of resistivity. Denoted by k. In table 1 the electron mobility is given in terms of lattice constants a and c for the polytypes 6H-SiC and 4H-SiC as these lattice constants are defined as axial lengths of the lattice in x and z direction respectively whereas a and c are equal in cubic and rhombohedral lattices but unequal in tetragonal, orthorhombic and hexagonal lattices [10].

The polytypes of the Silicon Carbide shown in the above table are the basic Silicon carbide polytype structures and are most frequently occurring polytypes among many other polytypes of Silicon Carbide (SiC). Indirect bandgap is defined as the energy difference between the valence band and the conduction band of a semiconductor. Thermal conductivity is defined as the heat flow per unit area per unit time for a semiconductor. Indirect bandgaps and thermal conductivity

differ in all the polytypes of the Silicon Carbide due to the difference in the arrangement of the Di-atomic layers (A, B and C) in each polytype [8]. The usage of 4H-SiC and 6H-SiC is predominant than other polytypes due to their high thermal conductivity (as shown in Table 1).

2.1 Doping of Silicon Carbide (SiC):

Doping of a semiconductor increases its conductivity along with the changes in the electrical properties of crystal. There are two types of doping possible in Silicon carbide i) doping with n-type elements namely nitrogen and ii) doping with p-type namely boron, aluminium and gallium [6]. The effects of doping of the dopants is illustrated below [6,12-15]:

a) Doping with nitrogen:

   This doping has an effect of replacing the 'Carbon' sites in the Silicon Carbide lattice. It is a wide range doping as to maintain the resistivity of the Silicon Carbide substrate. Nitrogen doping is done through the method of nitrogen incorporation. Nitrogen incorporation is performed as the process of adding the Nitrogen gas when the crystal is in growth stage. Diffusion method is used in most of the cases. Diffusion is the process of exposing the substrate to the Gas containing the doping agent in this case nitrogen gas. Due to the doping of the nitrogen there is an effect of Photoluminescence in the lattice of 6H-SiC and 4H-SiC.

b) Doping with Boron:

   Silicon carbide crystal exhibits property of Superconductivity when doped with the Boron. At a temperature of 1.5K the crystal resistance drop to zero and exhibits metallic properties after this critical temperature. Like the doping of nitrogen, even boron replaces the Carbon in the Silicon Carbide Crystal.

c) Doping with Aluminium:

In contrast to the doping of nitrogen, aluminium doping will replace the Silicon atom in the Silicon carbide crystal. Doping of Aluminium causes damage to the lattice as aluminum is heavier when compared to Boron. It is doped using the ion implantation method or diffusion method. Ion implantation is a method of implanting the doping ions on to the equally concentrated substrate. Annealing is required after the process of Ion implantation to restore substrate crystallinity.

d) Doping with gallium:

Gallium in form of gallium arsenide is generally used for doping the silicon based substrates. On doping with gallium, the Silicon Carbide crystal exhibits many deformations in the form of bond lengths, bond angles and energy gap. Energy bandgaps will increase but the conductivity decreases due to the change in the crystalline structure of the Silicon Carbide crystal upon doping.

2.2 Semiconductor Devices:

Since, the invention of the PN junction diode, which is formed when a semiconductor is doped with p-type (generally III group elements in the periodic table) and n-type (generally V group elements in the periodic table) dopants there has been many semiconductor devices introduced till today [17-19]. Modern day semiconductor devices namely transistors are having three or more terminals and are formed from the basics of the PN junction diode [17]. They are different types of transistors based on the operations in the device namely [1,3,6,17-19]

a) Bipolar Junction Transistors:

These transistors will have three terminals namely Emitter, Base and Collector. It is also called as current controlled device. It has very less input impedance which allows flowing of large current from emitter to collector when comparatively small amounts of current flows through

base. It is the only type of transistor to be operated by flow of current. There are three regions of operation

1) Cut-Off Region: It is also called as OFF state as there will be no current passing through the transistor.

2) Active Region: In this region, the input signal is amplified by the transistor where the transistor acting as amplifier.

3) Saturation Region: The transistor acts as an On Switch in this region.

b) Field Effect Transistors:

These transistors will also three terminals namely gate, source and drain. It is also called as Voltage controlled device as it uses the voltage applied at gate to control the current flow which is proportional to the input voltage. It has high input impedance which makes it sensitive to the change in the input. The following are the regions of operation

1) Ohmic region: In this region JFET acts as Voltage controlled resister and consists of a very small depletion layer of channel

2) Cut-Off region: It is also called as pinch-off region and JFET will act as an open circuit as it has maximum resistance due to ground and source voltage.

3) Active Region: It is also called as Saturation Region and JFET will act as a good conductor which is controlled by Gate-source voltage.

4) Breakdown Region: The resistive channel of JFET breaks down while operating in this region. This breakdown is due to high voltage between drain and source due to which there will be a large amount of current passing through JFET.

But, the following are the advantages of junction field effect transistors over bipolar junction transistor [17-20]

1) Junction Field effect transistors has less power consumption and dissipation when compared to Bipolar Junction Transistors.
2) Junction field effect transistors has positive temperature coefficient while compared to the bipolar junction transistor which have negative temperature coefficient which is responsible for overheating of the device.
3) Bipolar junction transistor has more noise when compared to junction field effect transistor due to low input impedance in bipolar junction transistor.
4) Junction Field effect transistors(JFET) possess high packing density as the size of JFET very small when compared to Bipolar junction transistor.
5) High doping of emitters will play an important role in decreasing the d.c gain which is typically ~ (5-15) for bipolar junction transistors.
6) Field effect transistor are more stable at high temperatures and are used in high temperature applications when compared to bipolar junction transistor which are sensitive to high temperatures.
7) Fabrication of the junction field effect transistors is more easy compared to the bipolar junction transistor and hence, junction field effect transistors are used in digital circuits.

Due to the following reasons, most of the modern-day semiconductor devices are represented by the junction field effect transistors (JFET).

As Junction field effect transistors are widely used in modern world we will discuss about the fabrication process of the Silicon carbide junction field effect transistors in the following part of the literature review.

2.3 Fabrication of Silicon Carbide Junction Field Effect Transistor:

Initiation for the development of the Silicon Carbide (SiC) devices was done by NASA for the usage of the electronic devices at higher temperatures of order 500 ˚C and this development of the epitaxial 6H-Silicon Carbide Junction field effect transistor having the cross section as shown in Figure 2 was the initial development of a durable technology which can be operated at the temperatures of order 500 ˚C for a longer time when compared to the Conventional CMOS devices [21].

But as shown in Figure 2 JFET having n-channel is chosen due to the following factors [24]:

a) The mobility of electrons in the n-channel is faster than the mobility of holes in the p-channel junction field effect transistors.
b) N-channel junction field effect transistors have low input noise and high trans-conductance when compared to the high input noise in the p-channel junction field effect transistors along with very small trans-conductance.

The schematic cross section of the Silicon Carbide Junction field effect transistor shown in the Figure 2 which consists of an epitaxial Silicon carbide p-n junction diode formed due to the low current at the gate terminal is stable and more robust to the degradation caused due to high temperature exposure of the transistor when compared to other transistor technologies and thereby having benefits of power dissipation, design, and performance along with frequency.

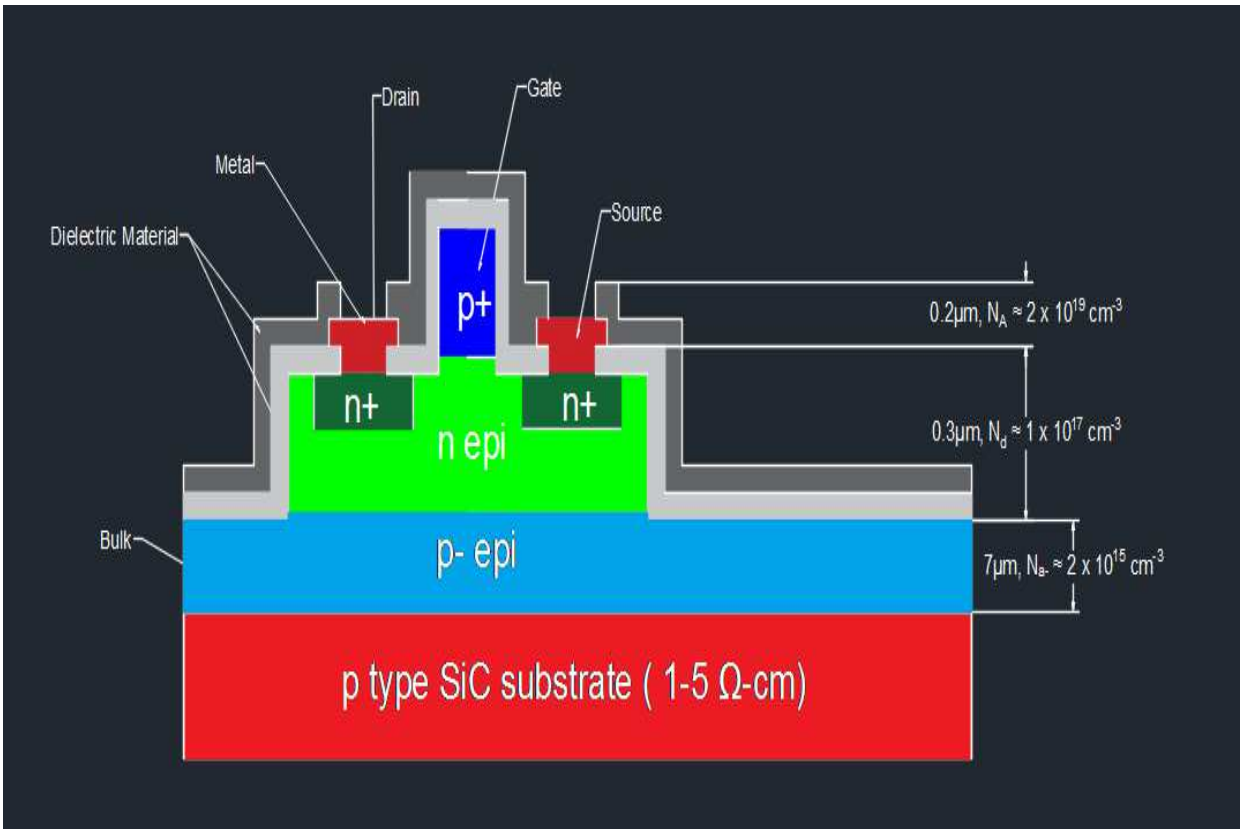

Figure 2 – Cross Section of Silicon Carbide JFET [23].

The performance of the Silicon Carbide Junction field transistors is indirectly dependent on the fabrication as defects formed during the fabrication process may degrade the ideal performance of the device [21]. There are two types of point defects (defects comprising of few number of atoms) present in the crystalline structure of the silicon carbide namely intrinsic and extrinsic defects as shown in Figure 3 and are explained in detail below [8, 25-30]:

a) Intrinsic defects: The Occurrence of these defects is due to the location of the Silicon and Carbon atoms in the crystalline structure of the Silicon Carbide. There is no involvement of any foreign atom in these defects. In these types of defects either of the atoms of the Silicon carbide are vacant or incorrectly placed.

First type of intrinsic defect namely Vacancies is due to the vacant spaces in the crystalline structure of the Silicon Carbide by the atoms of Silicon denoted as V_{Si} and Carbon denoted as V_C and missing of the atoms is generally caused during the formation of the crystal structure. The vacancies of Silicon and carbon atoms are studied using different spectroscopy methods namely Positron Lifetime measurement, Doppler broadening, and electron paramagnetic resonance spectroscopy.

Second type of intrinsic defect namely Antisite is due to the presence of a wrong atom in the lattice site of the other atom. Here, presence of Carbon atom in place of Silicon generates Antisite defect in the crystal denoted by C_{Si}, even Silicon atom in place of Carbon atom denoted by Si_C is also generates antisite defect. Same as Vacancy Defect these are also generated during the formation of the crystal lattice. Annealing of the lattice at 350 ˚C will remove these defects from the lattice. Most persistent antisite defect of the Silicon Carbide crystal is the Di-Carbon antisite denoted by D_{II} which is configured by the presence of two carbon atoms sharing a single silicon lattice site. By using method of low -temperature luminescence spectroscopy on a ion-implanted and annealed 3C-SiC we can detect the defect site of Di-carbon antisite.

Combination of the above two types of defects antisite and vacancy forms the third type of defect namely Vacancy-Antisite Pair. For instance, vacancy of Silicon and antisite of Carbon is denoted by $V_{Si} – Si_C$ is one combination of the pair. These defects are most persistent defects of Silicon Carbide crystal and they properties may vary with the Silicon Carbide polytype.

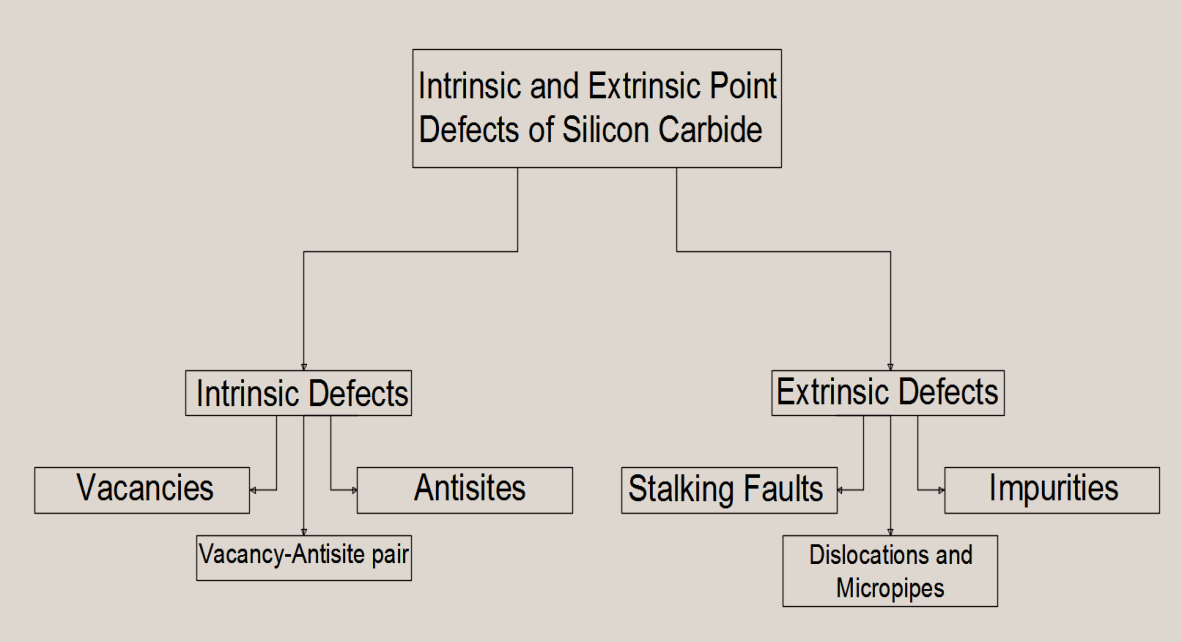

Figure 3: Intrinsic and Extrinsic Defects of Silicon Carbide [8].

b) Extrinsic Defects: Unlike intrinsic defects, these defects are caused due to presence of a foreign element in the crystal lattice of Silicon Carbide. They are of three types of extrinsic defects as follows

Silicon carbide forms a perfect stacking sequence using silicon and carbon atoms but in the case of extrinsic defect of Stacking faults, this sequence is deviated due to already grown intrinsic defects in the crystal lattice or inducing a foreign element into the lattice of silicon carbide which is called stress induced extrinsic defect. There are two types of stacking faults namely Dislocation glide (having a foreign element in the location of lattice element) and Stacking glide (inducing a foreign element into the crystal lattice) and stacking faults can be examined using Transmission electron microscopy.

Having an impurity in the crystal lattice of Silicon Carbide is an extrinsic defect of type Impurities. These extrinsic defects mostly consist a foreign atom either of Nitrogen or Boron as Nitrogen or boron have equal probability of occupying the three nonequivalent carbon sites

but this impurity can be easily resolved due to strong p character of nitrogen and strong s character of boron. Impurity extrinsic defect can be studied using Electron spin resonance spectroscopy.

The most predominant extrinsic defect of Silicon Carbide is dislocations and micropipes. These extrinsic defects mostly occur on the (001) surface (surface which is parallel to z-axis in 3D plane). Glide lines is the crystal property being exhibited at the glide plane (plane which exists in a combination of 2 axes like x-y or x-z or y-z plane). These extrinsic defects exhibit glide lines which intersect the glide lines of crystal lattice by being parallel to the plane in a perpendicular direction. X-Ray diffraction microscopy and etching in conjunction with optical microscopy are used to observe this extrinsic defect and for the identification of the intersecting glide lines of the extrinsic defect is done using conventional etching techniques.

The process of fabrication as shown in Figure 2 was developed at NASA Glenn Research center but there are some modifications done to the developed fabrication of Junction field effect transistor Integrated Circuits for the microfabrication (fabricating the integrated circuit at a micrometer scale usually for electronic circuit designing) [3,22]. The fabrication process is done on a p-type Silicon carbide wafer of 2 inches thick [3]. This Silicon Carbide Wafer is Aluminium doped having a resistivity of 1-5 ohms-cm [3]. The layer built on the Silicon Carbide Wafer of 7 micrometers thick and being doped by Aluminium having a doping level of approximately 2 X 10^{15} cm^{-3} of p^-type [3]. This layer acts as Bulk of the transistor as to ensure the channel depletion in the transistor formed is dominated by gate bias [3]. Bulk is considered as the first epitaxial layer in the fabrication process of Silicon Carbide Junction field effect transistor [3].

Coming to the second epitaxial layer of the Junction field effect transistor it is of 0.3 micrometers thick doped with nitrogen on top of the first epitaxial layer of p^- bulk layer to act as a

n-channel layer for the junction field effect transistor [3]. This layer is doped with doping level of approximately 1 X 10^{17} cm^{-3} [3]. At the last the third epitaxial layer is generated on top of the nitrogen-doped epitaxial layer consisting of 0.2 micrometers thick and doping level approximately of 2 X 10^{19} cm^{-3} [3]. This layer is doped with aluminium and it is called as p^{+} epitaxial layer or gate of junction field effect transistor [3]. The manufacturer of the Junction field effect transistor specifies ±10% variation on the thickness of the epitaxial layers and ±50% variation on the doping level of the dopant in each of the layers in the Silicon Carbide junction field effect transistor [21]. The doping levels and thickness are specified for the wide range of operation as the threshold voltage should be negative for the depletion region of the n-channel junction field effect transistor and the doping of gate channel is 10^{2} times the doping level of n-channel layer for the formation of depletion region in the junction field effect transistor channel [21]. Whereas the bulk is lightly doped when compared to all the epitaxial layers to reduce the effect of bulk on the parameters of the junction field effect transistor due to the formation of depletion region during the reverse substrate bias [21]. After the formation of the three epitaxial layers on the Silicon Carbide substrate (as per the source from Cree Inc.) the fabricated transistor is subjected to the following techniques to obtain discrete junction field effect transistor [3,5,21].

a) The processes of Inductively coupled plasma and reactive ion etching are used to pattern the gates and channels of junction field effect transistor for nearly vertical side walls by allowing well controlled etching process onto the transistor.
b) After the formation of side walls to form the n-layer ohmic contact areas for the drain and the source the fabricated junction field effect transistor is exposed to the vapor deposition method at low pressure to form 1.5 micrometers mask consisting of low temperature oxide and it is carried out at the temperature of 400 ˚C

c) After the formation of the ohmic contact areas we now exposed the obtained transistor having the contact areas to multiple nitrogen implants at a high temperature of 600 ˚C and doping concentration of the nitrogen implanted is approximately 6 X 10^{19} atoms/cm^3. After the implantation, it is exposed to nitrogen atmosphere at double the temperature for the formation of ohmic contact.

d) Now to generate the wafer passivation (protection from corrosion and for the enhancement of the Silicon carbide wafer) oxide layer of thickness 25 nanometers is thermally grown at the temperature of 1100 ˚C on the surface. It is grown in a wet Di-oxide (O_2) ambient.

e) Lastly the ohmic contacts for the n^+ and p^+ contacts we use the highly durable metallization like Ti/$TaSi_2$/Pt under very low pressure of 10^{-5} pascals pressure. Then the fabricated Silicon Carbide is exposed to the forming gas for 10 minutes under a high temperature of around 900 ˚C. The forming gas to which the finally fabricated junction field effect transistor is exposed is a combination of 5% hydrogen gas and nitrogen gas.

After all the processes a fabricated Silicon carbide wafer has three epitaxial layers of bulk layer, n-channel layer, and Gate along with the ohmic contacts forming a discrete junction field effect transistors of Silicon Carbide [3].

Modeling and Characteristics of a semiconductor device is an important measurable property as these characteristics will help in defining the usage of the semiconductor accordingly. Now in this part of the literature survey we will see about the characterization of the Junction Field effect transistor of Silicon Carbide and based on the channel depletion, Junction field effect transistor exhibits two types i) one as Normally On Junction Field effect transistor where the channel is partially depleted under zero gate bias condition and ii) second one is Normally Off Junction field effect transistor in which the channel is fully depleted under zero gate bias condition [32]. In

general, there are two regions of operation exhibited by the junction field effect transistor which are described as follows [32]:

1) Linear region: In this region, the current generated in the circuit will be proportional to the voltage applied to the circuit. Due to the voltage applied across the gate and source terminals there will be a depletion region formed in the channel which is in uniform width and is formed along the channel.
2) Saturation Region: The current across the circuit is in linear form or constant throughout the region when voltage is applied to the circuit.

These characteristics of the Silicon Carbide Junction field effect transistor output are like that of conventional CMOS semiconductor junction field effect transistor. These regions of operations are named as per the current flow in the circuit as per the voltage applied. These regions are renamed in the 3/2 power model and are explained in detail in the later parts of the literature review.

Coming to the characterization of the output in the junction field effect transistor formed by temperature dependent semiconductor is defined by Chompoonoot Anupongongarch who employed the 3/2 power model in his work for accurate measurement of the circuits which are driven by a large input voltage [31]. This model is a counter part of the square law approximation Schichman-Hodges model. The details of the two models are described as below [21]:

1) Schichman-Hodges Model: This model is based on square law approximation but will yield less accurate results when the circuit is subjected to the input of signal having large swings (swings are described as the difference of the maximum level of the signal to the minimum level of the signal). This method is mostly used in modeling of Metal Oxide Semiconductor

field effect transistors and can also be used for modeling of the Junction Field effect transistor due to its simple methodology. The large swings in the signal at the gate terminal generally occur in logical circuits due to which this model is very inaccurate for the characterization of the Silicon Carbide Junction field effect transistors at high temperatures.

2) 3/2 power model: Due to the inaccuracy in the measurements obtained during the characterization of the Junction Field effect transistor by the Schichman-Hodges model, 3/2 power model is introduced and it is helpful in obtaining accurate measurements for the characterization of the Junction Field effect transistor of Silicon Carbide at High temperatures. This model is generally known as traditional power model and it is relatively complex when compared to the square law approximation model.

SECTION 3

SPICE MODELS FROM NASA

The National Aeronautics and Space Administration has designed SPICE models of Order 1 for the 4H-Silicon Carbide Junction Field Effect transistors (JFET's). These 4H-SiC JFET models are used for the spice simulations at the extreme temperatures of about 500 ˚C [33]. These models are based on the temperature dependence and the radial device distance from the center of each wafer denoted by r. Behavior of the JFET devices changes with the change in the position of the radial device distance (r) [33].

The experimental results of the JFET device for the Drain Current against the drain voltage for different values of the radial device distance shows that the dependence of the radial device distance (r) is more when the value of r is small i.e., r < 1cm [33]. For a greater value of r the difference of the Current against Voltage is less when compared to the change for r < 1cm [33]. The threshold voltage exhibits a decrease in the voltage with the increase in the radial distance of the wafer [33]. Considering this radial distance for the JFET saturation current, the experimental data shows that there is an exponential increase in the current with the increase in the radial distance [33].

The change of the radial device distance from the center will not have much effect on the n-type sheet resistance of the JFET but in contrast there is a large difference in the n-type contact

resistivity [33]. Due to the effect of the radial device distance of the wafer on the properties of JFET like n-type contact resistivity, JFET saturation current and Drain Voltage we consider the radial device distance as a parameter along with the temperature parameter for the models generated by NASA [33].

The SPICE models have two parameters one is the radial device distance and other is the temperature parameter [33]. These parameters of radial device distance of the wafer and the temperature help in obtaining the SPICE models when they are implemented in the software tool based on LabVIEW [33]. The models obtained are designed by applying the experimentally obtained data along with the concepts of the 1-dimensional physics equation of the 4H-Silicon Carbide Junction field effect transistor [33].

The SPICE models generated results are approximately equal to the experimentally generated results when the device is having the source/drain contacts is a linear ohmic variant contacts [33].

The Nine test cases generated from the variation of the radial device distance parameter of the wafer and the temperature are based on the “boundaries + middle value” design methodology [33]. This methodology is based on the extreme values of the parameter along with the middle value of the parameter [33]. This type of simulations are called ratio-based circuit design simulations which provide the detail results of the device operation across the varied parameter. The extreme and middle values of the two parameters are given in Table 2 [33].

Parameter	Lower Extreme Value	Middle Value	Upper Extreme Value
Temperature	25˚C	300˚C	500˚C
Radial device distance of the wafer	0 cm	1.5 cm	3 cm

Table 2: Parameters values used for the SPICE test cases [33].

Using the above table 9 SPICE models are generated which are shown in Table 3.

T (˚C)	r(cm)	JFET SPICE Model Text
25	0	. MODEL sicnjet NMOS LEVEL=1 VTO=-8.85 KP=1.08E-5 GAMMA=0.897 LAMBDA=0.006 CJ=6.86E-5 PB=2.87 PHI=1.435 RD=3175 RS=3175
25	1.5	. MODEL sicnjet NMOS LEVEL=1 VTO=-10.27 KP=1.03E-5 GAMMA=0.953 LAMBDA=0.006 CJ=6.86E-5 PB=2.87 PHI=1.435 RD=3175 RS=3175
25	3	. MODEL sicnjet NMOS LEVEL=1 VTO=-15.03 KP=9.34E-6 GAMMA=1.12 LAMBDA=0.006 CJ=6.86E-5 PB=2.87 PHI=1.435 RD=3175 RS=3175
300	0	. MODEL sicnjet NMOS LEVEL=1 VTO=-9.23 KP=3.62E-6 GAMMA=0.897 LAMBDA=0.006 CJ=7.53E-5 PB=2.378 PHI=1.189 RD=4291 RS=4291

300	1.5	. MODEL sicnjet NMOS LEVEL=1 VTO=-10.67 KP=3.49E-6 GAMMA=0.953 LAMBDA=0.006 CJ=7.53E-5 PB=2.378 PHI=1.189 RD=4291 RS=4291
300	3	. MODEL sicnjet NMOS LEVEL=1 VTO=-15.45 KP=3.14E-6 GAMMA=1.12 LAMBDA=0.006 CJ=7.53E-5 PB=2.378 PHI=1.189 RD=4291 RS=4291
500	0	. MODEL sicnjet NMOS LEVEL=1 VTO=-9.55 KP=2.00E-6 GAMMA=0.897 LAMBDA=0.006 CJ=8.22E-5 PB=1.997 PHI=0.998 RD=6203 RS=6203
500	1.5	. MODEL sicnjet NMOS LEVEL=1 VTO=-11.00 KP=1.92E-6 GAMMA=0.953 LAMBDA=0.006 CJ=8.22E-5 PB=1.997 PHI=0.998 RD=6203 RS=6203
500	3	. MODEL sicnjet NMOS LEVEL=1 VTO=-15.80 KP=1.73E-6 GAMMA=1.12 LAMBDA=0.006 CJ=8.22E-5 PB=1.997 PHI=0.998 RD=6203 RS=6203

Table 3: 9 SPICE Models of 4H-SiC JFET [33].

These models are based on the parameters that change with a change in temperature. The parameters defined in the model are as follows [34]

VTO – Pinch off Voltage.

KP – Transconductance parameter (also called as BETA β).

GAMMA – Threshold Voltage.

LAMBDA – Channel Length modulation parameter.

CJ – Junction capacitance parameter.

PB – Gate junction potential.

PHI – Surface potential.

RD – Drain Ohmic Resistance of the JFET

RS – Source Ohmic Resistance of the JFET

These models are based on the layout of Unit cell JFET. To simulate for the larger models of the JFET we increase the number of unit cell models [33]. A Unit Cell JFET model is defined as Gate width W_G=12μm to the Gate length L_G= 6μm [33].

SECTION 4

PROPOSED SiC JFET SYNTHESIS FLOW

We have proposed the following synthesis flow for the Silicon Carbide JFET as shown in the Figure 4. The flow proposed was based on the requirement of generating the SPICE models in spectre from the schematic in Virtuoso.

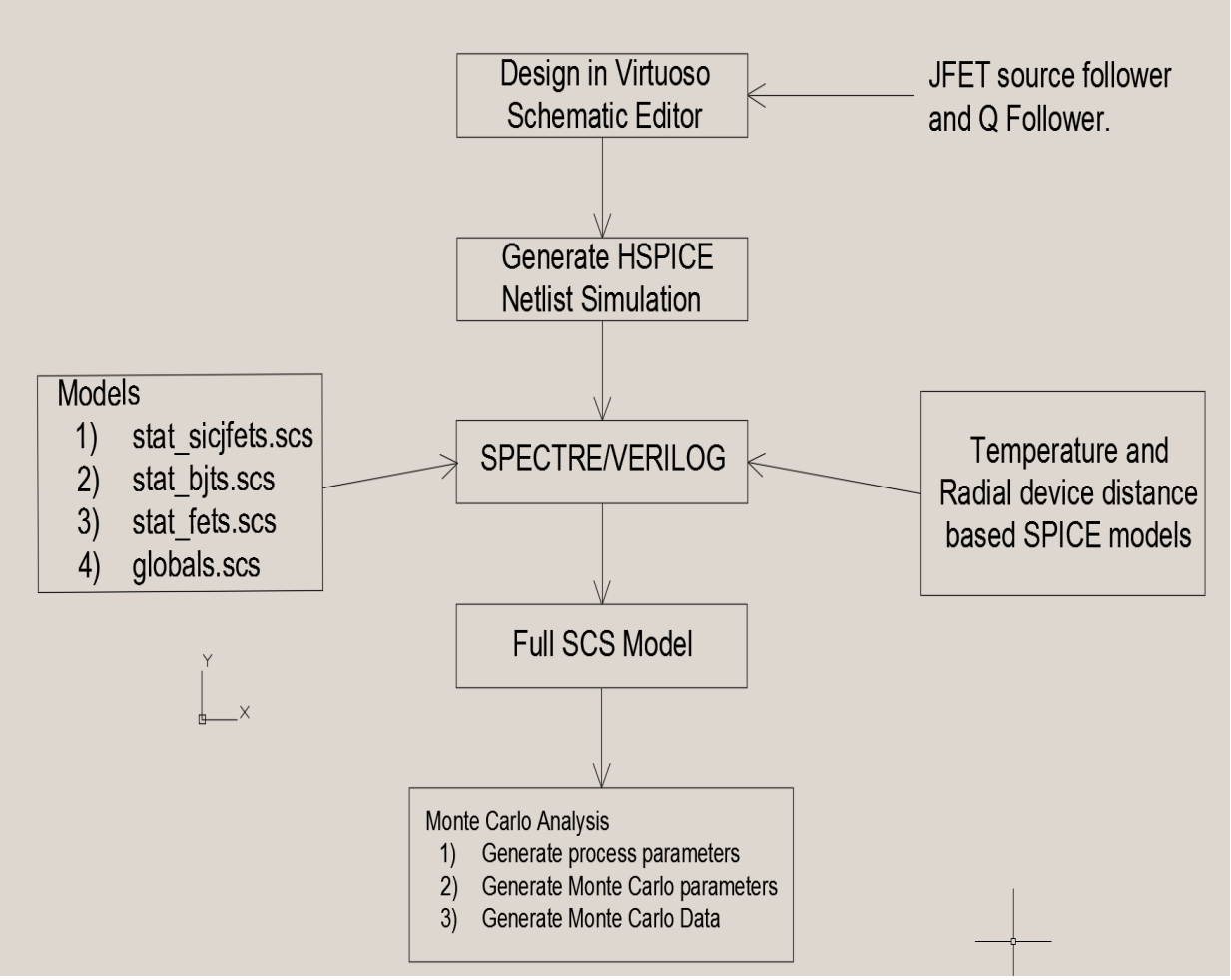

Figure 4: Proposed Silicon Carbide JFET Synthesis Flow.

As shown in the Figure 4 the proposed synthesis flow consists of the following blocks

1) Design in Virtuoso Schematic Editor:

We design the Full Adder Circuit using the Silicon Carbide Field Junction Transistor (JFET's) in the Cadence Virtuoso Schematic Editor. The Full Adder Circuit is comprised of Half Adders, Nor Gates and Follower Circuits.

The Follower circuit designed in this schematic can be of two types

a) Q Follower Circuit

b) Source Follower Circuit.

In Section 5 we will see the difference in the schematic as well as functional details of the two follower circuits.

2) Generation of HSPICE Netlist Simulation:

The Generation of the Netlist can be done from the Virtuoso Schematic Editor. This Schematic editor uses the circuit designed in the Virtuoso and will generate a netlist in the HSPICE model. To Generate a HSPICE model we can go to the Virtuoso Schematic Editor and click on the SPICE model generator. The HSPICE model netlist can be of two types as follows

1) Spectre model.

2) System Verilog Model.

Simulation tools require a SPICE netlist to start the synthesis of the circuit. This HSPICE generated is used for the simulation of the circuit designed in the Virtuoso Schematic editor.

3) Spectre/Verilog Spice File:

The spectre/Verilog file is used for the generating the monte carlo analysis data and the transient analysis for each of the spice model defined in the section 3. The Spectre or Verilog file can be added with the analysis statements for the simulations of the full adder model. Both the spice files are generated using the Hspice netlist simulation. Here, we use the spectre spice file generated from the netlist simulation.

4) JFET spice models:

These spice models are generated from the temperature and radial device distance from the center of the wafer as parameters taken from the SPICE models given by NASA as shown in the table 3. The spice models are used to generate spectre models which are in detailed explained in section 6. The spectre models are used along with the spectre/Verilog file for the simulations of the full adder at different temperatures and radial device distances.

5) Models required for the Simulation of the Spice File:

The models required for the generation of the Full SCS model from the Spectre/Verilog spice are

a) stat_sicjfets.scs

b) stat_bjts.scs

c) stat_fets.scs and

d) globals.scs

These files contain the spectre models required for the simulation of the full adder circuit. The stat_bjts.scs , stat_fets.scs and globals.scs files are given by Cadence. We generated the stat_sicjfets.scs file for the simulation and more details are given in the Section 6.

6) Full SCS Model:

This file contains the Schematic obtained from the HSPICE generation and will be added a set of statements for the monte carlo analysis. In Appendix A we have given the details about the scs file used for the simulation of the Monte Carlo Analysis and the transient analysis. Here, we use the spectre format obtained from the HSPICE netlist simulation. And the spice file is included with the model used for the simulation from the models in stat_sicjfets.scs file.

7) Monte Carlo Analysis:

These monte carlo analysis statements contains the sweep statements of the dc and transient analysis along with the sweep parameters of length of gate, width of gate, oxide thickness and the sheet resistance. These parameters are varied as per the values given in table 4. It also contains the slew rate export statements which help in exporting the slew rate data for each of the parameters. And the simulations are generated based on the values given in the sweep analysis and the process and mismatch parameters which are given along with the monte carlo analysis statements as statistics. We have not given much detail variations in the mismatch parameters as we were concerned about the variations in the characteristics of the SiC JFET due to the change in the temperature and the radial device distance. This Monte Carlo analysis generates the following data

a) Generates process parameters
b) Generates Monte Carlo parameters
c) Generates Monte Carlo Data.

The above data is generated using the monte carlo statement which contain details about the folder specified in mcparams, mcdata, processparam parameters. Here, we have given these parameters related to the folder created for the simulations of the model.

SECTION 5

PROPOSED SiC JFET CIRCUITS

The proposed Silicon Carbide Junction Field Effect transistor circuits are Full Adders which comprise of the Half Adders, Nor Gates and Follower Circuits (Q Follower / Source Follower). These Circuits are designed using the Cadence Virtuoso Schematic layout. The details of the Schematic design are as follows

5.1 Follower Circuits:

We have designed the following two follower circuits namely Q Follower Circuit and the Source Follower Circuit. Figure 5 shows the schematic layout of the Q Follower Circuit.

In the schematic of the Q Follower Circuit we have used the Junction Field effect transistor of instance mos1 having the parameters given from the models generated in the stat_sicjfet.scs file. There are 3 1K ohm resistors added to Gate, Drain and source terminals whereas the base terminal is grounded. A Voltage source V0 is added in parallel to the resistor at the Gate Terminal. We have three pin instances of ground (gnd), vdd and the output pin (opin).

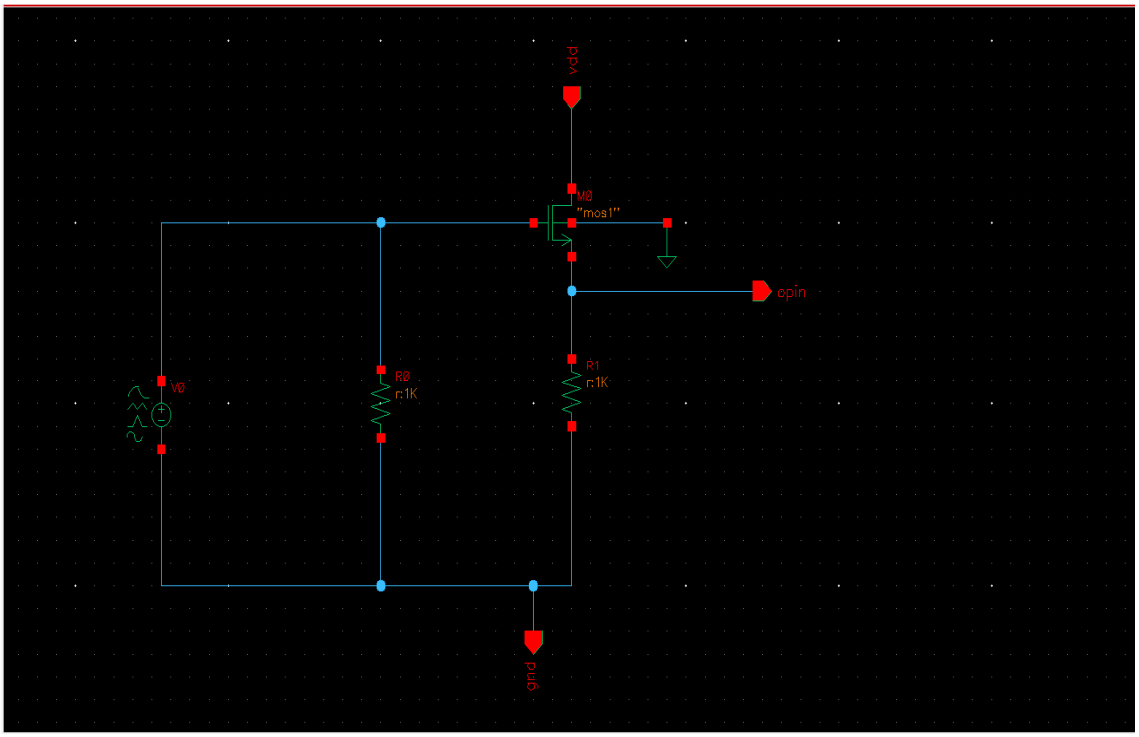

Figure 5: Virtuoso Schematic of Q Follower Circuit.

Now we will see the schematic of the Source Follower Circuit as shown in the Figure 6.

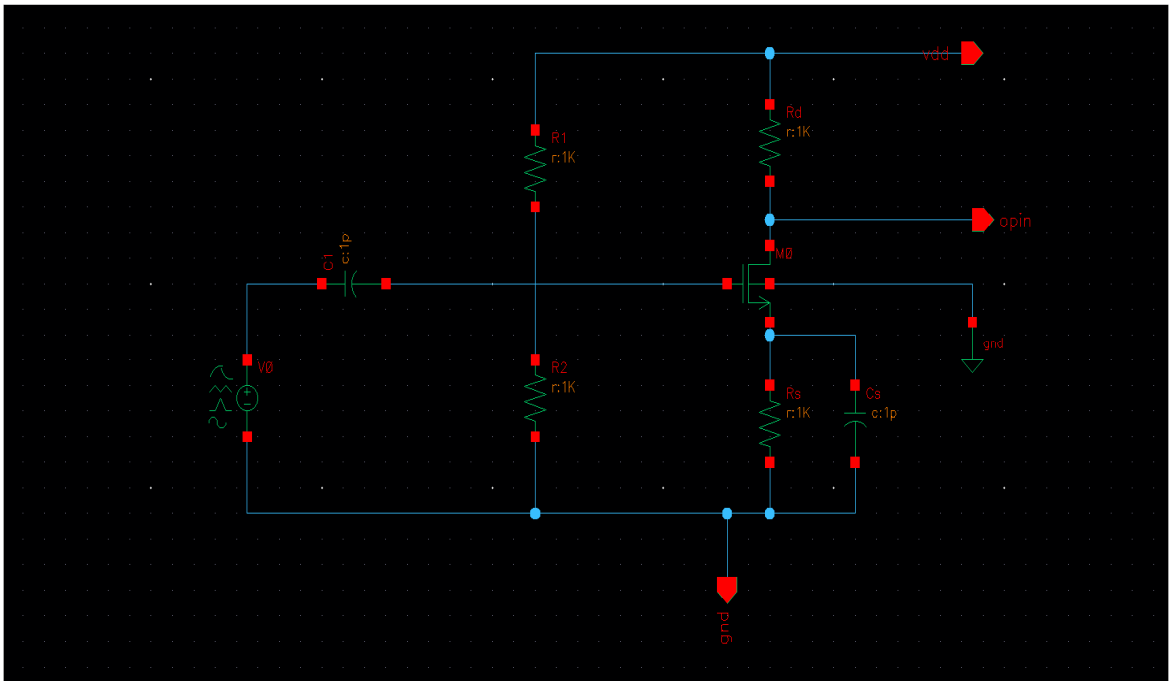

Figure 6: Virtuoso Schematic of the Source Follower Circuit.

The Source Follower Schematic is different from the Q Follower as it has the capacitances placed at the source and the gate terminals. There are two 1K ohm resistors placed across the two terminals of Drain and Source while two 1K ohm resistors connecting the vdd to the ground terminal. Similar to the Q Follower we have a voltage source connected at the gate terminal of the JFET and the base terminal to the ground as shown in Figure 6.

We use the Q Follower instead of the Source Follower due to the impact of the larger input on the capacitances of the Source Follower. We are forced to use the lesser value of the Supply voltage when compared to the Voltage applied at the Q Follower. For the Analysis we vary the Input Voltage which effects the capacitances of the source follower circuits whereas the Q Follower does not have much impact on the circuit.

5.2 Nor Gate Circuit:

The Follower Circuits are used for the designing of the Nor Gate the basic building block for the Full Adder Circuit. Figure 7 shows the Schematic of the Nor Gate Using the Q Follower as the Follower Circuit.

The Schematic of the Nor Gate Consists of two JFET's which are added on the vdd terminal of the Follower Circuit. The gate terminals of the two JFET's are connected to the two inputs in1 (input 1) and in2 (input 2). The ground terminal of the follower is connected to two resistors of 1K ohm each and also to the output pin (opin). In the Similar manner with the Follower Circuit the base of the two JFET's are connected to the ground as shown in the Figure 7.

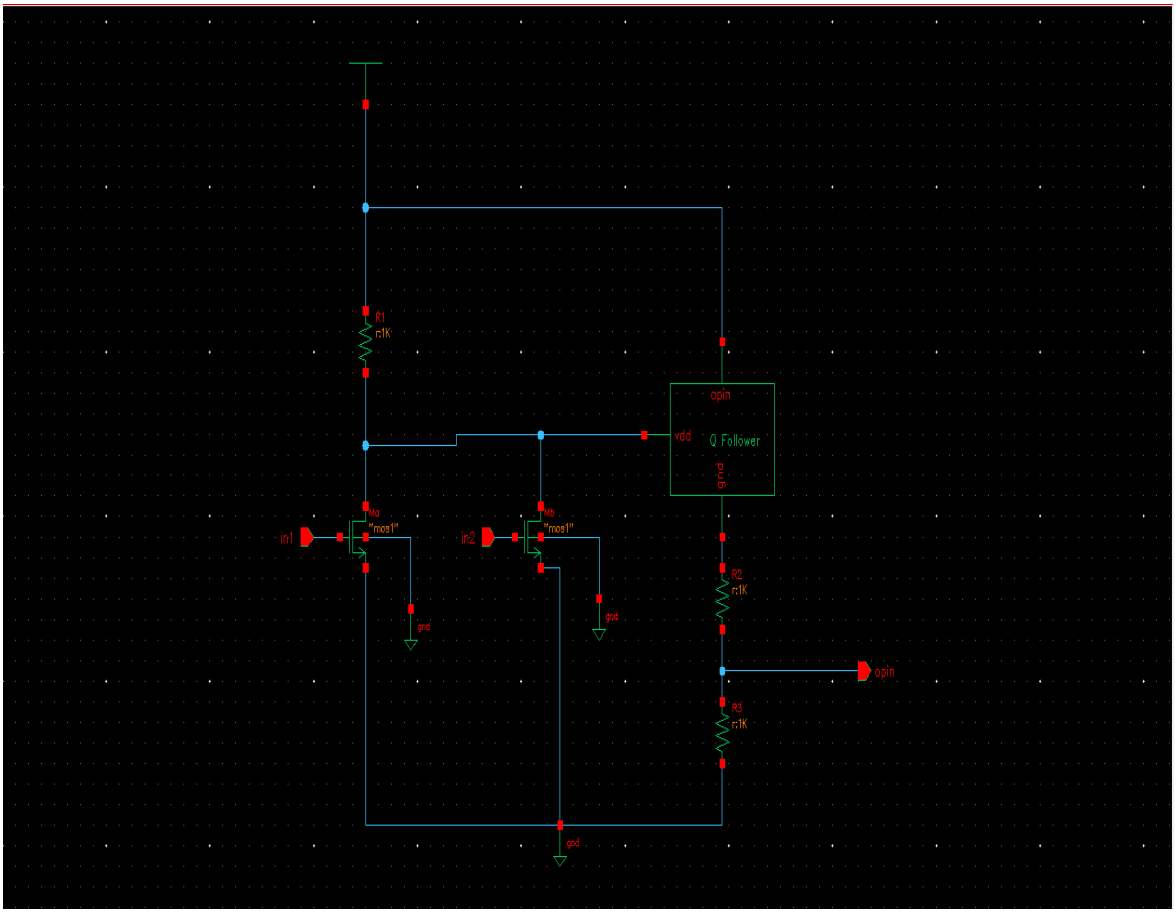

Figure 7: Virtuoso Schematic of the Nor Gate

5.3 Half Adder Circuit:

The Schematic of the Half Adder Circuit is shown in the Figure 8. Half adder contains 5 Nor gates to get the Sum and the Carry output for the Inputs of A and B.

The Following Equations 2 and 3 give the Sum and Carry of the Half Adder Circuit for the inputs of A and B

$$\text{Sum} = A \oplus B \qquad (2)$$

$$\text{Carry} = A \cdot B \qquad (3)$$

Each Nor gates uses the two inputs A and B to give the Sum and Carry outputs of the Half Adder Circuit.

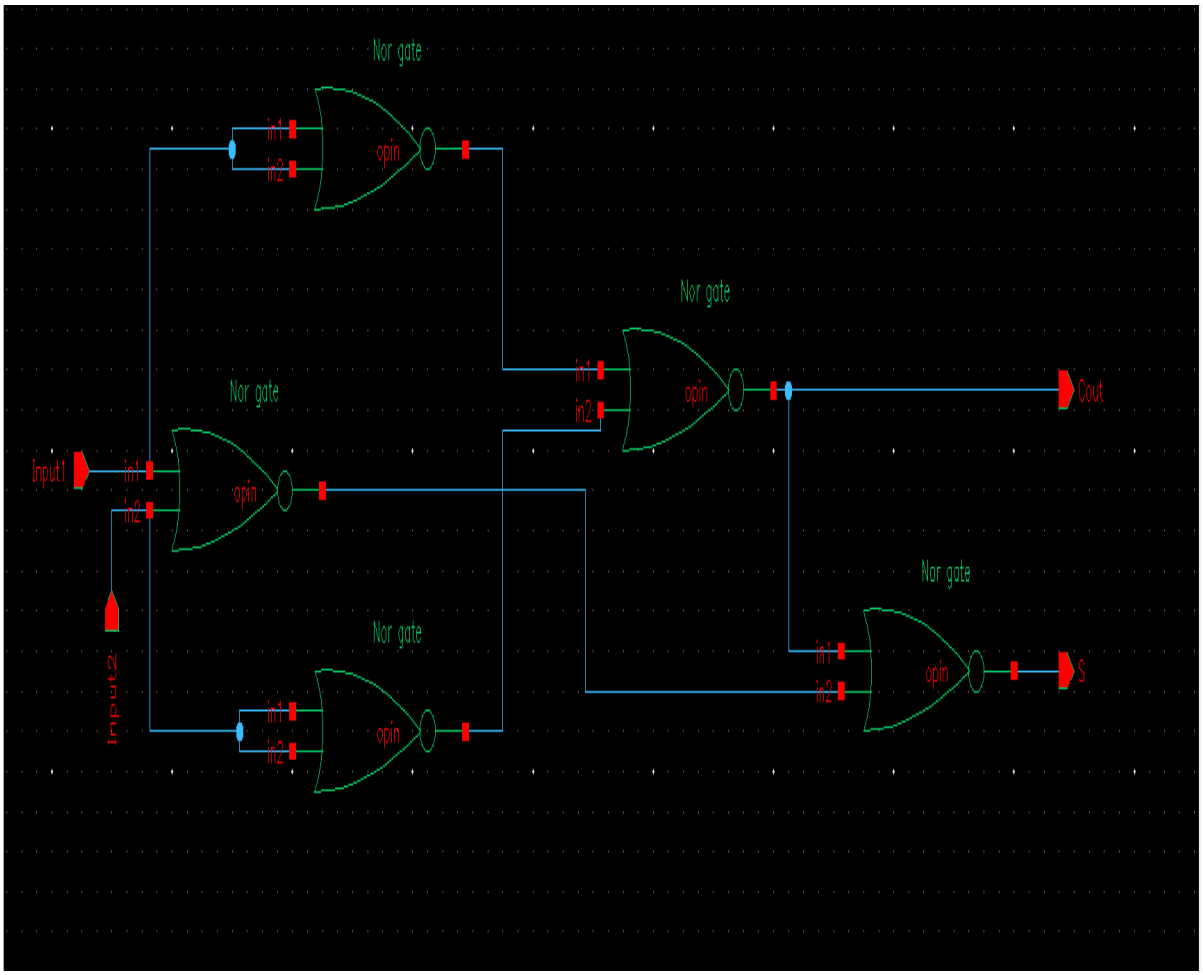

Figure 8: Virtuoso Schematic of a Half Adder Circuit.

As shown in the schematic the outputs of the Half Adder are given by Cout and S.

5.4 Full Adder Circuit:

The Schematic for the Full Adder Circuit is shown in Figure 9. It contains of the Half Adder Circuit and two Nor gates as shown. The half adders has the inputs of A, B, Cin and one of the output of the first half adder. Full adder circuit gives the output of the Sum of the three input and also the Carry of the three input A, B and Cin.

The Following Expressions 4 and 5 are for Sum and Carry of the full adder circuit for the Inputs A, B and Cin

Sum = $A \oplus B \oplus Cin$ 4

Carry = $A \cdot B \cdot Cin$ 5

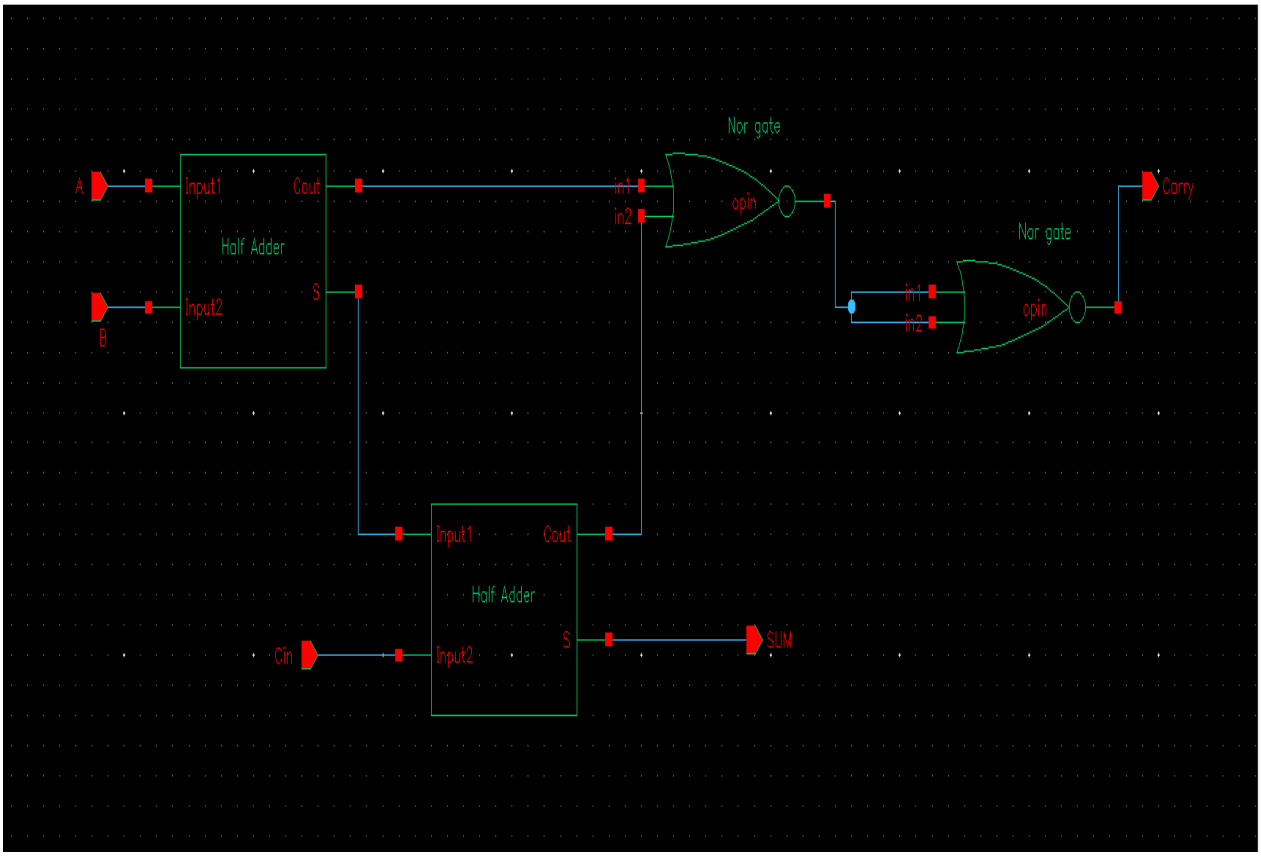

Figure 9: Virtuoso Schematic for a Full Adder Circuit.

As shown in the Schematic the Input to the Second Half adder is the Sum output of the First Half Adder and a new input Cin is given to the Second Adder. We use two Nor Gates one nor gate uses the carry outputs from the two half adders and which will be inverted to the desired output of the Carry. This Full Adder Circuit is Used for the Monte Carlo analysis using the models which will be described in the next section.

SECTION 6

SiC JFET SPECTRE SIMULATION CONSTRAINTS

This section contains the simulation constraints models require to conduct the Monte Carlo Analysis on the Full Adder Circuit described in the previous section. These models are written in Spectre format taken from the SPICE models given from NASA which are described in Section 3. The Following Figure 10-12 will show the spectre models for the temperatures from 25˚C to 500˚C and for the radial device distance from the center of the wafer from 0 cm to 3 cm. As shown in the Figure 10 is the spectre model for the temperature parameter being 25˚C and contains of three different values for the radial distance each being 0 cm for model bmenjfetsic_t25_r0, 1.5 cm for model bmenjfetsic_t25_r1half and 3 cm for model bmensicjfet_t25_r3 respectively.

This model contains sub circuits in the stat_sicjfet.scs file and the sub circuit name is used in the Full Adder spectre file to inherit the model used for the designing by applying the following parameters vto, kp, gamma, lambda, cj, pb, phi, rd and rs. These parameters are considered as they vary with the temperature and the radial device distance from the center for the wafer as described in the section 3 containing the SPICE models.

```
inline subckt bmenjfetsic_t25_r0 (d g s b )
bmenjfetsic_t25_r0 (d g s b ) sicnjfet
        model sicnjfet mos1 type=n  vto=-8.85 kp=1.08e-5 gamma=0.897 tnom=25
        + lambda=0.006 cj=6.86e-5 pb=2.87 phi=1.435 rd=3175 rs=3175
ends bmenjfetsic_t25_r0

inline subckt bmenjfetsic_t25_r1half (d g s b )
bmenjfetsic_t25_r1half (d g s b ) sicnjfet
        model sicnjfet mos1 type=n vto=-10.27 kp=1.03e-5 gamma=0.953 tnom=25
        + lambda=0.006 cj=6.86e-5 pb=2.87 phi=1.435 rd=3175 rs=3175
ends bmenjfetsic_t25_r1half

inline subckt bmenjfetsic_t25_r3 (d g s b )
bmenjfetsic_t25_r3 (d g s b ) sicnjfet
        model sicnjfet mos1 type=n vto=-15.03 kp=9.34e-6 gamma=1.12 tnom=25
        + lambda=0.006 cj=6.86e-5 pb=2.87 phi=1.435 rd=3175 rs=3175
ends bmenjfetsic_t25_r3
```

Figure 10: Spectre Models for Temperature 25˚C

The following Figure 11 also contains three models in Spectre format for the temperature of 300 ˚C and the model bmenjfetsic_t300_r0 is for the radial distance parameter of 0 cm, model bmenjfetsic_t300_r1half for radial distance parameter of 1.5 cm and model bmnejfetsic_t300_r3 for the radial distance parameter of 3 cm.

```
inline subckt bmenjfetsic_t300_r0 (d g s b )
bmenjfetsic_t300_r0 (d g s b ) sicnjfet
        model sicnjfet mos1 type=n vto=-9.23 kp=3.62e-6 gamma=0.897 tnom=300
        + lambda=0.006 cj=7.53e-5 pb=2.378 phi=1.189 rd=4291 rs=4291
ends bmenjfetsic_t300_r0

inline subckt bmenjfetsic_t300_r1half (d g s b )
bmenjfetsic_t300_r1half (d g s b ) sicnjfet
        model sicnjfet mos1 type=n vto=-10.67 kp=3.49e-6 gamma=0.953 tnom=300
        + lambda=0.006 cj=7.53e-5 pb=2.378 phi=1.189 rd=4291 rs=4291
ends bmenjfetsic_t300_r1half

inline subckt bmenjfetsic_t300_r3 (d g s b )
bmenjfetsic_t300_r3 (d g s b ) sicnjfet
        model sicnjfet mos1 type=n vto=-15.45 kp=3.14e-6 gamma=1.12 tnom=300
        + lambda=0.006 cj=7.53e-5 pb=2.378 phi=1.189 rd=4291 rs=4291
ends bmenjfetsic_t300_r3
```

Figure 11: Spectre Models for temperature of 300˚C

These are the models for the 2nd type of the temperature variations models used for the synthesis of the Full Adder Circuit.

The third model contains of the models based on the temperatures at 500˚C and with the same radial distance parameter variations as mentioned above. From the Figure 12 we have three models namely bmenjfetsic_t500_r0, bmenjfetsic_t500_r1half and bmenjfetsic_t500_r3 for the radial device distance from the center of the wafer parameter being 0 cm, 1.5 cm and 3 cm respectively.

```
inline subckt bmenjfetsic_t500_r0 (d g s b )
bmenjfetsic_t500_r0 (d g s b ) sicnjfet
       model sicnjfet mos1 type=n vto=-9.55 kp=2.00e-6 gamma=0.897 tnom=500
       + lambda=0.006 cj=8.22e-5 pb=1.997 phi=0.998 rd=6203 rs=6203
ends bmenjfetsic_t300_r0

inline subckt bmenjfetsic_t500_r1half (d g s b )
bmenjfetsic_t500_r1half (d g s b ) sicnjfet
       model sicnjfet mos1 type=n vto=-11.00 kp=1.92e-6 gamma=0.953 tnom=500
       + lambda=0.006 cj=8.22e-5 pb=1.997 phi=0.998 rd=6203 rs=6203
ends bmenjfetsic_t500_r1half

inline subckt bmenjfetsic_t500_r3 (d g s b )
bmenjfetsic_t500_r3 (d g s b ) sicnjfet
       model sicnjfet mos1 type=n vto=-15.80 kp=1.73e-6 gamma=1.12 tnom=500
       + lambda=0.006 cj=8.22e-5 pb=1.997 phi=0.998 rd=6203 rs=6203
ends bmenjfetsic_t500_r3
```

Figure 12: Spectre Models for temperature of 500˚C

All the three types of the models are present in the stat_sicjfets.scs file in the models folder of the Spectre/spectre_10_1. We use all the three models for the variation of the temperature of the JFET in the full adder circuit imposing the parameters to be used which vary with the

temperature and the radial device distance. These models are useful for creating the BLEO environment to test the Silicon Carbide JFET for the dependency of the temperature.

SECTION 7

SIMULATION RESULTS

This Section will deal with the Simulation Results obtained from the Full Adder Circuit spectre file which is given in Appendix A using the spectre models which are defined in the previous section. We have proposed the Monte Carlo Simulations for the full adder circuit as shown in the Figure 10.

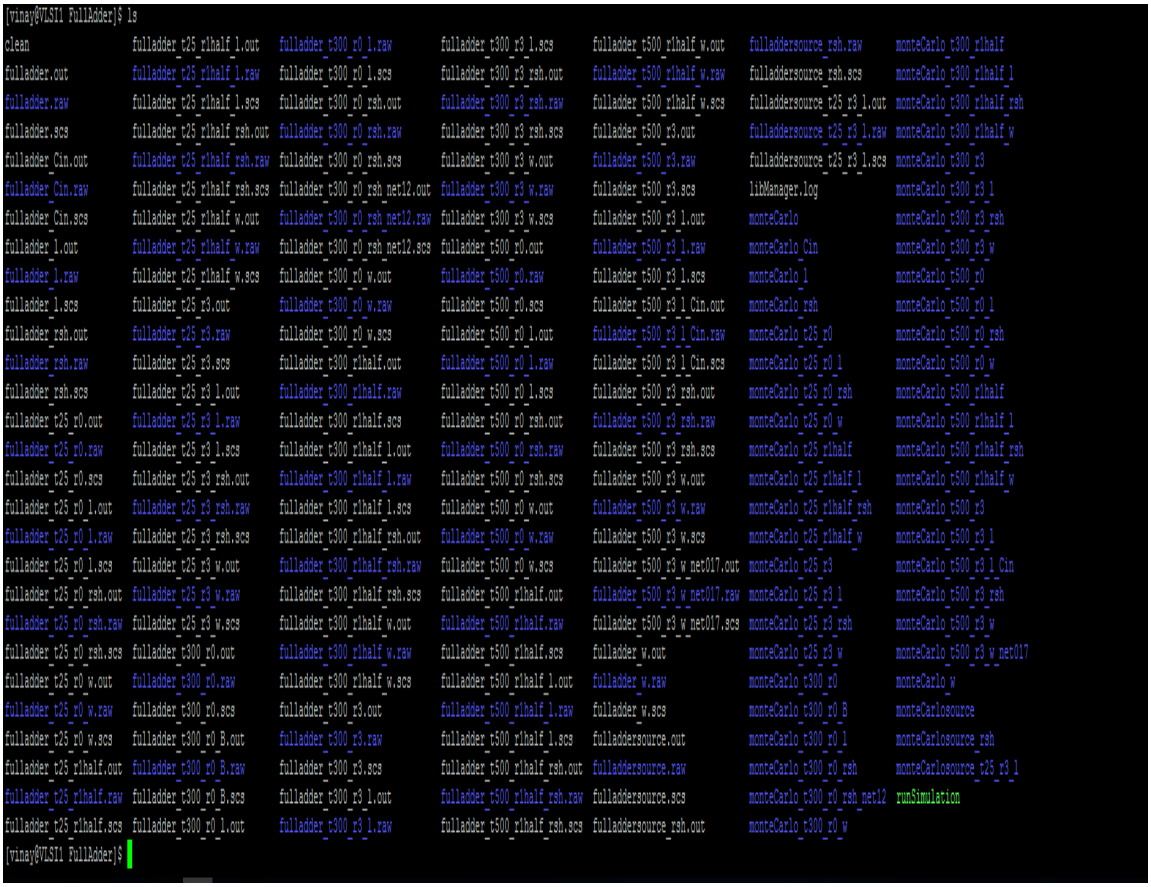

Figure 13: All the simulation of the Full Adder Circuit.

In the above Figure (Figure 13) we can see all the simulations that are conducted on the Virtuoso Schematic designed Full Adder and using the models in stat_sicjfets.scs file we have created the different models varying them by the temperature, radial device distance parameter along with the parameters of oxide thickness, sheet resistance and also by varying length and width of the gate. The parameters used for the Monte Carlo analysis are given in the Table 4 below.

Parameter Used for MC simulation	**Values of the parameters used in the Monte Carlo Analysis.**
Oxide Thickness (tox)	1e-7, 5e-7, 1e-6, 5e-6, 1e-5, 5e-5, 1e-4, 5e-4.
Sheet Resistance (rsh)	7e-4, 4e-4, 2e-4, 1e-4, 8e-5, 6e-5, 1e-5.
Length of the Gate (l)	4.8e-4, 4.5e-4, 4.2e-4, 5e-5, 4.5e-5, 4e-5, 6e-6, 5e-6.
Width of the Gate (w)	1e-7, 5e-7, 1e-6, 4e-6, 6e-6, 1e-5, 5e-5.

Table 4: Monte Carlo Parameters.

Varying the parameters used for the Monte Carlo Analysis for each of the model specified in the section 3 we have simulated for 36 models in total. The results obtained from the Monte Carlo analysis are present in the folder generated from the simulations. The folder is named after the full adder used in the simulation based on the sic jfet model. In the below Figure, we will show the Sample process parameters used for the Monte Carlo Simulations of the Full Adder circuit. These parameters are also shown in the Table 4 above and only one of the four parameters will be varied per simulation.

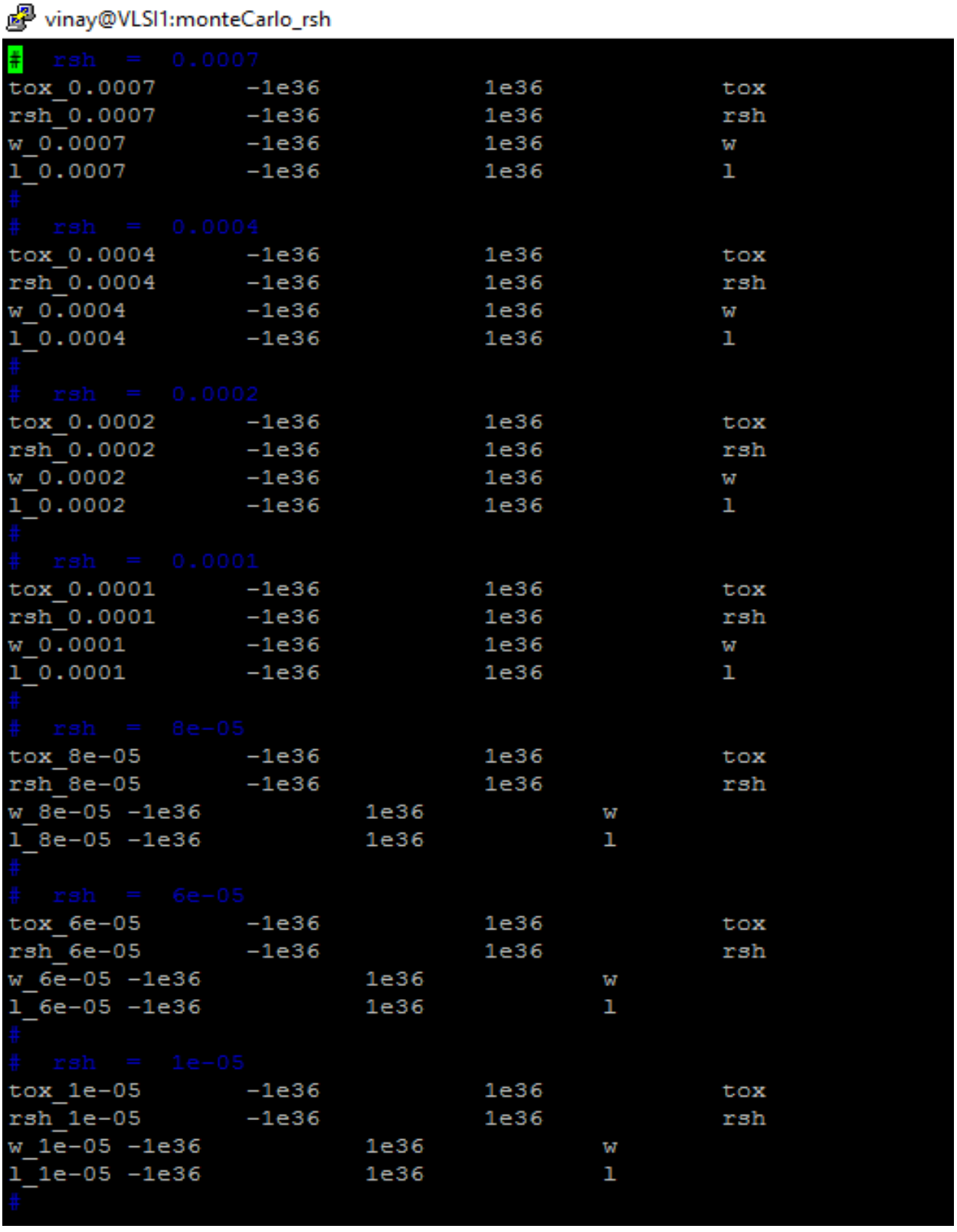

Figure 14: Sample Monte Carlo Process Parameters.

As shown in Figure 14 sheet resistance (rsh) parameter is varied. The other parameters are the mismatch parameters which are specified to be the same to know the effect of the sheet resistance on the Silicon Carbide JFET circuit.

The following Figure 15 will show the Sample Monte Carlo parameters (mcparam) in the Monte Carlo Simulation folder.

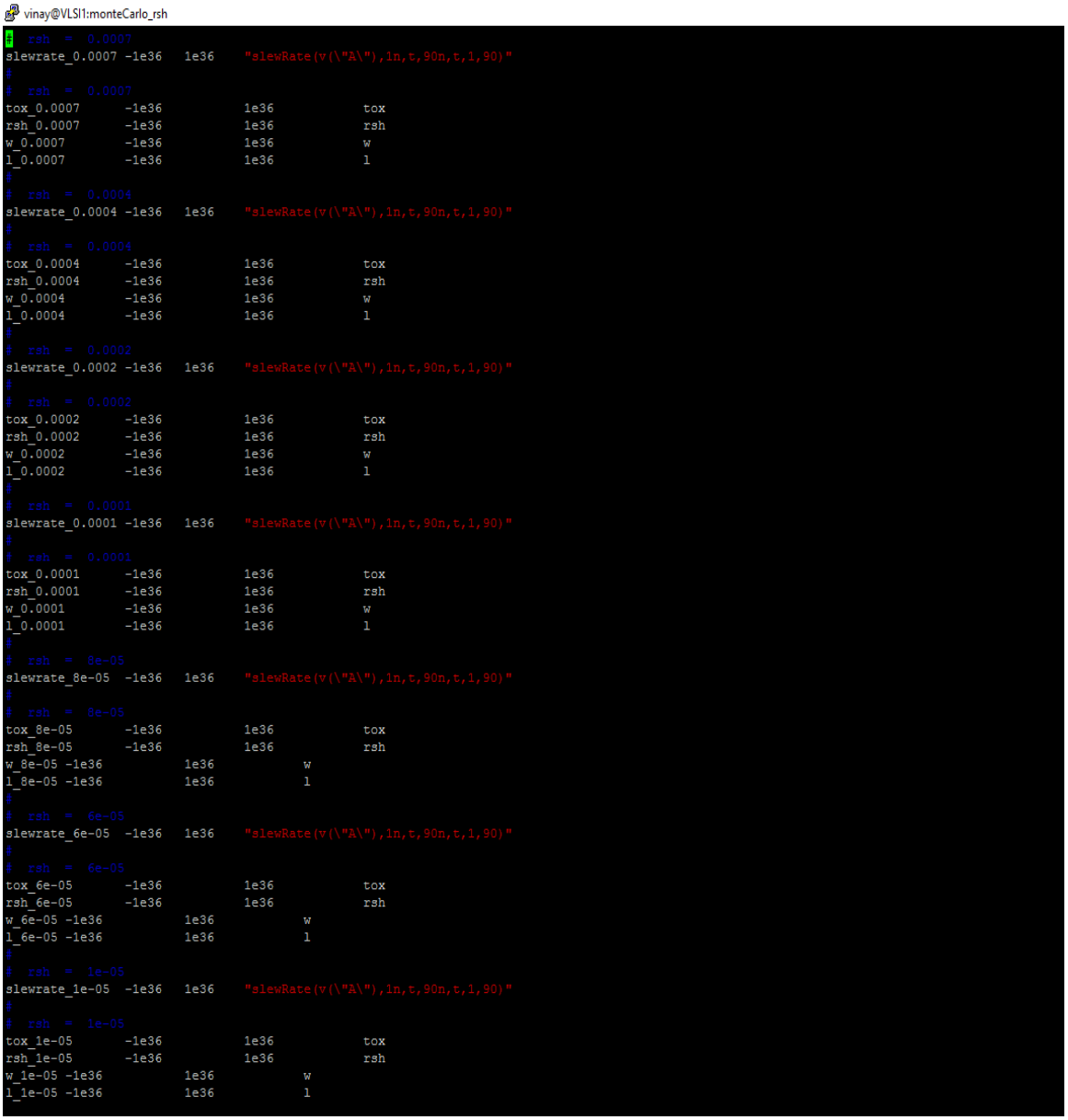

Figure 15: Sample Monte Carlo Parameters.

The difference between the Monte Carlo process parameters and the Monte Carlo Parameters is the export expression is given in the Monte Carlo parameters and will show the parameters that are used for the execution of the export statement. Here, from the Figure 15 we can see that the export statement along with the parameters tox, rsh, l and w. The slew rate is calculated using this export statement which is given in the monte carlo analysis statements in the spectre file of the full adder.

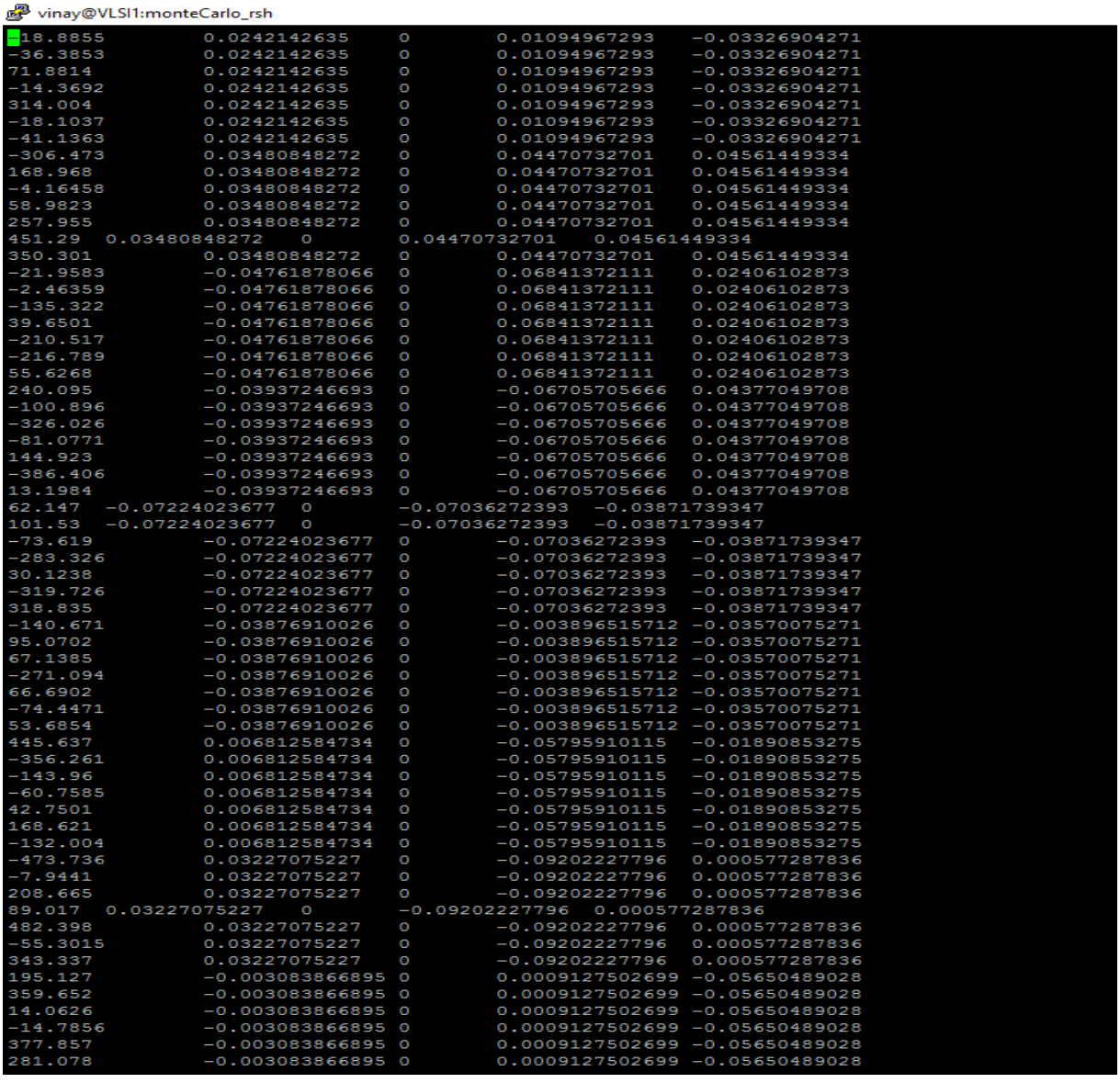

Figure 16: Sample Monte Carlo Analysis Data

The Figure 16 will show you the data generated during the monte carlo analysis which contains the first column as slew rate the export statement followed by the values of the oxide thickness, sheet resistance, length and width parameters. These are varied using the Gaussian distribution function.

Gaussian distribution function also considered as the bell-curve distribution. It has the maximum value at the mean value of the distribution and the value decreases with the increase in the x-axis parameter value [35]. Here the x-axis parameter value is considered as time [35].

For a variable "Z" it is said to be in a Gaussian function if it's PDF is of the following format as shown in the below expression 6 [35].

$$F_Z(z) = \frac{1}{\sqrt{2\pi}} \exp\{-z^2/2\} \qquad \text{for all } z \in R. \qquad 6$$

The Total Area formed by the PDF of the function is equal to 1.

7.1 Transient Analysis Data for the SiC JFET Models:

The following Figures will show the transient analysis data obtained from the monte carlo analysis of the Full adder circuit by varying the parameters of the length, width, oxide thickness and the sheet resistance.

We have obtained the following data from the synthesis tool of Cadence call as Viva (Virtuoso Visualization and Analysis tool). This tool takes the input the .raw file which is being generated during the synthesis of the full adder along with the output file (.out). This .raw file when used in the Cadence viva tool it will generate the waveforms for the given .raw file. Here, we use these .raw file and show the transient analysis for all the SiC JFET models. As shown in

the given Figures the parameter varied will be on the left hand side of the graph and the file folder is specified under the browser tab.

The following Figures 17-20 are for the transient analysis of the Full Adder for the temperature 25˚C and radial device distance from the center of the wafer of 0 cm.

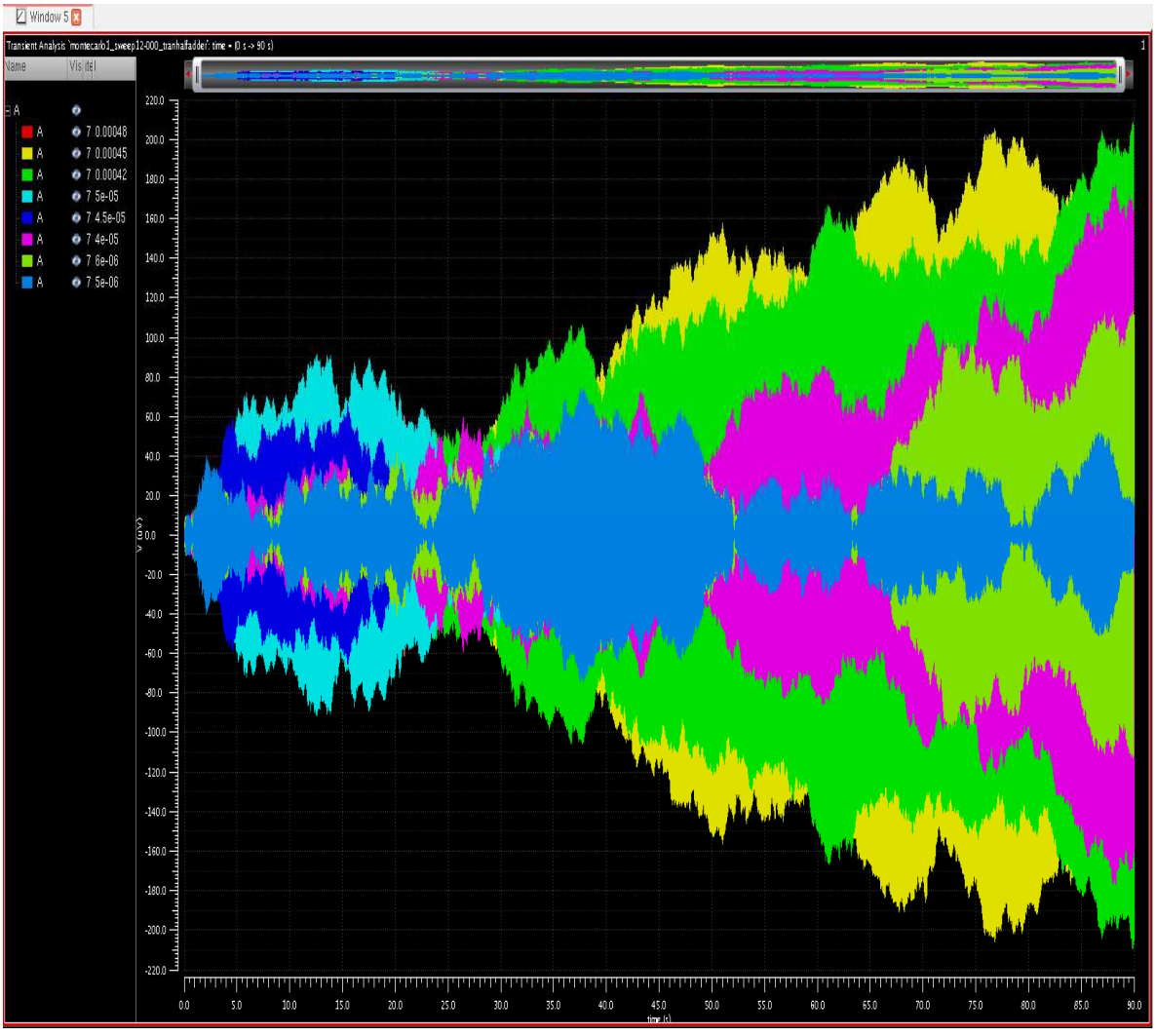

Figure 17: Transient Analysis for the variations of the length parameter (t25_r0_l).

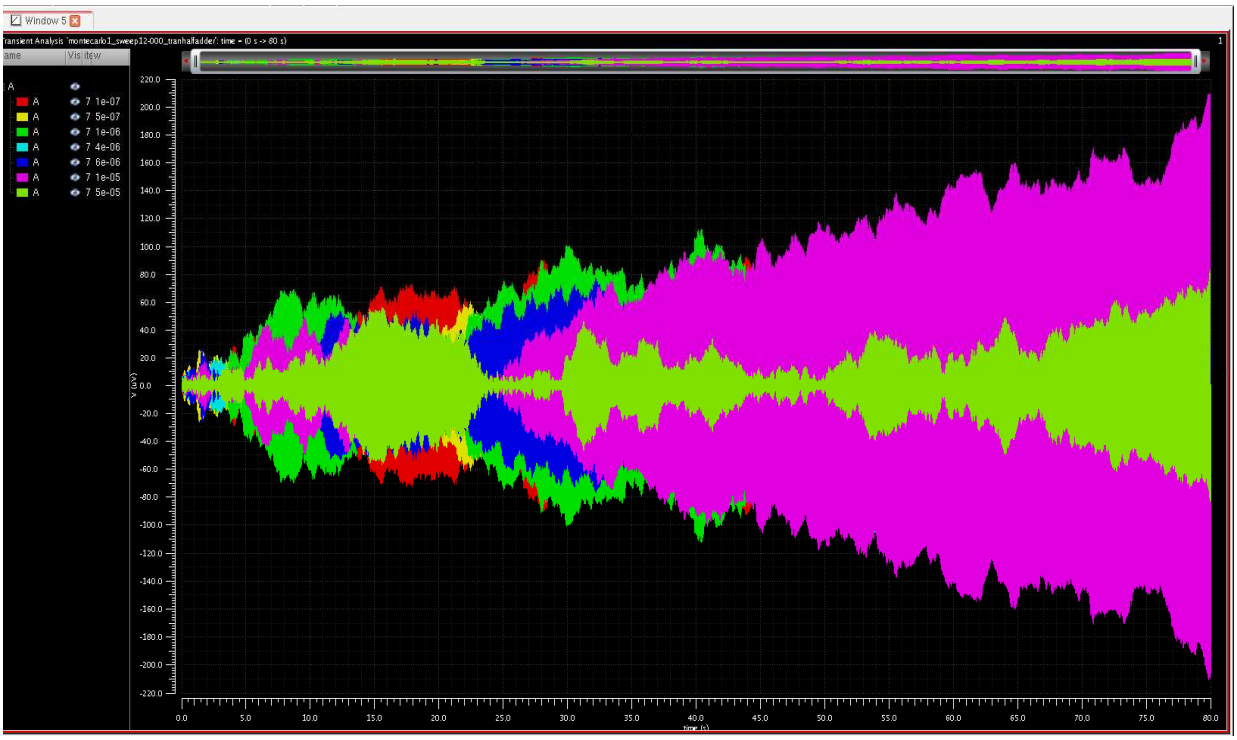

Figure 18: Transient Analysis for the variations of the width parameter (t25_r0_w).

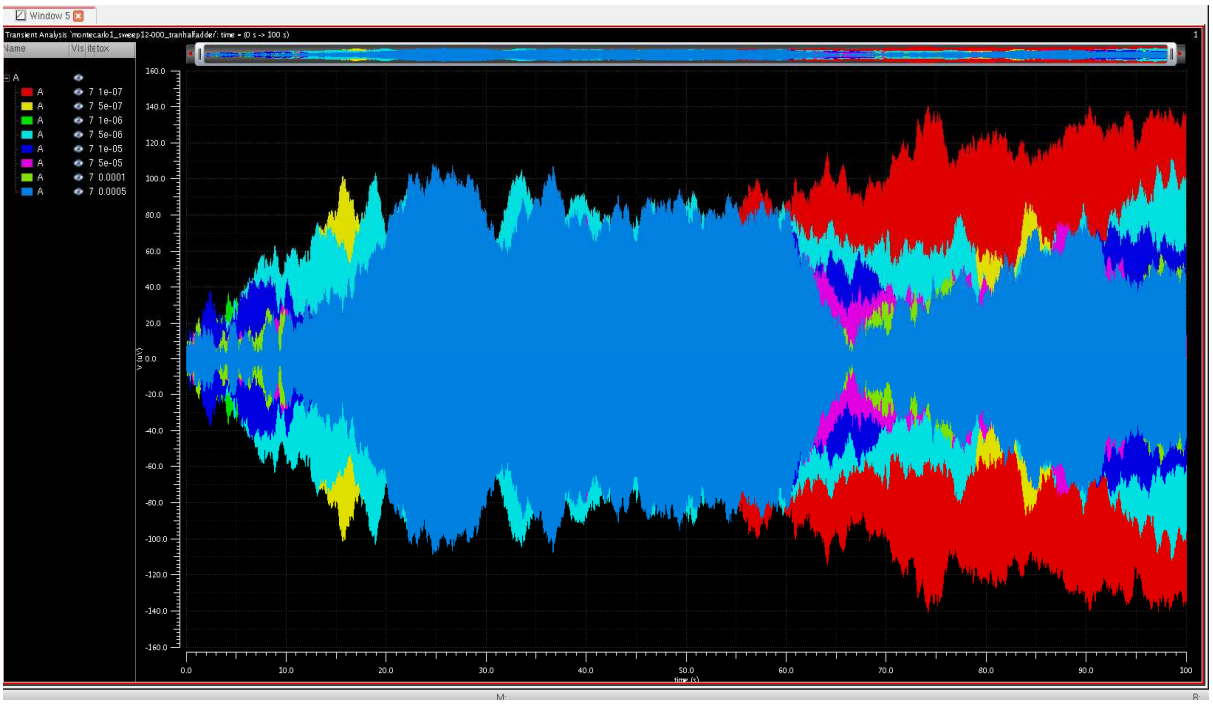

Figure 19: Transient Analysis for the variations of the Oxide thickness parameter (t25_r0_tox).

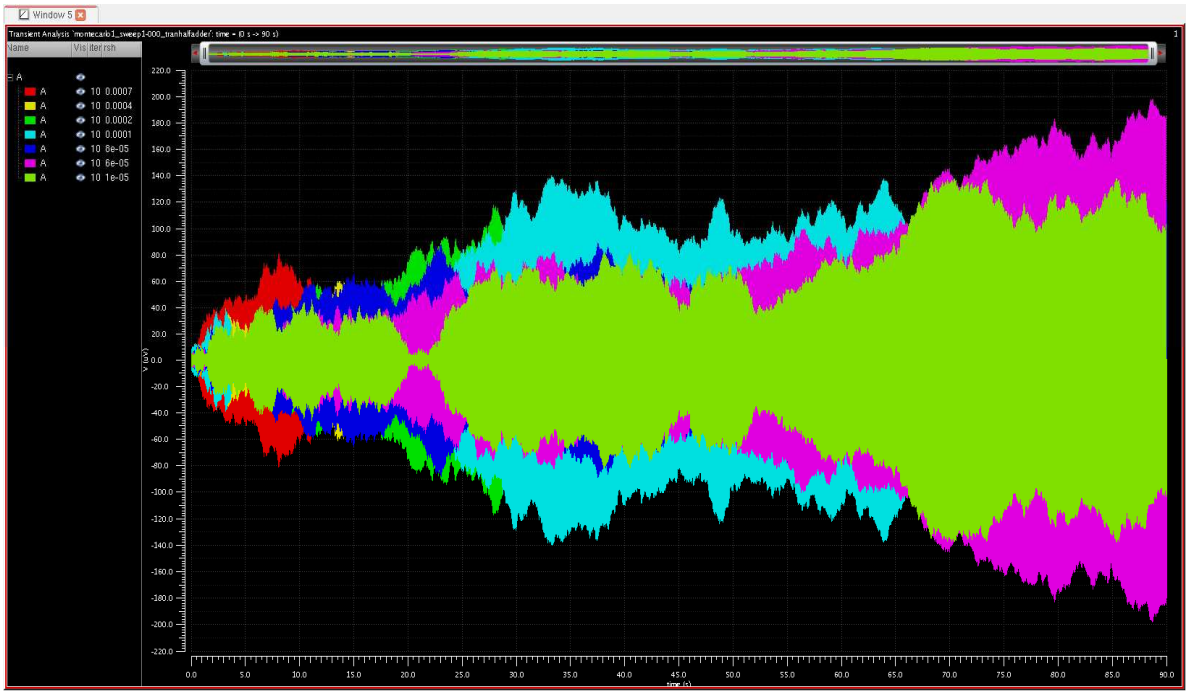

Figure 20: Transient Analysis for the Variations of the Sheet resistance parameter (t25_r0_rsh).

The Figures 17 – 20 are the transient analysis obtained from the variations of the length of the gate, width of the gate, oxide thickness and the sheet resistance parameters during the monte carlo simulations respectively. These parameters values are the values given in the table 4. As shown in the Figures 17-20 we can consider the region of operation for each of the parameter and can conclude the parameter value for this model. Here we can say that ideal transient analysis can obtained for the length parameter at l=5e-6 from Figure 17, for the width parameter it is 5e-5 from Figure 18, for the oxide thickness it is 1e-5 from Figure 19 and for the sheet resistance it is at 8e-5 from Figure 20.

The following Figures 21-24 are for the transient analysis for the full adder circuit at the temperature of 25˚C and the radial device distance from the center of the wafer of 1.5 cm

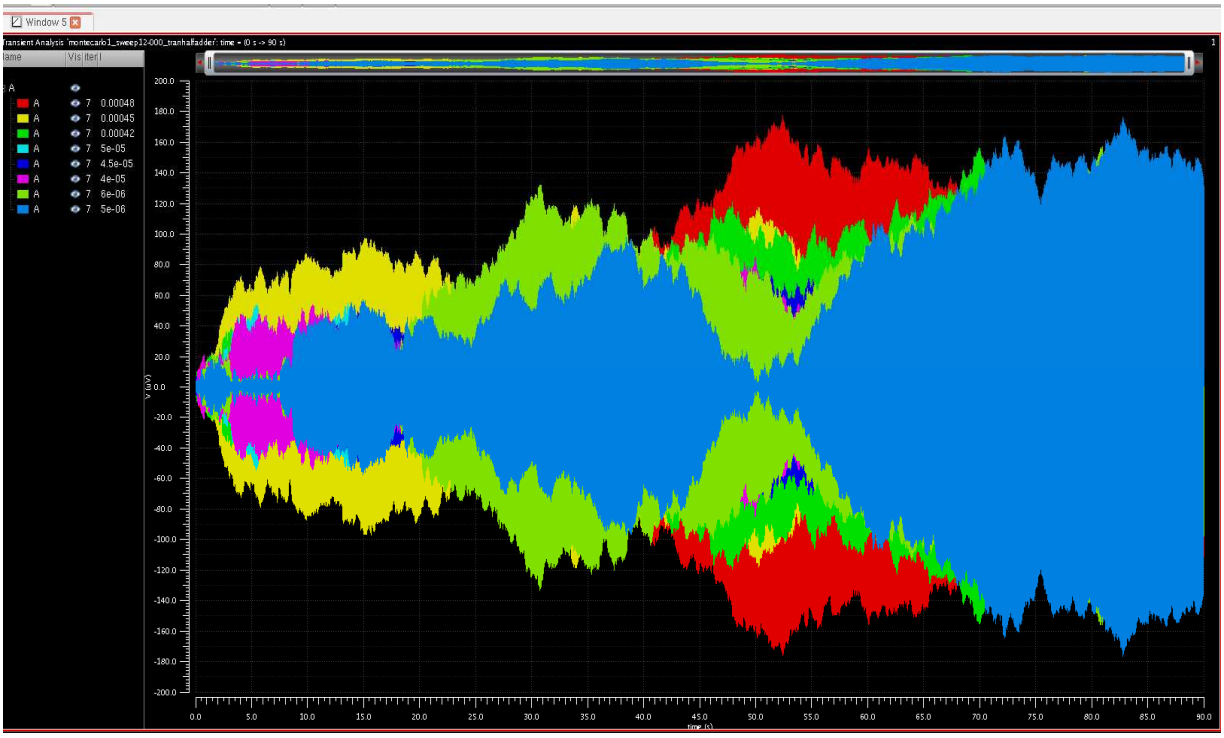

Figure 21: Transient Analysis for the Variations of the length parameter (t25_r1half_l).

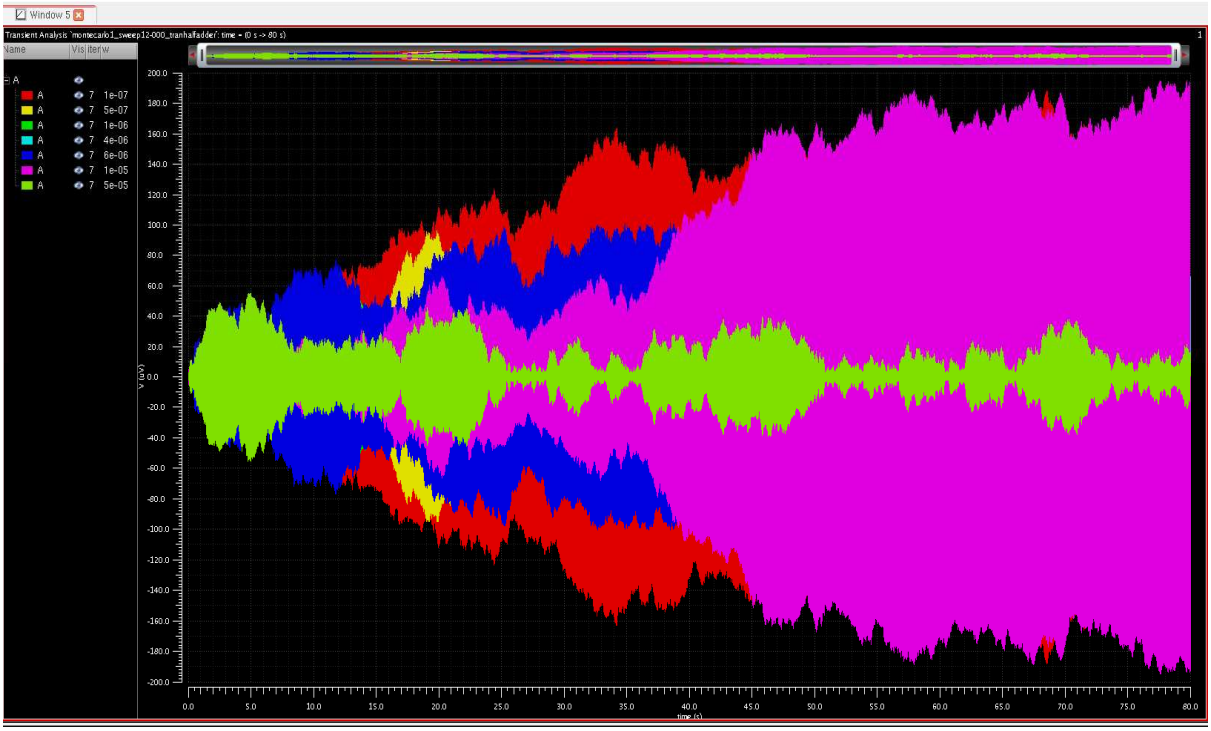

Figure 22: Transient Analysis for the Variations of the width parameter (t25_r1half_w).

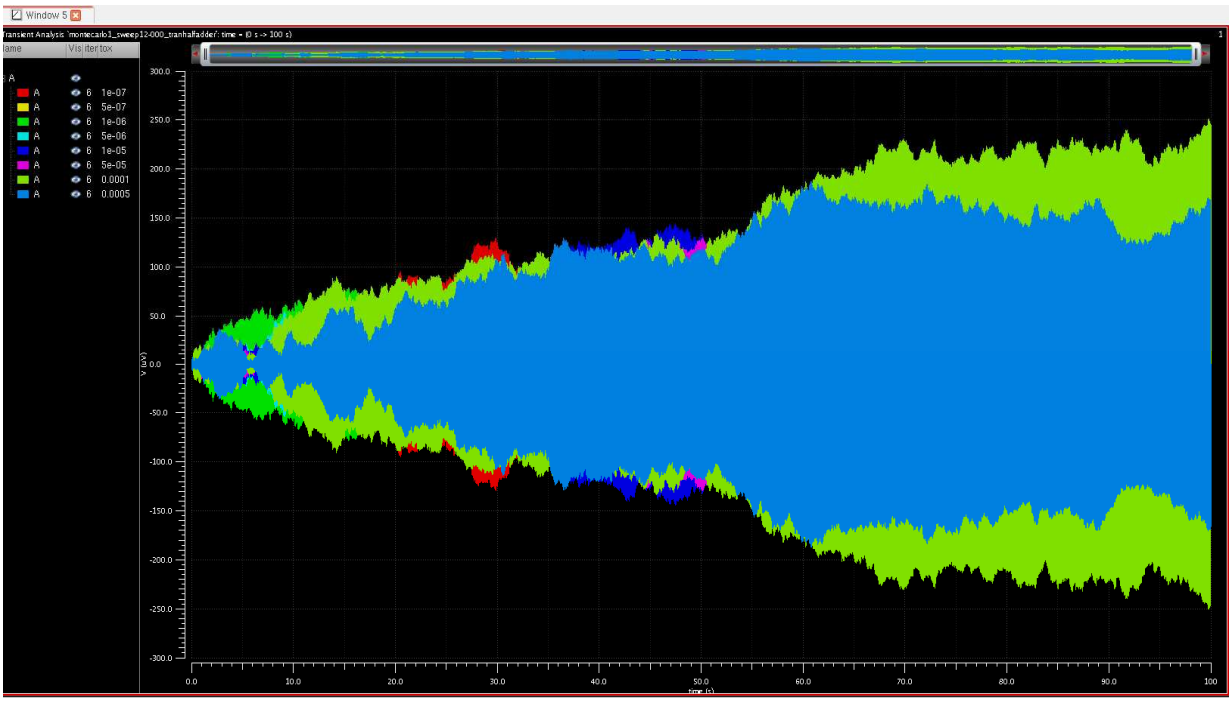

Figure 23: Transient Analysis for the Variations of the Oxide Thickness parameter (t25_r1half_tox).

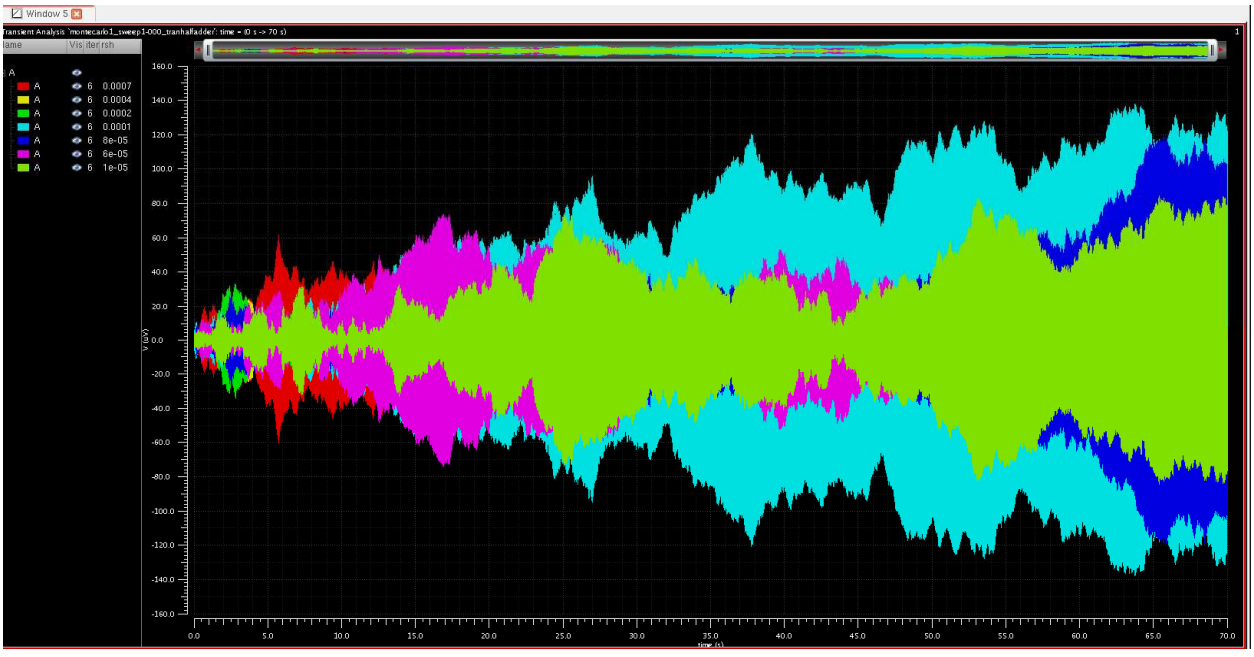

Figure 24: Transient Analysis for the Variations of the Sheet resistance parameter (t25_r1half_rsh).

As shown in the Figures 21-24 the region of operation can be considered for each of the parameters based on the Analysis obtained by the variations in each of the parameter values. From Figure 21 we can obtain the value of length parameter for the ideal operation of the circuit is 4e-5. In the same way for the width it is 5e-5 from Figure 22, for the oxide thickness it is 1e-6 from Figure 23 and for the sheet resistance 7e-4 from Figure 24. These parameter values are adjudged ideal from the voltage values obtained against the time during the transient analysis.

The Figures 25-28 are for the transient analysis for the full adder circuit at the temperature of 25˚C and the radial device distance from the center of the wafer of 3 cm.

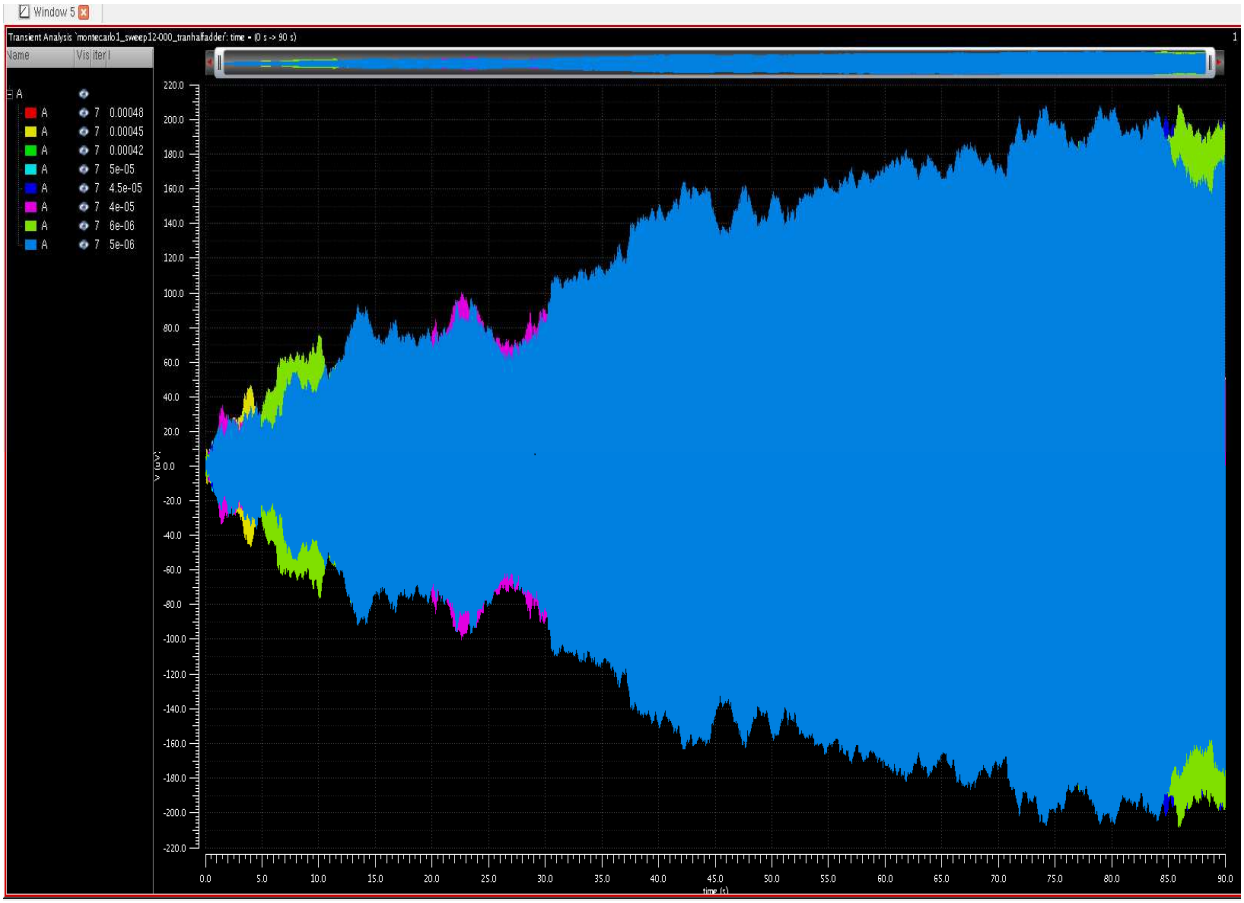

Figure 25: Transient Analysis for the Variations in the length parameter (t25_r3_l).

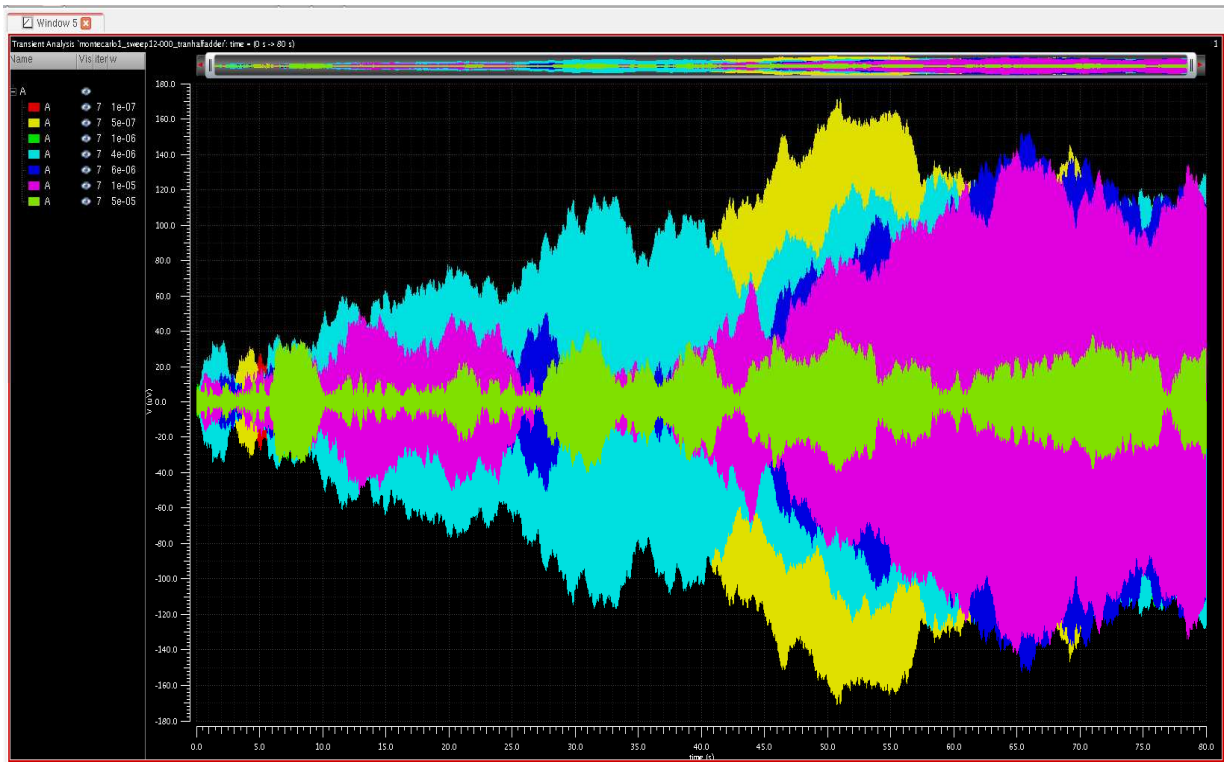

Figure 26: Transient Analysis for the variations in the width parameter (t25_r3_w).

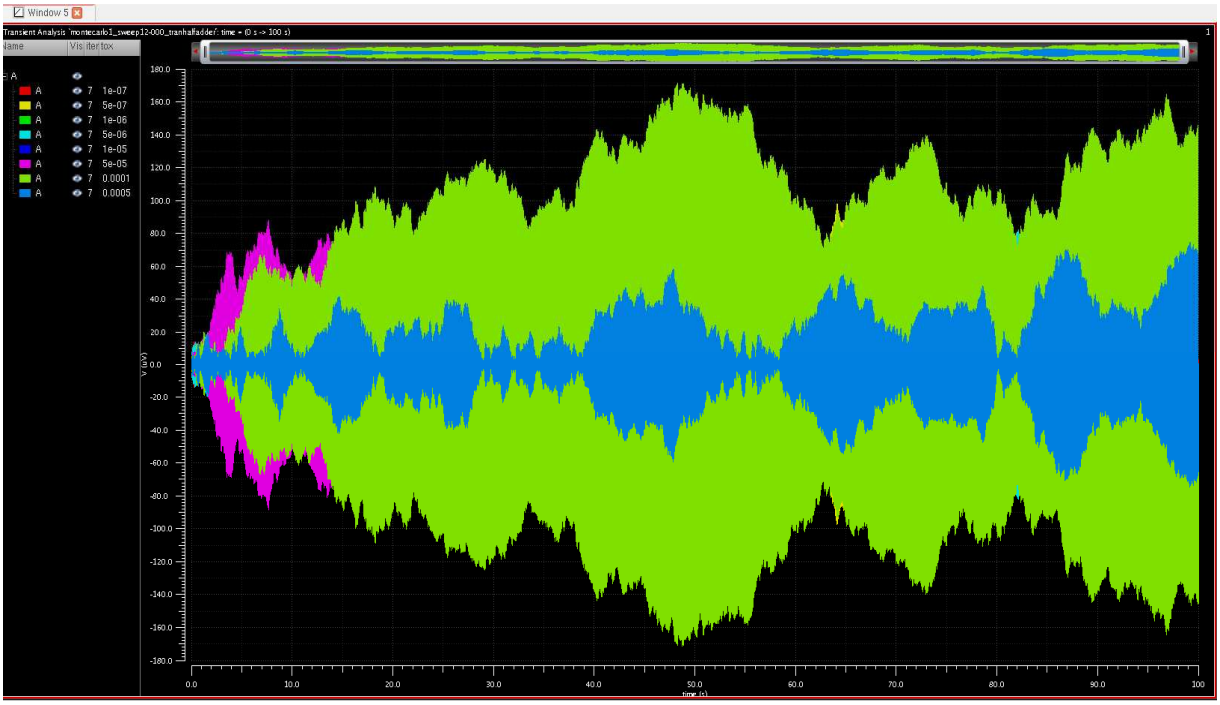

Figure 27: Transient Analysis for the Variations of the Oxide Thickness parameter (t25_r3_tox).

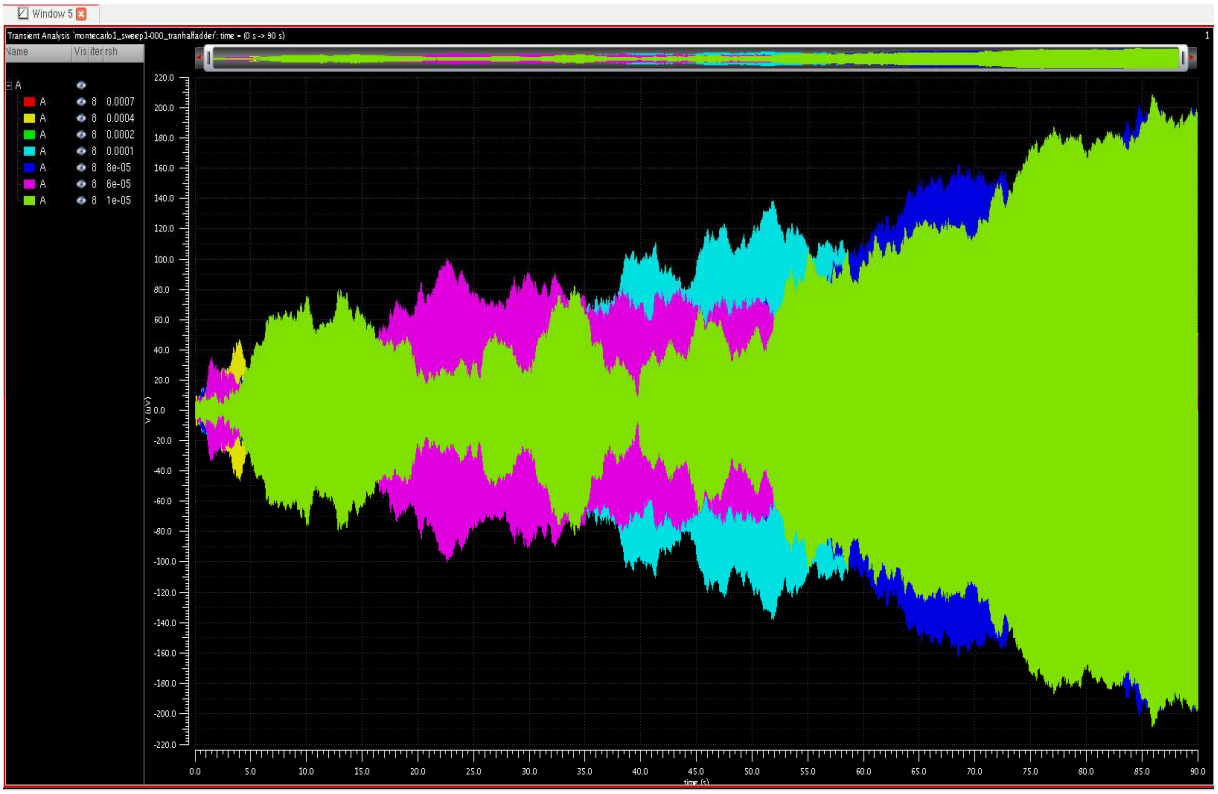

Figure 28: Transient Analysis for the Variations of the Sheet Resistance parameter (t25_r3_rsh).

As shown in the Figures 25-28 each varied parameter behaves in a different manner and the ideal operation of the circuit can be taken as a result. This ideal value of each parameter vary with each operation as the temperature is being varied with the radial distance. Here, we can say that the ideal parameter values are 5e-5 for the length, 1e-6 for the width, 5e-4 for the oxide thickness and 7e-4 for the sheet resistance. These parameter values will give a moderate monte carlo analysis for the given circuit model.

For the Transient Analysis for the model of having temperature constraint at 300 ˚C and the radial device distance from the center of the wafer constrain at 0 cm we obtain the following transient analysis of Figures 29 -32.

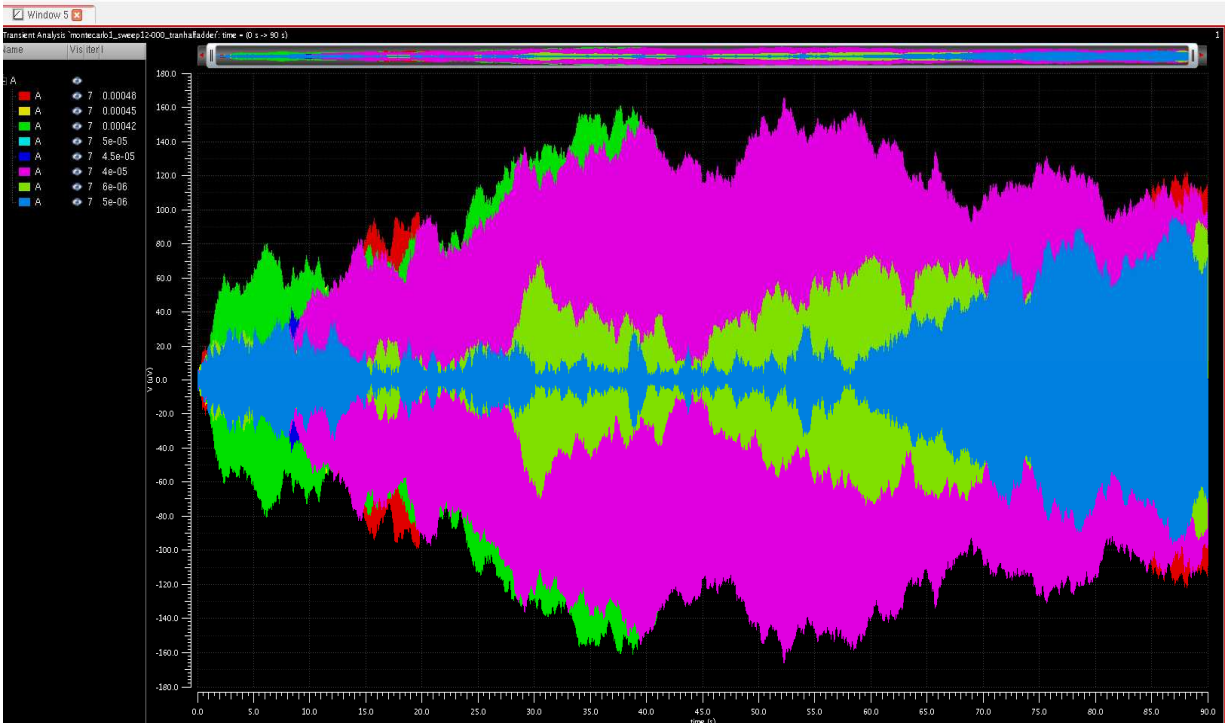

Figure 29: Transient Analysis for the length parameter variations (t300_r0_l).

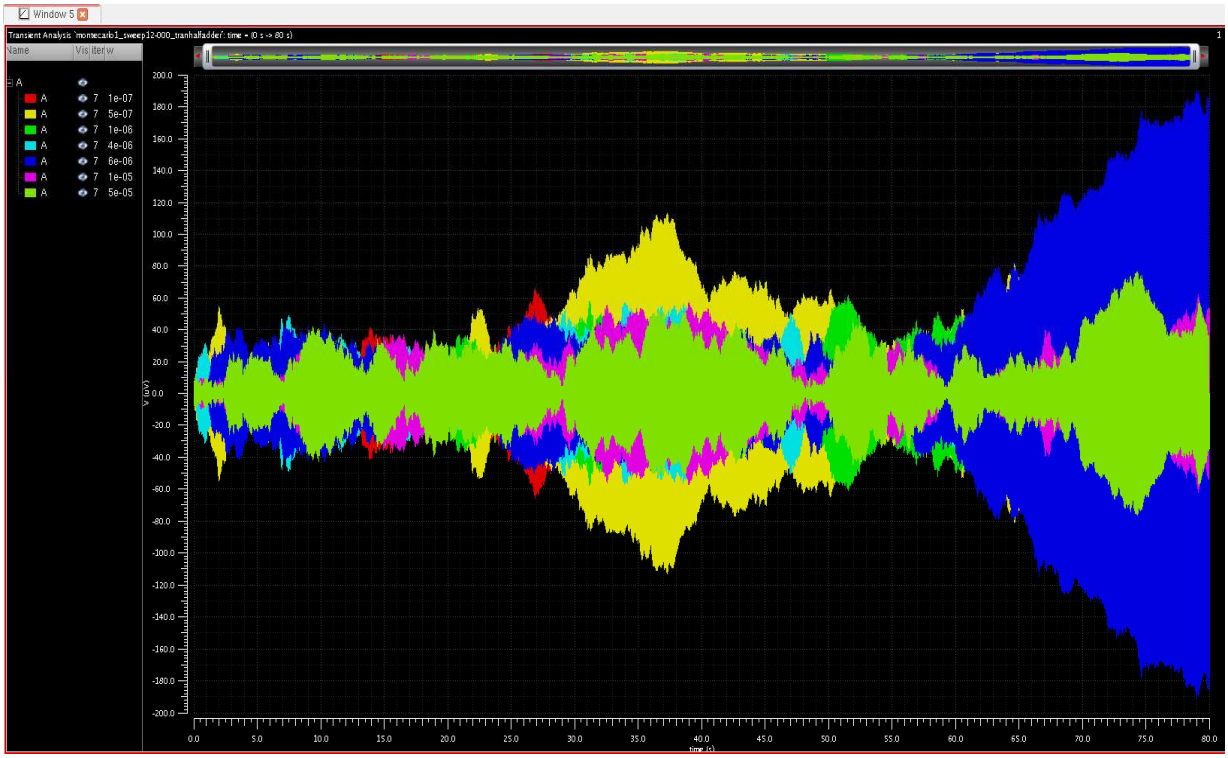

Figure 30: Transient analysis for the Width parameter variations (t300_r0_w).

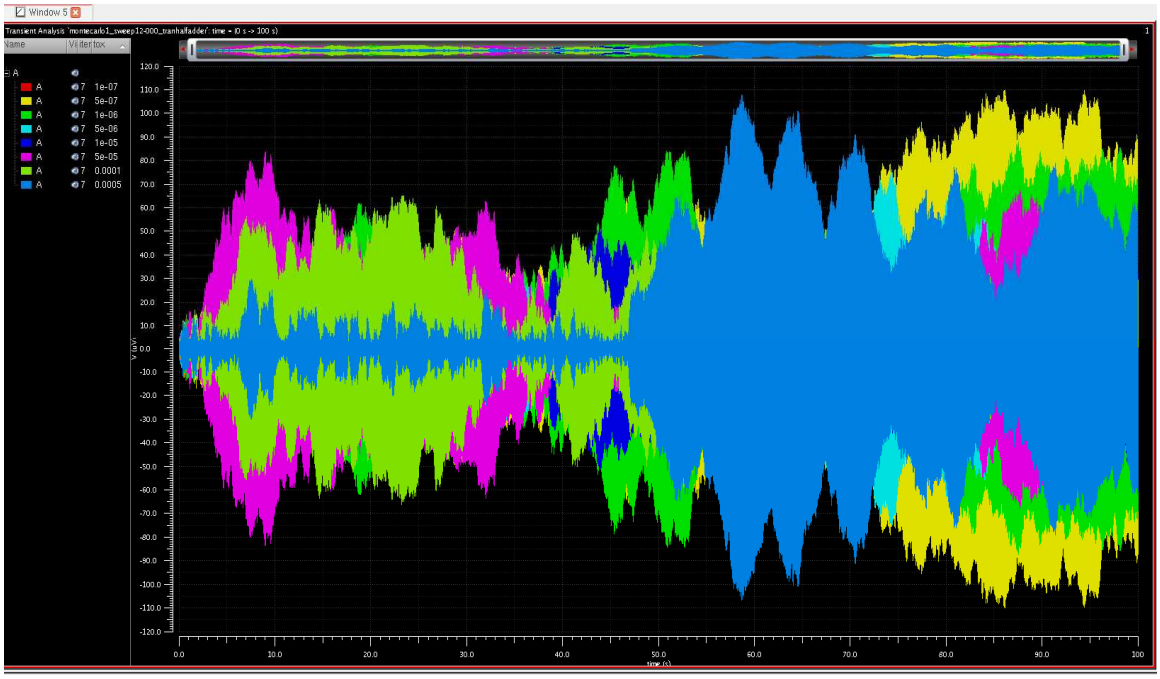

Figure 31: Transient analysis for the Variation in the Oxide thickness parameter (t300_r0_tox).

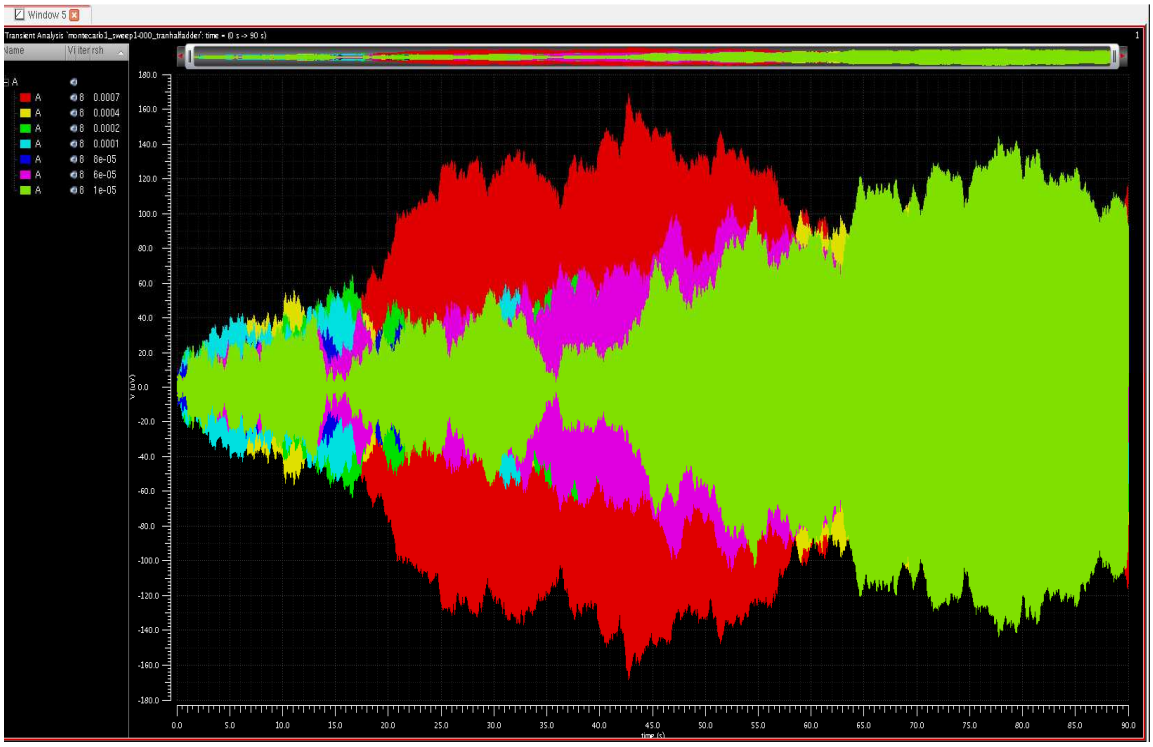

Figure 32: Transient Analysis for the Variations in the Sheet resistance parameter (t300_r0_rsh).

The Figures 29 – 32 are the transient analysis obtained from the variations of the length of the gate, width of the gate, oxide thickness and the sheet resistance parameters during the monte carlo simulations respectively. Here we can say that ideal transient analysis can obtained for the length parameter at l=4.5e-4 from Figure 29, for the width parameter it is 1e-6 from Figure 30, for the oxide thickness it is 1e-7 from Figure 31 and for the sheet resistance it is at 8e-5 from Figure 32.

In the similar way, we have obtained the transient analysis for the model having the temperature at 300˚C and the radial device distance from the center of the wafer parameter value at 1.5 cm as shown in the Figures 33-37.

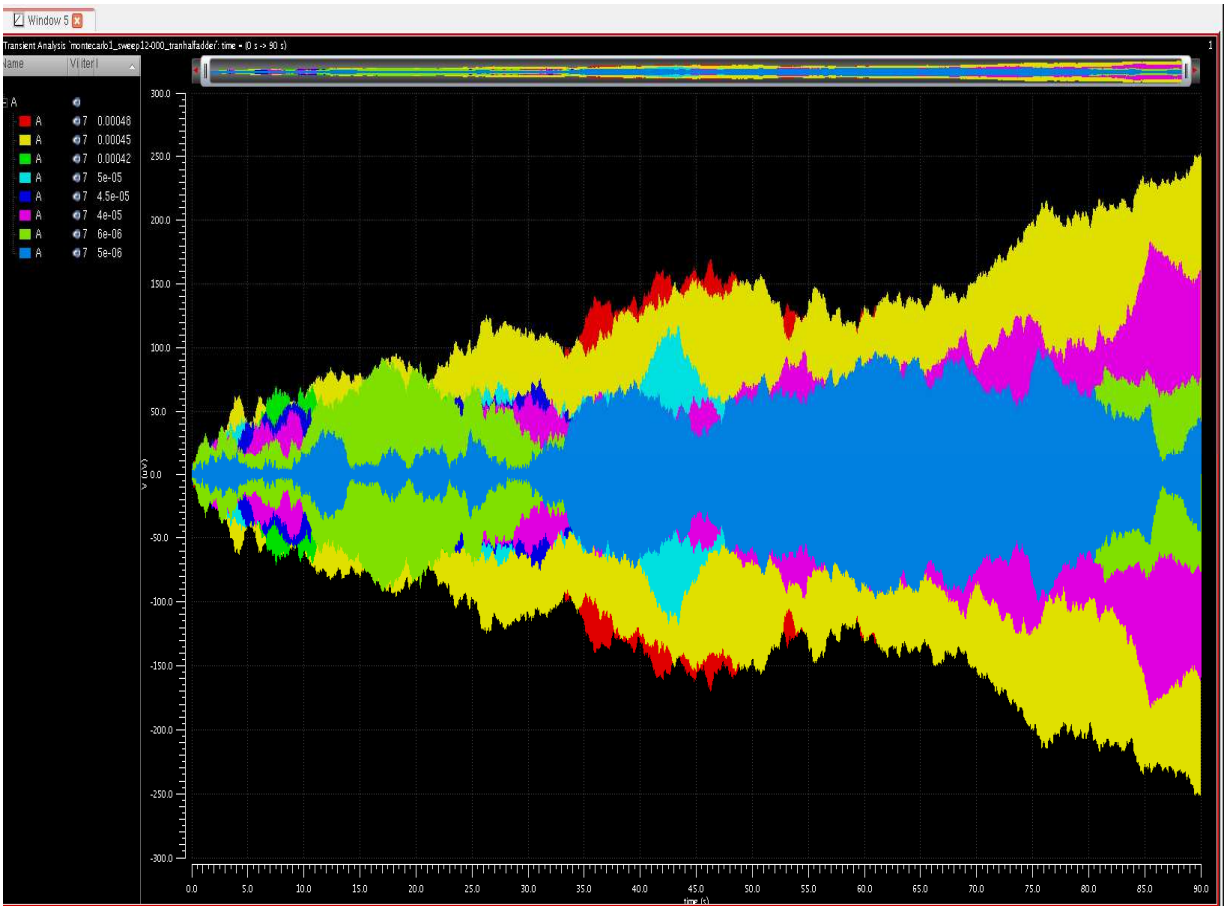

Figure 33: Transient Analysis obtained by the variation of length parameter (t300_r1half_l)

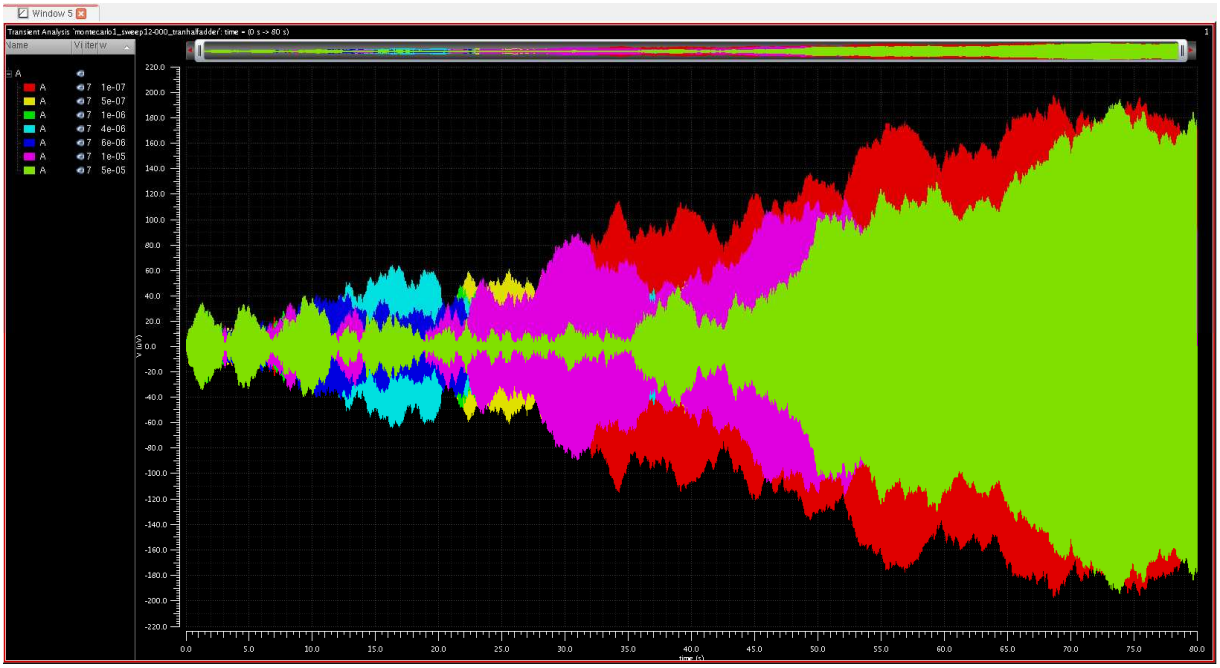

Figure 34: Transient Analysis obtained by the variation of width parameter (t300_r1half_w).

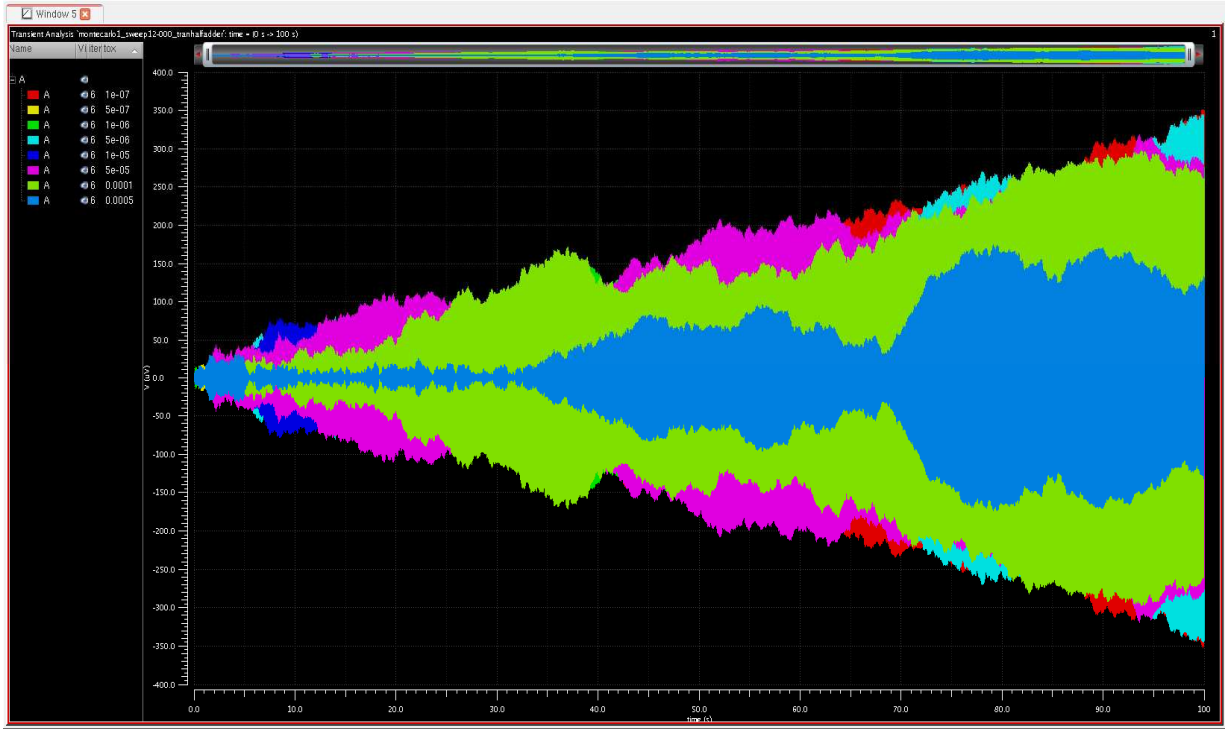

Figure 35: Transient Analysis obtained by the variation of oxide thickness parameter (t300_r1half_tox)

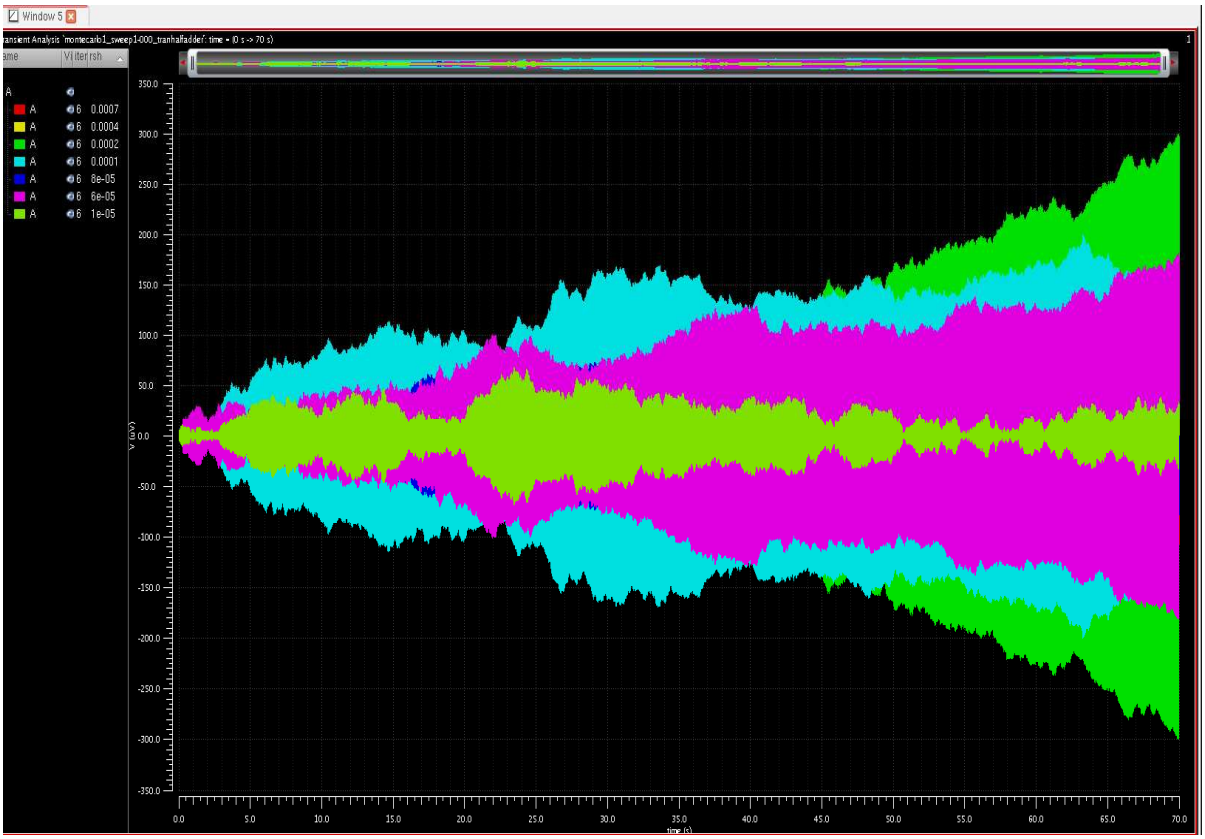

Figure 36: Transient Analysis obtained by the variation of sheet resistance parameter (t300_r1half_rsh)

As shown in the Figures 33-36 the region of operation can be considered for each of the parameters based on the Analysis obtained by the variations in each of the parameter values. For the variation in the length parameter the ideal operation can be seen when l=5e-6 and in the similar way the other parameters from the transient analysis can be obtained as w=6e-6, tox=5e-7 and the rsh value can be adjudged as 2e-4.

The model having the temperature at 300˚C and the radial device distance parameter at 3 cm exhibits following transient analysis when the model is subjected to the changes in the length of the gate, width of the gate, oxide thickness and also the sheet resistance. These are captured using Cadence Viva and are as shown in Figures 37-40.

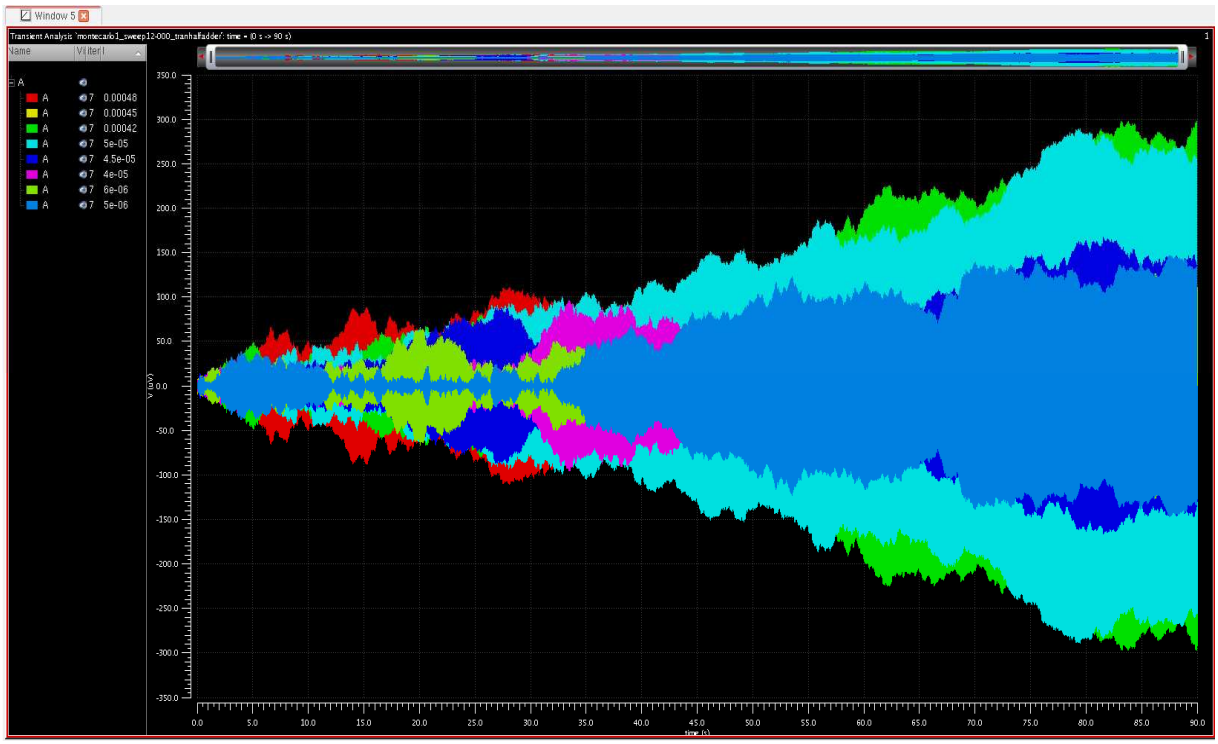

Figure 37: Transient analysis obtained for length parameter variation (t300_r3_l).

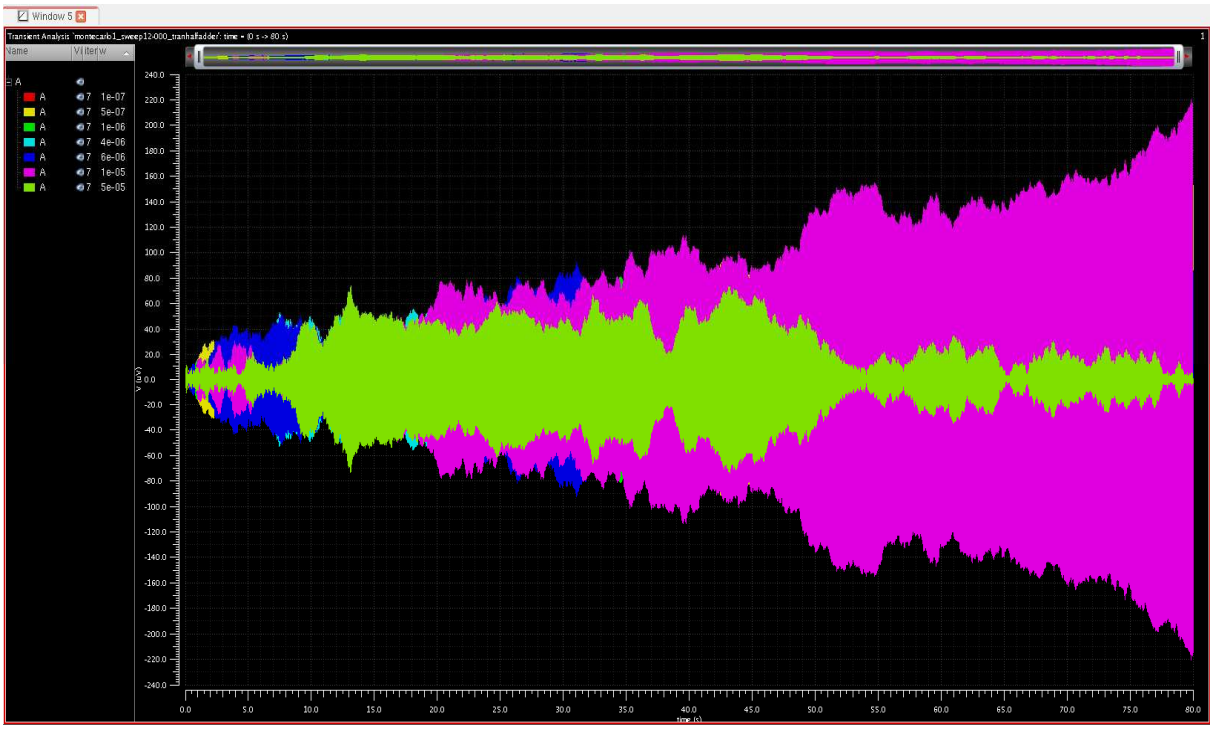

Figure 38: Transient analysis obtained for width parameter variation (t300_r3_w).

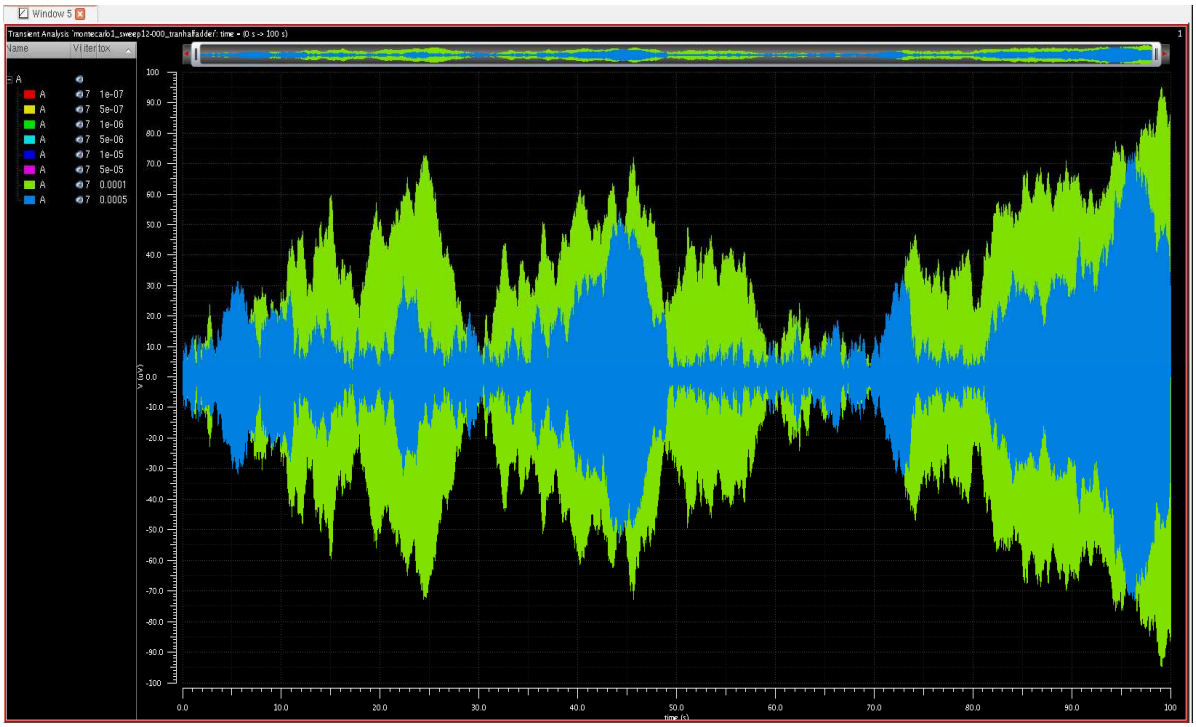

Figure 39: Transient analysis obtained for oxide thickness parameter variation (t300_r3_tox).

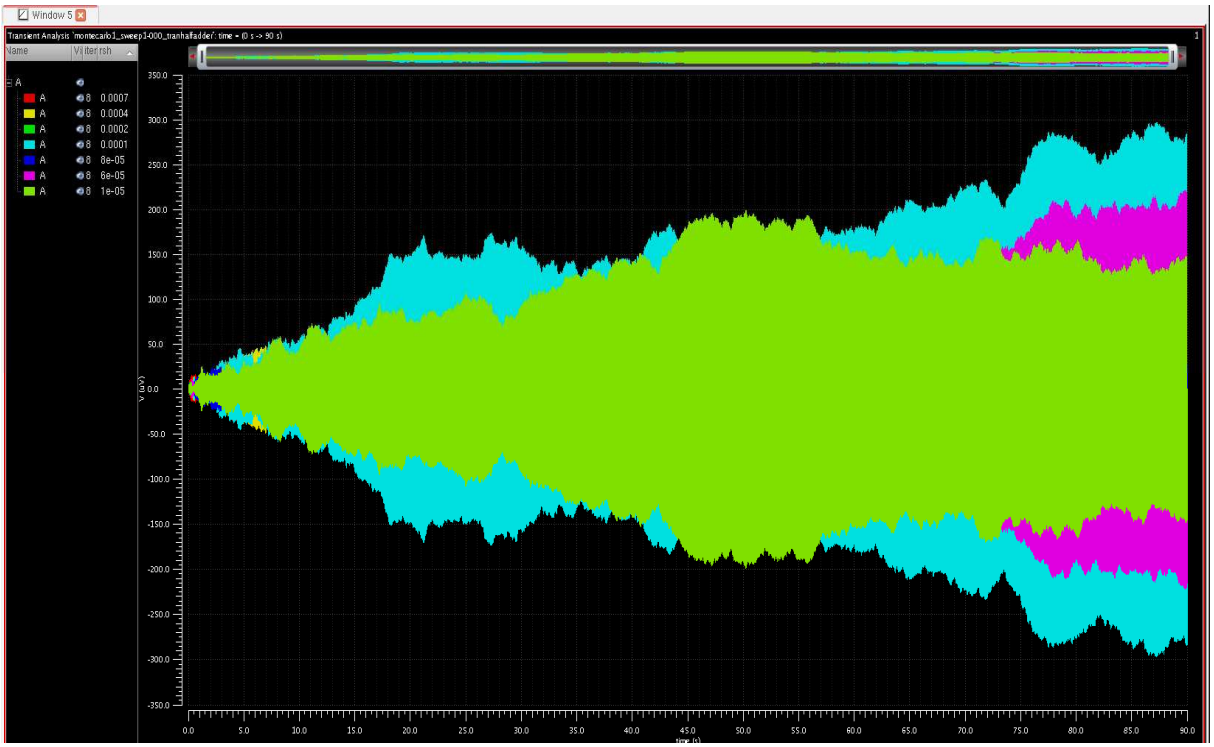

Figure 40: Transient analysis obtained for sheet resistance parameter variation (t300_r3_rsh).

These parameter variations provide us the detail analysis of the characteristics of the circuit. We can choose the ideal parameter for the operation from the transient analysis obtained for each parameter. From the Figure 37 we can say that the ideal condition is at 4.5e-4 for the length parameter. In the similar way from Figure 38 w=4e-6, from Figure 39 tox=any value excepts 1e-6 and 5e-4 and from Figure 40 rsh=7e-4. Here from the oxide thickness transient analysis all the values excepts the two values are ideal for the operation of the SiC JFET circuit as all the values show a decent amount of voltage when compared to the values of 1e-6 and 5e-4 which show a variable voltage over the time period.

The following Figures 41-44 are for the spice model having the temperature of 500˚C and the radial device distance parameter as 0 cm.

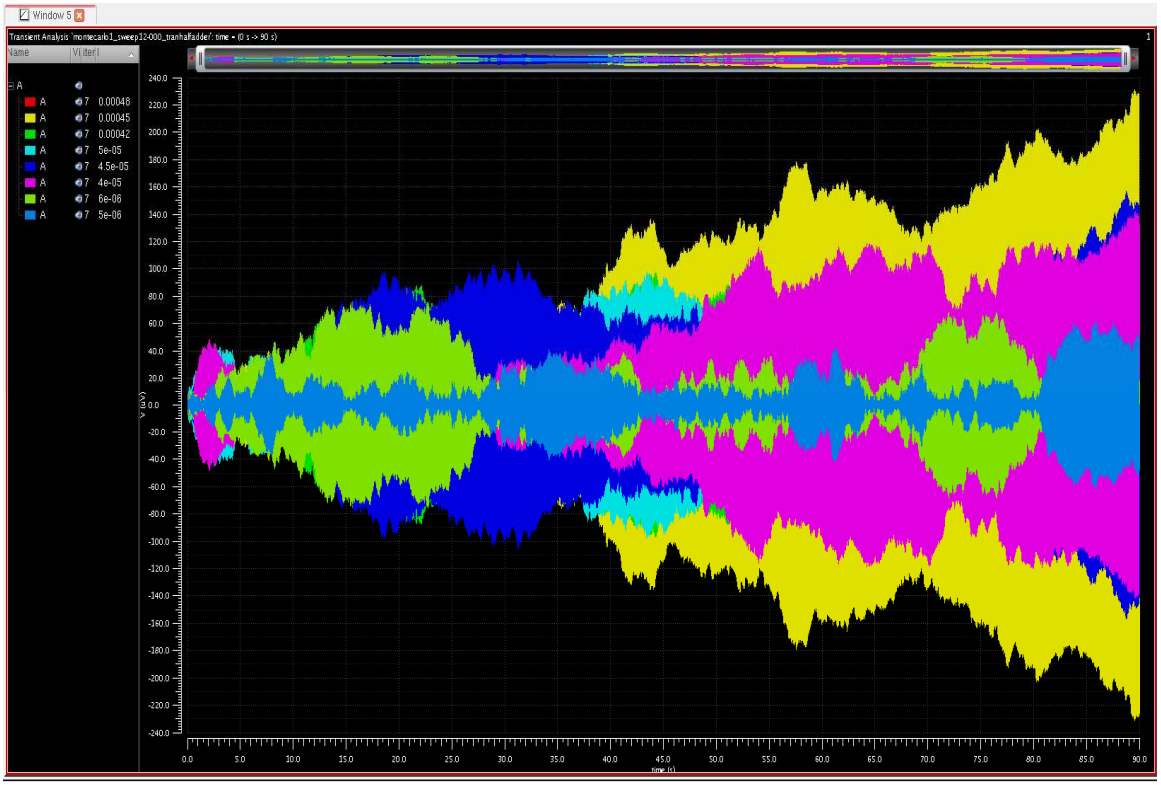

Figure 41: Transient Analysis obtained for length parameter variation (t500_r0_l).

Figure 42: Transient Analysis obtained for width parameter variation (t500_r0_w).

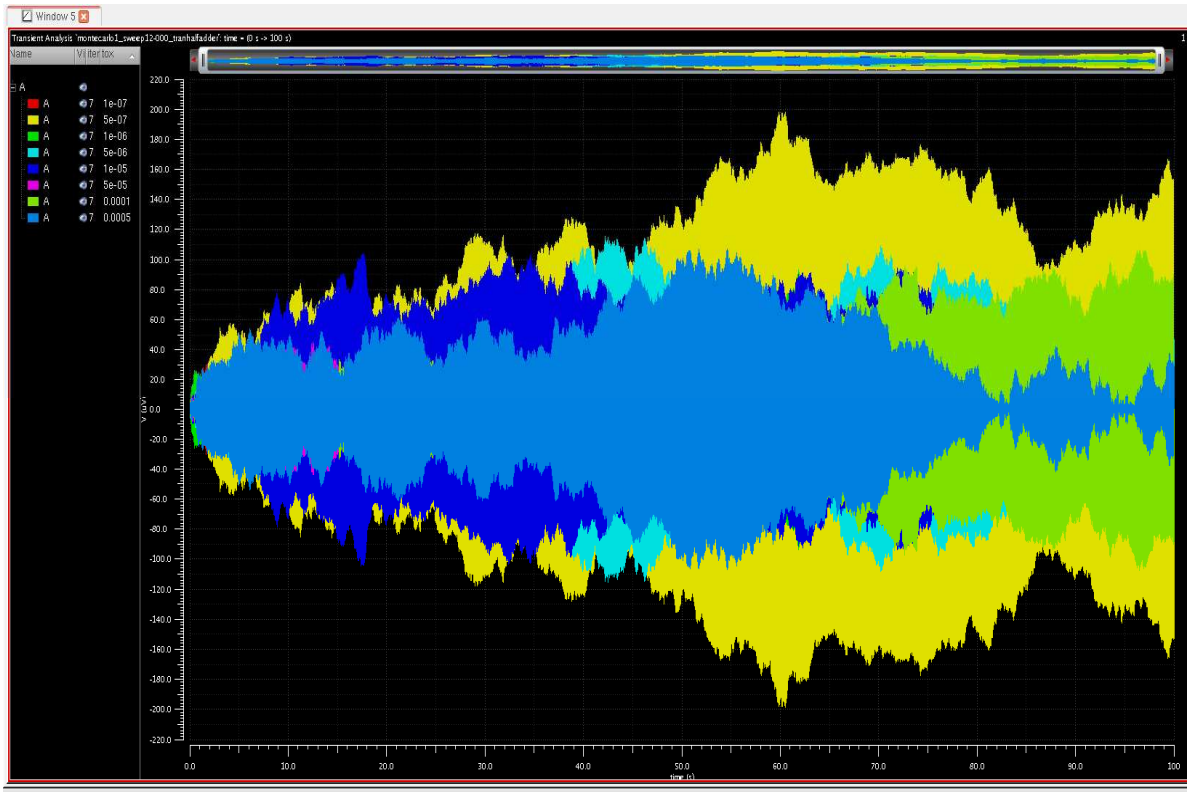

Figure 43: Transient Analysis obtained for oxide thickness parameter variation (t500_r0_rsh).

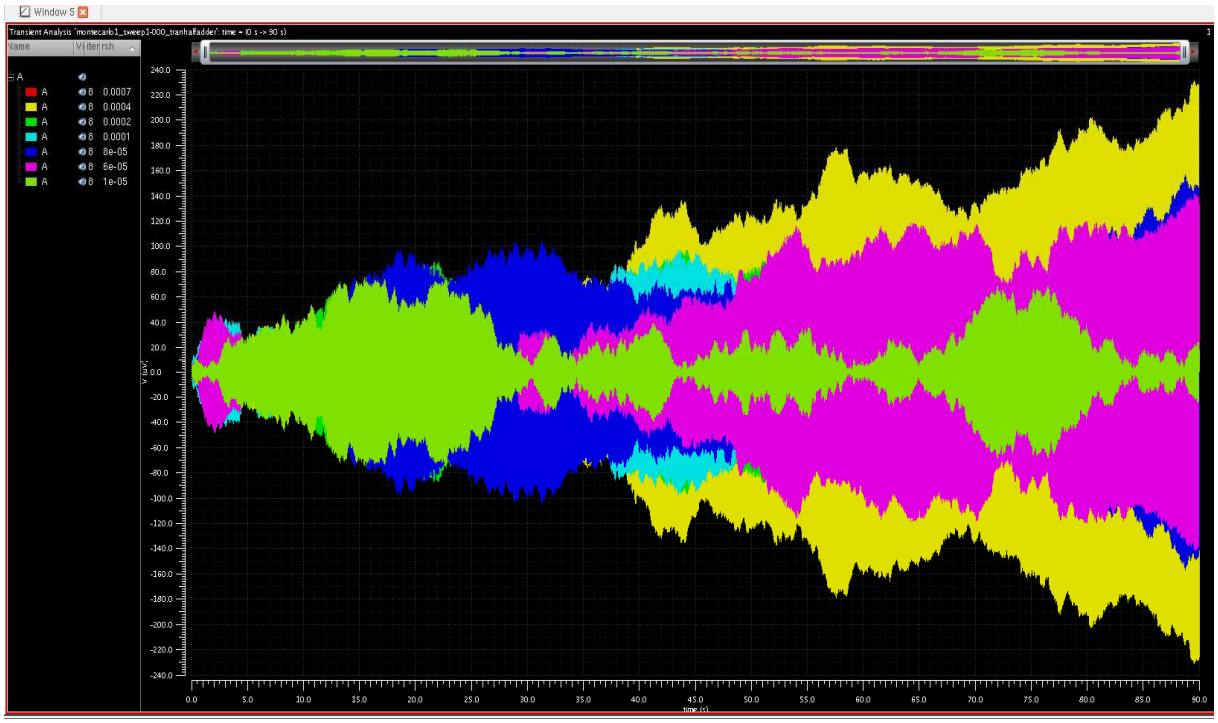

Figure 41: Transient Analysis obtained for sheet resistance parameter variation (t500_r0_rsh).

The transient analysis for the Full adder at 500˚C and r=0 cm by varying the parameters of length, width, oxide thickness and sheet resistance we can see that each of them have unique effects on the SiC JFET circuit. The ideal parameter for obtaining better results can be taken from the transient analysis. From Figure 41 we can see that the parameter length can be l=5e-6 for an ideal operation of the circuit. In the similar manner from Figure 42 for the parameter width w=6e-6, from Figure 43 for the parameter oxide thickness tox=1e-4 and from Figure 44 for the parameter sheet resistance rsh=7e-4.

Now coming to the spice model of SiC JFET at the temperature of 500˚C and the radial device distance of 1.5 cm we have obtained the following transient analysis Figures 45-48 by varying the parameters of length, width, oxide thickness and sheet resistance of the JFET circuit. We can obtain the ideal functioning of the JFET for each parameter by analyzing the transient analysis.

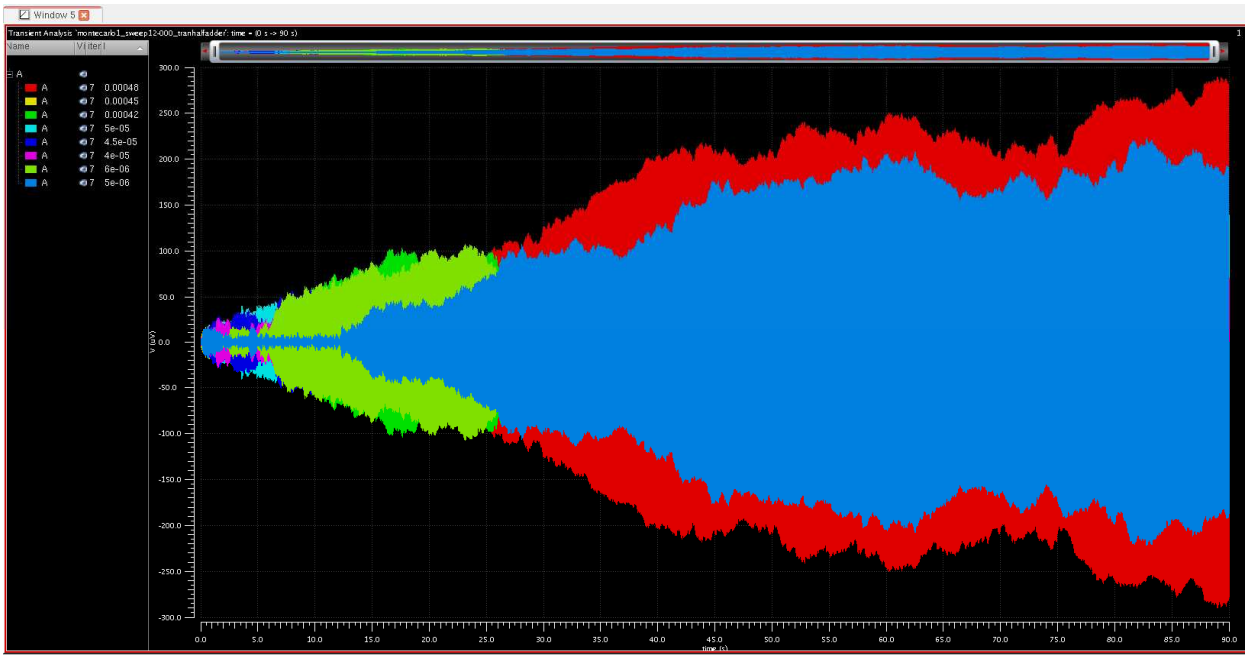

Figure 45: Transient Analysis obtained for length parameter variation (t500_r1half_l).

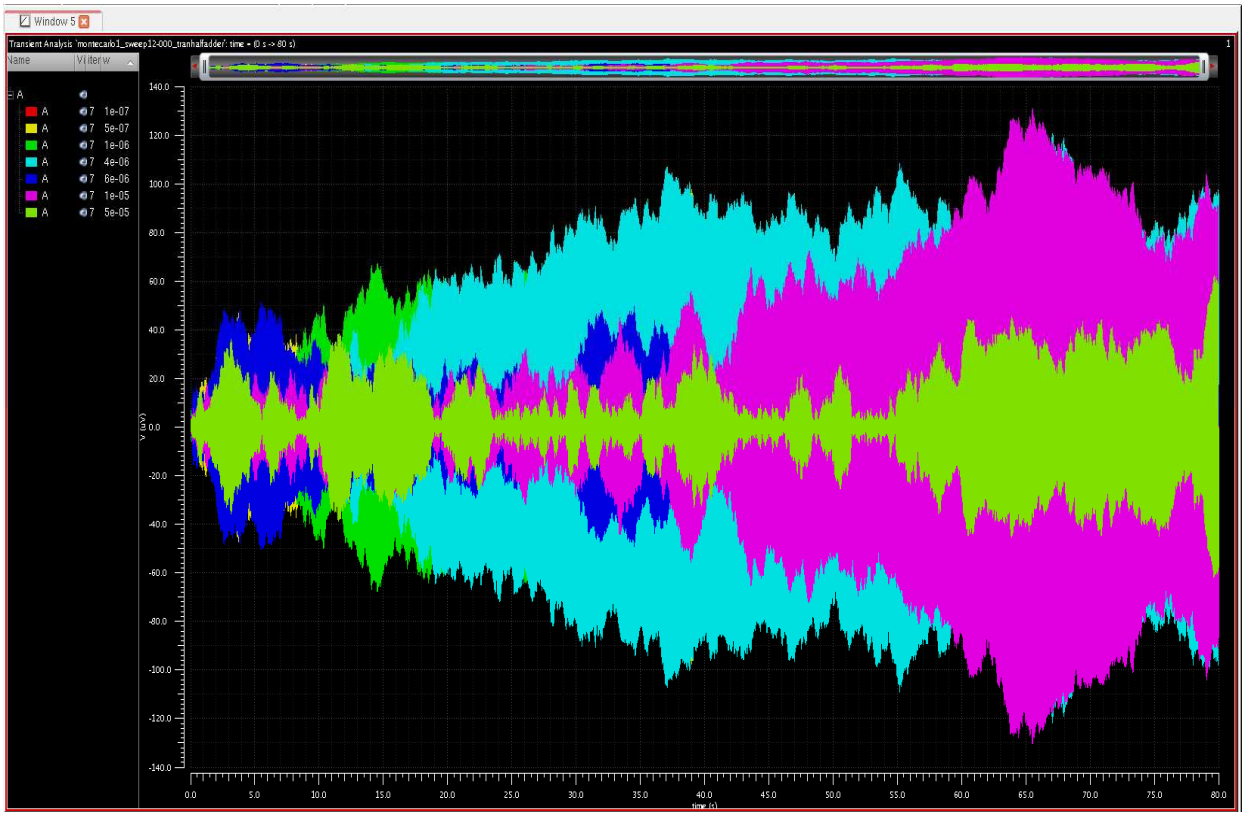

Figure 46: Transient Analysis obtained for width parameter variation (t500_r1half_w).

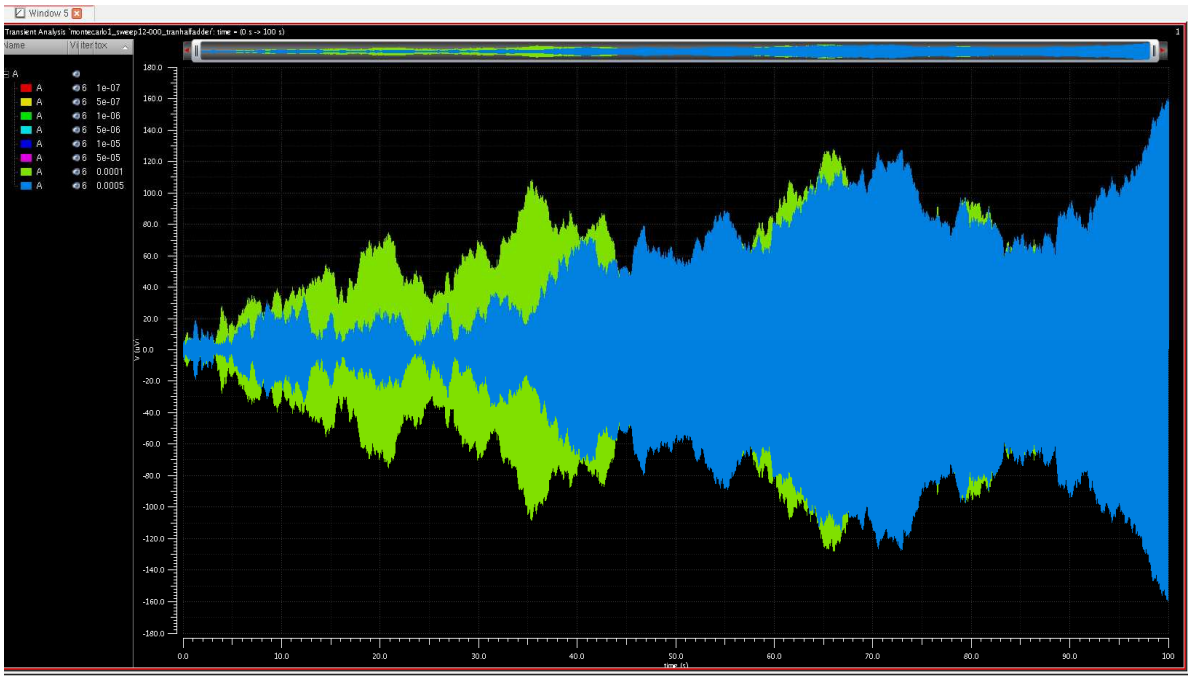

Figure 47: Transient Analysis obtained for oxide thickness parameter variation (t500_r1half_tox).

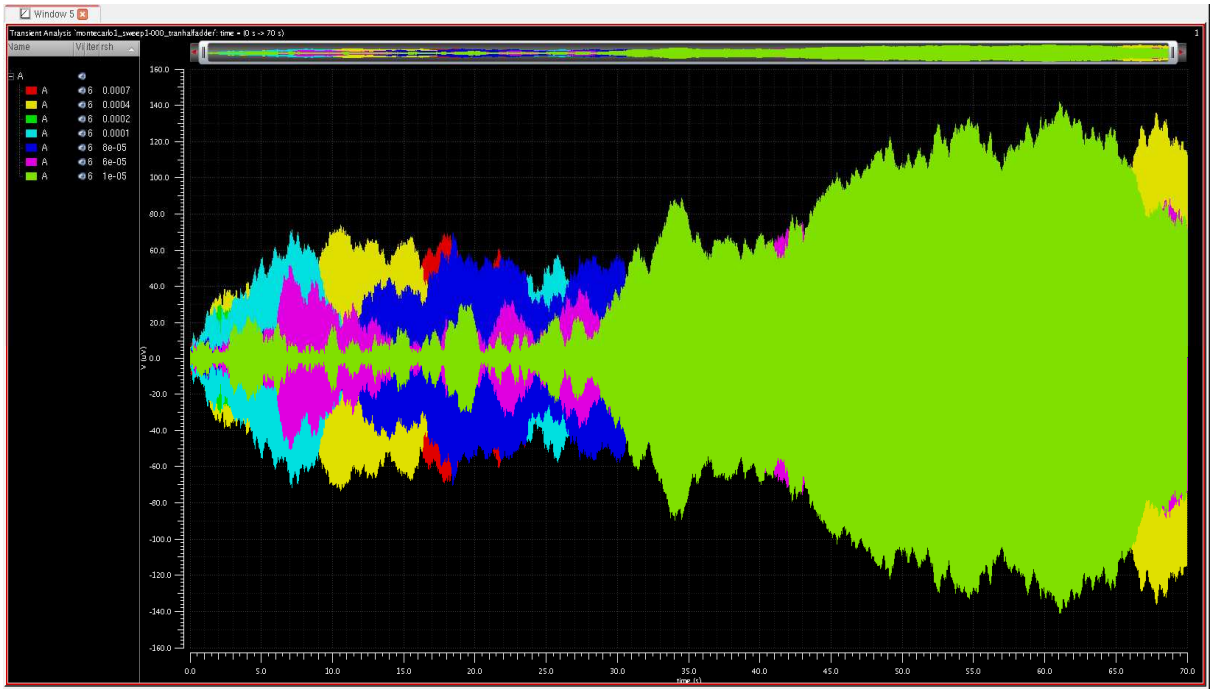

Figure 48: Transient Analysis obtained for sheet resistance parameter variation (t500_r1half_rsh).

From the above Figures, we can see that the parameters for ideal functioning of JFET are for length parameter l=4e-5 from Figure 45, for width parameter w=5e-5 from Figure 46, for oxide thickness parameter tox=5e-6 from Figure 47 and for sheet resistance parameter rsh=2e-4 from Figure 48.

The following Figures 49-52 are for the spice model having the temperature of 500˚C and the radial device distance parameter from the center of the wafer as 3 cm.

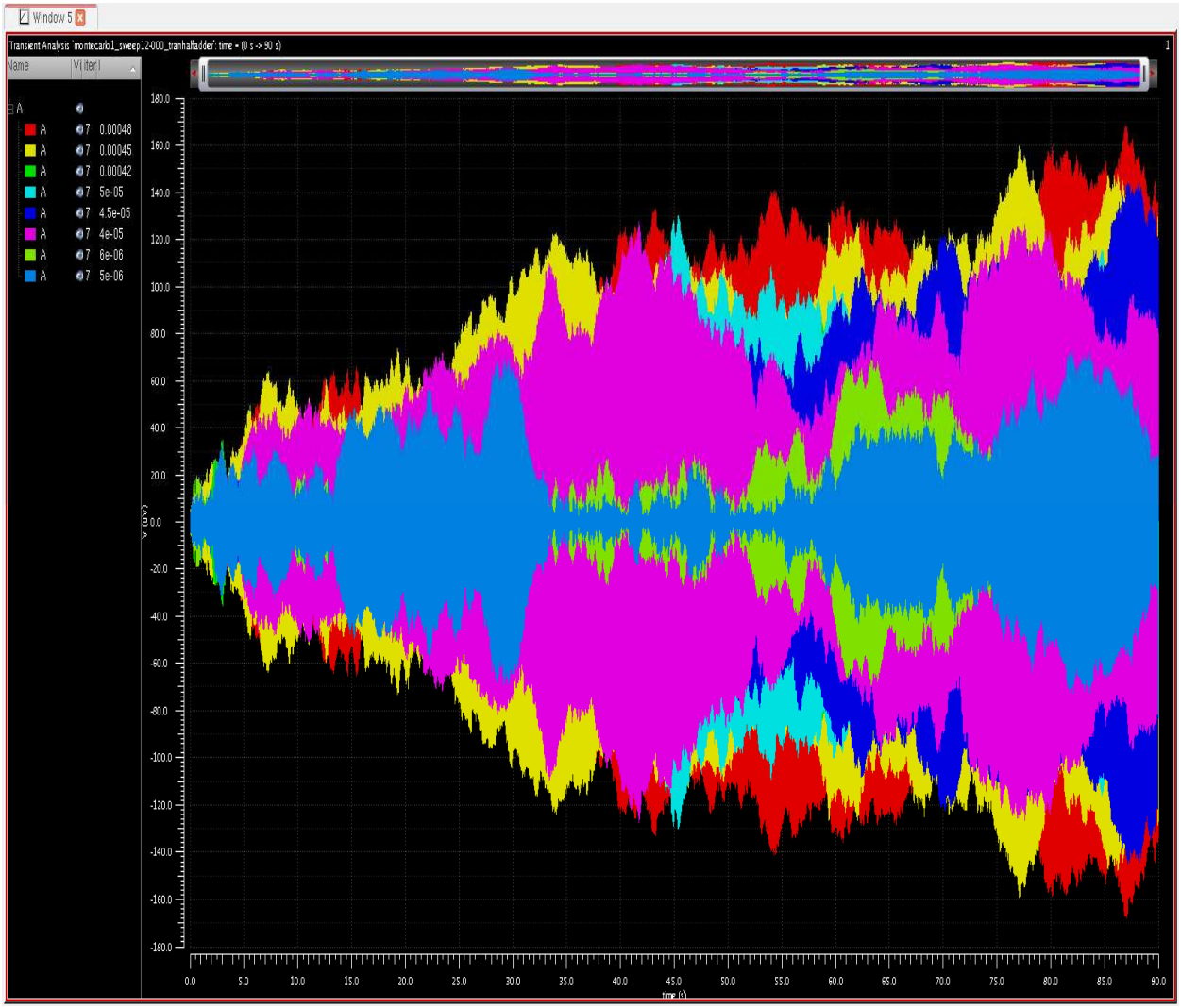

Figure 49: Transient Analysis obtained for length parameter variation (t500_r3_l).

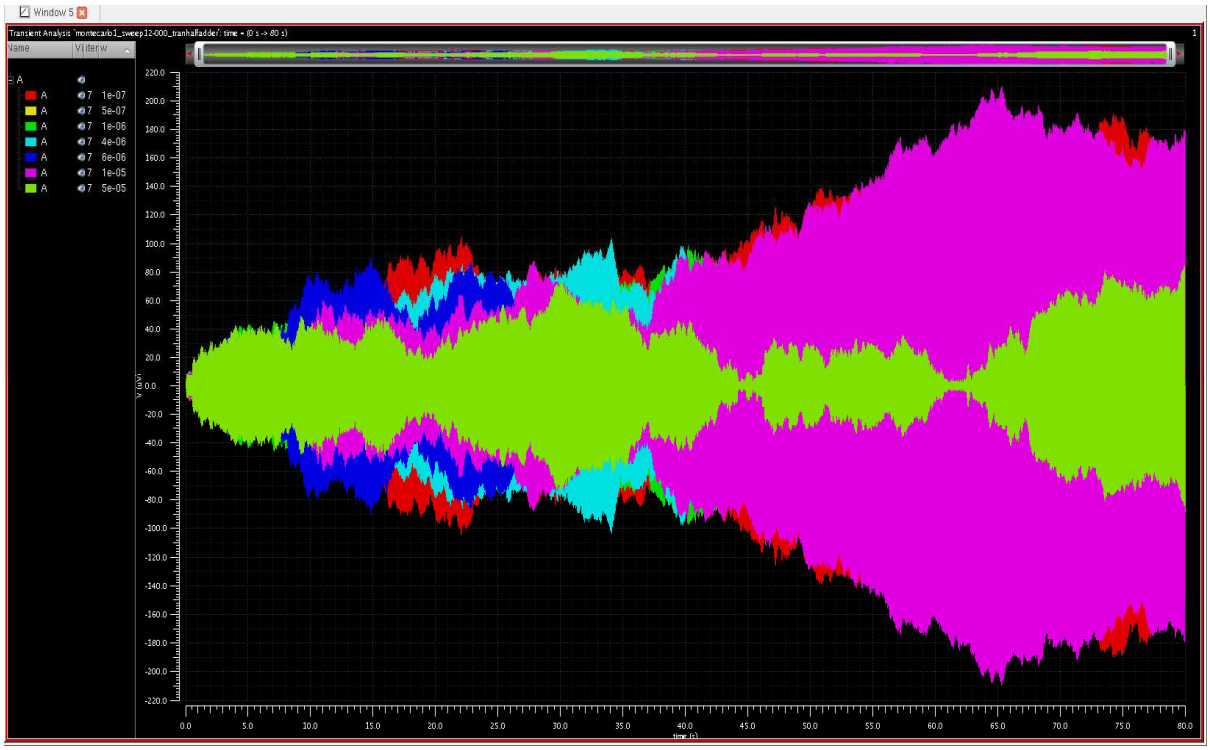

Figure 50: Transient Analysis obtained for width parameter variation (t500_r3_w).

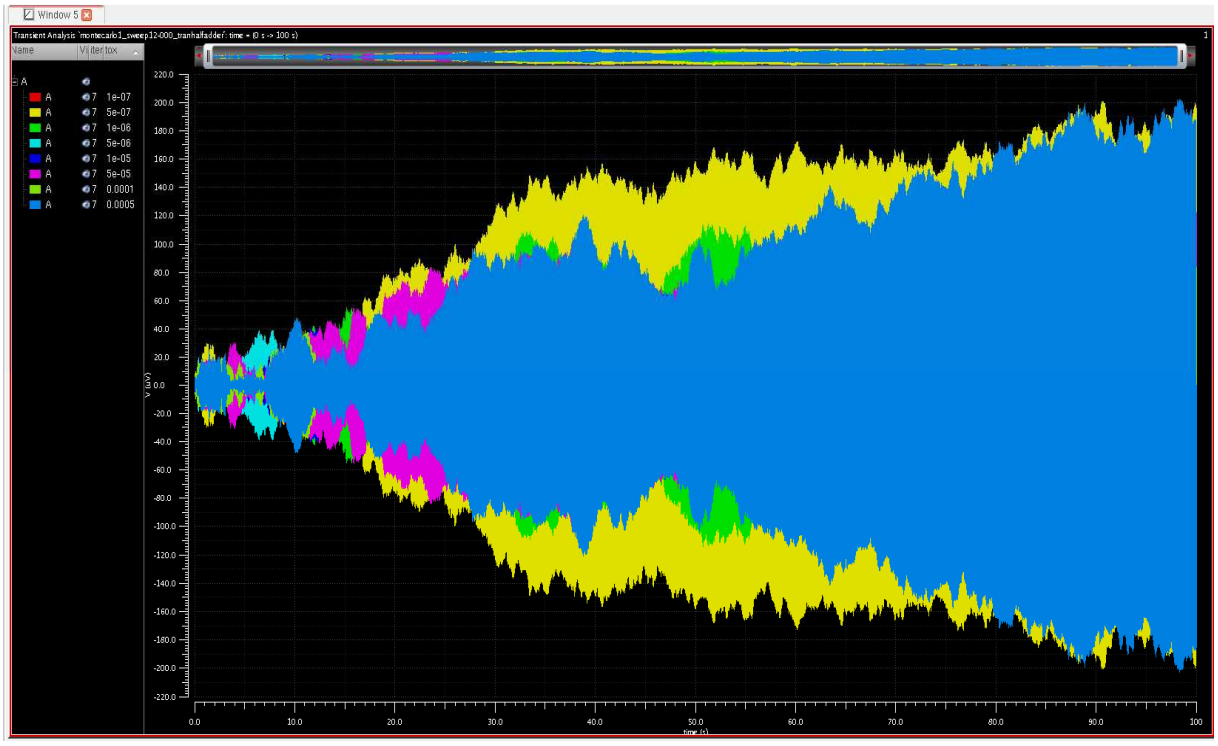

Figure 51: Transient Analysis obtained for oxide thickness parameter variation (t500_r3_tox).

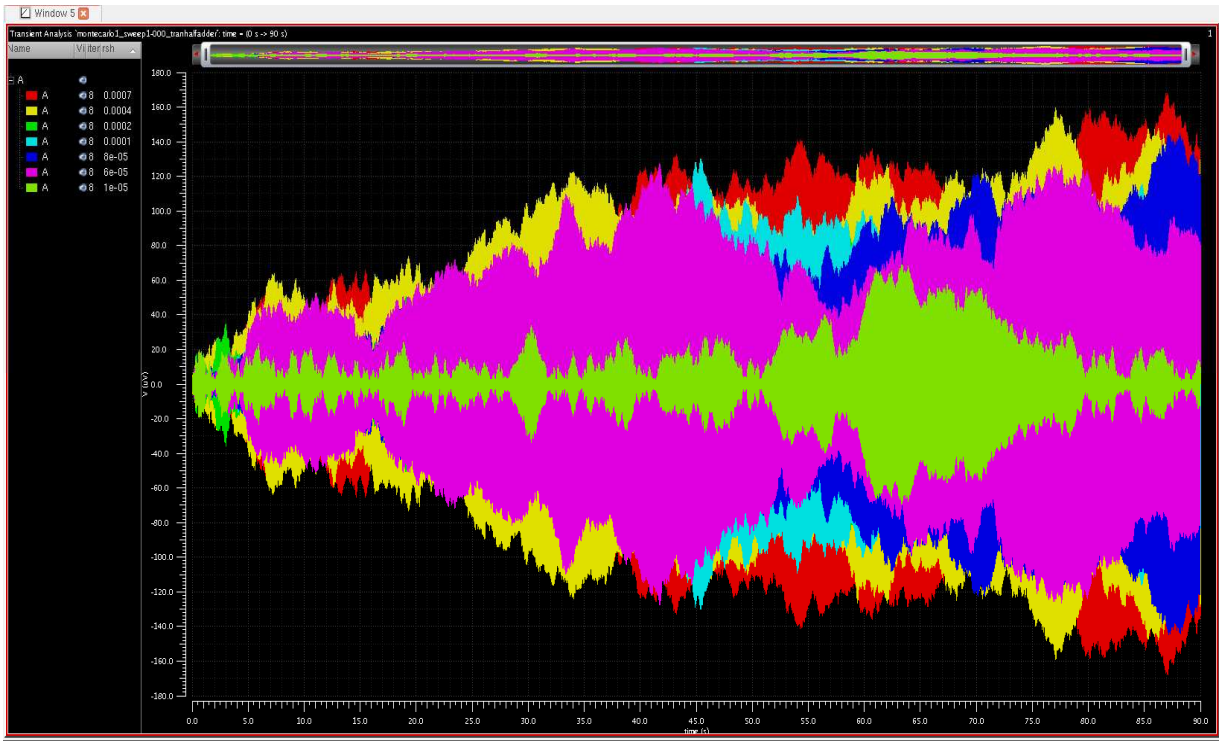

Figure 52: Transient Analysis obtained for sheet resistance parameter variation (t500_r3_rsh).

As shown in the Figures 49-52 the ideal region of operation can be considered for each of the parameters based on the transient analysis obtained by the variations in each of the parameter values. From Figure 49 we can say that the value of length parameter for the ideal operation of the circuit is 6e-6. In the same way for the width it is 5e-5 from Figure 50, for the oxide thickness it is 5e-6 from Figure 51 and for the sheet resistance 1e-5 from Figure 52.

From the given parameter in all the transient analysis we can see that parameter of the ideal operation varies from transient analysis to transient analysis. But these temperature variations effect the normal functioning of the Sic JFET when the parameters are of order e-4 except for the length and the effect will decrease for the lower orders that is of orders e-5, e-6. In contrast to this the parameters at order e-7 will have the same effects as of order e-4. So, in general the parameters

can have obtained an ideal result when they are order e-5 and e-6 and for the parameter of length will have general functioning when it is of order of e-4, e-5.

We have also obtained the following data during the monte carlo analysis of each of 9 Spice models and varying the parameters of length, width, oxide thickness and the sheet resistance of the JFET which are given the Table 1. We considered the same mismatch parameters like the transient analysis and obtained the slew rate generated using the export statement. We have used the following export statement for the Monte Carlo analysis

Slewrate= export ("slewRate (v (\" A \"),1n, t, 90n, t, 1, 90)").

SECTION 8

CONCLUSIONS

The following conclusions are obtained from the thesis project

1) Silicon Carbide JFET:

The Silicon Carbide JFET are very reliable devices when compared to the conventional CMOS devices. Silicon Carbide devices can be used in the higher temperatures when compared to the conventional CMOS. The CMOS devices fail in the BLEO environments due to leakage power, short circuit power, increase in device temperatures. For the Silicon Carbide devices, due to its crystalline structure the increase of the environmental temperature will not have much effect till 600˚C. There will be very less leakage and dynamic current produced at these temperatures.

2) Monte Carlo Simulations:

The Monte Carlo simulations using Spectre on the models of the SiC JFET implies the temperature and the radial device distance from the center of the wafer parameters have effect on the parameters of the JFET. But the length, width, sheet resistance and the oxide thickness parameters can be equally potential for the proper functioning of the JFET. The slew rate changes in the simulation data indicate that the physical parameters should also be taken into account.

3) Transient Analysis:

The Transient analysis using the Sweep parameter can indicate the parameter that can be used for different temperatures. This Analysis show the variation of the voltage with time for the variation

in the physical parameters of the JFET. The transient analysis show that the increase of the parameter like length, width, sheet resistance and the oxide thickness have adverse effects on the Silicon Carbide JFET.

4) Cadence Spectre tool:

This Cadence tool uses the spectre simulation code for the simulations of any circuit, but cannot generate any waveforms. Needed to use Viva and other waveform generators to view the waveforms.

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REFERENCES

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LIST OF APPENDICES

APPENDIX A: SILICON CARBIDE JFET SCS FILE

SILICON CARBIDE JFET SCS FILE

```
inline subckt bmenjfetsic (d g s b )
bmenjfetsic (d g s b ) sicnjfet
      model sicnjfet mos1 type=n vto =-8.85 kp=1.08e-5 lambda=0.006 tnom=25 rd=3175
rs=3175
      + is=2e-11 pb=2.87 fc=0.5 kf=0 af=1 gamma=0.897 cgso=8e-10 cgdo=1.8e-9
      + phi=1.435 cj=6.86e-5
ends bmenjfetsic

inline subckt bmenjfetsic_t25_r0 (d g s b )
bmenjfetsic_t25_r0 (d g s b ) sicnjfet
      model sicnjfet mos1 type=n  vto=-8.85 kp=1.08e-5 gamma=0.897 tnom=25
      + lambda=0.006 cj=6.86e-5 pb=2.87 phi=1.435 rd=3175 rs=3175
ends bmenjfetsic_t25_r0

inline subckt bmenjfetsic_t25_r1half (d g s b )
bmenjfetsic_t25_r1half (d g s b ) sicnjfet
      model sicnjfet mos1 type=n vto=-10.27 kp=1.03e-5 gamma=0.953 tnom=25
      + lambda=0.006 cj=6.86e-5 pb=2.87 phi=1.435 rd=3175 rs=3175
ends bmenjfetsic_t25_r1half

inline subckt bmenjfetsic_t25_r3 (d g s b )
bmenjfetsic_t25_r3 (d g s b ) sicnjfet
      model sicnjfet mos1 type=n vto=-15.03 kp=9.34e-6 gamma=1.12 tnom=25
      + lambda=0.006 cj=6.86e-5 pb=2.87 phi=1.435 rd=3175 rs=3175
ends bmenjfetsic_t25_r3

inline subckt bmenjfetsic_t300_r0 (d g s b )
bmenjfetsic_t300_r0 (d g s b ) sicnjfet
      model sicnjfet mos1 type=n vto=-9.23 kp=3.62e-6 gamma=0.897 tnom=300
      + lambda=0.006 cj=7.53e-5 pb=2.378 phi=1.189 rd=4291 rs=4291
ends bmenjfetsic_t300_r0

inline subckt bmenjfetsic_t300_r1half (d g s b )
bmenjfetsic_t300_r1half (d g s b ) sicnjfet
      model sicnjfet mos1 type=n vto=-10.67 kp=3.49e-6 gamma=0.953 tnom=300
      + lambda=0.006 cj=7.53e-5 pb=2.378 phi=1.189 rd=4291 rs=4291
ends bmenjfetsic_t300_r1half

inline subckt bmenjfetsic_t300_r3 (d g s b )
bmenjfetsic_t300_r3 (d g s b ) sicnjfet
      model sicnjfet mos1 type=n vto=-15.45 kp=3.14e-6 gamma=1.12 tnom=300
```

```
	+ lambda=0.006 cj=7.53e-5 pb=2.378 phi=1.189 rd=4291 rs=4291
ends bmenjfetsic_t300_r3

inline subckt bmenjfetsic_t500_r0 (d g s b )
bmenjfetsic_t500_r0 (d g s b ) sicnjfet
	model sicnjfet mos1 type=n vto=-9.55 kp=2.00e-6 gamma=0.897 tnom=500
	+ lambda=0.006 cj=8.22e-5 pb=1.997 phi=0.998 rd=6203 rs=6203
ends bmenjfetsic_t300_r0

inline subckt bmenjfetsic_t500_r1half (d g s b )
bmenjfetsic_t500_r1half (d g s b ) sicnjfet
	model sicnjfet mos1 type=n vto=-11.00 kp=1.92e-6 gamma=0.953 tnom=500
	+ lambda=0.006 cj=8.22e-5 pb=1.997 phi=0.998 rd=6203 rs=6203
ends bmenjfetsic_t500_r1half

inline subckt bmenjfetsic_t500_r3 (d g s b )
bmenjfetsic_t500_r3 (d g s b ) sicnjfet
	model sicnjfet mos1 type=n vto=-15.80 kp=1.73e-6 gamma=1.12 tnom=500
	+ lambda=0.006 cj=8.22e-5 pb=1.997 phi=0.998 rd=6203 rs=6203
ends bmenjfetsic_t500_r3
```

APPENDIX B: SPECTRE GENERATED NETLIST

SPECTRE GENERATED NETLIST

```
// Library name: classLib
// Cell name: Qfollower
// View name: schematic
subckt Qfollower gnd opin vdd
    R1 (opin gnd) resistor r=1K
    R0 (net06 gnd) resistor r=1K l=4 w=1
    M0 (vdd net06 opin 0) mos1
    V0 (net06 gnd) vsource dc=1 type=sine delay=1n freq=120 ampl=1 \
        sinephase=1.05 sinedc=1
ends Qfollower
// End of subcircuit definition.

// Library name: classLib
// Cell name: NORgate
// View name: schematic
subckt NORgate in1 in2 opin
    R3 (opin 0) resistor r=1K
    R2 (VDD! opin) resistor r=1K
    R1 (VDD! net07) resistor r=1K
    Mb (net07 in2 0 0) mos1
    Ma (net07 in1 0 0) mos1
    QFollower1 (VDD! VDD! net07) Qfollower
ends NORgate
// End of subcircuit definition.

// Library name: classLib
// Cell name: Halfadder
// View name: schematic
subckt Halfadder Cout Input1 Input2 S
    Nor4 (net12 net13 Cout) NORgate
    Nor3 (Input2 Input2 net12) NORgate
    Nor1 (Input2 Input1 net14) NORgate
    Nor5 (net14 Cout S) NORgate
    Nor2 (Input1 Input1 net13) NORgate
ends Halfadder
// End of subcircuit definition.

// Library name: classLib
// Cell name: FullAdder
// View name: schematic
Halfadder1 (net12 A B net017) Halfadder
Halfadder2 (net08 net017 Cin SUM) Halfadder
```

FNor2 (net15 net15 Carry) NORgate
FNor1 (net08 net12 net15) NORgate

APPENDIX C: VERILOG FILES

VERILOG FILES

The following Figure 53 will show the details about the netlist location.

Figure 53: Verilog Files folder

The Verilog Files folder will be available in FullAdder_run1/ihn1 when they are created using the Virtuoso Schematic. We can 4 folders related to the netlist. Cds0 contains the netlist of Q Follower, cds1 contains the netlist of Nor Gate, cds2 contains the netlist of Half adder and cds3 contains the netlist of Full adder. We will now see the netlists of Q follower, Nor gate, Half adder and Full adder.

Q Follower Netlist:

```
// Library - classLib, Cell - Qfollower, View - schematic
// LAST TIME SAVED: Apr  6 12:41:15 2017
// NETLIST TIME: Apr 13 12:04:04 2017
`timescale 1ns / 1ns

module Qfollower ( gnd, opin, vdd );

output  gnd, opin;

input  vdd;


specify
   specparam CDS_LIBNAME  = "classLib";
   specparam CDS_CELLNAME = "Qfollower";
   specparam CDS_VIEWNAME = "schematic";
endspecify
```

```
res  R1 ( .MINUS(gnd), .PLUS(opin));
res  R0 ( .MINUS(gnd), .PLUS(net06));
nmos4  M0 ( .D(vdd), .B(cds_globals.gnd_), .G(net06), .S(opin));
vsource #(1)   V0 ( .PLUS(net06), .MINUS(gnd));

endmodule
```

Nor Gate Netlist:

```
// Library - classLib, Cell - NORgate, View - schematic
// LAST TIME SAVED: Apr  6 12:53:11 2017
// NETLIST TIME: Apr 13 12:04:04 2017
`timescale 1ns / 1ns

module NORgate ( opin, in1, in2 );

output  opin;

input  in1, in2;


specify
   specparam CDS_LIBNAME  = "classLib";
   specparam CDS_CELLNAME = "NORgate";
   specparam CDS_VIEWNAME = "schematic";
endspecify

res  R3 ( .MINUS(cds_globals.gnd_), .PLUS(opin));
res  R2 ( .MINUS(opin), .PLUS(cds_globals.VDD_));
res  R1 ( .MINUS(net07), .PLUS(cds_globals.VDD_));
nmos4  Mb ( .D(net07), .B(cds_globals.gnd_), .G(in2),
    .S(cds_globals.gnd_));
nmos4  Ma ( .D(net07), .B(cds_globals.gnd_), .G(in1),
    .S(cds_globals.gnd_));
Qfollower QFollower1 ( cds_globals.VDD_, cds_globals.VDD_, net07);

endmodule
```

Half Adder Netlist:

```
// Library - classLib, Cell - Halfadder, View - schematic
// LAST TIME SAVED: Apr  6 12:30:58 2017
```

```
// NETLIST TIME: Apr 13 12:04:04 2017
`timescale 1ns / 1ns

module Halfadder ( Cout, S, Input1, Input2 );

output  Cout, S;

input  Input1, Input2;


specify
   specparam CDS_LIBNAME  = "classLib";
   specparam CDS_CELLNAME = "Halfadder";
   specparam CDS_VIEWNAME = "schematic";
endspecify

NORgate Nor4 ( Cout, net12, net13);
NORgate Nor3 ( net12, Input2, Input2);
NORgate Nor1 ( net14, Input2, Input1);
NORgate Nor5 ( S, net14, Cout);
NORgate Nor2 ( net13, Input1, Input1);

endmodule
```

Full Adder Netlist:

```
// Library - classLib, Cell - FullAdder, View - schematic
// LAST TIME SAVED: Apr 13 11:40:52 2017
// NETLIST TIME: Apr 13 12:04:04 2017
`timescale 1ns / 1ns

module FullAdder ( Carry, SUM, A, B, Cin );

output  Carry, SUM;

input  A, B, Cin;


specify
   specparam CDS_LIBNAME  = "classLib";
   specparam CDS_CELLNAME = "FullAdder";
   specparam CDS_VIEWNAME = "schematic";
endspecify
```

```
Halfadder Halfadder1 ( net12, net017, A, B);
Halfadder Halfadder2 ( net08, SUM, net017, Cin);
NORgate FNor2 ( Carry, net15, net15);
NORgate FNor1 ( net15, net08, net12);

endmodule
```

APPENDIX D: SAMPLE FULL ADDER SCS FILE

SAMPLE FULL ADDER SCS FILE

The following code is a Full Adder SCS file netlist used for the Monte Carlo analysis and Transient analysis. It is taken from fulladder_t25_r0.scs file. We have used the spectre netlist generated which is given in Appendix B.

Netlist of Full Adder:

```
// Example Full Adder netlist
simulator lang=spectre
global 0 vdd! gnd!
include "../models/globals.scs"
include "../models/stat_sicjfets.scs"

// last include statement is for including the inline subckt of bmenjfetsic.

//Need to include SiC JFET models

//parameters if required
parameters td=1p ph=1.05 frequency=120 v1=0.1 res=1K tox=1e-7 rsh=0 w=3e-6 l=3e-6

// Start of subcircuit defintion for q follower

//Library name: classLib
//Cell Name: Q Follower
//View Type: schematic

subckt q_follower vdd gnd
      R0 (net06 gnd) resistor r=res
      R1 (net04 gnd) resistor r=res
      Input (net06 gnd) vsource dc=v1 type=sine delay=td sinedc=v1 phase=ph freq=frequency
      M0 (vdd net06 net04 gnd!) bmenjfetsic_t25_r0

// bmenjfetsic is defined in stat_sicjfets.scs and it is also included in this file.
ends q_follower

//end of subcircuit definition of  q follower

// Start of subcircuit definition for Nor gate
```

```
//Library name: classLib
//Cell Name: Nor Gate
//View Type: schematic

subckt nor_gate in1 in2 opin
        Ma (net07 in1 gnd! gnd!) bmenjfetsic_t25_r0
        Mb (net07 in2 gnd! gnd!) bmenjfetsic_t25_r0
        R1 (vdd! net07) resistor r=res
        R2 (vdd!  opin) resistor r=res
        R3 (opin gnd!) resistor r=res
        QFollower1 (net07 vdd!) q_follower
ends nor_gate

// End of subcircuit definition for Nor gate

// Start of subcircuit definition for Half adder

// Library name: classLib
//Cell Name: Half Adder
//View Type: schematic

subckt Half_adder input1 input2 cout s
        Nor1 (input2 input1 net14) nor_gate
        Nor2 (input1 input1 net13) nor_gate
        Nor3 (input2 input2 net12) nor_gate
        Nor4 (net12 net13 cout) nor_gate
        Nor5 (net14 cout S) nor_gate
ends Half_adder

// End of subcircuit definition for Half adder

//Library name: classLib
//Cell Name: Fulladder.sim
//View name: schematic

//A1 (A gnd!) vsource type=pulse val0=1e-6 val1=0 period=1p width=0.3p
//B1 (B gnd!) vsource type=pulse val0=1e-6 val1=0 period=2p width=0.3p
//C1 (Cin gnd!) vsource type=pulse val0=1e-6 val0=0 period=4p width=0.3p
Halfadder1 (A B net12 net017) Half_adder
Halfadder2 (net017 Cin net08 SUM) Half_adder
FNor1 (net08 net12 net15) nor_gate
FNor2 (net15 net15 Carry) nor_gate

// Needed to add the analysis statements here.
// Monte Carlo Analysis Statements
// Only process statements are used as mismatch statements are required for mismatch
```

```
parameters for n jfet and p jfet.
// Here we are using n jfet.
// Including sweep statements on temperature

// Start of Monte Carlo Analysis Statements

montecarlo1 montecarlo variations=all seed=2 numruns=10
scalarfile="../monteCarlo_t25_r0_rsh/mcdata" paramfile="../monteCarlo_t25_r0_rsh/mcparam"
saveprocessparams=yes processparamfile="../monteCarlo_t25_r0_rsh/processParam" \
   processscalarfile="../monteCarlo_t25_r0_rsh/processData"{
      sweep1 sweep param=rsh values=[1e-4 2e-4 4e-4 7e-4 1e-5 6e-5 8e-5 ]{
            dchalfadder dc
            tranhalfadder tran start=0 stop=90 step=10

            export slewrate=oceanEval("slewRate(v(\"A\"),1n,t,90n,t,1,90)")
      }
}
// end of Monte Carlo Analysis

//Start of Statistics block for Monte Carlo Analysis

statistics{
      process{
            vary tox dist=gauss std=0.06
            vary rsh dist=gauss std=8 percent=yes
            vary w dist=gauss std=0.05
            vary l dist=gauss std=0.05
            }
      mismatch{
            vary tox dist=gauss std=4
            vary rsh dist=gauss std=0.6
            vary w dist=gauss std=0.1
            vary l dist=gauss std=0.1
            }

// Correlate some of the process parameters
      correlate param=[tox rsh] cc=0.6
}

//End of statistics block for Monte Carlo Analysis
```

VITA

Education Summary:

1) Vasavi College of Engineering
   Bachelor of Engineering in Electronics and Communication Engineering
   GPA 3.08 May 2012

Academic Employment:

Co-Instructor, 01/2016 – Present, University of Mississippi.

- Coordinating and scheduling the semester wide plan for the course and keeping students engaged in this online course.
- Helping instructor on the betterment of the course and getting feedback from students to make the course more valuable and interesting.

Professional Employment:

Software Engineer, 5/2013-7/2015, Prokarma Softech Pvt.Ltd.

Responsible for UI and Web Developer of the CattleXpert Management Software.

- UI Development of the Project and Project Related Database Functionality.
- Designing Screens using HTML5 and using Photoshop to make icons compatible.