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Mismatch Distance Term Compensation in Centroid Configurations with Nonzero-Area Devices

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Abstract

This paper presents an analytical approach to distance term compensation in mismatch models of integrated devices. Firstly, the conditions that minimize parameter mismatch are examined under the assumption of zero-area devices. The analytical developments are illustrated using centroid configurations. Then, deviations from the previous approach due to the nonzero device areas are studied and evaluated.

1. Introduction

The tendency in integrated circuit design towards the use of submicron technologies has motivated improvements in the modeling of the second order effects of the MOS transistor and of the random variations in the fabrication processes, which are critical in the design of high performance analog circuits [1]-[7].

Variability phenomena of electrical characteristics in integrated circuits can be classified into two groups: inter-die variability and intra-die mismatch. The first one accounts for differences die-to-die or wafer-to-wafer, while the second is due to the existence of parameter fluctuations in the wafer. We will focus on intra-die mismatch as it is the main responsible for the deviations in analog circuit behavior.

The mismatch effect on circuit performance has been examined by many authors, and different mismatch models have been proposed recently [3]-[9]. Section 2 will briefly describe the most widely known intra-die mismatch model: the Pelgrom's model. In section 3 we will focus on the second term of this model, which accounts for the mismatch due to the distance between devices. An analytical technique to compensate this mismatch is introduced and applied to several centroid configurations. Finally, section 4 examines the effect of taking into account device areas on the distance term and the magnitude of this perturbation is evaluated.

2. Mismatch modelling

In 1988, Pelgrom proposed a model which has become a reference for mismatch effects on analog integrated circuits [3]. For two samples of a device with equal $W \cdot L$ and a separation distance D_{12}, this model associates a stochastic variable with the difference between the values of the same parameter in each transistor (i. e. threshold voltage). This stochastic variable can be represented by its standard deviation,

$$\sigma^2 = \frac{A_p}{WL} + S_p^2 D_{12}^2 \quad , \qquad (1)$$

A_p and S_p being technology-dependent fitting constants.

The first term in (1) includes the influence of transistor sizes and shapes (these do not appear explicitly as rectangular shapes are assumed). It can be assumed that each transistor parameter has a nominal value and a superimposed white noise. Associating Laplace transforms to the transistor configuration, it can be considered as a noise filtering process. Then, this term in (1) appears as a result of noise power not eliminated in the filtering process by the configuration. Therefore, the configuration introduces a set of variables in (1), namely, sizes and shapes.

The second term in (1) represents the influence of the distance between transistors D_{12}, and is a consequence of the existence of gradients in the wafer. The value of any transistor electrical parameter P is represented by a function of distance in the wafer, $P=Kd$, where d is the distance from the point where P is evaluated to the point known as perturbation center. This perturbation center is the point in the wafer where the parameter takes its maximum/minimum value. Therefore, the radial dependence of a parameter can be modeled as a cone whose vertex is the perturbation center [4].

3. Mismatch Reduction Techniques

The physical interpretation of each term in (1) suggests different techniques to reduce them. The area term can only be reduced by increasing device areas [8]-[9]. For small devices, this is the dominant term and the distance term can be neglected. However, for high-performance design, in which areas are relatively large,

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distance term plays an important role. In order to reduce this influence, partitioning techniques and centroid configurations are commonly used, although this is only based in heuristic considerations. In the following, reduction techniques are analyzed using an analytical approach which allows to find out configurations with interesting statistical properties.

3.1. Device partitioning

Let us assume that the perturbation centre is the reference point for every distance. Therefore, the new set of variables d_i is the distance from each transistor to the perturbation centre (device separation D_{12} can be easily obtained as the difference vector), as illustrated in Fig. 1.

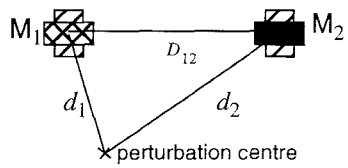

Figure 1: Distances to perturbación centre.

Given two devices, our technique partitions one or both of them into a set of subdivisions (M and N respectively) and tries to combine them, generating different configurations, to improve the statistical parameters. This is illustrated for the conventional centroid configuration in Fig. 2(b) where one of the devices in Fig. 2(a) has been partitioned into four pieces. The gradient effect compensation due to the four subdivisions seems to make the parameter value more uniform. In this way we could obtain a reduction of the standard deviation compared with the one in the original configuration.

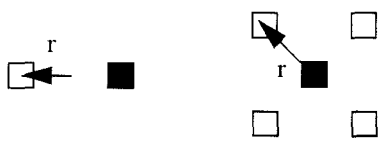

Figure 2: (a) Basic Structure; (b) Centroid structure.

3.2. Mathematical model

A mathematical model must be developed to evaluate the influence on mismatch of the partitions performed on the transistors. Parameter mismatch is an stochastic variable, hence the unique way to obtain this model is using its first- and second-order statistics: mean and standard deviation.

We will first assume zero-area transistors placed in their geometric centres. This is reasonable as we are trying to reduce the distance term of Pelgrom's model, and hence in a first approximation we are interested only in the distance between the partitions but not in their areas.

Assuming a radial dependence of the parameter P,

$$P = P_0 + K \cdot d \tag{2}$$

and averaging distances from each partition to the perturbation centre, the parameter variation is

$$\Delta P = \frac{K}{N}\sum_{i=1}^{N} d_i - \frac{K}{M}\sum_{j=1}^{M} d_j \tag{3}$$

where K is the gradient slope on the wafer, d_i and d_j, are the distances from each partition to the perturbation centre, and, M and N are the number of partitions in each device.

During the design of a circuit the relative position of the configuration with respect to the perturbation centre is unknown, so we must calculate mismatch as an average of ΔP for every possible configuration position with respect to the perturbation centre. The mean is,

$$E[\Delta P] = \frac{1}{2\pi}\int_0^{2\pi}\left(\frac{1}{N}\sum_{i=1}^{N} d_i - \frac{1}{M}\sum_{j=1}^{M} d_j\right)\Bigg|_{\alpha} d\alpha \tag{4}$$

and the standard deviation is given by,

$$\sigma^2 = \frac{1}{2\pi}\int_0^{2\pi}\left(\frac{1}{N}\sum_{i=1}^{N} d_i - \frac{1}{M}\sum_{j=1}^{M} d_j\right)^2\Bigg|_{\alpha} d\alpha - E^2[\Delta P] \tag{5}$$

This mathematical model can be used to compare different configurations. It requires the evaluation of (4) and (5), what can be done by expressing distances to the perturbation centre as a function of the symmetrical center of the configuration.

3.3. Evaluation for different centroid structures

Fig. 3 shows several centroid configurations and the evaluation of their statistical properties using equations (4) and (5). In each case, distances from transistors to perturbation centre, d_i and d_j were expressed as a function of the distance R from the configuration center to the perturbation center, as shown in Fig. 4. Assuming zero-area devices, distances can be expressed as:

$$d_i = R \cdot \sqrt{1 + \frac{r^2}{R^2} + 2\frac{r}{R}\cdot \cos\alpha} \tag{6}$$

It is impossible to solve (4)-(6) analytically. But, expanding d_i and d_j in Taylor series around R and truncating it appropriately, these integrals can be solved analytically with high accuracy (error is <0.1%). Truncation of Taylor series is a reasonable approximation, since $r \ll R$.

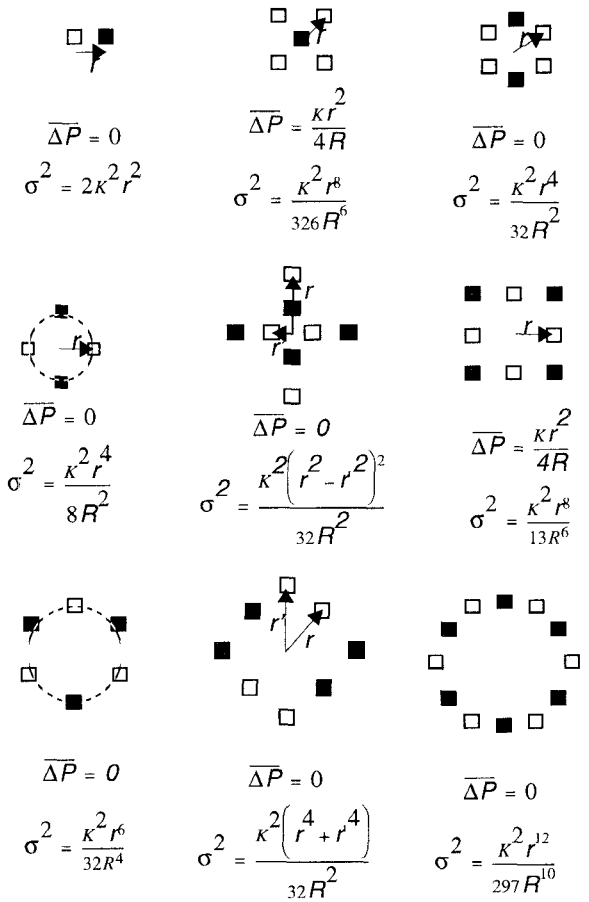

Figure 3: Mean and deviation for different structures.

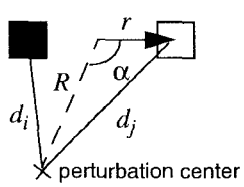

Figure 4: Illustrating distances to the perturbation center.

The results in Fig. 3 are very interesting for designers. For instance, the detailed analytical study of the conventional centroid structure shows that although it presents quite low standard deviation, the mean is not zero; on the contrary, it is inversely proportional to the distance to perturbation centre. This is disadvantageous compared for instance to circular structures. The price to pay in these is a larger layout area.

4. Area influence on distance term

In the model shown in section 3, the distances from each transistor to the perturbation center have been measured from the geometric center of each partition. In this section the influence of considering non-zero area partitions is studied. It must be noticed that we are focusing only on the distance term of Pelgrom's model. This will make clear that there exist a correlation between the mismatch term due to the distance between transistor partitions and their sizes.

In order to understand this influence, consider an isolated device, as illustrated in Fig. 5. If the transistor is considered a point located in its geometrical centre, much information is being lost. A more accurate calculation is to average out the distance to the perturbation center:

$$D_1 = \frac{1}{WL} \cdot \iint_A \sqrt{x^2 + y^2}\, dA \qquad (7)$$

Then, the zero-area model equations can be used substituting d by an average distance. The new mean is,

$$(2\pi)^2 E[\Delta P] = \int_0^{2\pi}\left[\int_0^{2\pi}\left(\frac{1}{N}\cdot\sum_{i=1}^{N}\frac{1}{A_i}\cdot\iint_{A_i} d\cdot dA_i\right)\Bigg|_{\alpha}\cdot d\alpha\right]\Bigg|_{\beta}\cdot d\beta - \int_0^{2\pi}\left[\int_0^{2\pi}\left(\frac{1}{M}\cdot\sum_{j=1}^{M}\frac{1}{A_j}\cdot\iint_{A_j} d\cdot dA_j\right)\Bigg|_{\alpha}\cdot d\alpha\right]\Bigg|_{\beta}\cdot d\beta \qquad (8)$$

and a corresponding expression can be obtained for the standard deviation. The interpretation of these equations has a clear geometrical meaning as shown in Fig. 6. First, for each angular position of the configuration to the perturbation centre α, an average distance for each partition must be calculated. Then, this previous result must be averaged for each possible initial position of a partition with respect to the perturbation centre β.

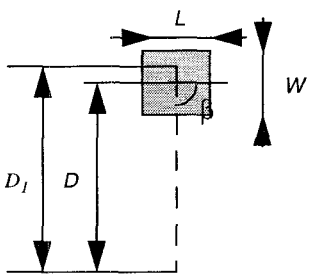

Figure 5: Illustrating area influence.

This technique is too complex as an average distance of each partition must be calculated for each angular position α. In the zero-area model, trajectories described by

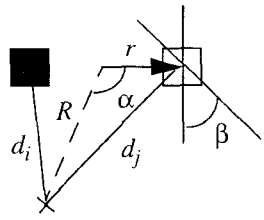

Figure 6: Geometric interpretation of (8).

partition centers are perfectly circular (partition center is constant and equal to the geometrical centre). However, in the nonzero-area model, these trajectories are not circular, because the average distance of each partition depends on the value of α.

The resolution complexity of equations in zero-area model was high but, assuming the partition centers dependent on α, the equation resolution is even more difficult. To avoid this problem, an equivalent β-independent point can be considered. With this approach, the area integrals are eliminated and the model complexity is significantly reduced. This point is obtained averaging all the area of each partition for each β value. This gives:

$$D_1 = \frac{1}{2\pi}\frac{1}{WL}\cdot\int_0^{2\pi}\iint_A \sqrt{x^2+y^2}\Big|_\beta dA\cdot d\beta \qquad (9)$$

which can be used in the equations for the zero-area models (4)-(5).

5. Perturbation magnitude

It is also impossible to solve equation (9) in general, but the displacement of the partition equivalent center with respect to its geometrical center can be avaluated for some simple case, i.e. $\beta = \frac{\pi}{2}$, shown in Fig. 5. Assuming $D>>W$, expanding equation (7) in a Taylor series, and integrating over the given area, an approximated analytical result can be obtained. A movement of the partition center with respect to the geometrical center is observed, which for the case in Fig. 5 is $\frac{L^2}{24D}$.

In the general case, we should average this movement for each value of β. The problem can be solved numerically, using enough β samples to obtain an accurate value of the displacement. The calculated value is around $0.042\frac{WL}{D}$.

Taking into account previous results, nonzero-area devices cause a loss of symmetry in the configuration. Assuming that we are working with a wafer diameter of 10 centimeters, that the perturbation center is on the wafer, and that we have typical values of device sizes (50μm), the assumption $D \gg r, W, L$ can be considered conservative, and hence the approximations in the models are valid.

Evaluating the partitition center movement using the previous numerical result, and the values for the different variables involved, the obtained average displacement is around 0.02μm. Consider the distance values used in section 3, which are the distances from the partition geometrical centers to the configuration center, which are half a transistor size at least (around 25μm). Therefore, the distance error using 25μm instead of values around 25.02 μm is smaller than 0.01%. So, this movement can be neglected.

But, it is the influence on the parameter mismatch the really significant information. The evaluation of the mean and standard deviation for each structure using nonzero and zero-area models gives a relative error between the results provided by each model around 0.5% in quite extreme cases (assuming square devices with a 200μm side and r/R=0.1).

6. Conclusion.

A mismatch evaluation technique for partitioned structures has been developed. Firstly, transistor parameters have been statistically characterized assuming zero-area devices. Then, the area influence has been examined. These areas cause a transistor center movement, but it is verified that their influence on zero-area results can be neglected, assuming typical distance values.

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