Ball Lens Embedded Through-Package Via To Enable Backside Coupling Between Silicon Photonics Interposer and Board-Level Interconnects

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Nivesh Mangal, Jeroen Missinne, Joris Van Campenhout, Bradley Snyder, and Geert Van Steenberge

***Abstract*—Development of an efficient and densely integrated optical coupling interface for silicon photonics based board-level optical interconnects is one of the key challenges in the domain of 2.5D/3D electro-optic integration. Enabling high-speed on-chip electro-optic conversion and efficient optical transmission across package/board-level short-reach interconnections can help overcome the limitations of a conventional electrical I/O in terms of bandwidth density and power consumption in a high-performance computing environment. In this context, we have demonstrated a novel optical coupling interface to integrate silicon photonics with board-level optical interconnects. We show that by integrating a ball lens in a via drilled in an organic package substrate, the optical beam diffracted from a downward directionality grating on a photonics chip can be coupled to a board-level polymer multimode waveguide with a good alignment tolerance. A key result from the experiment was a 14 μm chip-to-package 1-dB lateral alignment tolerance for coupling into a polymer waveguide with a cross-section of 20$\times$25 μm^2 . An in-depth analysis of loss distribution across several interfaces was done and a -3.4 dB coupling efficiency was measured between the optical interface comprising of output grating, ball lens and polymer waveguide. Furthermore, it is shown that an efficiency better than -2 dB can be achieved by tweaking few parameters in the coupling interface. The fabrication of the optical interfaces and related measurements are reported and verified with simulation results.**

***Index Terms*—Silicon Photonics; Optical Interposer; Datacenters; Polymer waveguides; Ball Lens; Chip-to-Board Coupling.**

I. Introduction

Adoption of deep learning and artificial intelligence based algorithms across several applications supported by GPU/TPU driven cloud computing platforms has resulted in an increased performance requirement from the hardware resources present in the datacenters of today [1]–[3]. While the very short-reach interconnections on a GPU chip can support high bandwidth density using electrical links, the same do not scale well with increasing bandwidth and reach requirement at the package or at the board-level, necessitating the requirement for optical links. For board-level inter-chip data communication, the interception point for optical interconnects in terms of bandwidth density lies around 500 Gbps/mm for them to outperform electrical interconnects. As an example, taking 50 Gb/s bandwidth per channel and 50 μm channel pitch on board-level optical interconnects for 20 channels, it is possible to achieve an aggregate bandwidth density of 1 Tbps/mm. The existing pluggable optical I/Os present in today's datacenters provide optical reach only up to the board-edge and suffer from a limited faceplate density and power dissipation in high-speed electrical interconnects over the PCB, to the pluggable optics at the board-edge [3]. In order to bring optics closer to the GPU/ASIC, silicon photonics transceivers can be co-packaged resulting in a power efficient, low latency co-packaged optical solution (Fig. 1). The CMOS-compatible silicon photonics technology offers several benefits such as wafer-scalability, dense integration, single-mode transmission, better modulation formats and wavelength division multiplexing (WDM) [4]. The chip-to-chip optical signaling between such co-packaged modules can be implemented via polymer or glass based on-board optical interconnects. At the board-level, with interconnect length ranging between few tens of centimeters, it is possible to maintain a high bandwidth-distance product by using multimodal optical interconnects (with spatial division multiplexing (SDM)), which provide the advantage of relaxed alignment tolerance and a possibility of reduction in overall cost with passive assembly. Thus, a chip-to-board optical coupling interface that is alignment tolerant, energy efficient, and agnostic towards channel-density scaling can help push the case of realizing on-board chip-to-chip optical communication.

So far, only a few research groups have reported integration schemes ranging from adiabatic optical coupling [7], [8] to cone-shaped optical pin coupling interface for multimode interconnections [9], [10]. As can be seen, all the approaches demonstrated before have used the device side of the chip to interface with a package or a board-level optical interconnect. From a perspective of 3D integration requiring the memory/logic die-stacking on the top of a photonics chip interposer, a face-up bonding scheme of the photonics die is desirable since the device top side of the die remains accessible for electrical interconnections. In that scenario, a through-substrate (backside) coupling I/O can enable the face-up integration of photonic chips, and also help avoid the necessity to reserve space for placement of fiber-array from the topside of the die in case the laser module is not integrated on-chip. By a through-substrate coupling interface [11], it is implied that the on-chip high-bandwidth optical signal can be directed off-normal through the bulk of an SOI substrate, as opposed to using other coupling alternatives like an edge-

N. Mangal, J. Missinne, G. Van Steenberge are with the Centre for Microsystems Technology, Ghent University and imec, Zwijnaarde Technologiepark 126, 9052 Ghent, Belgium (e-mail: nivesh.mangal@imec.be, jeroen.missinne@ugent.be;geert.vansteenberge@ugent.be)

N. Mangal, B. Snyder, J. Van Campenhout are with imec, Kapeldreef-75, Heverlee B-3001, Belgium (e-mail: nivesh.mangal@imec.be, bradely.w.snyder@gmail.com; joris.vancampenhout@imec.be)

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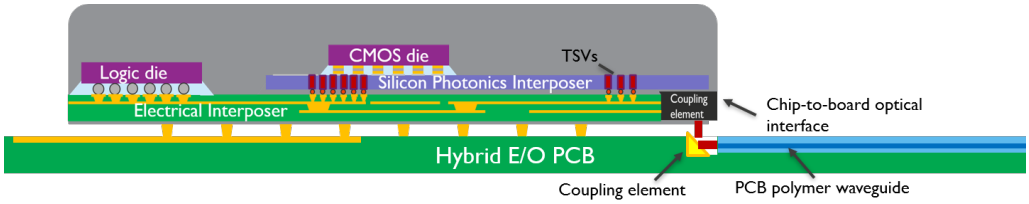


Fig. 1: A 2.5D/3D electro-optic scheme to integrate Silicon Photonics interposer with board-level optical interconnects [5].

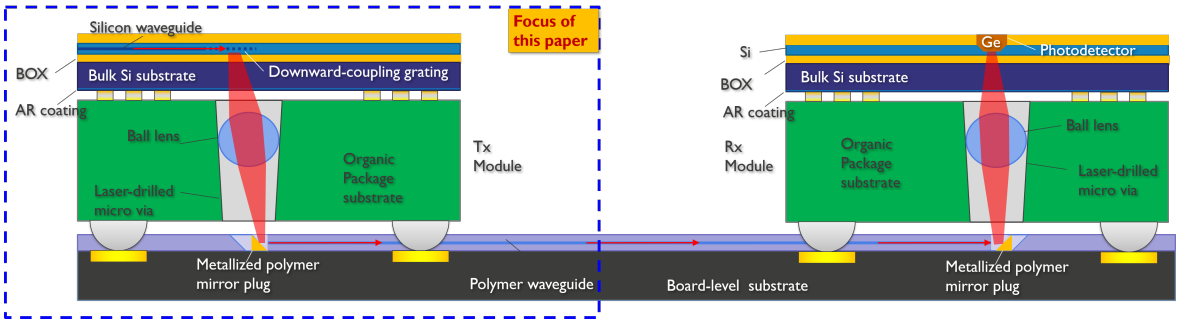


Fig. 2: Overview of the proposed chip-to-board coupling interface [6].

coupler or an upward-directionality based grating coupler. Using this approach, memory and logic dies can be assembled on the top of an optical interposer with TSVs and microbumps for low-frequency electrical interconnections (Fig. 1). In this framework, we demonstrated earlier a novel approach to integrate a silicon photonics chip, ball lens embedded in a package substrate and a board-level multimode interconnect [5], [6]. We showed that by embedding the ball lens in a tapered via of a package substrate, an expanded optical beam from a silicon photonic chip interposer can be refocused and coupled to a board-level optical interconnect with a good alignment tolerance. In this paper, we expand upon our earlier work to put forth a comprehensive analysis from the simulations for the proposed concept and showcase an improvement of coupling performance across the optical interface. This paper is organized in the following manner: firstly, the proposed concept is described in detail, followed by a discussion on the tolerance analysis obtained using ray-trace based system-level modeling; then, the fabrication and assembly of all the components is described; lastly, the experimental results are compared with the simulations and relevant conclusions are drawn.

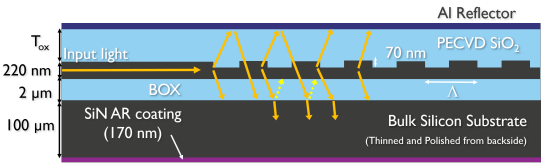
II. Description of the Concept

The operating principle and the different components within the concept are explained as follows (Fig. 2): The first component is a silicon photonics chip that comprises a downward directionality output grating coupler, which diffracts the optical signal downwards at an angle off-normal into the bulk substrate of an SOI chip. The photonics chip is lapped and polished from the backside, and then coated with an anti-reflection layer [11]. The second component is a ball lens that is integrated in the laser-drilled via of a package substrate, at an appropriate height to refocus the incoming expanded optical beam from the backside of the photonics chip. The focused optical beam is coupled into a polymer multimode waveguide (the third component), after reflecting off a 40° metallized mirror plug placed in a cavity laser-ablated in front of the waveguide facet. The far end of the polymer waveguide is connected to a multimode fiber to detect the resultant optical power coupled from the photonics chip-to-polymer waveguide. Also, instead of a metallized mirror plug, TIR mirrors [12] can be integrated within the polymer waveguide to couple the focused beam into the waveguide core, with a caveat that the TIR effect is lost if an optically transparent underfill material penetrates the ablated cavity. The optical power from the multimode waveguide, can in principle, be coupled in a similar way using a ball lens to a surface-illuminated photodetector integrated at the receiver side to perform high-speed opto-electronic conversion of the data in a server-scale computing environment (also shown via Rx module in Fig. 2) [13]. Also, the via-processing technology available across PCB manufacturing facilities can be leveraged to perform a pick-and-drop approach for the placement of the ball lens inside the tapered via of a substrate on a larger volume. Lastly, this concept allows for a simplified backside wafer-scale processing compared to the case of backside integration of microlenses [14], [15].

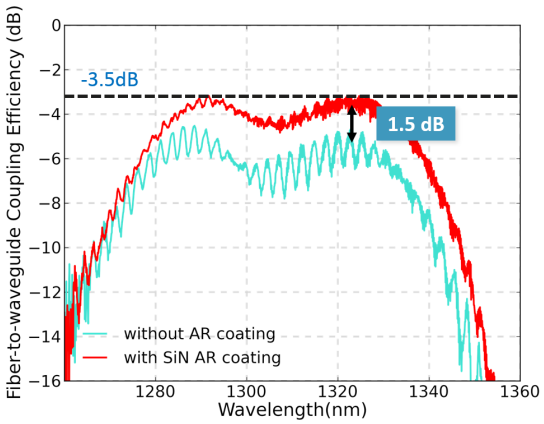
III. Design and Simulation

A. Through-Substrate Grating Couplers

Grating couplers are an important passive optical component that has enabled the wafer-scale testing of integrated photonic circuits [16]. Despite their limitation of relatively narrow bandwidth and sensitivity towards polarization compared to edge-couplers, they have a large alignment tolerance and hence, offer benefits from the standpoint of performing die-level or wafer-level high throughput testing and fiber-attach. So far, these couplers have been primarily demonstrated for upward



(a)



(b)

Fig. 3: a) An illustration of a through-substrate diffracting SOI grating coupler ($\Lambda = 490$ nm, fill-factor = 0.5); b) A reduction in Si-air Fresnel reflections and 1.5 dB improvement in the coupling efficiency of the grating couplers occurs when a SiN anti-reflection coating is deposited at the polished backside of the chip.

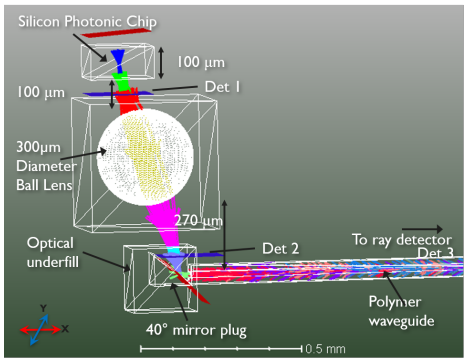
directionality for fiber-to-chip or chip-to-chip coupling. In order to improve the upward directionality of these couplers, one of the employed methods has been to deposit a metal reflector between the BOX layer and the bulk silicon substrate [17], [18]. Similarly, in order to achieve an improved directionality in the downward direction towards the SOI substrate, a metal reflector was deposited over an oxide clad above the grating, in this work. For an optimized oxide thickness, a maximized constructive interference takes place between the downward diffracted signal component from the grating and the reflected component from the metal reflector, resulting in a net downward directionality (Fig. 3a). As explained in the previous section, the benefit of developing a downward (backside) diffracting grating coupler is to enable face-up integration of photonic chips, and utilize space on the topside device layer for die-stacking and for other potential requirements needed in 2.5D/3D integration. For a maximum constructive interference, the oxide thickness (t_{ox}) needed between the grating and the reflector is given by:

$$t_{\mathrm{ox}} = \frac{\cos\theta_{\mathrm{ox}}}{n_{ox}} \cdot \left(\frac{m\lambda}{2} - \frac{t_{\mathrm{Si}} . n_{\mathrm{avg}}}{\cos\theta_{\mathrm{avg}}} \right) \tag{1}$$

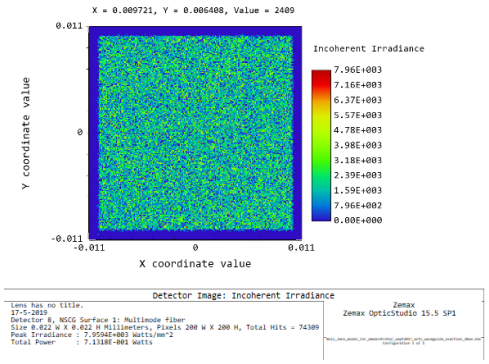
where t_{ox} is the thickness of the oxide cladding, t_{Si} is the thickness of the partially-etched silicon (70 nm in this case), m is an integer, n_{ox} is the refractive index of the oxide cladding, n_{avg} is the average refractive index of the etched grating, θ_{ox} the diffracted beam angle in oxide and θ_{avg} the corresponding diffracted beam angle in the averaged refractive index material of the grating. Keeping standard SOI wafer parameters of 220 nm thick Si waveguide layer and a 2 μm thick buried oxide layer (BOX), the TE-polarized gratings were designed with a period of 490 nm and etch depth of 70 nm in the FDTD simulations that corresponds to a 10° fiber-coupling angle in air and a 2.81° angle in silicon substrate. For an optimized downward directionality, a 2 μm oxide thickness between the reflector and the grating was verified with the help of 2D FDTD simulations. On performing fiber-coupling measurements from the chip backside, a -5 dB peak coupling efficiency was obtained (Fig. 3b). The ripples seen in the spectrum were caused by Fresnel reflections from the silicon-air interface and were reduced after a 170 nm thick anti-reflective SiN coating was deposited at the backside of the chip surface. This also resulted in a 1.5 dB improvement bringing the peak fiber-to-waveguide efficiency to -3.5 dB as shown in Fig. 3b.

B. System-level Optical Design

Although wave-propagation based modeling is needed to design the integrated-optic devices, a ray-trace approach helps the designer to arrive at a systemwide figure of merit when designing an optical system comprising of both integrated-optic and bulk-optic components. In order to gauge the coupling performance of the overall system described earlier (Fig. 1), a non-sequential ray-trace model was developed in Zemax as shown in Fig. 4a. The photonics chip was modeled with a silicon substrate of 100 μm thickness. An anti-reflective coating at the backside of the silicon substrate was also included in the model. Under the ray-based approximation, it is critical to know the far-field divergence and diffracted angle of the designed grating such that it can be incorporated in the source of the ray-trace model. These parameters were obtained from the FDTD simulations of the grating performed earlier. With an assumption of Gaussian beam propagation and a starting mode-field diameter of 9.2 μm from a downward-directionality grating coupler, the beam diameter at the end of a 100 μm thick substrate of the chip is expected to be 10.4 μm while it expands further to about 15.5 μm at the aperture of the ball lens. Also, relevant material parameters for ruby-doped sapphire ball lens (300 μm diameter) [19], epocore/epoclad based polymer waveguide [20] were plugged into the model. Although a ball lens with a larger diameter could also be used, the choice of the selection of 300 μm diameter ball lens was guided by the fact that a larger diameter ball lens will lens will increase the overall chip-to-board distance. The minimum dimension of the ball lens available off-the shelf was 300 μm, and hence, smaller dimensions were not considered. From an overall design perspective, the chip-to-polymer waveguide distance was constrained by package substrate's thickness that was chosen to be 500 μm in the model. A statistical distribution of rays from the source were traced onto a detector that was placed at the far end of the waveguide to simulate the percentage of rays coupled into the core of the waveguide. The simulations were performed for the O-band center wavelength of 1310 nm. It was found out that for a particular chip-to-board distance and an optimal alignment of all the components, a 71% (-1.5 dB) coupling



(a)



(b)

Power Loss	Percentage of Rays Detected	Loss in dB
No Loss due to presence of AR coating at the backside of the chip (Det1)	100% rays detected after the rays exit the chip	0 dB
Loss due to absence of AR coating on the ball lens (Det2)	85% rays detected after the ball lens	0.7 dB
Total chip to polymer waveguide coupling efficiency (Det 3)	71% rays detected at the end of waveguide core (14% lost in coupling)	0.8 dB
	Net Total Loss	**1.5 dB**

(c)

Fig. 4: (a) A non-sequential ray-trace model for the proposed photonic chip-to-board coupling concept. (b) Detector map for the rays that get traced into the polymer waveguide. The chip-to-polymer waveguide coupling efficiency was found to be 71%. (c) Loss Distribution from different coupling elements/interfaces determined from the ray-trace model.

efficiency can be achieved when coupled into a waveguide with a cross-section of 20×20 μm^2 (Fig. 4b). As shown in Fig. 4c, 15% rays are reflected by the ball lens due to the absence of an AR coating on the ball lens that were used in the experiment, resulting in a 0.7 dB loss from a total loss of 1.5 dB. The remaining 0.8 dB loss could be attributed to various mechanisms with respect to coupling from the mirror plug to the polymer waveguide, such as some rays not satisfying the TIR condition post-coupling etc. Also, a large $\pm$17 μm 1-dB alignment tolerance was obtained from the ray-trace model for a vertical displacement of the ball lens inside the via of the package substrate (Fig. 5). Furthermore, a study on the lateral and angular alignment tolerances of the chip, package and board-level waveguide was performed (Fig. 6). Initially, a

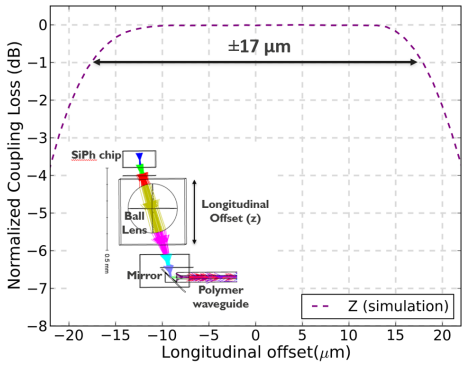


Fig. 5: A large $\pm$17 μm 1-dB longitudinal alignment tolerance of the ball lens inside the via of the package substrate was obtained from the ray-trace model.

package-to-board alignment tolerance analysis was carried out as a function of different dimensions of the waveguide core with a square cross-section.

On the expected lines, as the waveguide core dimension reduces, the package-to-board lateral alignment tolerance reduces (Fig. 6a). However, the package-to-board angular alignment tolerance (about y-axis, ref. Fig. 4) was found to remain consistent up to a waveguide core width of 15 μm (Fig. 6d). Hence, a 20 μm core width was chosen to investigate the alignment tolerances in greater detail. This dimension also falls well within the aperture limit of the Ge-based photodetector at the receiver side for high bandwidth performance [13]. This paper however, does not delve into the optical coupling design of the receiver side. From the model, a 1-dB chip-to-package and a package-to-board lateral alignment tolerance was derived to be $\pm$5 μm and $\pm$8 μm respectively (Fig. 6b and 6c). On the other hand, a $\pm$5° 1-dB chip-to-package and package-to-board angular alignment tolerance was estimated from the model for both the cases (Fig. 6e and 6f). Since, the effect of lateral and angular displacements of the chip-to-package and package-to-board have been computed under the assumption of both being mutually exclusive events, we briefly discuss here the impact on these misalignments in the presence of other non-idealities.

Effect of Chip-to-Package Misalignments: If one takes a look at the current state of the art in Cu-pillar technology [21]–[24], that has replaced solder based bumping technology, pitches as low as 40 μm are already in production [22], while a pitch of 20 μm with lithographically defined 10 μm diameter Cu-pillars have been demonstrated recently [25]. Thus, the lateral/angular displacement of the chip-to-package substrate is expected to be very small, which implies that the tolerances obtained for package-to-board misalignment from the ray-trace model would be more relevant than the chip-to-package misalignment as discussed in the next subsection.

Effect of Package-to-Board Misalignments: The effect of residual displacement of solder joints after the reflow of BGA packages is well-known and hence, the derived chip-to-package alignment tolerance values can be called ideal with an

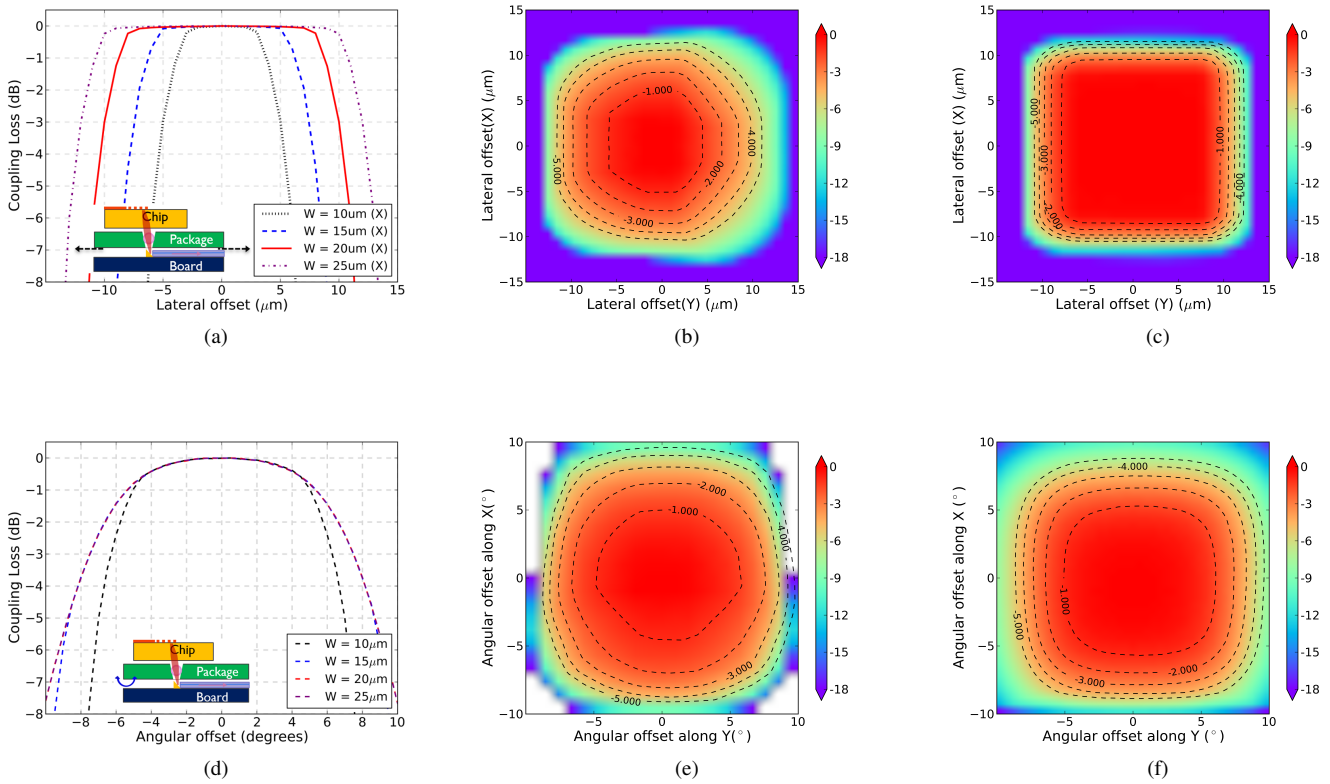


Fig. 6: (a) Package-to-board lateral alignment tolerance as a function of waveguide width; (b) Chip-to-package 1-dB lateral alignment tolerance: ± 6 μm ; (c) Package-to-board 1-dB lateral alignment tolerance: ± 8 μm; (d) Package-to-board 1-dB angular alignment tolerance as a function of waveguide width; (e) Chip-to-package 1-dB angular alignment tolerance: $\pm 5°$; (f) Package-to-board 1-dB angular alignment tolerance: $\pm 5°$. Figs. b-c and e-f have been evaluated for a waveguide cross-section dimensions of 20×20 μm^2 in the ray-trace simulations.

assumption of a perfect package-to-board alignment. However, it is expected that such misalignments can be shrunk further with the use of auxiliary pads in combination with the main metal pad. This helps to compensate for the lateral movement of the package substrate during solder reflow by tuning the surface tension of the molten solder [26]. To have a better estimate of the worst case loss, statistics from a Monte-Carlo based analysis fed with realistic input conditions might bring more insight, which is beyond the scope of discussion in this article.

IV. Fabrication and Packaging

A. Photonic Chip Fiber-Attach

The photonic chips with a 2 μm oxide thickness deposited over the grating couplers were obtained from the wafers that were fabricated in imec's 200 mm Si Photonics pilot line [27]. The post-processing of these chips was done later to deposit a Ti/Al reflector over the top oxide cladding on the gratings. These chips were bonded from the device topside onto a glass substrate with wax in order to perform thinning and polishing of the Si substrate from the backside of the chip. Starting with a full-chip thickness of 650 μm, a final Si thickness of 100 μm was obtained using a Logitech PM5 lapping and polishing tool. The rms surface roughness after polishing was measured to be within 15-20 nm using an optical profilometer. After the release of the chips from the glass carrier using Ecoclear solvent, a 170 nm thick SiN anti-reflective film was deposited on the backside of the chip. The input grating on the photonics chip was fiber-attached laterally with a $40°$ angle-polished fiber [28]. It is to be noted that the Al metal reflector was not deposited on the input grating to allow fiber-attachment from the topside of the die. The angle-polished fiber was glued in a silicon V-groove and was aligned actively to the topside of an input grating of the photonics chip. Subsequently, an acrylate (NOA-61) that is UV-curable, was applied few mm away from the end of the polished fiber facet, which due to its capillary action, then spreads between the fiber-chip surface. The applied acrylate also behaves as an index-matching medium between the oxide-air clad (on the chip) and fiber-air interface thereby resulting in the reduction of the Fresnel reflections. The curing of the dispensed acrylate was done with the help of a UV lamp. The fiber-attached die could then be used as a discrete component to perform active alignment with respect to the ball lens and polymer waveguide.

B. Ball Lens Embedded Through-Package Via

There are a few key advantages of integrating a lensed component inside the package substrate: a) there is no need of any additional backside processing of the photonics interposer chip for lensed coupling [14], [15]; b) the spherical shape of the ball lens allows it to self-align inside the sloped via of a particular diameter, thereby providing control over the lens height, and lateral and angular misplacement; and c) the assembly process gets relatively simplified and less constrained with a single lens in contrast to using two microlenses, each on the chip and the board-level coupling interface which might result in varying magnitude of lateral/angular misalignment per component due to the physical displacement of the components during solder reflow [29], [30].

For our experiment, a glass fiber reinforced organic package substrate was used to fabricate the vias. Organic package substrates have been ubiquitous in electronic manufacturing and assembly for advanced packaging applications. They are not only cheaper in cost compared to alternatives such as glass and ceramic substrates, but also provide relative ease in manufacturing. Also, by stacking multiple laminates together with copper layers, a multi-layer substrate helps in providing an increased electrical fan-out and I/O density. Despite not making any electrical interconnection on the package substrate in the experimental demonstration, the motivation behind using this substrate was also derived from the possibility of wire-bonding a driver chip on the package substrate to perform on-chip modulation of the optical signal in the future. Hence, a 400 μm thick organic package substrate was chosen and a tapered via was created through by using Nd-YAG laser ablation. The diameter of the via from both the sides of the substrate was determined using an optical microscope. From this measurement, the laser induced taper angle was determined to be 1.6° $\pm$ 0.5°. A ruby-doped sapphire ball lens with a diameter of 300 μm was placed in the fabricated via of the substrate. Thereafter, an optical profilometer scan was performed over both sides of the lensed package substrate to determine the position of the ball lens inside the via. As shown in Fig. 7, the lens was placed about 25 μm and 52 μm from the top and the backside of the via opening of the substrate respectively.

C. Mirror Plug

In order to deflect the beam oriented at 10° angle in oxide, a 40° mirror plug was fabricated from a polyimide substrate as described in [31]. A final thickness of 100 μm for the mirror plug was obtained to make it comparable to the total thickness of the polymer waveguide stack. Thereafter, the mirror plug was Au-coated using e-beam evaporation. The surface roughness (rms) of the mirror plug was measured to be between 15-20 nm over a surface area of 50×50 μm^{2}using optical profilometer and AFM. After the mirror plug was inserted inside the ablated cavity in front of the polymer waveguide, the air gap between the mirror plug and waveguide cross-section was filled with NOA-61 material to accomplish two purposes: a) minimize Fresnel reflections from waveguide-air interface and b) ensuring the beam angle to be oriented at 10° before it is incident on the surface of the mirror-plug.

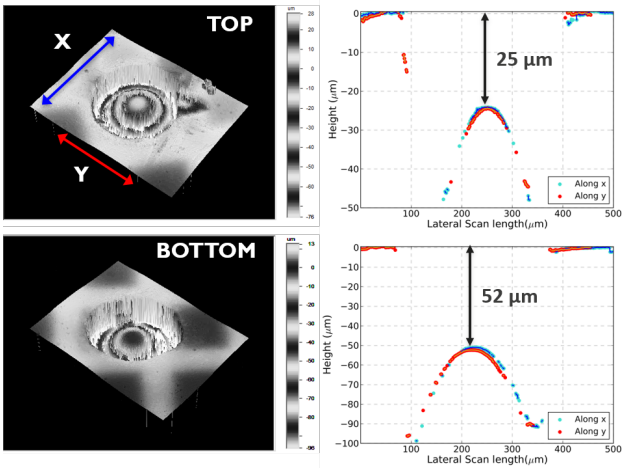


Fig. 7: Topside and backside white-light optical profilometry scans of the package substrate with the ball lens placed inside the via.

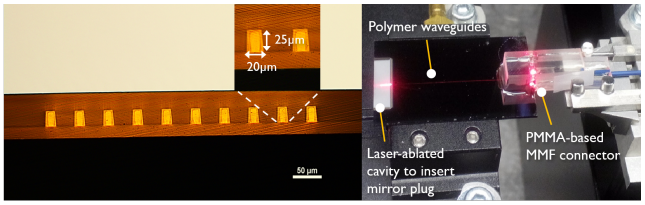
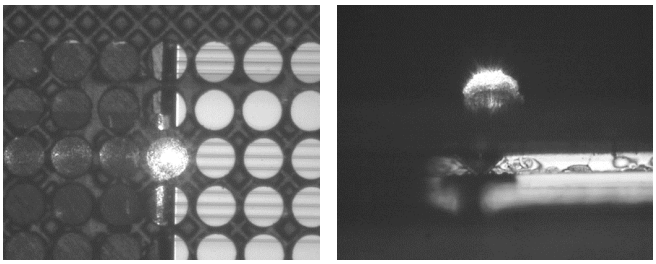


Fig. 8: (a) A 20×25 μm^2 cross-section was measured for the fabricated polymer multimode waveguides and (b) An image of polymer waveguides fabricated on a Si-substrate with a laser-ablated cavity made to insert the mirror plug in front of the polymer waveguide facet and a multimode fiber based connectorization at the opposite end of the waveguide.

D. Board-level Optical Interconnects

Although both polymer and glass based optical interconnects have been demonstrated in the past [32], [33], it is well-known that the polymer waveguide technology provides simplicity, flexibility and low-cost prospect with good optical properties. For the experimental demonstration, the substrate to fabricate the polymer waveguides was chosen to be silicon due to its high flatness and the benefit of spinning on the polymer layers easily. For waveguide patterning, the UV laser direct-write technique using Heidelberg DWL66 system was employed [34]. The technology has the benefit of being compatible with panels having a length of several centimeters [35]. The waveguides were fabricated using Epocore/Epoclad (micro resist technology GmbH) material and had core dimensions of 20×25 μm^2 (Fig. 8). A propagation loss of 0.8 dB/cm was measured in the O-band for the fabricated multimode waveguides using the cutback method. Subsequently, a cavity (3 mm-wide) was made using UV-excimer laser ablation at an end of the facet of the polymer waveguide, so that the mirror



(a) (b)

Fig. 9: (a) Top view and (b) Side view of the ball lens in the package substrate well-aligned with respect to the mirror plug-waveguide interface.

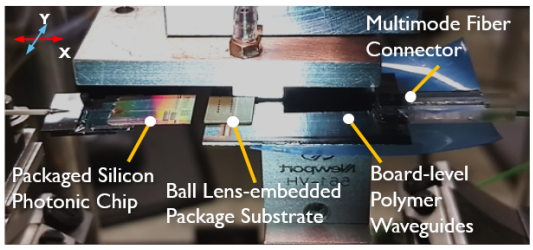


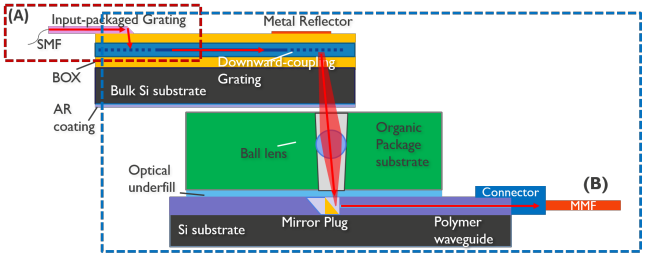
Fig. 10: An image to showcase the experiment performed to assess the alignment tolerance for chip-to-board coupling. After the board-level substrate and the package substrate were individually held with a vacuum chuck, and aligned well to each other, the fiber-attached photonic die was brought over the lens embedded via to perform active alignment.

plug can be inserted in it. The other end of the waveguide facet was connected to a 0.2 NA 50 μm core diameter multimode fiber (Fig. 8(b)).

V. Results and Discussion

Since the prime objective of the experiment was to evaluate the link performance and chip-to-package lateral alignment tolerance, the components were actively aligned and not passively bonded/soldered to each other. Firstly, the board-level silicon substrate with connectorized polymer waveguides was placed on a vacuum chuck. Next, the lens integrated package substrate was aligned actively to the mirror plug-waveguide interface with the help of an optical fiber (Fig. 9). Subsequently, the fiber-attached photonics chip was brought over the lens-integrated via of the package substrate and an active alignment was performed to optimize the coupling across the chip-to-board level polymer waveguide interface (Fig. 10).

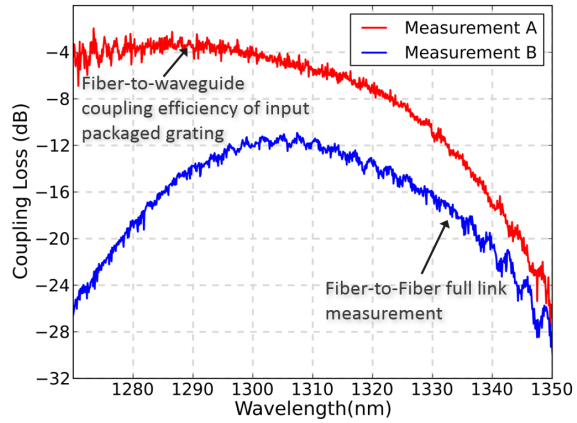
The results obtained from the experiment are shown in Fig. 11. In order to evaluate the performance of the entire link, firstly, the coupling efficiency spectrum of a fiber-attached input grating was determined (Measurement A in Figs. 11a and 11c). Then, after the alignment of the chip and the package substrate with respect to the board-level polymer waveguides was performed, the fiber-to-fiber full link spectrum was measured (Measurement B in Figs. 11a and 11c). The procedure to derive measurement A is described as follows: Firstly, the spectrum of the metallized output grating coupler was measured on a different location on the chip (similar to the schematic in the inset of Fig. 12). This was done to obtain a reference measurement of the downward-diffracting grating coupler with a metal reflector (Fig. 3b). Thereafter, on the actual testsite, the fiber-attachment of the input grating was performed as described earlier in Section IV-A. Then, the coupling efficiency spectrum for the fiber-attached input grating to the output grating downward coupled to a single-mode fiber was recorded. This measurement was then normalized with respect to the reference measurement of the grating with a metal reflector performed earlier, which enabled us to derive the fiber-to-waveguide coupling efficiency of the fiber-attached input grating shown as Measurement A in Fig. 11c. It can be seen that while the peak coupling efficiency of the fiber-attached input grating was measured to be -3.5 dB (Measurement A), the efficiency was measured to be -5 dB at the primary O-band wavelength of 1310 nm (Figs. 11a and 11c). A nonoptimal angle of the polished fiber that was used to package the input grating resulted in a blue shift of the peak wavelength in this measurement. Next, the fiber-to-fiber full link spectrum is shown as Measurement B in Fig. 11c, i.e., from the single mode angle-polished fiber attached to the input grating to the coupling interface and then to the multimode fiber attached at the other end of the polymer waveguide. Using these two measurements and other sources of losses determined earlier, the true efficiency across the chip-to-polymer waveguide coupling interface was evaluated to be -3.4 dB at 1310 nm wavelength (Fig. 11b). Here, the optical interface comprised of the output grating with a metal reflector, ball lens and the mirror plug-polymer waveguide interface, as tabulated in Fig. 11b. The measured efficiency can be improved further by improving the grating directionality as described here [11]. It was shown that reducing the thickness of Ti adhesion layer (from 5 nm to 2 nm) between the Al reflector and top oxide results in a lesser absorption and better directionality. As shown in Fig. 12, a -2.3 dB coupling efficiency can be obtained when the grating output is coupled to a single-mode fiber (an improvement of 1.2 dB in comparison to the efficiency shown in Fig. 3b), while a -1.7 dB efficiency is obtained when coupled to a 50 μm core multimode fiber. Moreover, the gratings can be apodized to achieve a Gaussian-like diffracted mode profile and also, help remove the two peak nature of the coupling spectrum. Furthermore, the ball lenses can be AR-coated to reduce the Fresnel reflections by 0.7 dB. Hence, a less than 2 dB coupling loss can be achieved over the optical interfaces evaluated in the experiment earlier. After the board-level substrate and the package substrate were individually held with a vacuum chuck, and aligned well to each other, a lateral alignment of the fiber-attached photonic die was performed over the the lens embedded via of the package substrate. A 1-dB chip-to-package lateral alignment tolerance of ± 7 μm was measured that was close to the ± 6 μm alignment tolerance estimated from the ray-trace model (Fig. 11d). The reason for a marginal increment in the measured alignment tolerance can be related to an overestimation of the far-field divergence calculated from



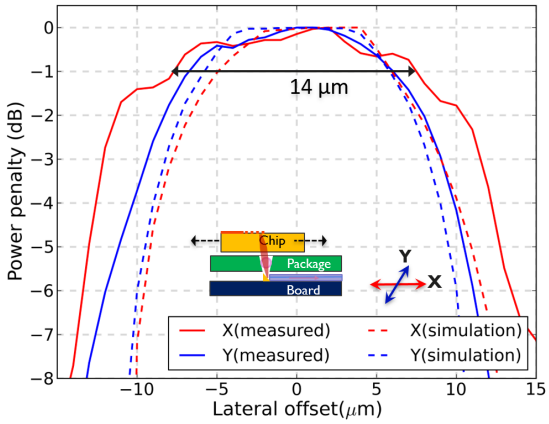
(a)

Various Components & Interfaces	Loss (dB) at λ=1310 nm
Silicon Photonic Chip	
Input Packaged Grating	5
4mm SOI Waveguide Propagation Loss (3dB/cm)	1.2
Output Grating with a Metal Reflector	
Organic Package Substrate	
Ruby-doped Sapphire Ball Lens	3.4
Board-level Optical Interconnect	
40° Au-coated Mirror plug	
3cm Polymer waveguide propagation loss(0.8 dB/cm)	2.4
Fiber-to-Fiber Loss Across The Complete Link	12

(b)



(c)



(d)

Fig. 11: (a) The coupling efficiency spectrum measurement was conducted in two steps: (A) Measurement of coupling efficiency of the fiber-attached input grating and (B) Measurement of fiber (SMF)-to-fiber (MMF) spectrum of the entire link; (b) A coupling efficiency of -3.4 dB was measured at λ=1310 nm across the actual coupling interface i.e. output grating, ball-lens and mirror plug - polymer waveguide interface; (c) Measurement A: Single-mode fiber-to-grating CE spectrum of fiber-attached input grating; Measurement B: fiber (SMF)-to-fiber (MMF) full link spectrum (both A and B are described schematically in Fig.(a)); and (d) A 1-dB chip-to-package lateral alignment tolerance of 14 μm was measured (bold lines) compared to 12 μm obtained from the simulations (dotted lines, also refer Fig. 6b).

the FDTD simulations of the output grating with a metal reflector. It is also noted that in contrast to the simulation, the alignment tolerance in the X-direction was unsymmetrical to that in the Y-direction which is correlated to the coupling in a 20×25 μm^2 dimension of polymer waveguide. Overall, it can be said that the numbers derived from the ray-trace model in Section III-B can help accurately predict the lateral and angular alignment accuracies for the proposed coupling concept.

Lastly, this paper has focused on the concept of assessing the various tolerances and efficiency involved in the proposed optical coupling interface. In order to accommodate a particular channel density, a cluster of multiple channels can be transmitted via each of the ball lenses placed successively in the substrate, where appropriate lens diameter and pitch would have to be determined accordingly. Also, if the proposed coupling concept were to be applied to couple to single-mode board-level optical interconnects, the single-mode condition for polymer waveguides would have to be relaxed by tuning the refractive index contrast between the core and the cladding material to go beyond 10×10 μm^2 waveguide cross-section to take advantage of the relaxed lateral and angular alignment tolerances (Fig. 6a). The ray-trace analysis performed in this work, would not be accurate in such a scenario and the optical model would need to be retuned to take overlap integral of the modes across the coupling interface. Alternatively, a possibility of employing a few-mode waveguide based coupling mechanism can not be completely ruled out either. On a separate note, although a $\pm$8 μm package-to-board lateral alignment accuracy looks good from the optical coupling standpoint, it still does not fall under the conventional assembly-level tolerances. We believe that the difference in margin can be reduced by adopting the technique of employing four auxiliary pads with the main metal pad so that the solder flow distribution can be tuned for minimum displacement during reflow. A less than $\pm$1 μm alignment accuracy has been derived recently for chip-to-board solder based connections and similarly, has the potential to improve

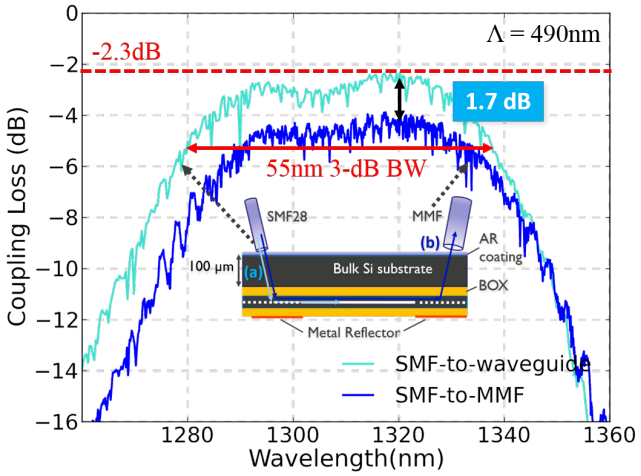


Fig. 12: A coupling efficiency of 1.7 dB was measured for an improved downward-directionality grating when coupled to a multimode fiber. This was evaluated by subtracting the single-mode coupling efficiency of the grating from fiber (SMF)-to-fiber (MMF) measurement [11].

the residual displacement of the reflowed solder bumps of BGA packages as well [26]. Also, for a solder bump diameter of 1 mm, a practical misalignment at the solder bump joint is ± 10 μm [36], which is closer to the 1-dB package-to-board alignment tolerance. So, a proper choice of solder bump dimension alongwith well-designed auxiliary pads can help in minimizing the package to board displacement.

VI. Conclusion

We have demonstrated a novel approach to integrate a silicon photonics interposer chip with board-level polymer waveguide by embedding the ball lens in a tapered via of a package substrate. A coupling efficiency of -3.4 dB across the optical interfaces between a photonic chip and polymer waveguide was deduced from the measurements at the wavelength of 1310 nm. Moreover, it was shown that an efficiency higher than -2 dB can be achieved across the proposed chip-to-board coupling interface by optimizing the grating directionality even further. A key outcome of the conducted measurements was a chip-to-package 1-dB lateral alignment tolerance of 14 μm for coupling from a downward directionality grating into a 20×25 μm^2 cross-section polymer multimode waveguide. These figures for lateral alignment tolerance were shown to match well with the data obtained from ray-trace simulations. Although the angular alignment measurement was not performed during the experiment, similar numbers as those obtained from the model are expected to be obtained. Finally, the demonstration of this concept highlight a few potential advantages: the self-alignment aspect of the ball lens in a sloped via of the package substrate, simplified chip-backside processing, compatibility with the existing PCB manufacturing and assembly flows and a relaxed lateral and angular alignment tolerances for coupling to board-level multimode (or few-mode) optical interconnects, interfaced with a photodetector at the receiver side. Although the experiment was conducted using active alignment, the numbers obtained from the tolerance analysis for the proposed coupling interface has a potential to simplify the process of passive assembly [37].

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References

[1] M. A. Taubenblatt, "Optical interconnects for high-performance computing," *Journal of Lightwave Technology*, vol. 30, no. 4, pp. 448–457, 2012.

[2] K. Schmidtke, *Designing 100G optical connections*, 2017 (Mar 8, 2017). [Online]. Available: https://code.fb.com/data-center-engineering/designing-100g-optical-connections/

[3] Q. Cheng, M. Bahadori, M. Glick, S. Rumley, and K. Bergman, "Recent advances in optical technologies for data centers: a review," *Optica*, vol. 5, no. 11, pp. 1354–1370, 2018.

[4] B. J. Offrein, "Silicon photonics for the datacenter," in *Optical Fiber Communication Conference*. Optical Society of America, 2015, pp. W3A–4.

[5] N. Mangal, J. Missinne, J. V. Campenhout, G. V. Steenberge, and B. Snyder, "Through-substrate coupling elements for silicon-photonics-based short-reach optical interconnects," in *Optical Interconnects XIX*, vol. 10924. International Society for Optics and Photonics, 2019, p. 109240D.

[6] N. Mangal, J. Missinne, J. Van Campenhout, G. Van Steenberge, and B. Snyder, "Integration of Ball Lens in Through-Package Via to Enable Photonic Chip-to-Board Coupling," in *2018 IEEE 68th Electronic Components and Technology Conference (ECTC)*. IEEE, 2018, pp. 1140–1145.

[7] I. M. Soganci, A. La Porta, and B. J. Offrein, "Flip-chip optical couplers with scalable I/O count for silicon photonics," *Optics express*, vol. 21, no. 13, pp. 16 075–16 085, 2013.

[8] R. Dangel, A. La Porta, D. Jubin, F. Horst, N. Meier, M. Seifried, and B. J. Offrein, "Polymer Waveguides Enabling Scalable Low-Loss Adiabatic Optical Coupling for Silicon Photonics," *IEEE Journal of Selected Topics in Quantum Electronics*, vol. 24, no. 4, pp. 1–11, 2018.

[9] K. Kurata, Y. Suzuki, M. Tokushima, and K. Takemura, "Silicon photonics for multi-mode transmission," in *Optical Interconnects for Data Centers*. Elsevier, 2017, pp. 197–222.

[10] K. Takemura, Y. Ibusuki, A. Ukita, M. Kurihara, K. Kinoshita, D. Okamoto, J. Fujikata, K. Yashiki, Y. Suzuki, T. Horikawa *et al.*, "High density optical and electrical interfaces for chip-scale silicon photonic receiver," in *2017 International Conference on Electronics Packaging (ICEP)*. IEEE, 2017, pp. 250–254.

[11] N. Mangal, J. Missinne, G. Van Steenberge, J. Van Campenhout, and B. Snyder, "Performance Evaluation of Backside Emitting O-Band Grating Couplers for 100 μm-thick Silicon Photonics Interposers," *IEEE Photonics Journal*, 2019.

[12] N. Hendrickx, H. Suyal, G. Van Steenberge, A. McCarthy, A. Walker, H. Ottevaere, H. Thienpont, M. Taghizadeh, and P. Van Daele, "Laser ablation and laser direct writing as enabling technologies for the definition of micro-optical elements," in *Integrated Optics: Theory and Applications*, vol. 5956. International Society for Optics and Photonics, 2005, p. 59561B.

[13] J. Osmond, L. Vivien, J.-M. Fédéli, D. Marris-Morini, P. Crozat, J.-F. Damlencourt, E. Cassan, and Y. Lecunff, "40 Gb/s surface-illuminated Ge-on-Si photodetectors," *Applied Physics Letters*, vol. 95, no. 15, p. 151116, 2009.

[14] N. Mangal, J. Missinne, G. Roelkens, J. V. Campenhout, G. V. Steenberge, and B. Snyder, "Expanded-Beam Through-Substrate Coupling Interface for Alignment Tolerant Packaging of Silicon Photonics," in *2018 Optical Fiber Communications Conference and Exposition (OFC)*. IEEE, 2018, pp. 1–3.

[15] J. Missinne, N. T. Benéitez, N. Mangal, J. Zhang, A. Vasiliev, J. Van Campenhout, B. Snyder, G. Roelkens, and G. Van Steenberge, "Alignment-tolerant interfacing of a photonic integrated circuit using backside etched silicon microlenses," in *Silicon Photonics XIV*, vol. 10923. International Society for Optics and Photonics, 2019, p. 1092304.

[16] D. Taillaert, P. Bienstman, and R. Baets, "Compact efficient broadband grating coupler for silicon-on-insulator waveguides," *Optics letters*, vol. 29, no. 23, pp. 2749–2751, 2004.

[17] W. S. Zaoui, M. F. Rosa, W. Vogel, M. Berroth, J. Butschke, and F. Letzkus, "Cost-effective CMOS-compatible grating couplers with backside metal mirror and 69% coupling efficiency," *Optics express*, vol. 20, no. 26, pp. B238–B243, 2012.

[18] S. K. Selvaraja, D. Vermeulen, M. Schaekers, E. Sleeckx, W. Bogaerts, G. Roelkens, P. Dumon, D. Van Thourhout, and R. Baets, "Highly efficient grating coupler between optical fiber and silicon photonic circuit," in *Conference on Lasers and Electro-Optics*. Optical Society of America, 2009, p. CTuC6.

[19] *Sapphire and Ruby Ball Lenses*. [Online]. Available: https://www.edmundoptics.com/f/sapphire-and-ruby-ball-lenses/12451/

[20] *Epocore/Epoclad Material*, 2015. [Online]. Available: https://www.microresist.de/en/products/negative-photoresists/uv-lithography-broadband-and-i-line-exposure/epocore-epoclad-serien

[21] Y. Ohara, A. Noriki, K. Sakuma, K.-W. Lee, M. Murugesan, J. Bea, F. Yamada, T. Fukushima, T. Tanaka, and M. Koyanagi, "10 μm fine pitch Cu/Sn micro-bumps for 3-D super-chip stack," in *2009 IEEE International Conference on 3D System Integration*. IEEE, 2009, pp. 1–6.

[22] X. Zhang, J. K. Lin, S. Wickramanayaka, S. Zhang, R. Weerasekera, R. Dutta, K. F. Chang, K.-J. Chui, H. Y. Li, D. S. Wee Ho *et al.*, "Heterogeneous 2.5 d integration on through silicon interposer," *Applied Physics Reviews*, vol. 2, no. 2, p. 021308, 2015.

[23] J. De Vos, A. Jourdain, M. Erismis, W. Zhang, K. De Munck, A. La Manna, D. Tezcan, and P. Soussan, "High density 20μm pitch CuSn microbump process for high-end 3D applications," in *2011 IEEE 61st Electronic Components and Technology Conference (ECTC)*. IEEE, 2011, pp. 27–31.

[24] A. Garnier, L. Arnaud, R. Franiatte, A. Toffoli, S. Moreau, F. Bana, and S. Cheramy, "Electrical Performance of High Density 10 μm Diameter 20 μm Pitch Cu-Pillar with Chip to Wafer Assembly," in *2017 IEEE 67th Electronic Components and Technology Conference (ECTC)*. IEEE, 2017, pp. 999–1007.

[25] P. Coudrain, J. Charbonnier, A. Garnier, P. Vivet, R. Vélard, A. Vinci, F. Ponthenier, A. Farcy, R. Segaud, P. Chausse *et al.*, "Active interposer technology for chiplet-based advanced 3d system architectures," in *2019 IEEE 69th Electronic Components and Technology Conference (ECTC)*. IEEE, 2019, pp. 569–578.

[26] T. F. Marinis and J. W. Soucy, "Design of solder connections for self-assembly of optoelectronic devices," *Journal of Microelectronics and Electronic Packaging*, vol. 16, no. 1, pp. 1–12, 2019.

[27] P. Verheyen, M. Pantouvaki, J. Van Campenhout, P. Absil, H. Chen, P. De Heyn, G. Lepage, J. De Coster, P. Dumon, A. Masood, D. Van Thourhout, R. Baets, and W. Bogaerts, "Highly uniform 25 Gb/s Si photonics platform for high-density, low-power WDM optical interconnects," in *Integrated Photonics Research, Silicon and Nanophotonics*. Optical Society of America, 2014, pp. IW3A–4.

[28] B. Snyder and P. O'Brien, "Packaging process for grating-coupled silicon photonic waveguides using angle-polished fibers," *IEEE Transactions on Components, Packaging and Manufacturing Technology*, vol. 3, no. 6, pp. 954–959, 2013.

[29] M. Karppinen, T. Alajoki, A. Tanskanen, K. Kataja, J.-T. Makinen, K. Kautio, P. Karioja, M. Immonen, and J. Kivilahti, "Parallel optical interconnect between ceramic BGA packages on FR4 board using embedded waveguides and passive optical alignments," in *Electronic Components and Technology Conference, 2006. Proceedings. 56th*. IEEE, 2006, pp. 7–pp.

[30] H. Nasu, N. Nishimura, Y. Nekado, and T. Uemura, "Polymer Waveguide-Coupled Solderable Optical Modules for High-Density Optical Interconnects," in *Electronic Components and Technology Conference (ECTC), 2016 IEEE 66th*. IEEE, 2016, pp. 1087–1092.

[31] E. Bosman, "Integration of optical interconnections and optoelectronic components in flexible substrates," Ph.D. dissertation, Ghent University, 2010.

[32] L. Brusberg, S. Whalley, C. Herbst, and H. Schröder, "Display glass for low-loss and high-density optical interconnects in electro-optical circuit boards with eight optical layers," *Optics Express*, vol. 23, no. 25, pp. 32 528–32 540, 2015.

[33] R. Dangel, F. Horst, D. Jubin, N. Meier, J. Weiss, B. J. Offrein, B. W. Swatowski, C. M. Amb, D. J. DeShazer, and W. K. Weidner, "Development of versatile polymer waveguide flex technology for use in optical interconnects," *Journal of lightwave technology*, vol. 31, no. 24, pp. 3915–3926, 2013.

[34] A. Elmogi, E. Bosman, J. Missinne, and G. Van Steenberge, "Comparison of epoxy-and siloxane-based single-mode optical waveguides defined by direct-write lithography," *Optical Materials*, vol. 52, pp. 26–31, 2016.

[35] L. Dellmann, C. Berger, R. Beyeler, R. Dangel, M. Gmur, R. Hamelin, F. Horst, T. Lamprecht, N. Meier, T. Morf *et al.*, "120 Gb/s optical card-to-card interconnect link demonstrator with embedded waveguides," in *Electronic Components and Technology Conference, 2007. ECTC'07. Proceedings. 57th*. IEEE, 2007, pp. 1288–1293.

[36] Y. Ishii, S. Koike, Y. Arai, and Y. Ando, "SMT-compatible optical-I/O chip packaging for chip-level optical interconnects," in *2001 Proceedings. 51st Electronic Components and Technology Conference (Cat. No. 01CH37220)*. IEEE, 2001, pp. 870–875.

[37] Y. Martin, S. Kamlapurkar, J. W. Nah, N. Marchack, and T. Barwicz, "Solder Mobility for High-Yield Self-Aligned Flip-Chip Assembly," in *2017 IEEE 67th Electronic Components and Technology Conference (ECTC)*, May 2017, pp. 667–674.

Nivesh Mangal received his MSc (Engg.) degree in the area of integrated optics from Indian Institute of Science (IISc), Bangalore in 2013. He was a Research Engr. with the computational lithography group at IBM SRDC (now GlobalFoundries Inc.), Bangalore from 2014-15. He is currently working towards the Ph.D. degree in optical engineering with Optical I/O group, imec and CMST (Center for MicroSystems Technology), an imec-affiliated research lab at Ghent University, Belgium since 2015. His current research interests range from system-level optical design to passive silicon photonic devices, particularly gratings and edge couplers, fiber-chip packaging and micro-optical components for board-level optical interconnects. He is also a member of IEEE Photonics Society, SPIE and OSA.

Jeroen Missinne received the Master of Science degree in Electrical Engineering in 2007 and his PhD in Electrical Engineering in 2011, both at Ghent University, Belgium. He is currently employed as part-time professor at Ghent University and employed at the CMST (Center for MicroSystems Technology), an imec-affiliated research lab at Ghent University. His research involves photonic sensors and photonic packaging, with activities in mechanically flexible photonics, polymer optical waveguides, integration of optical and optoelectronic components, optical coupling to photonic integrated chips and laser-based technologies.

Joris Van Campenhout received the Masters degree in physics engineering, in 2002, and the Ph.D. degree in electrical engineering, in 2007, both from Ghent University, Ghent, Belgium. After his Ph.D., he worked as a Postdoctoral Researcher with the IBM T. J. Watson Research Center, New York, NY, USA. In 2010, he joined imec, Belgium, where he is currently the Program Manager, Optical I/O.

Bradley Snyder (S'10) received the B.S. degree in computer engineering and the M.S. degree in electrical engineering with focus in electro-optics, both from the University of Dayton, Dayton, OH, USA, in 2002 and 2005, respectively, and the Ph.D. degree in applied physics from the Tyndall National Institute, University College Cork, Cork, Ireland, in July 2013. He was a Sr. Systems Engineer with Reed Elsevier Technology Services from 2000 to 2006, and a Software Developer with ColeSoft Marketing, Inc. from 2006 to 2009. After completing his doctoral studies, he worked as a Sr. R&D Engineer with imec in Leuven, Belgium from 2013-2018 and currently works in a Silicon Valley photonic quantum computing startup. His principal research interests include photonic integration and packaging.

Geert Van Steenberge is a part-time professor at Ghent University, and R&D team leader at imec. He obtained a PhD degree in Electrical Engineering from Ghent University in 2006, for his work on board-level parallel optical interconnects. His research interest includes on-board optics, electronics-photonics integration, polymer and glass waveguide based optical interposers, free-space optical coupling to photonic integrated circuits, low-temperature soldering, and high-speed assembly of micro-components based on laser-induced forward-transfer. He holds 9 patents or patent applications and has authored or co-authored over 100 papers in the field of photonics packaging and integration.