Real-Time 100-GS/s Sigma-Delta Modulator for All-Digital Radio-Over-Fiber Transmission

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Abstract—All-digital radio-over-fiber (RoF) transmission has attracted a significant amount of interest in digital-centric systems or centralized networks because it greatly simplifies the front-end hardware by using digital processing. The sigma-delta modulator (SDM)-based all-digital RoF approach pushes the digital signal processing as far as possible into the transmit chain. We present a real-time 100-GS/s fourth-order single-bit SDM for all-digital RoF transmission in the high-frequency band without the aid of analog/optical up-conversion. This is the fastest sigma-delta modulator reported and this is also the first real-time demonstration of sigma-delta-modulated RoF in the frequency band above 24 GHz. 4.68 Gb/s (2.34 Gb/s) 64-QAM is transported over 10-km standard single-mode fiber in the C-band with 6.46% (4.73%) error vector magnitude and 3.13 Gb/s 256-QAM can be even received in an optical back-to-back configuration. The carrier frequency can be digitally tuned at run-time, covering a wide frequency range from 22.75 to 27.5 GHz. Besides, this high-speed sigma-delta modulator introduces less than 1 μs latency in the transmit chain. Its all-digital nature enables network virtualization, making the transmitter compatible with different existing standards. The prominent performance corroborates the strong competitiveness of this SDM-based RoF approach in high-frequency RoF 5G communication.

Index Terms—All-digital transmitter, FPGA, quantization noise, radio-over-fiber, sigma-delta.

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I. INTRODUCTION

THE 5G wireless networks drive research in the direction of massive device connectivity, high data rates, decreased latency, and sustainable cost [1]. A centralized radio access network (C-RAN) in combination with radio-over-fiber (RoF) technology is viewed as one of the essential elements to address the challenges imposed by 5G [2]. Three different realizations of the radio-over-fiber link, including digitized radio-over-fiber (DRoF), analog radio-over-fiber (ARoF) and sigma-delta-over-fiber (SDoF), have been thoroughly discussed in [3], [4]. SDoF features superior resilience against noise and nonlinear impairments from both optical and microwave components, and a simple structure with reduced latency at the remote radio unit (RRU). The latter is beneficial to large-scale distributed antenna systems and ultra-dense networks such as the one proposed in [5]. In [3], we have verified the performance of this SDoF approach using low-cost off-the-shelf components by transmitting 4 parallel lanes of 3.5 Gb/s 256-QAM signals, processed by 7-GS/s sigma-delta modulators (SDMs) on a 3.5 GHz carrier and transported over 20 km standard single-mode fiber (SSMF) at 1310 nm. In [6], the authors demonstrated a real-time FPGA-based 5-GS/s sigma-delta modulator to digitize LTE signals with bandwidth up to 252 MHz and modulation scheme up to 1024-QAM at 960 MHz carrier frequency. These experiments confirm the competitive performance of SDoF approach for sub-6 GHz system in 5G New Radio (NR) [7].

However, moving to higher frequency bands above 24 GHz specified by the 3GPP [7], the required sampling rate of the SDM becomes impractically high. SDoF has not been reported for frequency bands beyond 24 GHz due to the limited sampling rate of the state-of-the-art SDMs as summarized in [4], [8], [9]. Therefore, when a simple RRU is required, prior works mainly rely on the ARoF, where the baseband or intermediate frequency (IF) signal is translated to the carrier frequency by either analog [10], [11] or optical up-conversion [12], [13]. However, the main drawbacks of these approaches are the sensitivity to nonlinearities in the electrical-to-optical (E/O) conversion [14] and the requirement of additional components for frequency up-conversion.

Our recent work presented in [8] decouples the parallelization degree and hence the effective sampling rate of SDMs from
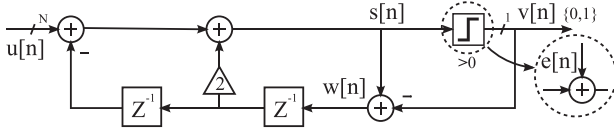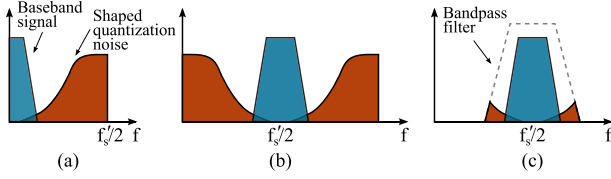
Fig. 1. Block diagram of a single-bit second-order low-pass SDM.

Fig. 2. Operation of sigma-delta modulation and all-digital transmission with $f_s = 2f_s' = 4f_c$. (a) Low-pass sigma-delta modulation processed at f_s'. (b) Digital up-conversion to carrier frequency f_c. (c) Bandpass filter removes the out-of-band quantization noise.

Fig. 3. (a) Block diagram of all-digital transmitter based on sigma-delta modulators with $f_s = 2f_s' = 4f_c$. (b) Digital up-conversion using a 2-to-1 multiplexer with output sampling rate f_s.

the critical path inside SDMs. It eliminates the sampling rate limitation of SDMs and shifts high-frequency operations to a single-bit multiplexer (MUX). In the meantime, [15] presented an 8-to-1 MUX (without equalization) beyond 100-Gb/s with 2-Vpp output swing in 130 nm SiGe BiCMOS technology. [16] demonstrated an integrated transmitter that can generate two parallel 100-Gb/s optical channels with simple non-return-to-zero (NRZ)/on-off keying (OOK) format over 500 m SMF. A 2-to-1 MUX supporting 103.125-Gbit/s OOK format has also been reported in [17]. The performance of these high-speed MUX's implies that the realization of a real-time SDoF transmission in the frequency band above 24 GHz is technically feasible.

In this paper, we combine the SDM parallelization technique for FPGAs with an in-house developed high-speed MUX [18], [19] in order to extend the SDM's sampling rate from 21 GS/s in [8] to 100 GS/s ($\approx 5 \times$ increase). As an upgrade of sub-6 GHz SDoF systems, we demonstrate a real-time 100-GS/s all-digital SDoF transmission at 1562 nm covering the 22.75–27.5 GHz band. This paper pushes the sampling rate of the digital SDMs a step further toward its limits and paves the road toward all-digital radio-over-fiber transmission for high-frequency bands.

This paper is an invited extension of our work presented at OFC 2019 [20]. In Section II, the system architecture and operation principle of the sigma-delta-modulated all-digital RoF transmitter for high-frequency bands are described. In Section III, the impact of clock duty-cycle distortion (DCD) and clock-data skew on the SDM performance is analyzed and compensation techniques are proposed. In Section IV, the measurement results are discussed. Finally, conclusions are drawn in Section V.

II. System Architecture and Key Components

A. 100-GS/s Sigma-Delta Modulator

Fig. 1 shows the block diagram of a single-bit second-order low-pass (LP) SDM based on the error feedback modulator (EFM) architecture. Fig. 2(a) shows the operation principle of this LP SDM. By oversampling the multi-level digital baseband (BB) signal with a closed feedback loop, the quantization noise
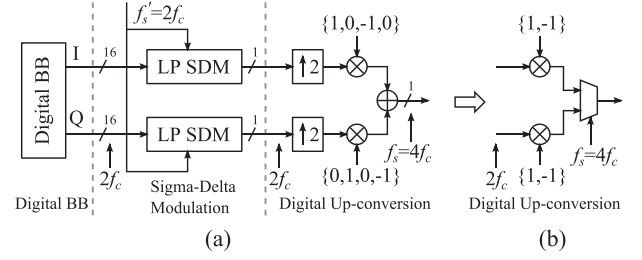
is pushed to high frequencies, away from the baseband signal, as shown in Fig. 2(a). The LP SDMs encode the 16-bit baseband I/Q signal into a single-bit sequence at the sampling rate f_s'.

Fig. 3(a) illustrates the system architecture of an SDM-based all-digital transmitter. After sigma-delta modulation, the digital baseband signal represented in one-bit format is digitally up-converted to the desired carrier frequency by a digital quadrature mixer as shown in Fig. 2(b) [21]. By choosing the carrier frequency f_c equal to a quarter of the output sampling rate f_s of the digital quadrature mixer or equal to a half of the LP SDM sampling rate f_s', the $\pi/2$ phase-shifted I and Q local oscillator (LO) signals can be respectively represented by the digital sequences $\{1, 0, -1, 0\}$ and $\{0, 1, 0, -1\}$. In this way, after summing up the I-channel and Q-channel, the output still remains one-bit format. This $\pi/2$ phase shift between I/Q LO signals is further realized by selecting I/Q samples in consecutive clock periods of f_s, as shown in Fig. 3(b). The adder can be replaced by a 2-to-1 multiplexer and the multiplications with -1 can be replaced by simple bit-wise negation. This greatly simplifies the up-conversion [21]. As shown in Fig. 2(c), a bandpass (BP) filter eliminates the out-of-band quantization noise and reconstructs the analog signal waveform.

However, it is very challenging to achieve the required sampling rate beyond 96 GS/s for the targeted high-frequency transmission above 24 GHz, since the SDM's feedback loop involves several high-precision additions in a single clock cycle. A feedback loop unrolling or parallelization technique for high-speed digital SDM is proposed in our previous work [8]. The multi-level digital baseband I/Q signal is first oversampled and converted to a two-bit stream by a multi-stage noise shaping MASH-1-1 LP SDM [22], [23]. This low-resolution bit stream is further converted to a single-bit stream by a bit-reduction process which predicts the finite-state-machine (FSM) behavior of a single-bit second-order digital LP SDM. This is possible because the low-resolution FSM has a limited number of possible states. This technique decouples the effective sampling rate from the critical path in the digital SDM and moves all high-frequency operations to a single MUX, therefore largely reducing the design difficulty and boosting the achievable sampling rate. As the digital signal is just converted into the analog domain by the final MUX, the MUX becomes the predominating factor in the system performance.

The system architecture and the experimental setup are illustrated in Fig. 4. A *Xilinx Virtex Ultrascale* FPGA VCU108
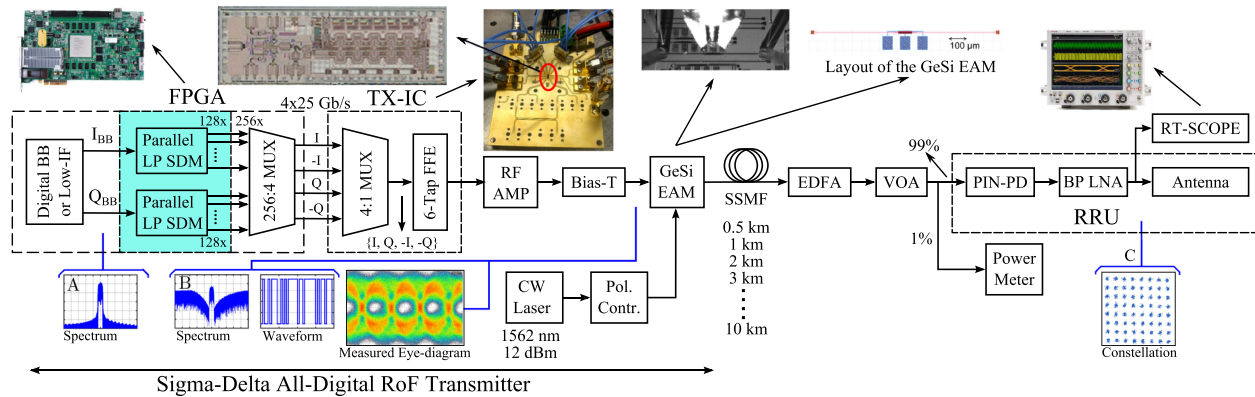
Fig. 4.   The system architecture and experimental setup for the real-time 100-GS/s sigma-delta radio-over-fiber transmission.
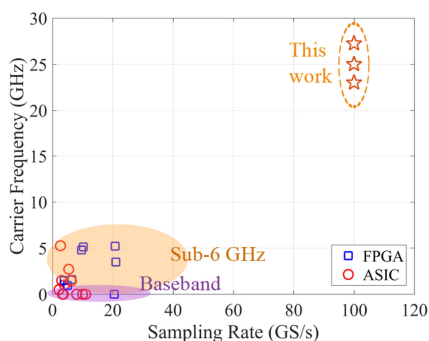

Fig. 5.   Summary of reported all-digital SDM-based transmitters. This work covers a wide carrier frequency range.

was adopted to generate the sigma-delta signals. On the FPGA operating at 390.625 MHz, a baseband or low-IF QAM-signal (390.625 MBd I_{BB} and Q_{BB} per channel with a roll-off factor of 0.28 for square-root-raised-cosine filter) is first oversampled and noise-shaped by LP second-order SDMs at an equivalent sampling rate of 50 GS/s for both I and Q channels using the parallelization techniques. Each parallel SDM has a parallelization degree of 128 and has a latency of approximately 691 ns. The low-IF signal is generated using a polyphase digital direct synthesis (DDS) and COordinate Rotation DIgital Computer (CORDIC) module. The 256 parallel streams are interleaved into 4 streams at 25 Gb/s to drive four FPGA high-speed serial interfaces. These interfaces generate I, -I, Q, -Q samples which are used for the subsequent up-conversion to 25 GHz.

An in-house developed transmitter IC (TX-IC) multiplexes these 4 × 25 Gb/s streams into a serial 100 Gb/s single-bit stream, accomplishing the digital up-conversion to a 25 GHz carrier. The second-order LP SDMs and the digital up-conversion result in an equivalent 100 GS/s fourth-order BP SDM with a 25 GHz carrier frequency without using analog/optical up-conversion. Fig. 5 shows a summary of reported all-digital SDM-based transmitters for BB or RF signals, implemented on ASIC or FPGA [4], [8], [9].

B. Electrical Transmitter

The utilized TX-IC, presented in [24] and [19], is fabricated in 55 nm SiGe BiCMOS technology and is comprised of a 4-to-1

MUX and a 6-tap feedforward equalizer (FFE). The PCB and die photo of the TX-IC are shown in Fig. 4. The MUX is capable of interleaving 4 parallel NRZ streams with rates up to 25 Gb/s into a single serial NRZ stream at 100 Gb/s. The die dimensions are 1.5 mm by 4.5 mm.

The FFE was tuned to compensate the bandwidth limitation of the interconnect toward the E/O converter. The TX-IC was initially designed to transmit over electrical backplanes, only requiring a low voltage swing. Therefore, to boost the TX-IC output single-ended signal of approximately 300 mVpp, two 67 GHz broadband RF-amplifiers amplify the signal from the TX-IC via an RF-probe to the bondpads of the E/O converter. It should be pointed out that, adding 1 or 2 amplification stages in the TX-IC is feasible in the used BiCMOS technology with a supply voltage of 2.5 V [25].

C. E/O Converter

A high-speed germanium-silicon (GeSi) based electroabsorption modulator (EAM) is used for the E/O conversion. This is a very compact GeSi EAM (80 μm, see inset Fig. 4) with >50 GHz bandwidth fabricated on a 200 mm silicon photonics platform without any traveling-wave electrodes and/or power-dissipating terminations, similar to the one in [19]. Light is coupled in and out of the waveguide structure through fiber-to-chip grating couplers with approximately 6 dB insertion loss per coupler. The grating couplers are used to facilitate optical probing and can easily be replaced with low-loss edge couplers (typically 1 dB/coupler) [26]. During the experiments, the modulator was reverse-biased at −0.75 V. The EAM modulates a continuous wave 1562 nm laser with 12 dBm output power. Owing to the digital up-conversion, neither analog nor optical up-conversion is necessary and the EAM is directly driven by NRZ/OOK signals, resulting in a simple transmitter structure. The transmitter is less vulnerable to nonlinear distortions, which is one of the main benefits of SDoF compared to ARoF [27].

D. Remote Radio Unit

An erbium-doped fiber amplifier (EDFA) and a variable optical attenuator (VOA) were used to control the signal power incident on a commercial 50 GHz III-V-based 50 Ω PIN-PD with 0.65 A/W responsivity at the RRU. This PIN-PD converts
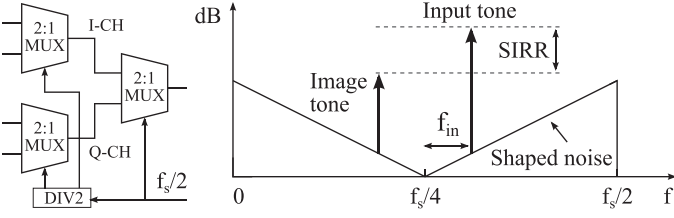
Fig. 6. Topology of the 4-to-1 MUX (left) and image signal due to the DCD effect on the final 2-to-1 MUX (right). f_{in} is the frequency of a sinusoidal tone in the baseband which will be further processed by the sigma-delta modulator and digital up-conversion.

Fig. 7. Mismatch errors caused by the DCD, illustrated with half-rate sampling clock of frequency $f_s/2$, $T_s = 1/f_s$ and duty-cycle error d_e.

Fig. 8. Simulated and estimated SIRR with or without DCD compensation, with sinusoidal tone frequency f_{in} at 270 MHz and $f_s = 100$ GHz.

the optical signal back into the electrical domain. A narrow-band receiver realized by a BP low noise amplifier (LNA) or a resonant TIA [28] is preferable as it helps remove the out-of-band quantization noise. In this work, a GaAs bandpass LNA HMC1040LP3CE was employed with 2.2 dB noise figure, 23 dB gain, and 22 dBm output IP3. The PD and LNA only need to receive the signal of interest around a 25 GHz carrier, it is not necessary to receive the complete 100 Gb/s NRZ/OOK signal. A Keysight real-time oscilloscope (DSAZ634A) and VSA soft-ware were used to demodulate QAM-signals and evaluate the performance.

III. IMPACT OF TIMING MISMATCH

As stated previously, the performance of the sigma-delta modulator is dominated by the MUX. The clock duty-cycle distortion (DCD) and the clock-data skew of the MUX largely influence the performance of the sigma-delta modulator.

Fig. 6 shows the tree topology of the employed 4-to-1 MUX which consists of a clock divider and three 2-to-1 MUX stages. The first stage MUXs operate on a clock frequency of $f_s/4$ and the last stage MUX uses an $f_s/2$ clock frequency. It is clear that this last stage will dominate the performance as its two input samples are multiplexed on the rising and falling edge of a 50 GHz clock and no master-slave D flip-flop at full-rate of 100 GHz for retiming is used at the MUX output.

A. Impact of Clock Duty-Cycle Distortion

Achieving an exact 50% clock duty-cycle at high speeds is very challenging. Due to the digital up-conversion, in addition to the quantization noise folding caused by the clock DCD [29], the single-sideband single-tone signal at $f = f_{in} + f_s/4$ is also mirrored with respect to the carrier frequency at $f_c = f_s/4$ to its image frequency $f_s/4 - f_{in}$, as illustrated in Fig. 6. Here, f_{in} is the frequency of a sinusoidal tone in the baseband which will be further processed by the sigma-delta modulator and digital up-conversion. The duty-cycle error d_e, i.e. a duty-cycle variation from 50%, causes an IQ gain mismatch and phase error shown in Fig. 7. By assuming a small duty-cycle error, the image signal is mainly caused by IQ gain mismatch at a frequency of $f = (f_{in} + f_s/4)$. Without loss of generality, d_e is assumed to be positive. This DCD impact is quantified by the signal-to-image
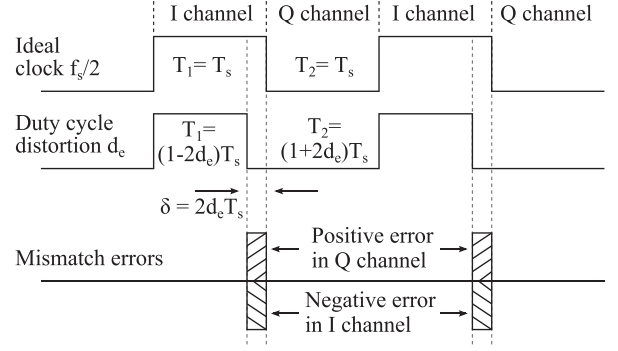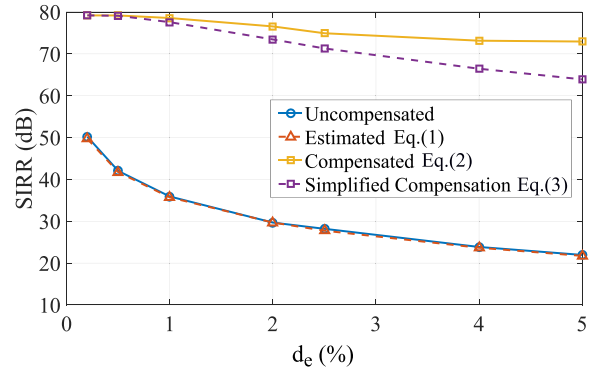
replica ratio (SIRR) [29], given by

$$\text{SIRR}_{\text{estimated}} = 20 \log \left(\frac{f_s}{2\pi d_e f} \right) \tag{1}$$

Fig. 8 shows that the SIRR for 270-MHz f_{in} frequency degrades fast with increasing d_e and the simulated SIRRs (denoted as 'Uncompensated') are in good agreement with the estimated values expressed in (1). During the simulation, an instant signal transition from 0 to 1 is assumed, and vice versa. For the DCD compensation in digital baseband, both the negative error in I channel and the positive error in Q channel, as indicated in Fig. 7, can be derived from (1). The negative error means that the average power in I channel is lower due to smaller duty-cycle. The DCD compensated baseband channels are given by

$$\text{I}_c = \text{I}_{\text{BB}} + \underbrace{\frac{2\pi d_e f}{f_s} \cdot \text{I}_{\text{BB}}}_{\text{I error term}} = \left(1 + \frac{2\pi d_e (f_{in} + f_s/4)}{f_s} \right) \cdot \text{I}_{\text{BB}}$$

$$\tag{2a}$$

$$\text{Q}_c = \text{Q}_{\text{BB}} - \underbrace{\frac{2\pi d_e f}{f_s} \cdot \text{Q}_{\text{BB}}}_{\text{Q error term}} = \left(1 - \frac{2\pi d_e (f_{in} + f_s/4)}{f_s} \right) \cdot \text{Q}_{\text{BB}}$$
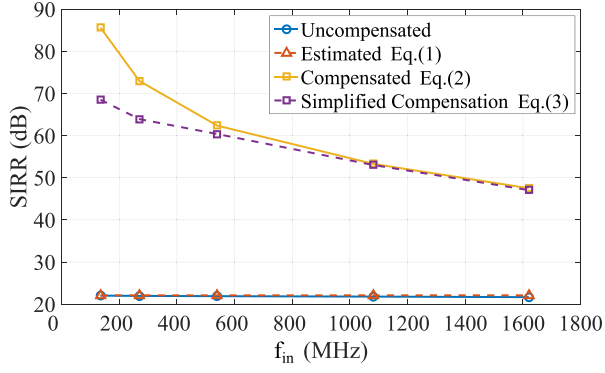
$$\tag{2b}$$

Fig. 9. Simulated and estimated impact of 5% DCD on SIRR as a function of baseband sinusoidal tone frequency.

where I_{BB} and Q_{BB} are first assumed to be single-tone signals with frequency f_{in} and $\pi/2$ out-of-phase. Since f_{in} is much smaller than the carrier frequency $f_s/4$, the baseband compensation can be simplified as follows:

$$I_{c,s} = \left(1 + \frac{2\pi d_e(f_s/4)}{f_s}\right)\cdot I_{BB} = \left(1 + \frac{\pi d_e}{2}\right)\cdot I_{BB} \quad (3a)$$

$$Q_{c,s} = \left(1 - \frac{2\pi d_e(f_s/4)}{f_s}\right)\cdot Q_{BB} = \left(1 - \frac{\pi d_e}{2}\right)\cdot Q_{BB} \quad (3b)$$

As (3) no longer contains frequency-dependent variables, therefore, this simplified compensation technique can be used for wideband signals.

As depicted in Fig. 8, after DCD compensation using (2) the SIRR experiences a negligibly slow degradation with increasing d_e and 70 dB SIRR is always guaranteed for d_e up to 5%. The SIRR with simplified compensation (3) degrades slightly more for larger d_e values. In Fig. 9, the DCD d_e is fixed at 5% and the frequency of the baseband sinusoidal tones is swept. Some degradation in both DCD compensation and its simplified version has been observed for increasing f_{in}.

B. Impact of Clock-Data Skew

The path through the clock divider and the 50-GS/s 2-to-1 MUXs to the data input of the final 100-GS/s 2-to-1 MUX introduces a significant delay. It is very challenging to match this delay with the path delay of 50-GHz clock to the final MUX. As there is no flip-flop and the final 2-to-1 MUX is the final stage of the digital circuit, the MUX requires a quite accurate skew alignment of data and clock.

The timing diagram of the clock-data skew is illustrated in Fig. 10. For the sake of simplicity, we assume only the I channel undergoes clock-data skew $t_d = \tau T_s$, which means the I channel data transition occurs after the rising clock edge by t_d. A similar SIRR estimation can be derived from (1):

$$SIRR_{estimated,\tau} = 20\log\left(\frac{f_s}{2\pi\tau f}\right) + 10\log(2) \quad (4)$$

where the second term of 3 dB is due to the fact that in contrary to the clock DCD case, here only I channel introduces mismatch error, which halves the average power of mismatch error over time.
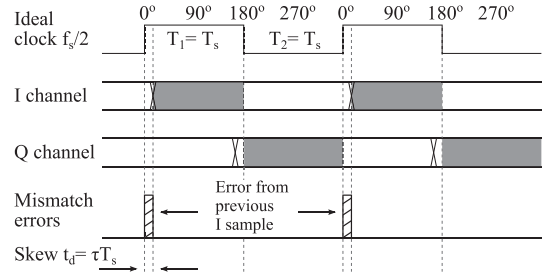

Fig. 10. Mismatch errors caused by the clock-data skew, illustrated with half-rate sampling clock of frequency $f_s/2$, $T_s = 1/f_s$ and skew $t_d = \tau T_s$.
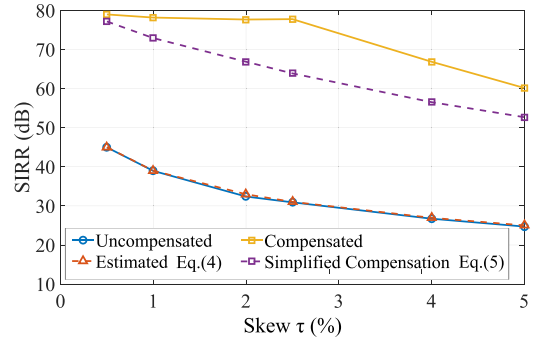

Fig. 11. Simulated and estimated SIRR with or without skew compensation, with sinusoidal tone frequency f_{in} at 270 MHz and $f_s = 100$ GHz.

The mismatch error from a previous I sample can be considered as an error component appended to the end of Q samples and this error component is proportional to the I samples. Besides, there is a gain error in the current I sample due to the skew effect. Therefore, the skew compensation takes these two main mismatches into account and the simplified compensation can be derived in a similar way, being:

$$I'_{c,s} = \frac{1}{1 - (\pi\tau)/2}\cdot I_{BB} \quad (5a)$$

$$Q'_{c,s} = Q_{BB} - \frac{\pi\tau}{2}\cdot I_{BB} \quad (5b)$$

Fig. 11 shows that the simulated SIRR under clock-data skew is consistent with the estimated SIRR. It is also evident that the skew compensation technique can guarantee a more than 60 dB SIRR up to 5% skew when taking $f = (f_{in} + f_s/4)$ as frequency component. The simplified compensation technique makes an approximation of $f = f_s/4$, which presents also a quite good performance against the skew mismatch. Fig. 12(a) shows the simulated constellation diagrams under the impact of 5% skew and Fig. 12(b) illustrates that the IQ-mismatch can be compensated with the simplified compensation technique expressed in (5).

IV. RESULTS AND DISCUSSION

A. Chromatic Distortion in the Fiber Channel

Not only the electrical transceiver chipset and the optical modulator are important parts of a 100-Gb/s link, but the fiber
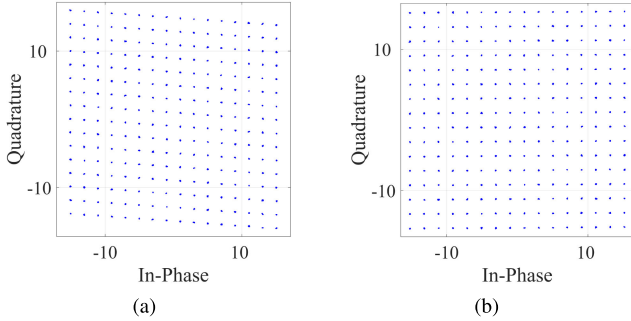
Fig. 12. Simulated constellation diagrams of 390.625 MBd 256-QAM under $\tau = 5\%$ clock-data skew, (a) without and (b) with simplified compensation.
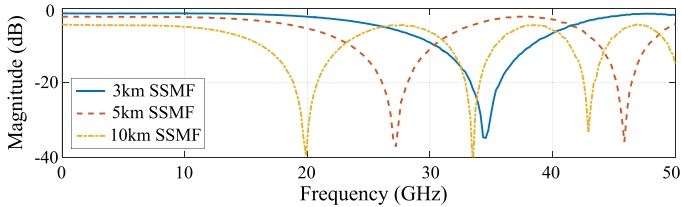

Fig. 13. The measured small-signal frequency response of the optical link, comprising a GeSi EAM and a 50 GHz commercial PIN-PD.
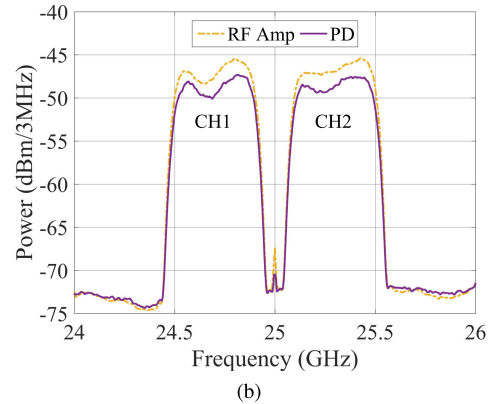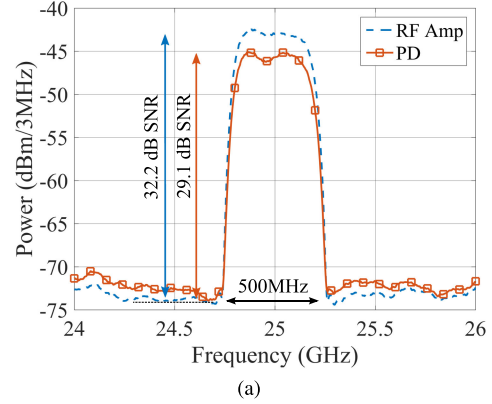

Fig. 14. The measured in-band spectra at RF amplifier output and PIN-PD output (optical B2B) in the (a) single-channel case and (b) two-channel case.

Fig. 15. (a) The measured rms EVM as a function of the optical power received by the PD in the single-channel case (optical B2B). (b) The demodulated constellation.

channel plays a critical role in the C-band, where the relatively large chromatic dispersion coefficient manifests itself as notches in the frequency response when using direct detection [30]. The RF power fading is dependent on the fiber dispersion parameter, the transmission distance, and the signal frequency. The measured small-signal frequency response of a link consisting of the EAM and the PIN-PD is given in Fig. 13 for different fiber spans (3 km, 5 km and 10 km) at 1562 nm. At 1562 nm, 5 km of SSMF introduces a notch around 27 GHz, which degrades the frequency responses.

B. Spectrum

The measured spectra at the RF amplifier output in electrical back-to-back (B2B) and at the 50 GHz PIN-PD output (optical B2B) are shown in Fig. 14(a) where signal-to-noise ratios (SNRs) of 32.2 dB and 29.1 dB are indicated as a performance reference. The wide frequency range of the low quantization noise from 24 GHz to 26 GHz, benefiting from the high sampling rate, allows us to transmit two channels (CH1 at 24.7 GHz and CH2 at 25.3 GHz) simultaneously. Besides, this wide clean spectrum where the noise floor remains low and flat is very beneficial in a real application as less band-specific filters are required and the filter order can be relaxed. Unless stated otherwise, the following measurements are referred to the single-channel case at 25 GHz.

C. Link Performance

The signal quality was investigated as a function of the optical input power on the PIN-PD in Fig. 15(a). The signal quality improves with higher optical input powers and the root-mean-square (rms) value of the error vector magnitude (EVM), normalized to the average power, drops below 4%, satisfying the 3GPP requirement for 64-QAM: EVM $< 8\%$ [31]. This measured EVM even enables adequate signal quality for 64-QAM with 1E-06 bit error rates (BERs) without error coding. The constellation at 8 dBm optical received power is presented in Fig. 15(b). This low EVM can even enable the reception of 390.625 MBd 256-QAM in optical B2B, as shown in Fig. 16, providing a net bit rate of 3.125 Gb/s. Fig. 16 illustrates that the

Fig. 16.   Constellation diagrams of 390.625 MBd 256-QAM in optical B2B (a) without and (b) with I/Q-mismatch compensation.

Fig. 17.   (a) Measured rms EVM vs fiber spans. (b) Demodulated constellation.

Fig. 18.   The measured rms EVM vs carrier frequency in electrical B2B.
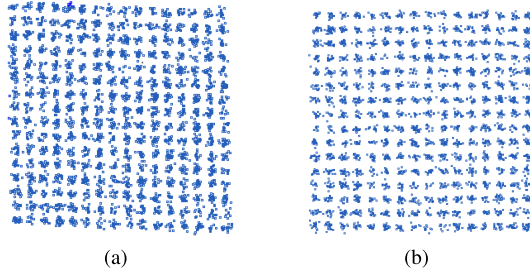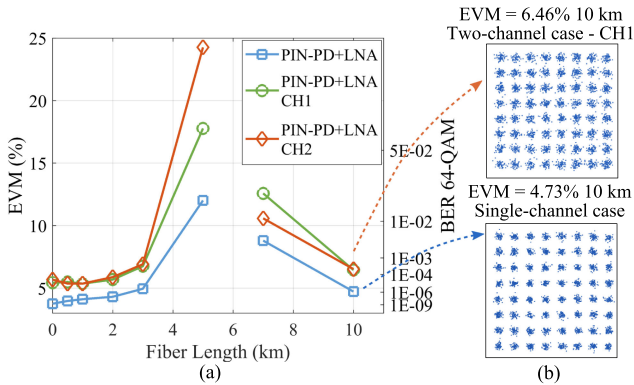
TABLE I
RESOURCE UTILIZATION OF FPGA VCU108 FOR 100-GS/s SDM

Resource	Utilization	Available	Percentage (%)
LUT	55905	537600	10.4
LUTRAM	29404	76800	38.29
FF	51378	1075200	4.78

I/Q mismatch can be compensated in the transmitter's digital baseband. During the experiment, the impact of clock-data skew is more obvious than that of clock duty-cycle distortion.

To explore the reach of this SDoF transmission, the EVMs were compared among different fiber spans at 8 dBm optical received power in Fig. 17(a). The measured EVMs are 3.09% and 3.76% for electrical B2B and optical B2B in single-channel measurements, respectively. The EVMs slightly increases to 4.2% and 5.43% in the two-channel measurements, respectively. No noticeable degradation in EVM has been observed for fiber spans below 3 km. The high EVMs (>25%) at 6 km fiber are caused by the notch around 25 GHz due to chromatic dispersion of the SSMF for 1562 nm, which is in good agreement with the S-parameter measurements in Fig. 13. The peak EVMs between CH1 and CH2 are slightly shifted owing to different carrier frequencies. For 10 km distance, the notch is shifted away from the carrier frequency, leading again to a good EVM. This EVM degradation caused by the chromatic dispersion notch can be alleviated by adding a dispersion compensation module [32]. Only a small degradation in EVM is observed from optical B2B to 10 km fiber. These EVM values are consistent with the measured SNR in Fig. 14. The demodulated constellations of the 64-QAM signals are compared in Fig. 17(b). The total information bit rate of the 64-QAM signal is approximately 2.34 Gb/s in the single-channel case and doubled in the two-channel case.

Moreover, by digitally shifting the IF frequency with DDS module, this all-digital transmitter covers a wide frequency band from 22.75 GHz to 27.5 GHz (with 500 MHz bandwidth around
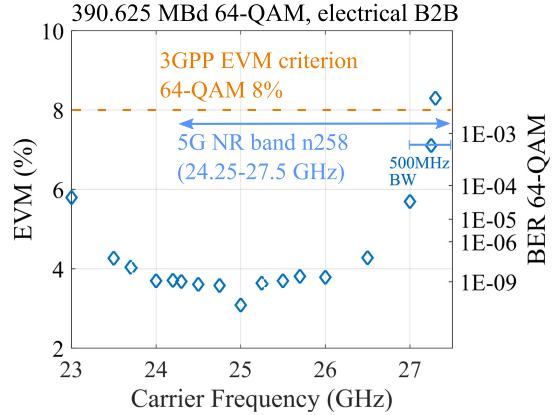
carrier frequencies 23-27.25 GHz) with relatively low EVMs as depicted in Fig. 18. It also shows the superior EVMs in the single-channel case (electrical B2B) e.g. EVM of 3.58% compared to 4.2% in the two-channel case at 24.7 GHz carrier where the input dynamic range of SDM is shared between two channels. When the carrier frequency deviating from 25 GHz, EVM degradation are caused by the shaped quantization noise. This frequency range covers the 5G NR band n258 specified in 3GPP [7] and these measured EVMs satisfy the 3GPP requirement for 64-QAM: EVM < 8% [31].

D. Resource Utilization and Power Consumption

The summary of the resource utilization of *Xilinx Virtex Ultrascale* FPGA VCU108 for 100-GS/s SDM (not including digital BB) is listed in Table I. As this sigma-delta implementation is compatible with CMOS technology, therefore, the clock frequency can be increased and hence the degree of parallelization and resource consumption will be decreased when migrating from FPGA to ASIC. Accordingly, the latency of SDM can be dramatically lowered. The TX-IC consumes 0.85 W where the FFE and output buffer account for 65% of the total power consumption. The total power consumption of this SDoF link is low by avoiding components such as high-speed digital-to-analog converters and frequency up-converters, and can be further reduced by packaging the MUX and EAM together and avoiding the RF interconnect losses between the MUX and EAM in the present demonstration, which makes it possible to reduce the equalization and gain requirements between MUX and EAM. A dedicated low-power EAM NRZ-driver proposed in [25] can also be used.

V. CONCLUSION

We have demonstrated the first real-time sigma-delta all-digital radio-over-fiber transmitter in the 22.75–27.5 GHz band without the aid of analog/optical up-conversion or carrier frequency doubling enabled by a low-latency 100-GS/s sigma-delta modulator. The current demonstrator consists of different individual building blocks: sigma-delta modulators on FPGA, a 100-Gbps MUX and an EAM. However, these function blocks can be integrated into a single module fitting standard pluggable form factors such as QSFP28-compatible. This would make it an easy and low-cost solution to provide direct radio access from a data center rack. The simple structure of the transmitter and RRU, digital reconfigurability of carrier frequency, and the prominent performance (4.68 Gb/s 64-QAM at low EVMs over 10-km fiber at 1562 nm) corroborate the strong competitiveness of the SDoF approach in high-frequency band radio-over-fiber for 5G communication.

Furthermore, by avoiding any processing at the RRU, the associated power consumption is removed. The SDoF approach pushes the digital signal processing as far as possible into the transmit chain. By removing all analog signal processing, a very flexible network is offered, making it compatible with any existing standard such as 4G-LTE, Wi-Fi, 5G New Radio etc. This all-digital SDoF transmission also opens up the possibility for more advanced wireless concepts. Different streams can be generated in a centralized manner. As such their timing is tightly controlled and they are frequency-synchronous because every sigma-delta modulated serial stream shares the same clock source. This fact can be used to minimize inter-cell interference, perform digital beam forming or even enable distributed MIMO.

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