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Correlation between pattern density and linewidth variation in silicon photonics waveguides

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Abstract: We describe the correlation between the measured width of silicon waveguides fabricated with 193 nm lithography and the local pattern density of the mask layout. In the fabrication process, pattern density can affect the composition of the plasma in a dry etching process or the abrasion rate in a planarization step. Using an optical test circuit to extract waveguide width and thickness, we sampled 5841 sites over a fabricated wafer. Using this detailed sampling, we could establish the correlation between the linewidth and average pattern density around the test circuit, as a function of the radius of influence. We find that the intra-die systematic width variation correlates most with the pattern density within a radius of 200 μm, with a correlation coefficient of 0.57. No correlation between pattern density and the intra-die systematic thickness variation is observed. These findings can be used to predict photonic circuit yield or to optimize the circuit layout to minimize the effect of local pattern density.

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1. Introduction

Silicon Photonics is promising for low-cost large-volume production of photonic circuits because of its compatibility with existing CMOS manufacturing technology. Also, it enables large-scale integration by its high contrast in refractive index (between silicon and silicon dioxide), which allows strong light confinement, and thus small footprint. However, the high material contrast and small feature size also make silicon photonic circuits very sensitive to nanometer-scale variations in component geometries, which can be induced by process variations. These variations affect optical properties of a device such as the effective index and group index of the guided waveguide mode, the coupling coefficient of a directional coupler and the peak wavelength of interferometric filter circuits. When connecting devices in a circuit, the variations at device-level propagate and accumulate at the circuit level. For instance, waveguide width variation affects the effective index of the waveguide, which in turn changes the optical delay in a filter delay line, which then shifts the filter response. If many of these random components and imbalances are introduced in the circuit, the circuit performance will deteriorate, making only a fraction of the fabricated circuits perform as intended [1].

A good measure for the variation within a silicon photonic circuit is the linewidth and thickness of the optical waveguide. Direct accurate measurements of these parameters are not easy, and often destructive, but practical methods have been developed using wafer-scale optical transmission measurements of compact interferometric circuits [2,3]. We have improved the design process of this extraction circuit in [3], and proposed a compact two-stage *Mach-Zehnder interferometer* circuit that can monitoring multiple waveguide and directional coupler parameters [4]. We put 117 copies of the design, shown in Fig. 1, on a mask, which is then replicated 52

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times over a wafer, resulting in 6,084 locations, of which 5,841 generated valid measurements from which we could extract waveguide width and thickness. From this measurement data, we generated a granular wafer map of the waveguide width for analysis. The wafer map contains rich input of variations from different origins. To analyze the statistics of process variations, we separated the contributions in the form of a hierarchical variability model [5,6]. This resulted in systematic and random wafer-level variation, and systematic and random die-level variation.

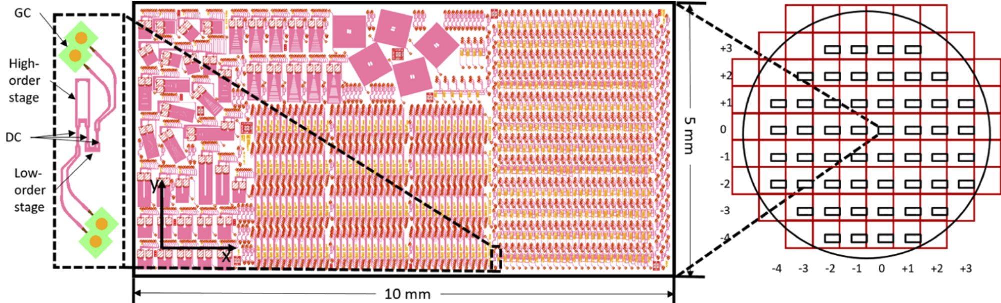

Fig. 1. Left: The layout of the 10 mm × 5 mm die that includes 117 monitoring circuits. Right: Location of 52 dies on the wafer. Inset: Layout of the two-stage monitoring circuits.

The *intra-die systematic* (IDS) variation refers to the systematic variations that are repeated on every die, which originates from fabrication steps repeated at the die level. With stepper/scanner based lithography, possible origins can be errors in the photomask such as pattern stitching errors, writing errors, or particles on the mask that we cannot do much about. Likewise, systematic variations can be introduced by aberrations in the lithography projection optics. In this paper, we look at IDS variation that can be induced by the designed layout patterns on the mask. In particular, the local pattern density can have an effect. For example, plasma etching typically used for waveguide or grating definition is influenced by the pattern density *PD*. The chemistry of the plasma above the chip, and therefore the etch rate, selectivity and anisotropy depend on the fraction of photoresist and the fraction of etching waste products generated during the etch process. This can result in a variation in etch depth, but also a variation in linewidth, as local over-etching can cause a significant attack on the sidewalls [7].

Another process that can be affected by pattern density is *Chemical Mechanical Polishing* (CMP). In a damascene process, the planarization depends on the presence and density of the material to be polished and the material that resists the CMP (stopping layer). Large areas without patterns can give rise to erosion and dishing, resulting in a different remaining thickness [8–10].

Confirming the correlation between IDS width variation and pattern density, and understanding how they are related, is critical for photonic circuit designs: some photonic designs necessarily have large areas without patterns (e.g. the free-propagation regions in AWGs or echelle gratings). These will affect the local pattern density and therefore the neighbouring circuits. Knowing how far this effect propagates over the chip is important for the placement of critical designs. In this paper, we will present the IDS width variation we measured and identify the correlation between the variation and the pattern density.

2. Intra-die systematic width variation on a 200 mm wafer

IDS variation makes a significant contribution to the process variation [11]. At die level, it is the main contributor to variation in waveguide width. To characterize the linewidth variations, we used a compact two-stage *Mach-Zehnder interferometer* (MZI) circuit as depicted in the inset of Fig. 1 that allows us to accurately extract the local effective index n_{eff} and group index n_g [4]. We can map the variations of n_{eff} and n_g onto variations of waveguide width and thickness.

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This design was replicated 117 times on a die of 5 × 10 mm as part of a multi-project wafer (MPW) fabrication run on IMEC's passive silicon photonics platform. The left part of Fig. 1 shows the layout of the die, while the right part of the figure shows the die locations on the wafer. Because there are multiple other designs on the MPW, our test sites cover only a ∼10% fraction of the die area and we do not have a uniform coverage over the wafer.

The fabrication process is schematically depicted in Fig. 2. The waveguide patterns are defined using 193 nm lithography and transferred into the 220 nm silicon layer using a plasma etching and a thin SiN hard mask. Two more similar sequences are used to define patterns that are etched 70 nm and 150 nm deep, respectively. Then the etched trenches are filled with silicon dioxide and planarized with a chemical-mechanical polishing (CMP) step. Finally, another 2000 nm of silicon dioxide cladding is deposited [12].

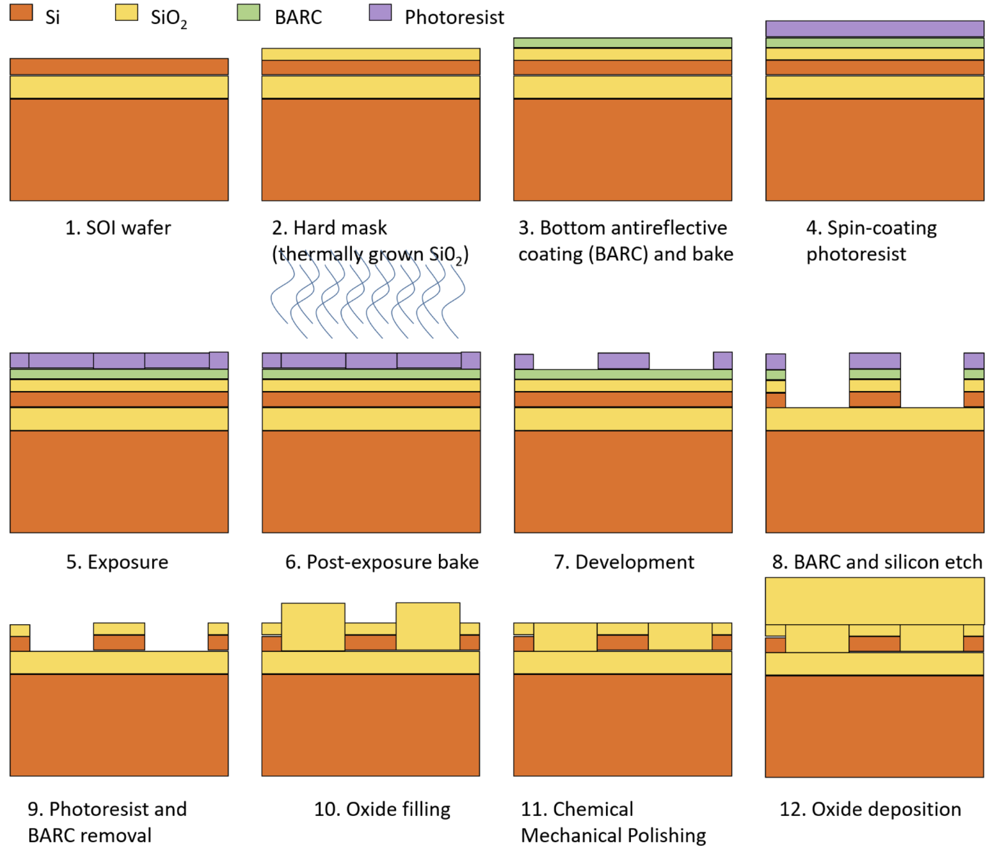

Fig. 2. Fabrication process for the waveguide layer.

Because the qualitative effect of pattern density on process conditions is already well known from electronics, the waveguide patterns are made as uniform as possible by adding dummy tiling in between the waveguide structures.

We characterized 5,841 of the 6,084 locations (Fig. 1) on the wafer by optical transmission measurements. Light is coupled into the grating couplers with fibre, and collected on the other end with another fibre, using an automated positioning system. We then measured the transmission as a function of wavelength using a calibrated tunable laser with 1 pm resolution.

The colour points in Fig. 3 present the IDS contribution to the waveguide width variation, separated from the full wafer map of the 200 mm wafer. The grey background represents the

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layout on the waveguide layer, including the tiling: the grayscale indicates the local pattern density from white (large unetched areas) to black (large fully-etched areas).

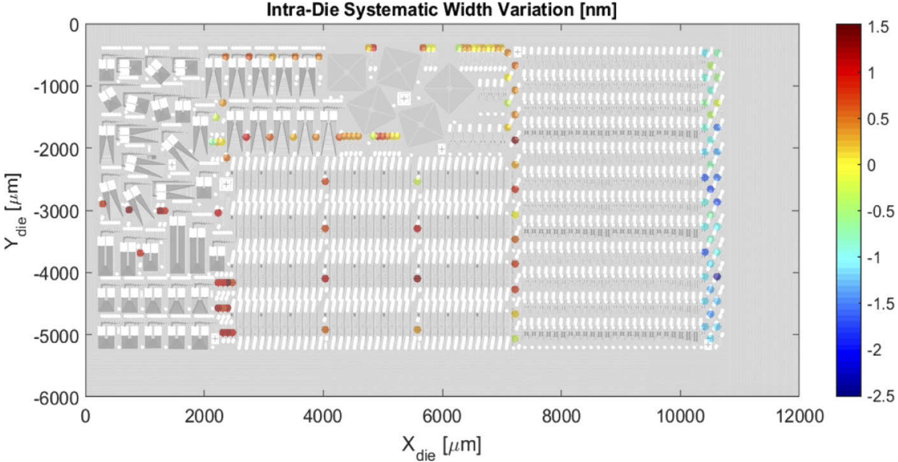

Fig. 3. Scatter plot of the intra-die systematic width variation. The plot is overlay with the layout in gray scale. The color of the marker indicates the value of the IDS width variation.

The maximum IDS width deviation we observe is 1.52 nm, and the minimum is -2.52 nm. The average of the IDS variation is zero by definition. The repeated variation on die-level covers a range of 4.04 nm. We observe that the IDS width variations on the 117 sites are very locally correlated. The IDS width is significantly larger near the array waveguide gratings and spirals, where the pattern density is large (i.e. where a lot of trenches are etched).

The variation tends to be negative near the east boundary that is also the border of the die where the pattern density is low. On the east border, the dense packing of grating couplers from 46 monitoring circuits also reduces the pattern density on the waveguide layer (grating couplers are printed in a separate step with 70 nm etch depth). Visually, we can see a correlation between pattern density and IDS width variation. To validate this observation, we will quantitatively correlate pattern density for the layout on the waveguide layer with our waveguide width and thickness measurements.

3. Generate pattern density from The Layout Mask

3.1. Choice of the Window to calculate pattern density

With pattern density, we define the fraction of trench that is being etched in a window over the windowed area on-chip. In a passive photonic chip, we can approximately think that the pattern is defined on the waveguide layer. The pattern density *PD* on a passive photonics chip is:

$$PD = \frac{A_{trenches}}{A_{window}} \tag{1}$$

where A_{trenches} is the area of the trench on the waveguide layer in the window, and A_{window} is the area of the window we observe. The value of *PD* is dependent on how we choose the window area. It depends on the size and shape of the window. When using a large window, the value of *PD* at each location is averaged over a large area, which would exhibit a low-frequency profile. On the contrary, when using a small window, *PD* is more determined by the adjacent patterns in a very local area. *PD* is also determined by the shape of the window. When semiconductor fabs try to determine if the pattern is too dense locally in the *design rule checking* (DRC) procedure, they often use a rectangle window to calculate the pattern density [13,14]. This procedure, which is

used to improve the *design for manufacturability* (DFM) by reducing pattern sensitive variations, is quite fast for rectangular windows.

However, from the point of view of physics, a rectangular window does not make sense. We want to find out how the pattern or the density of pattern affects the fabricated width, and therefore it is reasonable to use a circular window that imitates the plasma diffusion during the etch process. This relies mainly on the distance from the point of interest. To be more precise, a pattern close to the point of interest should have a stronger impact, and the impact should reduce gradually with the distance. So we assume that the impact of the pattern on *PD* can be filtered by a 2-dimensional Gaussian filter so that the impact decreases gradually over distance:

$$G(x, y) = \frac{1}{2\pi\sigma^2} e^{-\frac{x^2+y^2}{2\sigma^2}} \tag{2}$$

where x is the distance from the origin along the West-East axis on the wafer, y is the distance from the origin on the South-North axis, and σ is the standard deviation of the Gaussian distribution. The Gaussian filter works as a round window with entrance weight decreasing as the pattern moves away from the window centre. σ is an indicator of the weighted window size and presents the radial length of the round window in which pattern that has a strong impact on points of interest.

3.2. Calculate pattern density from mask layout

We generated a pattern map (background in Fig. 3) using a Gaussian filter from a high-resolution bitmap of the die layout. The greyscale bitmap file is converted from the layout GDSII file using the open-source python *gdsCAD* module. The resolution is guaranteed by a fine sampling of ~9.2 nm, which is enough to distinguish the pattern on the waveguide layer and the tiling. The fine pattern map ensures an accurate calculation of *PD*. After that, we processed the bitmap image using the Gaussian filter with various σ. Figure 4 presents *PD* maps under four window

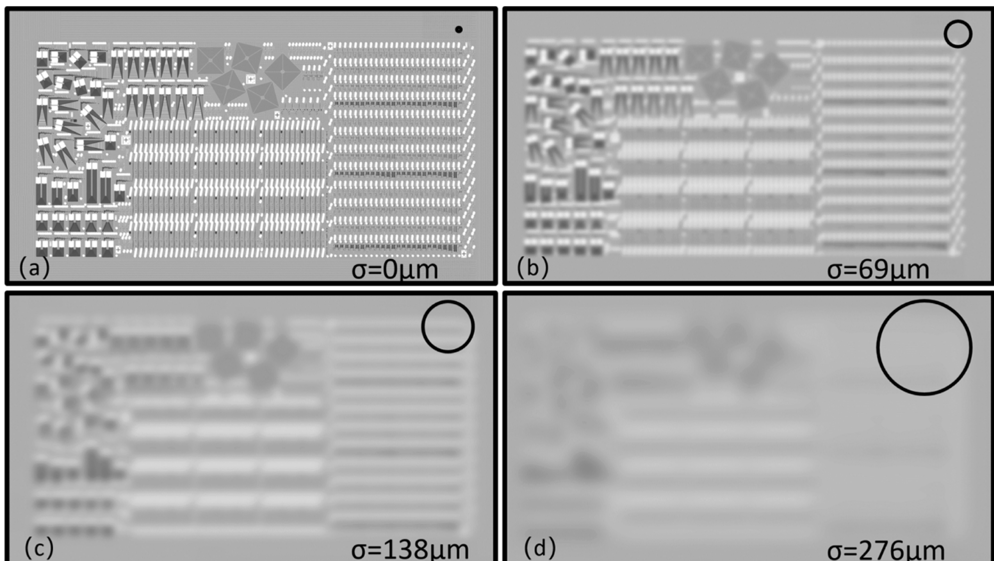

Fig. 4. We filtered the pattern image with a 2-D Gaussian filter with different sigma. (a) to (d) are examples of PD calculated using σ = 0, 69, 138, 276 μm, which correspond to 0, 7500, 15000 and 30000 pixels on the bitmap. The blue circle is the window with a radius of 3σ, which indicates the assumed region that *PD* has an influence on the IDS width variation.

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size σ . As window size σ increases, the image is blurred and *PD* is influenced by the pattern over a larger area.

4. Correlation between IDS width variation and pattern density

4.1. Window size and correlation strength

The value of σ which represents the window size is still to be determined. If the window size is overestimated, the impact of the distant pattern will be exaggerated, and we might space our designs too far apart. If the window size is underestimated, we will underestimate the impact from a distance, and we might place our critical circuits too close to a disturbing region. So, the value of *PD* calculated with the chosen window should be the one that is most correlated to the IDS width variation. The window with proper size should tell that within which range the pattern affects the IDS variation. So, we will sweep the value of σ and calculate the corresponding *PD*. The best correlation indicates the correct choice of σ.

We calculated the correlation between *PD* and IDS width and thickness variation at the locations of 117 monitoring circuits on the die. For example, Fig. 5(a) exhibits an example of *PD* and IDS width variation of the pattern in the block when $\sigma = 69\mu$m. The color contour shows the *PD* filtered from the pattern map. We swept σ from 0 to 920 μm. Figure 6(a) present the correlation at each σ. We observed that the correlation quickly increases with σ from $\sigma = 0$. When $\sigma = 69\mu$m, the correlation reaches the maximum. As the σ is further increased, *PD* and IDS width variation become less correlated.

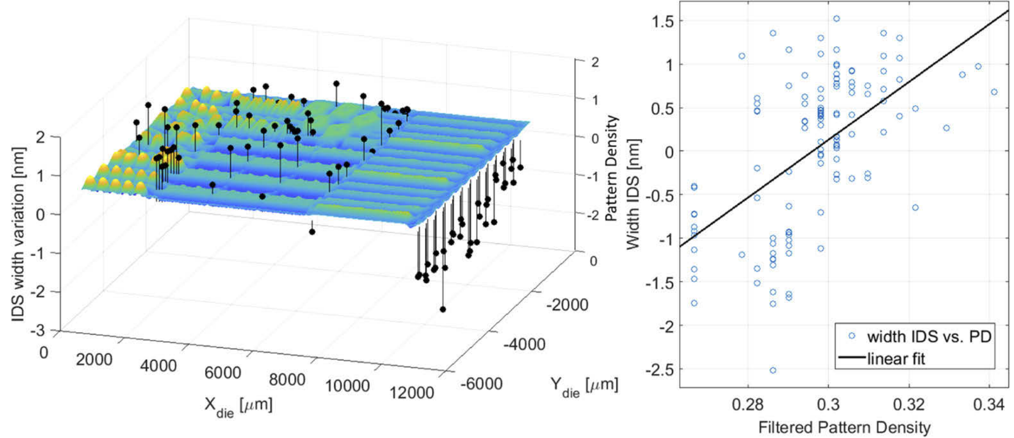

Fig. 5. (a) Contour plot of filtered *PD* vs. IDS waveguide width variation. 3-D contour presents the PD image processed by the Gaussian filter with radius of 69 μm. The stem plot with black head shows the IDS width variation. (b) Corresponding *PD* vs. IDS width variation (correlation=0.57). Blue solid dots are IDS width variation and corresponding *PD* on 117 locations on the die. The solid line is the linear fitting of the data.

Likewise, we performed the same analysis for waveguide thickness. Figure 5(b) presents the correlation at each σ. We swept σ from 0 to 2750 μm and the correlation coefficient is always below 0.25. Here we see that there is very little correlation. We can explain this because the silicon layer is fully etched in all cases, and the top of the waveguide is protected by a hard mask. Apparently, the pattern density is sufficiently uniform to have little impact from CMP variations, because the top of the waveguide is protected by a hard mask during CMP.

When $\sigma = 69\mu$m, the scatter plot in Fig. 5(b) shows PD at each of the 117 samples and the corresponding IDS width variation. The correlation is at its maximum, indicating $\sigma = 69\mu m$

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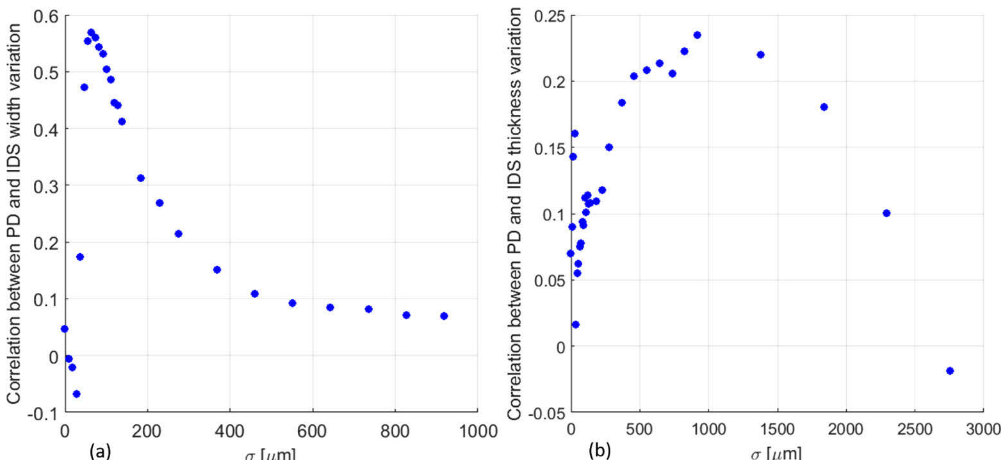

Fig. 6. Correlation between *PD* calculated using the Gaussian filter and (a) IDS width variation (b) IDS thickness variation.

is the optimal window size. The correlation coefficient of 0.57 means a moderate positive correlation between PD and the IDS width variation. There is still IDS width variation that cannot be explained by *PD*. It could be related to the extraction uncertainty due to limited extraction accuracy in linewidth. It could also be other origins that are not PD related such as mask errors and so on.

Equation 2 shows that the pattern within the 2-D round window with a 3σ radius has an overall weighting of 99.67% impact on calculated value of *PD*. The patterns outside the 3σ radius circle have little impact on *PD*. Therefore, layout outside the 3σ radius circle has little contribution to the *PD*-correlated width variation. For the wafer we measured, IDS width variation is immune to any pattern outside the $3\sigma \approx 200\mu$m circle.

It has an interesting implication that if we put a circuit $200\mu m$ away from a pattern, either the pattern is dense or loose, the influence it has on the circuit would be negligible. So when we evaluate *PD* in the DRC procedure, one quick way to avoid performance variation induced by *PD* variations could be to simply check if there is a densely patterned layout within the ~200 μm neighbourhood. We can just force the design to be ~200 μm away from dense patterns. Another implication could be active mitigation of the pattern density. If a fab could calculate *PD* before tiling using the Gaussian filter with the optimal window size, it can smooth the *PD* profile by optimizing tiles on the waveguide layer according to the actual pattern density at each location on the chip.

5. Conclusion

In this paper, we found a moderate correlation between pattern density and the intra-die systematic width variation. Our analysis showed that the intra-die systematic width variation is affected by the pattern within a distance of ~200 μm to the site. Our observation also showed that the intra-die systematic thickness variation has a negligible correlation with patterns on the chip. This finding helps to create design rules to alleviate the impact of the pattern density related non-uniformity.

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Disclosures

The authors declare no conflicts of interest.

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