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Influence of the spatial distribution of border traps in the capacitance frequency dispersion of Al_2O_3/InGaAs

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Abstract

In this paper, the capacitance frequency dispersion in strong accumulation of capacitance voltage curves has been studied for different high-k dielectric layers in MOS stacks. By studying experimental data at low (77K) and room temperature (300K), in oxides with different density of defects, it was possible reflect the spatial distribution of the defects in the capacitance frequency dispersion.The experimental data show that while at room temperature, the capacitance dispersion is dominated by the exchange of carriers from the semiconductor into oxide traps far away from the interface, at low temperature the oxide traps near the Al_2O_3/InGaAs interface are responsible for the frequency dispersion. The results indicate that the capacitance dispersion in strong accumulation reflect the spatial distribution of traps within the oxide, and that dielectric/semiconductor conduction band offset is a critical parameter for determining the capacitance dispersion for Al_2O_3/InGaAs based gate stacks.

I. INTRODUCTION

InGaAs is an attractive candidate to be used as channel material for the extension of CMOS (Complementary Metal-Oxide-Semiconductor) technology beyond Si due to its high electron mobility [1], [2]. However, one of the most important issues is the understanding of the large frequency dispersion that is observed in the experimental capacitance-voltage (C-V) characteristics in accumulation [3]–[6]. Particularly on InGaAs substrates, dispersion has been reported for a variety of dielectrics including Al_2O_3[7], [8], HfO_2[9], ZrO_2[10] and HfAlO[11].

Such dispersion cannot be explained by the conventional interface states whose time constant in accumulation is far too short for the range of frequencies (1 kHz–1 MHz) used in typical AC capacitance measurements[12], [13]. Since trap states inside the gate insulator, called border traps (BTs) or bulk traps, have long time constants as they interact with the conduction band electrons via

tunneling[14], some authors have proposed that these bulk traps are responsible for the frequency dispersion. In particular, the BT model developed by Yuan et al., [15], which assumes tunnelingbetween the border traps and the majority carrier semiconductor band, usually provides an excellent fit to experimental results (frequency dependent capacitance and conductance in accumulation) and allows the extraction of the border traps density[16], [17].

In this framework, the role of the substrate, high-k dielectric layer and fabrication process in the frequency dependent capacitance in accumulation are currently under intensive investigation. In this regard,Krylov et al [18]recentlyshowed that larger dispersion is obtained in HfO_2 based capacitors compared to Al_2O_3 based capacitors, deposited on the same semiconductor (InGaAs or InP), suggesting that this phenomenon is attributed to alower conduction band offset rather than to a higher border trap density. However, Vais et al [19] reported that the same dielectric (Al_2O_3) deposited on different substrates, InGaAs and InP, with very similar conduction band offsets at the dielectric/semiconductors interface, show different dependence of the capacitance in accumulation with frequency. The underlying substrate can influence subsequent nucleation of the atomic-layer-deposited (ALD) dielectric layers on top, determining the electrical quality of the oxide in the vicinity of the semiconductor interface, and hence the density of border traps [19]. Therefore,it is not straightforward to predict the frequency dispersion in accumulation of as it is jointly determined by parameters such as temperature, density of defects and conduction band offset.

Based on the distributed border traps model previously mentioned, Kim et al. [20] and Dou et al.[6]showed for a given sample, thatit is possible to understand the frequency dispersion of the C–V characteristics of InGaAs metal–oxide-semiconductor (MOS) capacitors in accumulation as variations in the probing depth (from the semiconductor/dielectric interface) reached by the AC measurement signal. Nevertheless, for the case of comparing multiple samples with different High-K dielectrics and/or semiconductor substrates, variations in the conduction band offset might mask changes in the density and spacial distribution of Border Traps, and cause larger dispersion for a less defective dielectric, as shown by Krylov et al in Ref. [18]. Such context, in addition to the lack of direct experimental evidence reporting such comparison makes it necessary to further investigate how the BT distribution impacts on the frequency dispersion, independently of barrier height.

Within this context, an interesting approach is toaddress the issue of frequency dispersion considering a group of stacks with relatively similar conduction band offsets and different trap densities.A goodchoice to combine these two requirements is ALD Al_2O_3,as it can be turned from Al_2O_3 to AlON with the addition of N, which increases the density of traps as N acts as defects precursor[21], while preserving a common interface with the semiconductor[22].

In the present paper, we investigate the capacitance frequency dispersion in accumulation of AlON/InGaAs-based stacks compared to Al_2O_3/InGaAs stacks at room and low temperature. In our experimental conditions, we can assess the influence of the oxide-semiconductor barrier height and the amount of generated defects in the oxide layer through the incorporation of N into the Al_2O_3 layer [21] while preserving the characteristics of the interfacial layer (IL) generated between the InGaAs substrate and the gate dielectric. The role playedby the dielectric/semiconductor interface is revealed by decreasing the temperature during the electrical characterization. Temperature lowering

enlargesthe time response of the oxide traps [6],which lowers the probing depth(X_P) during C-V measurements.these results are then extended to the interpretation of defect profiles for HfO_2 and Al_2O_3 dielectrics on InGaAs substrates.Also, by reporting the frequency dispersion as function of the maximal probing depth, it is possible to separate the contribution of both trap density (changes the total amount of traps being probed) from the conduction band offsets (affects the probing depth).

II. EXPERIMENTAL

All samples were fabricated on identical n-type InGaAs substrates epitaxially grown by Metalorganic Molecular Beam Epitaxy (MOMBE) on InP wafers. The dielectrics were deposited by Atomic Layer Deposition (ALD). Before dielectric deposition, the samples were cleaned in acetone, methanol, and propanol, rinsed in de-ionized water (DI), dipped into a diluted H_2SO_4 solution for 30 seconds, dipped into DI water, and treated with NH_4OH 36% solution for 1 min. The samples were introduced into the ALD chamber within less than 3 min after the pre-deposition treatment. This procedure results in a relatively low density of interface states [23]. The dielectrics thickness was measured by Transmission Electron Microscopy (TEM), and calibrated ellipsometry. The gate electrode, Ti(2nm)/Au(200 nm) was deposited by electron beam deposition and patterned by the lift-off technique. The samples were annealed in N_2 at 400^{o}C for 5 minutes.

Regarding the dielectric employed two different groups of samples were constructed. In the first group, AlO_xN_y dielectric films with different nitrogen concentration were deposited at 270^{o}C using Trimethylaluminium (TMA) as a metal precursor, and H_2O and NH3 as non-metal precursors. This was done by following a super-cycle approach [24], [25]alternating(TMA-H_2O) and (TMA-NH_3) cycles. This procedure allows to incorporate N into the Al_2O_3 layer turning it into AlOxNy, which changes the density of defects in the oxide layer.The different nitrogen concentration was achieved by changing the number (M) of TMA-NH_3 cycles following the TMA-H_2O cycle. The following samples sets were deposited under the described methodology. The TMA-NH_3 sub-cycle count (M) are 20, 5, and 0 for the Sets A, B and C respectively, resulting in a higher concentration of defects for the first set and a lower concentration for the latter. The dielectric thickness (20 nm) was kept constant for all gate stacks. It should be noted that the TMA PDT creates a thin AlO_x (<1 nm) inter layer between InGaAs and the gate oxide, which is a common feature for these three sets of samples[22].It is worth noting that the addition of N is considered to ensure an increase in the density of defects in the ALD Al_2O_3 layer, and not for any fabrication purpose. In the second group, Al_2O_3 (Set D) and HfO_2 (Set E) were deposited on the same n-type InGaAs substrate. Trimethylaluminium and H_2O were the metal precursor and oxidant for Al_2O_3, while tetrakisdimethylamino hafnium (TDMAHf) and NH_3 were used for HfO_2 deposition. The physical thickness of both dielectrics was measured to be 13 nm.

Capacitance–Voltage (C-V) measurements were conducted at different frequencies using an Agilent 4285A LCR meter. Current-Voltage (I-V) measurements were performed using an Agilent 4155C parameter analyzer. The flat-band voltage, V_{FB}, was determined using the recently introduced inflection point technique [26]. All samples were measured at temperatures of 300K (room temperature) and 77K.

III. RESULTS

A. Multi-Frequency Capacitance Voltage Measurements

Figure 1 shows the multi-frequency C–V (MFCV) curves (200Hz to 600KHz) for Set A at 300K and 77K. Strong frequency dispersion of the C–V curves can be observed from the depletion to the accumulation regions, and its magnitude is substantially reduced at low temperature. This effect in the depletion region can be attributed to the interface traps inside the band-gap[27], [28], while in accumulation it can be attributed to border traps[6], [15], [20]. The V_{FB} does not depend on the AC frequency, as expected when using the inflection point technique [26]. At low-temperature, a shift of V_{FB} is observed towards positive bias. This effect has been observed on similar Al_2O_3/InGaAs based stacks [17], and it may be due to the shift in the Fermi level at the semiconductor surface due to trapping effects generated by the temperature dependence in the rate of the emission/capture process [6], [12], [29], [30]. It is worth mentioning that although variations in the semiconductor work function ($_s$) (temperature dependence of the electron affinity ( ), the semiconductor band gap (E_g) and the potential difference between the Fermi level (E_F) and the intrinsic Fermi level (E_i)[12], [29]) could cause such variation, Vais et al. reported an ideal simulation taking non-parabolic band effects intoaccount for Al_2O_3/n- InGaAs stacks without traps, showing very small variations of the V_{FB} at 78 K [19].

Figure 2 shows the capacitance dispersion at a constant voltage in accumulation respect to V_{FB} (V_G-V_{FB}=+2V) as function of the AC signal frequency,calculated as the absolute value of the percent difference ratio ($C_{acc@f1=200Hz}$ - $C_{acc@f=fn}$)/ $C_{acc@f1=200Hz}$. For these samples, changes observed in total accumulation capacitance as the frequency is increased are largely consistent with those reported in the literature [3], [6], [19]. At room temperature (RT), large differences can be observed between the results for each set of samples. Set A (AlON layer with high N concentration) shows the largest frequency dispersion, while the Sets B and C (AlON layer with low N concentration and Al_2O_3 layer respectively) show much lower and similar frequency dispersion. However, at low temperature (LT) all sets of samples show a smaller overall capacitance dispersion with frequency. Note that the Set A (AlON layer with high N concentration) shows the largest reduction of the frequency dispersion in comparison with the rest. This behavior will be discussed in the next section of this work.

Since variations in the oxide thickness have influence on the frequency dispersion in accumulation [18], it is relevant to consider its possible impact in our results. Figure 3 shows, for one set (Set A), a reduction of the capacitancedispersion in accumulation, measured at constant electric field, for increasing oxide thicknesses for 77K and 300K. This effect is in full correlation with recently reported results [18], and it is attributed to the relative contribution of border traps to the dispersion in total accumulation capacitance for a given C_{ox} ($C_{ox} = \varepsilon_{ox}/t_{ox}$, where ε_{ox} is the relative dielectric constant of the dielectric layer, and t_{ox} the thickness of the dielectric layer)[31], which raises for thinner oxides in the border trap lumped model. Furthermore, the reduction in the frequency dispersion at low temperature was observed for all investigated AlON thicknesses. Hence, considering these results, it is possible to infer that small variations of the oxide thickness t_{ox} (due to fabrication uncertainties) in the sets of samples used in this work do not affect the general trend neither at 77K nor at 300K.

The incorporation of N into the Al_2O_3 is responsible for the generation of defects in the oxide layer and a lower conduction band offset, as demonstrated in Ref. [21]. This effect is clearly observed in the

current-voltage characteristics of the sets of samples. Figure 4(a) shows the current-voltage (I-V) characteristics in the accumulation regime (i.e. positive bias) for sets A, B and C. It can be observed that, at room temperature (300K), Set C (Al_2O_3 layer) shows an increase of the leakage current at larger bias (+7V), while Sets B and A (AlON layer with low and high N concentration, respectively) show the increase of the current level at lower biases (+6.5V and +3V respectively). As general trend, the leakage current increases with the N concentration present in the AlON layer and a strong temperature dependence is observed for samples of Set A when lowering the temperature to 77K, where the leakage current decreases almost three orders of magnitude in the low bias range (<+4V).

Lowering the temperature to 77K, sets B and C show negligible dependence of their I-V characteristics with temperature and, more importantly, show virtually the same slope as at 300K. This suggests a temperature independent conduction mechanism, such as Fowler-Nordheim (FN) tunneling [32], as proposed by other authors for similar material systems [33]–[35].

Considering a simple model for FN tunneling [12]through a triangular barrier (see eq.1)with an effective tunneling mass of m* = 0.3 m_0, as a value among those reported in the literature [33], [36], the fitting results report a barrier height decreasing from 2eV for set C, 1.75eV for set B down to 1.3eV for set A as the N density increases in the oxide (Figure 4(b)). It is worth noting that to minimize the influence of other temperature dependent conduction mechanisms, fittings of the I-V measurements considering this FN model have been carried out on low-temperature measurements.This barrier reduction is in agreement with the reduction of the bandgap as the N concentration increases as observed in several dielectrics [21], [37], [38], including AlON[39], [40]. Although the study of I-V variations at low temperature are not within the scope of this work, the observed variation in Set A (AlON layer with high N concentration) at 77K can be linked to the thermally activated behavior of capture and emission times inside the dielectric [41], and the alignment changes with the energy level of oxide traps due to strong temperature dependence of the semiconductor gap at low temperatures [42]. In summary, the larger leakage through AlON compared to that through Al_2O_3 can be attributed to either lower band offsets (lower bandgap) [37]–[40]or/and larger trap density [21]. In our experimental conditions, the I-V characteristic of anAlON layer with low N concentration (Set B)is mainly affected by a lower band offset, while in Set A(AlON layer with high N concentration) the large trap density in the dielectric layer plays a significant role in theaffects the I-V curves at room temperature.

$$J_{FN} = \frac{q^3}{16\pi^2 \hbar \phi_b} F_{ox}^2 e^{\left(-\frac{4\sqrt{2m_{ox}^*}\phi_b^{\frac{3}{2}}}{3F_{ox}\hbar} \right)} \quad (1)$$

These two parameters (band offset and border trap density) have been strongly linked to frequency dispersion in accumulation [6], [15], [18], [19], [21]and therefore this information is useful for the results analysis in the next section of this work.

B. Analysis of the frequency dependent capacitance at low temperature

The models for capacitance dispersion on III-V MOS devices usually involve trap states inside the gate insulator (called border traps or bulk traps), and transport of carriers (i.e. tunneling) from the crystalline semiconductor into these defects [6], [20]. It has been proposed that the response of border traps distributed through the thickness of the oxide is jointly determined by frequency, temperature and the tunneling barrier defined by the conduction band edge of the oxide and the trap energy [6], [19]. Such temperature dependence is inferred from the variation of the time response of the traps (i.e. the average time that an empty trap needs to wait before it captures an electron) when measured at different temperatures. Regarding the physical mechanism involved in the capture/emission process with the border traps, two models were proposed in the literature. While Vais et al [19] reported recently that such effect can be modeled by a combination of tunneling and a non-radiative multi-phonon process (NMP), Dou et al[6] describe the temperature dependence by a thermal activated capture cross-section. It is important to note that the physical mechanism of the capture/emission process only affects the functional dependence of the probing depth with the temperature, but not its general trend. As temperature is lowered, the probing depth (i.e. the region where the trapping/de-trapping processes of the traps contribute to the capacitance) decreases, and thus, the temperature dependent frequency dispersion of the C-V curvesshouldreflect the density of defects/traps in a narrower region near the interface.

$$X_P = \frac{1}{2K(E)} ln\left(\frac{1}{2\pi f \tau_o}\right) \tag{2}$$

$$K(E) = \frac{\sqrt{2m^*(E_C^{ox} - E)}}{\hbar} \tag{3}$$

$$\tau_o = \left[N_{C_0}\left(\frac{T}{T_0}\right)^{\frac{3}{2}} \vartheta_{th_0}\left(\frac{T}{T_0}\right)^{\frac{1}{2}} \sigma_0 e^{\left(\frac{E_b}{kT}\right)}\right]^{-1} \tag{4}$$

Considering the FN barrier height calculated in the previous section, the probing depth (X_P) was calculated according to equations (2) to (4) from Ref. [6]. Particularly, in equation (3) *K(E)* is the attenuation coefficient in the electron wave function for tunneling process, which is determined by the effective electron mass *m** in the oxide, the tunneling barrier is definedby the conduction band edges of the oxide (E_c^{ox}) and the trap energy (*E*), and the reduced plank constant ($\hbar$). In equation (4) τ_0 is the time constant of the interface trap at the same energy level, where N_C is the electron density at the semiconductor surface,σ_0 is the electron capture cross-section of the border traps, v_{th} is the electron thermal velocity, *k* is the Boltzman constant, E_b is thermal activation energy, $T_0$is the room temperature and *T* the probing temperature.The behavior of the probing depth as function of frequency is plotted in the inset of figure 2. Note that the FN barrier height is a good approximation when the Fermi level (E_f) is biased near the conduction band edge (E_C), and when $E_f > E_C$ in strong accumulation[6]. This plot shows how X_P varies with frequency (upper set of curves correspond to low frequency (LF) - 300Hz - and the lower to high frequency (HF) - 200kHz) and temperature, but it also

accounts for band offset dependence, presenting 3 different traces in each of the frequencies considered (LF and HF).Considering these differences and based on the equivalence between probing frequency and probing depth, frequency dispersion has been plotted against the probing depth calculated using expression (2)in figure 5, to get a better understanding of the consequences of the spatial distribution of the traps in the stack. It should be mentioned that in this way, and for a given maximal probing depth, the frequency dispersion can be attributed mainly to a variation in the BT density, as the conduction band offset has already been considered for the X_P calculation.

From Figure 5 and the inset of Figure 2it can be observed for all set of samplesthat the frequency dispersion of the C-V curves, in the range of 300Hz - 200kHzat 77K involve traps up to 0.8nm from the interface (i.e. X_P<0.8nm), while for 300K the probing depth reach 2nm from the interface. At this point, it is worth recalling that the TMA PDT cause the creation of a thin AlOx (<1 nm) interfacial layer (IL) between InGaAs and the gate oxide[22]. Since it is a common feature for all sets of samples, and at low temperature the probing depth is reduced in the range of this IL thickness (see figure 5), defects within this layer can explain the close values of frequency dispersion observed in figure 2.It is worth noting that given the similar values of frequency dispersion at low temperature observed in figure 5, it can be inferred that not only the AlO_X IL is a common feature, but the density of defects present in this region remains approximately constant for all samples regardless of the N concentration. On the contrary, the increase in frequency dispersion for the region going from 1nm to 2nm (measurements performed at 300 °K) suggests an increased BTdensity for this region.

The sets of samples A and C, with different densities of defects distributed along the depth from the interface into the oxide layer, show quite similar capacitance dispersion at 77K, since under this condition the traps far away from the oxide-semiconductor interface do not contribute to the capacitance dispersion (and most of the traps being probed lie within the IL). Regarding Figure 3, where the capacitance dispersion is studied as function of the oxide thickness for a dielectric layer with high density of defects (Set A), it is clear that at 77K the dependence of the capacitance dispersion with the oxide thickness is strongly reduced (in particular for t_{ox}>15nm), indicating that the frequency dispersion is a near interface located phenomenon.

It is worth noting that the observed differences between the probing depths due to the band offsets of thesets of samples (see inset figure 2) have negligible influence on the interpretation of the results, as the probing depth dependence with temperature is much stronger. Therefore, to further assess the impact of the conduction band offset on the C-V dispersion of MOS capacitors, a second subset of samples was investigated. These are MOS stacks with the same metal gate (Ti/Au), substrate (InGaAs), and physical oxide thickness (13 nm), but different dielectric layers, Al_2O_3 for Set D, and HfO_2 for Set E (see Figure 6). The idea of using such materials is to gain an insight into the profile of defects of these two materials and to observe to which extent does the difference in barrier heights impact on the observed dispersion. It should be pointed out that the carrier effective tunneling mass in the oxide also plays an important role on determining the interaction between carriers in the semiconductor and BTs. In this work, these constants are adopted after [43], where very similar values for m^* in HfO_2 and Al_2O_3 were used to extract BT density in similar MOS structures as those

reported here. Therefore, the differences observed in*Xp* as function of temperature in the following analysis are attributed to the conduction band offsets rather to a variation in the effecting electron mass. Nevertheless, it's worth noticing that using different values of *m** reported in the literature for Al_2O_3 and HfO_2[18], [33], [34], [36]does not change the qualitative interpretation of the results. Following the same methodology as for the previous samples, figure 6 shows the capacitance dispersion as function of the AC probing signal frequency. The overall data shows large differences in the capacitance dispersion between the MOS stacks with Al_2O_3 (Set D) and HfO_2 (Set E) as gate oxides. In both cases, 77K and 300K, the stacks with HfO_2 as gate oxide show the largest capacitance frequency dispersion. It is worth to mention that, for both sets of samples, the leakage current level is around 1pA in the DC voltage range of the C-V curves, indicating negligible contribution from additional components.

Dispersion data presented in fig. 6 can be also represented as function of the probing depth, as in figure 5. Plotting the frequency dispersion against the maximal probing depth (X_P) calculated with equations (2) to (4), as shown in Fig 7, reveals, in our experimental conditions and fabrication procedure, that despite the variations in the conduction band offset between samples D and E, the variation in the frequency dispersion can be attributed to a larger density of traps in the Set E, as for a given maximal probing depth (X_P) the frequency dispersion is always bigger for Set E, independently of the temperature. As mentioned above, this is due to the fact that the maximal probing depth already accounts for the barrier height, and the dispersion comparison is done for the same region of the stack. Therefore, an increase of the BT density is the most suitable candidate to explain the larger dispersion. It is worth noting that at 77K, the region being probed is practically the same for both stacks, and Set E shows a clearly higher dispersion. This suggest that the impact of the barrier height in the probing depth is reduced at low temperature

By comparing thefrequency dispersion vs. maximal probing depth plots shown in Figure 5 and Figure 7, it can be seen than this methodology might be useful to qualitatively compare different samples, as it helps to relate the frequency dispersion to a region in the stack. In this case, Fig 5 reveals a common frequency dispersion feature for a region comprising 1nm from the interface (the AlO_X interfacial layer, common to all samples and probed at low temperature) while for higher probing depths (probed at room temperature) it effectively reflects the expected variations in the BT density generated by the increasing N concentration. By contrast, Fig. 7 shows the frequency dispersion vs. maximal probing depth plot of samples containing different dielectrics (Al_2O_3 and HfO_2). For this case for both the region close to the interface and the oxide bulk, the dispersion clearly changes from Set D to Set E, suggesting a difference in the BT densitybetween both stacks, independently of the region being probed. This result is consistent with the fact that contrary to the AlON/InGaAs and Al_2O_3/InGaAs, there is no common interface between these two samples.

Finally, it is worth to note that it was clearly demonstrated by different authors that the interface trap densities (D_{it}) do not play a role in the capacitance frequency dispersion in strong accumulation [18], [44], suggesting that the traps/defects involved in our experimental conditions should be attributed to the dielectric layer in the MOS stacks under study. It is also important to recall that the final values of capacitance dispersion in accumulation are jointly determined by the border traps density and the probing depth. In other words, for two different dielectrics, if the probing depth is the same, changes in

the dispersion should be attributed to a different profile of defects and, vice versa, if the density of defects remains the same in both dielectrics, the probing depth (which depends on temperature, frequency and band offset among other parameters) will have a decisive impact in the dispersion characteristic of the sample.

IV. SUMMARY

In this work, the capacitance frequency dispersion of C-V curves in strong accumulation, commonly observed in III-V MOS stacks, has been studied as function of temperature for different dielectric layers. Different sets of samples using Al_2O_3 or AlON as gate oxide were engineered to include different amounts of defects in the bulk of the oxide through the addition of N, while preserving a common dielectric / semiconductor interface. Within this context, an experimental report on the influence of the border traps density in the frequency dispersion is presented.

At room temperature, the capacitance dispersion has a large contribution from deep traps within the dielectric (i.e. far away from the interface), while at 77K, it is generated by traps near the oxide-semiconductor interface.Hence, based on the experimental results, it has been demonstrated that the capacitance dispersion in strong accumulation reflect the spatial distribution of traps within the oxide.In this case, samples containing a more defective oxide bulk exhibit a lager frequency dispersion at room temperature, while all the samples present a relatively similar frequency dispersion at low temperature.A thin AlO_x(<1 nm) interfacial layer (IL) between InGaAs and the gate oxide is a common feature for all sets of samples, therefore at low temperature where the probing depth is reduced in the range of this interface layer thickness, the defects within this layer can explain the close values of frequency dispersion observed experimentally.

To better understand the influence of the conduction band offsets and the density of border traps, frequency dispersion against probing depth plots are proposed. In that way, and for a given maximal probing depth (X_P), the frequency dispersion can be attributed mainly to a variation in the BT density, as the conduction band offset has already been considered for the X_P calculation.

Moreover, the comparison of HfO_2/InGaAs and Al_2O_3/InGaAs based MOS stacks suggest that a larger high-k/InGaAs barrier is not only mandatory to reduce the leakage current through the gate oxide, but also helps in reducing the capacitance frequency dispersion in accumulation.

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VI. FIGURE CAPTIONS

Figure 1: Typical multi-frequency capacitance-voltage curves (200 Hz to 600KHz) for Set A (AlON with a high concentration of N) at 300K and 77K. Vertical dashed lines indicate the V_{FB} of each set of measurements.

Figure 2: Capacitance dispersion in strong accumulation as function of the frequency used to measure the capacitanceat a constant voltage in accumulation respect to V_{FB} (V_G-V_{FB}=+2V), for sets A, B and C. The inset shows the estimated probing depth of the 300Hz and 200 kHzAC signal

frequency as a function of temperature, according to Ref. [6], using the following parameters Nc = $2.2x10^{17}cm^{3}$, v_{th} = $5.6x10^{7}$cm/s, σ_n = $6x10^{-15}cm^{2}$$Ec_{offset}$(Set A)= 1.38eV, Ec_{offset}(Set B)= 1.77eV, Ec_{offset}(Set C)= 1.94eVand E_b = 65meV [6]. The parameters here adopted are applicable for an n-InGaAs MOS capacitor biased in accumulation.

Figure 3: Capacitance dispersion in strong accumulation measured at constant electric field E_{Ox} and frequency (400KHz) as function of the oxide thickness (tox) for the Set A (AlON layer with a high N concentration) at room temperature (300K) and at 77K.

Figure 4: Typical current-voltage characteristics for positive bias at 300K and 77K (a) and Fowler-Nordheim plot of the of the same measurements showing the fitting results (b). The sets of samples have the same physical thickness of the dielectrics (20nm), substrate (InGaAs), and metal (Ti/Au), but different oxides layers. Set A correspond to aAlON layer with a high N concentration, Set B correspond to a AlON layer with a low N concentration, and Set C correspond to a Al_2O_3 layer.

Figure 5: Capacitance dispersion in strong accumulation as function of maximal probing depth, for sets A, B and C. The inset shows the estimated probing depth of the 300 Hz and 200 kHz AC signal frequency as a function of temperature, according to Ref. [6], using the following parameters Nc = $2.2x10^{17}cm^{3}$, v_{th} = $5.6x10^{7}$cm/s, σ_n = $6x10^{-15}cm^{2}$, Ec_{offset}(Set A)= 1.38eV, Ec_{offset}(Set B)= 1.77eV, Ec_{offset}(Set C)= 1.94eVand E_b = 65meV [6]. The parameters here adopted are applicable for an n-InGaAs MOS capacitor biased in accumulation. The shaded region represents the common AlOx region of approx. 1nm.

Figure 6: Capacitance dispersion in strong accumulation as function of the frequency used to measure the capacitanceat a constant voltage in accumulation respect to V_{FB} (V_G-V_{FB}=+2V), for sets D and E. The inset shows the estimated probing depth of the 200 Hz and 200 kHz AC signal frequency as a function of temperature, according to Ref. [6], using the following parameters: $m^*(Al_2O_3)=0.23m_0$, $m^*(HfO_2)$= $0.22m_0$ [38], $Ec_{offset}(HfO_2)$= 1.4eV, $Ec_{offset}(Al_2O_3)$= 2.3eV, Nc = $2.2x10^{17}cm^{-3}$, v_{th} = $5.6x10^{7}$cm/s, σ_n = $6x10^{-15}cm^{2}$ and E_b = 65meV [6]. The parameters here adopted are applicable for an n-InGaAs MOS capacitor biased in accumulation.

Figure 7: Capacitance dispersion in strong accumulation as function of maximal probing depth, for sets D and E. The inset shows the estimated probing depth of the 200 Hz and 200 kHz AC signal frequency as a function of temperature, according to Ref. [6], using the following parameters: $m^*(Al_2O_3)$= $0.23m_0$, $m^*(HfO_2)$= $0.22m_0$ [38], $Ec_{offset}(HfO_2)$= 1.4eV, $Ec_{offset}(Al_2O_3)$= 2.3eV, Nc = $2.2x10^{17}cm^{-3}$, v_{th} = $5.6x10^{7}$cm/s, σ_n = $6x10^{-15}cm^{2}$ and E_b = 65meV [6]. The parameters here adopted are applicable for an n-InGaAs MOS capacitor biased in accumulation.

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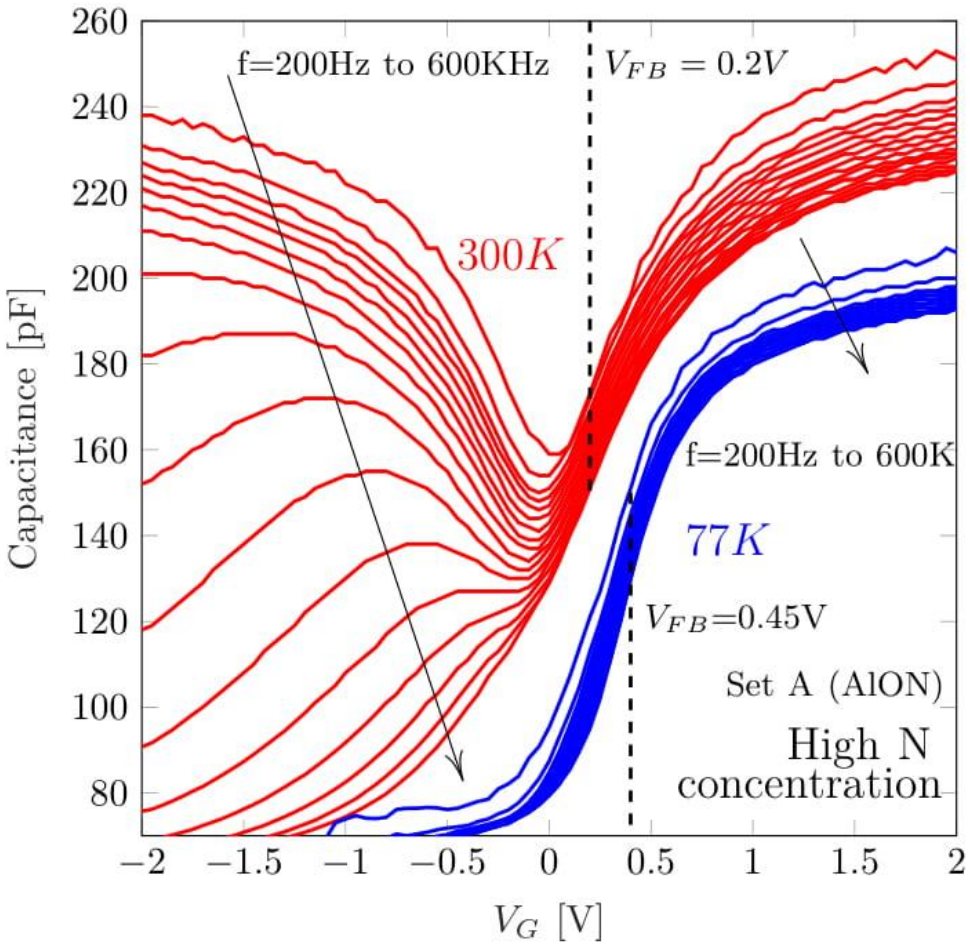

Figure 1

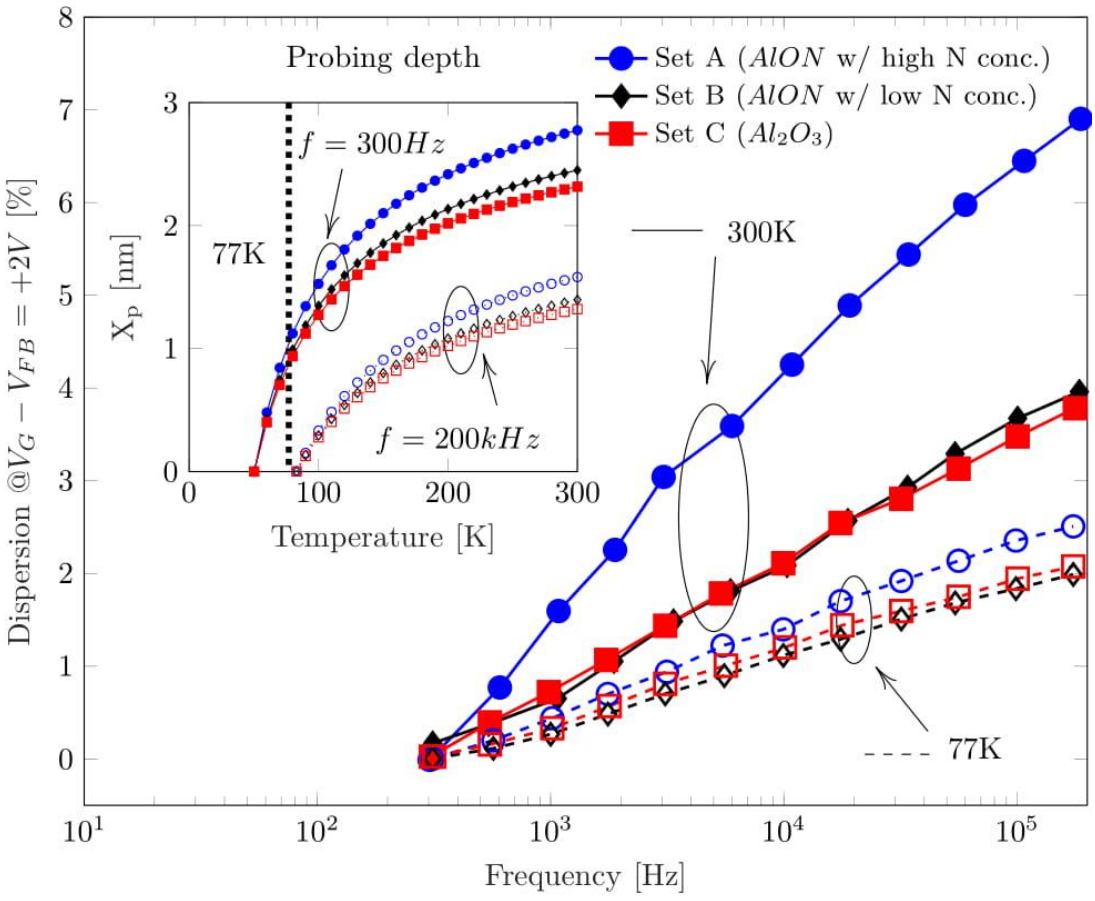

Figure 2

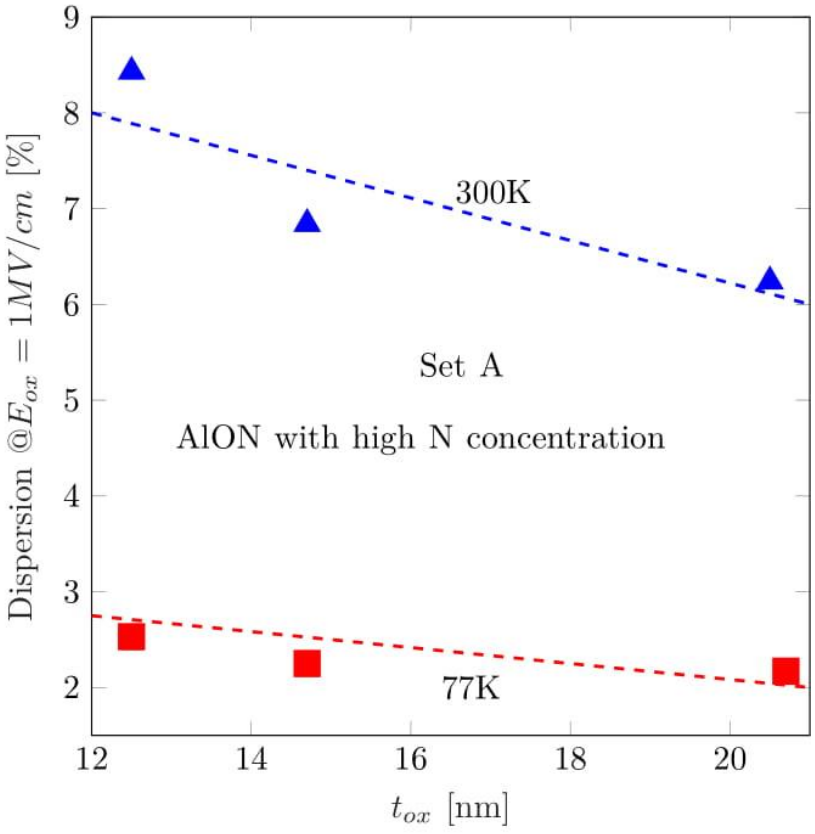

Figure 3

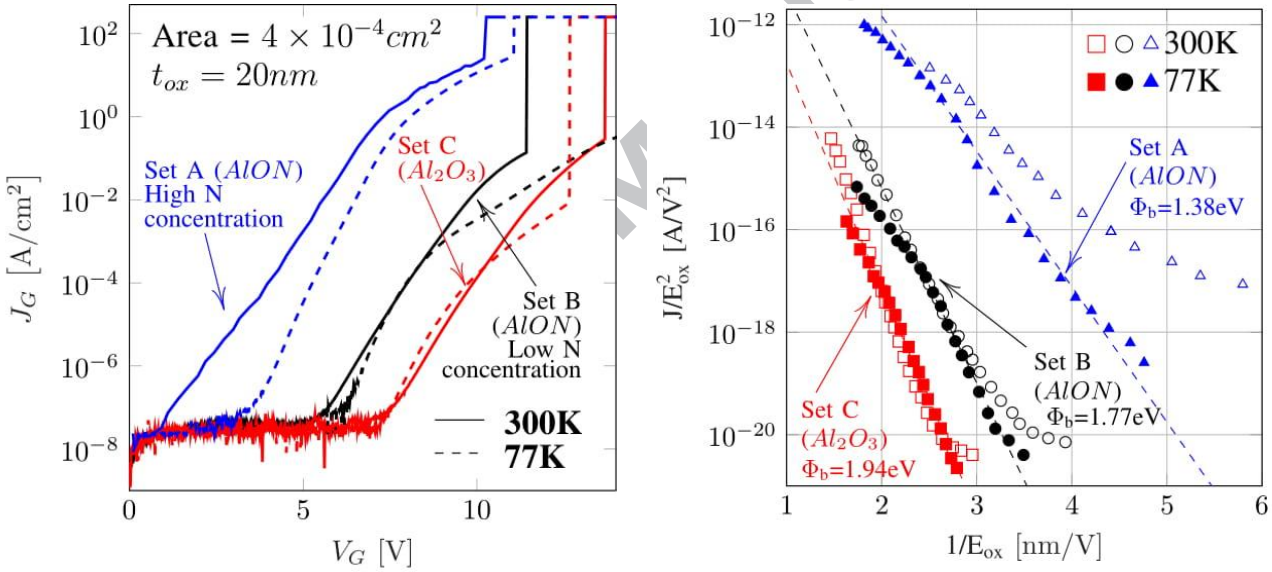

Figure 4

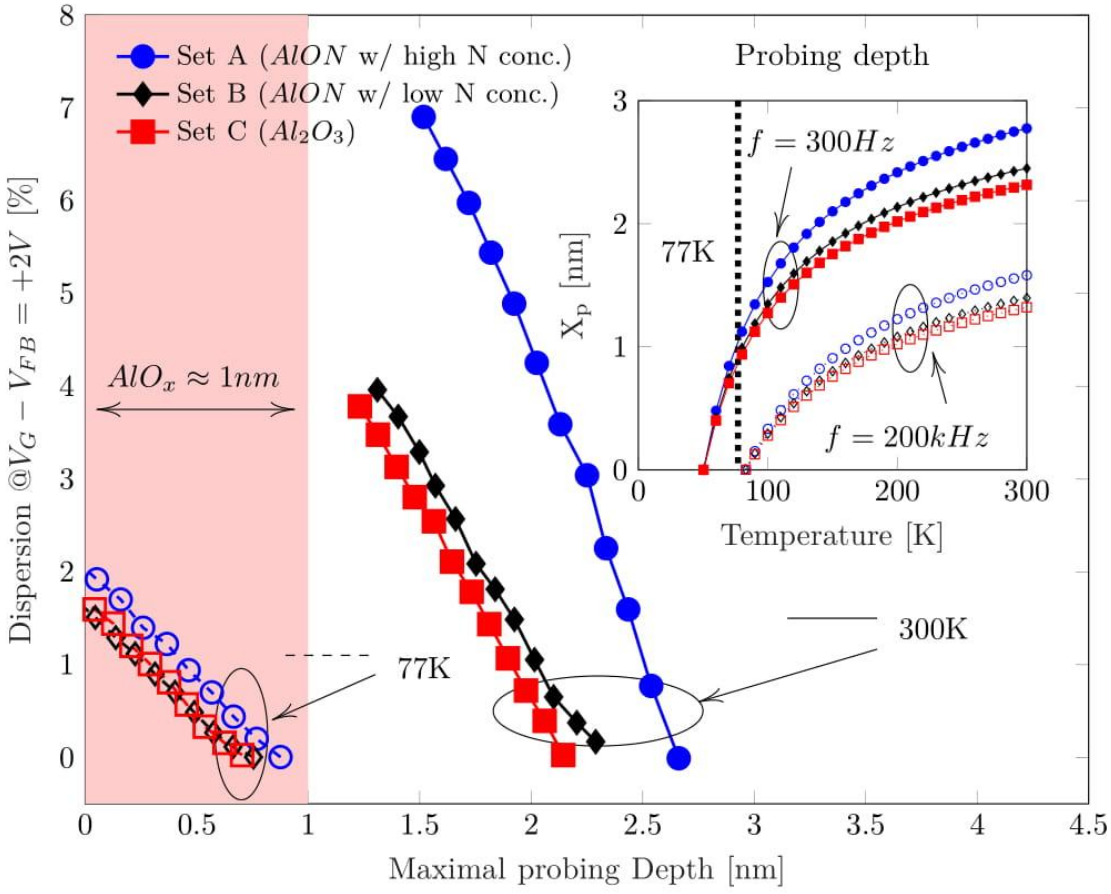

Figure 5

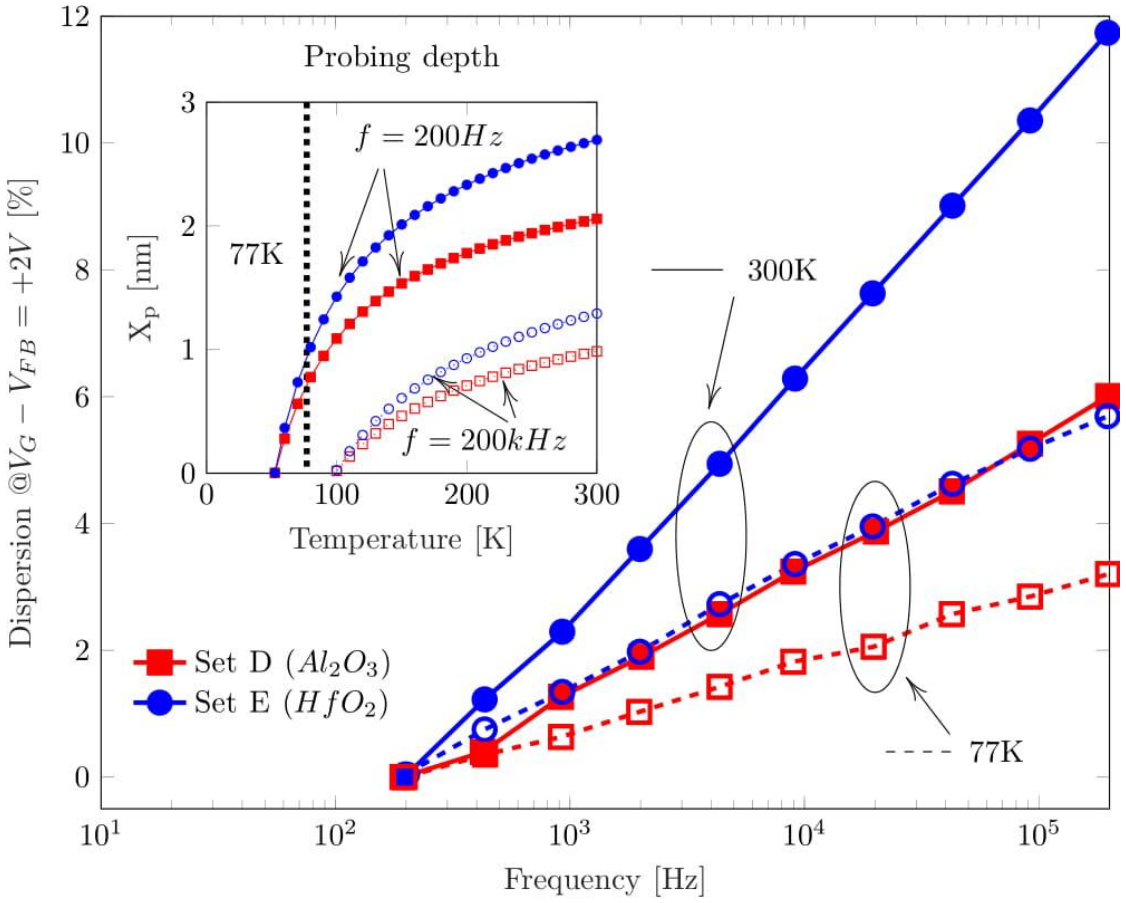

Figure 6

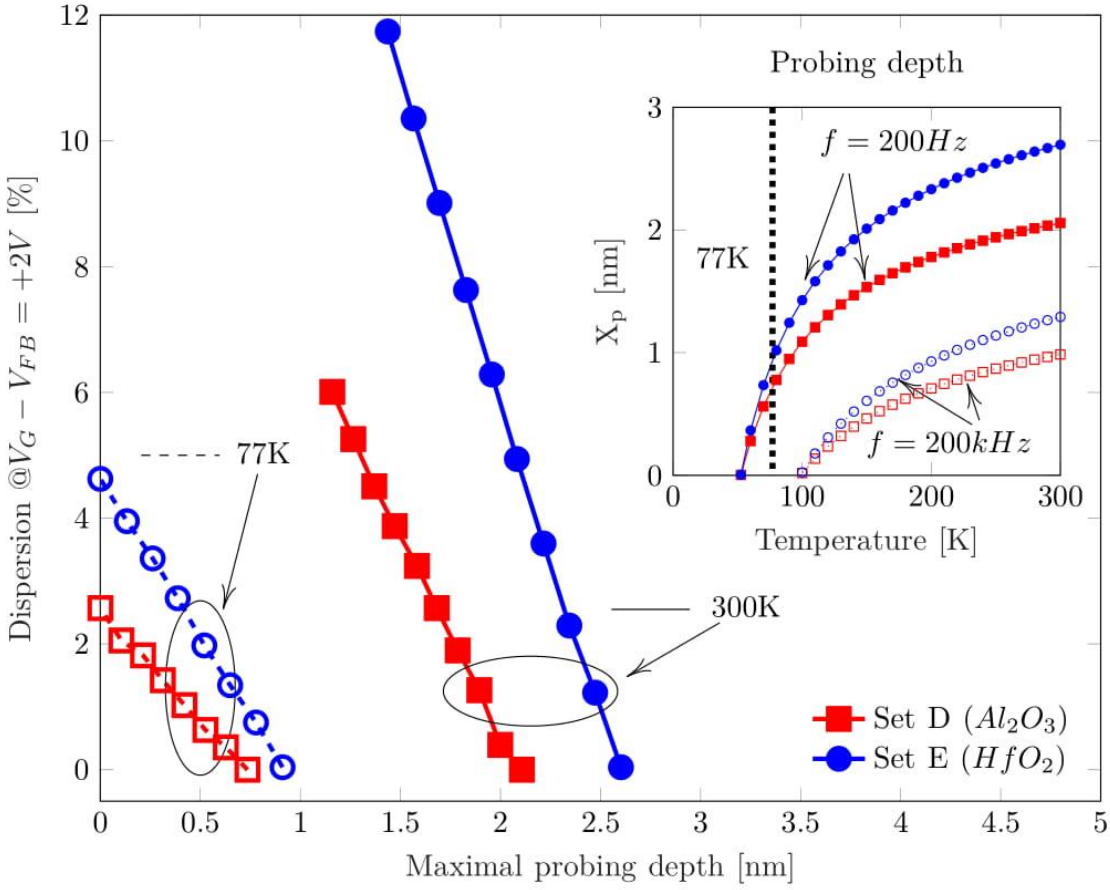

Figure 7

Highlights

•capacitance frequency dispersion in strong accumulation for InGaAs -MOS stacks

• the oxide traps near the high-k/InGaAs interface are responsible for the frequency dispersion at low temperature

•the dielectric/semiconductor conduction band offset is a critical parameter

Felix Palumbo has received the MSc. (2000) and the PhD (2005) both in physics from the University of Buenos Aires, Argentina. He is an active researcher in the field of semiconductor device physics and reliability, transport in mesoscopic systems and oxide-semiconductor interfaces with experience in the academy and industry.

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