A 2-MS/s, 11.22 ENOB, Extended Input Range SAR ADC With Improved DNL and Offset Calculation

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***Abstract*— A 12-bit successive approximation register analog-to-digital converter (ADC) with extended input range is presented. Employing an input sampling scaling technique, the presented ADC can digitize the signals with an input range of 3.2 V_{pp-d} ($\pm$1.33 V_{REF}). The circuit also includes a comparator offset compensation technique that results in a residual offset of less than 0.5 LSB. The chip has been designed and implemented in a 0.13-μm CMOS process and demonstrates the state-of-the-art performance, featuring an SNDR of 69.3 dB and the SFDR of 79 dB without requiring any calibration. Total power consumption of the ADC is 0.9 mW, with a measured differential non-linearity of 1.2/−1.0 LSB and INL of 2.3/−2.2 LSB.**

***Index Terms*— Analog-to-digital converters, SAR, comparator offset, capacitor segmentation, feedback control system.**

I. Introduction

SENSOR-BASED monitoring systems increasingly need signal acquisition systems. Such systems often require analog-to-digital converters (ADCs) capable of digitizing inputs exceeding the core voltages of modern CMOS processes. Also, these ADCs are used in feedback loops, requiring monotonic behavior (with a differential-non-linearity (DNL) not exceeding beyond −1 least-significant-bit (LSB)). Moreover, such systems typically need to operate in very harsh environments and are required to have a life span of several years like any other chip. In addition, maintaining the required performance over the whole life period for such systems is very important [1].

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Successive approximation register (SAR) ADCs have become the architecture of choice for realizing medium resolution, 10-12 bit ADCs, in such applications. Considering the digitally driven nature of modern architectures and the fact that most of them employ switched-capacitors (SC) as the underlying digital-to-analog converter (DAC), makes their implementation in modern CMOS technologies more attractive as compared to other Nyquist rate ADCs (flash, pipeline, subranging ADCs). Other advantages include the scaling of ADC resolution and programmable conversion rates [2], [3].

This paper presents a SAR ADC intended for sensor-based monitoring interfaces. The chips meant for such applications employ the reference signal which is provided by the core supply while the input signals are provided from the input/output (I/O) domain. It is quite useful as chips are becoming more and more digital centric designs and hence to save area and power, there is a push towards smaller nodes. That also means that for some applications the input signal does not scale with process. The proposed architecture targets such applications and is capable of digitizing an input signal up to $\pm$1.33 times the reference voltage, V_{REF}. The conventional scaling approaches employ additional capacitors during sampling phase thus resulting in excessive area consumption [4]. The technique employed in this design, does not require any additional capacitors and can extend the input range to 3.2 V_{pp-d} compared to previous reported architecture having a 2 V_{pp-d} (or $\pm V_{REF}$) [5]. Same technique is extendable to other scaling factors making it an area and power efficient option for the SAR ADCs realization in the latest CMOS nodes for sensor-based interfaces. In addition, a foreground offset compensation technique is presented to dynamically correct any comparator offset that may be present.

Unlike the previously reported approach [6], requiring additional DAC for the offset calibration, the proposed ADC does not have any additional circuitry for offset compensation/calibration, resulting in lower area and power overhead. The SAR ADC is realized with a 6-6 binary weighted attenuation capacitor (BWA) DAC. BWA-DACs are more attractive due to the reduced number of capacitors compared to their conventional binary weighted (CBW) counterparts. However, their linearity is more sensitive to top plate par-

asitic capacitances and capacitor mismatch. To address this, a custom metal-oxide-metal (MOM) capacitor with full shielding having lower parasitic, has been utilized. To reduce the impact of capacitors mismatch, capacitor segmentation has been used in [7]. By segmenting the MSB and MSB-1 capacitors on a 5-bit SAR ADC, the DNL was lowered by a factor of $\sqrt{2}$. This ADC employs a 4-bit segmentation which results in up to 2.82 times better DNL, at 12-bit, when compared to conventional architectures for the same random mismatch, hence improving the resultant monotonicity. Experimental results validate the presented circuits and systems techniques, featuring a competitive behaviour with the state of the art.

The paper is organized as follows. The statistical analysis of the linearity of CBW and BWA based architectures, is presented in Section II. The proposed ADC architecture along with the input scaling technique is detailed in Section III. The circuit level design of the switches and layout of custom MOM capacitors are also presented in the same section. Section IV discusses DAC segmentation and its implementation along with comparator offset calculation technique. The DAC and full ADC layout is given in Section V. Finally, experimental results are presented in Section VI and conclusions are drawn in Section VII.

II. Background on Linearity of SAR ADCs

The linearity of the overall SAR ADC is determined by the linearity of the DAC. Over the years, several DAC architectures have been proposed [5]–[12]. Two of the most important architectures include the SC and resistive ladder DACs [7], [10]. In modern CMOS processes, resistor mismatches are much higher than capacitors [13]. Moreover the area and power requirements with the SC implementation are drastically reduced compared to the equivalent switched resistor implementations [13]. Therefore, the majority of SAR ADCs employ capacitive DACs. Two commonly employed capacitive DAC architectures are the CBW and the BWA DACs [14]. The linearity of a SAR ADC, specifically the integral-non-linearity (INL) and DNL are deteriorated once the capacitor ratios inside the embedded DACs deviate. Two important factors deteriorating the capacitor ratios inside DAC are the parasitic capacitances and capacitor mismatches. This section gives a comprehensive linearity analysis of BWA and CBW architectures considering parasitic capacitances and capacitor mismatches (with bottom plate sampling).

A. Effect of Parasitic Capacitances on Linearity

As the bottom plate of the capacitors are connected to input and references sources, therefore, the parasitic capacitance from the bottom plate to substrate do not impact the linearity. Moreover, the top plate parasitic capacitance to the substrate does not impact the linearity performance of CBW architectures [14].

A single-ended simplified version of N-bit CBW DAC array having a unit capacitor C_U is depicted in Fig. 1. The binary weighted capacitors inside the capacitor array are controlled by

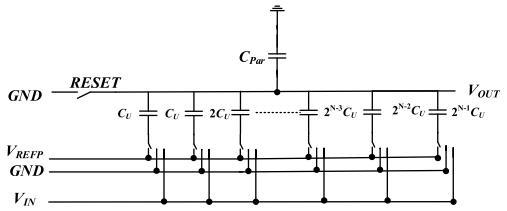

Fig. 1. Parasitic capacitance in CBW DAC.

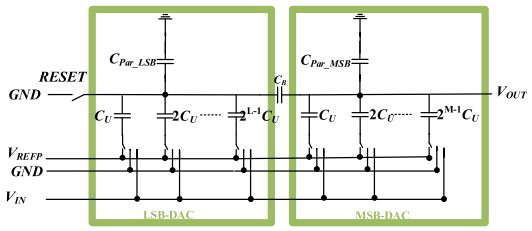

Fig. 2. Parasitic capacitance in BWA DAC.

the control signals which are generated from the SAR logic. Based on the states of control signals, voltage at top plate (i.e. V_{Out}) is given as:

$$V_{Out} = V_{REF}\left[\frac{\sum_{i=0}^{N} C_i D_i}{C_{Total} + C_{Par}}\right] \tag{1}$$

where C_i is the i^{th} capacitor in the DAC array (i.e. $2^{(i-1)}C_U$), C_{Total} is the total capacitance and C_{Par} represents the parasitic capacitances connected from the top plate of capacitor array to ground. It is apparent from (1), that C_{Par} impacts the magnitude of the V_{Out}, but it does not influence its polarity [14], [15].

A single-ended version of capacitor array in a BWA DAC is illustrated in Fig. 2, with MSB-side and LSB-side DACs consisting of M and L bits respectively with $M = L = N/2$. The output voltage at the top plate of MSB-side, which connects to the comparator input, can be written as [14]–[16]:

$$V_{Out} \cong V_{REF}\left[\frac{\sum_{i=0}^{M-1} C_i D_i}{C_{Total\_MSB} + C_{Par\_MSB}}\right] + A_{tt}C\left(V_{REF}\left[\frac{\sum_{i=0}^{L-1} C_i D_i}{C_{Total_LSB} + C_{Par\_LSB}}\right]\right) \tag{2}$$

where

$$A_{tt}C = \left[\frac{C_U}{C_{Total\_MSB} + C_{Par\_MSB}}\right]$$

Shown in (2), is that effect of the top-plate parasitic at the LSB-side (i.e. C_{Par_LSB}) on output voltage of DAC

(i.e. V_{Out}), which is not constant with changing input digital code and hence results in degraded linearity. On the other hand, the effect of top plate parasitic capacitances on the MSB-side (i.e. C_{Par_MSB}) only impacts the magnitude. For the case $M = L = N/2$ the maximum DNL occurs every $2^{N/2}$ codes and is given as [14]:

$$DNL \cong V_{REF}\left[\frac{(2^N - 2^{N/2})C_{Par\_LSB} + 2C_U}{2^N C_U}\right] \quad (3)$$

The proposed ADC employs a 6-6 BWA DAC based architecture and requires a monotonic behavior (DNL not exceeding beyond -1 LSB). Equation (3) shows that in order to keep the DNL within the ± 1 LSB, C_{Par_LSB} should be smaller than C_U. Usually the MOM capacitors available in 0.13-μm CMOS design kit feature a top plate parasitic in the range of 5-to-7% (exact value of parasitics depend upon the unit capacitor value). In that sense, as an example, for a 6-6 BWA DAC based ADC with a C_U of 20 fF, resultant C_{Par_LSB} could be in the range of 64 fF-to-89.6 fF. In order to keep C_{Par_LSB} lower than C_U, maximum allowable top plate parasitic capacitance for a single C_U should not exceed 1.5%. Therefore, a custom MOM capacitor having lower top plate parasitic (lower than 0.25%) has been designed for this ADC. A detailed discussion about custom MOM capacitor architecture is given in Section III.

B. Effect of Capacitor Mismatch on Linearity

Capacitor mismatch is a major limitation in realizing higher resolution SAR ADCs. Capacitor mismatch can be modelled assuming a Gaussian probability distribution of the unit capacitor value with a mean equal to the nominal capacitance, C_U, and a standard deviation of ΔC_U [16]:

$$[\Delta C] = \frac{K_C C_U}{2A} = K_C\sqrt{\frac{C_{Sperc}C_U}{2}} \quad (4)$$

where K_C, A and C_{Spec} being the Pelgrom mismatch coefficient [17], the capacitor area and the specific capacitance, respectively.

This expression can be used as a starting point for the evaluation of the different trade-offs associated with the capacitor mismatch. For a large device area, the effects associated with area dominate, and dependency in (4) is reduced to Pelgrom's mismatch coefficient and $1/\sqrt{A}$. However, for a small device area, the mismatch is dominated by the edge effects of the process. Hence, the actual mismatch of the device due to device area and the edge effects is determined by process and the topology of the capacitor.

Due to mismatch, the DAC output voltage deviates from nominal values resulting in linearity degradation. In CBW based architectures, the impact of mismatch is worst at the mid code transition, as the number of capacitors changing their states could be maximum during this transition. Theoretically the variance of maximum DNL and INL during this bit trial

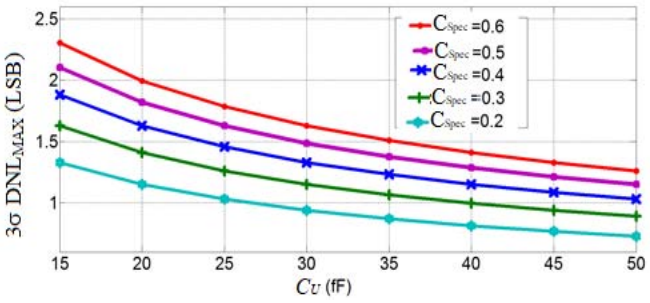

Fig. 3. $3\sigma(\mathrm{DNL}_{MAX})$ incurred for BWA DAC based SAR ADC over a range of CU and Cspec .

is given as [16]:

$$\sigma\,(DNL)_{CBW,MAX} = 2^{N/2}\left(\Delta C/C_U\right)V_{REFP} \quad (5)$$

$$\sigma\,(DNL)_{CBW,MAX} = 2^{N/2}\left(K_C \cdot \sqrt{\frac{C_{Spec}}{2.C_U}}\right)V_{REFP} \quad (6)$$

$$\sigma\,(INL)_{CBW,MAX} = \sigma\,(DNL)_{CBW,MAX} = 2^{N/2-1}\left(\Delta C/C_U\right)V_{REFP} \quad (7)$$

$$\sigma\,(INL)_{CBW,MAX} = 2^{N/2-1}\left(K_C \cdot \sqrt{\frac{C_{Spec}}{2.C_U}}\right)V_{REFP} \quad (8)$$

In the case of a differential implementation, number of capacitors is doubled; therefore, the variance of maximum DNL and INL is scaled by $\sqrt{2}$. For BWA architectures, as illustrated in Fig. 2, the worst case standard deviation of INL and DNL also occurs at mid code transition. For an N-bit BWA-DAC with MSB and LSB-DACs, both having $N/2$ bits, the variance of maximum DNL and INL can be written as [16]:

$$\sigma\,(DNL)_{BWA,MAX} = 2^{3N/4}\left(K_C \cdot \sqrt{\frac{C_{Spec}}{2C_U}}\right)V_{REFP} \quad (9)$$

$$\sigma\,(INL)_{BWA,MAX} = 2^{3N/4-1}\left(K_C \cdot \sqrt{\frac{C_{Spec}}{2C_U}}\right)V_{REFP} \quad (10)$$

Equations (9) and (10) set the achievable DNL and INL for the given mismatch. The MOM capacitor mismatch is approximately three times that of MIM capacitors (having same area) [18]. Based upon the mismatch data from different design kits, K_C for a MOM capacitor having the same capacitance as that of a MIM, as a rough estimate, can be taken as 2.55% μm (i.e. 3×0.85). For high level analysis, 3% μm is a good approximation. Employing equation (10) with a K_C of 3% μm, the value of the standard variance of the maximum DNL for a 6-6 BWA architecture are calculated for different values of C_U and C_{Spec}. The resulting $3\sigma(DNL_{MAX})$ over a wider range of C_U and C_{Spec} is illustrated in Fig. 3. It demonstrates that a C_U of 20 fF having C_{spec} below 0.2 fF/μm2 can achieve the required linearity performance (DNL $< \pm 1$ LSB). But the resulting area for such a low C_{spec} becomes too large (as an example 100 μm^2 for a capacitor

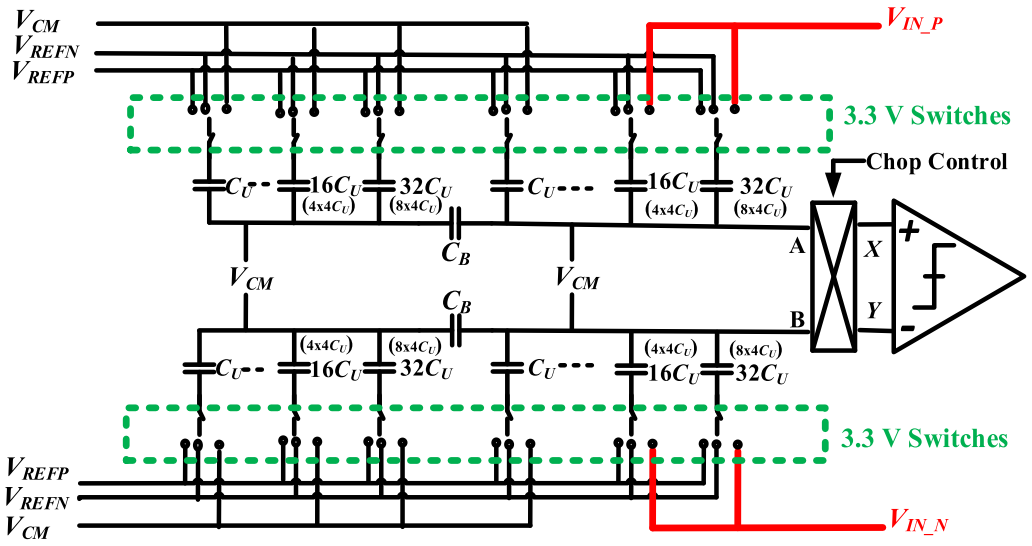

Fig. 4. Proposed 6-6 BWA 12 bit SAR ADC architecture with input scaling.

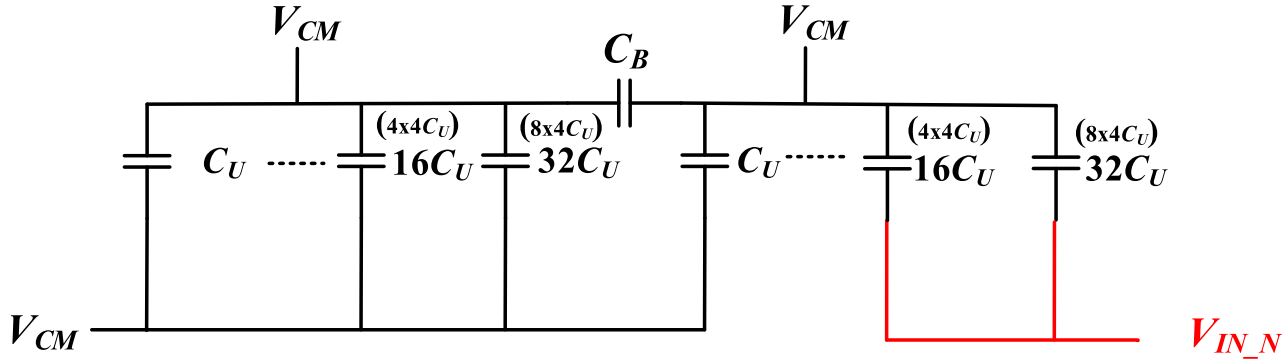

Fig. 5. Sampling of the input voltage.

of 20 fF). In order to obtain the desired linearity performance with a smaller C_U either calibration or some other measures need to be employed. This ADC employs a 4-bit segmentation in the MSB-DAC to achieve better linearity which results in up to 2.82 times better DNL than the conventional architecture.

III. ADC Architecture and Input Scaling

The proposed SAR ADC architecture is illustrated in Fig. 4. For a given C_U, BWA DAC implementation is more efficient in terms of area. Therefore, a 6-6 BWA architecture has been selected for this ADC.

The circuit employs bottom plate sampling. The bottom plate sampling ensures that the large input signal is not applied directly to the comparator inputs, hence enabling the comparator to be realised using core 1.2 V devices. In addition, the input signal is not sampled onto the LSB-DAC, as the voltage on the top-plate of the LSB-DAC could otherwise exceed the core power rails (0 or 1.2 V) during the bit trials, ensuring that the parasitic diode of the top plate switches do not turn ON. If these diodes are turned ON, it could result in a loss of sampled charge and hence corrupt the sampled input signal. In this architecture, input sampling scaling is realized by only sampling the input signal onto the bottom plates of the MSB and MSB-1 capacitors while the common mode voltage (V_{CM}) is sampled onto the bottom plate of all the remaining capacitors as shown in Fig. 5. In this way, the input is sampled onto the ¾ of total effective capacitance and has the effect of scaling the input signal by ¾. By employing a different number of input capacitors during sampling phase, this technique can be further extended to realise different input scaling ratios to enable larger input ranges.

A. Switches

CMOS switches are used to connect the capacitors of the DAC to the reference voltages (V_{REFP} and V_{REFN}), the input signal (V_{IN}) and the V_{CM}. In order to balance the parasitic capacitance and to facilitate the capacitor segmentation, a modular design approach has been used when designing and completing the capacitor array. Capacitors in the DAC are arranged in the columns of 4 unit capacitors (i.e. 4 C_Us). An equivalent single ended DAC schematic is shown in Fig. 6. Hence, the MSB capacitor consists of 8 columns; the MSB-1 capacitor consists of 4 columns and so on. Each capacitor column is controlled by an independent set of three switches (SW_{REFP}, SW_{REFN} and $SW_{IN\_}$. The top plates of all columns (either MSB-DAC or LSB-DAC)

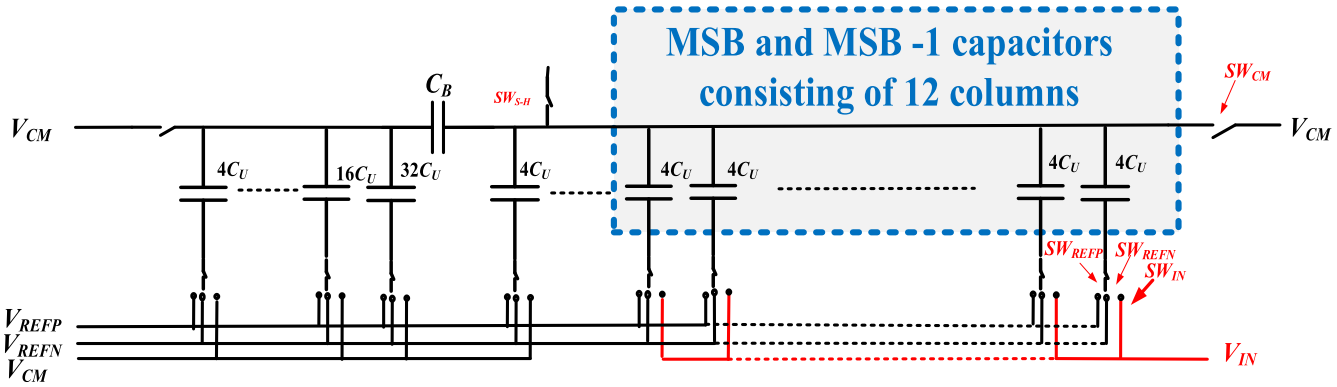

Fig. 6. Simplified schematic of SE DAC of the SAR ADC.

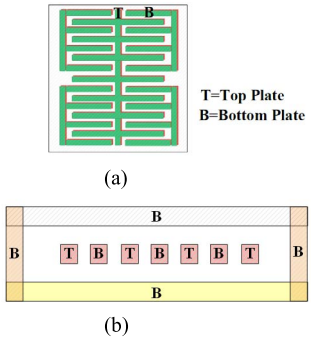

Fig. 7. MOM Cap (a) Top view (b) Cross-sectional view.

are shorted together and connect to V_{CM} using $\mathrm{SW_{CM}}$. The reference switches (SW_{REFP} and SW_{REFN}) are activated during bit trials to connect the bottom plates to V_{REFP} and V_{REFN}, respectively. Due to ease of implementation and reliability, the ADC employs 3.3 V NMOS IO devices for the input (V_{IN}, 0-to-3.2 V_{pp_d}), V_{REFP} (1.2 V), V_{REFN} (0 V) and V_{CM} (0.8 V) switches.

B. Custom MOM Capacitors

As stated in Section II, in terms of parasitics, a DNL of ± 1 LSB requires the capacitors with a top plate parasitics lower than 1.5%. Therefore, a custom MOM capacitor having top plate parasitic lower than 0.25% has been designed.

The top and cross-sectional views of the custom MOM capacitor are depicted in Fig. 7 (a) and (b), respectively. The top and bottom plates of capacitor consist of metal 3 and 4 with each plate consisting of 8 inter-digitated fingers. The capacitor top plate is shielded with metal 2 and metal 5, which are connected to the bottom plate of the capacitor. As bottom plate surrounds the top plate in all directions, therefore, any parasitic capacitance from the top plate is to the bottom plate, where it adds to the core capacitance only (main capacitance between top and bottom plates), and not to ground where it would impact on the resultant DAC linearity. The entire structure of the capacitor array is placed in N-well to further isolate it from the P-substrate. It also mimics the capacitances to the adjacent capacitors/columns. The size of a single C_U is 8 μm $\times$ 8 μm. The extracted capacitance between top and bottom plates is 20 fF. The top and bottom plate to substrate parasitic capacitances are 40 aF (0.2%) and 1.2 fF (6.2%), respectively.

IV. Techniques to Improve DAC Linearity and Reduce Comparator Offset

The DAC is the most important block in SAR ADC, and is used for sampling and reference generation. It was shown in Section II that capacitor mismatches limit the achievable linearity. Capacitor segmentation has already been used to improve the DNL of an ADC [7]. This ADC employs 4-level segmentation to achieve better linearity. This section explains the segmentation algorithm for a 2-bit SAR ADC, followed by a qualitative analysis of a 4-bit segmented DAC and its associated achievable performance. Also, the comparator offset correction is explained in this section.

A. DAC Segmentation

A detailed analysis of DAC segmentation is given in [7] and [19]–[21]. For the purpose of analysis, a 2-bit binary CBW-DAC based SAR ADC has been chosen (as illustrated in Fig. 8). Fig. 8 (a) and (b) shows the switching of capacitor array in conventional and segmented DACs, respectively. Here the unit capacitor value is C_U. In Fig. 8, C_{U1} represents the LSB-capacitor while the MSB-capacitor is split into two equal parts; $C_{U2,0}$ and $C_{U2,1}$. All of these unit capacitors have equal capacitances i.e. $C_{U2,1} = C_{U2,0} = C_{U1} = C_{U.}$. The conversion process starts by sampling the input signal onto the bottom plates of all capacitors. During sampling phase, connections of all the capacitors are same in both types of DACs (i.e. conventional and segmented DACs). After sampling, during first bit trial, in both switching algorithms, all of the MSB capacitors (i.e. $C_{U2,0}$ and $C_{U2,1}$) are connected to V_{REFP} (i.e. positive reference), while the LSB-capacitor (C_{U1}) is connected to V_{REFN} (negative reference).

Resultantly, voltage at the comparator's input becomes $V_{\mathrm{X}} = -V_{IN} + V_{REFP}/2$. If $V_{\mathrm{IN}} > V_{REFP}/2$ then $V_{\mathrm{X}} < 0$ and the comparator output is "1." Therefore, during the next trial, an "up" transition is to be performed. Due to "up" transition, during the second bit trial, number of capacitors connected to V_{REFP} need to be increased. For this transition, capacitors in both DACs change their states in the same way. All the

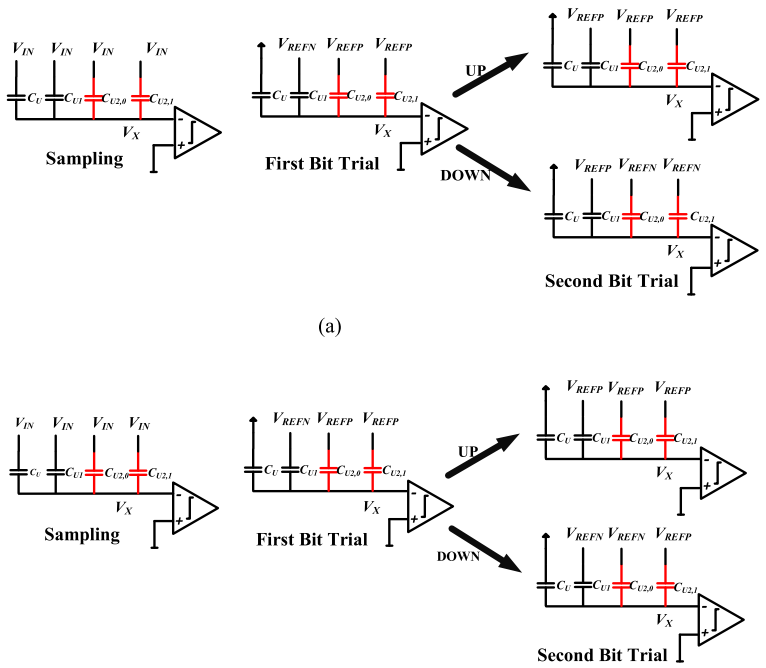

Fig. 8. 2 bit SAR ADC operation with (a) Conventional DAC (b) Segmented DAC.

capacitors in the MSB-capacitor (i.e. $C_{U2,0}$ and $C_{U2,1}$) remain connected to the V_{REFP} while the LSB capacitor (i.e. C_{U1}) is also connected to V_{REFP} (as depicted by the "up" transition part of the second bit trial of Fig. 8(a) and (b)). Therefore, the comparator input becomes $V_X = -V_{IN} + 3V_{REFP}/4$. Based upon this input, second output bit is obtained.

On the other hand, if during the first bit trial, $V_{IN} < V_{REFP}/2$ then $V_X > 0$ and the comparator output is "0." Therefore, during the next trial, a "down" transition is to be performed. Hence, number of capacitors connected to V_{REFN} need to be increased. For this transition, conventional DAC and segmented DAC behave differently. In conventional DAC, (as depicted by the "down" transition part of the second bit trial of Fig. 8(a)), the MSB capacitors ($C_{U2,0}$ and $C_{U2,1}$) change their state from V_{REFP} to V_{REFN} while LSB capacitor (C_{U1}) changes it's state from V_{REFN} to V_{REFP}. During this bit trial, the maximum number of capacitors changes their states (i.e. 3 capacitors) in conventional DAC. In contrast to this, in a segmented DAC, half of MSB-array capacitors (i.e. $C_{U2,1}$) change its state to V_{REFN} while other half i.e. ($C_{U2,0}$) is connected to V_{REFP} (as depicted by the "down" transition part of the second bit trial of Fig. 8(b)). LSB capacitor (C_{U1}) remains connected to V_{REFN}. Therefore, only one capacitor (unlike 3 in conventional DAC) changes its state (i.e. $C_{U2,1}$) and hence result in lower differential non-linearity (i.e. DNL). The same concept can be extended to multibit implementation as stated in the next section.

B. Linearity Analysis of Segmented DAC Array

It was discussed out in Section II that for a BWA architecture, the worst case standard deviation of INL and DNL at mid (MSB-1)th bit trial. For an N-bit BWA-DAC with MSB and

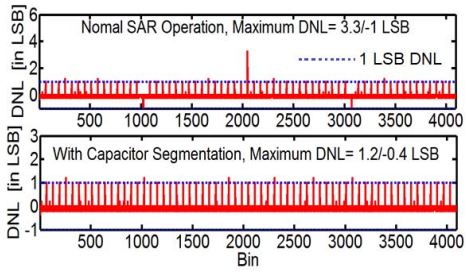

Fig. 9. DNL Plots of 12-bit SAR ADC, 0.81% mismatch in MSB and MSB-1 in 6-6 BWA based SAR ADC with conventional and segmented DACs.

LSB-DACs having M and L bits such that $M = L = N/2$ bits, the variance of maximum DNL is given as [16]:

$$\sigma\,(DNL)_{MAX} = 2^{3N/4}\left(\Delta C/C_U\right) V_{REFP} \tag{11}$$

Now consider the DAC where upper "K" bits out of "M" bits are segmented. In this configuration, the maximum number of switching occurs during the (MSB-1-K)th bit trial, resulting in the maximum DNL. The variance of maximum DNL during this bit trial can be written as follows [19]:

$$\sigma\,(DNL)_{MAX,Segmented} = 2^{\binom{3N/4-\sqrt{K}}{}}\left(\Delta C/C_U\right) V_{REFP} \tag{12}$$

A comparison of (11) and (12) shows that the maximum standard deviation of DNL in the segmented DAC is reduced by a factor of $\sqrt{K}$.

In the proposed architecture, the upper 4-bits of MSB-DAC are segmented. Multiple Monte Carlo runs with Gaussian

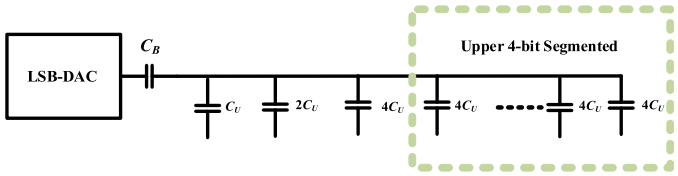

Fig. 10. 6-6 BWA DAC having MSB-DAC with 4 upper bits segmented.

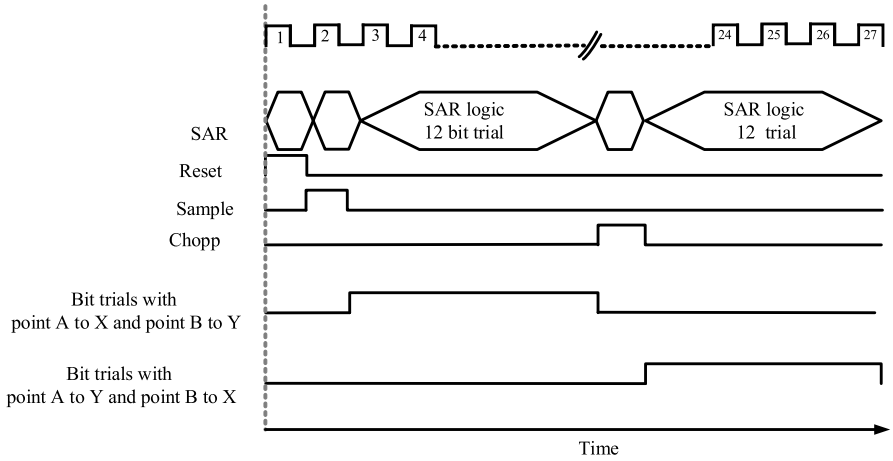

Fig. 11. ADC operation sequence in offset-calculation.

distributed mismatch errors in capacitors ($\Delta C_U/C_U$ = 0.5-to-3%) were performed at behavioral level to validate the accuracy of segmentation. As an example, Fig. 9 presents the DNL plot with conventional and segmentation approach while having 0.81% mismatch in MSB and MSB-1 capacitors

As discussed earlier, the capacitors in DAC are arranged in columns with each column consisting of 4 C_Us and are controlled by an independent set bottom plate switches. This arrangement also enables the capacitor segmentation. For 4-bit capacitor segmentation, 17 additional sets of bottom plate signals are required to be generated from the SAR. The capacitor array schematic with 4 upper bit segmented is illustrated in Fig. 10.

C. Comparator Offset Removal

The comparator offset can vary with time due to temperature and aging effects and is the primary source of offset within the ADC. As described in Section I, the proposed ADC is going to be incorporated in a sensor-based monitoring system that will have a life span of several years (5-to-10) and hence requires an accurate and dynamic estimation of the ADC offset. A chopping circuit is placed at the comparator's differential inputs. The SAR ADC operation sequence during offset-calculation mode is depicted in Fig. 11. As a first step, the nodes A and B are initially connected to nodes X and Y, respectively, as shown in Fig. 4. After the reset and sampling phase, the SAR algorithm goes through a regular bit trial sequence. However, instead of progressing to the next sample, the comparator inputs are then switched, thus connecting nodes A and B with Y and X, respectively. The two respective digital outputs are then processed to find the offset.

The offset-calculation can be performed for any input level. When run in offset-calculation mode, two output codes are obtained which are subsequently averaged and the offset is determined. Based upon the requirement of offset-calculation frequency, ADC can be run in this mode. ADC has a conversion time of 0.5 μs (i.e. output rate = 2 MS/s) and requires 1 μs in offset-calculation mode. As an example, ADC can be run in normal mode for a longer time (let's say 1 ms) and then in the offset-calculation mode for a single time (i.e. 1 μs). In this sense, the impact of offset-calculation upon the throughput of ADC is not significant. Offset-calculation mode is activated using a control signal of SAR logic that can be controlled from outside.

V. ADC Layout and Chip Implementation

The proposed SAR ADC has been designed and fabricated in a 0.13-μm 1P6M CMOS process. For better noise isolation, all NMOS devices are placed in deep-n-well (DNW). The unit capacitors in the DAC are arranged in columns with each column consisting of 4 C_Us, with additional dummy capacitors added for matching purposes. All the capacitor columns in the array are arranged in pseudo common centroid fashion to facilitate the routing and at the same time improving the relative matching as depicted in Fig. 12. Here 32, 16, 8, 4 represent the MSB, MSB-1 and MSB-2 capacitors respectively and so on. The complete capacitor array is surrounded by two rows (above and below) and two columns (at either ends) of dummy capacitors. Bridge capacitor has been realized using the same structure as the other capacitors but with slightly larger finger sizes to get the desired value. A complete layout of the full DAC along with switches, break-before-make (BBM) circuits and level shifters is depicted in Fig. 13. The ADC layout along

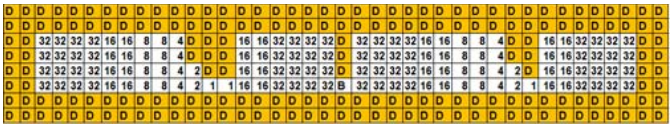

Fig. 12. Pseudo-random arrangement of capacitors.

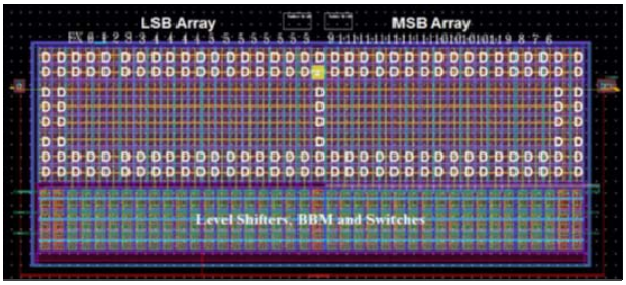

Fig. 13. Complete DAC layout with capacitor array, switches, BBM and level shifters.

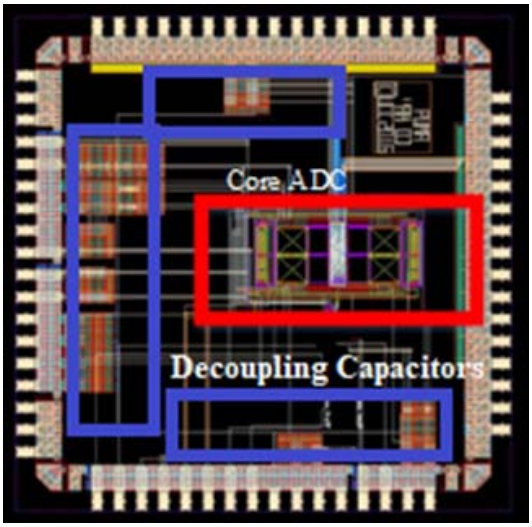

Fig. 14. Core ADC and IO ring.

with the IO ring is shown in Fig. 14. The dimensions of the core ADC are 640 μm $\times$ 370 μm. The vacant regions of the chip are filled with the decoupling capacitors. Fig. 15 shows the chip photograph highlighting its main parts, namely: SAR logic, level shifters, switches and capacitor array.

VI. Experimental Results

A photograph of test PCB and a block diagram of test setup are shown in Fig. 16 and 17 respectively. The ADC has been characterized at an output data rate of 2 MS/s. The comparator, SAR logic and BBM circuits have been realized with low voltage devices and operate at 1.2 V supply. The input and reference switches operate at a 3.3 V supply.

At first, the ADC was run in the offset-calculation mode. To this end, ADC was characterized with differential DC inputs with different inputs (i.e. 0-to-1.6 V). The measured offset is 340 μV. The dynamic performance of the ADC is characterized by means of applying a sinusoid signals to

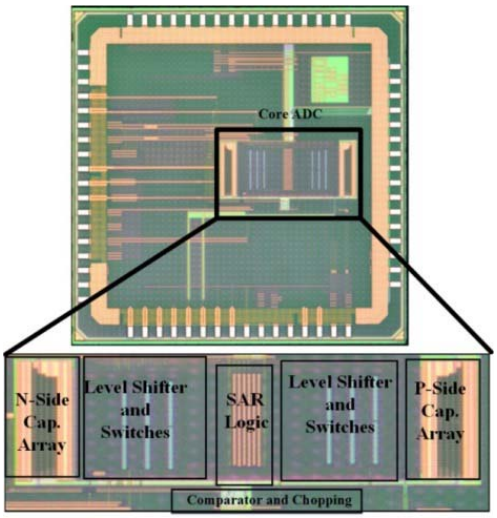

Fig. 15. Chip micrograph and core ADC.

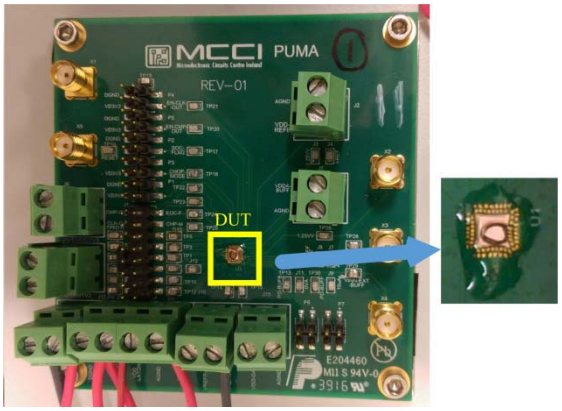

Fig. 16. Photograph of test-PCB.

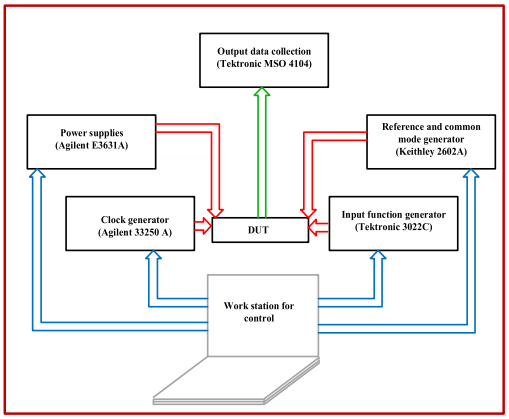

Fig. 17. Block diagram of test setup.

the input over the range of 100 kHz-to-1 MHz (i.e. Nyquist Frequency). The test setup is depicted in Fig. 17. A differential input or sinusoid is provided using an arbitrary function generator (Tektronix 3022C). A highly precise DC voltage source (Keithley 2602A) capable of providing accuracy in the order of nV, has been utilized for the reference and

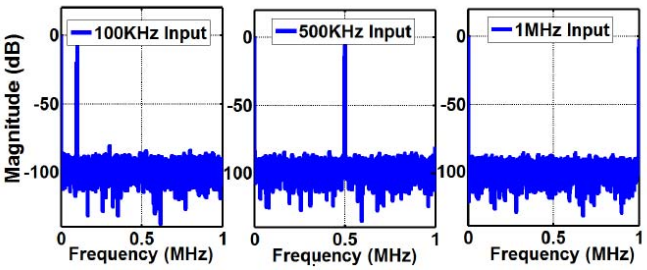

Fig. 18. Measured FFT spectrum of 3 different frequencies.

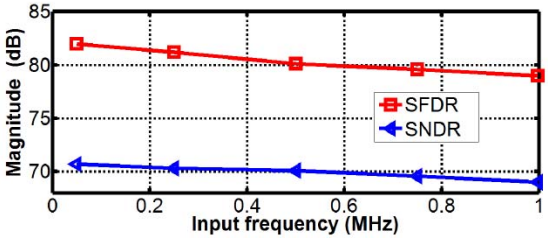

Fig. 19. SNDR and SFDR vs input frequency.

common mode generation. The master clock is generated by an Agilent 33250A signal source generator and the digital output bit-streams are collected by a MSO-4104 oscilloscope. The set-up is controlled by Labview® program in order to be processed in a workstation. Matlab® is used to compute 64 k point Kaiser-windowed FFTs of the ADC output, and hence to obtain the SNDR, SFDR performance metrics. Output spectra corresponding to three different frequencies (namely 100 kHz, 500 kHz and Nyquist frequency) are shown in Fig. 18. The SNDR and the SFDR at the Nyquist frequency are 69.3 dB and 79 dB, respectively, with no capacitor mismatch calibration. Fig. 19 shows the SNDR and SFDR versus input frequency plot. The SNDR drops by almost 2 dB with a Nyquist input compared to near DC input. The ADC achieves an effective number of bits (ENOB) of 11.2 at Nyquist frequency. The static performance of the ADC can be extracted using a variety of tests. The code density test has been employed for this ADC static performance characterization. This test involves deriving the digital output code histogram with a slowly varying ramp. The test was conducted using a full-swing (0-to-1.6 V), differential ramp. The output reconstructed ramp has a voltage range of 0-to-1.2 V, before digital scaling is applied, that signifies the accuracy of the input signal scaling. The measured DNL and INL at 2 MS/s are shown in Fig. 20, and are within 1.2/-1.0 LSB and 2.3/-2.2 LSB at 12 bits, respectively. The INL plot shows a saw-tooth characteristic at a code spacing of 128 (7 bits). As the ADC has a 6-6 BWA architecture, this characteristic manifests that top plate parasitic on the MSB-DAC and LSB-DAC are not quite balanced. Nonetheless, for the 11-bit performance, measured DNL and INL are 0.6/-0.5 LSB and 1.15/-1.1 LSB. The DNL performance at 11-bits clearly achieves the required monotonic behaviour.

Table I summarizes the measured chip performance. The prototype consumes a total power of 0.82 mW. The comparator

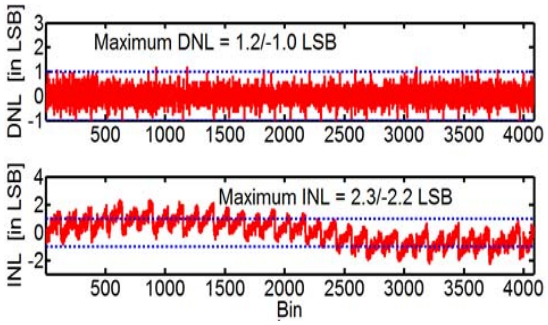

Fig. 20. Measured INL and DNL at 2MS/s.

TABLE I
MEASURED PERFORMANCE OF SAR ADC

Process		0.13-μm
Active Area(mm^2)		0.24 (0.35mm x 0.657mm)
Supply Voltage (V)		1.2/3.3
f_S(MHz)		2
Peak SFDR(dB) at 1MHz		79
Peak SNDR(dB) at 1MHz		69.3
Comparator Offset (LSB)		< 0.5
Power Consumption (mW)	Comparator and BBM	0.13
	SAR Logic	0.23
	Level Shifters	0.46

and the BBM circuit consume 0.13 mW, while the SAR logic takes 0.23 mW all operating from a 1.2 V supply. The level shifters operate at 3V and consume 0.46mW.

VII. CONCLUSIONS

To conclude this paper, Table II compares the measured performance with the designs having almost same order of resolution. One of the salient features of the proposed ADC compared to the similar architectures designed in the same process nodes ([5] and [22]), is the embedded input scaling. The chip is capable of digitizing an extended input range of 3.2 V_{pp-d}, (compared to 2 V_{pp-d} and 2.4 V_{pp-d} in previous art i.e. [5] and [27]) which corresponds to ± 1.33 times the reference voltage.

By employing the reduced number of capacitors during sampling phase, other different scaling factors can be achieved very easily making it an attractive option for the sensor based systems. The designed ADC has also shown comparable performance in terms of linearity. Architecture reported in [6] achieves a DNL of $1.08/-1$ LSB and INL of 3.79 LSB but at the cost of background calibration for capacitor mismatches and comparator offset. Similarly, architecture reported in [27] also used a background calibration for capacitor mismatches. The designed ADC does not require any capacitor calibration and can achieve a monotonic behaviour at 11-bits. Other competitive SAR ADCs are the ones reported in [28] and [29]. The former includes noise-shaping while the later uses a higher supply voltage. Performance of the designed ADC is also compared against these two architectures.

TABLE II
MEASURED PERFORMANCE AND STATE OF THE ART

Specification	[5]	[22]	[23]	[24]	[25]	[26]	[6]	[27]	[28]	[29]	**This Work**
Technology(μm)	0.13	0.13	0.18	0.065	0.040	0.18	0.04	0.065	0.13	0.35	**0.13**
Supply Voltage VDD, (V)	1.2	1	1	0.7	0.45	0.45	1	1.2	1.2	3.3	**1.2/3.3**
Data Rate (MS/s)	50	11	0.1	1e-3	0.2	0.2	6.4	50	[c.] 0.25	0.25	**2**
Input Signal Swing(V)	2 ($\pm V_{REF}$)		1 (V_{REF})	0.7 (V_{REF})	0.9	0.9		2.4 ($\pm V_{REF}$)		50	**3.2** ($\pm 1.33 V_{REF}$)
DNL (LSB)	0.91/-0.63	±0.8	[a.] ±2 .4	0.48/-0.55	0.44	<0.5	1.08/-1	0.5/-0.7		0.55	**1.2/-1.0**
INL (LSB)	1.27/-1.36	±3.0	[a.] ±2.8	0.52/-0.61	0.45	<1	3.79	1.0/-0.9		1.81	**2.3/-2.2**
Resolution	10	12	12	10	10	9	13	12	10	14	**12**
ENOB	9.18	10.1	9.4	9.1	8.95	8.27	10.35	10.9	12	13.03	**11.22**
Power (mW)	0.82	3.57	0.0038	3e-6	0.084e-3	0.94e-3	0.046	2.09	0.061	4.29	**0.9** [b.] **0.44**
FoM(fJ/conv.st)	29	311	56	5.5	0.85	22	5.5	21.9	59.5	2050	**189** [b.] **93**

[a]Extrapolated to 12 Bits. [b.] Without level shifters. [c.] Sampling Rate is 2 MS/s with an oversampling ratio of 8.

Overall, it can be concluded that the input scaling technique presented in this paper can be embedded in SAR ADCs, while achieving a performance competitive with the state of the art. The presented chip does not achieve the lowest FoM, although that was not the main design goal of this design. Instead, the main design objective and an attractive feature of the ADC circuit is the offset calculation mechanism. This technique enables a dynamic control of offset calculation over the whole operational life of the chip. All these features, together with the measured performance metrics, make the proposed ADC a suitable option for sensor A/D interfaces used for monitoring systems in a number of application scenarios.

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