Characterization of charge trapping mechanisms in GaN vertical Fin FETs under positive gate bias

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Abstract

In this paper, we present a comprehensive analysis of the charge trapping mechanisms that affect the GaN based vertical Fin FETs when the devices are submitted to positive gate bias. Devices with higher channel width show lower threshold voltage: with 2D simulations of the electron density we are able to explain the phenomenon and propose a trade-off to improve the technology. By using double pulse measurements and threshold voltage transients, two trapping/detrapping mechanisms under positive gate bias can be identified according to two voltage ranges. At low positive gate bias, electrons (previously trapped inside the oxide during the fabrication process) are detrapped toward the gate metal (mechanism 1). At higher gate bias, electrons are trapped at the GaN/oxide interface, moving the threshold towards positive values (mechanism 2). The second mechanism is observable at higher time of stress and it is predominant for higher voltages. Moreover, mechanism 2 is found to be recoverable only when the device is exposed to UV-light and electrons trapped in a specific level in the oxide acquire the energy necessary to escape and reach the n-type GaN. We demonstrate our hypothesis by calculating the interface state density in trapping/detrapping conditions by using photo-assisted Capacitance-Voltage measurements.

1. Introduction

Ideal devices for power applications should be able to manage high voltage with no current passing in OFF state and have a small on-resistance in ON state. Wide-bandgap semiconductors (SiC and GaN) are promising material candidates for the next generation of power devices. GaN power devices with lateral and vertical structures are currently studied to meet power applications needs. Commercial samples of lateral GaN power devices with operating voltage up to 650 V are available in the market [1]. Compared to the lateral structure, a vertical power device has several advantages that potentially make it suitable for power applications such electric vehicles, data centers and power grids that require high power levels (>10kW) [2]. Vertical devices reduce the die size and promise a strong reliability as the electric field peaks far away from the surface [3], and they allow an easier thermal management [4]. Several vertical GaN devices (CAVET [5][6][7], trench MOSFET [8][9][10]) have recently demonstrated to represent an excellent alternative to lateral transistors. In fact, they allow to reach high power densities (compared to lateral devices), and breakdown voltages in the kV range [11], [12]. An example of GaN device with vertical structure is the Vertical Fin Field Effect Transistor (VFET) tested in this work. The VFET is based on a multiple fin structure, where current flows vertically through nanometer-sized channels operating in parallel having a Metal-Oxide-GaN stack on the sides (see Fig. 1). GaN VFETs can reach high breakdown voltages (>1000 V) with excellent performance (0.2 $m\Omega cm^2$) [13] without the need of a p-GaN layer or epitaxial regrowth.

The aim of this paper is to give a detailed analysis of the trapping mechanisms which affect the threshold stability of GaN VFET submitted to positive gate stress. We demonstrate that: 1) the VFETs with larger channel width show lower threshold voltage due to a parasitic current formed at the center of the channel layer. 2) When the devices are submitted to a positive bias, a moderate negative shift in threshold voltage is observed for low gate voltages; by increasing the gate bias, the threshold voltage shift becomes positive. 3) Two different processes are induced at different gate

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bias, one responsible for negative threshold voltage shift (detrapping of electrons from the Al_2O_3 to the metal), the other responsible for positive threshold voltage shift (injection of electrons from the channel to the gate insulator). Both these mechanisms are independent on channel width.
4) The second mechanism is predominant for larger stress time of stress and high gate voltages and a fully recovery is observed only when the devices are submitted to UV-light. 5) In order to quantify the interface states responsible of positive threshold voltage shift under positive gate bias, we carried out photo-assisted capacitance-voltage measurements. 2D simulations are used to support the interpretation of the experimental data.

2. Device and measurement setup description

2.1. Vertical GaN fin FET

The pictorial cross section of a single fin of the GaN VFET is reported in Figure 1. By increasing the gate bias, electrons accumulate at the Al_2O_3-GaN interfaces, forming conduction channels. The epitaxial layers, grown on a 2-inch GaN substrate by IQE, consist of 8-µm-thick n-GaN channel and n^--GaN drift layer doped $2\times10^{16}cm^{-3}$, and 0.3-µm-thick n^+-GaN layer. 15nm-Al_2O_3 layer was deposited by ALD (Atomic layer deposition) using H_2O and TMA (Trimethylaluminium) at 250 C as gate dielectric on smooth vertical sidewalls obtained by using a combined dry-wet etching technique [14]. At V_{GS} = 0 V, two depletion regions induced by the two surfaces of the fin are created due to the work function difference between the gate metal and GaN, if the channel (fin) width is tight enough (below 500 nm), the depletion regions merge inducing a normally-off transistor operation. In Figure 2 we report the threshold voltages calculated for different devices. The devices with larger channel width show lower threshold voltage. From the simulation of the electron density at the turn-on for different channel width (Figure 3) we observe that at V_{GS}=0.5 V the electron density located at the center of the fin remains nearly constant by increasing the fin width; on the other hand, the electron density accumulated at the interface is higher for narrower channel widths. The choice of fin width can significantly impact threshold voltage. A more positive Vth can be obtained by decreasing the channel width.

3. Results

3.1. Double Pulse

In Figure 4 double-pulse I_DV_G is reported for several quiescent bias points in the off-state with $V_{DS,Q}$ = 0 V and $V_{GS,Q}$ from 0 V to 5 V. A square-wave driving waveform was used, with 5 ms off-time and 5 µs on-time. That is, the devices were biased in off-state condition (trapping condition) for 5 ms and then the gate and the drain terminals were synchronously pulsed in measurement condition (V_{DS} = 2 V) for 5 µs.

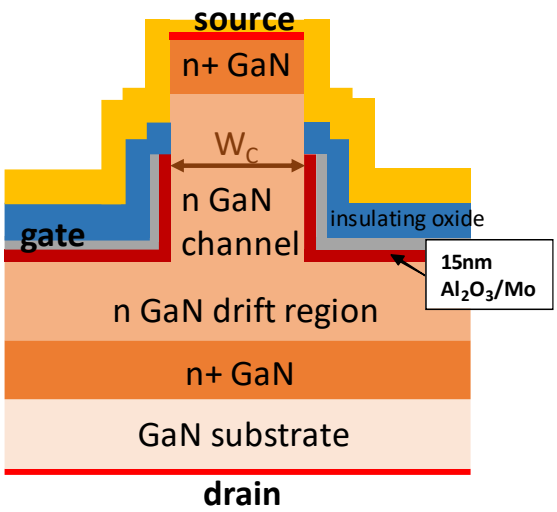

Fig. 1. Pictorial figure of the 2D structure of one fin of the GaN VFET under test: for V_{GS}=0 V the device is in off condition, hence the electron density in the channel is low and the maximum is located in the center of the n-GaN region far from the interfaces. At V_{GS}>1 V the electron density peaks at the Al_2O_3/GaN interfaces. A difference in threshold voltage is observed between devices with different channel width.

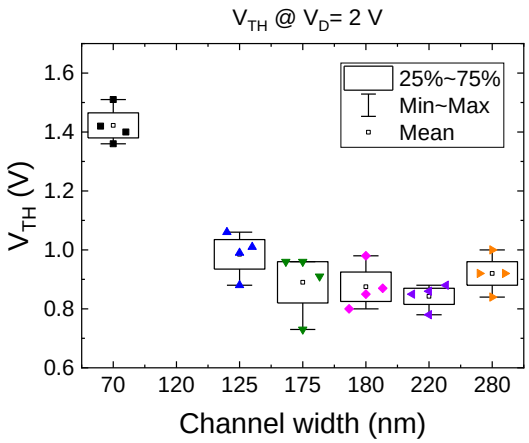

Fig. 2. Plot of threshold voltages calculated for devices with different channel width: the devices with higher channel width show lower threshold voltage.

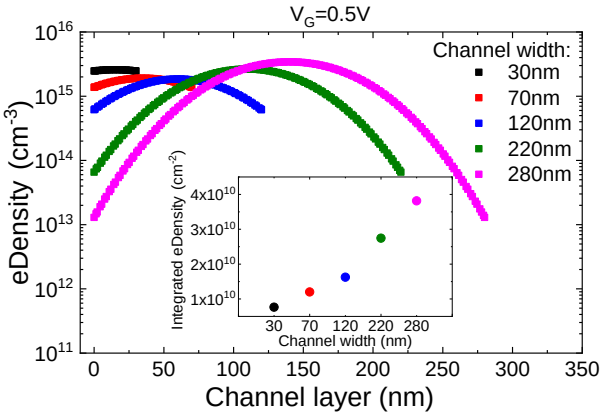

Fig. 3. Simulation of electron density in the channel layer for different channel width. For V_{GS}=0.5 V (subthreshold) the device with lower channel width shows the same value of electron density at the center and at interface, by increasing the channel width the electron density at the interface is decreasing by almost 2 decades.In the inset is reported the integral of the charge as a function of fin width.

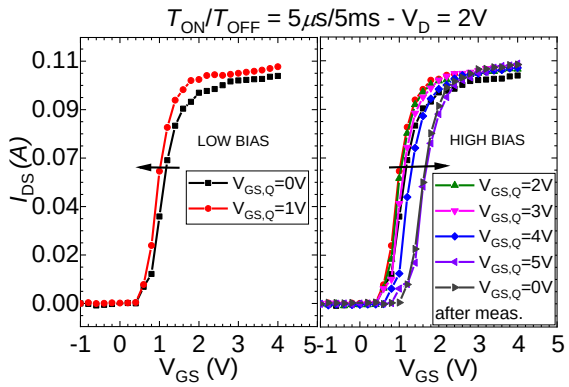

Fig. 4. Pulsed I_DV_G performed at different $V_{GS,Q}$. For $V_{GS,Q}$ < 2 V (left) a negative shift of the threshold voltage is observed, higher gate bias induces a positive shift of the threshold voltage (right).

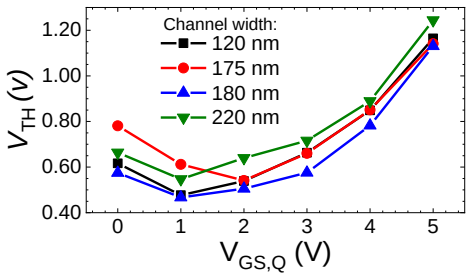

Fig. 5. Plot of the shift of the threshold voltage for different $V_{GS,Q}$. The same trend (negative shift at low gate bias and positive shift at higher gate bias) is observed for devices with different channel width.

Two mechanisms have been observed: trapping conditions at low gate bias (Figure 4 (left)) induce negative shift of the threshold voltage (mechanism 1), for high gate bias a positive shift of the threshold voltage is observed (mechanism 2), which is not recoverable (Figure 4 (right)). The instability of the threshold voltage when the device is submitted to positive gate bias is not dependent on the geometry of devices, as reported in Figure 5.

3.2. Vth transients

We investigate the trapping kinetics by monitoring the threshold voltage during a trapping phase at different trapping voltages, $V_{G,BIAS}$ (0 V, 1 V, 2 V, 3 V, 4 V, 5 V). In the V_{TH} transients measurement experiment the gate is kept under positive bias with $V_S = V_D = 0$ V, for a variable trapping period Δt and I_DV_G measurements are performed at the end of each period of trapping. The trapping period Δt is increased at each step from 10 μs up to 100 s.

The V_{TH} transients during the trapping phase are reported in Figure 6.

The V_{TH} transients measurements confirm what previously observed in the double pulse characterization: two mechanisms are induced at different gate bias, one responsible for negative threshold voltage shift (mechanism 1), the other responsible for positive threshold voltage shift (mechanism 2). Moreover, the second mechanism takes place for higher time of stress and it is predominant for higher gate bias.

In order to evaluate the kinetics of detrapping we subjected the device to the same procedure in recovery conditions ($V_{G,BIAS}$ = 0 V).

From the results reported in Figure 7 (left), we observe that the device is not able to recover in 100s of recovery phase. The slight positive shift of the threshold voltage observed after tens of second is probably due to the repeated I_DV_G performed up to 5V for 10 us. In Figure 7 (right) we report the results of the same measurement performed with the device submitted to UV-light (LED with peak wavelength at 365nm): the recovery is completed achieved.

On the basis of experimental results we formulate the following hypothesis: when the GaN Vertical Fin FET is submitted to positive gate bias two mechanisms occur at different gate voltage ranges (Figure 8 (a)). At low gate voltage a slight negative shift of the threshold voltage is observed, due to detrapping of electrons from the oxide; at high gate voltage the injection of electrons from the channel to the gate dilectric interface induces a positive shift of the threshold voltage. This shift is not recoverable in dark condition, but under UV-light the electrons trapped at

the GaN/Al_2O_3 interface and in the gate insulator are able to be detrapped thanks to the additional energy given by the light (Figure 8 (b)). The same recovery is not observed by using LEDs at longer wavelengths: we can suppose that electrons are trapped at a specific energy level at the interface between GaN and Al_2O_3. When the device is exposed to UV-light, the electrons are detrapped and can proceed towards the GaN layer through hopping [15][16], thus being collected at the semiconductor side and contribute to the conductive channel and the turn ON. Another possibility is that the recovery is hole-assisted, since the UV-light exposure could lead to the creation of electron-hole pairs inside the GaN. The holes accumulate at the interface GaN/Al_2O_3 and/or reduce the trapped electron density.

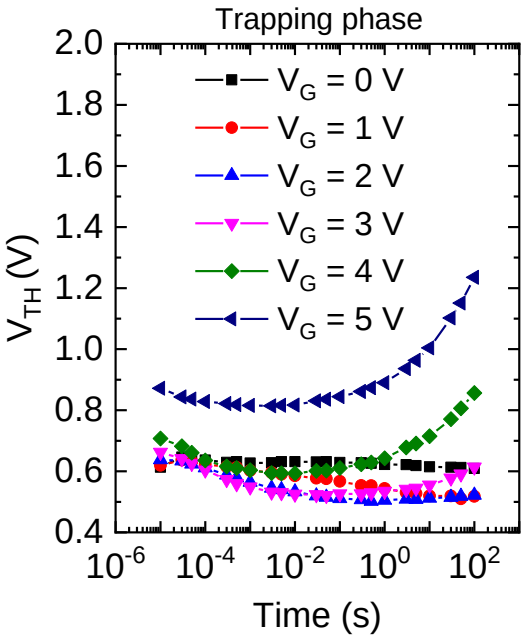

Fig. 6. Plot of the threshold voltage transient performed by increasing the time of bias at each point from 10us to 100s. For stress time < 1 s the negative shift is predominant, for higher time of stress the second mechanism occurs (trapping of electrons) and we observe a positive shift of the threshold voltage. This second mechanism occurs earlier for high gate voltage.

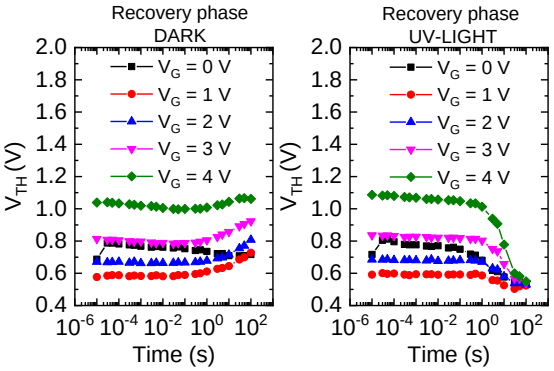

Fig. 7. Plot of the threshold voltage transient during the recovery phase after 100s of trapping phase (each point is obtained after biasing the device with all terminals grounded for an increasing period). No recovery is observed if the phase is performed in dark condition (left). When the device is submitted to UV-light (right) a complete recovery is achieved.

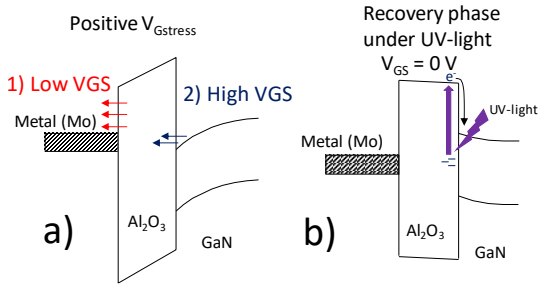

Fig. 8. (a) Pictorial representation of the trapping/detrapping mechanisms with positive gate bias: when a low positive gate bias is applied electrons (previously trapped inside the oxide during the fabrication process) are detrapped toward the gate metal (mechanism 1). At higher gate bias, electrons are trapped at the GaN/oxide interface moving the threshold towards positive values (mechanism 2). (b) Pictorial view of the effect of UV-light on the device at 0V after a period of positive gate voltage stress: under UV-light electrons can be detrapped from oxide traps either by hopping either by recombination with holes generated by band-to-band under UV-exposure.

3.3. Photoassisted C-V characterization of trap states

In order to quantify the interface states responsible of the instability of the threshold voltage in Vertical Fin FETs, we evaluate the changes in the gate-source capacitance as a function of voltage in trapping and de-trapping conditions [17]. The procedure of the measurement is depicted in Figure 9: 1) the device is biased in OFF-state for 10 s, then it is exposed to UV-light for 50 s in order to detrap all the electrons and set the device in a ideal condition. The device is kept in OFF-state for 2000 s to in order to make free holes leave the system and eliminate variations in capacitance. 2) Without breaking the bias, a

capacitance measurement was performed by sweeping the gate voltage from -3 V to 5 V. 3) At this point, the device remains biased at 5 V for 1000 s in order to induce the injection of electrons in the trap states at Al_2O_3/GaN interface. 4) Then a back capacitance-voltage was performed from 5 V to -3 V. The two capacitance-voltage curves are plotted in Figure 10 (a). The C-V curve performed after biasing the device in accumulation (at 5 V) shifts the threshold towards more positive values, in good agreement with the previous results. The C-V curve performed after UV-exposure in OFF-state moves the threshold to the left, and we observe a change in the slope at the turn-on. The Figure 10 (b) shows the two curves superimposed: the difference in voltage at a constant capacitance between the ideal C-V curve and the trapping one is proportional to the amount of interface state charge that changed occupancy below the Fermi level. The fixed charge within the oxide is responsible of the rigid shift in the C-V curves.
We calculate analytically the interface state density from:

$$D_{it} = \frac{C_{ox}}{qA}\left(\frac{d\Delta V}{d\psi_s}\right)$$

Where q is the electron charge, ΔV is the voltage difference between the ideal and the trapping C-V curve, ψ_s is the interface potential and it depends on the doping concentration N_d (2×10^{16}cm^{-3}) as follows:

$$\psi_s = \frac{q\varepsilon_s\varepsilon_0 N_d A^2}{2C_{sc}^2}$$

Where ε_s and ε_0 are the relative permittivity of GaN and vacuum, respectively. A is the area of the metal-oxide-GaN stack taken as the sum of the two rectangular areas of metal-oxide that form the capacitor with the channel layer, multiplied for the number of ribbons. C_{sc} is the depletion capacitance.
In Figure 10 (c) the plot of the interface state density as a function of the interface potential is reported. By comparing the state density with the applied voltage (blue dots) we obtain that when the device is submitted to low voltage ($V_G < 1.5\ V$), the traps states are traps for holes. When the device is at 2 V the density of interface states is $4 \cdot 10^{13} cm^{-2} eV^{-1}$ and the states behave as traps for electrons.

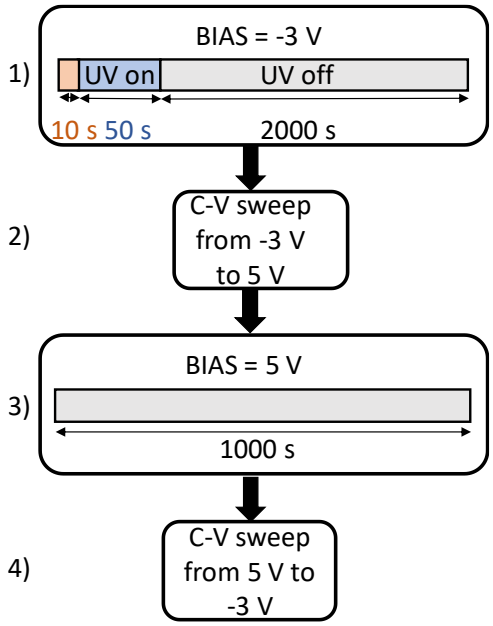

Fig. 9. Schematic representation of the procedure to obtain C-V plots in trapped and detrappped conditions.

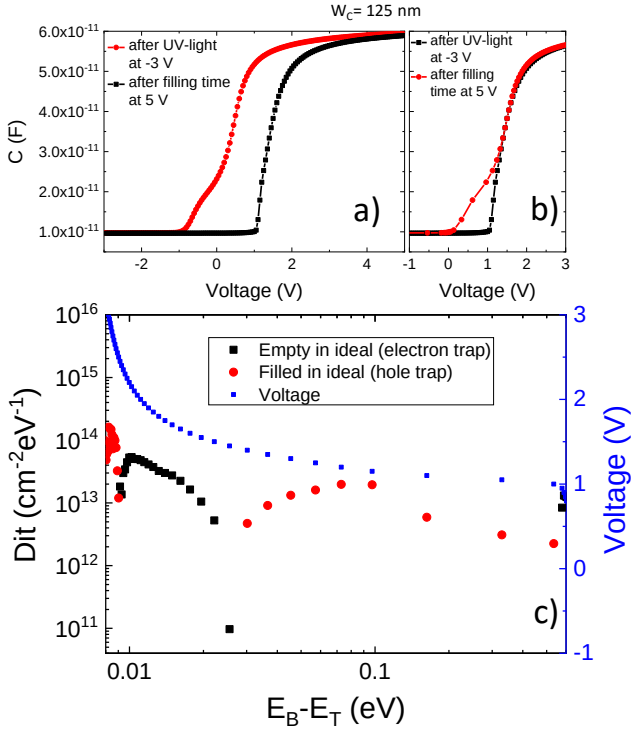

Fig. 10. (a) Plot of the Capacitance Gate-Source of a 125nm device performed from -3 V to 5 V after lighting up the device with UV-light (red curve) and from 5 V to -3 V after biasing the device at 5 V in dark condition for 1000s. (b) The post-UV curve is shown fitted and translated to the dark curve. (c) Plot of the interface state density as a function of the interface potential compared with the applied voltage (blue dots).

4. Conclusion

In conclusion, an extensive analysis was carried out on GaN Vertical Fin FETs. With a DC characterization supported by simulations we were able to identify the causes of the difference in the threshold voltage for devices with different channel width. With double pulse analysis, Vth transients and photoassisted C-V we obtained the following original results: (i) when the devices are submitted to positive gate bias two mechanisms occur depending on gate voltage range; at low gate bias electrons are detrapped from the gate dielectric causing a slight negative shift of the threshold voltage (mechanism 1), at high gate bias electrons are injected from the GaN to the dielectric interface inducing a positive shift of the threshold voltage (mechanism 2). (ii) The second mechanism is recoverable only when the device is exposed to UV-light suggesting the presence of a specific trapping level. (iii) We report a peak interface state density of $4 \cdot 10^{13} cm^{-2} eV^{-1}$ at V_G = 2 V by using photoassisted capacitance voltage procedure.

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