IEEE Access
Multidisciplinary | Rapid Review | Open Access Journal

Received February 14, 2019, accepted March 17, 2019, date of publication March 25, 2019, date of current version April 9, 2019.

Digital Object Identifier 10.1109/ACCESS.2019.2907151

Simulation Perspectives of Sub-1V Single-Supply Z^2-FET 1T-DRAM Cells for Low-Power

CARLOS NAVARRO[1], CARLOS MARQUEZ[1], SANTIAGO NAVARRO[1], CARMEN LOZANO[1], SEHYUN KWON[2,3], YONG-TAE KIM[2], AND FRANCISCO GAMIZ[1], (Senior Member, IEEE)

[1]Departamento de Electrónica y Tecnología de Computadores, University of Granada, 18071 Granada, Spain
[2]Korean Institute of Science and Technology, Seoul 02792, South Korea
[3]Division of Materials Science and Engineering, Hanyang University, Seoul 04763, South Korea

Corresponding author: Carlos Navarro (carlosnm@ugr.es)

This work was supported in part by the H2020 REMINDER European under Grant 687931, and in part by the Spanish under Project TEC2017-89800-R and Project IJCI-2016-27711.

ABSTRACT With the upcoming Internet of Things (IoT), low-power devices are becoming mainstream these days. The need for memory elements able to operate at reduced biasing conditions is therefore of utmost importance. In this paper, one of the most promising capacitor-less dynamic RAM cell, the Z^2-FET (zero subthreshold swings, zero impact ionization field-effect transistor), is analyzed through advanced numerical simulations to study its sub-1V operation capabilities. SiGe compounds and tuned workfunction are selected to further reduce the operating voltage to limit energy consumption. The results demonstrate functional SiGe cells with up to 75% energy reduction with respect to identical Si cells.

INDEX TERMS 1T-DRAM, capacitor-less, FD-SOI, germanium, memory, low-power, p-i-n diode, single supply, silicon, TCAD, workfunction, Z^2-FET.

I. INTRODUCTION

The irruption of the IoT (Internet of Things) era is driving nano-electronics towards ultra-low power and more efficient circuits [1]. As smart devices and embedded systems become commonplace, the need to moderate the energy consumption grows in importance, being essential in ubiquitous circuits such as memories. The research of innovative storing elements alternatives satisfying high-reliability, low-cost and easy co-integration while minimizing the energy consumption is therefore crucial. One of the potential solutions are the capacitor-less cells, analogous to traditional DRAM cells where the external capacitor is suppressed [2].

Among the available 1-Transistor capacitor-less (1T-DRAM) candidates, the Z^2-FET [3], [4] is the sole one not relying on degrading high-voltage programming mechanisms as impact ionization [5] or band-to-band tunneling [6], [7] and thus the optimum candidate to implement low power operation memory cells. The first and simpler challenge is to move from the default dual-supply (positive and negative biases [8], [9]) to single supply (only positive voltages) configuration. From a designer point of view, this simplification represents an advantage over other capacitor-less DRAM cells that require positive and negative biases simultaneously [2], [5]. The second goal is to reduce the biasing conditions to decrease the power consumption. In order to fulfill both objectives, back-gate bias, body doping tuning, lower band-gap materials as germanium [10] and tuned metal gates can be explored. In this work, the gate workfunction and silicon-germanium alloys are investigated via advanced 2D-TCAD simulations. The main expected drawback when moving to Ge compounds is the reduced potential well to accumulate holes as observed in other reduced band-gap semiconductors [7]. This issue is however not critical as long as the Ge concentration is not excessively high since the band-gap difference is less than 0.2 eV at 50% Ge [11].

The associate editor coordinating the review of this manuscript and approving it for publication was Tae Hyoung Kim.

II. Z^2-FET BASICS AS CAPACITOR-LESS DRAM CELL

The Z^2-FET is a band-modulated diode able to present two well-differentiated conductivity regions [12], [13]. Under low gates biasing and/or high anode voltage the device exhibits the typical p-i-n diode behavior (Fig. 1a). However, with a sufficiently high front-gate (positive) and back-gate (negative) biasing, an additional gate-induced virtual p-n junction (Fig. 1b) blocks the carrier normal diffusion from anode and cathode. The current is then very low until the anode voltage exceeds a given value, known as ON voltage (V_{ON}).

2169-3536 © 2019 IEEE. Translations and content mining are permitted for academic research only.
Personal use is also permitted, but republication/redistribution requires IEEE permission.
See http://www.ieee.org/publications_standards/publications/rights/index.html for more information.

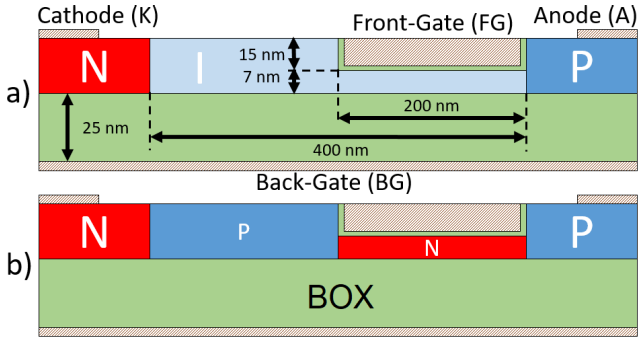

FIGURE 1. Simplified SOI Z²-FET cell structure a) without and b) with gate-induced virtual doping regions. The intrinsic region changes to an additional p-n junction (induced by the back-/front-gate, respectively). The substrate below the BOX insulator layer is not illustrated.

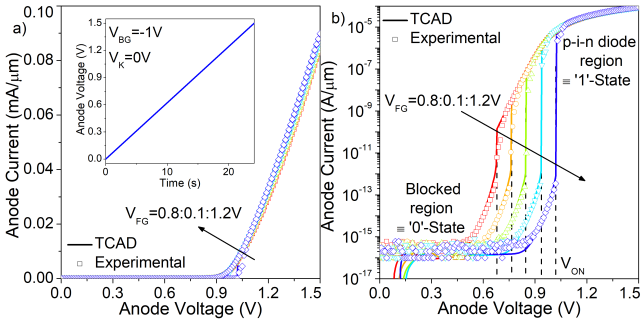

FIGURE 2. Silicon Z²-FET cells TCAD results vs. experimental $I_A(V_A)$ results in a) linear and b) logarithmic scale. The applied anode bias pattern (inset in a) consists on a rising signal from 0 to 1.5 V with 24.16 s ramping time. Default parameters with $W = 100\ \mu m$, $L_G = L_{In} = 200$ nm, $V_K = 0$ V and $V_{BG} = -1$ V. 0% Ge and $T = 300$ K.

Once V_{ON} is overcome, the current abruptly changes from one regime to the other enabling ultra steep switching slopes (Fig. 2). Since V_{ON} is sensitive to the stored charge under the front-gate (thanks to the floating body effect, FBE [14]) that screens the top-gate induced barrier, it is possible to operate the Z²-FET as dynamic memory cell thanks to the body charge transient modulation [12]: the logic '0'-state is defined while in the low-conductivity region ($V_A < V_{ON}$) and the logic '1'-state once the device has switched on ($V_A > V_{ON}$).

III. Z²-FET STRUCTURE AND SIMULATION SETUP

The Z²-FET cell consists of a double-gate FD (fully depleted) SOI p-i-n diode. The whole active semiconductor layer, including side terminals, is made of SiGe where different mole fractions are considered. While the bottom gate lies below the SOI and BOX layers, the top gate partially masks the intrinsic semiconductor section allowing to define two characteristic lengths: the top gated length, L_G, and the intrinsic (ungated) distance, L_{In}. The ultra-thin semiconductor thickness is typically $t_S \simeq 7$ nm whereas a 15 nm epitaxy along the ungated and anode/cathode (A/K) regions leads to $\simeq 22$ nm thick active layer. Below, a buried SiO_2 insulator layer, with $t_{BOX} \simeq 25$ nm, is present. The side electrodes, anode and cathode (A/K), are highly doped ($N_A \approx N_K > 10^{21}$ cm^{-3} p/n-type, respectively). The intrinsic zone is residually p-type doped with $N_{SOI} = 10^{16}$ cm^{-3}. The substrate ground-plane (not shown in the simplified structure depicted in Fig. 1), $N_{Sub} \approx 10^{18}$ cm^{-3}, acts as back-gate (BG) terminal effectively ending the electric field lines. Finally, the front-gate (FG) stack is formed by a $\simeq 3$ nm high-k multi-layer structure, SiO_2/HfO_2, capped with TiN ($\simeq 4.7$ eV workfunction).

Regarding the simulation setup [15], Poisson's, charge continuity and density gradient (to implement the spatial quantization in the ultra-thin semiconductor film [16], [17]) equations are considered for electrons and holes. Other included models and parameters are SRH (Shockley-Read-Hall) recombination/generation, band-to-band tunneling [18] and several mobility models (doping dependence, high field velocity saturation, transverse electric field with remote-Coulomb scattering, and thin-layer). Additional details about the Z²-FET basics and simulation features can be found in [12], [13].

With the aim of validating the simulation data, DC $I_A(V_A)$ switching characteristics were experimentally characterized from moderately wide silicon Z²-FETs. These DC results were used to later fit a 2D simulation deck as in [12], [19]. The carrier lifetime ($\tau_n = 2.5 \cdot 10^{-8}$ s and $\tau_p = 10^{-8}$ s) and series resistance ($R_{A/K} = 400\ \Omega \cdot \mu m$) were used to match the data. Figure 2 illustrates, on the one hand, the characteristic Z²-FET sharp current onset at $V_A = V_{ON}$ and, on the other hand, the curve fitting with the experimental results demonstrating an exceptional agreement.

IV. RESULTS

A. STATIC DC CHARACTERISTICS

Since the memory biasing conditions are closely related to the static V_{ON}, this metric is used to monitor and study possible scenarios for ultra-low operating voltages. Figure 3 illustrates the ON voltage dependence with several parameters in SiGe cells. Fig. 3a shows that employing a 50% Ge in the Z²-FET automatically reduces V_{ON} over 300 mV (from 0.845 to 0.515 mV) enabling reduced V_A operation. The lower Ge energy band-gap reduces the anode-body energy barrier (Fig. 3b). Decreasing V_{FG} too much prevents the possibility of obtaining the low-current '0'-state, Fig. 3c. On the other hand, for this particular cell (dimension and architecture) the back-gate voltage does not strongly impacts the V_{ON} due to the limited ground-plane electrostatic control, hence it can be left grounded as long as the steep switch still occurs, Fig. 3d. Finally, the p-type body doping also affects the ON voltage location due to the energy barrier enhancement along the ungated region: larger body doping require larger anode voltages to induce carriers to overcome the energy barriers and trigger the device (not shown). This parameter might be tuned in order to achieve sharp switching characteristics at given gate biasing conditions. Fortunately, in this case the Z²-FET exhibits abrupt switching at grounded back-bias and no doping tuning is required. The interplay

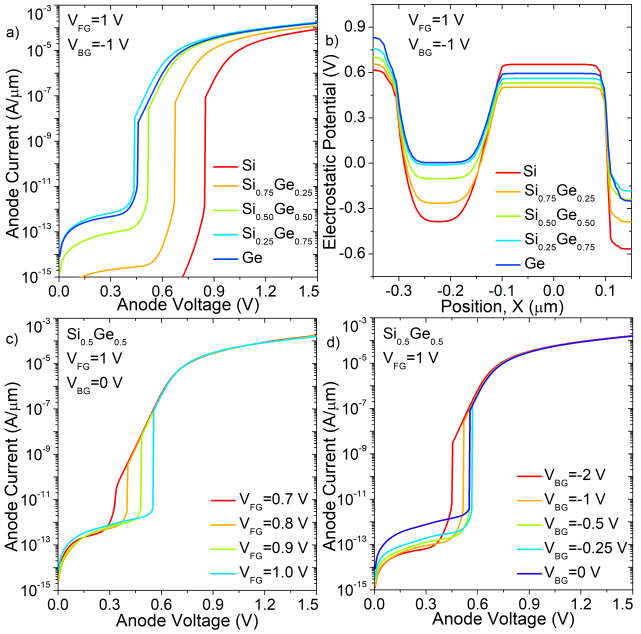

FIGURE 3. Simulated static DC anode current characteristics as a function of the anode voltage, $I_A(V_A)$, for distinct a) Ge concentrations (b) detail of the horizontal electrostatic potential cuts 3.5 nm above BOX layer with $V_{FG} = 1$ V and $V_{BG} = -1$ V and $V_A = V_K = 0$ V), c) front-gate voltage and d) back-gate biases. Default parameters with $W = 100$ μm, $L_G = L_{In} = 200$ nm, $V_K = 0$ V and $T = 300$ K.

between all these parameters potentially provides functional Z^2-FETs at reduced biasing conditions without sacrificing too much performance.

B. TRANSIENT MEMORY OPERATION

Figure 4a depicts the test bias pattern employed to analyze the memory response. It consists of a W_0-R-W_1-R pattern where the maximum anode (both for programming the '1'-state and reading) and front-gate (holding and reading) voltages, V_A and V_{FG}, are gradually reduced. The timing conditions are close to those demonstrated in experimental results [8], [9] although faster operation is possible as reported via TCAD simulations [12]. Meanwhile, the transient memory performance (current levels, margin and ratio) is monitored for several SiGe Z^2-FET cells to validate the low-bias operation. Different anode current readouts are illustrated in Fig. 4b,c corresponding to distinct cells and biasing scenarios. For example, Fig. 4b shows the transient response to a high bias pattern ($V_A = V_{FG} = 1$ V) where both cells show functional memory operation (Si: $I_1 = 5.4$ μA/μm and $I_0 \simeq 0.9$ pA/μm; SiGe: $I_1 = 22.7$ μA/μm and $I_0 \simeq 0.2$ nA/μm). The silicon cell shows lower currents due to the enhanced barriers and lower mobility [10] but improved off state levels. If the anode voltage is reduced down to $V_A = 0.7$ V (Fig. 4c), the silicon cell still shows memory operation but the current levels are strongly reduced significantly hardening the logic state discrimination (Si: $I_1 = 0.2$ nA/μm and $I_0 \simeq 17$ fA/μm; SiGe: $I_1 = 10.7$ μA/μm and $I_0 \simeq 0.1$ nA/μm). The '1'-state, '0'-state and current ratio at $V_{FG} = 1$ V are

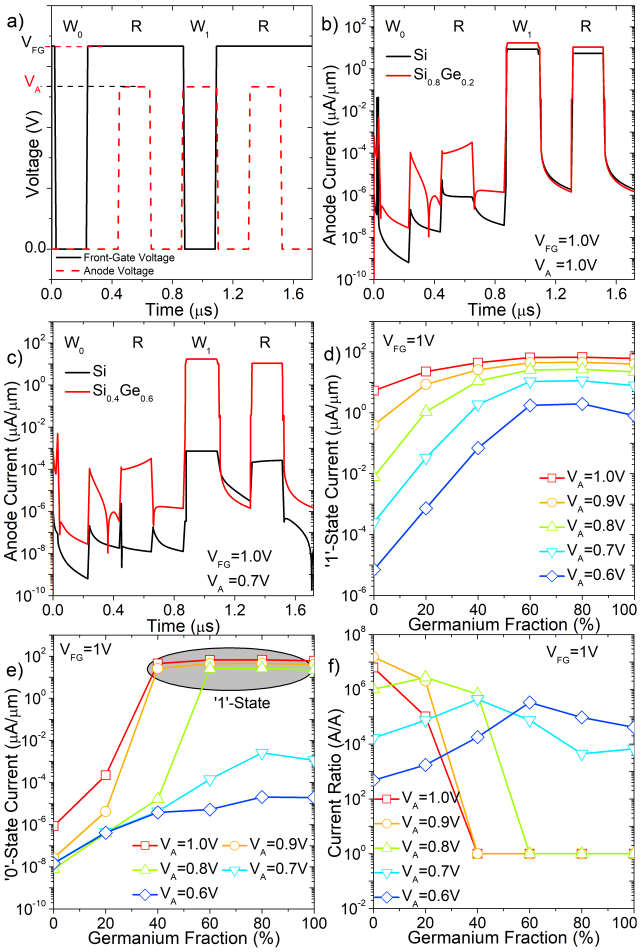

FIGURE 4. a) Transient bias pattern to test the memory behavior. The maximum anode, V_A, and front-gate, V_{FG}, voltages are not fixed to analyze the sub-1V operation for low-power applications. Anode current readout for different cells at b) $V_A = V_{FG} = 1$ V and c) $V_{FG} = 1.0$ and $V_A = 0.7$ V. d) '1'-state, I_1, e) '0'-state, I_0, and f) current ratio, I_1/I_0, as a function of the Ge fraction at $V_{FG} = 1$ V. $V_{BG} = V_K = 0$ V and $T = 300$ K.

depicted in Fig. 4d-f where, depending on the application, the optimum SiGe cell can be targeted. Figure 4d shows that increasing the Ge fraction enhances the current (due to the barrier lowering, Fig. 3b). At 60% Ge it saturates as observed for the ON voltage in Fig. 3a. The '0'-state current shows that, at high Ge fractions, if V_A is also high the '0'-state turns into a '1'-state, hence the current ratio drops to one. The key takeaway is that SiGe compounds are more suitable for low anode biasing memory scenarios.

The following step is to reduce the front-gate voltage below 1V. Given that the gate current is almost negligible, the impact on the power consumption will be marginal but it is required to operate the cell using a single low-voltage supply. Since V_{FG} is still necessary to induce the energy barrier and achieve the '0'-state, the front-gate bias cannot be strongly reduced. Figure 5a,b illustrates the transient memory operation at $V_A = 0.7V$: Si cells do not drive enough current while SiGe cells only show valid memory operation at $V_{FG} \simeq 1V$. In order to further downscale V_{FG}, the front-gate metal work-function is reduced from $\Phi_{FG} = 4.7$ eV, close to mid-gap,

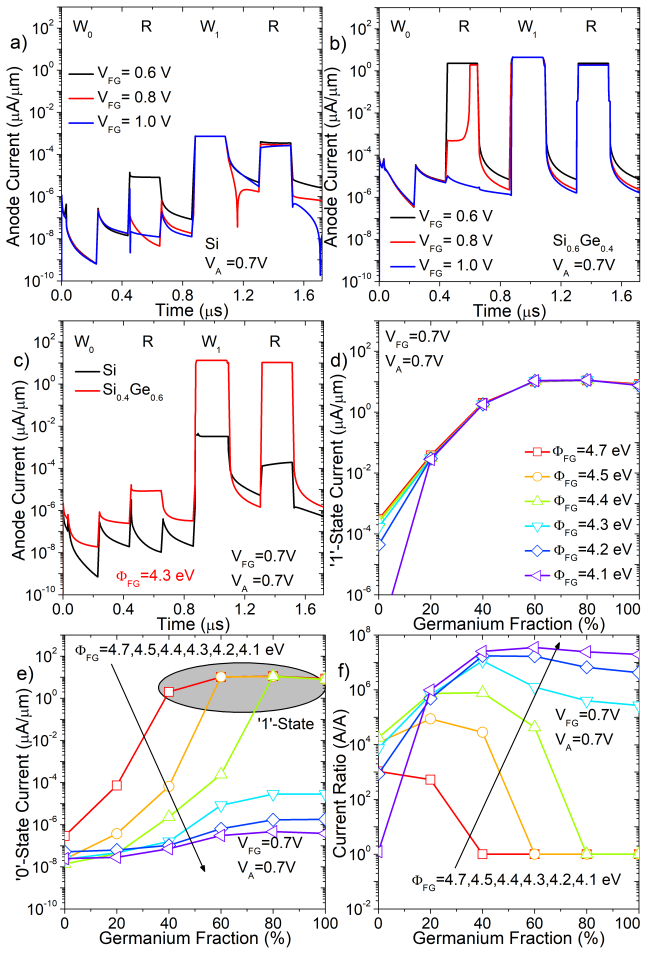

FIGURE 5. Anode current readout for different cells at $V_A = 0.7$ V and distinct V_{FG} for a) Si and b) $Si_{0.6}Ge_{0.4}$ cells. c) Anode current readout at $V_{FG} = V_A = 0.7$ V with $\Phi_{FG} = 4.3$ eV. d) '1'-state, e) '0'-state and f) current ratio as a function of the top-gate workfunction for the SiGe cell in c). $V_{BG} = V_K = 0$ V and $T = 300$ K.

down to 4.1 eV, close to the silicon conduction band. These workfunction values can be tuned through Ti and Ni compounds (see for example [20]). The transient memory operations at $\Phi_{FG} = 4.3$ eV for Si and $Si_{0.4}Ge_{0.6}$ are shown in Fig. 5c. By reducing the top-gate workfunction, the required V_{FG} is relaxed and the memory operation in SiGe compounds is possible with reasonable states current levels (Si: $I_1 = 0.2$ nA/μm and $I_0 \simeq 51$ fA/μm; SiGe: $I_1 = 10.6$ μA/μm and $I_0 \simeq 8.4$ pA/μm). It is worth noting that, in contrast with n-MOSFETs where the off-state current is severely degraded when decreasing the workfunction, Z²-FETs are not affected thanks to the steep subthreshold slope. The top-gate workfunction impact on the current levels and ratio are illustrated in Fig. 5d-f at $V_A = V_{FG} = 0.7$ V. Since the impact of the front-gate bias is screened when the carrier density is high underneath the gate insulator (corresponding to the '1'-state) only the '0'-state is modulated with Φ_{FG}. A top-gate workfunction of 4.3 eV and 40-60% Ge seems to optimize the current ratio with reasonable I_1, Fig. 5d,f. The optimum Ge concentration and biasing conditions will depend on the targeted application. Limiting the

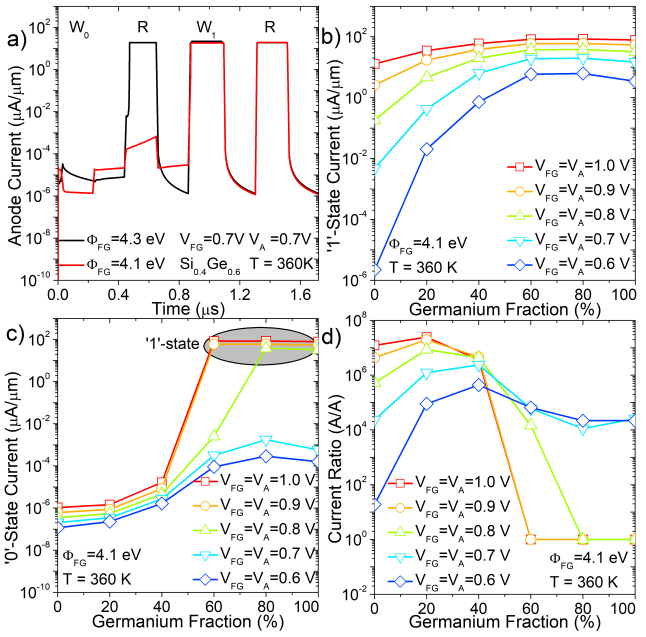

FIGURE 6. a) Anode current readout for identical cells at $V_{FG} = V_A = 0.7$ and $T = 360$ K and different workfunctions. b) '1'-state, c) '0'-state and d) current ratio as a function of the maximum supply voltage (V_{FG} and V_A) for the SiGe cell in a). $V_{BG} = V_K = 0$ V.

gate workfunction is therefore an effective and simple method to reduce the front-gate voltage in Z²-FET devices.

C. TEMPERATURE IMPACT

Due to the energy gain, carriers are more easily injected when rising the temperature [21]. This effectively reduces the ON voltage and induces the logic-state swap from the '0'-state to the '1'-state which prevents the memory operation. In order to solve this problem, the V_{FG} can be increased but this goes against the goal of this work. The alternative is then to further reduce Φ_{FG}. Figure 6a shows additional simulations at high temperature (360 K, typical test temperature for memories) demonstrating that $\Phi_{FG} = 4.3$ eV is not enough to maintain the '0'-state (it turns into the '1'-state) and at least $\Phi_{FG} = 4.1$ eV is required to avoid increasing V_{FG}. The current levels and ratio are depicted in Fig. 6b-d. Note that due to the strong diode current dependence on temperature, the logic levels, especially for the '1'-state, have increased significantly (80% for the $Si_{0.4}Ge_{0.6}$ cell at $V_{FG} = V_A = 0.7$ V). It can also be observed that $\Phi_{FG} = 4.1$ eV is not enough for large anode biasing ($V_A \geq 0.8$) and high Ge concentration due to the larger anode currents in these cells. Nevertheless, SiGe compounds enable low voltage supplies even at elevated temperatures.

V. ENERGY CONSUMPTION COMPARISON

The cell energy consumption is now analyzed. The static consumption is essentially zero due to the grounded anode terminal and negligible anode and gate currents during holding. On the other hand, the dynamic consumption is extracted, by averaging the writing or reading energy between both logic states with $E \simeq \Sigma I \cdot V \cdot t$ (E: energy; I: each terminal

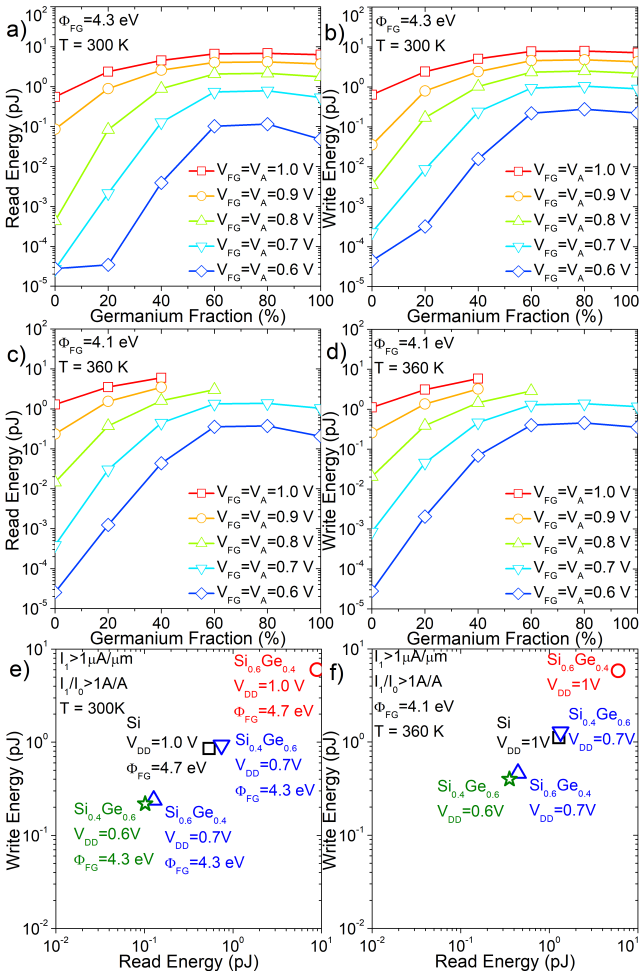

FIGURE 7. a,c) Read and b,d) write energy as a function of the Ge concentration for different voltage supplies at a,b) room (300 K) and c,d) high (360 K) temperature. Only cells with $I_R > 1$ A/A are illustrated. Energy consumption comparison at e) room and f) high temperature for some representative cells satisfying $I_1 > 1$ μA/μm and $I_R > 1$ A/A. $V_{BG} = V_K = 0$ V. 200 ns pulse widths (as in Fig. 4a) are assumed to calculate the energy.

current extracted at mid pulse; V: each terminal bias; t: pulse width), and compared for different SiGe concentrations at room (300 K) and high temperature (360 K), Fig. 7a-d. The reading and writing energies are always in the same order of magnitude. The larger anode currents at 360 K induce the systematic energy increase with respect to room temperature. Due to the high current ratio in the Z^2-FET, the '1'-state is responsible of over 95% of the wasted energy. Figure 7e,f illustrates the energy of some cells satisfying $I_1 > 1$ μA/μm and $I_R > 1$ A/A at both temperatures. Si cells are rapidly degraded when reducing the biasing conditions and only exhibit high current levels at high voltages. SiGe cells drive more current at similar biasing (Fig. 4b), hence present larger power consumption. At reduced biasing conditions and gate workfunction, SiGe cells show different behaviors: i) 40% Ge cells benefit from the lower current and voltage enabling reduced energy consumption of only 24%/28% (up to 75% saving at 300 K) when reading/programming; and ii) 60% Ge cells show similar consumption but enhance current levels (with respect to Si cell with $\Phi_{FG} = 4.7$ eV and $V_{FG} = V_A = 1.0$ V). In any case, limited supply-voltage range and minimum 30%/15% saving can be achieved at identical current levels thanks to the bias reduction from 1.0 V down to 0.7 V. The achieved power consumption values are below those found in advanced DRAM cells of 1-4 pJ/bit. Further reduction is possible if moving to $V_{FG} = V_A = 0.6$ V or, by fixing the '1'-state anode programming voltage to a lower value as 0.5 V [22]. However, sub-0.5 V operation is challenging due to the reduced driven anode current: although moving to alternative materials, featuring lower band-gap, seems feasible, the CMOS fabrication flow integration would not be possible preventing its interest. Thanks to the pulsed memory operation and the reduced biasing-conditions, no drastic self-heating effect is expected to arise in these cells.

VI. CONCLUSION

The logic current levels are limited in silicon Z^2-FET memory cells when downscaling the anode bias. This issue prevents their application for ultra-low voltage memory cells. The use of silicon-germanium compounds and modified front-gate metal workfunctions enables valid memory operation below 1 V (all terminals comprised) and reasonable current levels for low-power applications even at high temperatures. These single-supply biasing schemes strongly simplify the design and reduce the power consumption. The final energy saving depends on the application requirement and the reading/writing rates. However a minimum saving of 30% and 15% when reading/programming, respectively, is guaranteed at similar anode currents with 0.7 V supply, although the bias can be even further reduced down to 0.6 V. This makes the promising Z^2-FET 1T-DRAM more suitable (or the sole available option) for low-power IoT devices and embedded systems with respect to other memory alternatives even when typically featuring a larger footprint.

REFERENCES

[1] M. A. M. Albreem *et al.*, "Green Internet of Things (IoT): An overview," *Proc. IEEE 4th Int. Conf. Smart Instrum., Meas. Appl. (ICSIMA)*, Putrajaya, Malaysia, Nov. 2017, pp. 1–6. doi: 10.1109/ICSIMA.2017.8312021.

[2] H.-J. Wann and C. Hu, "A capacitorless DRAM cell on SOI substrate," in *IEDM Tech. Dig.*, Washington, DC, USA, Dec. 1993, pp. 635–663. doi: 10.1109/IEDM.1993.347280.

[3] J. Wan, C. Le Royer, A. Zaslavsky, and S. Cristoloveanu, "A compact capacitor-less high-speed DRAM using field effect-controlled charge regeneration," *IEEE Electron Device Lett.*, vol. 33, no. 2, pp. 179–181, Feb. 2012. doi: 10.1109/LED.2011.2176908.

[4] A. Z. Badwan, Z. Chbili, Y. Yang, A. A. Salman, Q. Li, and D. E. Ioannou, "SOI field-effect diode DRAM cell: Design and operation," *IEEE Electron Device Lett.*, vol. 34, no. 8, pp. 1002–1004, Aug. 2013. doi: 10.1109/LED.2013.2265552.

[5] S. Okhonin, M. Nagoga, J. M. Sallese, and P. Fazan, "A SOI capacitor-less 1T-DRAM concept," in *Proc. IEEE Int. SOI Conf.*, Durango, CO, USA, Oct. 2001, pp. 153–154. doi: 10.1109/SOIC.2001.958032.

[6] N. Rodriguez, C. Navarro, F. Gamiz, F. Andrieu, O. Faynot, and S. Cristoloveanu, "Experimental demonstration of capacitorless A2RAM cells on silicon-on-insulator," *IEEE Electron Device Lett.*, vol. 33, no. 12, pp. 1717–1719, Dec. 2012. doi: 10.1109/LED.2012.2221074.

[7] C. Navarro *et al.*, "InGaAs Capacitor-Less DRAM Cells TCAD Demonstration," *IEEE J. Electron Devices Soc.*, vol. 6, pp. 884–892, 2018. doi: 10.1109/JEDS.2018.2859233.

[8] S. Navarro *et al.*, "Experimental demonstration of operational Z^2-FET memory matrix," *IEEE Electron Device Lett.*, vol. 39, no. 5, pp. 660–663, Mar. 2018. doi: 10.1109/LED.2018.2819801.
[9] S. Navarro *et al.*, "Evaluation of thin-oxide Z^2-FET DRAM cell," *Solid-State Electron.*, to be published. [Online]. Available: https://www.sciencedirect.com/science/article/pii/S0038110119301510?via%3Dihub. doi: 10.1016/j.sse.2019.03.040.
[10] B. G. Streetman and S. Banerjee, *Solid State Electronic Devices*, 5th ed. Upper Saddle River, NJ, USA: Prentice-Hall, 2000.
[11] M. E. Levinshtein, S. L. Rumyantsev, and M. S. Shur, *Properties of Advanced Semiconductor Materials: GaN, A1N, InN, BN, SiC, SiGe*. Hoboken, NJ, USA: Wiley, 2001.
[12] C. Navarro *et al.*, "Extended analysis of the Z^2-FET: Operation as capacitor-less eDRAM," *IEEE Trans. Electron Devices*, vol. 64, no. 12, pp. 4486–4491, Sep. 2017. doi: 10.1109/TED.2017.2751141.
[13] S. Cristoloveanu *et al.*, "A review of the Z^2-FET 1T-DRAM memory: Operation mechanisms and key parameters," *Solid-State Electron.*, vol. 38, pp. 10–19, May 2018. doi: 10.1016/j.sse.2017.11.012.
[14] J.-P. Colinge, *Silicon-on-Insulator Technology: Materials to VLSI*. New York, NY, USA: Springer, 2004. doi: 10.1007/978-1-4419-9106-5.
[15] *Sentaurus Device User Guide (N-2017.09)*, Synopsys Inc., Mountain View, CA, USA, 2017.
[16] M. G. Ancona and H. F. Tiersten, "Macroscopic physics of the silicon inversion layer," *Phys. Rev. B, Condens. Matter*, vol. 35, no. 15, pp. 7959–7965, 1987. doi: 10.1103/PhysRevB.35.7959.
[17] M. G. Ancona and G. J. Iafrate, "Quantum correction to the equation of state of an electron gas in a semiconductor," *Phys. Rev. B, Condens. Matter*, vol. 39, no. 13, pp. 9536–9540, 1989. doi: 10.1103/PhysRevB.39.9536.
[18] K.-H. Kao, A. S. Verhulst, W. G. Vandenberghe, B. Sorée, G. Groeseneken, and K. De Meyer, "Direct and indirect band-to-band tunneling in germanium-based TFETs," *IEEE Trans. Electron Devices*, vol. 59, no. 2, pp. 292–301, Feb. 2012. doi: 10.1109/TED.2011.2175228.
[19] C. Navarro *et al.*, "Z^2-FET as capacitor-less eDRAM cell for high-density integration," *IEEE Trans. Electron Devices*, vol. 64, no. 12, pp. 4904–4909, Dec. 2017. doi: 10.1109/TED.2017.2759308.
[20] I. Polishchuk, P. Ranade, T.-J. King, and C. Hu, "Dual work function metal gate CMOS technology using metal interdiffusion," *IEEE Electron Device Lett.*, vol. 22, no. 9, pp. 444–446, Sep. 2001. doi: 10.1109/55.944334.
[21] H. El Dirani, Y. Solaro, P. Fonteneau, P. Ferrari, and S. Cristoloveanu, "Properties and mechanisms of Z^2-FET at variable temperature," *Solid-State Electron.*, vol. 115, pp. 201–206, Jan. 2016. doi: 10.1016/j.sse.2015.08.015.
[22] M. S. Parihar *et al.*, "Low-power Z^2-FET capacitorless 1T-DRAM," in *Proc. IEEE Int. Memory Workshop (IMW)*, May 2017, pp. 1–4. doi: 10.1109/IMW.2017.7939093.

CARLOS NAVARRO received the Ph.D. degrees in electrical engineering from the University of Granada, Granada, Spain, in 2014, and the Institute of Microelectronics, Electromagnetism and Photonics, Grenoble, France, in 2015. He is currently a Postdoctoral Researcher with the University of Granada. He has authored or co-authored over 70 journal articles and conference abstracts. His research interests include SOI devices and capacitor-less memory cells.

CARLOS MARQUEZ received the M.Sc. degree in telecommunication engineering, the M.S. degree in electrical engineering, and the Ph.D. degree in electronics from the University of Granada, Granada, Spain, in 2012, 2014, and 2017, respectively, where he is currently a Postdoctoral Researcher. He is the author or coauthor of 11 peer reviewed international journal articles, two book chapters, and 12 conference proceedings. His research interests include the electrical characterization of semiconductor devices, MOSFET front-end-of the line (FEOL) reliability, one-transistor dynamic-random access-memory cells (1T-DRAM), and two dimensional (2D) materials.

SANTIAGO NAVARRO was born in Granada, Spain, in 1984. He received the B.Sc. degree from the University of Granada, in 2011, and the M.Sc. degree from the University of Seville, in 2013. He is currently pursuing the Ph.D. degree in electronics engineering with the University of Granada. His research interests include SOI devices and 1T-DRAM cells.

CARMEN LOZANO received the B.Sc. degree in electronic industrial engineering from the University of Granada, Spain, in 2017, where she is currently pursuing the Ph.D. degree with the Nanoelectronic Research Group. Her research interest includes the characterization of semiconductors and devices.

SEHYUN KWON received the B.Sc. degree from Hanyang University in Materials Science and Engineering, in 2016. He is currently pursuing the Ph.D. degree with Hanyang University and the Korean Institute of Science and Technology. His research interest includes capacitor-less 1T-DRAM memory cells.

YONG-TAE KIM received the Ph.D. degree from KAIST. Since 1982, he has been with the Semiconductor Materials and Device Laboratory, KAIST/KIST (Korean Institute of Science and Technology), as a Principal Scientist, the Outstanding Scientist, and a Professor with Korea University and Hanyang University. He had served as the General Director of the National R & D Program for commercialization of nano process and materials, Ministry of Industry. He holds 61 patents and has published 295 papers related to emerging memory and compound semiconductor devices.

FRANCISCO GAMIZ received the B.S. degree (Hons.) (Best Student Award) in physics and the Ph.D. degree (Hons.) (Best Student Award) from the University of Granada, in 1991 and 1994, respectively.

Since 2005, he has been the Full Professor of electronics, and since 2008, he has been the Head of the Nanoelectronics and Graphene Research Labs. He has co-authored more than 350 refereed papers in major journal and international conference proceedings, several book chapters, and he is the Co-Holder of several international patents related to multi-body 1T-DRAM.