CLOCK GATING ASSERTION CHECK: AN APPROACH TOWARDS EFFICIENT VERIFICATION CLOSURE ON CLOCK GATING FUNCTIONALITY

by

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ACL2	A Computational Logic for Application Common Lisp
ASIC	Application Specific Integrated Circuit
BFM	Bus Functional Model
CDI	Clock Domain Information
CEC	Clock Enable Control
CGAC	Clock Gating Assertion Check
CMOS	Complementary metal–oxide–semiconductor
CPU	Central Processing Unit
CRG	Clock and Reset Generator
DPI	Direct Programming Interface
DUT	Design Under Test
EDA	Electronic Design Automation
FPGA	Field Programmable Gate Array
HDL	Hardware Description Language
IC	Integrated Circuit
LRM	Language Reference Manual

NMOS	N-type metal-oxide-semiconductor
OOP	Object Orientated Programming
OVM	Open Verification Methodology
PIC	Programmable Interrupt Controller
PMOS	P-type metal-oxide-semiconductor
PNR	Pseudo Netlist Representation
RAM	Random Access Memory
RTL	Register Transfer Level
SIP	Soft Intellectual Property
SLN	Sequential Logic Network
STG	State Transition Graph

SEMAKAN PENEGASAN 'CLOCK GATING': SATU PENDEKATAN KE ARAH PENUTUPAN PENGESAHAN YANG BERKESAN UNTUK FUNGSI 'CLOCK GATING'

ABSTRAK

Salah satu teknik pengurangan kuasa yang digunakan secara meluas dalam Peringkat Daftar Pemindahan (PDP) peringkat reka bentuk adalah 'clock gating'. Walau bagaimanapun, penambahan logik 'clock gating' telah meningkatkan kerumitan reka bentuk dan usaha pengesahan yang lebih besar diperlukan. Kaedah pengesahan konvensional digunakan secara meluas yang merupakan mekanisme papan memeriksa dalam Kaedah Pengesahan Terbuka (OVM). Sebagai tambahan, terdapat beberapa kaedah yang dicadangkan dahulu seperti penggunaan benih induk yang sama dalam pelbagai simulasi, RTL kepada ACL2 translasi dan pengesahan masa sekatan jam. Akan tetapi, kaedah-kaedah yang dicadangkan dahulu masih tidak mempunyai keupayaan untuk benar-benar memastikan ketepatan logik 'clock gating' dalam reka bentuk. Kaedah pengesahan yang dicadangkan, yang dipanggil Semakan 'clock gating' (CGAC) bertujuan menangani kelemahan kaedah pengesahan konvensional. Kaedah ini adalah bebas daripada persekitaran pengesahan yang digunakan di bangku ujian. Selain itu, kaedah yang dicadangkan juga bertujuan untuk mencapai pengesahan yang lebih cepat terhadap logik 'clock gating' dalam reka bentuk dengan usaha yang minimum. Kaedah yang dicadangkan adalah aliran automatik yang mengambil dua input utama iaitu kod yang ditulis dalam Bahasa Penerangan Reka Bentuk (BPRB) dalam peringkat PDP dan 'clock domain' maklumat

reka bentuk. Dengan menggunakan input utama, kaedah yang dicadangkan menjana semakan ‘clock gating’. Kaedah yang dicadangkan digunakan pada dua reka bentuk untuk mengesahkan ‘clock gating’ reka bentuk-reka bentuk yang tersebut. Butiran mengenai pelaksanaan kaedah yang dicadangkan terkandung dalam tesis ini. Dengan menggunakan kaedah ini, sebanyak lima kesalahan ‘clock gating’ ditemui dan analisis kesan kesalahan tersebut dibincangkan. Kaedah yang dicadangkan meningkatkan keberkesanan masa yang digunakan untk pengesahan ‘clock gating’ sebanyak 87.5% dan 75% masing-masing untuk kedua-dua reka bentuk yang digunakan berbanding dengan kaedah OVM. Namun begitu, terdapat beberapa had dalam kaedah yang dicadangkan iaitu kaedah ini digunakan di Intel, maklumat reka bentuk yang digunakan tidak boleh didedahkan dan reka bentuk tidak dikawal oleh penulis. Kesimpulannya, kaedah yang dicadangkan terbukti berkesan dalam memastikan pelaksanaan ‘clock gating’ yang betul dalam reka bentuk.

CLOCK GATING ASSERTION CHECK: AN APPROACH TOWARDS EFFICIENT VERIFICATION CLOSURE ON CLOCK GATING FUNCTIONALITY

ABSTRACT

One of the power reduction techniques widely used in Register Transfer Level (RTL) stage of a design is clock gating. However, the addition of clock gating logics has increased the complexity of a design and therefore considerable amount of verification effort is required. The conventional verification method used widely is the scoreboard checking mechanism in Open Verification Methodology (OVM) verification environment. In addition, there are several methods proposed over the years to solve the verification of clock gating logics, for example, same master seed usage in multiple simulations, RTL to ACL2 translation and gated clock timing verification. However, the previous proposed methods still lack the capability to completely comprehend the checking of the correctness of clock gating logics of a design. The proposed verification method, called Clock Gating Assertion Check (CGAC) is aimed at addressing the limitation of the conventional verification method. The method is independent of verification environment used in a test bench. Besides, the proposed method is also aiming at achieving an efficient pre-silicon verification closure on clock gating logics with minimum verification effort. The proposed method is an automated flow that takes in two main inputs, namely codes written in Hardware Description Language (HDL) in RTL stage and clock domains information of a design. By using the main inputs, the proposed method generates assertion checks at possible clock gating boundary conditions. The clock gating logics of two Soft Intellectual

Property (SIP) designs were verified using the CGAC method. The details of the implementation of the method are discussed in this thesis. By using the method, a total of five clock gating bugs were found and analysis on the impacts of the bugs is discussed. The proposed method further improved the efficiency of clock gating functional verification by 87.5% and 75% in terms of verification time spent in weeks for the first and second design respectively compared to the conventional method used which is OVM. However, there are a few limitations in the proposed method whereby it is used within Intel, the design information cannot be disclosed in this thesis and the designs are not within the author's control. As a conclusion, based on the results obtained, it is concluded that the proposed method is proven effective in ensuring the correct clock gating implementation in a design.

CHAPTER ONE

INTRODUCTION

1.1 Background

During the early days of Integrated Circuits (IC) development, performance, area, cost and reliability of the IC were the primary concerns while power management was not given its due importance (Sharma and Kaur, 2014). However, with the emerging demands for portable and computation devices such as smart phones and tablets which require fast performance and complex functions, power saving is becoming a major concern during IC development (Dhanotiya and Sharma, 2014). Therefore, there is a need to reduce power dissipation in battery operated devices in order to achieve longer battery lifetime and reasonable battery weight. While the motivation to reduce power dissipation in non-battery operated devices such as workstations is driven by system cost and long term reliability of the devices (Thakur and Kumar, 2014).

In order to tackle power dissipation issue in current design circuitry, a number of power management methods have been introduced. One of the mostly used power management methods nowadays is clock gating method since clock component contributed to 70% of total dynamic power of a design (Wimer and Albahari, 2014). Clock gating method in general can be used in either Register Transfer Level (RTL) and/or integrated clock gating cells insertion at design synthesis stage to reduce power usage by reducing the switching activity in a design circuitry when the chip is in the idle condition.

Currently, there are a number of methods proposed on reducing power dissipation in RTL by using clock gating implementation and the benefits had been

widely known and published. Among others, clock gating implementation in a communication system managed to reduce total power by 68.27% under 20MHz and 200MHz clock frequencies (Sahni et al., 2015) while clock gating usage in Serial Peripheral Interface (SPI) managed to reduce power consumption from 12.4mW to 4.9mW (Kaur and Sharma, 2015). Besides, clock gating usage in the design of Fast Fourier Transform managed to reduce power consumption up to 25% (Sarada and Vigneswaran, 2016).

In terms of verification, currently pre-silicon verification is used to verify clock gating functionality in a design. Logics simulations are conducted on a hardware design implemented in RTL stage to ensure the correctness and behavior of the design using commercial logic simulators like VCS by Synopsys or ModelSim by Mentor Graphics. Even though it is possible to simulate the behavior of the system accurately using a RTL model, it often took numerous amount of cycles, in the range of hundreds or thousands of cycles to detect finely detailed errors for a fairly complex design (Bertacco, 2011).

Usually, Open Verification Methodology (OVM) is widely chosen as the verification methodology used to verify the functionality of a design (Poikela et al., 2012) (Šimková et al., 2012) (Oliveira et al., 2012), coupled with commercial logic simulators. Conventionally, the most common clock gating verification method adopted in the industry currently is by developing test cases from test plans written based on the architecture of a design. The test cases developed are compliant to the common verification methodology used in the industry nowadays, which is OVM. Functional simulation is then performed using the test cases and a test bench developed with an OVM Scoreboard. OVM Scoreboard is developed for checking purposes as shown in the test bench in **Figure 1.1**. OVM Scoreboard is a checking mechanism in

OVM verification environment whereby it checks for end to end transactions in a design (Glasser, 2009). However, this method considers a Design Under Test (DUT) as a black box unit and only checks for the correct behavior of the interface signals, which does not have insight on the internal logics of a design, including clock gating logics.

In **Figure 1.1**, OVM Bus Functional Model (BFM) at point ① acts as the generator to generate stimulus to the DUT through interface at point ①. While OVM BFM which acts as the responder is responsible to respond to the transactions at point ② that result from the stimulus generated at point ①. OVM Scoreboard is checking for transactions at point ① and point ② by comparing the transactions with a reference set of pre-determined expected results (Glasser, 2009) to determine if the DUT is functioning correctly. Based on the OVM Scoreboard architecture described, OVM Scoreboard does not know the micro-architectural details of the design. Therefore, using OVM Scoreboard to verify clock gating logics implemented in micro-architectural level of a design is inadequate and incomplete since OVM Scoreboard does not have insight on the micro-architectural details of a design, including clock gating logics. Furthermore, implementation of an OVM Scoreboard is based on design specifications, the linearity of the data flow of a design, the existence of a golden reference model and OVM Scoreboard developer's depth of knowledge on the architectural details of the design (Brown, 1996).

Although there is a significant number of known previous works on power management techniques using clock gating method (Soni and Hiradhar, 2015) (Huda et al., 2009) (Shaker and Bayoumi, 2013), ironically, there had not been much works or researches done to validate the correctness of the clock gating logics implemented in a design. Therefore, the method proposed in this thesis is aiming at presenting an

efficient, effective and time-saving method to verify the correctness of the implementation of clock gating logics in RTL, which is arguably one of the widely used power management techniques in the semiconductor industries nowadays.

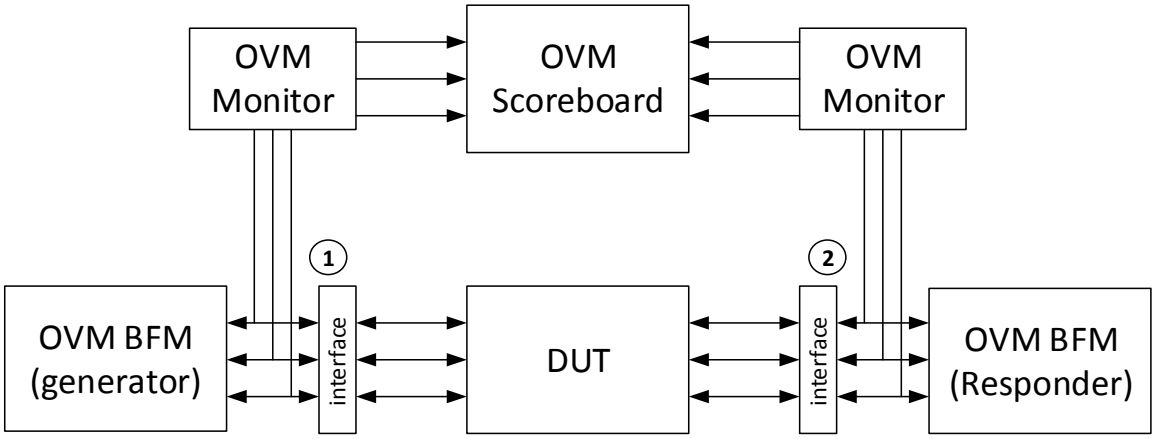

Figure 1.1. Top level block diagram of a test bench developed using OVM.

1.2 Problem Statements

The research in this thesis is centered on the theory of clock gating implementation should not affect the functionalities of a design. Therefore, any additional clock gating logics in a design must be verified besides ensuring the correct functionalities of a design (Ahuja and Shukla, 2009). However, the functional verification effort to validate clock gating logics in design is becoming more complicated as two main objectives are needed to achieve concurrently, which are functionality of the design and clock gating functionality correctness. The task of functionality verification is further burdened by the fact there is a trend of increasing corner cases to be verified due to the increasing amount of the gate counts over the years. The validation effort needed in terms of engineering years and the amount of simulation vectors needed to validate a design is increasing with the increasing amount of logic gates (Spirakis, 2004). Furthermore, up to 70% of the time and resources of a design cycle are spent on functional verification (Fine and Ziv, 2003) which means functional verification is the critical path in a product development. Without any automated or faster approach to verify clock gating functionalities, this task will take a very long period of time to complete.

Among previous works done on verifying clock gating functionalities including timing verification done on a controller design circuitry containing memory elements in a gated clock domain (Kawarabayashi et al., 1993). This method requires the usage of state transition graph (STG) extracted from the net list of the controller in order to perform timing verification on different operations of a controller circuitry. This method requires a design to be synthesized into net list before verification can be performed. Therefore, in the event of any violations found during

verification in net list stage, the design synthesis flow will need to be rerun again which is time-consuming.

Another method is the translation of RTL codes into ACL2 (A Computational Logic for Application Common Lisp) to perform formal verification (Seidel, 2011). This method translates gated clock signal into a common clock signal during the translation of RTL into ACL2. This approach does not provide a complete solution to verify the functionalities of clock gating logics, since gated clock signal is translated into a common clock signal and does not verify the condition to gate or un-gate a gated clock.

Furthermore, another clock gating verification method presented by Habermann which utilizes the same master seed to run two different simulations with two different dynamic clock gating configurations (Habermann et al., 2012). Traces from the two simulations are printed out in two different files of which comparison between the two files is made. This method introduces more validation effort since two simulations are needed in order to produce traces to be compared.

In addition, the checking mechanism using OVM Scoreboard still has many dependencies and often requires changes during the course of a design cycle. Furthermore, in the event of the OVM Scoreboard developer misses any critical design or architecture changes, the checking mechanism using OVM Scoreboard is no longer correct and will result in false positive results on functional simulations performed. This approach will likely cause many RTL bugs to be missed if this method is used solely in clock gating verification and assertion checks implementation is able to solve this shortcoming (Nordstrom, 2013).

1.3 Research Objectives

There are 3 main objectives to be achieved in this research, which are:

1. To develop an efficient clock gating RTL bug detection method in clock gating functional verification of a chip design towards achieving efficient verification closure on clock gating functionality in terms of the time spent in clock gating verification.
2. To develop a method in clock gating verification in pre-silicon verification stage that is resilient to functional verification methodology used, which is OVM.
3. To propose an automated method which will be able to identify all corner cases of clock gating logics in a design of in a very short duration, which is within one minute. In this thesis the size of the two designs used is roughly 500k and 70k logic gates respectively.

1.4 Research Scope

The scope of this research is on clock gating logics functional verification at RTL, which is the front end design stage of a chip design cycle. This research is focusing on developing a verification tool in the pre-silicon verification stage of a design. The test cases used are specifically meant to verify the clock gating logics of the designs. However, there are two external limitations in this research as listed below:

- The designs used in this research are intellectual properties of Intel Corporation and cannot be disclosed in this thesis.
- The designs used are not under the author's control.

1.5 Research Contributions

This research will be able to provide another faster, automated and efficient method to verify clock gating functionality in RTL and thus achieving faster closure in clock gating functional verification. The proposed method will be able to provide alternative solution in conventional functional verification practices besides complementing limitations in existing verification methodology used, which is OVM.

1.6 Thesis Outline

There are a total of five chapters in this thesis, Chapter 2 consists of literature review on the background and theories behind power dissipation, which is then followed by one of the most common power management methods used currently in RTL – clock gating method. Besides, literature review also includes previous methods done in order to verify clock gating functionality in a design and conventional clock gating functional verification method commonly adopted in the industry nowadays. It is followed by the research method proposed in chapter 3, including the flow chart of the method and the details on how RTL codes written in Hardware Description Language (HDL) are being converted into assertion checks. In chapter 4, the experiment setup, results and discussions from using the proposed method to verify clock gating functionality on Soft Intellectual Property (SIP) are discussed. This thesis is then ended with conclusions and potential future works to be performed in chapter 5.

CHAPTER TWO

LITERATURE REVIEW

2.1 Introduction

The theory of power dissipation in a design circuitry is being discussed in this chapter followed by the power management method used widely in RTL which is clock gating implementation. Clock gating method is mainly used to reduce switching activity in a design during when it is in idle condition, and therefore achieving power saving objective in a design. Understanding power dissipation theory and the concept of clock gating method are very important whereby the method proposed is aiming at verifying clock gating implementation in a design to ensure its functionality correctness. Besides, this chapter also investigates three methods previously done by other researchers in verifying clock gating functionality as well as common clock gating functional verification practice adopted in the semiconductor industry nowadays.

2.2 Power Management

Understanding components that contribute to power dissipation will eventually lead to better power management strategy during the definition and design phases of an IC development. Currently, there are a number of methods used to reduce power dissipation in a design. In this section, brief introduction on power dissipation and power management strategy adopted in RTL are being investigated and discussed since the method proposed in this thesis is aiming at verifying the clock gating functionality correctness in RTL.