# PREDICTION OF ELECTROSTATIC DISCHARGE SOFT ERROR ON TWO-WAY RADIO USING SIMULATION AND IMMUNITY SCANNING TECHNIQUE

**ROSNAH ANTONG**

**UNIVERSITI SAINS MALAYSIA**

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**by**

**ROSNAH ANTONG**

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"In the name of Allah, most Gracious, most Compassionate"

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# LIST OF ABBREVIATIONS

| | |
|---|---|
| A/m | Ampere per meter |
| A/m | Ampere per meter |
| API | Amber Precision Instruments |
| BGA | Ball Grid Array |
| CDM | Charged Device Method |
| CLK | Clock |
| CMOS | Complementary Metal − Oxide Semiconductor |
| CST MWS | Computing Simulation Technology Microwave Studio |
| DUT | Device under Test |
| DFM | Design for Manufacturing |
| ECAD | Electronic Computer−Aided Design |
| EEPROM | Electrically Erasable Programmable |
| E-field | Electric Field |
| EM | Electromagnetic |
| EMC | Electromagnetic Compatibility (Ability of device to function in its electro magnetic environment without introducing disturbance to that environment or to other device) |
| EMI | Electromagnetic Interference |
| EMF | Electromagnetic Force |
| ESD | Electrostatic Discharge |
| ESDA | Electrostatic Discharge Association |
| ESDS | Electrostatic Discharge Sensitive |
| FCB | Flexible Circuit Board |
| FDTD | Finite−Differences Time-Domain |

| | |
|---|---|
| FIT | Finite Integration Technique |
| Flex | Flexible Printed Circuit |
| FR4 | Flame Resistant 4 (a glass fiber epoxy laminate) |
| GCAI | Global Communication Accessory Interface |
| GND | Ground |
| GPU | Graphics Processing Unit |
| GRP | Ground Reference Plan |
| GTL | Gunning Transistor Logic |
| HBM | Human Body Method |
| HCP | Horizontal Coupling Plane |
| H-field | Magnetic Field |
| IBIS | Input/Output Buffer Information Specification |
| IC | Integrated Circuit |
| IEC 61000−4−2 | International Electrotechnical Commission (Part 4−2 Testing and Measurement techniques − Electrostatic discharge immunity test) |
| JEDEC | Joint Electron Device Engineering Council |
| kV | Kilovolt |
| LED | Light−emitting diode |
| MIC | Microphone |
| $\mu$ | Micron |
| MM | Machine method |
| mm | Millimeter |
| ns | Nanosecond |
| ODB++ | Open Database (CAD−to−CAM data exchange format used for electronic database of printed circuit board manufacturing) |
| PBA | Perfect Boundary Approximation |

| | |
|---|---|
| PCB | Printed Circuit Board |
| pF | Pico farads |
| PN | P−N type junction |
| ProE | Pro Engineer |
| ps | Picoseconds |
| RLC | Resistor, Inductor and Capacitor |
| SDRAM | Synchronous dynamic random−access memory |
| SPKR | Speaker |
| T | Tesla |
| TTL | Transistor−Transistor Logic |
| TLP | Transmission Line Pulse |
| ULC | Ultra Low Cost |
| V | Volt |
| V/m | Voltage per meter |
| VCP | Vertical Coupling Plan |

# RAMALAN RALAT ANJAL NYAHCAS ELEKTROSTATIK RADIO DUA HALA MENGGUNAKAN SIMULASI DAN TEKNIK PENGIMBASAN IMUNITI

## ABSTRAK

Nyahcas elektrostatik (ESD) merupakan faktor utama kepada kegagalan dan kerosakan radio komunikasi dua hala. Kegagalan ralat anjal seperti kegagalan logik, selak-atas atau tersalah set boleh berlaku disebabkan ESD secara berlebihan. Secara umumnya diketahui bahawa peranti-peranti Semikonduktor Pelengkap Oksida-Logam (CMOS) amat terdedah kepada ESD. Kegagalan CMOS yang disebabkan oleh ESD boleh juga menyebabkan radio dua hala ditetapkan semula atau berhenti berfungsi sepenuhnya. Lazimnya, kegagalan ini hanya boleh diketahui selepas radio dipasang and diuji. Melalui kajian ini, satu kaedah baru telah dicipta untuk menguji risiko ESD pada peringkat litar radio. Vektor Poynting digunapakai untuk mengira kuasa yang diterima oleh litar bersepadu semasa berlakunya ESD. Melalui kaedah ini, radio dua hala telah dimodel secara 3-dimensi menggunakan piawaian IEC 61000-4-2. Model ini dapat memberikan satu gambaran mengenai penyebaran arus ESD di dalam Papan Litar Tercetak (PCB) dan satah bumi. Kuasa purata berpemberat masa $(S_{twa})$ yang dikira melalui produk silang di antara medan-E dan medan-H diguna secara meluas dalam permodelan, hasilnya nilai had maksimum sebanyak 3.7 $W/m^2$ telah ditetapkan untuk meramal kegagalan ESD. Keputusan simulasi komputer menunjukkan persetujuan yang baik dengan nilai yang telah diukur di dalam had toleransi. Kajian ini mendapati bahawa radio yang diperbaharui menggunakan batang logam mempunyai $S_{twa}$ kurang dari had maksimum berbanding radio asal. Kajian ini juga meramal kegagalan ESD akan berlaku pada 8 kV and 11 kV bagi radio asal dan diperbaharui masing-masingnya. Hasil kajian ini juga menghasilkan

satu skim baru bagi jurutera untuk menilai risiko ESD pada radio dua hala di peringkat PCB. Mengenalpasti komponen yang paling berisiko kepada ESD di peringkat awal juga bermakna kegagalan ESD dapat ditangani secukupnya sebelum pengeluaran secara besar-besaran.

# PREDICTION OF ELECTROSTATIC DISCHARGE SOFT ERROR ON TWO-WAY RADIO USING SIMULATION AND IMMUNITY SCANNING TECHNIQUE

## ABSTRACT

Electrostatic discharge (ESD) is a major cause of failures and malfunctions in two-way communication radio. Soft error failures like logic error, latch-up and wrong reset can occur as a result of the excessive ESD. It is a well-known fact that the Complementary Metal-Oxide-Semiconductor (CMOS) devices are more susceptible to ESD. The failure of CMOS ICs due to ESD can also cause radio to reset or shutdown completely. Presently the failures are detected after the radio is built and tested only. In this research, new methodology is developed to assess the ESD risk of two-way radio at circuit level. Poynting vector is used to calculate the incident power received by susceptible integrated circuit during ESD. In doing so the two-way radio is modeled in 3-D using the IEC 61000-4-2 standard. The result provides a graphical means to visualize the propagation of ESD current in Printed Circuit Board (PCB) and ground plane. Time-weighted average power density $(S_{twa})$ calculated as a cross product between E-field and H-field was used extensively in the modeling, from which a maximum limit of 3.7 $W/m^2$, $S_{twa}$ was established for predicting ESD failures. It was observed that results obtained through computer simulation agree well with measured values within some tolerance limit. It was also discovered that the improved radio with metal bar is well above this limit compared to the original radio. It is also predicted that the soft error due to ESD would occur at 11 kV and 8 kV for improved and original radio respectively. Results from this study provide a new scheme for engineers to assess ESD risk of two-way radio at PCB level. Identifying most susceptible component to ESD allows radio failures to be addressed adequately before mass production.

# CHAPTER ONE

# INTRODUCTION

## 1.1 Introduction

Electrostatic discharge (ESD) is a discharge of electricity where a charge moves at different electrical potentials. ESD is a high voltage event which is generated from the released electrical energy through tribocharging or electrostatic induction. ESD can cause device failure during production, assembly, testing and at the user site. Among Integrated Circuit (IC) devices, Metal-Oxide-Semiconductor (MOS) is most susceptible to ESD damage (Unger (1981)). Complementary Metal-Oxide-Semiconductor (CMOS) IC can be very susceptible to system-level ESD stress although it has passed the component-level ESD specification (Yen and Ker (2007)). As ESD current is a source of system level failures, when the current flows through components or IC, it can cause a system failure (upset). The current induces electric fields (E) and magnetic fields (H) when travelling on the printed circuit boards (PCB), or any packaging components. This can lead to component malfunction and system failure (Voldman (2012)).

There are two types of ESD failure at system level – (i) ESD hard error failure (ii) ESD soft error failure. The hard error failure is commonly caused by physical destruction in interconnection inside a device or physical damage due to the high level of ESD current. The soft error failure is mainly caused by a logic error of IC such as glitches, abnormal interrupt request signal or signal inversions of the IC. The root cause of hard error failure is easily analyzed compared to soft error failure and it is traceable by finding the location of device breakdown. However it is difficult to find a root cause of ESD soft error failure because it is a temporary event and system is recovered after rebooting.

The history of electrostatic was not discovered until 600BC. Thales of Miletus began conducting experiments that involved charging amber by rubbing it with a piece of fur to observe an attraction to lightweight object such as fur and feather. In 1600, serious work in the field of electrostatic began with De Magnete, a book published by William Gilbert in the year 1600. Over the next several centuries, experiments by Gauss, Coulomb, Faraday and Franklin are established to understand the basis of electrostatics (Weitz (2015)).

From past history summarized in Table 1.1, the electrostatic discharge testing has evolved from a company based reliability test in the 1960s and 1970s to a performance test on electronic product. This requirement is that electronic products should operate normally when subjected to ESD phenomena by representing it in the real-world environment. The emphasis has switched from susceptibility of equipment to quote how immune a product to air-discharge and contact discharge from a portable ESD tester whose output is compliant with the latest international standard criteria (Hoolihan (2014)).

Table 1.1: Recent history of ESD testing of electronic product (Hoolihan (2014))

| Decade | Event |
|---|---|
| 1950s | − The electronic companies are concerned with the damage in electronic component and functional interruption of electronic products. |
| 1960-1970 | − Most companies started to use 5 kV then 7.5 kV discharge voltage as the passing level of ESD system level. |
| 1980s | − The First International Electrotechnical Commission (IEC) Publication 801-2 was released in 1984 for air-discharge test method. |
| 1990s | − Second edition of IEC 801-2 was released in 1991. Major change was to define the contact discharge mode as a preferred test method. |
| | − The first IEC 100-4-2 was released in 1995 for International Standard on Electrostatic Discharge Immunity test. It introduced Horizontal and vertical coupling planes on references. |
| | − Second edition of IEC 6100-4-2 was released in 2008 to replace the first edition in 1995. Key parameters of ED generator remain unchanged. |