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A ma famille

Résumé

Ces dernières années, l'utilisation des systèmes de transport aérien s'est considérablement amplifiée. Par conséquent, les considérations environnementales actuelles poussent à réduire leur utilisation. Des projets tels que Clean Sky 2 tentent d'apporter une réponse à ce problème, en proposant une réduction des émissions de CO_2 et des nuisances sonores. Le recours à l'hybridation de la propulsion des avions réduirait ces émissions en réduisant la taille et la masse des systèmes et en utilisant des systèmes électriques plus efficaces ce qui permettrai d'augmenter le nombre de passager. Cela permettrait de réduire la consommation de carburant et donc les émissions polluantes.

Ces travaux s'inscrivent dans le cadre du projet européen HASTECS Clean Sky 2 qui vise à optimiser l'ensemble de la chaîne électrique de l'avion à propulsion hybride en intégrant toutes les contraintes aéronautiques telles que les décharges partielles pour les équipements électriques placés en zone non pressurisée. Le projet HASTECS s'est fixé le défi de doubler la densité de puissance des machines électriques pour passer de 5 kW/kg à 10 kW/kg, y compris leur refroidissement, tandis que pour l'électronique de puissance, avec son système de refroidissement, le but sera de passer à 15 kW/kg en 2025 et à 25 kW/kg en 2035.

Pour augmenter la densité de puissance, la masse du système de refroidissement doit être diminuée dans un premier temps soit en optimisant ses composants, ce qui est fait par le 4ème lot de travail (WP4), soit en réduisant les pertes. La réduction des pertes de l'onduleur pourrait être obtenue en utilisant de semi-conducteurs de faible calibre en tension, en jouant sur les stratégies de modulation ou en utilisant des semi-conducteurs plus performants. La première option peut être faite en utilisant des architectures multi-niveaux pour éviter l'association en série direct. Contrairement à l'association directe en série, l'association parallèle est plus facile à gérer en termes de commande d'interrupteurs, ce qui a été autorisé dans nos études. Plusieurs topologies d'onduleurs (topologies à 2, 3 et 5 niveaux) et stratégies de modulation (PWM, injection de troisième harmonique, PWM discontinu et pleine onde) ont été comparées en utilisant plusieurs technologies de semi-conducteurs pour choisir la solution la plus performante en termes de rendement et de densité de puissance. Pour le profil de mission considéré, l'onduleur pourrait être dimensionné pour le point de puissance maximum (décollage) ou la phase de vol la plus longue (croisière). Une étude comparative des stratégies de modulation a été réalisée pour mettre en évidence la structure et la modulation présentant les meilleures performances afin de minimiser les pertes pour les points de dimensionnement choisis en utilisant les topologies les plus intéressantes pour le profil de mission étudié en utilisant deux configurations différentes de bobinage du moteur électrique proposées par le WP1.

Mots clés

Propulsion aéronautique hybride, Onduleur multiniveaux, Stratégies de modulation, Semi-conducteurs, Electronique de puissance.

Abstract

Recently, the use of air transport systems has increased considerably. Therefore, the current environmental considerations are pushing to reduce their ecological impact. Projects such as Clean Sky 2 provide an answer to this problem, by proposing a reduction in CO_2 emissions and noise pollution. The development of a hybrid-electric aircraft would reduce these emissions by reducing the size and weight of the systems and using more efficient electrical systems. This would reduce fuel consumption and therefore pollutant emissions.

This work takes part into HASTECS Clean Sky 2 European project which aims to optimize the complete electrical chain of the hybrid aircraft integrating all aeronautical constraints such as partial discharges for electrical equipment placed in the non-pressurized zone. HASTECS project has set itself the challenge of doubling the specific power of electric machines including their cooling from 5 kW/kg to 10 kW/kg, while the power electronics, with their cooling system, would evolve from 15 kW/kg in 2025 to 25 kW/kg in 2035.

To increase the specific power, the cooling system mass should be decreased either by optimizing its components which is done by the 4th work package (WP4) or by reducing power losses. Inverter losses reduction could be achieved by using small voltage rating components, by playing on modulation strategies or by using more performant semiconductors. The first option could be done by using multilevel architectures to avoid the direct series association. Unlike direct series association, the parallel one is easier to manage in terms of switches command so it was allowed in our studies. Several inverter topologies (2-, 3- and 5-level topologies) and modulation strategies (PWM, third harmonic injection, discontinuous PWM and full-wave) were compared using several semiconductors generations to choose the most performant solution in terms of efficiency and specific power. For the considered mission profile, the inverter could be sized for the maximum power point (takeoff) or the most extended flight phase (cruise). A comparative study of modulation strategies was carried out to highlight the structure and modulation presenting the best performance to minimize the losses for the chosen sizing points using most interesting topologies for the studied mission profile using two electrical motor windings configurations proposed by WP1.

Key words

Hybrid aircraft propulsion, Multi-level inverter, Modulation strategies, Semiconductors, Power electronics.

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List of acronyms

ANPC: Active Neutral Clamped Point topology

Avg: average

Cond: conduction

DPWM: Discontinuous Pulse Width Modulation

EMF: electromotive force

FC: Flying capacitor topology

FW: Full Wave modulation

GT: Gas turbines

HASTECS: Hybrid Aircraft reSearch on Thermal and Electric Components & Systems

MTOW: Maximum Take-Off Weight

NPC: Neutral Clamped Point topology

PMSM: Permanent Magnet Synchronous Motor

PWM: Pulse Width Modulation

RMS: Root Mean Square

SMC: Stacked Multicell Converter topology

SW: switching

THD: Total Harmonic Distortion

THIPWM: Third Harmonic Injection Pulse Width Modulation

WP: work package

General introduction

The environmental and ecological footprint of transport systems, particularly aircraft, has been increasing steadily in recent years. Current environmental considerations are, therefore, pushing to reduce their ecological impact. Projects such as the Clean Sky 2 project offer an answer to this problem, by proposing a reduction in CO_2 emissions and noise pollution. The development of a hybrid-electric propulsion aircraft would reduce these emissions by reducing the size and mass of systems and using more efficient electrical systems. This would reduce fuel consumption and thus pollutant emissions. It would also improve system reliability and reduce design and operating costs.

This work takes part in HASTECS Clean Sky 2 European project, which studies the possibility of series electric propulsion hybridization in an aircraft, and aimed to develop a simulation tool to pre-size inverters meant to drive hybrid-electric propulsion aircraft's motor. To do so, power electronics topologies, smart control and modulation strategies and also semiconductor technologies were taken into account.

To increase the specific power, the cooling system mass should be decreased either by optimizing its components which is done by the 4th work package or by reducing power losses. Inverter losses reduction could be achieved by using small voltage rating components, by playing on modulation strategies or by using more performant semiconductors.

The first chapter presents the main problem related to current aviation and the opportunities that hybrid-electric propulsion aircraft offers. Hybrid-electric propulsion aircraft principle and necessity will be shown due to the evolution of the commercial aircraft industry and environmental needs in addition to the Clean Sky 2 European project HASTECS goals. The problematic and objectives of this work will be presented in this chapter as well as the used load model.

In chapter II, the software organization and used power losses and thermal models will be presented. The used semiconductor database will also be discussed. This work aims to develop a simulation tool which allows to pre-size converters. It computes different results for different conversion architectures. Its entries are the design constraints, the foreseen converter topologies, and the semiconductor family or manufacturer choice from the available components database. The results such as the efficiency, number of semiconductor devices, maximal junction temperature, switching and apparent frequencies, total losses, and semiconductors, heat exchanger, DC bus capacitor and flying capacitor weights, and also the power density are shown as figures for different parameters of different architectures behaviors.

The studied inverter topologies and modulation strategies will be presented in chapter III. Then the performances will be compared using several semiconductors to choose the most performant solution in terms of efficiency and specific power. The main factor to increase the specific power that was identified in the first chapter is decreasing the cooling system mass,

optimizing its components which is a part of WP4 work or by reducing power losses. Inverter power losses reduction could be achieved either by using small components or by playing on modulation strategies or by using more performant semiconductors.

The main objective of chapter IV is to evaluate several power converter architectures and associated modulation strategies to power the electric machine used for the aircraft propulsion. A comparative study of modulation strategies was carried out to highlight the structure and modulation presenting the best performance to minimize the losses for the sizing point using 3-level topologies using two electrical motor windings configurations; 2 and 3 conductors per slot.

I. State of the art and context

Aviation undoubtedly brings economic and social benefits to society. However, related activities also contribute to climate change, environmental degradation, noise, and local air pollution. The aviation industry contributes about 2 % of the world's global carbon dioxide (CO_2) emissions [1], and this is set to rise so it is under pressure to reduce these emissions, even if air travel continues to gain popularity around the world as shown in Fig. I-1. To reduce the impact of air transport, new technologies are being studied. One solution could be to transpose the hybrid propulsion developed for land vehicles using batteries or fuel cells as an additional energy source to reduce fuel.

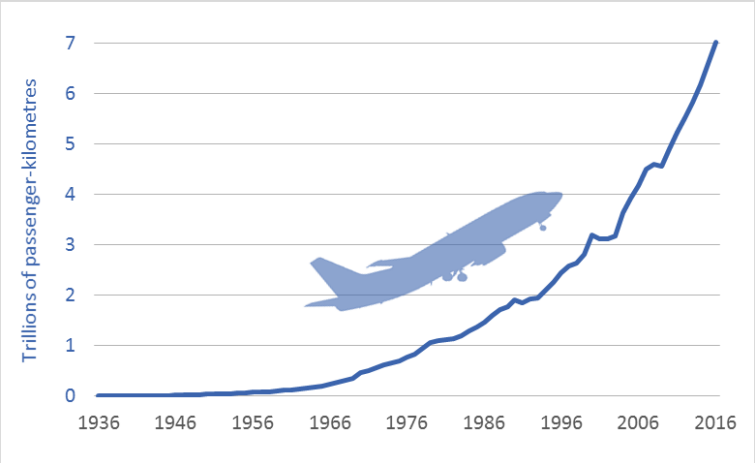


Fig. I-1. Global air travel 1936-2016 [2]

This chapter will present the main problem related to current aviation and the opportunities that hybrid-electric propulsion aircraft offers. To do so, the hybrid-electric propulsion aircraft principle and necessity will be shown due to the evolution of the commercial aircraft industry and environmental needs. These needs were set as the Clean Sky 2 European project HASTECS goals. This work takes part into this project [3] which aims to optimize the complete electrical chain of the hybrid aircraft integrating all aeronautical constraints such as partial discharges for electrical equipment placed in the non-pressurized zone or, in case of high operating voltage, even in the pressurized area. The problematic and objectives of this work will be presented in this chapter as well as the used motor model. To choose an adapted inverter topology, a regular 2-level inverter with a regular PWM was sized for the maximal power point to get a reference in terms of efficiency and specific power using a simple solution which will help to identify the areas to be worked on to reach the targets.

1. Hybrid-electric propulsion aircraft

Each year, about 37 million commercial aircraft carry 4 billion passengers[4], connecting 20,000 city pairs. Commercial aircraft now consume more than 270 million tons of jet fuel per year and thus produce more and more CO_2 emissions [5] as shown in Fig. I-2. Therefore, any discussion on reducing carbon emissions from commercial aircraft will have to be applicable

and effective at this scale. A clean sky is the objective of recent developments and research carried out by all aircraft manufacturers.

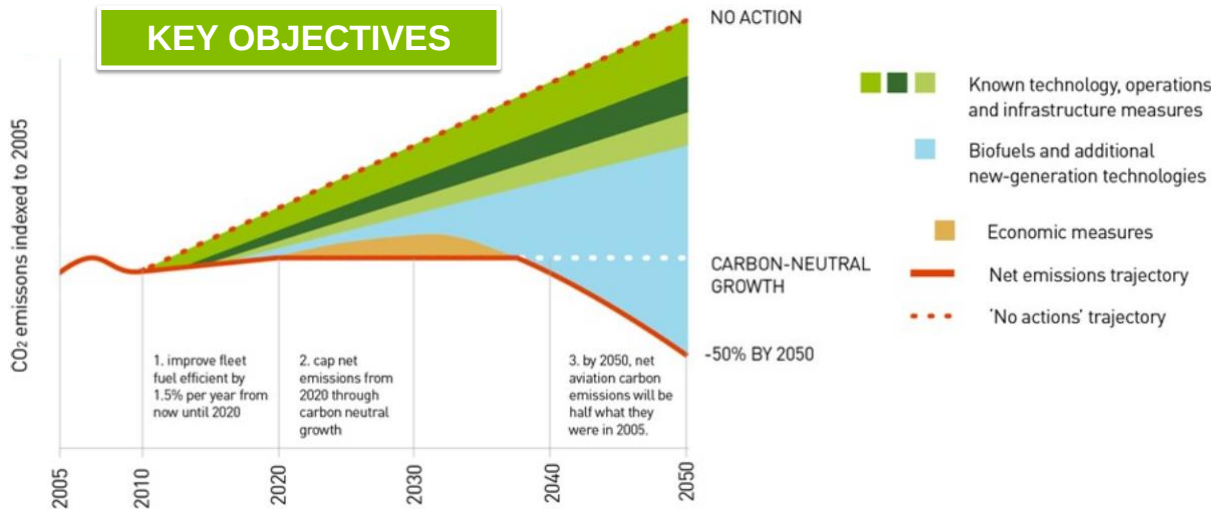


Fig. I-2. CO_2 Emissions Trends from International Aviation, 2005 to 2050

CO_2 emissions from a commercial aircraft can be reduced by reducing the energy required to fly the aircraft by reducing its weight or by improving the propulsion system efficiency or by reducing the amount of drag. This must include total life-cycle carbon emissions during fuel production. For electrical aircraft, this also would include carbon emissions generated by the power source, either on the ground for battery-powered aircraft or onboard electric aircraft equipped with a generator.

The desired overall objective of hybrid and fully electric transport vehicles/aircraft is to limit/cancel the CO_2 emissions caused by internal combustion engines to drive the propeller of the system. Weight may not be a desired optimized parameter in the terrestrial vehicle system, but on the other hand, for space vehicles, it is a highly recommended optimized parameter, because less mass means fewer energy requirements.

Electric propulsion has the potential to revolutionize flight: from cleaner and quieter travel to completely new vehicles, the benefits could be enormous. Faced with estimations that air traffic will double every 15 to 20 years, Airbus believes that electric and hybrid propulsion can offer a viable solution that allows their industry to grow sustainably while reducing its impact on the environment [6]. The international organization ATAG (Air Transport Action Group) in the aviation sector set objectives to have a cleaner sky. It wants to reduce fuel consumption by an average of 1.5 % per year from 2009 to 2020, and to cap CO_2 emissions with carbon-neutral growth from 2020 onwards, as well as to reduce net CO_2 emissions from aviation activities by half by 2050.

These objectives cannot be achieved with current technologies. That is why several projects on research and development of electric and hybrid-electric propulsion technologies are held. In addition to the obvious benefits of reducing CO_2 emissions and noise levels, electrification also makes it possible to completely re-evaluate the design of an aviation vehicle. Different range of vehicles will take advantage of the electrification. One of them concerns the low-capacity and limited-range urban air mobility demonstrators which are developed by Airbus: Vahana and CityAirbus, for intra-urban flights. These are all-electric air vehicles with a capacity of one to four passengers. In the longer term, Airbus believes that hybrid-electric propulsion will probably be installed on larger civil aircraft before becoming fully electric, as the power-to-weight ratios of battery technology are still far from being sufficient [7].

i. Hybrid and electric propulsion aircraft evolution

TABLE I-1 and TABLE I-2 summarize characteristics of some hybrid and electric propulsion aircraft that could be found in the literature.

This table shows a wide range of electric and hybrid propulsion aircrafts. There are mostly small power range aircraft. The small general aviation aircraft using the electric and hybrid propulsion systems are already flying. Indeed, small aircraft can be useful for testing in-flight new technologies. However, not all technologies suitable for general aviation aircraft are scalable to the large dimensions, long flight distances and high operational rates that are key characteristics of large commercial aircrafts.

The Boeing Sugar Volt has the closest power range to our studied case. However, the battery specific energy target reported by Boeing seems high compared to the other ones.

TABLE I-1. Hybrid-electric aircraft characteristics [8], [9],[10]

Name	Architecture	Max power (kW)	Maximum Take-Off Weight (kg)	Battery energy (Wh/kg)	Year
Boeing Sugar Volt [11], [12]	Parallel hybrid	1300-5300	70k-85k	750	2008
ENFICA – FC [13]	Series hybrid	40	550	100	2010
Siemens/Diamond E-Star [14]	Series hybrid	70	800	-	2011
Embry-Riddle Eco-Eagle	Parallel hybrid	105	1075	125	2011
Siemens/Diamond E-Star 2	Series hybrid	80	800	-	2013
Hypstair [15]	Series hybrid	200	-	-	2014
Cambridge SOUL[16], [17]	Parallel hybrid	20	235	144	2014
Airbus E-Fan 1.2	Series hybrid	60	600	-	2016

TABLE I-2. Full electric aircraft characteristics [8], [9],[10]

Name	Maximum power (kW)	MTOW (kg)	Battery energy (Wh/kg)	Year
Lange Antares [18]	42	660	136	2003
Fishman Electraflyer C [19]	13.5	283	-	2008
Yuneec E430 [20]	40	470	154	2009
Pipistrel Taurus Electro G2 [20]	40	450	-	2011
Pipistrel Taurus Electro G4 [21]	150	1500	180	2011
FB Stuttgart eGenius [21]	60	950	204	2011
Chip Yates Long ESA	192	680	-	2012
Airbus E-Fan	60	600	207	2014
Nasa X-57 Maxwell [12], [22]	132	1360	-	2014
Pipistrel Alpha Electro	60	550	171	2015
Siemens Extra 300 (330LE) [23]	260	1000	-	2016

Unlike Boeing who developed its hybrid-electric propulsion aircraft in 2008, Airbus began its journey to electric flight later. Fig. I-3 presents Airbus electro-mobility roadmap starting from 2010. As noticed in Fig. I-3, in only 10 years, the needed power is 100 times higher than for the single-seat Cri-Cri that was designed to fly 30 minutes. There is a multitude of challenges that must be researched and mastered to design the new single-aisle aircraft requiring 20 MW.

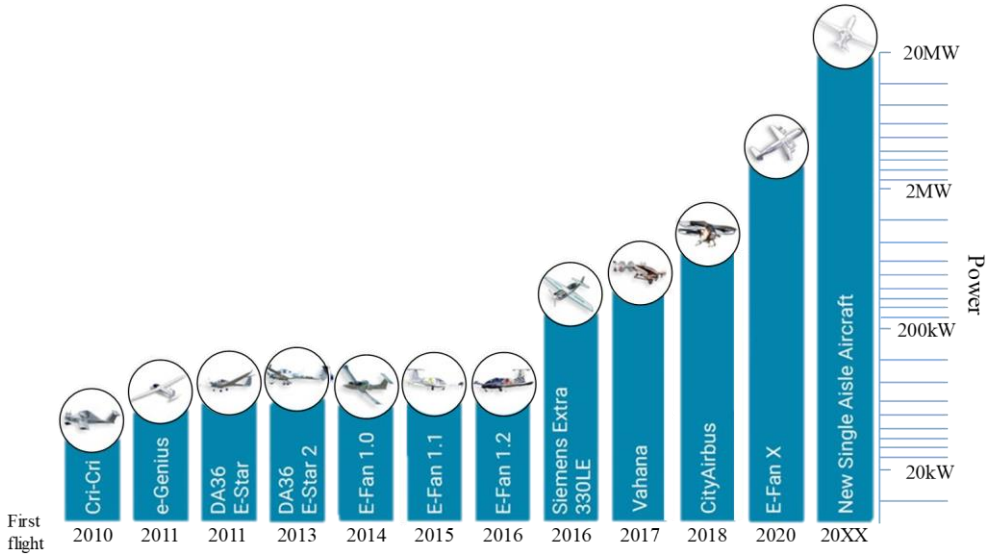


Fig. I-3. Airbus electro-mobility roadmap [24] [25]

The E-Fan family of aircraft allowed Airbus to learn many lessons from the hundreds of flights performed. In November 2017, Airbus launched the E-Fan X with its partners Siemens and Rolls-Royce which aims to replace only one propeller of the four by a hybrid-electric one. In June 2019, Rolls-Royce took over Siemens' e-Aircraft division, so Siemens is no longer involved in this project. This partnership aims to accelerate and take the technological maturity and performance of hybrid-electric propulsion to a new level. The E-Fan X is an ambitious technology demonstrator project that will be a decisive step towards the manufacture of a hybrid

electric civil aircraft on the scale of today's single-aisle aircraft. The consortium will use a BAe146 as a flight test platform for a hybrid serial architecture by 2020, consisting of a 2 MW electric motor, a gas turbine with integrated 2 MW generator and a 2 MW battery controlled by a control unit called "e-supervisor". E-fan X has the same power range as the one studied in our project presented later in this chapter.

ii. Hybrid-electric architectures

Recently, the idea to use hybrid architecture in aircraft propulsion has expanded. This idea is similar to what can be found in Hybrid Electrical Vehicles (HEV). Three different hybrid architectures exist: Series, Parallel and Series/Parallel systems, presented below. Each type of them has its benefits and criteria that differ from the others [26]. However, all three types share the idea of using a storage system that separates the thermal engine operating point (Gas Turbine, Electrical Generator or Auxiliary Power Unit (APU)) from the propulsion, thereby optimizing the efficiency of the thermal engine.

- Series Hybrid Propulsion:

In the series hybrid-electric architecture, the Gas turbines (GT) or the engine as in Fig. I-4 runs at constant RPM and drives a mechanically-coupled electrical generator that produces electric power. This power is then delivered to the system where it is combined with the electric power coming from the auxiliary power sources. To supply the AC electric motor, the DC power supply from the batteries and/or generator must be converted to AC power, which is done by power converters so that it can finally operate the electric motor that drives the propeller.

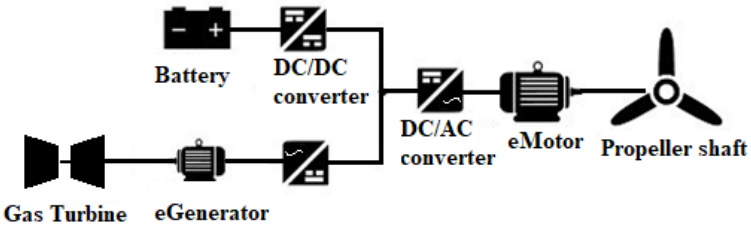


Fig. I-4. Series hybrid propulsion system [27]

- Parallel Hybrid Propulsion:

The parallel hybrid-electrical architecture (Fig. I-5) is more complex than that of the series. Indeed, to be able to have the propeller-driven simultaneously by the GT and the electric motor, a complex gearbox is required. Besides, the GT does not always operate at its maximum efficiency point but rather is required to operate at a wide range of speeds, which generally makes it less efficient. Conversely, the parallel architecture has the advantage that the electric motor can be less powerful and therefore smaller and lighter than in series architecture since it does not have to provide the maximum power required for the propeller alone. Since it is not necessary to convert the GT mechanical power into electrical power, the electrical generator is not present, but the advantages of getting rid of it are reduced by the need for the complex

mechanical transmission and gearbox part used to distribute the mechanical power between the electric motor, the GT and the propeller.

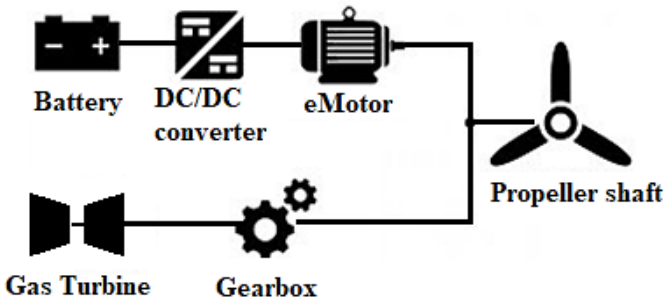


Fig. I-5. Parallel hybrid propulsion system [27]

- Combined Hybrid, mixed or association of Parallel/Series Hybrid Propulsion:

This architecture merges the two series and parallel types. The main advantages of this architecture are that it allows a smaller gas turbine to operate optimally and directly during the cruise mission phase, and also to charge the batteries, a possibility that traditional parallel architectures do not allow. This powertrain architecture is widely used in the automotive industry.

TABLE I-3 sums up the advantages and disadvantages of both series and parallel hybrid architectures. The series-parallel configuration benefits from most of the advantages of both configurations. The engine propulsion power is divided into two power-flows, which are transmitted to the propeller over a mechanical and an electrical branch. However, this configuration is more complex to design and control.

TABLE I-3. Advantages and disadvantages of series and parallel hybrid propulsion architectures

Architecture	Series	Parallel
Pros	• E-motor configuration is relatively simple to control • Engine able to operate at its maximum efficiency point • Gas turbine is more efficient at low speed and high load	• A small engine and motor help reduce vehicle mass • Performs well in high average power and high load conditions • higher transmission efficiency due to the mechanical connection
Cons	• Low transmission efficiency	• complex mechanical transmission • The design and control is relatively more complex than the series configuration

iii. Energy management for the studied solution

Only the series propulsive system is taken into account in the scope of this study.

The general schematic of the system during different phases of a mission is shown in Fig. I-6. In the meantime, our study considers only the power conversion for motor driving. There are two main phases in this mission profile; the takeoff which represents the maximal power point and the cruise which is the longest phase of the flight mission. Taxi out and in and descent could be powered using full electric energy given by auxiliary electric source either the batteries or the fuel cell. During these sequences, the power demand is low and the turboshafts could be relieved by electric power sources which are more efficient. This scenario corresponds to a light hybridization. The gas turbine could be sized for the cruise power point and auxiliary electric source could be used to help the gas turbine to supply the needed electric power for the takeoff.

This study does not cover hybridization and energy generation but focuses mainly on the inverter that feeds the electric motor connected to the propeller.

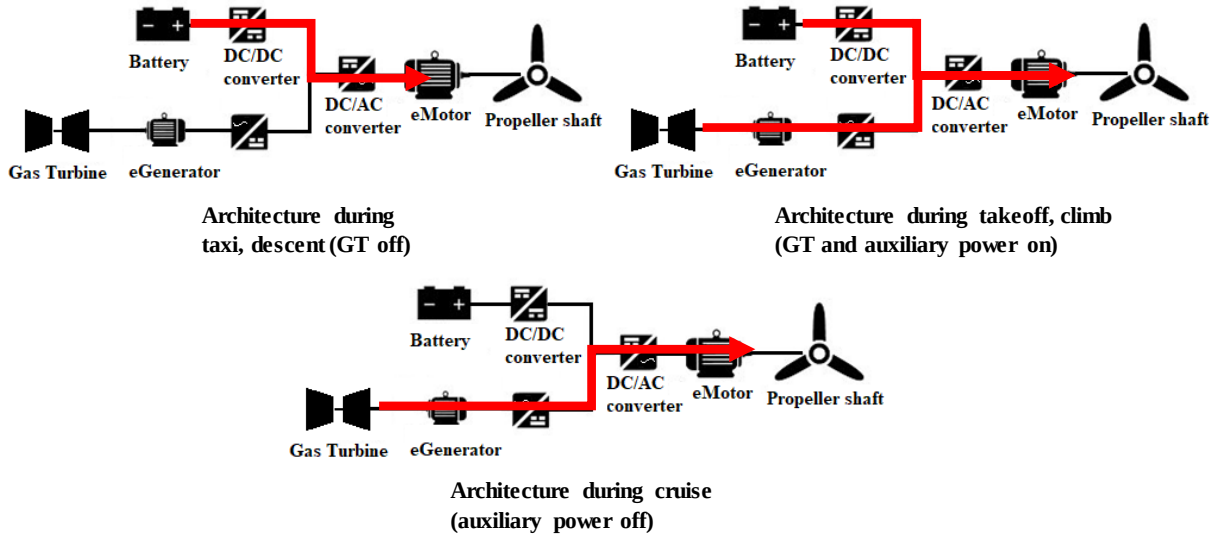


Fig. I-6. General propulsion schematic system during a mission of an aircraft [28]

2. Problematic and objectives

i. HASTECS project

The overall objective of the HASTECS (Hybrid Aircraft: Academic research on thermal & Electric Components & Systems) project is to support a hybrid-electric demonstration by developing models and tools that can help designers evaluate the main benefits of architectures and energy management. The assessments will be integrated at system level and will include the design and analysis of the main components of the hybrid energy chain: electrical machines and their cooling, cables, power electronics and associated thermal management taking into

account the main environmental constraints, including partial discharges due to the new high power and ultra-high voltage standards.

To this end, the various working groups will try to optimize the performance of electrical and thermal components in terms of specific power (kW/kg) or specific energy for batteries or fuel cells. The energy efficiency of the components and the entire system with its energy management is a second major objective. The performance evaluation will be based on the "basic architecture" presented in Fig. I-7 and extrapolations will, of course, be made to generalize our results to other architectures and other power levels.

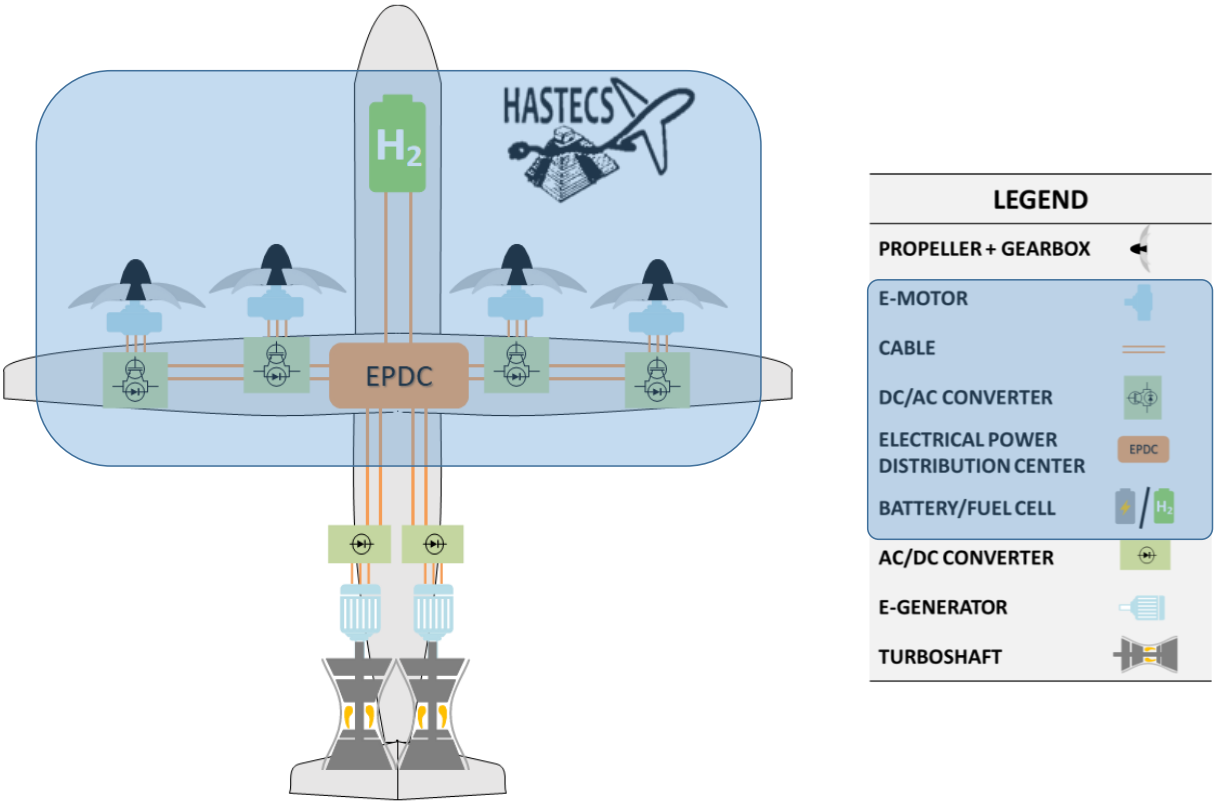


Fig. I-7. Baseline architecture for assessments

The " brakes on innovation " and the subsequent physical limitations that would make it difficult to achieve performance objectives will be identified, and a sensitivity analysis will be carried out to select the most significant impact on technologies and components taking into account the environmental constraints. These constraints are mainly partial discharges and thermal cooling systems and they depend on environmental conditions (external temperature, pressure, humidity, air velocity) in the nacelle as well as in the fuselage.

ii. Hybrid-electric components specific power targets

The power chain needs careful design to minimize the weight of the whole system. This last element is directly linked to the weight of the converter but also the losses through the weight

of the heat exchanger. To obtain an aircraft with a propulsive system weight similar to the current one, some research projects have set targets in terms of specific power for the different components of the power chain as reported in TABLE I-4. Based on this specific power values, our project sets its targets that will be detailed in the project presentation.

TABLE I-4. Electric components specific power state of the art and research targets [29]

	Motor & Generator		**Power Electronics**		**Battery**
	Power (MW)	**Specific Power (kW/kg)**	**Power (MW)**	**Specific Power (kW/kg)**	**Specific Energy (Wh/kg)**
Current state of the art (2016)					
Non cryogenic	0.25	2.2	0.25	2.2	200-250
Cryogenic	1.5	0.2			
Research goals (2016)					
NASA 10-year goals	1-3	13	1-3	15	
NASA 15-year goals	5-10	16	5-10	19	
US Air Force 20-year goals	1	5	1	5	400-600
Ohio State University 5-year goals	2	15	2	23	

However, this project sets two main objectives in terms of specific power. The first is the "medium-term objective of 2025" which corresponds to 15 kW/kg for power electronics including their cooling system and 5 kW/kg for electrical machines including cooling. The second is the "2035 long-term objective" which corresponds to 25 kW/kg for the power electronics and 10 kW/kg for electrical machines including their cooling systems (TABLE I-5).

TABLE I-5. Electric components HASTECS specific power targets

	Electric motor Specific Power (kW/kg)	**Inverter Specific Power (kW/kg)**
HASTECS targets (2016)		
2025	5	15
2035	10	25

Achieving these objectives would have major positive consequences for the environment, with a constant reduction in fuel consumption in flight and a reduction in ground noise thanks to entirely electric taxiing.

iii. Flight mission profile

The flight mission profile, in terms of electric motor voltage and current, considered in the project is shown in Fig. I-8. The maximum power is in the range of MW and due to confidentiality issues, the value of the maximum power cannot be given: all power values will be given in per unit.

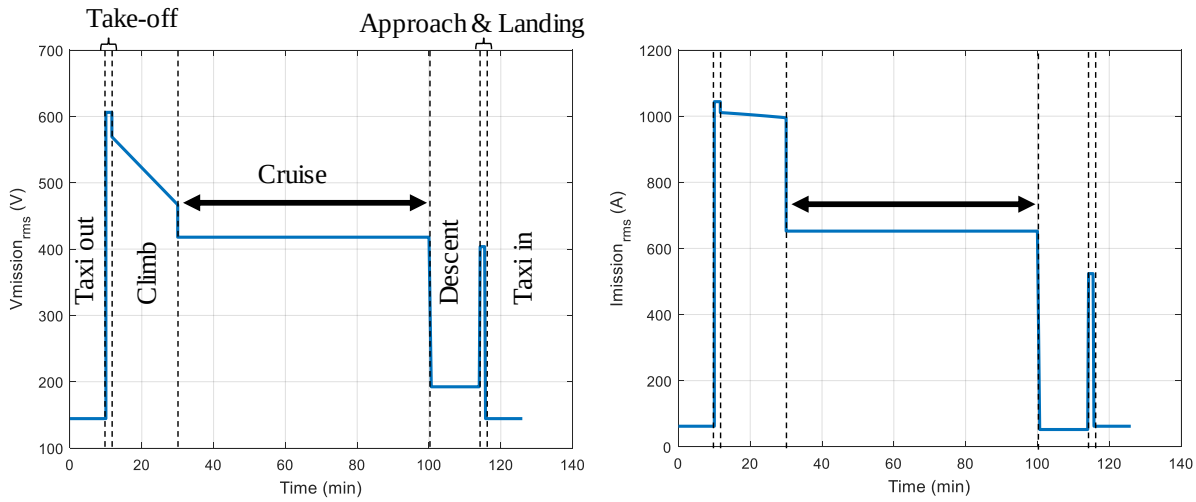


Fig. I-8. Voltage and current RMS mission profile

Two targets in term of efficiency for the power electronics were set by HASTECS project. For the 2025 target, the efficiency should be higher than 98 % for the cruise point and higher than 96.5 % for the maximal power point. On the other hand, for the 2035 target, the efficiency should be higher than 99.5 % for the cruise point and higher than 99 % for the maximal power point (TABLE I-6).

TABLE I-6. HASTECS inverter efficiency targets

	Take-off Efficiency (%)	**Cruise Efficiency (%)**
HASTECS targets (2016)		
2025	96.5	98
2035	99	99.5

iv. HASTECS work packages

To achieve these objectives, the INPT has assembled a consortium of 3 research laboratories with experience in the preliminary design of electrical and thermal components and architectures for aerospace applications:

- Laboratory on Plasma and Energy Conversion (LAPLACE), Toulouse (FR)
- Research and Engineering Institute for Transport and Environment (P'), Poitiers (FR)
- Inter-university Material Research and Engineering Centre (CIRIMAT), Toulouse (FR)

To achieve these general objectives, the HASTECS project has identified six technical work packages derived from the baseline architecture (Fig. I-9). It started in September 2016 and will last for 5 years and it includes 6 Ph.D. thesis and 2 post-doctoral positions. Each work package objectives are detailed below.

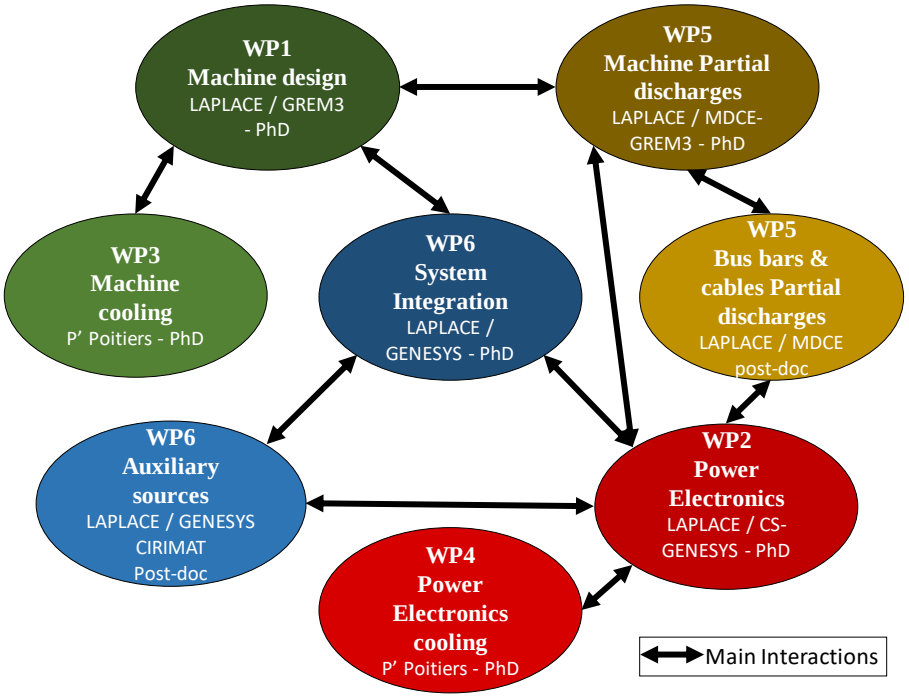


Fig. I-9. HASTECS consortium structure

WP 1: develop a target-setting tool to help evaluate the design of electric machines for hybrid-electric propulsion. The main objective is to analyze the phenomena that limit the specific power of electrical machines and to propose technological and structural innovations (geometry);

WP 2: develop sizing trends of static converters for a hybrid-electric propulsion system. Define two or three levels of DC bus standards for which every component will be designed; the first at a "moderated voltage" (~700 V); the second (and potentially third) at few kV (<7 kV); and develop a design tool for the estimation of power electronics performances;

WP 3: propose and analyze original machine cooling solutions;

WP 4: provide cooling and heat exchanger system solutions for power electronic converters;

WP 5: take into account the partial discharges phenomenon and assess impacts in the design of the power electronics and electric machines of the Hybrid Electric Propulsion System;

WP 6: develop simplified models for the most promising technologies of auxiliary sources (Lithium-Ion batteries, fuel cells) for 2035; and integrate technological bricks (machines, power electronics, cables, storage components, cooling system) and new concepts proposed in other WPs, then optimize the overall hybrid chain integrating its power management strategy.

For example, for our work package (WP2) strong links with the other WPs (Fig. I-9) exist, detailed below for each one.

- WP4: converter losses and components heat fluxes in W/cm^2 will impact heat exchanger system sizing and the transient capacity of this latter will influence converter sizing point.

- WP5: the voltage variation generated by the change of switch state, both in static and dynamic, will represent the stress of bus bars, cables and motor windings leading to possible partial discharges.

- WP6: to optimize the whole architecture, the WP2 needs to develop equations and models representing the trends studied in the "system integration" task.

WP1: To design the power electronics converter, a machine model is needed. Moreover, the switching frequency has a great impact on motor losses and current waveform.

Many possible electrical motors can be used in the scope of aircraft propulsion system design. Recent applications in the transportation domains are mostly using Permanent Magnet Synchronous Motor (PMSM) due to many specifications mainly high power density. This work does not highlight the mechanical solution of the system design since this part is a main study of WP1.

The simplified electrical model of a PMSM consists of the synchronous inductor with a resistor and the electromotive force (EMF) in series which is presented in Fig. I-10. The iron losses are not represented but have been taken into account in the sizing by WP1. The choice here is to maximize the torque, so the current is in phase with the EMF (non-salient pole rotor). This results in the vector diagram of Fig. I-10. The current is not in phase with the output voltage, leading to a power factor not equal to one and an oversizing of the inverter. Equations (I-1) and (I-2) can be determined.

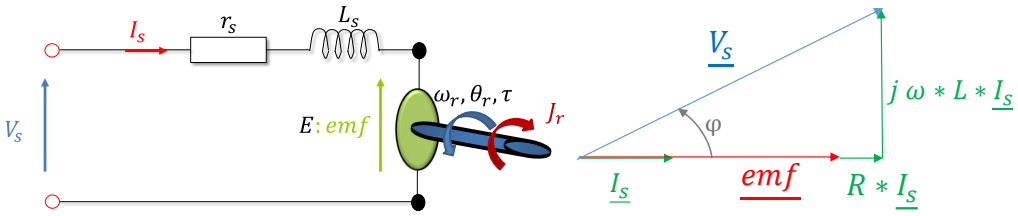


Fig. I-10. Electrical PMSM model (single phase), Vector diagram of the PMSM for a maximum torque

$$\underline{V_s} = R * \underline{I_s} + jL\,\omega\,\underline{I_s} + \underline{emf} \quad \text{(I-1)}$$

$$emf(t) = \Phi_{no\_load} * \omega * \sin(\omega t) \quad \text{(I-2)}$$

So the given parameters from WP1 are R and L the stator resistance and inductance and Φ_{no_load} the no-load flux and ω the electric pulsation or the frequency.

v. Work Package 2 (WP2)

The work package focuses only on the inverter used to power the electric motor that drives the propeller.

WP2's goal is to develop a software tool that determines the best static converter architectures for hybrid-electric propulsion shown in Fig. I-11, taking into account both environmental and cooling constraints. The tool must evaluate the efficiency of the chosen solution, its weight and other factors for the medium term (2025) or the future (2035). In order to facilitate the integration tasks of the WP6 system, an output model representing the design trends will be provided to process them in an optimization cycle. The proposed study will be based in particular on the post-doctoral study "High power conversion chain for aircraft hybrid propulsion" carried out by Mohammad IBRAHIM [28] in cooperation with Airbus FPO.

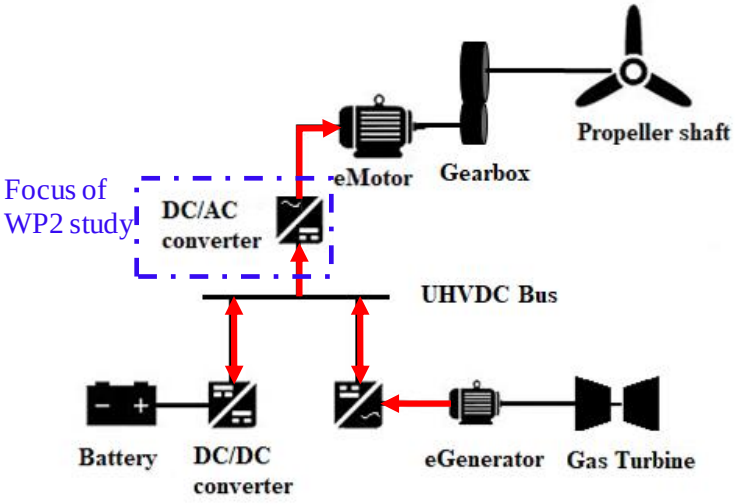


Fig. I-11. Hybrid Electric propulsion system configuration

Even if the system is inside the fuselage (i.e. in a pressurized area), the cruise cabin altitude is higher than the limit given by manufacturers of the high-power modules for ground equipment. Besides, the ability to extract heat losses from the converter is a huge problem: for example, a 1 MW converter with 95 % efficiency will have 50 kW of losses!

Compared to the static converters used today in aeronautical electrical networks, the nominal power of the converters will increase significantly (more than 1 MW). Therefore, the bus voltage value must also increase above 700 V, which will be critical in the event of partial discharge.

The variation of the operating point during flight sequences as shown in Fig. I-8 represents a serious issue that should be investigated. Maximum power is only required during the "take-off" and "climb". The cruise power requirement is lower (half the maximum power) and represents more than half the duration of the mission. Thus, if the converter is sized for maximum power, it will be mainly used at operating points where its efficiency is not optimized. This is a major difference compared to the electric propulsion of land vehicles. The

study will, therefore, attempt to optimize the choice of converter sizing points to be able to accept peak consumption while having the highest efficiency throughout the mission (especially during the cruise).

If the sizing power of the converter is close to the take-off power, solutions to increase the efficiency of the converter when it is used at low power can be studied: for example, the number of converter legs or switches in parallel can be changed according to the desired power (because the power is directly linked to the current, the speed of the machine being close to constant). Of course, such a solution will lead to a heavier sizing, only used at its nominal capacity during a short period (take-off). Another possibility is to use two or more converters. In the case of two converters, both are operated during take-off. Then, only one is connected to the motor, the other one being used for other non-propulsive functions.

Several converter architectures will be evaluated according to the value of the DC bus and the sizing power, through different criteria (weight, losses, output frequency, passive components weight, etc.), using today silicon components as IGBTs, which are the most suitable for the needed power, voltage and frequency ranges, with the first target around 2025. But since the project is designing the aircraft of the future (long term target for 2035), a sizing with silicon carbide components (SiC) or other new technologies will also be made.

To study all aspects and to achieve these objectives, WP2 was composed of two successive tasks. The first one deals with the study and design of a unique power converter for the whole power needed by the application. It will take into account the possible value for the DC Bus and different architectures of the power converter based on silicon power devices. The second one was devoted to the study of power converter architectures using components based on new generations and technologies and several control strategies. Moreover, in this study, the filters are not considered since network quality constraints are not taken into account as well as their potential impact on the mass of the system.

3. Reference case: 2-level PWM inverter solution

To choose an adapted inverter topology, a regular 2-level inverter with a sine PWM was sized for the maximal power point to get an idea about what could be achieved in terms of specific power using a simple solution.

For this study case, the DC voltage (V_{DCBus}) is chosen to deliver the needed maximal voltage of the electric machine ($V_{out_{max}}$) as in TABLE I-7. The inverter is sized for the maximal power point with a 2 kV DC bus and a switching frequency of 5.8 kHz which represents approximately 11 times the PMSM nominal frequency parameter given by WP1. To estimate the inverter specific power including the heat exchanger, a 0.34 kW/kg coefficient is taken into account which translates the power losses directly into cooling system weight. This value is used as a base value issued from the specification dossier. The passive components weight, capacitors, in this case, are also taken into account.

TABLE I-7. Used specification

Fundamental frequency (Hz)	532.3
$\boldsymbol{V_{out_{max}}}$ **(V)**	857.3
$\boldsymbol{I_{out_{RMS}}}$ **(A)**	1054
Modulation index	0.86
Power factor	0.78

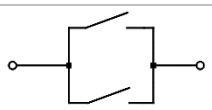
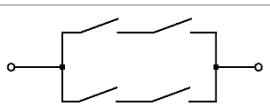
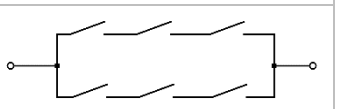
To withstand the current imposed by the machine, semiconductors are put in parallel if the needed current rating exceeds the maximally available one. On the other hand, to withstand the voltage depending on the voltage using rate (K_v), components may be associated in series (n_{series}). The components are used up to 100 % of their current rating.

$$n_{series} = \frac{2*K_v}{V_{rating}} * V_{DCBus} \tag{I-3}$$

If the direct series association is not allowed and the components should be used up to 50 % of their nominal voltage, only one component rating could be used which is 6500 V. However, these components are not adapted to the used high switching frequency. If the second largest voltage rating components (3300 V) are to be used, they should be used up to 61 % of their rating in order to use only one component in series.

The first study case uses two 3300 V / 800 A Infineon components associated in parallel to withstand the current and are used at 61 % of their voltage caliber. The second one uses two 1700 V / 600 A Infineon components associated in parallel and two components in series used at 59% of their voltage caliber even if the direct series association is hard to realize. For the third case, two 1200 V / 600 A Infineon components are associated in parallel and three components in series used at 56 % of their voltage caliber. TABLE I-8 sums the main inverter performances for these three study cases.

TABLE I-8. 2-level inverter performances

Components voltage ratings	3300 V	1700 V	1200 V
$\boldsymbol{\eta}$**(%)**	92.55	98	98.54
Junction temperature (°C)	244	307	98
Specific Power (kW/kg)	3.39	8.86	9.23
Series and parallel associations (per switch)			
Total number of semiconductors (per phase)	4	8	12

For the 3.3 kV components, the obtained efficiency is very low so as the specific power compared to smaller components. The maximal junction temperature exceeds the limit of 150 °C for the 3.3 kV and 1.7 kV components. If the efficiency is higher so the cooling system mass is lower, which leads to a higher specific power. But these results are still far from the targets. To have an acceptable solution using the 3.3 kV components, the switching frequency should be reduced to 2 kHz ($3.8 \times 532\ Hz$) whereas for the 1.7 kV ones it is not possible even if the switching frequency is equal to the machine fundamental frequency (532 Hz).

Fig. I-12 shows the inverter weight distribution for the different used voltage rating components. The cooling system mass, which is a direct image of the power losses through the coefficient given by Airbus, is the predominant weight of the inverter. The bus bar comes in second place and will be dominant if the heat exchanger weight is reduced.

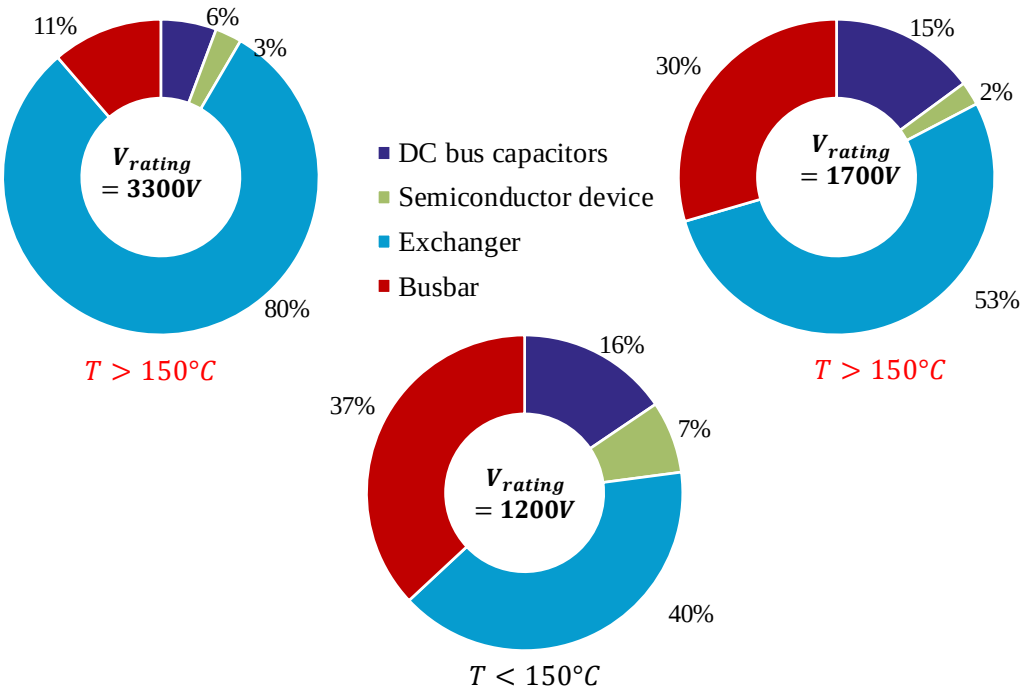


Fig. I-12. Inverter weight distribution for different used voltage rating components

Small rating components have of course better performances, but the direct series association is hard to realize so using multilevel topologies could be a solution. From these examples, the main factors to increase power density are identified. The first one is decreasing the cooling system mass, optimizing its components or by reducing power losses. The second one will be to optimize the bus bar weight.

4. Conclusion

HASTECS project studies the possibility of electric propulsion hybridization in an aircraft. Besides the global architecture, the different work packages aim to increase the specific power of the different components of a high-power electric chain incorporating a high-voltage DC

bus, its wiring and power electronics interfacing the bus and the electric motor to have a solution that can be fitted in an aircraft.

This study will lead to an optimization of the complete chain that will propose the interesting structures integrating all aeronautical constraints such as partial discharges for electrical equipment placed in a non-pressurized zone or case of high operating voltage even in a pressurized zone. In this Ph.D., power electronics topologies, smart control, and modulation strategies and also semiconductor technologies will be taken into account. This work objective is to design a highly integrated power electronics inverter with a specific power of 15 kW/kg for 2025 target and 25 kW/kg for 2035 target including its cooling system.

Our work package focuses on the power electronics converter. To guide the work of the various work packages of the project, a first step is to define an optimal DC bus voltage range. This has a direct impact on the study of partial discharges but also in the design of motor windings. This will be done using a developed simulation tool, detailed in Chapter II, which uses the conventional inverter topologies model and components from the available database, to compute the inverter performances as efficiency, maximal junction temperature, and total weight.

Then, it is necessary to compare the efficiency and power density of several multilevel topologies, modulation strategies and components technologies which will be evaluated in Chapter III, to find the optimal solution. A 3D inverter model will be designed to estimate more accurately the total inverter weight including the bus bar. This study will lead to the inverter topologies choice for the given specification.

In chapter IV the chosen inverter topologies will be evaluated for two electric motor configuration for the entire flight mission. A comparative study of modulation control strategies will be carried out to highlight the structure and modulation presenting the best performance to minimize the losses.

II. Simulation tool

This work aims to develop a pre-design tool which allows to pre-size the converters and their components for a DC to AC 3 phases inverter as in Fig. II-1. It computes different performance results for different conversion architectures. Its main entries and results are as follows:

Entries:

- Specification (DC bus voltage, output power, load power factor…),
- Inverter topologies,
- Modulation strategy,
- Switching frequency,
- Semiconductor manufacturer,
- Heat exchanger coefficient is given by WP4 that translates power losses to cooling system weight.

Results:

- Efficiency
- Semiconductor power losses (conduction and switching),
- Number of semiconductors associated in series and in parallel,
- Maximal junction temperature,
- Semiconductors, capacitors and cooling system weights,
- Specific power.

The results are shown as figures for different parameters of different architectures behaviors.

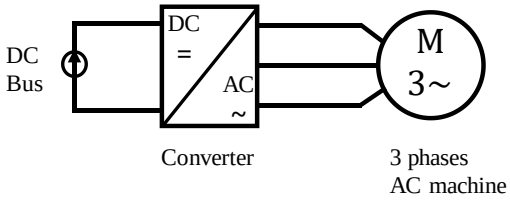


Fig. II-1. Studied electric system

In this chapter, the organization of the software will be presented. In this software, the inverter topologies and modulation strategies are fixed so that the user can choose his inputs from those available. It calculates the power losses and junction temperature for each selected case according to the model that will be detailed later in this chapter using the parameters of the selected semiconductor. This semiconductor device is selected from the available database or can be generated in such a way as to adapt to the necessary current and voltage calibers if the user so decides, according to the generation principle which will be described and validated below. The sizing of the capacitor will then be explained. The loss models will then be validated using a time simulation on *Plecs* for several inverter topologies. These models and the generated components will then help to define the voltage range of the DC bus, which corresponds to the first step of the WP2's work.

1. Software organization

The tool makes it possible from a specification to size the converter according to the chosen topology. It also makes it possible to carry out parametric studies by varying the DC bus voltage, the requested power or the modulation index to determine the optimum operating point. It can also take into account a mission profile that allows checking the performances of the converter for a given mission[28].

Then the tool computes the different results. It is realized in *Matlab* object programming to model converters architectures and is based on analytical calculations of the losses in the semiconductor components for the various integrated multilevel architectures considering several modulation strategies. These losses result in heating up the semiconductors. The thermal rising in the semiconductor will affect its functionality and its lifetime, however, this was not taken into account in this work. Moreover, the losses impact the size of the cooling system needed in the design.

For example, to size a 3-level FC inverter using the user specifications, the tool defines firstly the needed voltage and current components ratings for semiconductors, DC bus and flying capacitors. Then, from the available database, using a database manager program, choses the most appropriate components and uses their parameters to compute the inverter performances including the power losses, efficiency, maximal junction temperature and also the total weight.

To get an image of the object-oriented principle used to model the converters topologies in *Matlab*, a diagram in Fig. II-2 is established. It illustrates the class diagram of the proposed model. Hence we can distinguish all the links and dependencies between objects.

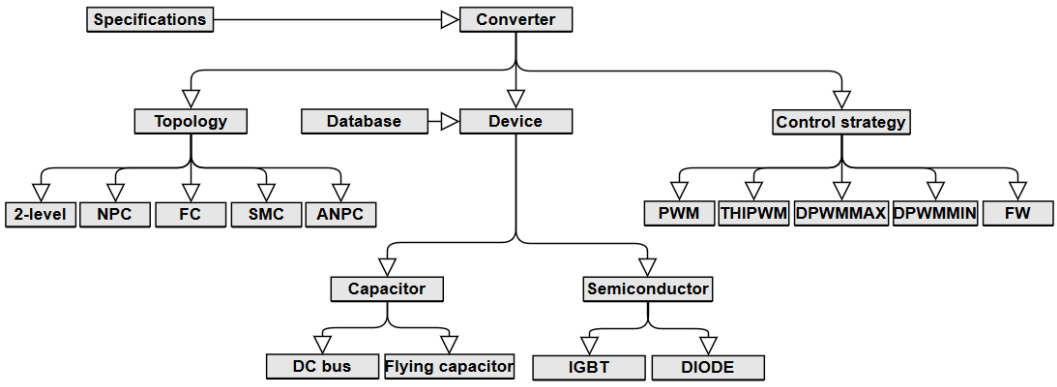


Fig. II-2. Software organization

The ‘Device’ object, for example, is a class that can be linked to a database. This element can then be characterized as a semiconductor, capacitor, or any other type of item. For example, inductors are integrated to the software as a Device object and not used in this work but it could be used if necessary, for example, as a filtering components. So the software is completely modular and could be easily modified to add new objects. Each element has a number of

associated properties and methods. For a semiconductor element, an object of either type IGBT or type DIODE is created.

Furthermore, an object of type converter is proposed and can be characterized into multiple topologies (2-level topology, FC, NPC, SMC or ANPC). This converter object is then linked with a specification object and a set of semiconductor and capacitor elements. It is also composed of control or modulation strategies that uses the selected topology and devices parameter to evaluate the power losses. Each block may contain one *Matlab* m-file script or multiple ones. Moreover, each script has data and characteristics of classes and their properties; the scripts are named as the including class inside them. These converter components will be detailed in Chapter III.

For each design point, it selects from the available database, the most appropriate semiconductor components that fit well the desired voltage and current. In order to do so, an adapted algorithm was developed (Fig. II-3).

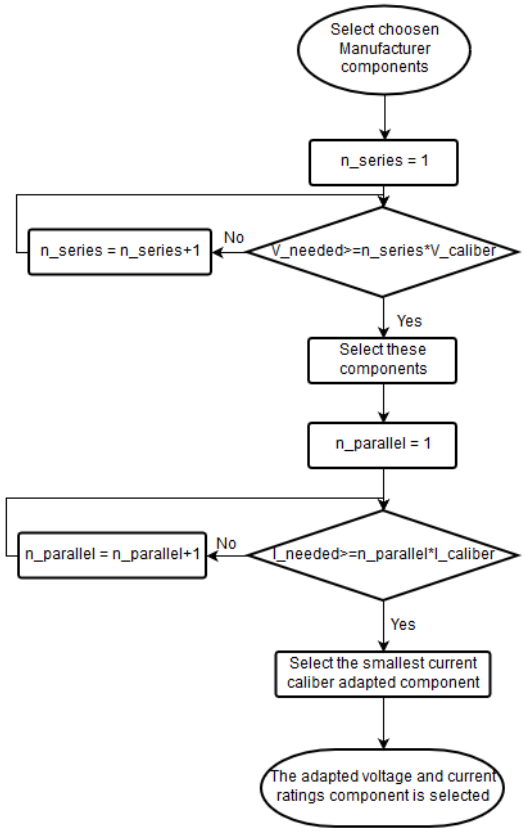


Fig. II-3. Available component selection algorithm

The first step of this algorithm is selecting the manufacturer chosen by the user to extract the corresponding components from the database. It is then determined whether the requested voltage rating can be achieved by the available components. If none of the components is adapted and therefore the biggest component is too small, components are connected in series to obtain the desired voltage. Otherwise, if several component calibers are suitable, the smallest caliber is chosen among those which are suitable so to have the best performing component as

noticed in Chapter I. for the current caliber, if the required current is higher than the largest current rating component, components are associated in parallel. Otherwise, if several components are adapted, the smallest one is selected.

This software allows great flexibility and a large degree of freedom for different designs and their behaviors during studies. This adds many advantages regarding multiple methods implementations and desired parametric sweep modeling.

2. Power losses and thermal modeling

After selecting the components, the next step is to compute the power losses to evaluate the inverter efficiency. They will also be used to calculate the maximal junction temperature. These losses and junction temperature are computed using a simplified models presented below.

i. Modeling principle

In order to model the losses in the semiconductor, we need to calculate the switching and conduction losses. Both losses depend on the circuit parameters and device characteristics. In order to simplify the calculation of the losses caused by power semiconductors, a number of preliminary assumptions have been made. In this case, the used semiconductor are only silicon IGBTs and diodes. These are set out below:

- The modulation depth is represented by the index k which value is between 0 and 1. Only the sine PWM power losses will be presented in this chapter;

- The load is considered linear: the load current is sinusoidal with an RMS value depending on the voltage value applied;

- Current and voltage ripples are neglected;

- The system is considered to be in steady state;

- The load (PMSM sized by WP1 presented in Chapter 1) is always inductive so the phase shift θ between the phase current and the associated single voltage belongs to the interval $[0, \pi/2]$.

- No dead time on IGBT drive orders.

For the power losses model, the current and voltage characteristics of a transistor during a switching period are represented in Fig .II-4. There are two types of power losses, switching and conduction losses.

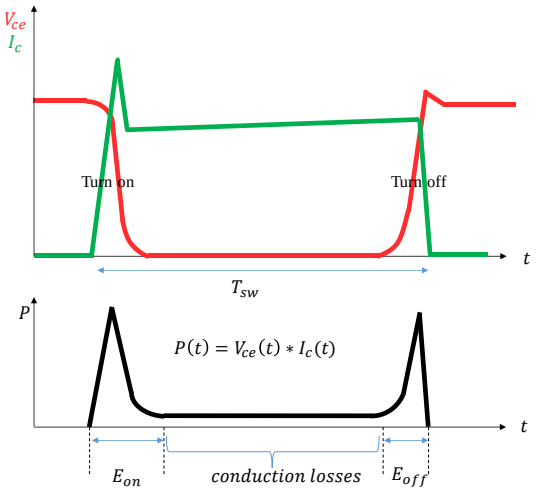


Fig .II-4. IGBT current and voltage waveforms during switching and conduction and switching losses

The power losses are compute using the current-voltage product. To calculate the conduction ones, the IGBT and diode can be modeled by a voltage drop and an internal resistance connected in series considering only a positive current[30] [31]. The voltage is obtained with the formula (II-1).

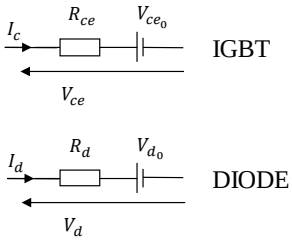


Fig. II-5. IGBT and Diode equivalent electric circuit

$$V_{ce} = V_{ce_0} + R_{dson} * I_c \tag{II-1}$$

Then the conduction losses can be computed using (II-2):

$$P_{cond} = \frac{1}{T_{modulation}} \int_0^{T_{modulation}} V_{ce}(t) * I_c(t) dt \tag{II-2}$$

The switching losses are neglected for the conduction losses calculation.

$$P_{cond} = V_{ce_0} * I_{c_{average}} + R_{dson} * {I_{c_{rms}}}^2 \tag{II-3}$$

Where $I_{c_{average}}$ and $I_{c_{rms}}$ are respectively the average and RMS values of the current.

To calculate the switching losses, the curves of the energy losses versus the switched current given for a switched voltage, present in the datasheets (Fig. II-6), are used. They can be approximated by a second-order equation with three parameters A_x, B_x, and C_x as shown in Fig. II-6.

$$E_x = A_x + B_x * I + C_x * I^2 \quad \text{(II-4)}$$

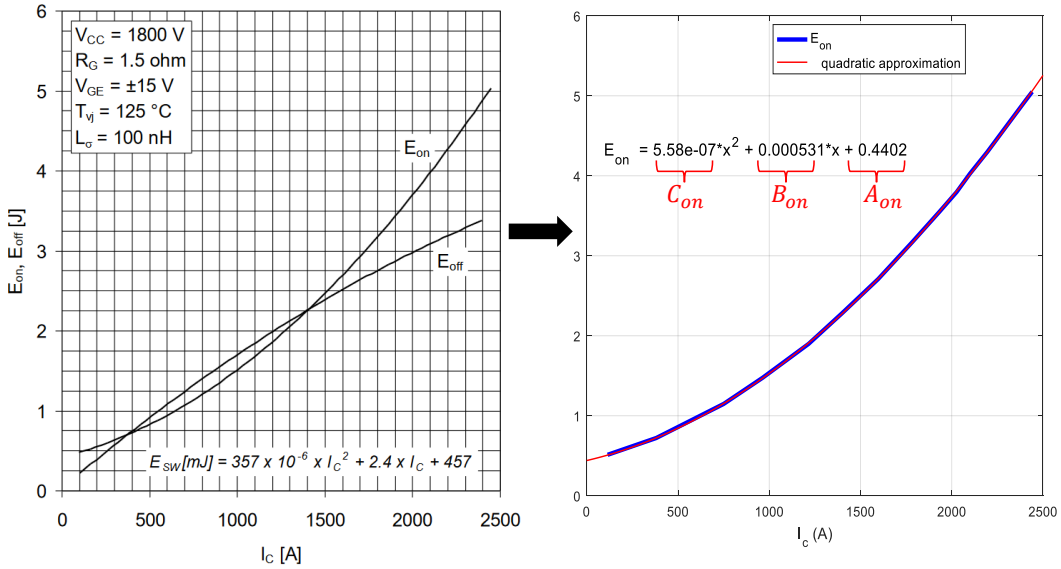


Fig. II-6. E_{on} datasheet parameters' extraction (ABB's 5SNA 1200E330100 IGBT)

For a switching frequency f_{sw} and a modulation period $T_{modulation}$, the switching losses are computed with:

$$P_{sw} = \frac{1}{T_{modulation}} \frac{1}{T_{sw}} \int_{t_1}^{t_2} \frac{V_{sw}}{V_{def}} E_{V_{def}}(I_{load}).dt \quad \text{(II-5)}$$

$$P_{sw} = f_{sw} * \frac{V_{sw}}{V_{def}} * (A \frac{\Delta sw}{T_{modulation}} + B * I_{sw_{average}} + C * {I_{sw_{rms}}}^2) \quad \text{(II-6)}$$

Where $I_{sw_{average}}$ and $I_{sw_{rms}}$ are respectively the average and RMS values of the switched load current, V_{sw} is the switched voltage of the semiconductor that depends on the topology, V_{def} is determined from the datasheet and is often equal to the half of the component voltage rating ($V_{def} = \frac{V_{rating}}{2}$). Δ_{sw} is the switching time interval $[t_1, t_2]$ in which the semiconductor switches ($\Delta_{sw} = t_2 - t_1$).

The previous equations for the conduction and switching losses are also valid for the diode, knowing that the diode has only recovery losses as switching losses. The total losses are the sum of conduction and switching losses for both IGBT and diode.

$$P_{total} = P_{cond} + P_{sw} \quad \text{(II-7)}$$

Because of the semiconductors losses, a thermal model is needed in order to determine and manage the chip temperature. As for the electrical circuit analysis, the thermal analysis integrates power sources which represent the losses, temperature at different nodes and thermal resistors depending on the thermal conductivity and chip sizes. This is a steady-state study so the thermal capacitances are not taken into account.

In our architecture, a single power switch contains a transistor with an antiparallel diode that ensures a path for the reverse current. So the thermal model circuit will include two thermal resistors as in Fig. II-7. Each resistor has a heat energy flow caused by the losses of each component. The temperatures of the different points in the switch package can be determined using the following equations:

$$T_{Transistor} = P_{losses_{transistor}} . R_{th_{jc}T} + T_{case} \quad \text{(II-8)}$$

$$T_{Diode} = P_{losses_{diode}} . R_{th_{jc}D} + T_{case} \quad \text{(II-9)}$$

$$T_{case} = (P_{losses_{transistor}} + P_{losses_{diode}}) . R_{th_{ch}} + T_{heatsink} \quad \text{(II-10)}$$

Where R_{th-jc} is the junction to case thermal resistance, R_{th-ch} is the case to heatsink thermal resistance and R_{th-ha} is the heatsink to ambient thermal resistance in K/W. Here, the heatsink to ambient resistance is not considered because of the fixed heat sink temperature (70°C - 90°C in our example). The used cooling system has a non-constant heatsink to ambient thermal resistance (R_{th-ha}) which makes it possible to set the heatsink temperature. This resistance is defined by the 4th work package evaporator conductance in function of the power losses per module as in Fig. II-7.

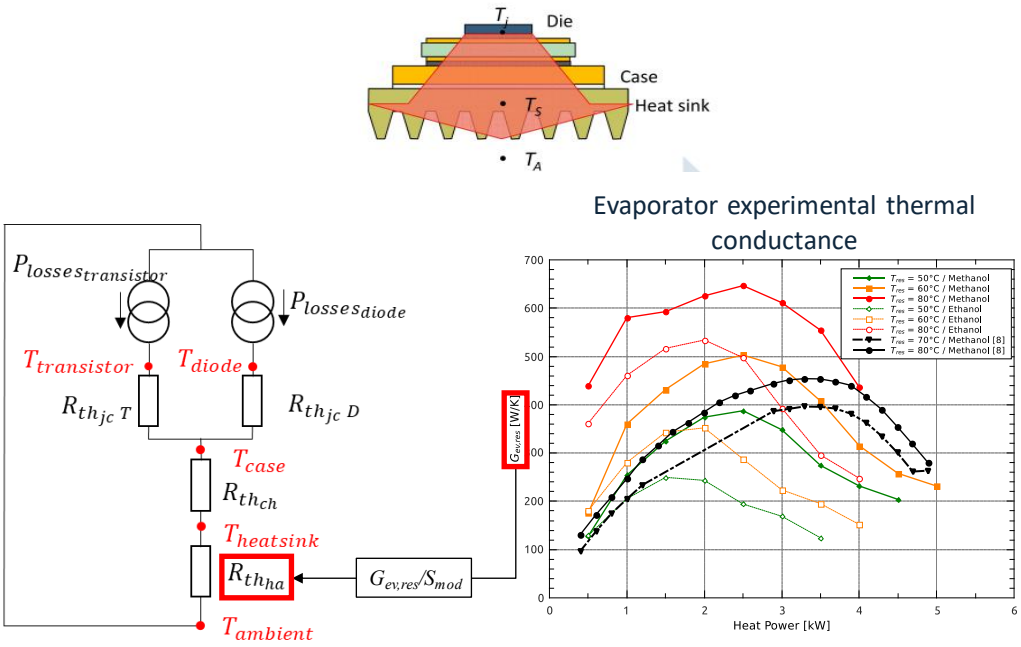


Fig. II-7. Equivalent thermal model of an IGBT component with antiparallel diode [30] [32]

ii. Needed parameters

In order to evaluate losses and components temperature, we need the following parameters:

- Thermal resistance: R_{th-jc_T}, R_{th-jc_D}, R_{th-ch}
- Conduction parameters for IGBT: V_{ce0} R_{dson}, and diode: V_d, R_d.
- Switching losses parameters (E_{on}, E_{off} et E_{rec}): A_x, B_x and C_x

- Component surface: Surface (mm^2) needed to calculate the heat flux in W/cm^2 in order to size the heat exchanger and the cooling system.

These parameters are extracted from semiconductor manufacturer datasheets and used to create the semiconductor database.

iii. Example of the method for determining the formulas of switching and conduction currents

To calculate the switching and conduction losses, the currents need to be defined. To find the conduction and switching losses, a simulation is done using *Plecs* to identify the switching intervals for each switch. In this part, an example will be shown to illustrate this method.

The output current absorbed by the source is supposed to be sinusoidal with a θ phase shift as in the equation (II-11). The considered load is a 3-phase electric motor model presented in Chapter I.

$$I_{out}(x) = \sqrt{2}I\sin(x-\theta), \quad x = \omega \cdot t \tag{II-11}$$

As a case study to show how to derive the currents values of a converter during its different mode of functionality, the 5-level ANPC architecture schematic shown in Fig. II-10 is considered. This topology will be studied in detail in the next chapter and it is used here to illustrate the power losses calculation method. The specificity of this converter is that it combines a 3-level FC one working at high frequency and a 2-level one working at a low frequency. The connection of both elements gives this ANPC five levels output voltage and an output frequency with a multiplication of two times the switching frequency. As Switcher semiconductors switch only half of one cycle of conduction phase at low frequency so the switching losses are lower than if it was switching at high frequency.

The current waveforms for each switch of the low and high frequencies part of the converter are shown in Fig. II-9. In this figure, only one semiconductor current waveform of the FC part is shown (T_1) due to the symetry of this topology. On the other hand, for the low switching frequency part, two semiconductors current waveforms are shown (T_5, T_6)and the other two remaining have similar waveforms.

This will help in the determination of the limits of the integrations used in the losses derivations equations and hence proper results as validated in the tables shown later in this chapter.

The command functions of the firing gates signal shown in Fig. II-9 are expressed by:

$$\text{3-level FC: } f(x)_{T_1,T_3} = 1 - f(x)_{T_2,T_4} = \begin{cases} k * sin(x), & 0 \le x < \pi \\ 1 + k * sin(x), & \pi \le x \le 2\pi \end{cases} \tag{II-12}$$

$$\text{Switcher: } f(x)_{T_5,T_7} = 1 - f(x)_{T_6,T_8} \begin{cases} 1, & 0 \le x < \pi \\ 0, & \pi \le x \le 2\pi \end{cases} \quad \text{(II-13)}$$

With k the modulation index.

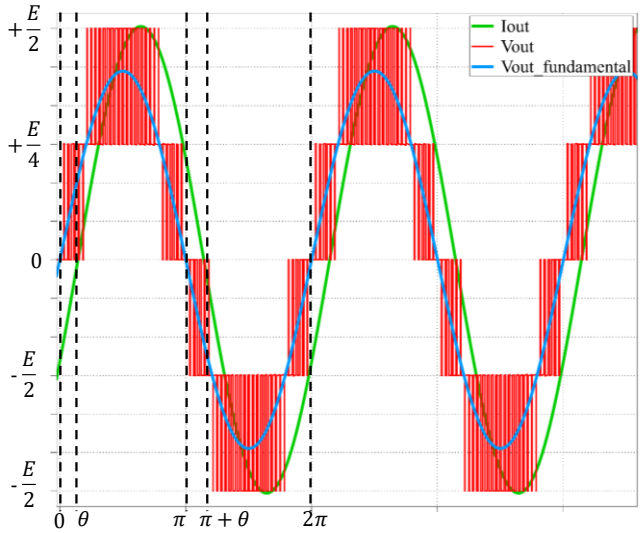


Fig. II-8. Output voltage & current waveforms of a single phase 5-level ANPC obtained by *Plecs* simulation

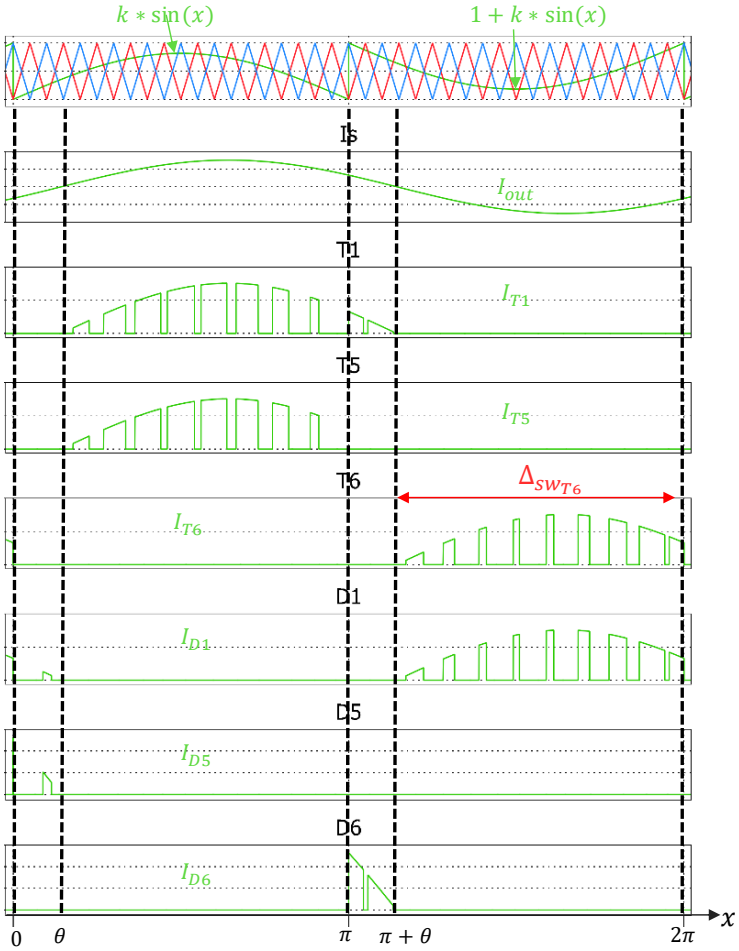


Fig. II-9. Waveforms of ANPC semiconductors commands and currents obtained by simulation in *Plecs*

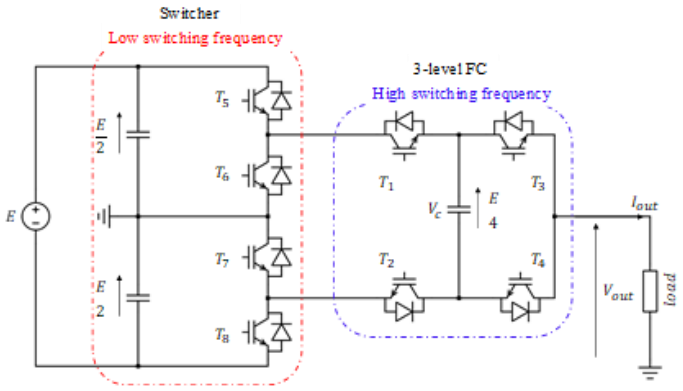


Fig. II-10. ANPC 5L Converter schematics: 3-level FC + Switcher (2-level, DC)

TABLE II-1 summarizes the operation properties of ANPC converter with its characteristics and function modes durations which are issued from the simulation current waveforms.

TABLE II-1. Current distribution during an operating period

Current Direction	Active components	Intervals	Output Voltage
$I_{out} > 0$	T_1, T_3, T_5	$[\theta, \pi + \theta]$	$+E/2$
	T_1, T_5, D_4	$[\theta, \pi]$	$+E/4$
	T_3, D_2, D_8	$[\pi, \pi + \theta]$	$-E/4$
	T_1, T_3, D_6	$[\theta, \pi]$	0
$I_{out} < 0$	T_4, T_2, D_7	$[\pi + \theta, 2\pi + \theta]$	0
	T_2, T_8, D_3	$[\pi + \theta, 2\pi]$	$-E/4$
	D_1, T_4, D_5	$[0, \theta]$	$+E/4$
	T_2, T_4, T_8	$[\pi + \theta, 2\pi]$	$-E/2$

Following the formulas presented in the previous section with the help of the waveforms shown in Fig. II-9; the calculations for average & RMS conduction and switching currents for each semiconductor can be found appendix 1. For more converters topologies waveforms simulation results and currents derivations, they could be found in [2] and [4] and could be resumed in the appendix.

3. Semiconductors Database

The simulation tool uses a created database that sums up the semiconductors technological parameters obtained from the manufacturer datasheets. The components are classified as families according to their manufacturer. In this case, only Silicon IGBT components are studied in the first part of the project.

Our work package (WP2) focuses on the static converters and the DC bus design. In order to help the work of the other work packages of the project, a first step is to determine an optimal DC bus voltage range. This will have a direct impact on the study of partial discharges but also in the design of motor windings. Then, it is necessary to compare the efficiency and power density of several multilevel topologies. Using the simulation tool and the available database, the efficiency is plotted for 2-level inverter in green in Fig. II-11 and the used voltage calibers are reported below the efficiency curves. The noticed jumps of efficiency are due to the change in the used component voltage calibers. These jumps are also present for the other studied topologies as noticed in Fig. II-11.

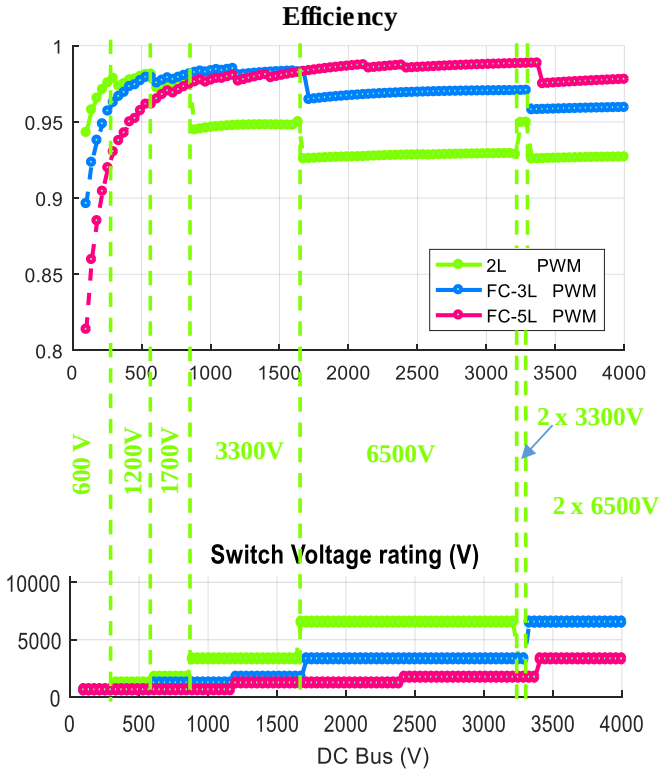


Fig. II-11. Efficiency for several topologies using available database components

Therefore, it is made difficult to find the optimal DC bus voltage due to the discretization of available voltage ratings. To overcome this problem, we created a continuous components database that suits the needed voltage rating by fitting and extrapolating the existing database components. Of course, these components may never exist, but it allows to see the effect of the choice of static conversion architecture on the efficiency over the voltage range considered while removing a bias (discretization of ratings).

This solution will help us explore several possible solutions. Validation of the results will be done by simulation so as not to limit the number of proposed architectures. The experiment will be done in a second time, after this project, to verify the solutions that will come from the overall optimization.

For these study cases, the switching frequency is chosen in order to eliminate subharmonics components. Therefore, it should be higher than 7 times the fundamental frequency as stated in [33]. In our case, the switching frequency was set to 4 kHz which represents about 7 times the electric machine fundamental frequency.

i. Components' families

Semiconductor manufacturers can offer relatively low IGBT devices rates but can reach as high as 6.5 kV/0.75 kA.

As shown in Fig. II-12, the used database has two families of silicon components. The first consists of ABB components with four available voltage ratings (1700 V, 3300 V, 4500 V, and 6500 V). Current ratings vary from 250 to 1600 A.

The second family is made up of Infineon components whose voltage ratings are: 600 V, 1200 V, 1700 V, 3300 V and 6500 V. For current calibers, they are smaller than those of the previous family and range from 200 to 800 A.

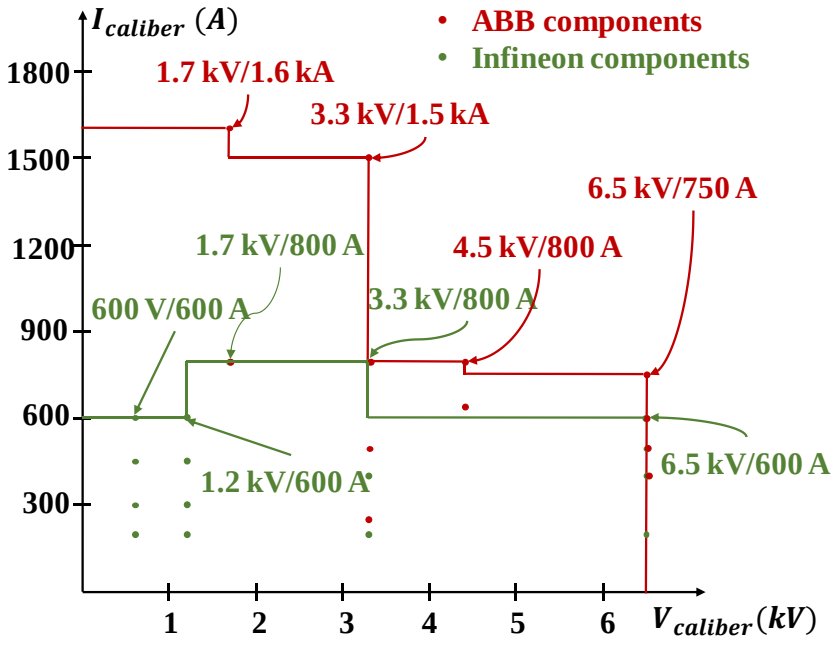


Fig. II-12. Voltage and current ratings of semiconductor devices in the database

ii. Generated components

There are discontinuities in the first resulted curves (Fig. II-11) due to the discretization of the components shown in Fig. II-12. These jumps are due to the change in component size used since the selected family (ABB components, for example) has a limited number of calibers (1700 V, 3300 V, 4000 V, and 6500 V).

The manufacturer does not make a customized component. However, using discrete components in our simulation brings up jumps in the resulted performances curves which will

be problematic for the global system optimization. Since it is an exploratory study, it is interesting to have components for all voltage and current ratings which will involve determining component parameters for sizes that vary continuously. In order to have a continuous database, we have to create components for the different desired ranges. The user will still have the choice of using real components instead of the created ones.

To create a component that does not exist in our database, we first select the family or manufacturer to which the created component will belong. For this purpose, all the parameters of the components belonging to this family are extracted from the *Matlab* file. The closest voltage and current ratings components are selected to be used in the extrapolation.

Once the various components have been selected, they will be used to generate the parameters of the desired component. The laws of variation of all the parameters are then identified as a function of the voltage caliber or current-voltage calibers product as stated in TABLE II-2 and then applied to the desired one.

TABLE II-2. Needed parameters dependency

Generated parameter	**Depending parameter**
Switching losses parameters A_x, B_x and C_x	Voltage rating
Conduction parameters for IGBT and Diode V_{ce0} R_{dson}, V_d, R_d.	Voltage rating * Current rating
Thermal resistance R_{th-jc_T}, R_{th-jc_D} and R_{th-ch}	Voltage rating * Current rating
Surface	Voltage rating * Current rating

For the switching energies E_{on}, E_{off} and E_{rec}, we can model the variation of their parameters (A_x, B_x, and C_x seen in equation (II-4)) using a polynomial function which is the function that fits the best our data as in Fig. II-13. Variation of Aon, Bon et Con versus voltage rating and E_{on} versus the current In this figure, the blue asterisks stand for the real components parameters and the red curve the approximation function. Variation of Aon, Bon et Con versus voltage rating and Eon versus the current. Second-degree polynomial functions are chosen because we do not have enough points in order to pick higher degree polynomial functions. In the fourth figure, the turn-on energy is plotted using both real and generated components and as noticed, our approximation fits well the real components and allows to go beyond the available current and voltage ratings.

The same method is used to generate the IGBT and the diode, we need the on-state voltage drop at zero current condition and resistive elements and the thermal resistors (heatsink-case, junction-case for both transistor and diode) as a function of the voltage and current calibers.

In order to generate the surface of the component, we search for a function that fits the variation of this parameter depending on the current-voltage calibers. We can approximate this parameter

also with a polynomial function. The value of the created component surface will be very helpful to design the cooling system allowing the computation of the thermal density.

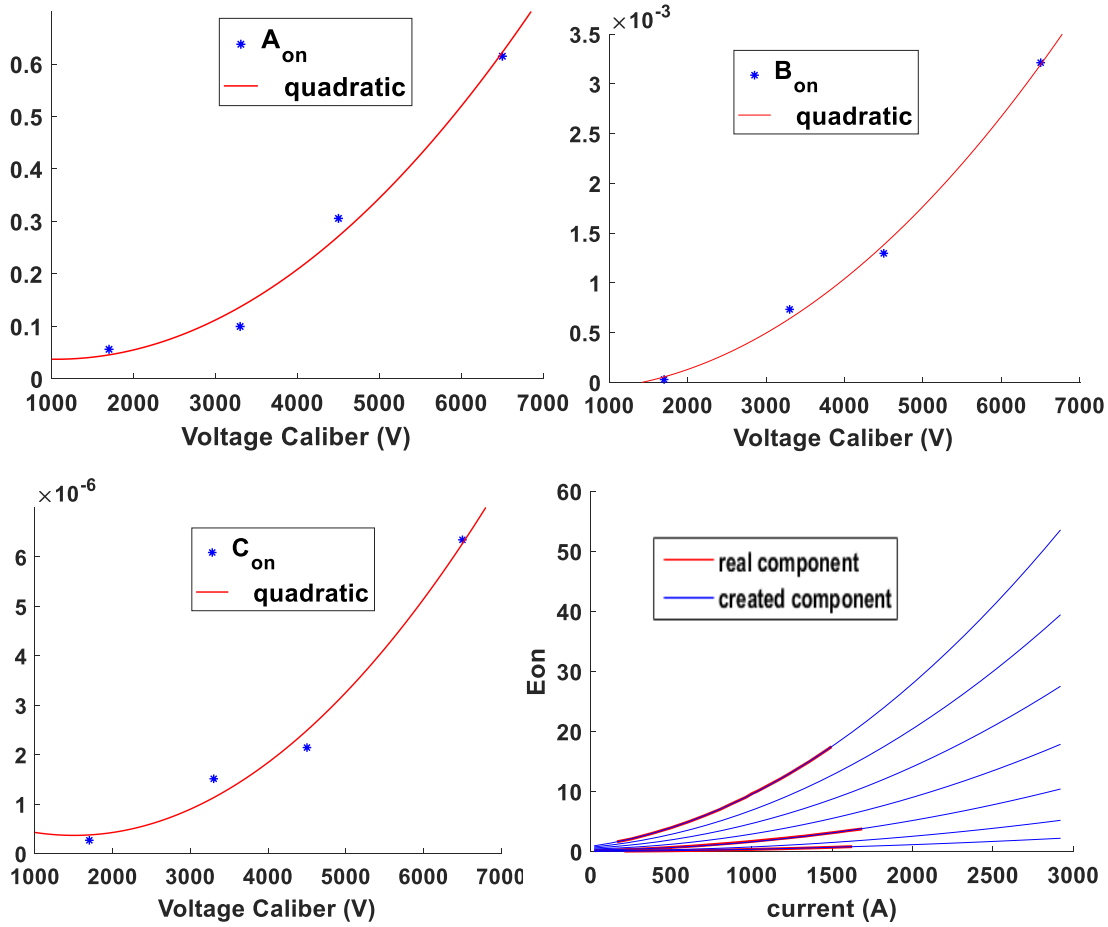


Fig. II-13. Variation of Aon, Bon et Con versus voltage rating and E_{on} versus the current

TABLE II-3 summarizes the order of the polynomial functions for the different parameters modeled.

TABLE II-3. Summary of generated parameters

Generated parameter	**Depending parameter**	**Approximation function**
Switching losses parameters A_x, B_x and C_x	Voltage rating	Second-degree polynomial $f(x) = ax^2 + bx + c$
Conduction parameters for IGBT and Diode V_{ce0} R_{dson}, V_d, R_d.	Voltage rating * Current rating	First-degree polynomial $f(x) = ax + b$
Thermal resistance R_{th-jc_T}, R_{th-jc_D} and R_{th-ch}	Voltage rating * Current rating	Second-degree power $f(x) = ax^b + c$
Surface	Voltage rating * Current rating	First-degree polynomial $f(x) = ax + b$

The generated semiconductor components will make it possible to compare the different parameters of the studied topologies in order to choose the optimum voltage range which will minimize the losses and increase the power density.

These generated components will be useful for the global hybrid-electric propulsion system optimization which will be done by the 6th work package.

iii. Comparison of real and generated components

The first studies will verify that the results with the generated components are coherent with the ones obtained with the real components. A DC voltage sweep is carried out using Infineon components and the component choice is fixed manually in the simulation tool. Due to the limitation of the existing voltage calibers, the sweep range is limited to 4000 V due to the limitation of the existing components' voltage calibers which corresponds to 6500 V so a definition voltage of 3600 V using a 2-level inverter topology. The power is fixed to 1 per unit.

With these generated components, several options are available. The first one could be setting a voltage and current calibers which will be done in the first test in order to compare these components to the real ones. The second option is to set only the voltage rating so the direct series association would be allowed and using the adapted current rating in order to avoid parallel association. The third one consists of generating adapted voltage and current rating components and compare them to the case of using only available components calibers associated in series and parallel so to withstand the needed voltage and current required by the load.

1. Fixed component choice

For this study case, the voltage and current calibers are fixed for both real and generated components in order to check the validity of the generated components and also compare the impact of component calibers on the inverter performances. Real and generated with same calibers, side-by-side, will be compared under the same conditions. Both components calibers are fixed for both real and generated components. Fig. II-14 represents the efficiency for fixed components allowing direct series association.

In order to have the adapted component, series and parallel connection are made if the needed component ratings are beyond the available current and voltage rating. The series connection is used to adapt the input voltage while the parallel connection is needed to adapt the current of the transferred power.

For the tested components, the generated components have the same properties as the real ones. The difference between components conduction losses remains low compared to switching losses which is higher for larger voltage caliber components.

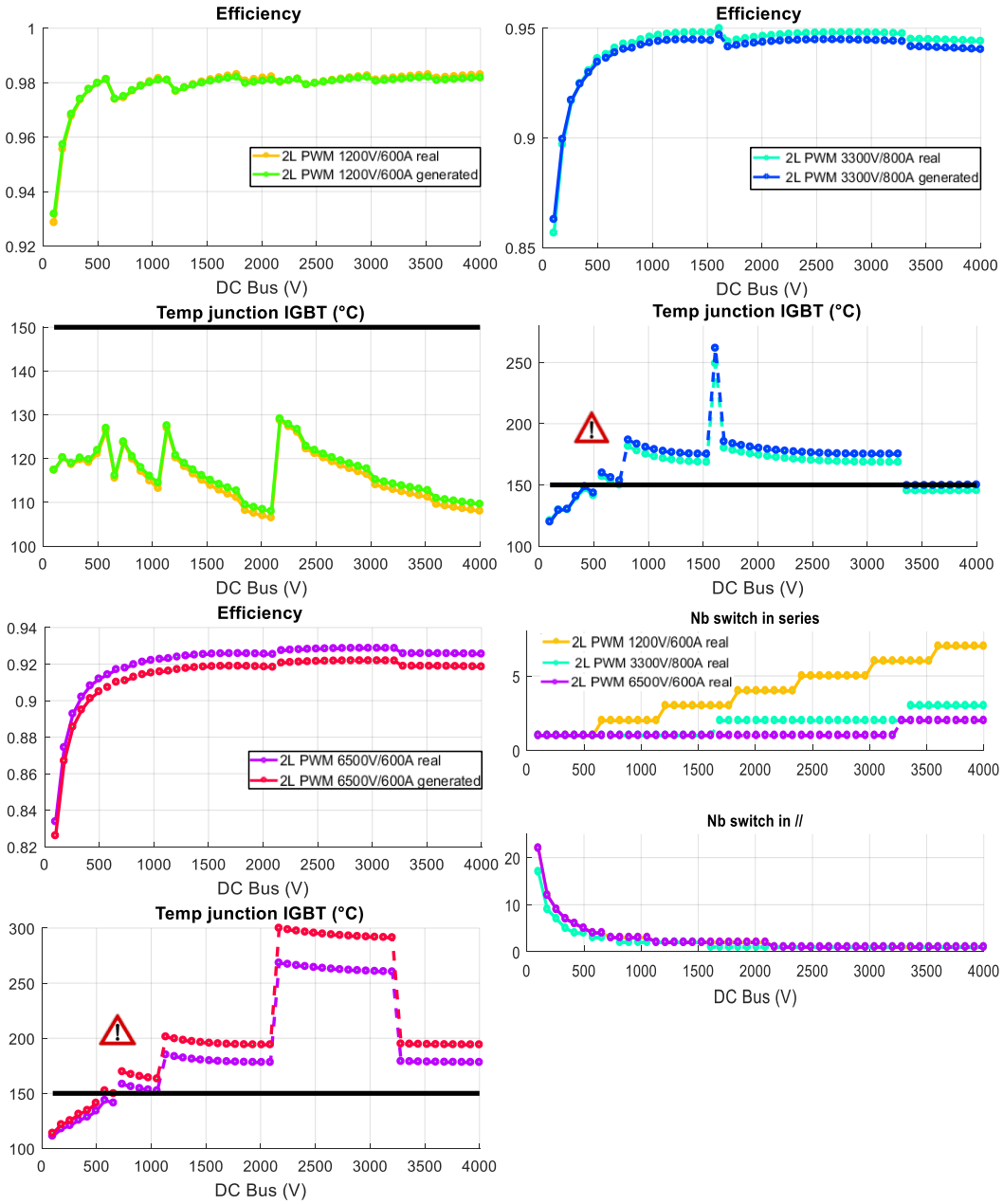


Fig. II-14. Real versus generated components efficiencies, maximal junction temperatures and parallel and series associated switches number for fixed calibers

2. *Fixed choice of the components' voltage caliber and adapted current*

For the next simulation, the voltage calibers are fixed however the current ones are chosen in order to respond to the needed current with both real and generated components, so the last ones will always have good use of the Silicon surface. In this case, the real components are used at their nominal current.

In this case, the real components have smaller thermal density due to the surface of the component which is bigger than the generated components ones. The bigger surface is, the lowest the current density is so the component junction temperature will be lower.

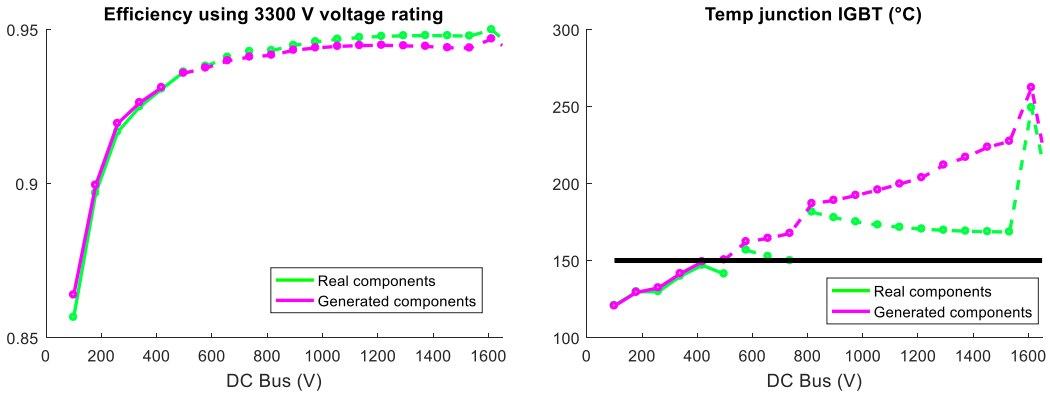


Fig. II-15. Real versus generated components efficiencies and maximal junction temperatures for fixed voltage calibers and adapted current calibers

The jumps noticed for the temperature of the generated components are mainly due to the thermal resistor which does not correspond to the optimal value. The generated components have a higher thermal resistance as shown in Fig. II-16. This is linked to the distribution of the thermal resistances that do not follow an obvious mathematical law. This data spread is related to the gap between the selected components which result in noise, sampling errors and nonlinearity of the distribution law.

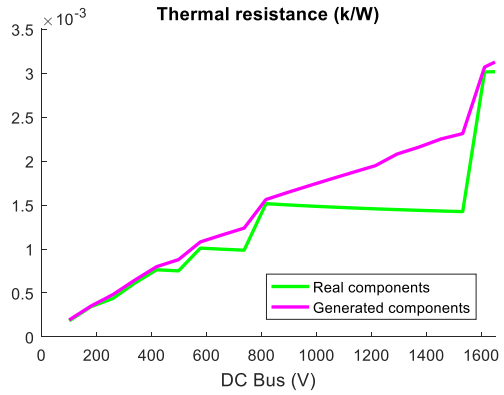


Fig. II-16. Thermal resistance for real and generated used components

In order to see the effect of the current caliber, the efficiency and maximal junction temperature are plotted as function of the power (Fig. II-17). The 3300 V components were used for a DC bus of 1600 V so to be used at 48% of their rating.

The current rating variation is not as important as the voltage one in terms of efficiency jumps. However, it has a great effect on the thermal resistances and therefore the maximal junction temperature.

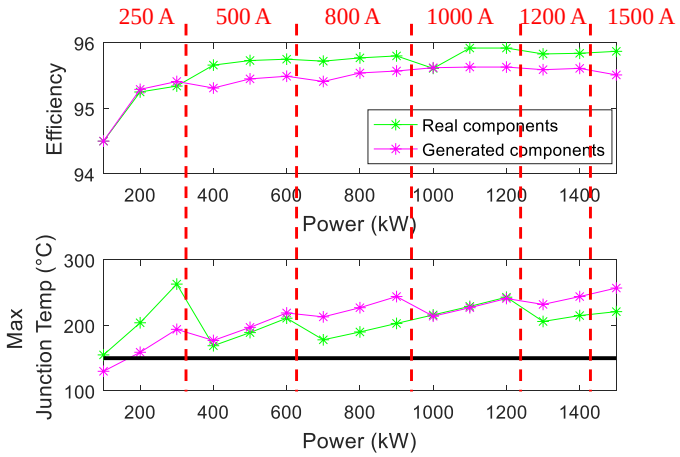


Fig. II-17. Efficiency and maximal junction temperature for real and generated 3300 V components for a power sweep

3. *Adapted voltage and current calibers*

For the third case, the voltage and current calibers are chosen in order to respond to the needed voltage and current to both real and generated components.

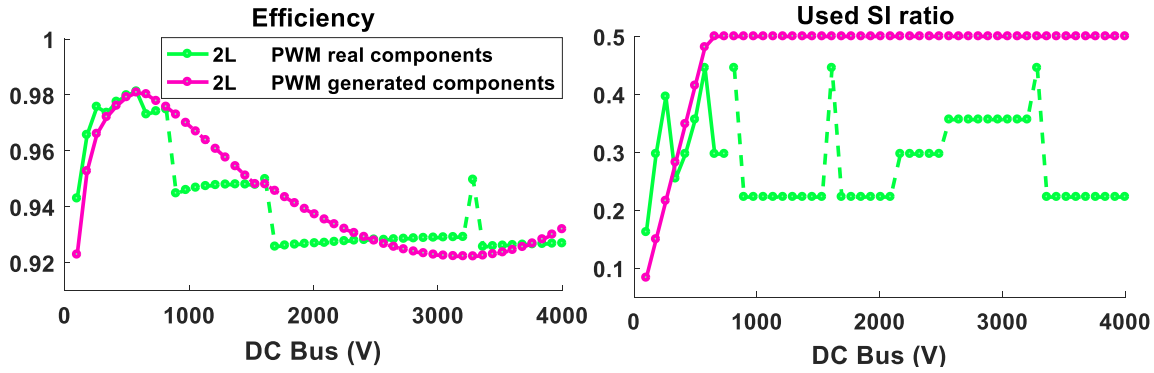


Fig. II-18. Real versus generated components efficiencies and used Silicon ratio for adapted voltage and current calibers

The very high switching losses and maximal junction temperature for the first points of the simulation are due to the very low voltage calibers (100 to 500 V) that are lower than the smallest available caliber which is 600 V.

The efficiency curves overlap for the points that match a used Silicon ratio of 50% for the real components. This ratio is computed as follows:

$$Used_{Si_{ratio}} = \frac{V_{DC_{bus}} * I}{n_{switch} * \frac{V_{caliber}}{2} * I_{caliber}} \quad \text{(II-14)}$$

Where $V_{DC_{bus}}$ is the DC bus voltage, I is the load current, n_{switch} is the number of the used switches depending on the studied topology.

The generated components are optimized in order to use 50% of the installed Silicon (50% of voltage rating and 100% of current one) since the recommended ratio is between 50 % and 70 % so to have an optimal efficiency and an acceptable over-voltage. The same remarks about the junction temperature can be made again.

The generated components can be used to replace the real components in our study so to avoid the efficiency jumps. Although these jumps could still be present for the maximal junction temperature.

These components will be used for to define the optimal DC bus voltage to use for each multilevel topology in Chapter III.

4. Capacitor sizing

Capacitors are key components of the power electronics that are used as part of the electric motor drive system. In the state of the art inverters, the capacitors are the largest components and essentially determine the inverter volume. Consequently, an increase in the energy storage density of capacitors would have a huge impact on the size and power density of power electronics.

The capacitor value could be calculated from the stored energy as shown in the following equations.

$$Energy = \frac{1}{2}\frac{Q^2}{C} = \frac{1}{2}\,CV^2 \tag{II-33}$$

$$Q = CV \tag{II-34}$$

But $\Delta Q = I\Delta t$, then

$$I\Delta t = \mathrm{C}\Delta V \quad \Rightarrow \frac{I}{f} = C\Delta V \tag{II-35}$$

$$C = \frac{I}{f*\Delta V} \tag{II-35}$$

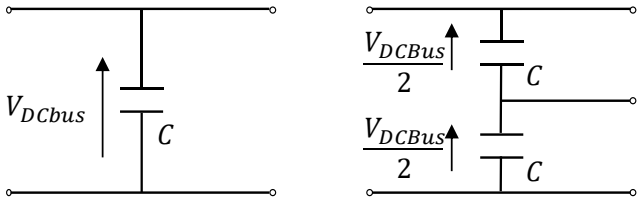
To define the capacitance value, the current, frequency and voltage ripples are needed. In this part, the capacitor current will be evaluated for two capacitor types. The first one is the DC bus capacitor that is needed by all the topologies and the second one is the flying capacitor which is used in some 3-level and 5-level topologies. These capacitors are selected form an available database according to a selection process detailed below.

i. DC bus capacitor

Picking a DC link capacitor is decided by two constraints: one is the capacitance which is determined by the voltage ripple, the other one is the RMS current ripple across the capacitor

for the worst case, which will cause the capacitor internal temperature rise and has to be under a certain value to ensure the proper operation of the capacitors. This ripple depends on the switching depending on the control type (with or without homopolar injection), modulation index, frequency and the load phase.

Therefore, an algorithm was developed to estimate the worst case, assuming that the filtering is perfect and that only the non DC part goes through the capacitor. There are two types of DC bus capacitor depending on the used inverter topology. The first one is the 2-level type capacitor and the second one is the NPC one as in Fig. II-19.



2-level type inverter NPC type inverter

Fig. II-19. DC bus link types

The sizing method is similar for both cases; however, the current calculation is not. The used method to find out the capacitor value is described in detail in [34]. The algorithm developed determines the worst case. It scans different parameters: the load phase (0° to 90°), modulation depth from 0 to 1.15 and zero-sequence control strategies (nothing, harmonic 3, SVM).

In order to choose the most appropriate component from the datasheet, the capacitor current is needed. The RMS current in the DC bus capacitors is analytically calculated for sine wave output currents with arbitrary phase shift angles $\mathrm{acos}(P_f)$ and modulation factors k. With pulse width modulation (PWM), the three sinusoidal desired curves are compared with the triangle modulation one.

For both cases, the capacitor RMS current value could be calculated using the inverter average and RMS currents as follows:

$$I_{capa_{RMS}} = \sqrt{I_{inv_{RMS}}^2 - I_{inv_{avg}}^2} \tag{II-15}$$

For the first DC bus type, according to [34] the capacitor RMS current can be calculated as follows:

$$I_{inv_{avg}} = \frac{3}{4}\sqrt{2} I_{out_{rms}} k * P_f \tag{II-16}$$

$$I_{inv_{RMS}} = \sqrt{2} I_{out_{rms}} \sqrt{\left(\frac{\sqrt{3}k}{4\pi}\right) * (1 + 4 * P_f^2)} \tag{II-17}$$

With $I_{out_{rms}}$ the inverter output RMS current imposed by the 3-phase electric motor.

From equations (II-16), (II-17) and (II-18), the capacitor current is defined in equation (II-18).

$$I_{capa_{RMS}} = \sqrt{2}\, I_{out_{rms}} \sqrt{\sqrt{3}\frac{k}{4\pi} + (\sqrt{3}\frac{k}{\pi} - 9 * \frac{k^2}{16}) * P_f^2} \quad \text{(II-18)}$$

For the second DC bus type, for each angular sector $\frac{\pi}{3}$, we look at one switch current in each phase knowing that the inverter current is the composition of the three (Fig. II-20) and are represented in the following equations by functions f_1 to f_6. To obtain the RMS value, the

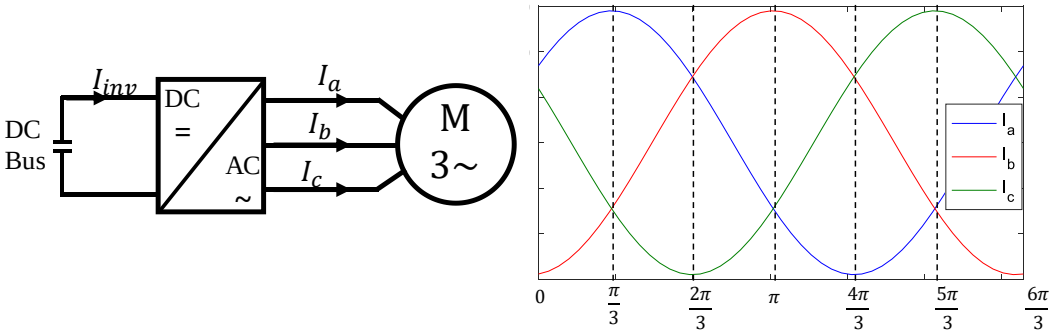


Fig. II-20. Inverter input and output currents

square currents are then modulated by taking into account the double product.

The RMS and average current values depend on the 3 phases currents (I_a, I_b, I_c), the modulation index and ω the electric pulsation or the frequency.

$$I_{inv_{RMS}} = \sqrt{\frac{1}{2\pi} * (\int_0^{\frac{\pi}{3}} f_1 + \int_{\frac{\pi}{3}}^{\frac{2\pi}{3}} f_2 + \int_{\frac{2\pi}{3}}^{\pi} f_3 + \int_{\pi}^{\frac{4\pi}{3}} f_4 + \int_{\frac{4\pi}{3}}^{\frac{5\pi}{3}} f_5 + \int_{\frac{5\pi}{3}}^{\frac{2\pi}{3}} f_6)} \quad \text{(II-19)}$$

The six $\frac{\pi}{3}$ sectors currents are defined by the following functions:

$$f_1 = k * (I_a^2 * sin(\omega t) + I_c^2 * sin(\omega t - 4\pi/3) + 2 * (I_a * I_c) * sin(\omega t) * k * sin(\omega t - 4\pi/3)) \quad \text{(II-20)}$$

$$f_2 = k * I_a * sin(\omega t) \quad \text{(II-21)}$$

$$f_3 = k * (I_a^2 * sin(\omega t) + I_b^2 * sin(\omega t - 2\pi/3) + 2 * (I_a * I_b) * sin(\omega t) * k * sin(\omega t - 2\pi/3)) \quad \text{(II-22)}$$

$$f_4 = k * I_b^2 * sin(\omega t - 2\pi/3) \quad \text{(II-23)}$$

$$f_5 = k * (I_c^2 * sin\left(\omega t - \frac{4\pi}{3}\right) + I_b^2 * sin\left(\omega t - \frac{2\pi}{3}\right) + 2 * (I_b * I_c) * sin\left(\omega t - \frac{4\pi}{3}\right) * (k * sin(\omega t - 2\pi/3)) \quad \text{(II-24)}$$

$$f_6 = k * I_c^2 * sin(\omega t - 4\pi/3) \quad \text{(II-25)}$$

Now, the average current will be calculated. It could be calculated using each function above in the right section over one period $[0\ ,2\pi]$.

$$I_{inv_{avg}} = \frac{1}{2\pi} * (\int_0^{\frac{\pi}{3}} f_{1_{avg}} + \int_{\frac{\pi}{3}}^{\frac{2\pi}{3}} f_{2_{avg}} + \int_{\frac{2\pi}{3}}^{\pi} f_{3_{avg}} + \int_{\pi}^{\frac{4\pi}{3}} f_{4_{avg}} + \int_{\frac{4\pi}{3}}^{\frac{5\pi}{3}} f_{5_{avg}} + \int_{\frac{5\pi}{3}}^{2\pi} f_{6_{avg}}) \quad \text{(II-26)}$$

The used function $f_{1_{avg}}$ to $f_{6_{avg}}$ are as follows:

$$f_{1_{avg}} = k * (I_a * sin(\omega t) + I_c * sin(\omega t - 4\pi/3)) \quad \text{(II-27)}$$

$$f_{2_{avg}} = k * (I_a * sin(\omega t)) \quad \text{(II-28)}$$

$$f_{3_{avg}} = k * (I_a * sin(\omega t) + I_b * sin(\omega t - 2\pi/3)) \quad \text{(II-29)}$$

$$f_{4_{avg}} = k * (I_b * sin(\omega t - 2\pi/3)) \quad \text{(II-30)}$$

$$f_{5_{avg}} = k * (I_c * sin(\omega t - 4\pi/3) + I_b * sin(\omega t - 2\pi/3)) \quad \text{(II-31)}$$

$$f_{6_{avg}} = k * (I_c * sin(\omega t - 4\pi/3)) \quad \text{(II-32)}$$

For example, for a 3-level NPC inverter with a 2 kV DC bus and 1024 A RMS output current, the inverter currents are as follows in TABLE II-4. The RMS capacitor current obtained using the previous equations with the inverter simulation current values equals to 547 A versus 521 A obtained by using *Plecs* simulation. This difference is due to *Plecs* RMS measure which is discrete in *Plecs* so the results varies with the sample number. Yet, the obtained values using the analytic analysis are comparable to the *Plecs* ones.

TABLE II-4. Inverter and capacitor currents calculation comparison

	Analytic analysis	**Plecs simulation**
$\boldsymbol{I_{inv_{avg}}}$ **(A)**	740.73	742.1
$\boldsymbol{I_{inv_{RMS}}}$ **(A)**	852.76	922
$\boldsymbol{I_{capa_{RMS}}}$ **(A)**	422.51	521

ii. Flying capacitor

If the used converter structure needs flying capacitors to maintain a proper blocking voltage sustained by the power switches in order to have a correct output voltage, these capacitors could be sized according to the stored energy. So normally the nearest capacitor to DC bus is the largest one. However, for an industrial point of view, a hypothesis is taken to have the same flying capacitance for all capacitors within the architecture. It could also be sized according to the ripple voltage across the capacitor ($\Delta V_{C_{FY}} \approx 10\%$).

The flying capacitor sees only switching frequency current harmonic components so it is sized using this frequency.

$$C_{FY} = \frac{I_{out\_max}}{\Delta V_{C_{FY}} * V_C * f_{sw}} \tag{II-36}$$

The value V_C depends on the converter topology, and here is taken to be equal the value of the nearest capacitor voltage in the topology as stated before. TABLE II-5 summarizes the values of the worst case V_C for different topologies which are in the scope of our study.

TABLE II-5. Summary of flying capacitor number and voltage value

Topology	**Number of C_{FY}**	**V_C(largest)**
FC N Cells	$N-1$	$(N-1)E/N$
SMC $n \times p$ /6 SWs	$(n-1) \times p$	$(n-1)E/(n \times p)$
SMC $n \times p$ /4 SWs	$(n-1) \times p$	$(n-1)E/(n \times p)$
ANPC including (FC N Cells)	$N-1$	$(N-1)E/N/2$

The capacitor sizing was validated by comparing our results to the *Powerforge* [35] which is a software based on frequency analysis.

iii. Selecting the capacitor from the database

To select the adapted capacitor from the available database two methods are possible. The first one consists of using the capacitor total energy and the second one depends on the required voltage and current.

If the first method is chosen, according to the manufacturer's data, the coefficients K_{vol} and K_{weight} can be defined by the following equations.

$$\begin{cases} Volume\ (cm^3) = \frac{1}{2} \cdot C(\mu F) \cdot V^2 \cdot K_{vol} \\ Weight\ (kg) = \frac{1}{2} \cdot C(\mu F) \cdot V^2 \cdot K_{weight} \end{cases} \tag{II-37}$$

These coefficients are almost constant for a given technology depending on the operating frequency (high or low frequency). So a customized capacitor could be easily made by the manufacturer, unlike the semiconductors.

The sizing algorithm will give a desired capacitor value C_{des} and an operating voltage V_{des}. If these ranges are not available, series or parallel associations will be made.

To withstand the maximum RMS current through the capacitor, a parallel connection is needed as in equation (II-38).

$$n_{p_C} = \frac{I_{rms}}{I_{rms,max;\,DataSheet}} \tag{II-38}$$

It is necessary that the capacitor should be able to hold an overvoltage of $(1 + \Delta V_C) * V_{DCbus}$ before its breakdown. The data sheet covers a range of maximum capacitor voltage up to 3000V. So to overcome a needed overvoltage higher than 3000V, a series connection of small standard capacitors can be implemented, and so form a bank capacitor association as shown in Fig. II-21.

$$n_{s_C} = \frac{V_C}{V_{C,max;\,DataSheet}} \tag{II-39}$$

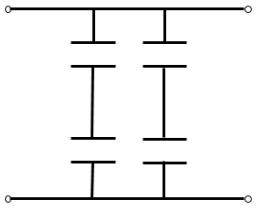


Fig. II-21. Series and parallel capacitor association

As the value of C is known, the next step is to look for a proper capacitor technology in the capacitor file that includes different capacitors datasheets and their tendencies. The foreseen technologies of the capacitors are Film Capacitors (Polypropylene (PP), Polyethylene Terephthalate Polyester (PET), etc.…). This step is done manually, hence increasing the degree of freedom of the designer for the choice of C. The calculation will then indicate values for the size and volume of the chosen capacitor(s).

If the desired voltage exceeds the range, n_s capacitors are put in series of the value $n_s * C_{des}$ in order to keep the same capacitance value. The capacitors will see a voltage V_{des} divided by ns. To ensure the capacitance, parallel association may also be used. This gives total energy of:

$$E_{tot} = n_s * \tfrac{1}{2} n_s \cdot C_{des} \left(\frac{V_{des}}{n_s}\right)^2 = n_p * \tfrac{1}{2} \cdot \frac{C_{des}}{n_p} V_{des}^2 = \tfrac{1}{2} C_{des} \cdot V_{des}^2 \tag{II-40}$$

5. Model validation using *Plecs*

In order to validate the converters losses' models, the results obtained with the *Matlab* tool are compared to *Plecs* simulations. To simulate converters in *Plecs*, we use the components from

the same database as for the *Matlab* tool. It allows having the same data on *Matlab* and *Plecs* so to compare the results of both tools. Then we compare the results for different topologies. For the *Plecs* simulations, we have the same assumptions as for the analytic analysis.

As an example, the results will be compared using the following parameters, which does not correspond to our specification.

- DC bus voltage : 600 V
- I_out_rms : 214 A
- Switching frequency : 5 kHz
- modulation depth : 0.8165
- power factor : 0.9
- Used component : FF300R06KE3 (600 V, 300 A)

TABLE II-6. 2-level power losses comparison using analytic analysis (*Matlab*) and *Plecs* simulation

2-level	Switching losses (W)		Conduction losses (W)	
	Matlab	*Plecs*	*Matlab*	*Plecs*
IGBT	145	145.37	114.67	114.8
Diode	111	111.23	28.85	28.88

We note in TABLE II-6 that we have the same losses unlike the results of the study carried out in [2] which did not give the same losses by conduction. This error was due to not using identical components losses parameters on *Matlab* analytic analysis and *Plecs*.

For the other used topologies that will be presented in detail in the next chapter, the power losses analytic analysis was validated for several points and case scenario using *Plecs* simulation.

i. Multilevel Flying Capacitor topology (FC):

For this topology, we will compare the results for different number of FC cells. The first one to be simulated is a 3-level FC with the same parameters as for the 2-level presented above.

TABLE II-7. 3-level FC power losses comparison using analytic analysis (*Matlab*) and *Plecs* simulation

3-level FC	Switching losses (W)		Conduction losses (W)	
	Matlab	*Plecs*	*Matlab*	*Plecs*
IGBT	26	26.25	113	112.94
Diode	12.04	12.01	27.22	27.25

Similar results with both tools are noticed for both cases.

Secondly, a 5-level FC is simulated keeping the same parameters as for the FC 3 levels with a switching frequency of 2.5 kHz (10 kHz/4 switching cells) to keep an apparent frequency of 10 kHz.

TABLE II-8. 5-level FC power losses comparison using analytic analysis (*Matlab*) and *Plecs* simulation

5-level FC	Switching losses (W)		Conduction losses (W)	
	Matlab	*Plecs*	*Matlab*	*Plecs*
IGBT	6.55	6.65	113	112.95
Diode	3.01	2.95	27	27.26

Then, a 7-level FC is simulated keeping the same parameters as for the previous case with a switching frequency of 1.67 kHz (10 kHz/6 switching cells).

TABLE II-9. 7-level FC power losses comparison using analytic analysis (*Matlab*) and *Plecs* simulation

7-level FC	Switching losses (W)		Conduction losses (W)	
	Matlab	*Plecs*	*Matlab*	*Plecs*
IGBT	2.91	2.97	113	112.92
Diode	1.34	1.29	27	28.02

For the FC topology overall, the results are similar in both cases and allow validating the analytical analysis carried out with *Matlab*.

ii. 3-level Neutral clamped point topology (NPC):

For the 3-level NPC topology, we used the same case-study as for the FC using the FF450R06ME3 (600 V, 450 A) switch and 10 kHz as the switching frequency.

TABLE II-10. 3-level NPC power losses comparison using analytic analysis (*Matlab*) and *Plecs* simulation

3-level NPC	Switching losses (W)		Conduction losses (W)	
	Matlab	*Plecs*	*Matlab*	*Plecs*
Clamping Diode	20	20.3	49	49.54
IGBT (outer)	54	53.8	71	70.95
Diode (outer)	1.15	1.91	0.63	0.63
IGBT (inner)	4.14	4.25	118	118.23
Diode (inner)	0.77	1.88	0.63	0.63

For this topology, we notice that there is an imbalance between the diodes' losses because the analytical analysis considers that the diodes see an $\frac{E}{2}$ voltage during the overlap, which is not

the case in *Plecs* simulation. In the simulation, the closest diode to the current source (Inner Diode) sees $0.2 \times E$ while the other one (Outer Diode) sees $0.3 \times E$.

We changed the switching voltages on the *Matlab* file for the diodes in order to match the *Plecs* ones and we got the following results:

TABLE II-11. 3-level NPC outer diode switching losses

3-level NPC	Switching losses (W)	
	Matlab	*Plecs*
Diode (outer)	1.15	1.16
Diode (inner)	0.77	0.77

iii. 5-level Active neutral clamped point topology (ANPC):

We check the 5-level ANPC topology results for the same input data as for the 3-level NPC and a 5 kHz switching frequency.

This inverter combines a 3-level FC switching at high frequency (5 kHz) and a 2 cells 2-level switching at a low frequency (50 Hz) which gives a 5-level output voltage and 10 kHz as the apparent frequency. As Switcher switches at low frequency, the switching losses of this cell are very low.

TABLE II-12. 5-level ANPC power losses comparison using analytic analysis (*Matlab*) and *Plecs* simulation

5-level ANPC	Switching losses (W)		Conduction losses (W)	
	Matlab	*Plecs*	*Matlab*	*Plecs*
IGBT(FC)	15	14.54	75.02	75.11
Diode(FC)	6	5.57	45.45	45.51
IGBT (Switcher outer)	0.27	0.16	70.87	70.94
Diode (Switcher outer)	0.01	0	0.63	0.63
IGBT (Switcher inner)	0.27	0.3	43.08	43.12
Diode (Switcher inner)	0	0	4.67	4.67

iv. Multilevel Stacked Multicell Converter topology (SMC):

Using the same input data as before and a 10 kHz switching frequency, we first simulate the 3-level SMC 1x2.

TABLE II-13. 3-level SMC power losses comparison using analytic analysis (*Matlab*) and *Plecs* simulation

SMC 1x2	Switching losses (W)		Conduction losses (W)	
	Matlab	*Plecs*	*Matlab*	*Plecs*
IGBT inner	4.14	4.13	47	47.28
Diode inner	20.41	20.49	49	49.54
IGBT outer	26.93	26.96	71	70.95
Diode outer	0.96	0.99	0.63	0.63

Then we simulate a 5-level SMC 2x2:

TABLE II-14. 5-level SMC power losses comparison using analytic analysis *(Matlab*) and *Plecs* simulation

SMC 2x2	Switching losses (W)		Conduction losses (W)	
	Matlab	*Plecs*	*Matlab*	*Plecs*
IGBT inner	1.03	1.03	49.17	47.28
Diode inner	5.1	5.08	51.84	49.54
IGBT outer	6.73	6.75	69.9	70.88
Diode outer	0.24	0.24	0.63	0.63

For the SMC topologies, we have the same losses with both tools.

The data show that the analytic analysis using *Matlab* and the simulation using *Plecs* have the same results so we can validate the analytic analysis.

6. Introduction of Multilevel Necessity

The first step of the project defined in Chapter I was to define the DC bus voltage. As seen in the part 3 of this chapter (Fig. II-18), using the adapted generated component for a 2-level inverter implies an optimal DC bus voltage around 600 V. If real components meant to be used for this DC bus voltage, the number of semiconductors in parallel would be important.

To define the DC bus voltage using real components, the limits of components voltage and current ratings and the high switching frequency should be taken into account. For a two-level inverter, a DC bus voltage sweep was done using several real components and plotted the efficiency in Fig. II-22. For 6500 V and 3300 V components that are not adapted to 6 kHz switching frequency, the losses are high so is the temperature. With the used switching frequency, these components cannot be used**.** For 1700 V components, the efficiency is higher and gets better with 1200 V ones. If we want to use a 4 kV DC bus, for example, we should use several components associated in series**.** But in these cases, the direct series association is allowed, unlike the red curve. The shadowed part of the curves cannot be realized without direct series association.

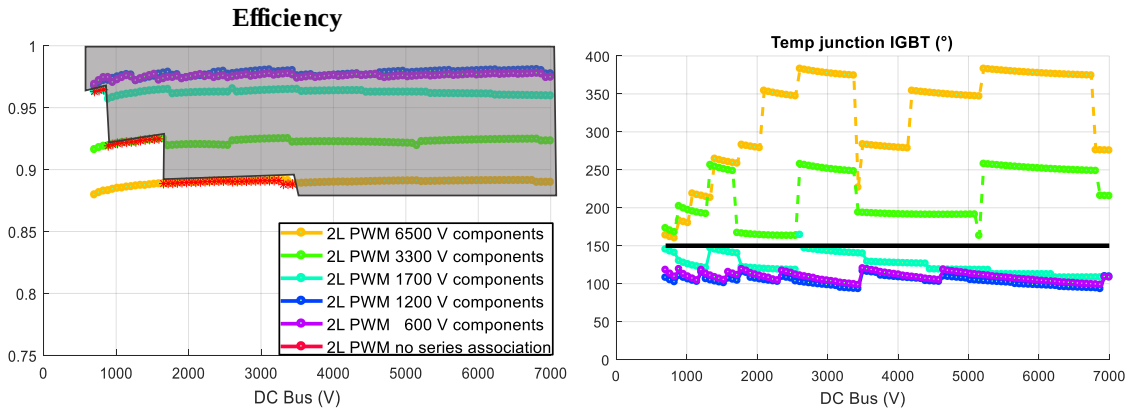


Fig. II-22. Efficiency for 2-level inverters with different voltage rating components for DC bus voltage sweep

Fig. II-23 shows the efficiency of the 2-level inverters studied above with an adapted switching frequency so to keep the maximal junction temperature under 150 °C. For the 6500 V and 3300 V components, the switching frequency should be nearly equal to the electric motor fundamental frequency (around 500 Hz) which will create current harmonics that should be eliminated by using a filter. The big switching frequency jumps correspond to the series association. For example, for the 1700 V components, around 1000 V, the inverter goes from 4 components in parallel and one in series to 3 in parallel et 2 in series. As the DC bus voltage increases, the needed current decreases for the same power. If the installed silicon is not optimally used, it results in more losses so the component heats up and the temperature exceeds the thermal limit so the switching frequency has to be reduced.

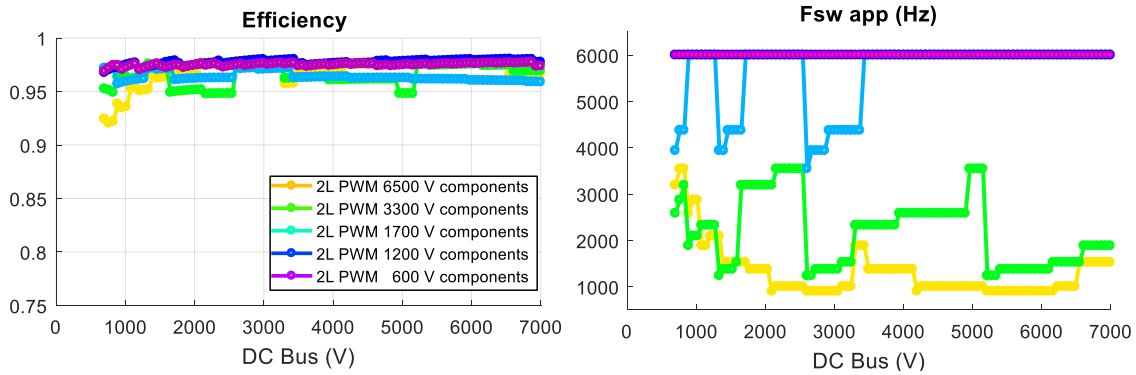


Fig. II-23. Efficiency for 2-level inverters with different voltage rating components for DC bus voltage sweep with adapted switching frequency

To choose the optimal DC bus voltage, using the available component voltage ratings, we estimated the possible DC bus voltages to use fully the available Silicon considered here as 60% of the component rating. This value was chosen so to have optimal use of the 1200 V and 1700 V components with an acceptable overvoltage. With the 5-level topologies, we can go up to 7 kV however with 2-level one, 2 kV is still high for the available components as it is noticed in Fig. II-24. The shadowed points are not feasible due to the high switching frequency which implies a high junction temperature.

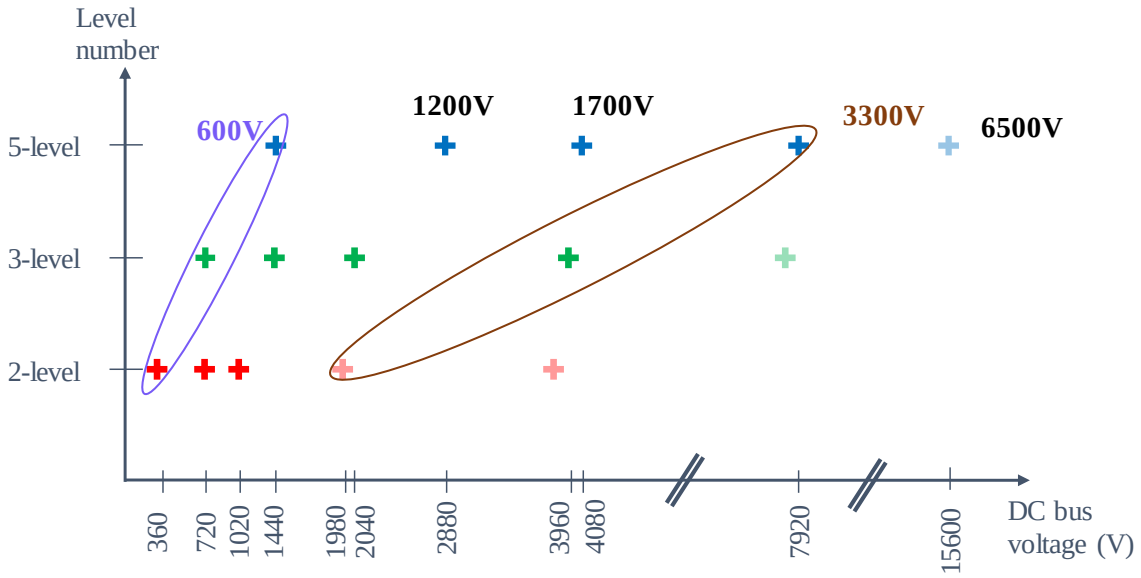


Fig. II-24. DC bus optimal voltage value depending on components voltage rating and topologies level number

If a 1.7 kV DC bus voltage, which seems to be an optimal value, is considered, the possible topology and components associations to withstand this voltage value are shown in Fig. II-25.

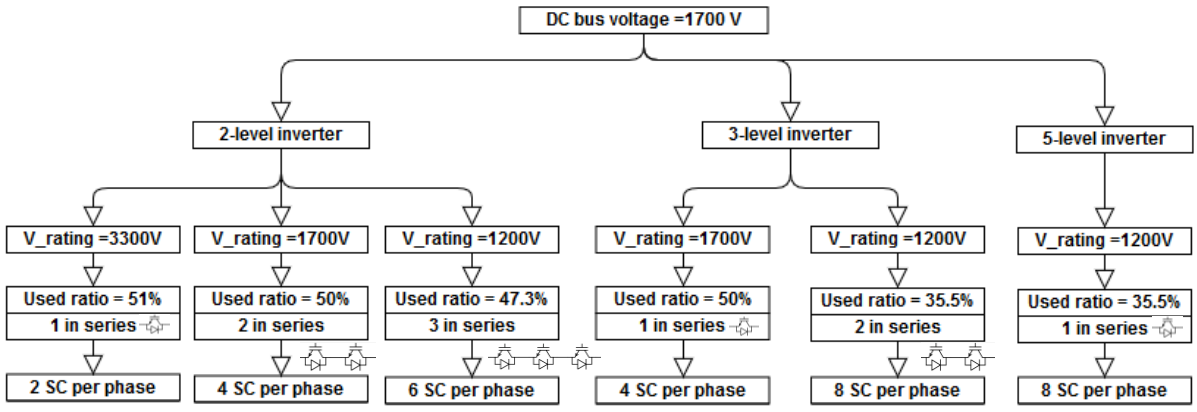


Fig. II-25. Number of topology level to use for 1.7 kV DC bus voltage

If direct series association is not allowed, a 3.3 kV component can be used with a 2-level inverter, or 1.7 kV one with 3-level topologies or 1.2 kV components with 5-level topologies. However, the 1200 V components are not fully used in this case.

So to use small voltage rating components, multilevel topologies must be used and the selected topologies will be shown in the Chapter III.

7. Conclusion

To size the power converter used to feed the electrical motor for the aircraft propulsion, a pre-design tool was developed. This tool is developed using *Matlab* object-oriented programming and is based on analytic analysis of the inverter power losses so to evaluate the efficiency and components temperatures to respond to our specification. The used power losses and thermal models were presented in this chapter. These models need several components such as capacitors and semiconductors parameters that are issued from the available database or generated based on it so to satisfy the current and voltage requirements. These components were validated using several study case scenarios and would help to define the DC bus voltage which is the first task of this work.

The available semiconductors voltage ranges limit the DC bus voltage that could be chosen if the 2-level topology was to be used without allowing direct series association. The high switching frequency represents also a constraint to the large voltage caliber components that were not meant to operate at these frequency levels due to the high switching losses. With all this said, using smaller voltage rating components but with high DC bus voltage to reduce the needed current rating would be more interesting. This could be done by using multilevel topologies.

The studied multilevel topologies will be presented in the next chapter as well as the different control strategies. The used components technologies will also be compared so to choose the optimal solution in terms of efficiency and specific power.

III. Comparison of possible solutions sized for the maximal power point

The main factor to increase the specific power that was identified in Chapter I is decreasing the cooling system mass by optimizing its components which is a part of WP4 work or by reducing power losses. Inverter power losses reduction could be achieved either by using small components or by playing on modulation strategies or by using more performant semiconductors (Fig. III-1). The first option, which is using small voltage rating components, could be done by using multilevel architectures to avoid the direct series association.

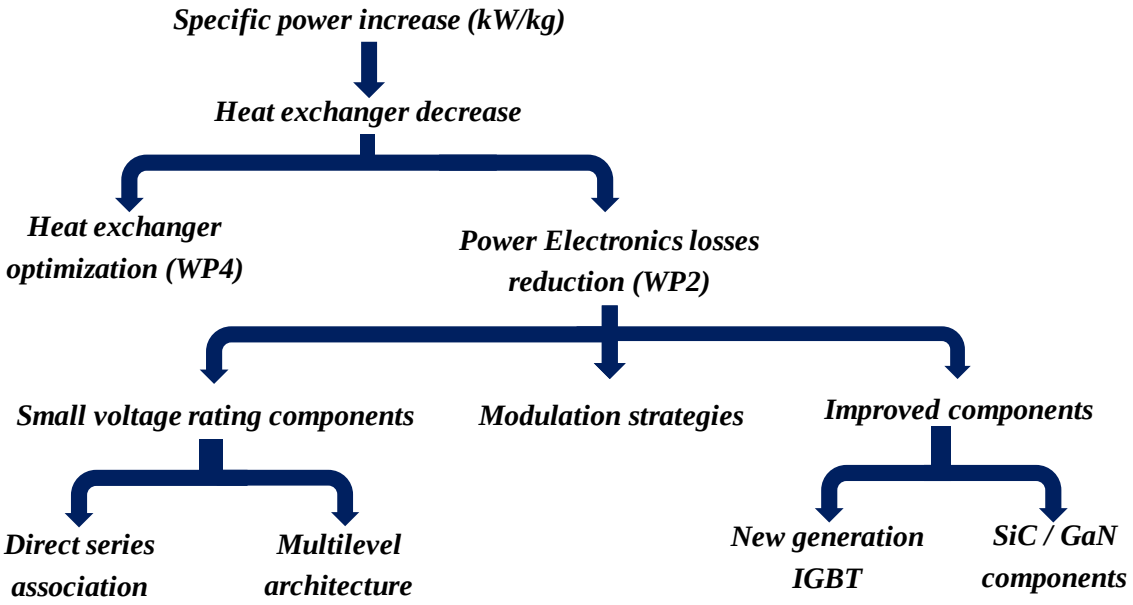


Fig. III-1. Specific power increasing study line

To design and compare power inverters to choose the most suitable solution, the simulation tool presented and developed in the previous chapter was used. It can easily compute different results for different power converters architectures. It takes into account the design constraints (DC bus voltage, output power, …), the foreseen converter topologies, and the semiconductor family choice from the included components database. The study results such as efficiency, number of semiconductor devices, voltage rating selection, maximal junction temperature, losses, cooling system mass, DC bus capacitor, and specific passive elements (such as flying capacitor weights), as well as the power density, are shown as figures for different parameters of different architectures performances.

The power chain needs careful design to minimize the mass of the whole system which is directly linked to the mass of the converter and also the losses through the weight of the cooling system.

In this chapter, the studied inverter topologies and modulation strategies will be presented. Then the performances will be compared using several semiconductors to choose the most performant solution in terms of efficiency and specific power. For this Chapter, the considered design point

is the maximal power point which corresponds to the takeoff shown in the mission profile in Chapter I.

1. Comparison of topologies with PWM modulation strategy

i. Multilevel inverter topologies

The need in terms of power electronics has evolved and tends to increase power or usage voltage and to decrease the needed current to reduce losses and cables mass. However, this is not possible with a conventional two-level structure since the semiconductor ranges are limited in voltage to 6500 V which corresponds to a maximum blocking voltage of about 3600 V. The performance of these components is reduced for high voltages since the components are slower, which means more switching losses. These power electronics topologies are used in the medium-voltage drive application. For a marine propulsion for example [36], the onboard DC grid system contains a 1 kV DC bus and 2 x 4.5 MW propellers with 2 x 6.6 MVA low-voltage inverters. For this type of application, ABB uses the ACS1000 which contains a three-level inverter, without series or parallel connected power semiconductors, that is one of the least complex, most robust and efficient drive topologies [37].

To address the voltage needed levels, two solutions are possible and will be detailed below and are as follows:

• Split up the voltage or current constraints

• Use cell or converters associations.

1. Split components' constraints

The first possibility is the direct series association of the components (Fig. III-2), which makes it possible to split the voltage constraint and to use combinations of cells or converters.

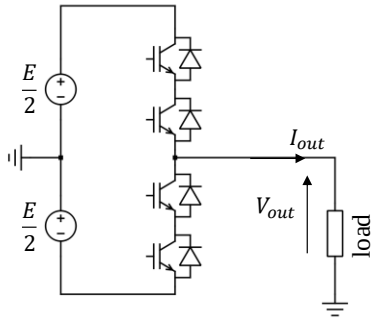


Fig. III-2 : Direct series component association

This method increases the voltage while keeping the voltage range of the component low which is more performant than high voltage rating components. This association also makes it possible to increase the switching frequency since the constraint is divided over components associated in series but does not improve the waveforms and the distribution of the dynamic constraints.

The spontaneous balancing of the constraints can't be guaranteed without additional components such as resistors. The switches do not commute exactly at the same time and therefore a switch must be able, in the worst-case scenario, to handle twice its sizing voltage which leads to its breakdown. In static, the association works very well even if, in dynamic, there may be a delay in the turn-on or blocking of the switch. It is then necessary to guarantee the constraints balance using, for example, intelligent drivers.

The second possibility is the parallel association of the components (Fig. III-3) which makes it possible to increase the current. This method does not improve output waveforms.

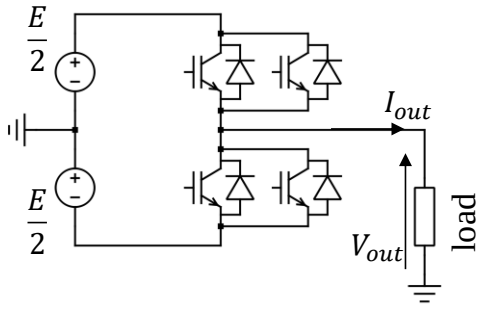


Fig. III-3 : Parallel component association

In this case, the sizing is the same as for a conventional two levels and the balancing depends on the ship temperature coefficient that can lead to a self-balancing or divergence. In this case, for the dynamic aspect, the switch must support the twice current if there is a delay in starting or blocking, which causes the temperature to rise, which could lead to thermal breakage. However, the static balancing is not guaranteed as for the voltage constraint stated above. But this solution is less penalizing than direct serialization thanks to thermal inertia.

2. Multilevel inverters

Even if the multi-level converters are used for high power medium voltage drive applications, they seem to be the best option to reduce the weight of the converter and still have high efficiency with smaller DC bus voltage.

More and more applications that require medium-voltage use multilevel topologies. With this type of inverters, the output voltage harmonics quality can be improved. The multilevel inverter is also used for renewable energy generation such as wind or solar that are medium and high power applications [38].

However, using a multilevel inverter to approximate sinusoidal waveforms from stepped waveform have sharp voltage transitions which create harmonics in addition to the fundamental frequency of the sinusoidal waveform [39]. The power quality and THD are affected by these harmonics. However, the generated harmonics are high-frequency one so they could be easily

filtered compared to the low frequency ones. So the multilevel inverter is more advantageous than a conventional two-level inverter.

The more levels the inverter has, the less THD will be. However, the limit of levels number is fixed by the voltage balancing problems, voltage clamping requirement circuit layout and packaging constraints [40]. The main disadvantage of this type of structure is the numbers of used switches and maintaining the voltage balanced in the voltage sources.

The high power converters could be classified as in Fig. III-4. In this work, the chosen converter topologies are medium voltage high power multilevel voltage source ones. The studied topologies will be the Neutral Point Clamped (NPC), the Flying Capacitor (FC), the Stacked Multicellular Converter (SMC) and the Active NPC topology (ANPC) [28].

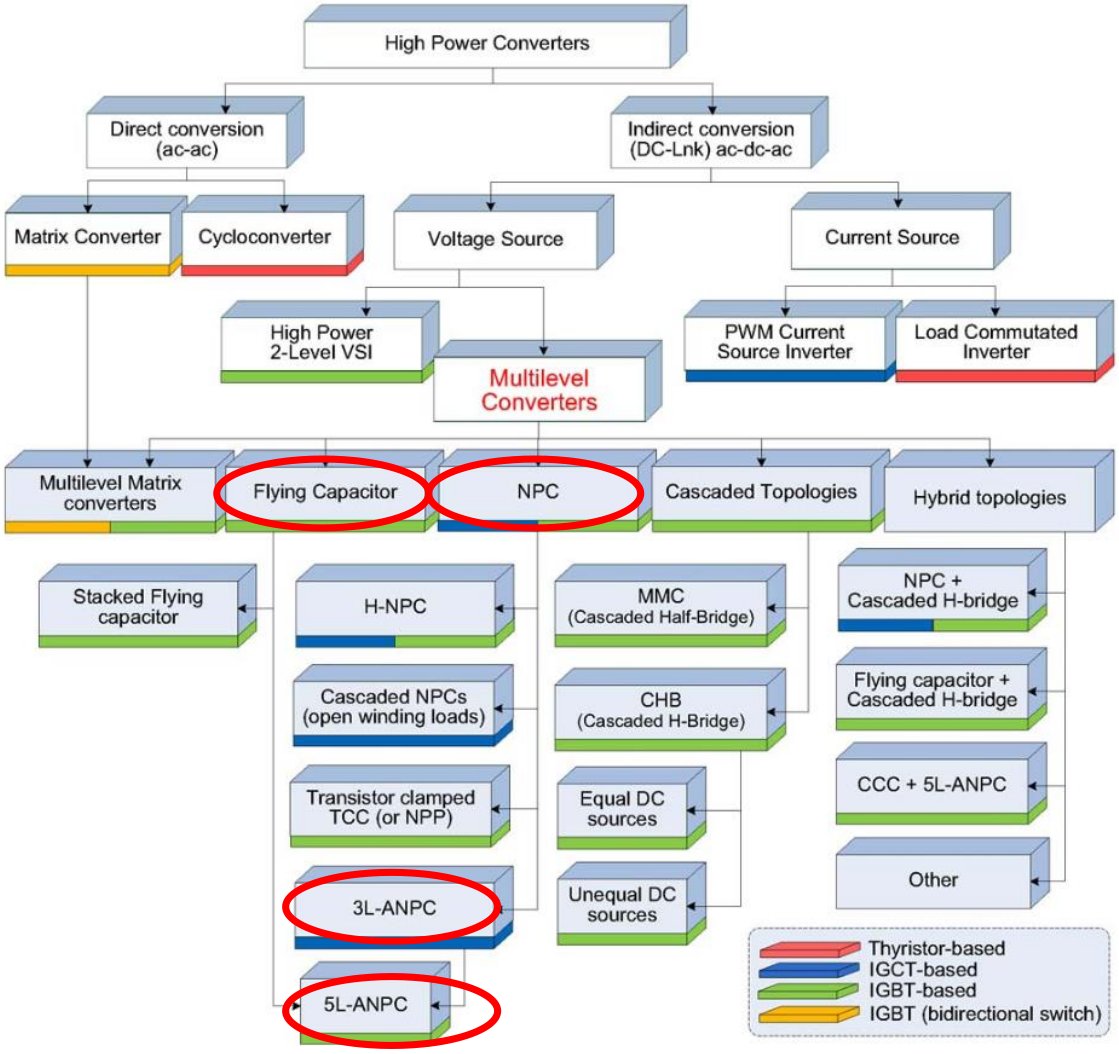


Fig. III-4 : Multilevel converter classification [41]

ii. Studied topologies

Several studied conventional topologies will be presented in this part. The chosen topologies are mainly 3 and 5-level ones as shown in Chapter II based on the DC bus choice according to

the components voltage ratings. Firstly, the 2-level inverter topology is presented so to have reference for comparison. Then Neutral Clamped Point, Flying Capacitor and Stacked Multi-Cell inverter topologies are shown. For each topology, the properties such as the components voltage rating (V_{rating}) and apparent switching frequency ($F_{sw_{app}}$) will be stated.

1. Two level inverter topology

The two-level voltage inverter for the 3-phase configuration is composed of six active switches with a freewheel diode in parallel with each switch. Fig. III-5 represents the 3-phase two-level inverter.

This structure is widely used for low voltage application (under $900\,V$) [42] but it can be extended to medium voltage high power applications.

The two-level inverter has several advantages such as the simplicity of its control. The conventional carrier-based sinusoidal modulation or space vector modulation scheme could be implemented for this inverter.

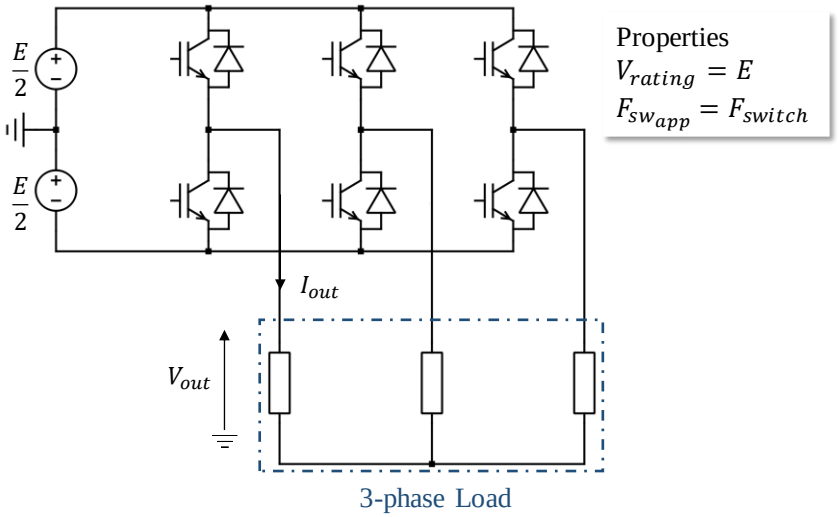


Fig. III-5. 2-level 3-phase inverter

However, there are some drawbacks associated with the two-level inverter such as the high $\frac{dV}{dt}$ in the output voltage due to the fast switching speed of the IGBT. This could lead to premature failure of motor winding insulation, early bearing failure and wave reflection. It could also generate high harmonic distortion in the stator voltage and current if it operates at a low switching frequency. These harmonics produce additional power losses in the motor.

These problems could be solved by adding an LC filter between the inverter and the motor. However, the use of the LC filter can increase the inverter weight and fundamental voltage drops.

2. Flying Capacitor inverter topology (FC)

The flying capacitor inverters have evolved from the two-level and based on a direct series association by adding an intermediate flying capacitor between two switching cells associated in series to fix the switches voltage and allows to split the input voltage by combination [43]. There are two complementary switch pairs in each commutation cell of the 3-level inverter (highlighted in red and blue in Fig. III-6).

The flying-capacitor inverter in Fig. III-6 can produce a phase voltage with three voltage levels.

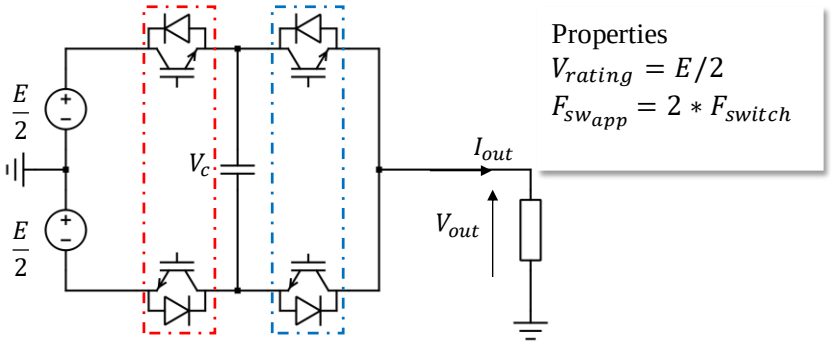


Fig. III-6. 3-level FC inverter's leg

In this case, it is necessary to guarantee the balancing of the voltage across this flying or floating capacitor. Some voltage levels can be obtained by more than one switching state. The voltage level 0, for instance, can be produced by two sets of different switching states. The switching state redundancy is a common phenomenon in multilevel converters, which provides great flexibility for the switching pattern design and control of intervals states variables.

As for the NPC, as a result of the serial connection, this structure thus makes it possible to divide the sizing voltage of the switches, in addition to that, it makes it possible to increase the apparent switching frequency at the output and to reduce the current ripple or the size of the inductance at the output, which makes it possible to improve the output performances.

Since the FC inverter topology is derived from the two-level inverter, it carries the same features as the two-level inverter such as a modular structure for the switching devices. It is also a multilevel inverter, producing the voltage waveforms with reduced $\frac{dV}{dt}$ and THD. However, the flying-capacitor inverter has some drawbacks such as their voltage balancing issues and also a large number of capacitors needed which take up a very large volume of the inverter.

3. Neutral Point Clamped (NPC) and Active NPC (ANPC) inverter topologies

The neutral point clamped inverter employs clamping diodes and cascaded DC capacitors to produce alternative voltage waveforms with multiple levels. The inverter can generally be configured as a 3, 4, or 5-level topology, but only the three-level inverter has found wide

application in medium voltage high power drives [44] [45]. Fig. III-7 represents the 3-phase three-level NPC inverter.

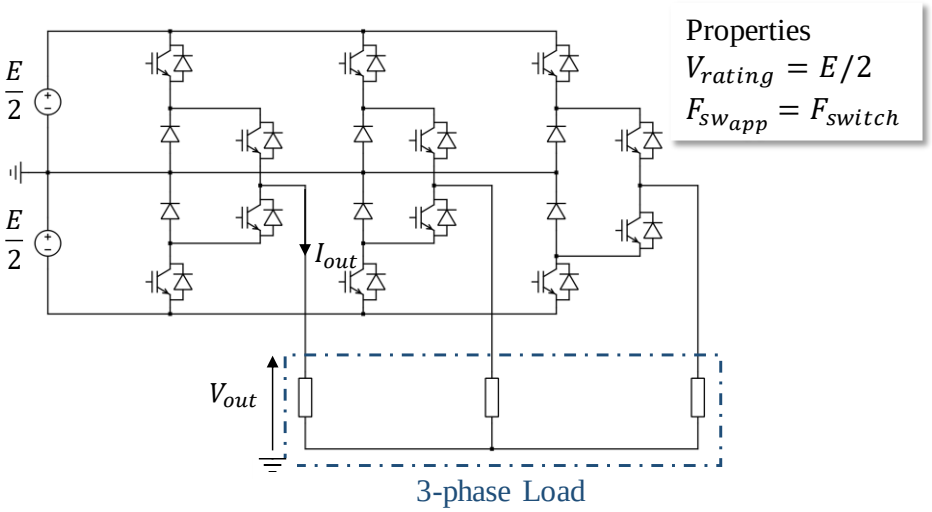


Fig. III-7. 3-level NPC inverter

This structure is based on a direct series association by adding a clamp to fix the switches voltage and allows to divide the input voltage. This structure does not improve the inverter output apparent switching frequency and the clamping circuit is a little complex to realize for 5 and above level topologies.

The main advantage of this structure is the reduced $\frac{dV}{dt}$ and output harmonics compared to the two-level inverter working at the same DC bus voltage and switching frequency. Yet, it needs additional clamping diodes and possible deviation of neutral point voltage which should be taken into account using this structure [46].

There is another NPC inverter type called Active NPC (ANPC) that overcomes the drawback of the unequal current distribution and has additional active switches in antiparallel to the clamping diodes as in Fig. III-8. So to balance the losses distribution, this topology offers multiples command strategies. The first one consist of switching the part in the red dotted frame at low frequency and the blue one at a high frequency so to use the switches near the voltage source as a switcher. The second strategy would be to use the reverse strategy which means switching at low frequency the switches near the load. The third strategy consists of switching both red and blue frames components at high frequency which will lead to double the output apparent frequency, but with higher switching losses [47], [48].

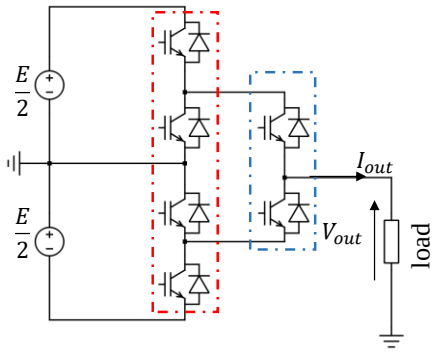


Fig. III-8. 3-level single phase ANPC

The 5-level active neutral point clamped inverter shown in the figure below (Fig. III-9) was developed by ABB to increase the voltage level without highly increasing the price. The idea was based on connecting converters in series. A three-level DC supply alone cannot supply five voltage levels, and so the circuit does require an additional capacitor per output phase. But the solution ABB ingeniously created keeps this capacitor charged without the need for dedicated control circuitry [49].

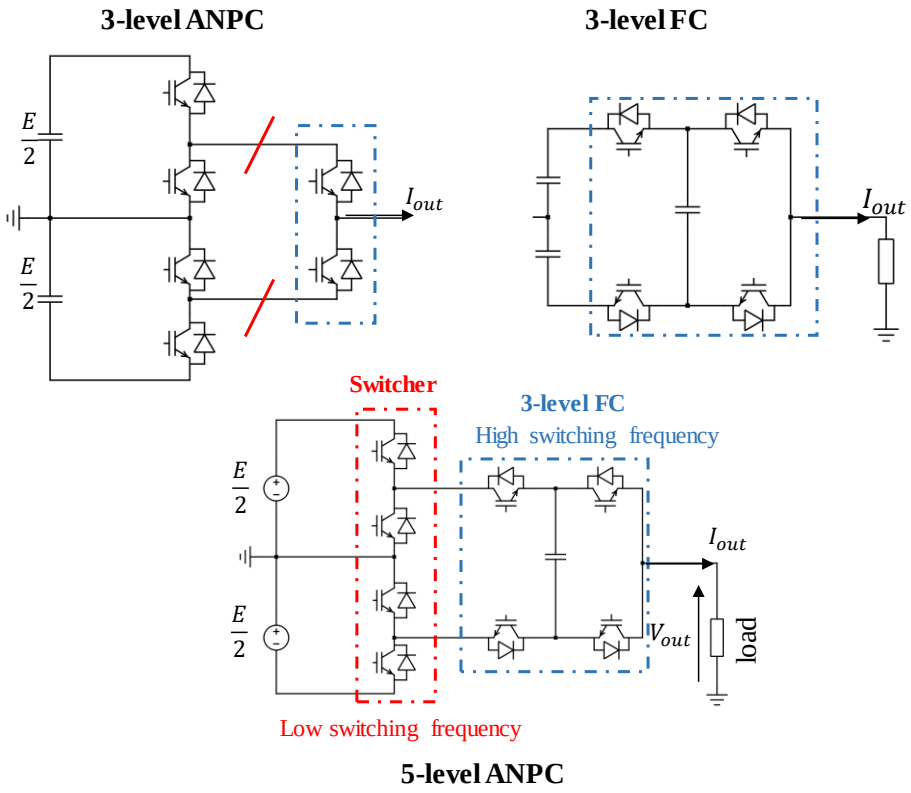


Fig. III-9. 5-level ANPC single phase inverter

The flying capacitor is kept charged to half the voltage of the capacitors in the DC link, one-quarter of the total DC-link voltage. The overall principle of the circuit can be considered as a three-level NPC converter plus an additional capacitor. This phase capacitor is switched in series with the three-level converter as required and provides two additional intermediate output levels (Fig. III-9). Moreover, it requires only one more capacitor and two switches per phase than an ANPC three-level converter.

4. Stacked Multicell Converter inverter topology (SMC)

The stacked multicell converter is based on a hybrid association of elementary switching cells as shown in Fig. III-10 for 2 × 2 SMC. An SMC $p \times n$ inverter has p switching cells in series and n stacks [50].

As for the FC topology, this topology enables to share the voltage constraint between several switches and also improves the output waveforms of the converter in terms of the number of levels and switching frequency.

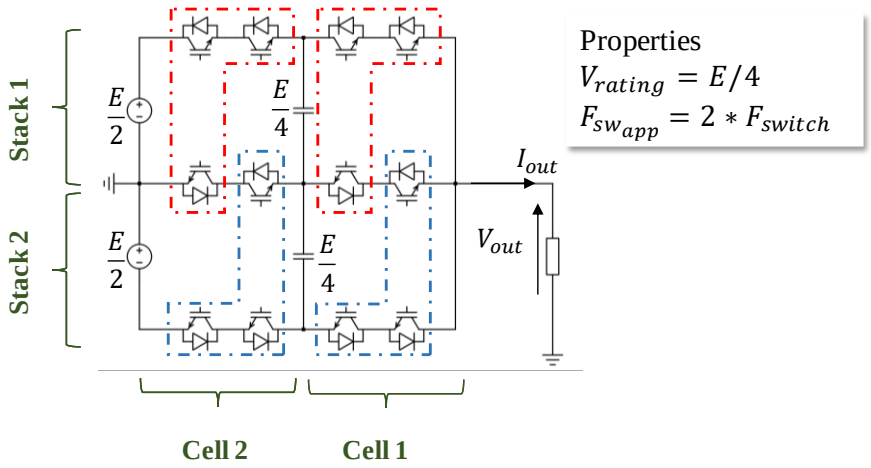


Fig. III-10. 5-level SMC 2x2 single phase inverter

Although the SMC requires more switches than an FC, it reduces the stored energy in the converter and thus the size of the flying capacitors proportionally to the number of stacks [50].

The following table sums up the studied topologies properties.

Table III-1. Summary of topology properties

Topology	**number of levels**	**SC Voltage rating**	**Output Switching Frequency f_{out}**	**Passive components**
2 levels	2	2E	f_{sw}	-
FC $\boldsymbol{N}$ Cells ($\boldsymbol{N \geq 2}$)	$N + 1$	$\frac{2E}{N}$	$N * f_{sw}$	(N-1) Capacitors
3-level NPC	3	E	f_{sw}	-
SMC $\boldsymbol{1 \times 2}$	3	E	f_{sw}	-
SMC $\boldsymbol{n \times p}$	$n \times p + 1$	$\frac{2E}{n \times p}$	$n * f_{sw}$	n Capacitors
ANPC including FC **2** Cells	5	$\frac{E}{2}$	$FC: 2 * f_{sw}$ $Switcher: f_{low\_freq}$	1 Capacitor

where: E is the DC Bus input Voltage, $n \times p$ is $Cell \times Stack$ numbers of the SMC topology.

iii. Comparison of studied topologies and DC bus voltage definition

These topologies performances will be compared so to define the best operating parameters for our specifications.

The first step of this work was to find out the DC bus voltage by taking into account the problem of partial discharges which limits the possibility of increasing the voltage level if the conductors are placed in the non-pressurized zone. To choose an optimal bus voltage range, it is necessary to compare the efficiency of several multilevel topologies. However, it is difficult to do so due to the discretization of available voltage ratings. To overcome this problem, the generated components database developed in Chapter II, that suits the needed voltage caliber by fitting and extrapolating the existing database are going to be used.

For the first phase of the project, the study will be based on the topologies shown before with silicon components and a standard machine. The DC voltage of the hybridization bus (0.7-7kV) must, therefore, be set [51]. The optimum voltage range will be defined by comparing the results of the parametric study for the various topologies studied using the available components database.

In this first approach, the evolution of converters specifications is studied for different DC bus voltages. The converters under study are: 2L (PWM), 3-level FC (PWM), 5-level FC (PWM) and 5-level ANPC. A parametric sweep of the DC bus voltage is implemented starting from 100 V to 4 kV for an imposed power of 1 p.u. which corresponds to the first specification. Due to the limitation of the existing components' voltage calibers which corresponds to 6500 V so a definition voltage of 3600 V, for the low-level topologies, the results for higher DC bus voltage should not be taking into account.

As regards the switching frequency, a ratio of 10 between the electric motor fundamental frequency and the apparent switching frequency was maintained. This study was done based on the first specification.

1. Comparison of 2-, 3- and 5-level topologies

To verify earlier conclusions concerning the use of low-voltage components, three topologies using small and large voltage calibers for each topology are compared. Using ABB component available in our database, 2-level, 3 and 5-level topologies performances were estimated for a DC bus sweep from 700 V to 7 kV with a switching frequency of 5.8 kHz and the maximal power point with a fixed case temperature of 80 °C. Fig. III-11 shows the inverter efficiency, power losses, maximal junction temperature and number of total used switches for the studied topologies. The generated components are used at 50 % of their voltage rating and 100 % of their current rating.

The high voltage components that are used for the 2-level topology have more switching losses due to their properties and also to the high switching frequency which is lower for 3 and 5-level topologies.

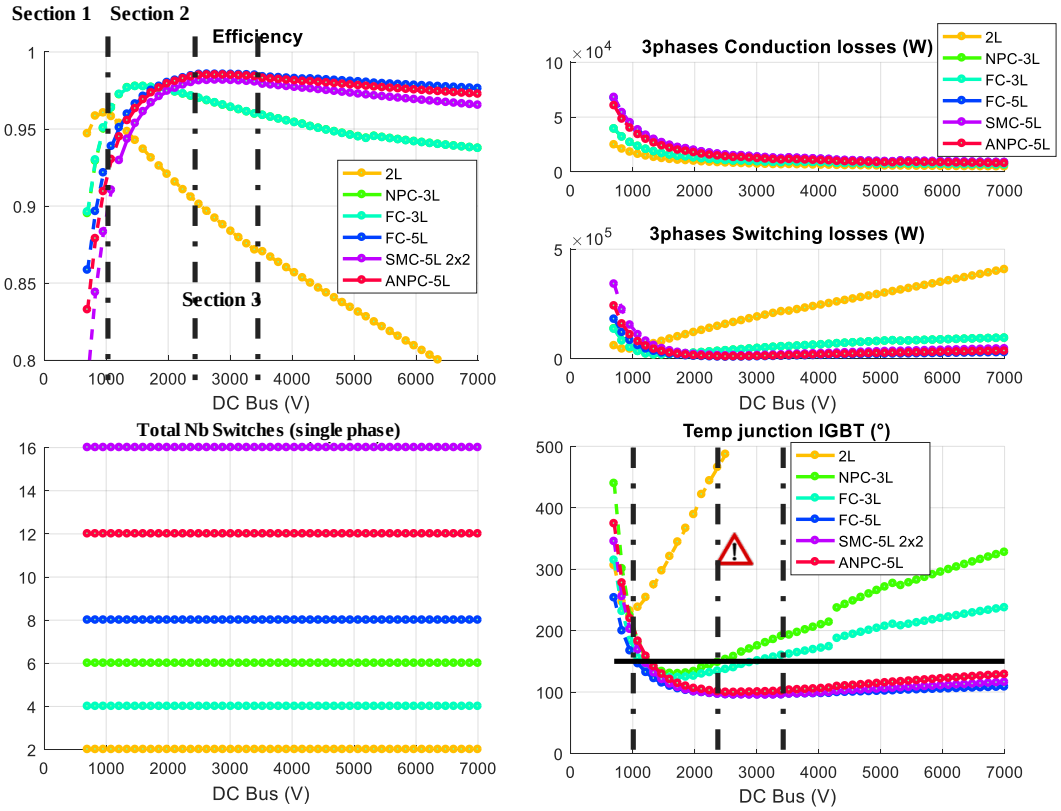


Fig. III-11. Generated components response for DC bus sweep for 2-, 3- an 5-level topologies

In the first section ($700\ V \leq V_{DCBus} \leq 1\ kV$), the 2-level topology has higher efficiency than the other ones, however, if this solution is selected, it would be disadvantaged by the number of needed components in parallel to withstand the needed current. Above 700 V, the maximal junction temperature of the used semiconductors is higher than the 150°C limit.

In the second section ($1\ kV \leq V_{DCBus} \leq 2.4\ kV$), the 3-level topology efficiency is slightly better than the 5-level topologies so no need to use them. In the third section ($2.4\ kV \leq V_{DCBus} \leq 3.5\ kV$), both 3 and 5-level topologies are equivalent in terms of efficiency. For a DC bus voltage higher than 3.5 kV, the maximal junction temperature of the 3-level topology semiconductors is higher than the thermal limit so only the 5-level topologies are interesting for this voltage range in terms of efficiency and maximal junction temperature.

Multilevel topologies use more components than a 2-level one but have better performances and lower maximal junction temperature. As seen before, the high voltage components have more switching losses due to their properties and also to the high switching frequency that is lower for 3 and 5-level topologies. They have therefore lower junction temperature even if they are use more semiconductors.

2. Switching frequency impact study

The purpose of this part is to verify if the switching frequency value can change the tendencies seen in the previous part, namely that the use of the multilevel structures makes it possible to improve the efficiency by using components with smaller voltage rating in spite of their greater number. The high voltage components are not meant to be used at high switching frequencies which lead to great losses that heat the components and their junction temperature exceeds the thermal limit of 150 °C.

Fig. III-12 shows the previously studied topologies for a DC bus voltage sweep using an adapted switching frequency so to have an acceptable maximal junction temperature. The apparent or output switching frequency was limited to the electric motor fundamental frequency of 532.3 Hz (represented in black limit in the figure) so it can't be lower than this value. The relation between the switching frequency and apparent one depends on the topology. For example, if the apparent or output switching frequency is 5 kHz for the 3-level NPC, it is then 2.5 kHz for the 3-level FC and 1.25 kHz for the 5-level FC.

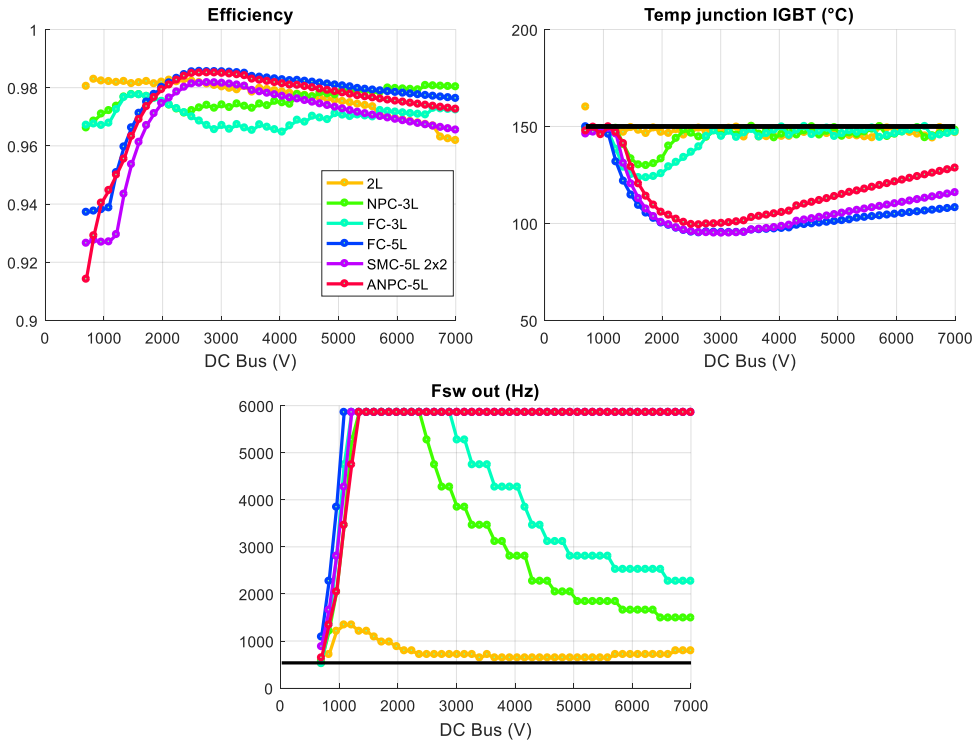


Fig. III-12. 2-,3- and 5-level topologies performances for a DC bus voltage sweep with adapted switching frequency

The 2-level topology should operate at a low switching frequency so to have an acceptable maximal junction temperature. Above 2.4 kV, the switching frequency should be reduced to keep the 3-level topologies temperature under the 150 °C limit unlike the 5-level ones that have acceptable temperature starting from 1 kV DC bus voltage.

The multilevel converters are the best solution to keep an acceptable junction temperature with a high efficiency whatever is the switching frequency. This conclusion is even stronger when the switching frequency is higher, the efficiency gap between the structures increasing.

3. Specific power

To estimate the specific power, the total weight of the inverter including the DC bus capacitor, the semiconductors, the heat exchanger coefficient given in the specification dossier (0.34 kW/kg) and the flying capacitors is calculated for 3- and 5-level studied topologies using the generated components. Fig. III-13 shows the specific power for the studied topologies as a function of the DC bus voltage value using generated components.

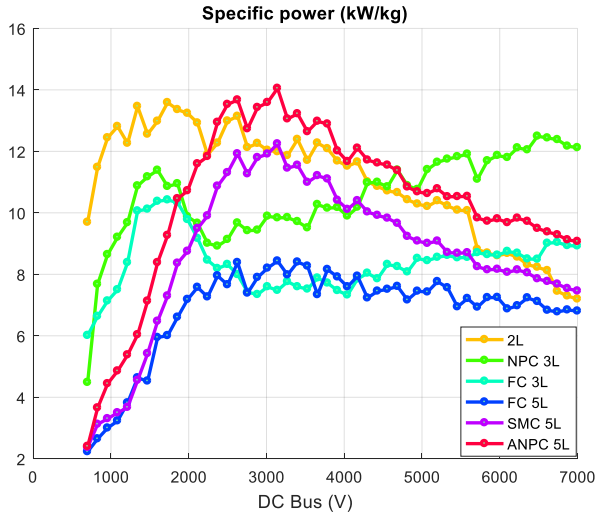


Fig. III-13. Specific power for studied topologies using generated components and adapted switching frequency

The following table sums up the maximal power density and the corresponding DC bus voltage and efficiency using generated components. The 2-level is written in red since its maximal junction temperature is higher than the thermal limit with a 5.8 kHz switching frequency. Its switching frequency is then adapted to satisfy the thermal constraint.

TABLE III-2. Maximal power density for 2-level, 3-level FC, 5-level FC and 5-level ANPC with generated components

Switching frequency (Hz)	Topology	Maximal specific power (kW/kg)	Corresponding DC bus voltage (V)	Efficiency (%)
5855	2-level	6.73	957	96.04
	3-level NPC	11.39	1600	97.76
	3-level FC	10.42	1730	97.77
	5-level FC	8.43	3143	98.53
	5-level SMC	12.24	3143	98.12
	5-level ANPC	**14.05**	**3143**	**98.47**
879	2-level	14.98	1986	98.19

Fig. III-14 represents the total weight repartition for the studied topologies using generated components for the points corresponding to the highest specific power with a maximal junction temperature lower than 150 °C. The cooling system represents the predominant weight for almost all the topologies expect for the 5-level FC in which the flying capacitors represent 36 % of the total weight. Using multilevel topologies makes it possible to reduce the total weight at least by 20 % compared to the 2-level one.

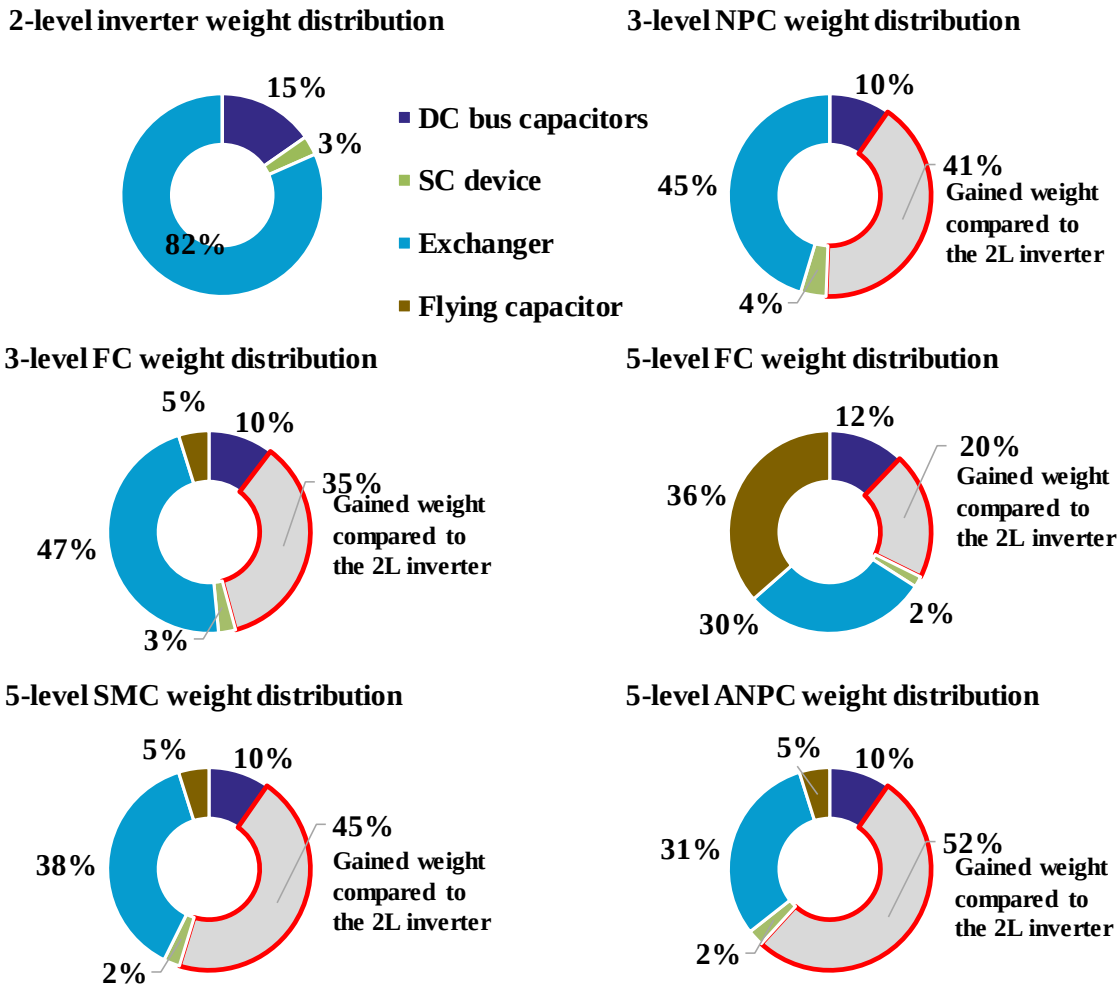


Fig. III-14. Weight distribution for studied topologies with generated components

Due to the flying capacitors weight, the FC topologies have lower power density than the other multilevel topologies even if their efficiency is high. To go beyond the 2025 target, the 5-level ANPC seems to be the best option if it is used at a low switching frequency. The 3-level NPC is also to be considered to reach this target even with the high switching frequency.

Now let's see what could be achieved using real components. Fig. III-15 shows the specific power for the studied topologies as a function of the DC bus voltage value using real components and shows only the points satisfying the thermal limit condition. For the 2-level topology, the switching frequency should be reduced to have a maximal junction temperature under 150 °C.

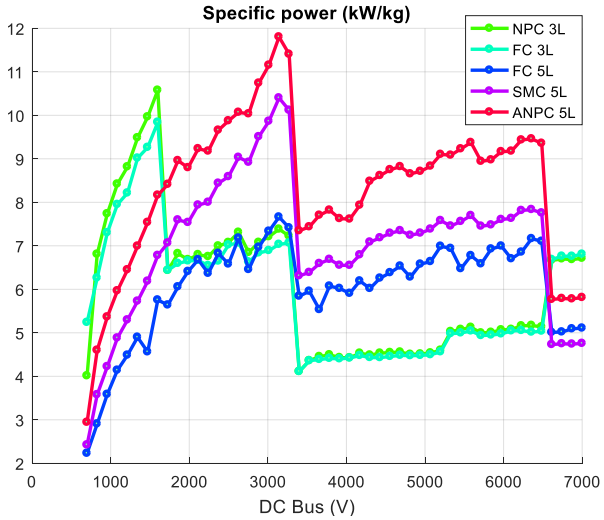


Fig. III-15. Specific power for studied topologies using a switching frequency of 5.8 kHz using real components

In TABLE III-3, the maximal specific power using real components is at the same range as for the generated components. With the 2-level topology, the specific power is the closest to the 2025 targert of 15 kW/kg, however, the switching frequency is so low that it could degrade the THD and output waveforms.

TABLE III-3. Maximal power density for 2-level, 3-level FC, 5-level FC and 5-level ANPC with real components with adapted switching frequency

Switching frequency (Hz)	Topology	Maximal specific power (kW/kg)	Corresponding DC bus voltage (V)	Efficiency (%)
577	2-level	13.05	2886	98.29
5855	3-level NPC	10.58	1600	97.67
5855	3-level FC	9.84	1600	97.67
5855	5-level FC	7.66	3143	98.27
5855	5-level SMC	10.40	3143	97.85
5855	5-level ANPC	**11.80**	**3143**	**98.22**

To achieve the specific power targets, the used topology will mainly be a 3-level one which is the most adapted for the used voltage and power ranges. 5-level could be an option if the DC bus voltage was to be increased ($\geq 2kV$) to optimize the whole power chain. However, flying capacitor topologies are penalized by the added capacitor weight. The bus bar weight will also be taken into account, in the part 4 of this study, to get a more accurate estimation of the inverter specific power.

4. Design for different power values

Another study is done using two parametric sweeps of the DC voltage [700 V – 7 kV] and power [25 - 1500 kW] considering a fixed apparent frequency (5.8 kHz). The simulation results

are shown in Fig. III-16 with taking into account the thermal limit using generated components. These figures give an impression of the efficiency tendencies of each studied topology. For all the topologies, the efficiency is very low for low power because the used components are not adapted to this power range.

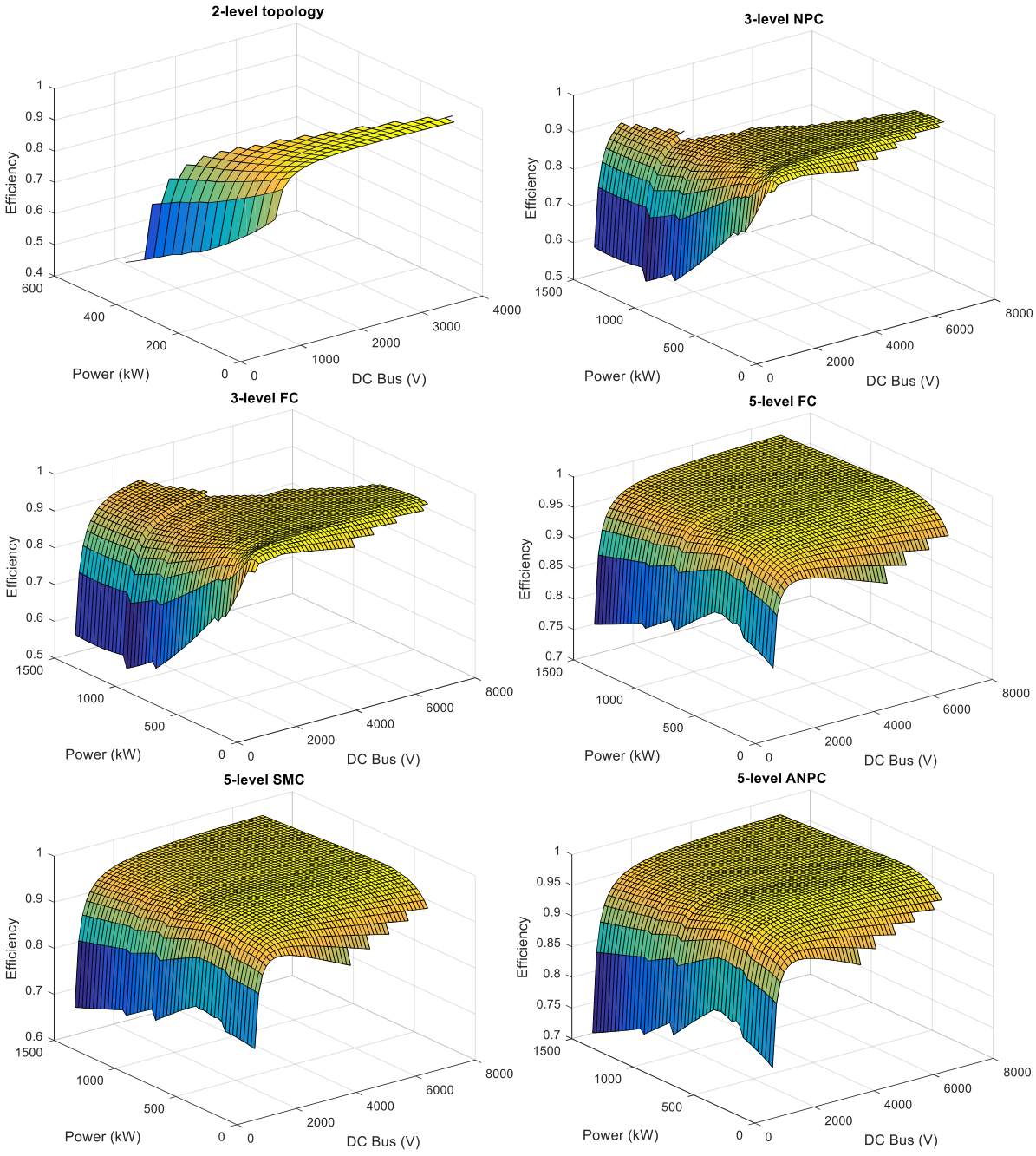


Fig. III-16. Efficiencies of studied topologies for DC voltage and power parametric sweeps

More power means more absorbed current by the load for a DC bus voltage, thus more losses in the semiconductors. This leads to increase junction temperature due to the high thermal resistance related to the needed high current rating which heats up of the components. Hence larger and heavier exchanger and cooling dissipation system are needed.

The 2-level inverter could only be used at low power with a DC bus voltage that decreases with the used power for the used switching frequency. So this inverter does not seem to be the best option for our application as stated before. The 3-level inverters could be used up to 2 kV all over the studied power range and they have an optimal efficiency between 1 kV and 2 kV. However, for the 5-level topologies, they have an optimal efficiency between 3 kV and 4 kV. I It can be drawn that for these topologies, from the efficiency graphs, that the optimal efficiency is for a DC Bus voltage is between 1 kV and 4 kV.

2. Modulation strategies

Modulation strategies aim to get an output voltage that approximates a sinusoidal waveform with adjustable amplitude or frequency. Each strategy has its switching configuration which generates control reference and keeps the voltage sources balanced. The multilevel modulation techniques could be classified as in Fig. III-17 [52].

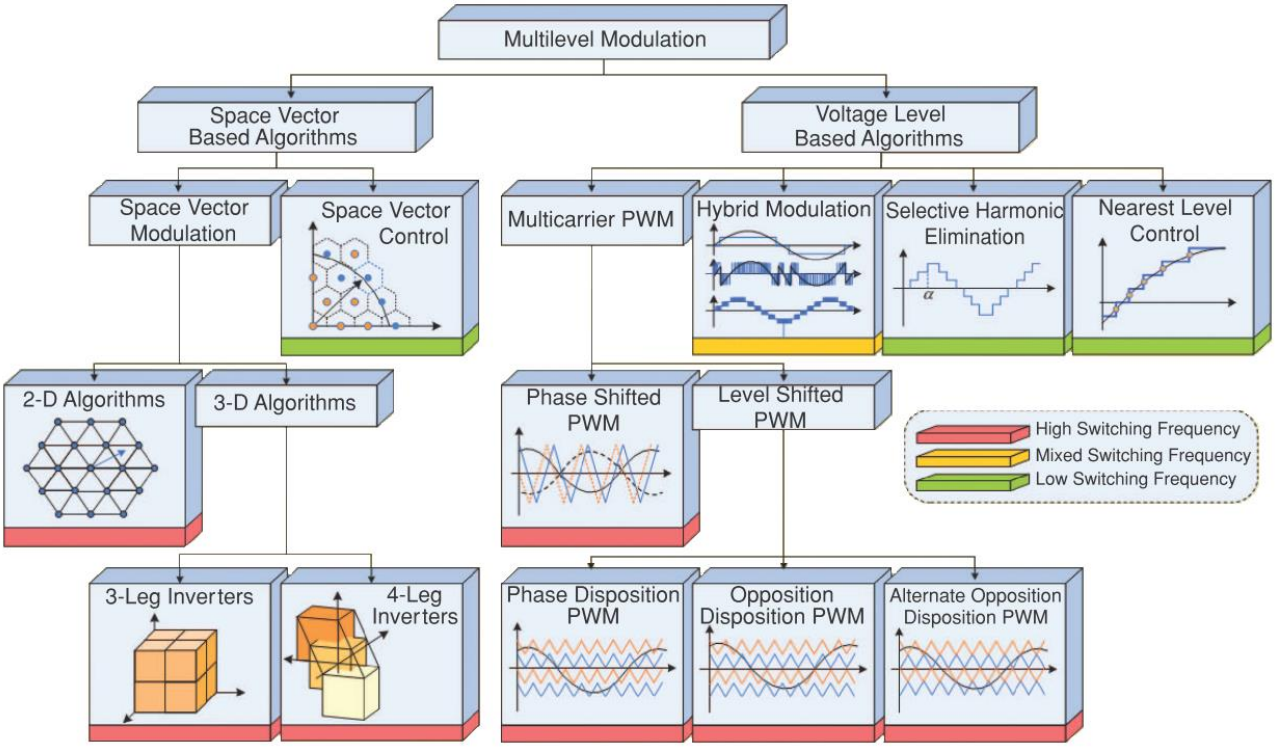


Fig. III-17. Multilevel inverter modulation classification

Modulation algorithms are divided into two main groups. The first one corresponds to the space vector, in which the operating principle is based on the generation of the voltage vector, and the second one corresponds to the time domain, in which the method is based on the generation of the voltage level over a given period. The different methods could be sorted as a function of the switching frequency they produce. In general, low switching frequency methods are preferred for high power applications due to the high voltage components' low switching speed, while the higher output power quality and bandwidth of high switching frequency algorithms are better suited for high dynamic range applications. They can also be classified according to

switching frequency [53]. The switching frequency is at least 7 times higher than the fundamental frequency so to have acceptable waveforms [33].

The studied multilevel modulations are based on the voltage level algorithms and could be classified as in Fig. III-18. They can be grouped into two types of modulation based on the used switching frequency. The first one, based on high switching frequency, is the Pulse Width Modulation including three options: the regular sine PWM, third harmonic injection PWM, and discontinuous PWM. The second one, based on low switching frequency, is the Full-Wave Modulation. These modulation strategies will be presented in detail later in this chapter.

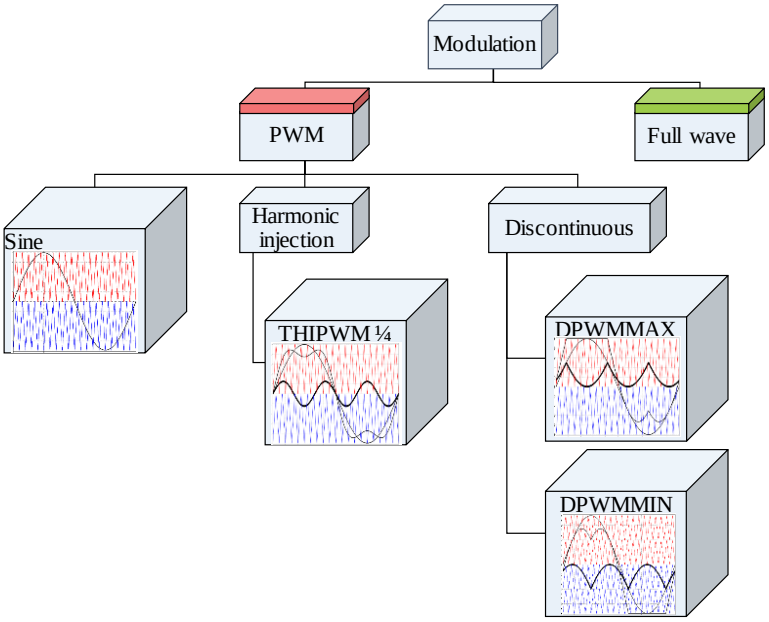


Fig. III-18. Studied modulation strategies

To have a point of reference, results using the sine PWM are given with a 3-level inverter. The voltage is not purely sinusoidal because of the switching and we will also plot the fundamental as in Fig. III-19. This fundamental will be controlled since the machine will filter the harmonics to obtain an almost sine wave current.

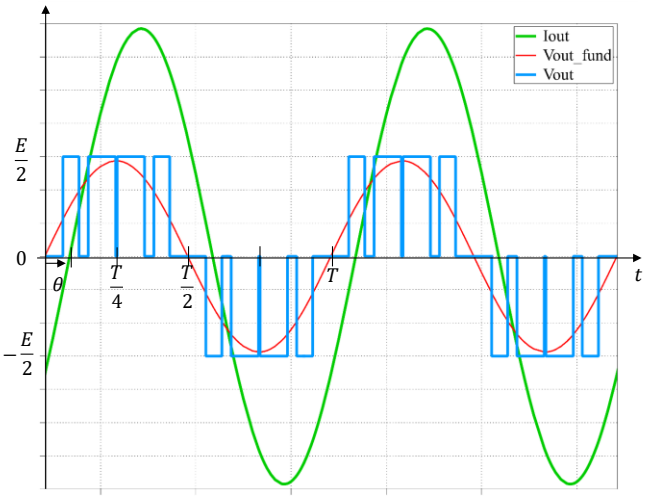


Fig. III-19. Output desired voltage and current 3-level PWM waveforms

The switching losses account for a significant amount of the total power losses in this type of inverters. Unlike conduction losses, they can be reduced by reducing the switching frequency without reducing the current or changing the used component parameters. Moreover, the cooling system represents a large part of the mass. Reducing the cooling requirements by reducing the losses in the converter would decrease the global weight of the system, also reducing its physical size and manufacturing cost. It would also increase the specific power. The switching loss minimization can be done by using a full-wave modulation. However, the reduction of switching frequency generally causes an increase in harmonic distortion of the line- and motor-side waveforms of the drive which will be the case of the full-wave modulation. THD must be monitored.

The full-wave, discontinuous and harmonic injection PWM methods will also allow generating more output voltage to feed the machine as in TABLE III-4. Using the Full wave modulation provide 30 % more voltage than a sine PWM which will able us to reduce the DC bus voltage for the same needed output voltage.

However, to take into account the dead time, the required time delay for the conduction of the transistors, to ensure that their complementary transistors have had time to lock, the maximal modulation index for PWM was fixed to 0.9 and not 1.

TABLE III-4. Maximal output voltage magnitude as function of DC bus voltage and modulation strategy

	PWM	**THIPWM / DPWM**	**Full wave**
$\boldsymbol{V_{out\_max}}$	$\frac{V_{DCbus}}{2}$	$1.15 * \frac{V_{DCbus}}{2}$	$1.3 * \frac{V_{DCbus}}{2}$

To define the needed DC bus voltage and appropriate modulation strategy, the output needed voltage during the flight mission profile which will be developed in Chapter IV.

i. Multilevel SPWM

Sinusoidal pulse width modulation is the most popular method where a high-frequency triangular carrier wave is compared with a sinusoidal reference of the desired frequency. The switching or commutation instants are defined by the intersection of both waves. For this modulation, the harmonics are around the switching frequency. This was the method used so far for this project [28].

Fig. III-20 shows a phase-shifted PWM two cells carrier and sine reference that will be compared to generate the switches command signal for a 3-level inverter. Other strategies as carrier phase opposition and phase disposition could be used depending on the used topology and the desired output performances.

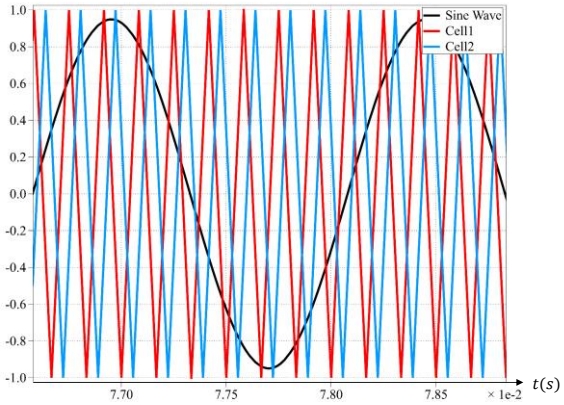


Fig. III-20. PWM triangular carrier and sine reference

ii. Discontinuous PWM (DPWM)

Discontinuous PWM method is an effective strategy to reduce switching losses. DPWM involves locking each phase leg to a fixed DC voltage level for 120° per fundamental cycle while the remaining two-phase legs are pulse width modulated [54]. Theoretically, DPWMs reduce about 33% of the inverter switching losses compared to continuous PWMs [55].

The easiest approach for discontinuous modulation of a multilevel inverter is to simply lock particular phase legs to the upper or lower voltage rails for fractions of the fundamental cycle [33].

To do so, a signal is added to the sinusoidal reference which results in the new reference (equations III-1) represented in black in Fig. III-21 that is compared to the triangular carrier, in which the switching cell does not switch for a third of the modulation period.

$$\begin{cases} V_{off,DPWMMIN}(t) = -\left(1 + \min\left(V_{1N,ref}(t), V_{2N,ref}(t), V_{3N,ref}(t)\right)\right) \\ V_{off,DPWMMAX}(t) = -\left(1 + \max\left(V_{1N,ref}(t), V_{2N,ref}(t), V_{3N,ref}(t)\right)\right) \\ V_{1N_{ref}\,DPWM} = V_{1N,ref}(t) + V_{off,DPWM}(t) \end{cases} \quad \text{(III-1)}$$

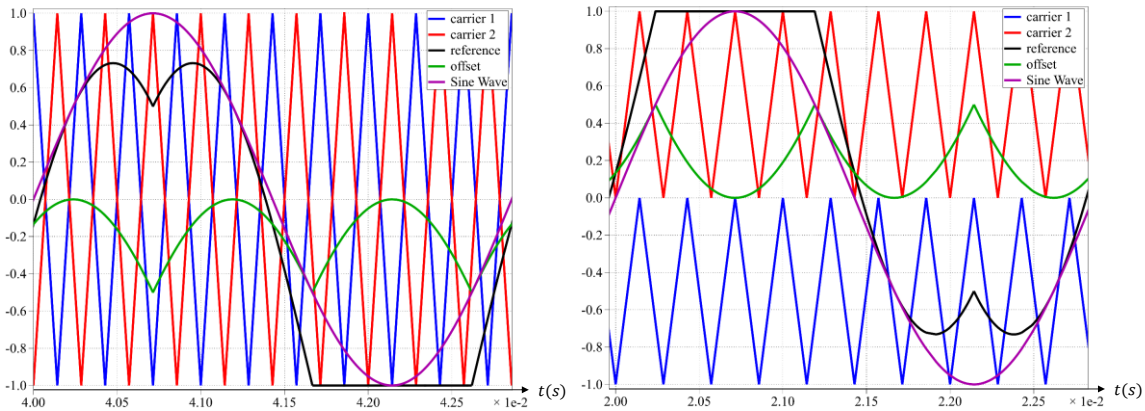


Fig. III-21. DPWMMIN with phase opposition and DPWMMAX with phase disposition triangular carrier and sine reference

iii. Third Harmonic injection PWM (THIPWM ¼)

The sinusoidal pulse width modulation does not fully utilize the DC bus voltage. So, the third harmonic injection pulse width modulation strategy was developed to increase the inverter output voltage fundamental magnitude for the same DC bus voltage as for a Sine PWM.

The third harmonic injection PWM (THIPWM) method is suitable for three-phase inverters. To obtain the modulation reference, a triangular homopolar component is added to the sine wave which is the commonly used method, equivalent to the Space Vector strategy.

$$\begin{cases} MAX = \max\left(V_{1N,ref}\,(t), V_{2N,ref}\,(t), V_{3N,ref}\,(t)\right) \\ MIN = \min\left(V_{1N,ref}\,(t), V_{2N,ref}\,(t), V_{3N,ref}\,(t)\right) \\ V_{off(t)} = -\frac{MAX+MIN}{2} \\ V_{1N_{ref}\,SVPWM} = V_{1N,ref}\,(t) + V_{off}(t) \end{cases} \quad \text{(III-2)}$$

However, in our study, a sinusoidal homopolar at three times the fundamental frequency and amplitude ¼ of the fundamental (equations (III-3)) is used instead of the triangular one as in Fig. III-22.

$$\begin{cases} V_{off}(t) = \frac{M_{ref}}{4}\sin(3 * \omega * t) \\ V_{1N_{ref}\,THIPWM} = V_{1N,ref}\,(t) + V_{off}(t) \end{cases} \quad \text{(III-3)}$$

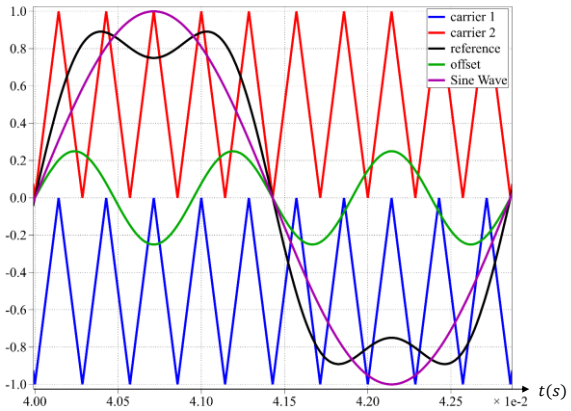


Fig. III-22. 3-level THIPWM1/4 modulation

iv. Full-wave modulation

The full-wave modulation is a low-frequency method which is interesting for high power applications as each semiconductor switches twice per period in which losses minimization is crucial. However, this method has a main drawback which is the low-frequency range harmonics contents. In this part, several full-wave strategies will be shown for 3-level NPC and FC topologies.

1. Full Wave modulation 1 (FW1)

The considered full wave modulation is a 3-level wave (+E/2,0,-E/2) in which, the 0 level duration or α (equation III-4) is used to control the supplied RMS voltage ($V_{s_{rms}}$) or amplitude value ($V_{s_{max}}$), with E the DC bus voltage value (Fig. III-23). The considered switching cell are consisting of components T1 and T3 for the first one and T2 and T4 for the second one. The switches of a switching cell have complementary states ($T3 = \overline{T1}$, $T4 = \overline{T2}$).

$$\alpha = \frac{1}{\pi} * asin\left(\frac{V_{s_{max}}}{2 * \frac{E}{\pi}}\right) \quad \text{(III-4)}$$

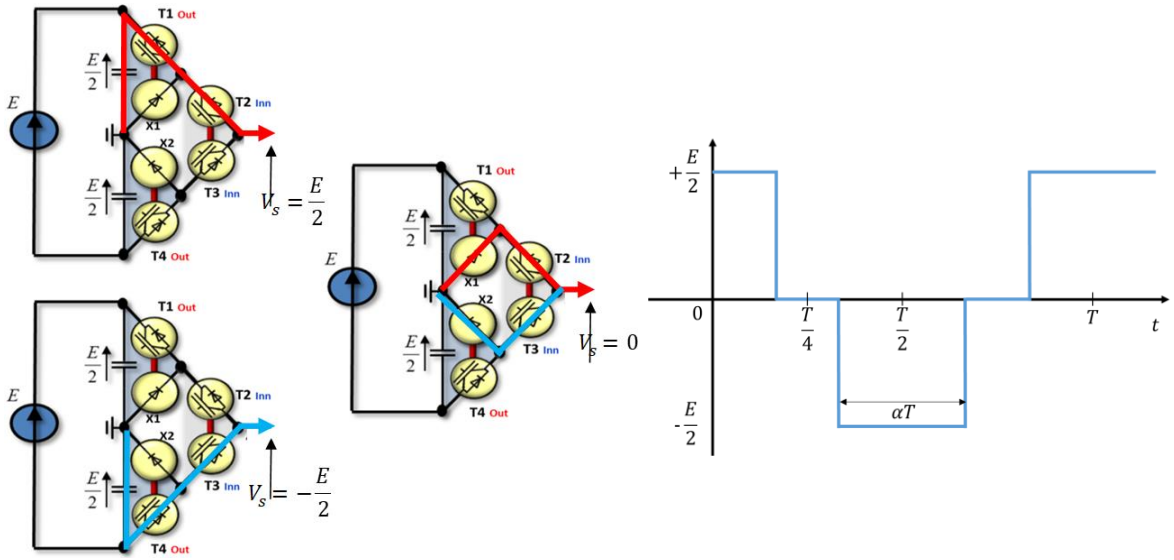


Fig. III-23. Switching cell combinations for 3-level NPC and output desired voltage waveform

This modulation will generate the desired voltage and current waveforms with only low-frequency switching which will reduce the overall power losses of the inverter. Simulation results will be presented later in this chapter. The generated control signals are shown in the following figure (Fig. III-24).

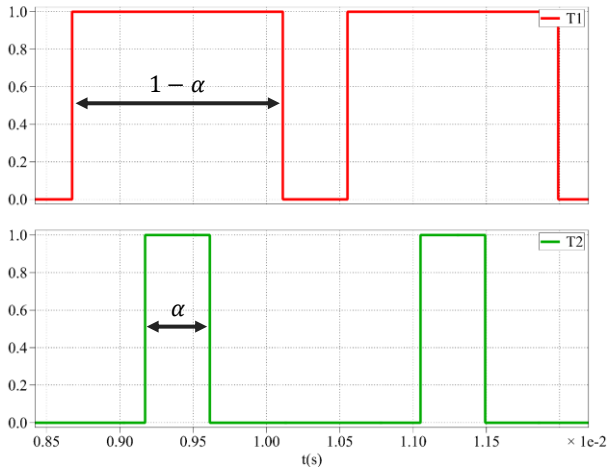


Fig. III-24. T1 and T2 3-level NPC control signals

To obtain the desired output voltage waveform, the two switching cells' control signals are issued of comparison of a constant α (III-4), and a low-frequency triangular wave for the first cell and a half a period delayed triangular wave for the second cell as in Fig. III-25.

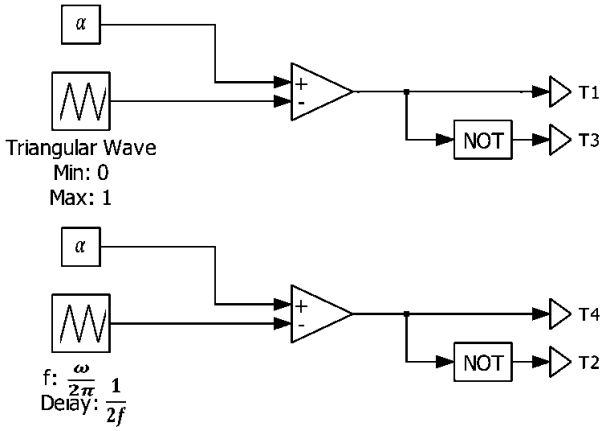


Fig. III-25. Switching cell command schematic

For the 3-level FC topology, we still have the 4 switches states to deal with (same switching cells defined above) in addition to the flying capacitor voltage. Various modulation strategies have been implemented to improve the operation of this inverter, loss distribution and voltage regulation of the flying capacitor. In this simulation, the converter is studied using perfect voltage sources instead of flying capacitors assuming that the voltage of the flying capacitor is perfectly controlled.

For the full-wave modulation called "Full Wave 1", the control of both switching cells are centered, and the duty cycle is chosen to control the RMS voltage value (Fig. III-24). Fig. III-26 shows the different states obtained and the voltage then generated and that this leads to a fixed 0 state which was chosen as in the figure. This leads to an imbalance in the flying capacitor voltage which is only compensated for at the scale of the low frequency period with the current direction inversion. This method unbalances the losses of the switches of this topology, which prevents us from taking advantage of one of the key strengths of this structure, which is the balanced distribution of losses.

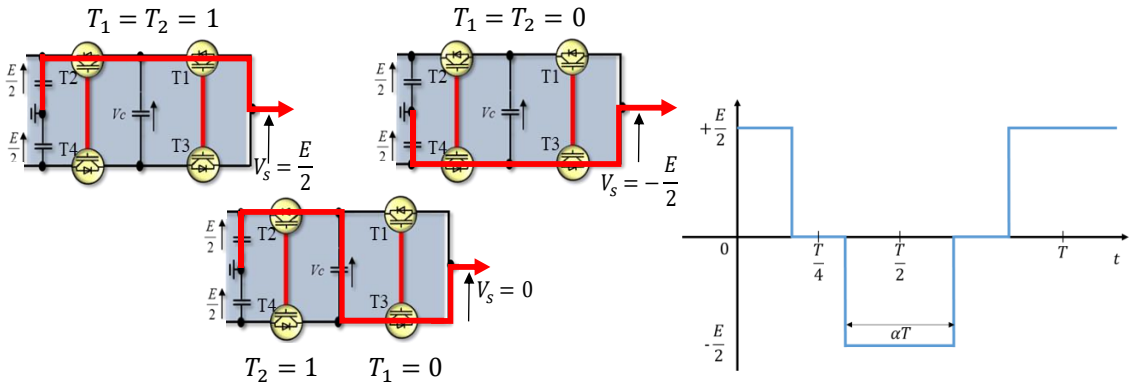


Fig. III-26. Full wave 1 used switches combination

For a DC bus voltage of 2 kV, the needed flying capacitor value is 13.4 mF which is more important than the DC bus capacitor of 1.07 mF. In this case, the flying capacitor is sized according to the low-frequency component of the current with a voltage ripple of 10 %. For the capacitors sizing, chapter II formulas were used.

2. *Full wave modulation 2 (FW2)*

The second modulation idea consists of adding to the "Full Wave 1" command, the combination of the two possible configurations for the 0 voltage level (Fig. III-27), and thus be able to balance the losses of the two switching cells over two periods.

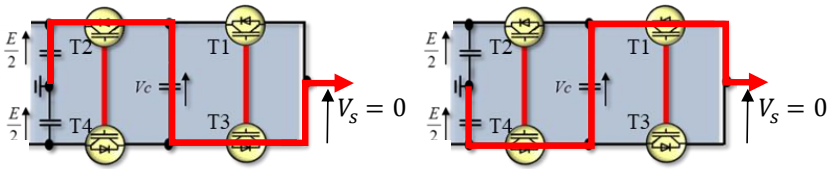


Fig. III-27. 0 voltage level switches combination for full wave 2

The full-wave modulation called "Full Wave 2" is designed as over a first period, switch T1 is primed, and T2 is blocked to create the voltage level at 0 V, and in the following one, switch T2 is primed, and T1 is blocked to generate the 0 V as mentioned in the state machine in Fig. III-28. This command, therefore, balances the losses in the switches over two periods.

This modulation strategy uses the same state machine as for a regular PWM, however, the switching frequency corresponds to the fundamental one.

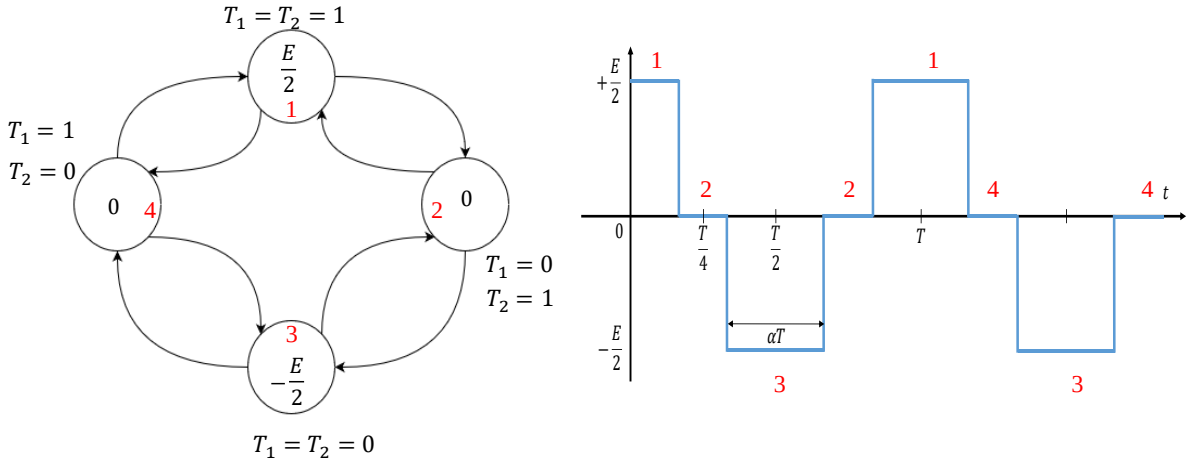


Fig. III-28. FW2 State machine

Fig. III-29 shows the switches T_1 and T_2 control signals that correspond to the previous state machine.

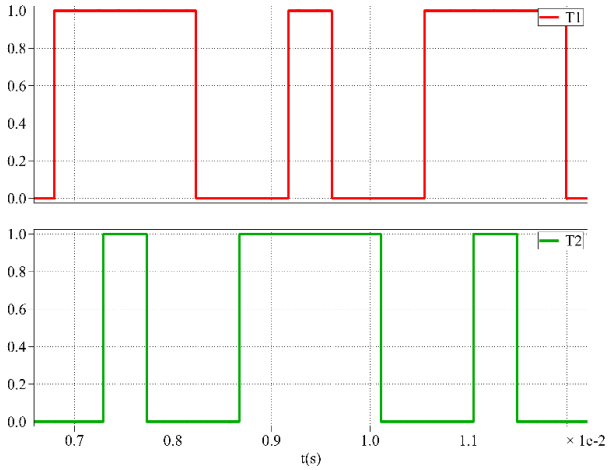


Fig. III-29. T1 and T2 3-level FC full wave 2 control signals

For this modulation, the flying capacitor sizing does not change since the capacitor voltage balancing is done over two low-frequency periods.

3. *Full wave modulation 3 (FW3)*

Following the idea of the previous case, as to improve the losses balancing over a single period, but with a smaller flying capacitor, the "Full Wave 3" was developed. It consists in switching the two switches combinations (over the same period) in high frequency to make the output voltage level at $0\,V$ as shown in Fig. III-30. This will result in a zero average current in the flying capacitor which will help to maintain its voltage at an average value of $\frac{E}{2}$. It also allows a reduction of the size of the flying capacitor.

To maximize the reduction of the flying capacitor weight, the 0 V level could be achieved by switching at a high frequency of 6 kHz which corresponds to about 11 times the electrical machine frequency. This switching frequency engenders a flying capacitor of 1.34 mF as for the PWM strategy.

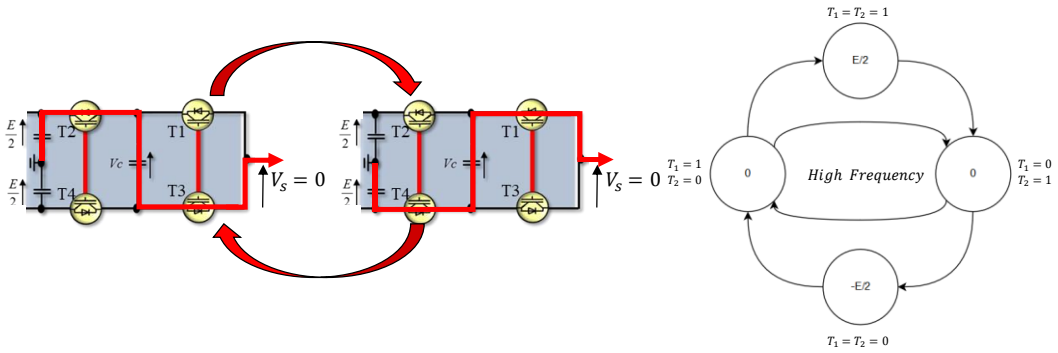


Fig. III-30. Switching at high frequency between the two possible configurations

In this case, using about 6 kHz switching frequency will not be interesting due to the high value of the electrical machine frequency (532 Hz, $T = 1.88\,ms$) and the duration of the 0 V level

which is very short ($\left(\frac{1}{2} - \alpha\right) * T$ with $\alpha = 0.45$). The 0 level lasts for $0.09\ ms$ which is in the same range of the half switching period ($0.083\ ms$) if the used apparent switching frequency is 6 kHz so the 0 level does not appear clearly to include changes of state. The ratio between the two frequencies must be higher for this method to be interesting.

To have more than two commutations, the switching frequency should be higher than 32 kHz. That is why a second example is given in Fig. III-31 with a switching frequency of 60 kHz. This switching frequency engenders a flying capacitor of 0.23 mF.

For the FC topology using full-wave modulation, the study was realized using perfect voltage sources instead of flying capacitors. Flying capacitors' voltage balancing should be taken into consideration. The 0 voltage level phase of the output voltage can be used to balance the flying capacitor voltage at high frequency actively since the current sign is not the same for both configurations. However, this will not change the output waveforms.

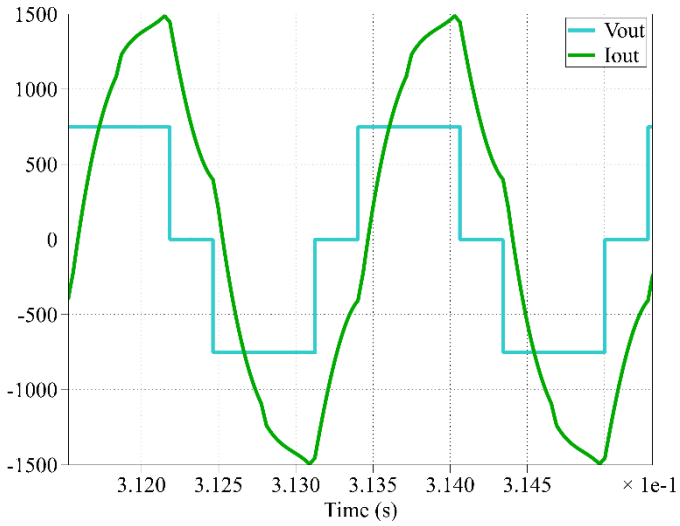


Fig. III-31. Voltage and current waveforms for 3-level FC using full wave 3 for an apparent switching frequency of 60 kHz

The full-wave modulation effect on the THD will be studied in the Chapter IV. To improve this THD, the selective harmonic elimination could be considered as a solution. It is based on harmonic elimination theory. It allows eliminating some low order harmonics by varying the commutation instants. This modulation generates a staircase output voltage waveform. Using this modulation reduces switching losses because each switch is turned ON /OFF once in a switching cycle and switching angles are usually chosen based on specific harmonic elimination or minimization of THD in the output voltage [53]. The control is done by determining the angles α_i (Fig. III-32).

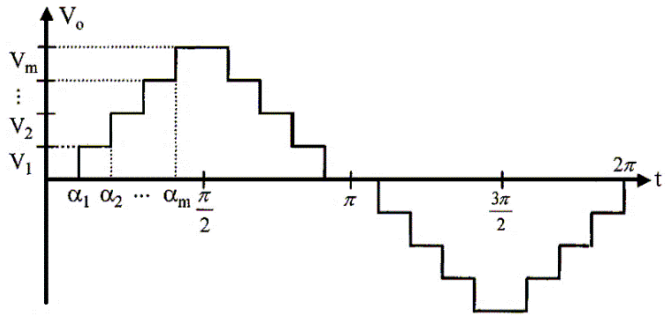


Fig. III-32. Staircase or selective harmonic elimination modulation strategy

v. Comparison of modulation strategies

To compare the different modulation strategies, the following specifications are taken and the results for the 3-level Flying capacitor topology are shown below. The inverter was sized for a DC bus of 2 kV which result in a DC bus capacitor of 2.5 mF using Chapter 2 sizing method.

As noticed in TABLE III-5, DPWM and full-wave strategies have better efficiency. However, for the full-wave modulation, the flying capacitor is sized for the low frequency which results in a bigger capacitor. For the third harmonic injection and discontinuous PWM, the DC bus voltage was sized taking into account the additional 15 % output voltage than the sine PWM and the FW one was sized taking into account the additional 30 % output voltage for the same power point as the sine PWM.

TABLE III-5. 3-level FC performances for different modulation strategies

Topology	**3-level Flying Capacitors**			
Modulation Strategy	PWM	THIPWM1/4	DPWMMAX	Full wave 2
$\boldsymbol{\eta}$ **(%)**	96.54	97.80	97.85	98.09
Temperature (°C)	122	132	137	112
$\boldsymbol{C_{FC}}$ **(mF)**	1.35			5.7

Fig. III-33 shows the losses repartition for the previous modulation strategies. The switching losses could be decreased by changing the used modulation method. However, the conduction losses depend on the components parameters and are not very much affected by the modulation strategy.

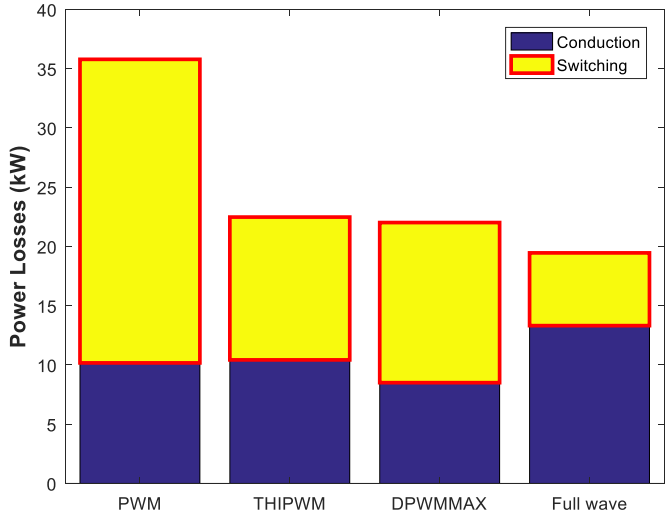


Fig. III-33. Losses repartition for 3-level FC

To optimize the inverter efficiency during the cruise, changing the inverter modulation strategy during the flight could be considered. For example, the inverter could be sized for the cruise with PWM and FW could be used for the takeoff and climb or it could be done using only FW which will be studied in Chapter IV.

3. Comparison of component generations and technology with a chosen strategy and topology

The component choice has a great impact on the inverter performances since the power losses depend on the semiconductor conduction and switching parameters. Several components are available on the market due to the increased demand in the recent years for industrial equipment such as inverters for UPS, wind power and photovoltaic power generation, and due to the rising demand for more efficient and longer lifetime equipment.

i. 7th generation IGBTs

To achieve high efficiency and reliability, Mitsubishi has developed the 7th generation modules that include new thinner IGBT chips and RFC (Relaxed Field of Cathode) diode chips (1200 V, 1700 V products) mounted and an improved internal structure of the unit which reduces power losses. This new generation also maintains a compact and lightweight packaging.

In the 7th generation IGBT module, a new structure is adopted for the NX and std types respectively as in Fig. III-34. The NX type are more compact and lighter than std ones. The internal structure is shown in Fig. III-35. The NX and std types have a low inductance reduced by 30 % compared to conventional models by optimizing the internal layout of the module. The optional pre-applied phase changes thermal interface material and eliminates the grease coating

process. Besides, the NX types are simpler to assembly. The NX and std models offer a wide range of breakdown voltages from 650 V, 1200 V, and 1700 V.

Fig. III-34. NX and std Mitsubishi modules Type packaging

To reduce conduction and switching losses leading to improved module energy-saving performance, the structure of the seventh generation IGBT and MOS charge storage chips has been optimized using thinner wafers. The 7th generation diode chip was manufactured with a thinner wafer which means lower resistance.

ii. 6th generation IGBT vs 7th Generation IGBT (Mitsubishi)

To compare the performances of the Mitsubishi IGBT last generations, Fig. III-35 shows the std type packaging structure evolution and TABLE III-6 sums the main characteristics improvements.

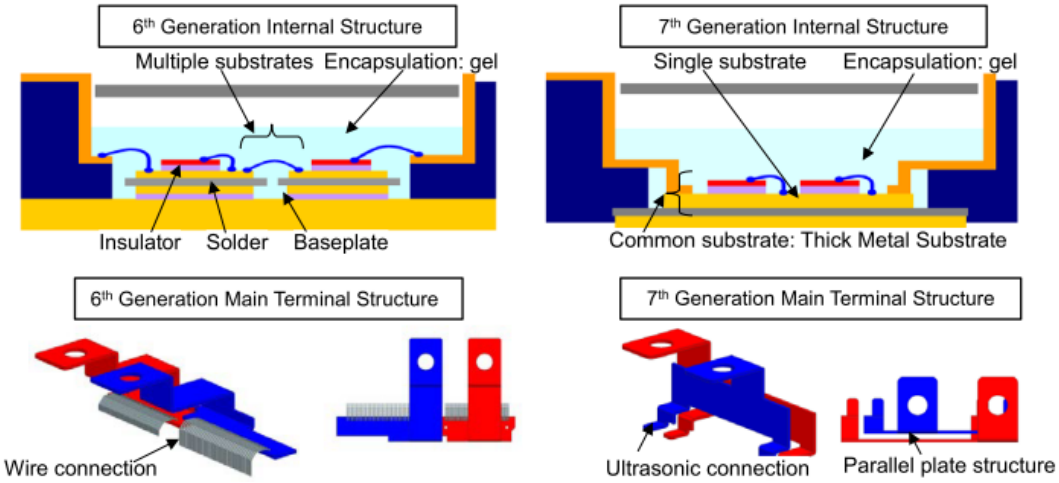


Fig. III-35. Packaging structure (std Type)

By adopting a unique substrate structure and Mitsubishi bonding technology, the mounting surface of the chips has been extended and the nominal current improved in the same housing. The 1200 V / 600 A module, for example, is replaced by a 20 % smaller packaging and the weight is reduced by 45 % compared to the 6th generation.

For the NX type packaging, the same module has been kept and the weight has been reduced by 15 % thanks to a new internal structure. In addition, by increasing the thickness and width of the copper circuit inside the module and using a single optimized substrate structure instead of several conventional insulating substrates, the mounting surface of the chips is expanded to improve the rated current in the same package.

TABLE III-6. 6th vs 7th generation std type module characteristics

Item	**6th gen**	**7th gen**	**Improvement**
Thermal resistance (ratio)	1	0.5	Reduction of 50%
Inductance (ratio)	1	0.7	Reduction of 30%
Package size (W*D*H)	110*80*29 mm	108*62*30 mm	Reduction of 20%
Weight (g)	580	320	Reduction of 45%
Power losses (ratio)	1	0.85	Reduction of 15%

To compare both generations and choose the most suitable component, we started with the 1700 V ones, with a DC bus of 2 kV to fully use the 1700 V module (60 % as mentioned in the Datasheet) in a 3-level architecture. The components are compared using a 3-level NPC with a sine PWM modulation strategy and associating two components in parallel to withstand the imposed current. The inverter performances are shown in TABLE III-7.

TABLE III-7. 6th vs 7th generation 1700 V/ 600 A IGBTs

	6th generation	**7th generation**
Efficiency (%)	97.62	98.94
Conduction losses (kW)	11.05	10.87
Switching losses (kW)	25.60	5.17
Temp junction max (°C)	129	121

Compared to the 6th generation IGBT module, the 7th one has significantly less switching losses for the same specifications. Similar results were obtained for the other studied topologies and modulation strategies. For the same specifications, the losses were reduced by more than 50 % with the 7th generation IGBT modules compared to the 6th one.

To see the difference between the 6th and 7th generation components, a comparison will be done using the 1200 V components which are mostly used in industry and therefore optimized compared to the 1700 V ones, were compared, for a DC bus of 1440 V to use them at 60 % of their voltage rating. The compared results are for a 3-level NPC using a DPWMMAX modulation strategy and associating three components in parallel to withstand the imposed current to withstand the voltage. The obtained results are reported in TABLE III-8.

TABLE III-8. 6th vs 7th generation 1200V IGBTs

	6th gen	**7th gen**
Efficiency (%)	98.64	98.88
Conduction losses (kW)	13.96	11.30
Switching losses (kW)	6.78	5.73
Temp junction max (°C)	112	110

The difference between 6th and 7th generation 1200V components is not huge compared to the previous case due to the lower switching losses as a result of the discontinuous used PWM. However, the 7th generation is still better.

To choose the adapted component, the 1200 V components, which are mostly used in industry and therefore optimized compared to the 1700 V ones, were compared, for DC bus voltages that make them work at 60 % of their rating to fully use installed Silicon. The compared results are for a 3-level NPC using a DPWMMAX modulation strategy and associating three components in parallel to withstand the imposed current for the 1200 V components versus two for the 1700 V ones. The obtained results are reported in TABLE III-9. The 1200 V modules are the best for this application but the 1700 V 7th generation are still interesting; since we will avoid adding one more component in parallel to withstand the current.

TABLE III-9. 7th generation 1200V vs 1700V IGBTs

	1200 V 7th gen **3 in parallel** **1 in series**	**1700 V 7th gen** **2 in parallel** **1 in series**
Efficiency (%)	98.88	98.80
Conduction losses (kW)	11.30	11.55
Switching losses (kW)	5.73	6.38
Temp junction max (°C)	110	121
Total switches number per phase	18	12

The 1700 V modules are adapted to our application and allow to use fewer modules which will reduce the inverter weight and volume.

iii. Silicon Carbide (SiC) vs Silicon (Si) components

To compare both generations to SiC modules and choose most suitable technology, the inverter is designed using 1200 V / 600 A modules, with a DC bus of 1.2 kV to fully use the module (50 % as mentioned in the Datasheet). The compared results are for a 3-level NPC using a sine

PWM modulation strategy and associating two components in parallel to withstand the imposed current. The power was adapted to use only two components in parallel since the DC bus voltage was reduced.

TABLE III-10. 6th and 7th generation 1200V/600A IGBTs vs 1200V/600A SiC module

	1200 V 6th gen 2 in parallel 1 in series	**1200 V 7th gen 2 in parallel 1 in series**	**1200 V SiC 2 in parallel 1 in series**
Efficiency (%)	98.53	98.84	98.51
Conduction losses (kW)	11.4	8.95	14.48
Switching losses (kW)	3.52	2.81	0.679
Temp junction max (°C)	95.6	90.6	111.3

For our specification, the 1200 V Full SiC module does not add much to our solution. Even if the switching losses are low, the conduction losses remain higher than the total losses of the 7th generation module. The used switching frequency is low because it is not necessary to have sinus currents so we do not take fully advantage of SiC technology. Moreover, the thermal resistance is higher for the SiC module so is the junction temperature. Furthermore, SiC technology is only at its beginning and therefore is less advanced than Silicon and may be an interesting option in the future.

4. Total weight repartition

Using the shown topologies, modulation strategies, and 7th generation components, the inverter is designed for the maximal power point and 2 kV DC bus. The efficiencies for 3-level FC and NPC with sine and Discontinuous PWM are shown in TABLE III-11.

TABLE III-11. Efficiencies for the two studied topologies and modulation strategies

Topology	**3-level FC**		**3-level NPC**	
Modulation	PWM	DPWMMAX	PWM	DPWMMAX
Efficiency (%)	98.81	99.01	98.85	98.98

The obtained efficiencies are higher than the 2-level one (92.5 %) shown in chapter I and both 3-level topologies have similar efficiencies. The decisive point will be their total weight which will be compared below.

i. 3D inverter design

To more accurately estimate the total mass, 3D models of the inverter was done on ***Inventor*** to evaluate the weight of the needed bus bar and also the volume of a single phase. The 3D model of the FC inverter is shown in Fig. III-36.

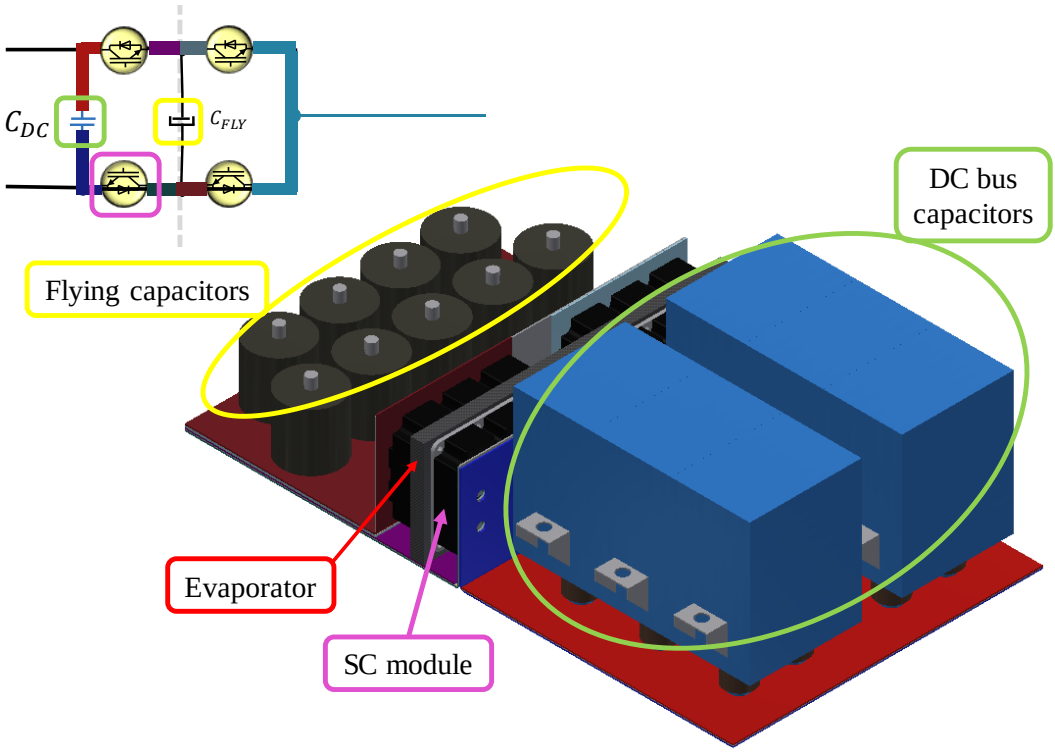


Fig. III-36. 3D single phase 3-level FC inverter

To design the inverter, several constraints should be taken into account. The first one concerns the heat exchanger and the cooling system designed by WP4.

The increasing power and the miniaturization of electronic components make the classical cooling solutions inadequate to evacuate the thermal load generated by chips. It is thus necessary to find and use more efficient and easy-to-integrate solutions [56]. In general, the choice of cooling technology depends on efficiency and performance requirements. The Capillary Pumped Loop for Integrated Power (CPLIP) shown in Fig. III-37, allows a temperature range controllability, like a classical CPL without all the instabilities. High heat flux removing capability is undeniable for this kind of loop. It has a theoretical thermal evacuation capability up to 40 W·cm^{-2}, in our case, we are around 35 W·cm^{-2}. Accorinti et al. [57] have deeply explained the ability to maintain a constant operating temperature on the evaporator walls, where electronics power modules are installed, for any cold source temperature variation and power cycle with large amplitude heat load steps. In particular, Accorinti et al. [32] showed, changing cold source temperature from 5 to 40°C, at constant applied thermal power, that the evaporator wall temperature change was negligible. Moreover, it was demonstrated, parametrizing the reservoir temperature, at constant cold source

temperature and heat power, that it is possible to control the evaporator wall temperature and so to fix the junction temperature.

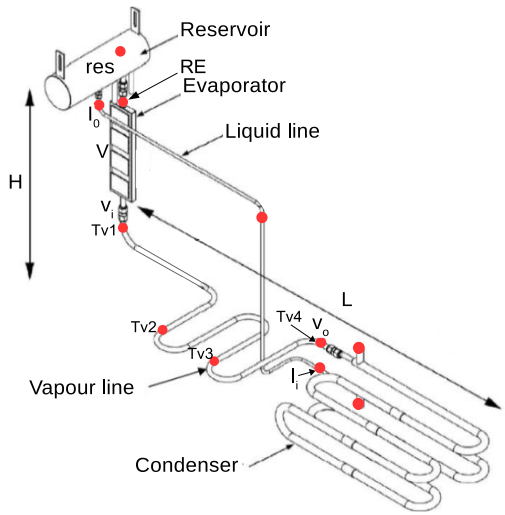


Fig. III-37. CPLIP concept scheme [32]

The four semiconductor module that constitutes one 3-level FC inverter phase, are placed on both evaporator sides as shown in Fig. III-38. This was recommended by WP4 to take advantage of both the evaporator side to evacuate the thermal losses and balance the constraints on both sides. This solution will also help to reduce the volume and weight of the inverter since it creates a more compact inverter and divides by 2 the number evaporators compared to when using only one side of the evaporator. In this case, we end up with 3 evaporators in parallel for the three phases instead of 6.

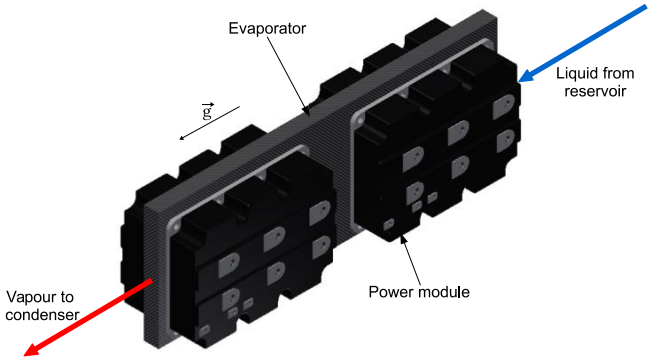


Fig. III-38. Module/evaporator assembly

The second constraint concerns the partial discharge (PD) risk estimated by WP5. Fig. III-39 shows the bus bar points that may be problematic from a PD aspect. The bus bar consists of copper flat bars (2 mm-thick each) connecting input bus capacitors, power modules, and flying capacitors. The DC bus is powered by a 2 kV input voltage. PTFE films are sandwiched between each copper bus bars pairs. In such topology, many triple points (area in the air with both metal and insulator in the neighboring) appear in bus bars/PTFE/air interfaces. These points are well known to be weak points, as the electric field is enhanced in such a particular area. Both confinement and power densities increasing expose electric insulation systems to

more PD risks. Added to materials defects, these partial discharge inceptions locally increase the stress within the dielectric material. This stresses change the intrinsic material properties and reliability, with the consequence of an irreversible insulators damage that can affect the whole insulation system.

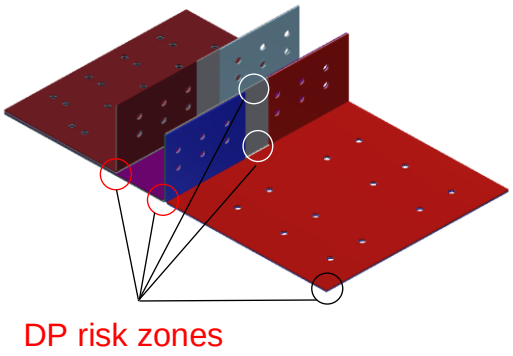


Fig. III-39. Bus bar configuration for a 3-level FC single phase

So to reduce these risks the dielectric used between the copper layers should be thicker. However, if it is thicker this would increase the bus bar stray inductance. This parasitic inductance is responsible for DC bus overshoots and overvoltage spikes across the power semiconductors during switching [58]. As a result, semiconductor device losses increase. In our case, no devices such as snubbers were considered to reduce the overvoltage generated by the leakage inductance.

This inductance could be estimated using *ANSYS Electronic Desktop* and the bus bar CAD model. The evolution of this inductance as a function of the dielectric thickness is represented in Fig. III-40. A trade-off has been made and the dielectric thickness was set to 2 mm.

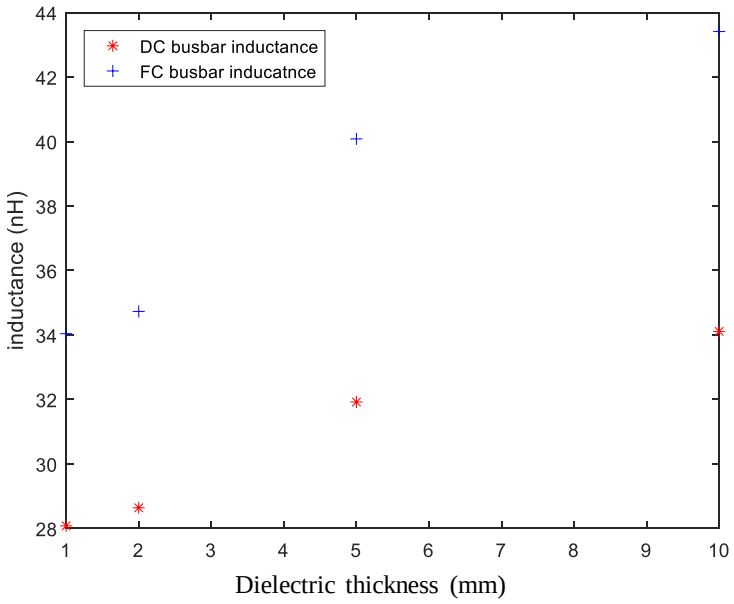


Fig. III-40. Bus bar leakage inductance

As a result of the WP5 study, rounded edges are to be used so to reduce PD risks. A solution without a bent bus bar would be better, however, to use both sides of the evaporator, the bus bar has to be bent.

ii. Specific power comparison

The DC bus capacitors are represented in Fig. III-36 in blue and account for a large amount of the total volume and thus its weight. The used bus bar is made of copper which is mostly used in similar range inverters.

For the weight distribution, it changed and the exchanger is not the predominant anymore but instead, the Bus bar and capacitors are the heaviest components (see Fig. III-41). The cooling system weight accounted for 11 times the semiconductors one for the 3-level NPC (Fig. III-14) versus only 2 times for the last solution using the same inverter topology (Fig. III-41).

Compared to the FC inverter, the NPC one is 26% lighter due to the lower capacitor (lesson flying capacitors) and bus bar weights (17 % less bus bar). It results to a specific power of 14.10 kW/kg for the 3-level that does not match the 2025 target of 15kW/kg unlike the 3-level NPC (19.01 kW/kg) (TABLE III-12).

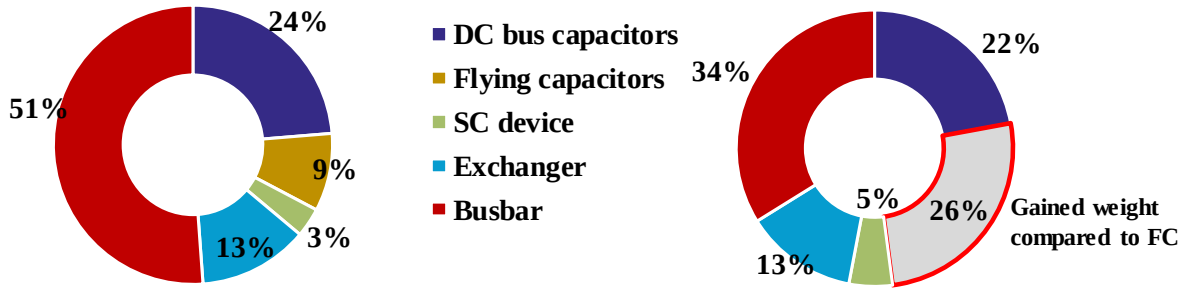


Fig. III-41. 3-level DPWMMAX FC (left) and 3-level DPWMMAX NPC (right) weight distribution

TABLE III-12 Specific power the two studied topologies using DPWMMAX modulation strategy

	3-level DPWMMAX FC	**3-level DPWMMAX NPC**
Specific Power (kW/kg)	14.10	19.01

To compare, for the same topology, the effect of the modulation strategy, used semiconductor and the cooling system weight coefficient, a simulation was done using a 3-level NPC inverter. Both sine PWM and DPWMMAX were compared combined with the 6th generation IGBTs for the first one and 7th generation for the second one. The heat exchanger coefficient went from 0.34 to 1.3 kW/kg thanks to the work of WP4 due to the CPLIP properties [56]. The obtained weight distribution is shown in Fig. III-42. The specific power went from 9.77 kW/kg to 19.01 kW/kg and the 2025 target is reached. However, we are still far from the 2035 one which was 25 kW/kg.

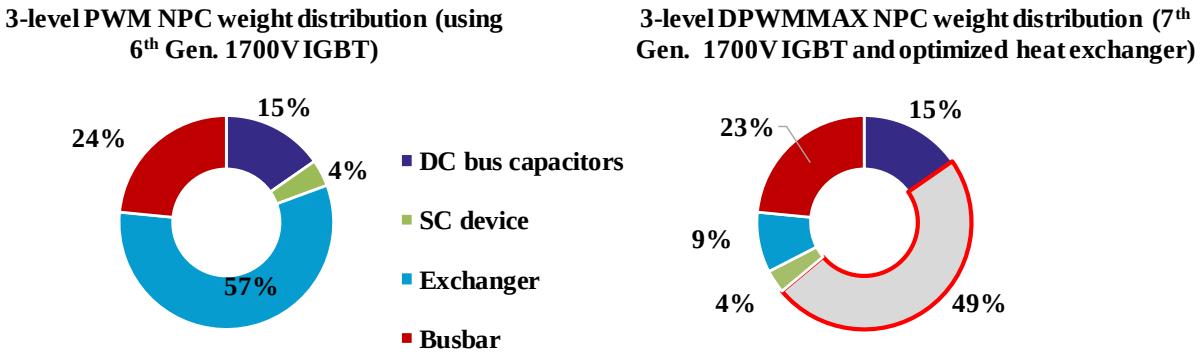


Fig. III-42. 3-level NPC weight distributions

To reach efficiency targets and have a higher efficiency during the cruise, changing the inverter modulation strategy during the flight could be interesting which will be discussed in detail in the next chapter.

iii. Module packaging for bus bar reduction and capacitor weight reduction

Even if there are no power losses in the semiconductors (no need for a heat exchanger), a specific power of 23 kW/kg is reached. In order to achieve the 2035 target (25 kW/kg) the bus bar and the capacitors weights have to be optimized.

To reduce the capacitor weight, it is now designed according to the desired voltage ripple which corresponds here to 5 % instead of sizing it depending on the energy as shown in Chapter II. In this case, the specific power goes from **19.01 kW/kg** to **23.29 kW/kg** for the 3-level DPWMMAX NPC. Moreover, the percentage of the DC bus capacitor weight represents 5.86 % instead of 15.31 % as noticed in Fig. III-43.

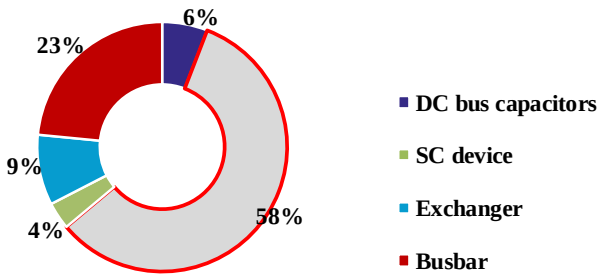


Fig. III-43. 3-level NPC weight distributions with the new sized capacitor

To reduce the Bus bar weight, creating a single-phase power module will remove the bus bar between the power modules and all that remains is the connection between the module and the DC bus capacitors and between the module and the motor phase. This study was carried out in collaboration with ***Deep Concept***. They designed a specific power module for a 3-level single-phase NPC and carried out a 3D design taking into account schematic, dimensional and environmental constraints. Then they did an EMC simulation of the module by finite elements to evaluate the loop inductances and current distribution.

The designed module includes half a phase of the 3-level ANPC or NPC type inverter.

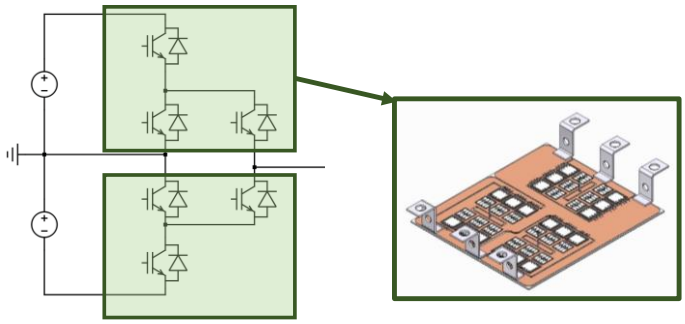


Fig. III-44. Design of a 3-level ANPC inverter power module

The obtained modules are placed on each side on the evaporator as in Fig. III-45.

Fig. III-45. Lower (left) and upper (right) power modules placed on the evaporator

These power modules are so compact that the final 3-phase inverter assembly is smaller as noticed in the different views in Fig. III-46. The bus bar weight is reduced by 56 %.

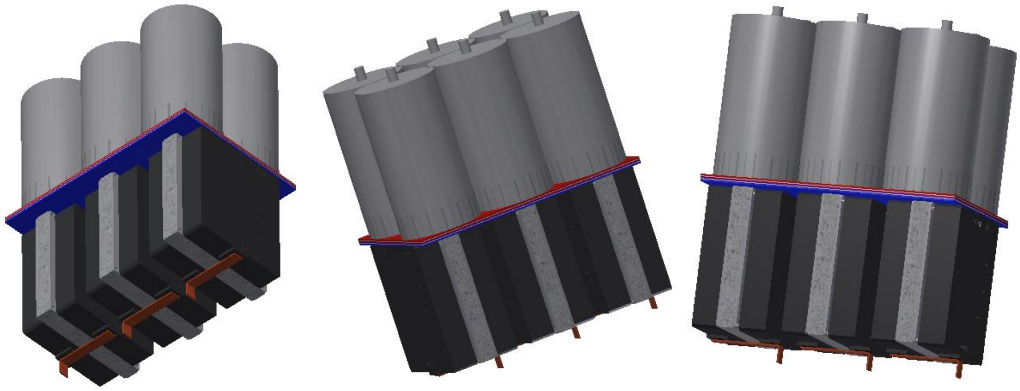


Fig. III-46. 3-level 3-phase NPC inverter with new power modules

The module weight was estimated from the available module that has the same dimensions which is 1.5 kg per module which lead to a total semiconductor devices weight of 9 kg. Fig. III-47 represents the new weight repartition compared to the sine PWM 3-level NPC using 6th generation IGBTs and non-optimized cooling system. The weight is reduced by 83 % which lead to a specific power of 57.59 kW/kg for the inverter including only its cooling system, bus bars, semiconductor modules and DC bus capacitor. The heat exchanger coefficient for this solution is set to 4.5 kW/kg.

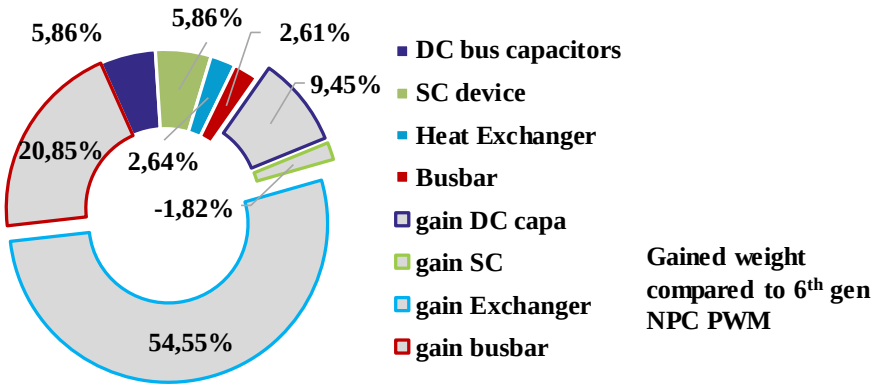


Fig. III-47. 3-level NPC weight distributions with the new sized capacitor and power modules

The obtained specific power seems high but it does not take into account several inverter components such as drivers, snubbers, components attaching elements, etc. To have a more accurate estimation, these parameters should be included. Filters are not also take into account since we do not have network quality constraints to be fulfilled.

5. Conclusion

The main factor to increase the specific power was identified in Chapter I. two options were conceivable. The first one was decreasing the cooling system mass by optimizing its components which was done by WP4 work. The second one was reducing power losses which is a part of our work package (WP2) tasks. Using the simulation tool developed in Chapter II, the inverter design was conducted.

The first point that was covered was the inverter topologies. Inverter power losses reduction could be achieved by using small rating components. This was done by using multilevel architectures to avoid the direct series association. The used topologies were 2, 3 and 5 levels ones. They were compared using DC bus voltage sweeps to find the optimal DC bus voltage range for each group of topologies. If the DC bus voltage is between 700 V and 1 kV, the 2-level topology could be used, however, in this case, to withstand the machine current, several components should be associated in parallel which will increase the inverter weight and volume. If the DC bus voltage is between 1 and 2.4 kV, the 3-level topologies have the best efficiencies for this voltage this range. However, if the DC bus voltage is between 2.4 and 3.5 kV, the 5-level ones must be recommended. This voltage range depends also on the used switching frequency. This parameter is very important especially for the high voltage components that were used and have a great impact on the power losses and therefore the semiconductors maximal junction temperature. The 3-level topologies and the 5-level ANPC seemed to be the most adapted ones to our specification. This study showed also that, so to use some topologies such as 2-level or 3-level ones, they should be used with a low switching frequency so to have an acceptable junction temperature. This means that the sine PWM strategy is not adapted in some cases.

This leads to the second covered point in this chapter which is the modulation strategies. The multilevel modulation techniques could be classified according to switching frequency. High switching frequency modulations have higher switching losses but less impact on the machine current since the high-frequency filtering is better than low-frequency one. Therefore, with low switching frequency methods, efficiency is higher. In this work, four modulation strategies, which are sine PWM, Third Harmonic Injection PWM, Discontinuous PWM MIN and MAX, and Full Wave adapted to 3-level inverter topologies, were studied and compared in terms of efficiency so to find the most performant. The sine PWM had the lowest efficiency among all the topologies but still near to the others' performances. The DPWMMAX was the one with the highest efficiency for both studied 3-level topologies.

The third tackled point was semiconductors technologies. The component choice has a great impact on the inverter performances since the power losses depend on the semiconductor conduction and switching parameters. The market evolution of silicon components seemed to be saturated in recent years. However, with the new Mitsubishi 7th generation IGBT module, this is not the case anymore. These components have fewer losses and come in a compact light-weighted packaging. These components were compared to the previous IGBT generation and also to SiC modules with the same current and voltage calibers and seems to be the best option for our specifications.

Using these components, the DPWMMAX modulation and an optimized cooling system with a 3-level NPC topology, the 15 kW/kg specific power target was exceeded (23.29 kW/kg) but it stills far from the 2035 one which is 25 kW/kg. To reach the second target, a specific power module was designed so to integrate half a phase in a single module. This solution reduced the used bus bar and make it possible to achieve a specific power of 57.59 kW/kg for the 3-phase inverter taking into account only the bus bar, DC bus capacitor, semiconductors and its cooling system. To have a more accurate estimation, parameters such as drivers and components attaching elements should be included.

As noticed in the mission profile presented in Chapter I, three sizing points can be considered, however in this chapter only the takeoff power point was considered. In the next chapter, several modulation strategies and sizing points will be studied so to find out the best scenario for the 3-level inverter modulation strategies taking into account the flight mission.

IV. Performance of the chosen solutions during the mission profile

The developed tool presented in Chapter II makes it possible, from a specification to size the converter according to the chosen topology and carry out parametric studies to determine the optimum sizing point by varying: the DC bus voltage, the requested power or the modulation index. It can also take into account the aircraft mission profile that allows checking the performances of the converter as a function of time [28].

The considered power mission profile is shown in Fig. IV-1. Three sizing points can be considered. The first one consists of sizing the inverter for the take-off which corresponds to the maximum power along the profile; the second one would be the cruise phase which represents the most extended phase of the flight mission; a middle point for the third case (climb phase). The maximum power is in the range of MW and due to confidentiality issues, the value of the maximum power cannot be given: all values will be given in per unit.

Two targets in term of efficiency for the power electronics were set by HASTECS project. For the 2025 target, the efficiency should be higher than 98 % for the cruise point and higher than 96.5 % for the maximal power point. On the other hand, for the 2035 target, the efficiency should be higher than 99.5 % for the cruise point and higher than 99 % for the maximal power point.

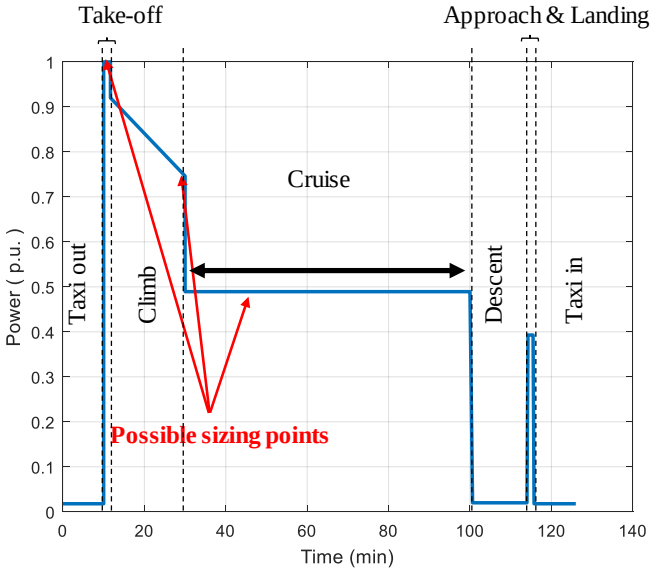


Fig. IV-1. Electrical power mission profile

The main objective of this chapter is to evaluate the chosen inverter topologies and associated modulation strategies to power the electric machine used for the aircraft propulsion. A comparative study of modulation control strategies is carried out to highlight the structure and modulation presenting the best performance to minimize the losses for the chosen sizing point associated 3-level FC and NPC topologies.

1. DC bus voltage sizing and components choice depending on the voltage mission profile and control strategy

To define the needed DC bus voltage and appropriate modulation strategy, the output needed voltage magnitude during the flight mission profile was plotted for two electric motors winding configurations sized by WP1 (Fig. IV-2 and Fig. IV-3). The first configuration uses two conductors per slot and needs less voltage but more current than the second one (3 conductors per slot) since they are both sized for the same power.

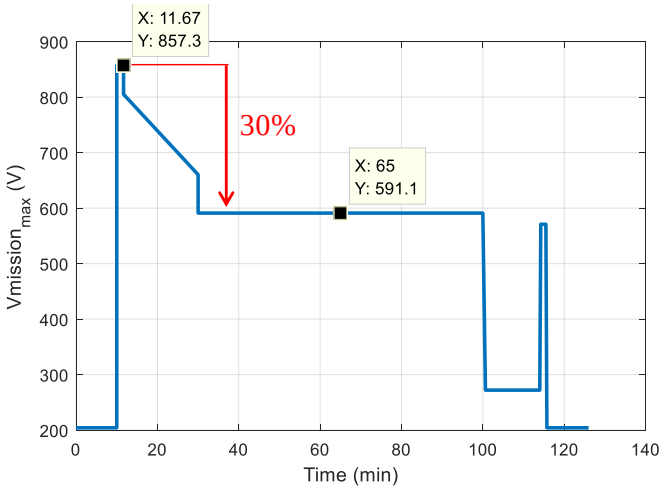


Fig. IV-2. Needed machine voltage during the flight mission with the first e-motor winding configuration

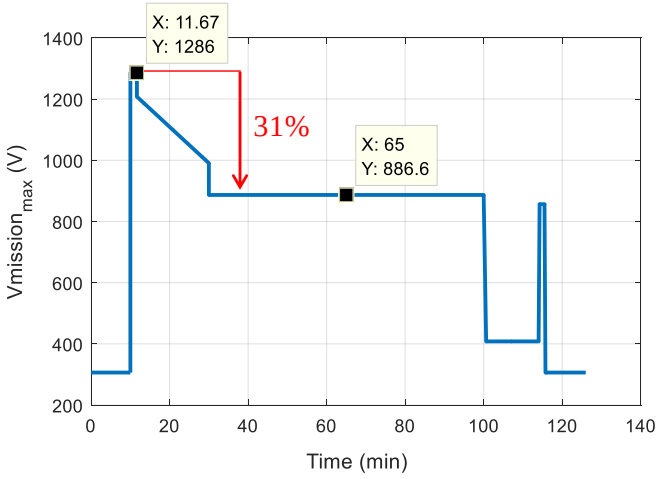


Fig. IV-3. Needed machine voltage during the flight mission with the second e-motor winding configuration

A 30 % voltage difference between the maximal power point which corresponds to the take-off and the cruise is noticed for both studied electric motor winding configurations. Based TABLE III-4, using full-wave modulation for the take-off and climb phases and PWM for the cruise could be considered to optimize the efficiency during the longest phase which is the cruise.

The DC bus voltage, as in equation (IV-1), is defined so to be able to provide the maximal needed voltage and the modulation index which based on the used modulation strategy as in TABLE IV-1.

$$V_{DCbus} = \frac{2*Vout_{max}}{mod\_index} \quad \text{(IV-1)}$$

TABLE IV-1. Maximal output voltage as function of DC bus voltage and control strategy

	PWM	**THIPWM / DPWM**	**Full wave**
$\boldsymbol{V_{out\_max}}$	$\frac{V_{DCbus}}{2}$	$1.15 * \frac{V_{DCbus}}{2}$	$1.3 * \frac{V_{DCbus}}{2}$

For the first electric motor, if only PWM is used which corresponds to a modulation index of 0.9 to take into account the dead time of the switching operations, the DC bus voltage should be equal to 1.9 kV versus 1.5 kV if third harmonic injection or discontinuous PWMs were to be used. However, if the full-wave modulation is used for the maximal power point, the DC bus voltage should be around 1350 V.

For the second electric motor configuration, if only PWM is used, the DC bus voltage should be around 2300 V versus 2250 V if third harmonic injection or discontinuous PWMs were to be used. If the full-wave modulation was to be used for the maximal power point, the DC bus voltage should be around 2 kV.

TABLE IV-2 sums up the required DC bus voltage values for both machine configuration depending on the used modulation strategy.

TABLE IV-2. DC bus voltage value for the different studied modulation strategies and electric motor winding configurations

		PWM	**THIPWM / DPWM**	**Full wave**
$\boldsymbol{V_{DCbus}}$	1st e-motor	1900 V	1500 V	1350 V
	2nd e-motor	2300 V	2250 V	2000 V

2. Inverter performances during the mission profile

In this part, the studied modulation strategies performances will be compared for the entire mission profile. The adapted DC bus voltage and semiconductors choice will be explained for each case.

The first studied cases will be done using PWM strategies. So to not oversize the inverter, it will be sized for the maximal power point (takeoff) using the third harmonic injection PWM which will be used during takeoff and climb and Sine PWM will be used for the remaining parts of the flight mission (cruise, taxi out and in and descent).

The second study case compares two modulation strategies that have the same required DC bus voltage which are THIPWM and discontinuous PWM. The third one will be using only full-wave modulation for the whole flight mission and then used in combination with other PWM strategies to find the most efficient combination for these inverters the flight mission.

i. Strategy 1: Sine PWM and THIPWM

For the PWM strategy, the DC bus voltage is fixed to 1500 V to have a modulation index of 1.15 at the maximal power point. For the take-off and climb, third harmonic injection PWM will be used. Fig. IV-4 represents the efficiencies of 3-level FC and 3-level NPC inverters during the mission profile.

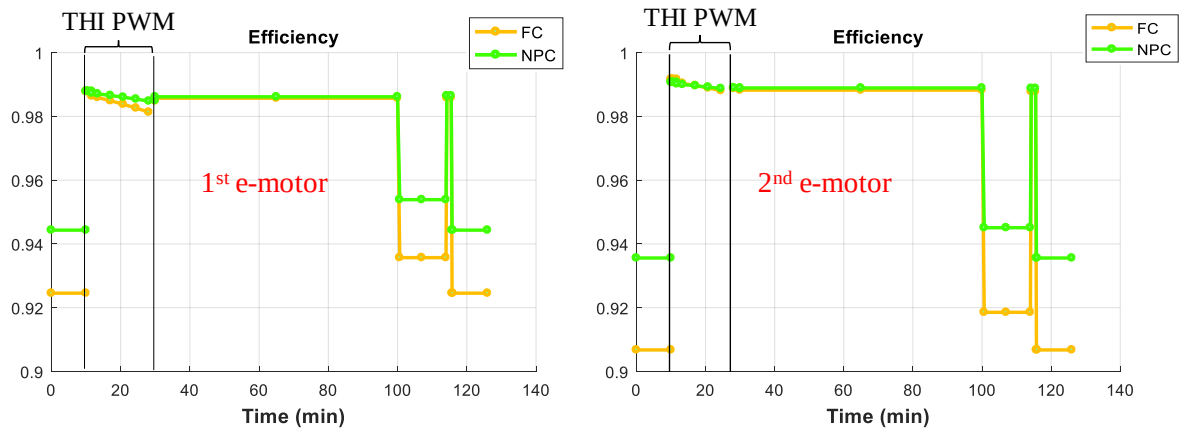


Fig. IV-4. 3-level FC and NPC efficiencies using PWM strategies with both e-motor winding configurations

By sizing the inverter for the maximal power point with a THIPWM, the efficiency in the cruise phase is maximized. For this sizing, 1700 V IGBTs are used at 44 % of their voltage rating for a 1500 V DC bus voltage for the first e-motor and used at 66 % for a DC bus voltage of 2250 V.

The difference between both topologies is negligible for the take-off, climb and cruise phases, however for the taxi out and in, the difference is more important. This is due to the switching losses that are 35 % higher for the FC than the NPC topology in this particular case. For the first point of the mission profile, which corresponds to the taxi-out phase, the total IGBTs' equivalent losses are similar for both topologies. However, for the Diodes, only the conduction losses are similar. The reverse recovering losses are 7 times higher for the FC topology; 709 W versus 101 W for the NPC topology. Several parameters could be leading to this situation. The main reason is the higher switched current and its repartition in the different diodes which is not symmetrically done in the NPC. It is also due to the current-voltage phase shift which depends on the electric machine parameters. The current-voltage phase shift which depends on the electric machine parameters in this phase is almost equal to 0. In this case, only the IGBTs and clamping diodes are used to create the 3-level voltage waveform as in Fig. IV-5. To create the high level ($+\frac{E}{2}$) the current is positive and goes through T1 and T2. For the 0 level with a positive current, it goes through the clamping diode X1 and T2. If the current is negative, it

goes through X2 and T3and to creat the low level ($-\frac{E}{2}$), the current is still negative and goes through T3 and T4. So the D1, D2, D3, and D4 diodes do not see the current therefore don't have additional losses.

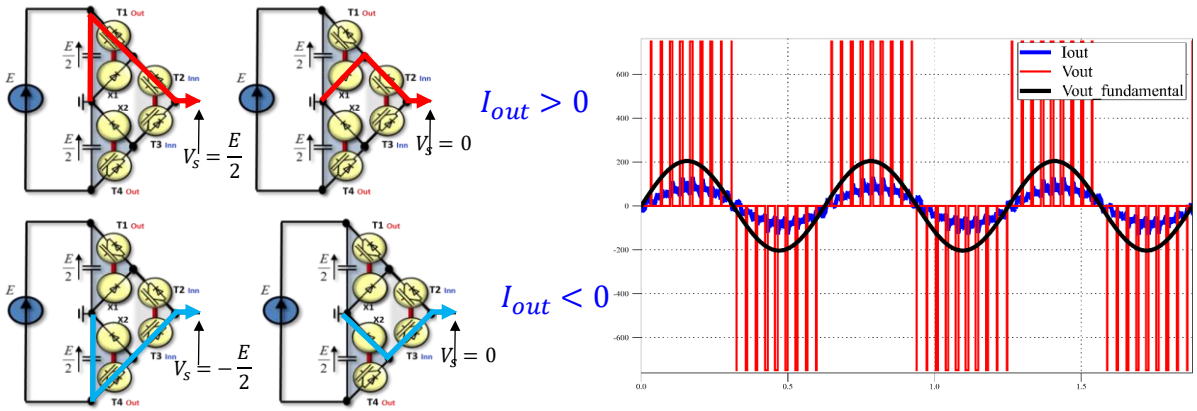


Fig. IV-5. 3-level NPC current repartition during Taxi out phase

The use of the second machine parameters increases the efficiency of the inverter since for the same power, the used DC bus voltage is higher and therefore the current is lower, which reduces power losses in semiconductors.

ii. Strategy 2: THIPWM versus DPWM

For the third harmonic injection and discontinuous PWMs, the modulation index could reach 1.15 so the chosen DC bus voltage is 1500 V as for the previous case using the 2-conductor per slot machine parameters. However, this time, these modulations are used during the whole flight mission to find out the best one to use for each flight phase.

Fig. IV-6 presents the efficiencies of 3-level FC and NPC topologies using third harmonic injection PWM and discontinuous PWM max strategies. The last one has better results overall the mission profile. This is due to the conduction losses that are higher for the first strategy. Yet, the difference or the gap between both inverter topologies during low power phases is still noticeable no matter what modulation strategy was used. However, for the DPWMMAX, the situation is reversed; the NPC has higher losses than the FC which is due to the unbalanced power losses and currents repartition caused by this control strategy that reduces significantly the switching power losses.

For the second motor winding configuration, the overall efficiencies are better than the previous case but still, the same remarks apply to this case as above. In this case, the 1700 V IGBTs are used for about 66 % of their voltage rating they are slightly overused. However, the maximal junction temperature does not increase much due to the low losses. For the high power phases; take off, climb and cruise, the efficiencies are higher compared to the previous machine ones because the components are optimally used as the manufacturer advises to use it around 60 % of its voltage rating and the conducted and switched currents are lower.

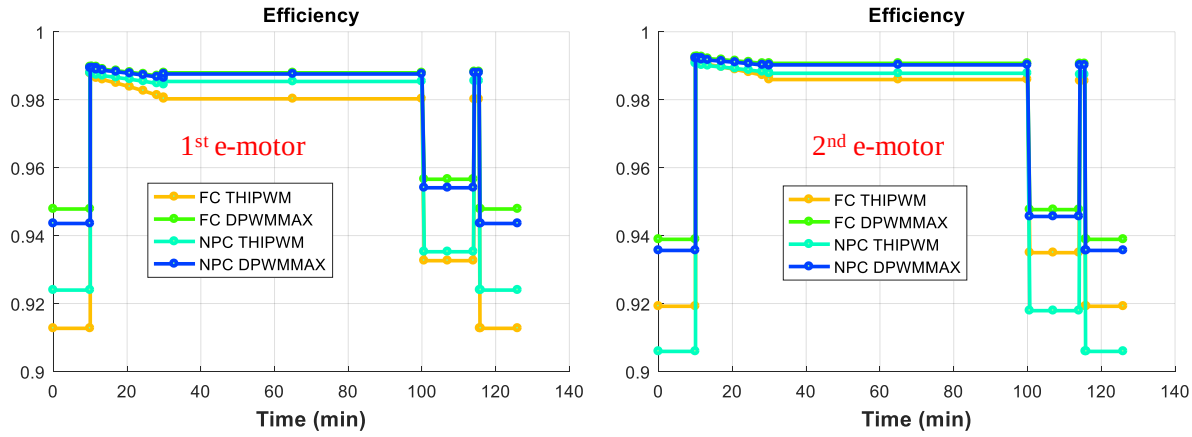


Fig. IV-6. 3-level FC and NPC efficiencies using THIPWM and DPWMMAX strategies with both e-motor winding configurations

We propose now to compare only the discontinuous strategies (Fig. IV-7).

For the FC topology, the converter is fully symmetric so if the modulating signal is saturated in the top or bottom it will not have an impact on the converter operation which is exactly what was obtained and shown in the efficiency plot below. On the other hand, for the NPC, the current sign determines its path used for the current, this implies that the losses are not symmetrically distributed in the inverter. In this studied case, the DPWMMAX has better performances than the MIN for the 3-level NPC.

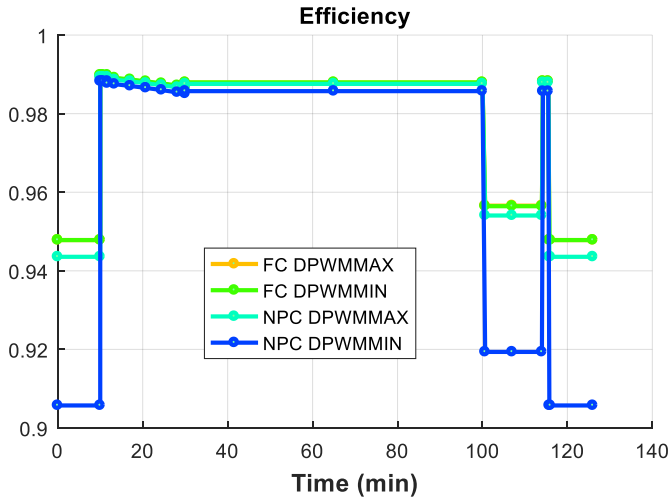


Fig. IV-7. 3-level FC and NPC efficiencies using DPWMMAX and DPWMMIN strategies for the 1st e-motor winding configuration

So the best modulation to use to minimize the overall power losses is the DPWMMAX.

The current THD, which is calculated as in equation (IV-2), is then evaluated for the 3-level FC using the DPWMMAX and reported in TABLE IV-3. The obtained THD values remain acceptable.

$$THD = \frac{\sqrt{\Sigma \ \ I_n^2}}{I_1} \tag{IV-2}$$

With I_1 the current fundamental amplitude and I_n the amplitudes of the harmonics.

TABLE IV-3. THD for some mission profile points for the 3-level FC using DPWMMAX modulation for the 1st e-motor winding configuration

Flight phase	Current THD
Taxi out & in	0.13
Take-off	0.05
Cruise	0.08
Descent	0.76

This modulation strategy has a low current THD so it will not degrade the output waveforms.

iii. Strategy 3: Full-wave modulation

For the 3rd strategy, the DC bus voltage is fixed to 1350 V to have an equivalent modulation index of 1.30 for the maximal power point. Fig. IV-8 shows the efficiencies of both inverters during the mission profile using only full-wave modulation. In this case, the 1700 V IGBTs will be used for about 40 % of their installed silicon so they will be underused and will not have optimal efficiency. The low efficiency is due also to the high conducted and switched current which is a consequence of the lower DC bus voltage for the same needed power.

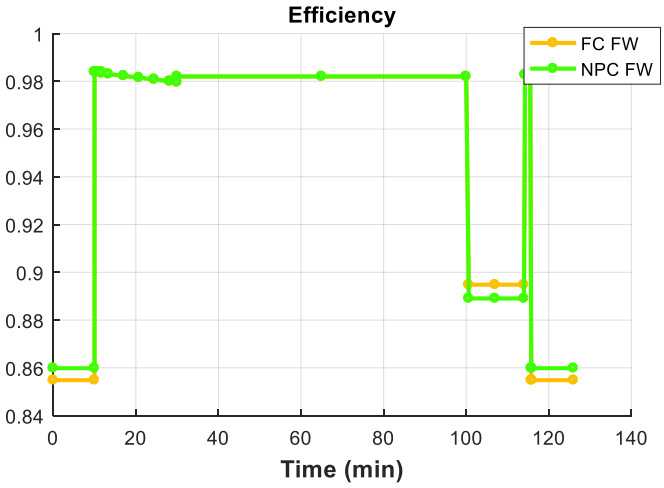


Fig. IV-8. 3-level FC and NPC efficiencies using FW strategy with the 1st motor winding configuration

The FW modulation strategy is a low-frequency modulation strategy, therefore, the output current waveforms are impacted which can lead to more low-frequency harmonic components. This can deteriorate the current THD that is calculated using equation (IV-2), which will increase the electric motor losses.

The efficiencies during the taxi out & in and descent (low power and speed phases) are low compared to the PWM results for the same points. The current waveforms for the different flight mission phases are shown in Fig. IV-9. The losses and current THD are high due to the 5th and 7th harmonic components as noticed in TABLE IV-4. For the takeoff and cruise, the full-wave modulation does not alter the THD unlike what was expected. This is due to the used high-speed synchronous machine thanks to its low inductance that results in a higher reactance and to the electromotive force presence.

TABLE IV-4. THD and harmonics amplitudes for some mission profile points for the 3-level FC using full wave modulation

Flight phase	THD	Fundamental amplitude (A)	5th harmonic amplitude (A)	7th harmonic amplitude (A)
Taxi out & in	4.03	97.55	303.3	165
Take-off	0.059	1633	78.61 (4.8%)	31.64 (1.93%)
Cruise	0.078	1021	74.24 (7.2%)	53.38 (5.22%)
Descent	1.14	81.97	57.99	59.56

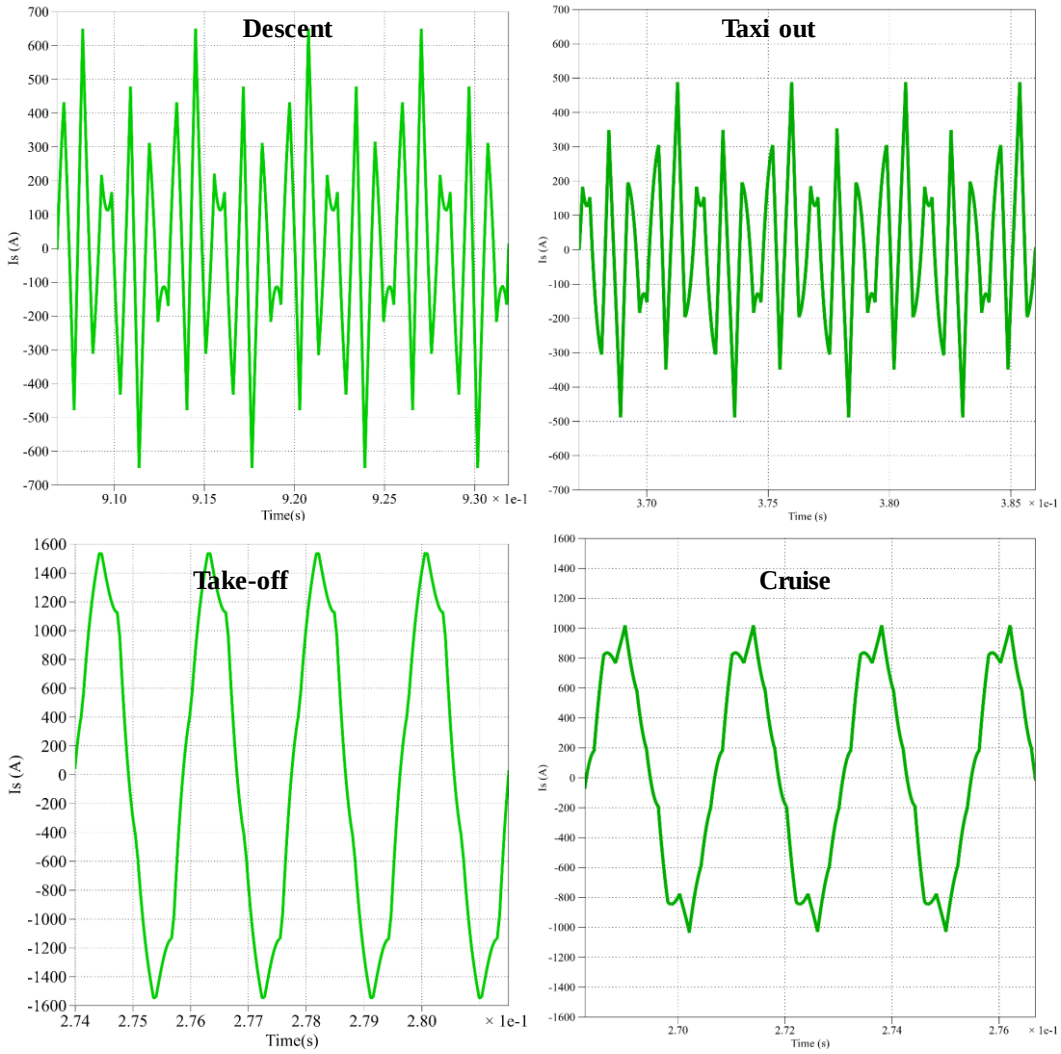


Fig. IV-9. Current waveforms for Taxi out, take off, cruise and descent using the 1st motor winding configuration

For the second studied machine configuration, the DC bus voltage is fixed to 2 kV to have a modulation index of 1.28 for the maximal power point. Fig. IV-10 presents the efficiencies of both inverters during the mission profile using only FW modulation.

In this case, the 1700 V IGBTs will be used for about 59 % of their installed silicon. For the high power phases (take off, climb and cruise), the efficiencies are higher compared to the previous machine ones because the components are optimally used as the manufacturer advises to use it around 60 % of its voltage rating. The low efficiencies during the taxi out & in and descent are due to the high losses and 5th and 7th harmonic current components as shown in TABLE IV-5 as for the previously studied machine.

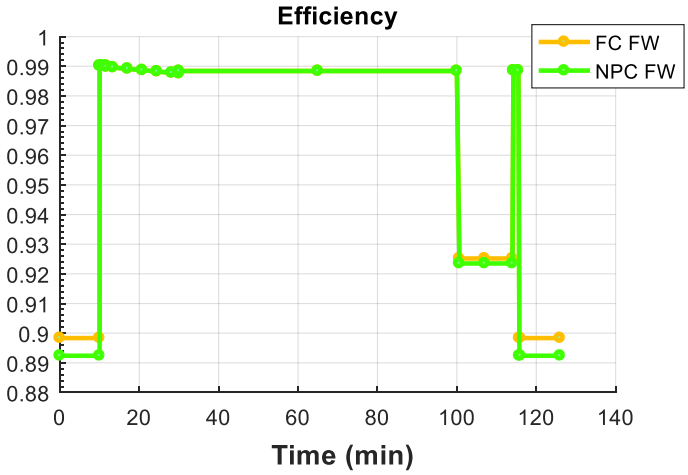


Fig. IV-10. 3-level FC and NPC efficiencies using FW strategy with the 2nd motor configuration

TABLE IV-5. THD and harmonics amplitudes for some mission profile points for the 3-level FC using full wave modulation with the 2nd motor configuration

Flight phase	**THD**	**Fundamental amplitude (A)**	**5th harmonic amplitude (A)**	**7th harmonic amplitude (A)**
Taxi out & in	4.01	57.70	201	108
Take-off	0.078	965.2	64.35 (6.6%)	32.8 (3.3%)
Cruise	0.106	605.77	52.7 (8.6%)	33.12 (5.4%)
Descent	3.6	48.47	160.6	62.1

The full-wave modulation strategy increases efficiency during the takeoff, climb, and cruise. However, during the low power, the efficiency is very low as well as the current THD due to the high 5th and 7th harmonic components that are a result of the low modulation strategy.

iv. Strategy 4: hybrid modulation using Sine PWM and FW

For the 4th strategy, the 1st electric machine configuration was considered and thus the DC bus voltage was fixed to 1350 V to have a modulation index of 1.3 for the maximal power point and a modulation index around 0.9 during the cruise. For the take-off and climb, full-wave modulation will be used and PWM for the remaining parts of the mission so to have better

waveforms than during these phases. The same semiconductors are used even if they are oversized (Fig. IV-11). For the first case, 1700 V components are used to compare it to the previously studied cases.

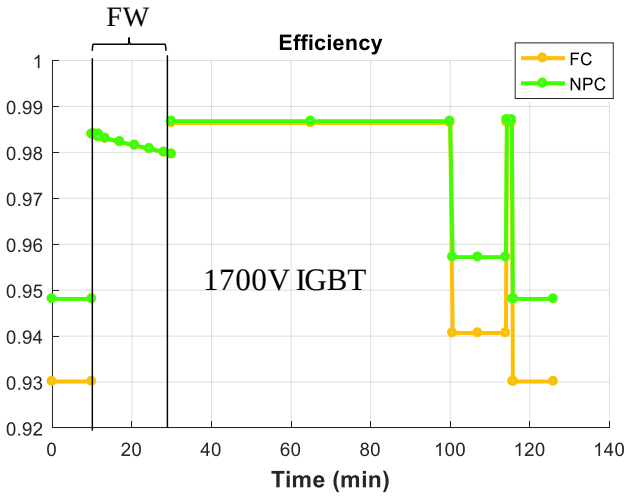


Fig. IV-11. 3-level FC and NPC efficiencies using FW and PWM strategies with 1700 V IGBTs

Compared to the third harmonic injection which had an efficiency of 98.79 % for the 3-level FC during the takeoff, the FW has lower efficiency (98.4 %). However, if more adapted components are used as in Fig. IV-12, the takeoff efficiency is slightly 98.81 %. The overall efficiency is better than the sine PWM combined with third harmonic injection. The 1200 V IGBTs are used up to 56 % of their voltage rating. Even if they are slightly overused, the maximal junction temperature (< 110 °C) is still lower than the manufacturer's thermal limit of 150 °C.

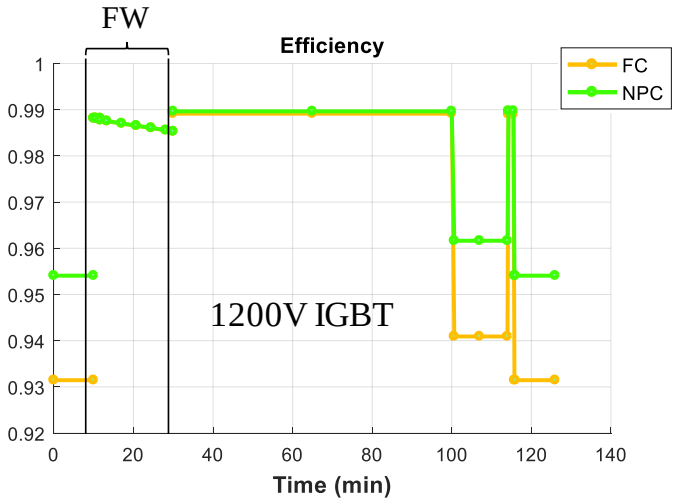


Fig. IV-12. 3-level FC and NPC efficiencies using FW and PWM strategies with 1200 V IGBTs

For the 2nd electric machine configuration, the DC bus voltage was fixed to 2 kV to have a modulation index of 1.28 for the maximal power point and a modulation index around 0.9 during the cruise. As for the 1st machine configuration, full-wave modulation is used for the take-off and climb and PWM for the remaining parts of the mission (Fig. IV-13). Compared to

the third harmonic injection (3-level FC efficiency during the takeoff 99.07 %), the FW has lower efficiency for the take-off (99.02 %) and climb but the cruise efficiency using PWM with this DC bus voltage and components is better which was the one needed to be optimized. For the cruise, the efficiency with this configuration is 98.97 % for the 3-level FC which is higher than the one for the first strategy (THIPWM + PWM) which was equal to 98.89 %.

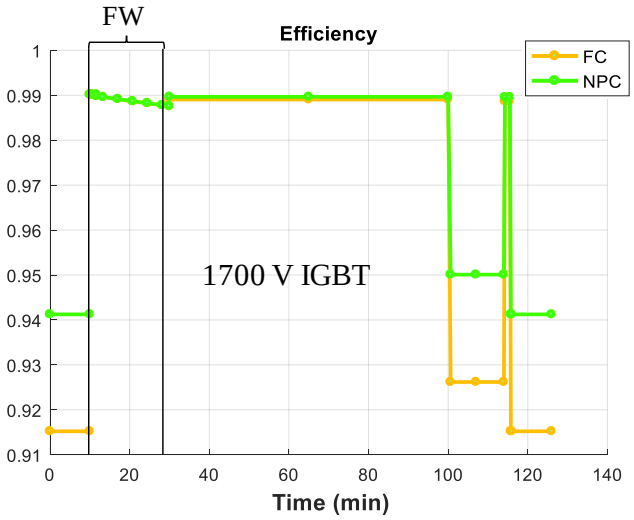


Fig. IV-13. 3-level FC and NPC efficiencies using FW and PWM strategies with 1700 V IGBTs for the 2nd e-motor

TABLE IV-6 shows the current THD and 5th and 7th harmonics amplitudes for the 2nd electric machine configuration using full-wave for the take-off and climb and sine PWM for the remaining parts of the mission profile. We can clearly see that using the combination of both strategies for the studied mission profile improves the overall current THD and inverter efficiency.

TABLE IV-6. THD and harmonics amplitudes for some mission profile points for the 3-level FC using full wave and PWM modulation for the 2nd e-motor configuration

Flight phase	THD	Fundamental amplitude (A)	5th harmonic amplitude (A)	7th harmonic amplitude (A)
Taxi out & in (PWM)	0.82	57.70	0.015	0.014
Take-off (FW)	0.078	965.2	64.35	32.8
Cruise (PWM)	0.077	605.77	0.25	0.49
Descent (PWM)	1.15	48.47	0.03	0.03

The FW strategy combined with a sine PWM improves the inverter efficiency during the cruise which was our objective. This reduces also the current THD during the low power phases which improve the waveforms.

v. Strategy 5: DPWMMAX and FW modulation

For this 5th strategy, the 2-conductor per slot electric machine configuration was considered and thus the DC bus voltage was fixed to 1350 V to have a modulation index of 1.3 for the

maximal power point. For the take-off, full-wave modulation will be used and DPWMMAX for the remaining part of the mission (Taxi out and in, climb, cruise and descent). The 1700 V semiconductors are used even if they are oversized (Fig. IV-14). These components are used at 40 % of their voltage rating.

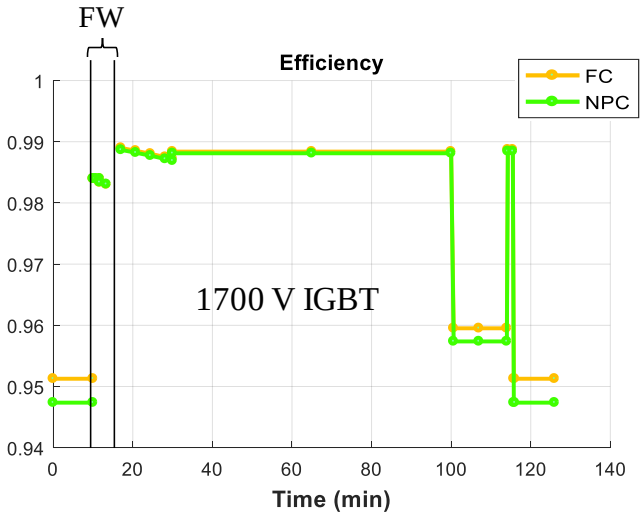


Fig. IV-14. 3-level FC and NPC efficiencies using FW and DPWMMAX strategies with 1700 V IGBTs

The efficiency is higher than for the previous combination (FW + sine PWM), which was 98.64 % during the cruise for the NPC topology and is equal to 98.84 % with this strategy. However, if 1200 V components that are more adapted to this voltage are used at 56 % of their rating as in Fig. IV-15, the efficiency is even better due to this component's parameters and is equal to 99.06 %. The maximal junction temperature is still lower than the manufacturer's thermal limit of 150 °C as for the previously studied case.

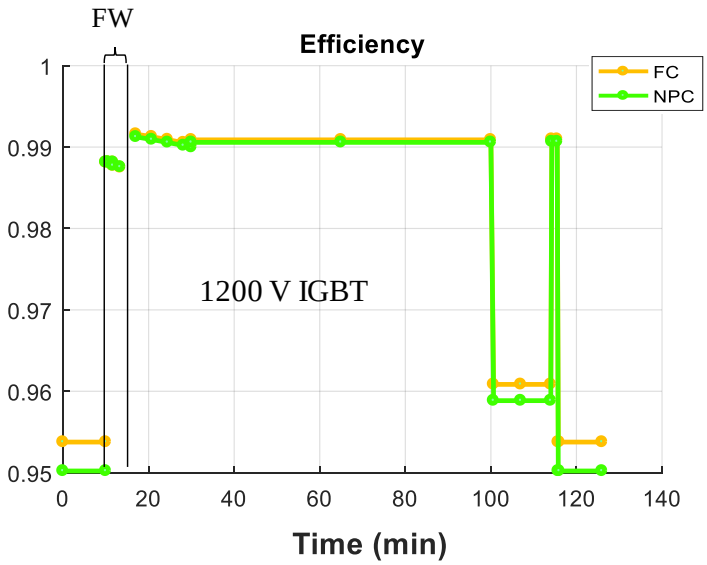


Fig. IV-15. 3-level FC and NPC efficiencies using FW and DPWMMAX strategies with 1200 V IGBTs

For the second electric machine configuration, the DC bus voltage was fixed to 2 kV to have a modulation index of 1.28 for the maximal power. For the take-off, full-wave modulation will

be used and DPWMMAX for the remaining part of the mission (Fig. IV-16). Compared to the third harmonic injection, the FW has lower efficiency for the takeoff than if only the DPWMMAX was used (99.02 % vs 99.26 % for the NPC) however, with DPWMMAX, the efficiency is higher during the cruise (99.09 % vs 99.07 % for the NPC) which meant to be optimized.

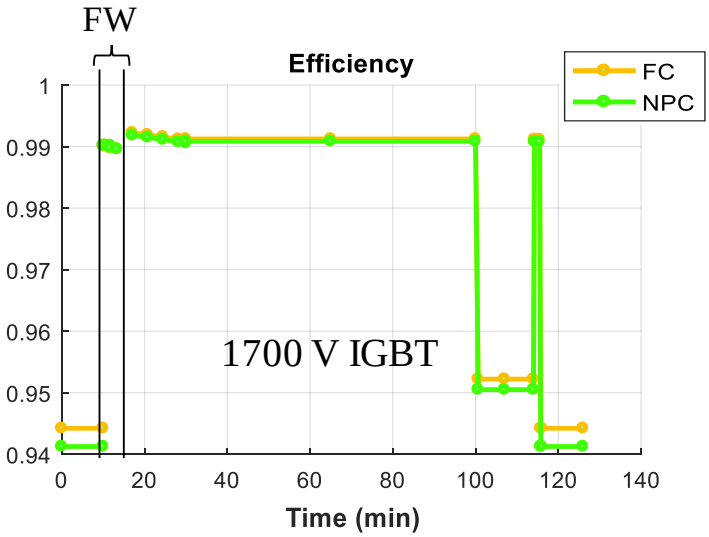


Fig. IV-16. 3-level FC and NPC efficiencies using FW and DPWMMAX strategies with 1700 V IGBTs for the 2nd e-motor

Using the combination of both strategies for the studied mission profile improves the overall inverter efficiency.

vi. Overview of control strategies

TABLE IV-7 to TABLE IV-10 sum up the different studied control strategies for the 3-level NPC topology sized for the appropriate strategy using 1700 V components and TABLE IV-9 and TABLE IV-10 sums up those for the FC topology. The worst efficiencies backgrounds are in red and the best ones are in green. The global efficiency presents the overall inverter efficiency during the flight mission.

TABLE IV-7. Efficiencies for different mission profile points for the NPC topology 1st e-motor

Flight phase	PWM+ THIPWM (Takeoff)	DPWM MAX	FW	PWM + FW (Takeoff / Climb)	DPWMMAX + FW (Takeoff)
Design strategy for $Pmax$	THIPWM	DPWM MAX	FW	FW	FW
Taxi out	94.43%	94.36%	85.98%	93.01%	**94.74%**
Takeoff	98.79%	**98.93%**	98.39%	98.39%	98.39%
Cruise	98.61%	98.76%	98.20%	98.64%	**98.81%**
Descent	95.39%	95.41%	88.91%	94.07%	**95.74%**
Global efficiency	97.62%	97.72%	95.26%	97.20%	**97.76%**

TABLE IV-8. Efficiencies for different mission profile points for the NPC topology 2nd e-motor

Flight phase	PWM+ THIPWM (Takeoff)	DPWM MAX	FW	PWM + FW (Takeoff / Climb)	DPWMMAX + FW (Takeoff)
Design strategy for $Pmax$	THIPWM	DPWM MAX	FW	FW	FW
Taxi out	93.56%	93.56%	89.24%	91.52%	**94.42%**
Takeoff	99.07%	**99.22%**	99.02%	99.02%	99.02%
Cruise	98.89%	99.02%	98.84%	98.90%	**99.12%**
Descent	94.51%	94.56%	92.35%	92.62%	**95.22%**
Global efficiency	97.59%	97.69%	96.62%	97.05%	**97.92%**

TABLE IV-9. Efficiencies for different mission profile points for the FC topology 1st e-motor

Flight phase	PWM+ THIPWM (Takeoff)	DPWM MAX	FW	PWM + FW (Takeoff / Climb)	DPWMMAX + FW (takeoff)
Design strategy for $Pmax$	THIPWM	DPWM MAX	FW	FW	FW
Taxi out	92.46%	94.78%	85.48%	94.81%	**95.13%**
Takeoff	98.78%	**98.98%**	98.39%	98.39%	98.39%
Cruise	98.57%	98.80%	98.20%	98.68%	**98.84%**
Descent	93.57%	95.66%	89.48%	95.72%	**95.95%**
Global efficiency	97.08%	97.84%	95.24%	97.69%	**97.86%**

TABLE IV-10. Efficiencies for different mission profile points for the FC topology 2nd e-motor

Flight phase	PWM+ THIPWM (Takeoff)	DPWM MAX	FW	PWM + FW (Takeoff / Climb)	DPWMMAX + FW (Takeoff)
Design strategy for $Pmax$	THIPWM	DPWM MAX	FW	FW	FW
Taxi out	90.68%	93.89%	89.83%	**94.12%**	**94.12%**
Takeoff	99.16%	**99.26%**	99.02%	99.02%	99.02%
Cruise	98.82%	99.07%	98.84%	98.97%	**99.09%**
Descent	91.86%	94.76%	92.52%	95.01%	**95.05%**
Global efficiency	96.81%	97.80%	96.74%	97.77%	**97.84%**

Since the ratio between the switching frequency and the machine frequency is not very high, the full-wave control does not have much interest in this case compared to the discontinuous PWM modulation. For the Taxi out, Cruise and Descent, the DPWMMAX efficiencies and THD are close to the sine PWM ones due to the low switching frequency as noticed in Fig. IV-17. However, the best compromise would be to size the inverter for the takeoff using the

FW and use the DPWMMAX for the other flight mission phases which improve the global inverter efficiency.

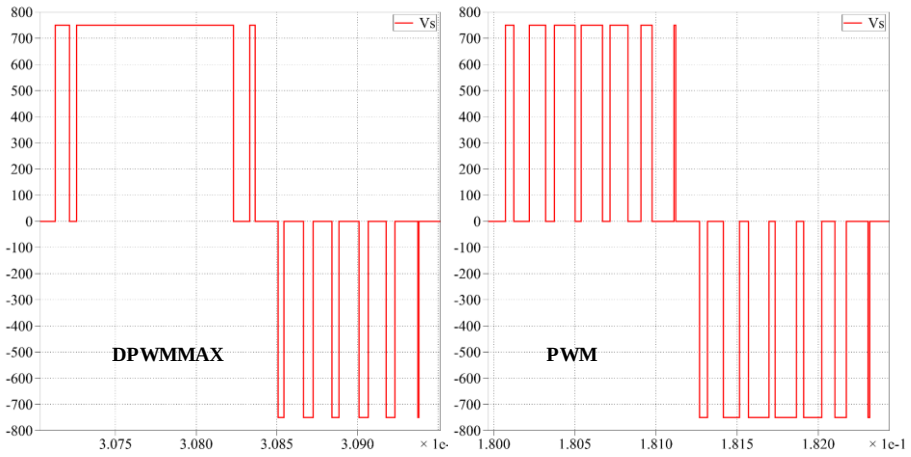


Fig. IV-17. Output voltage for 3-level FC during the cruise using DPWMMAX and PWM

The highest efficiency for these studied scenarios corresponds to the 2nd machine configuration with hybrid FW + DPWMMAX for both 3-level FC and NPC topologies.

TABLE IV-11 sums the target efficiencies during takeoff and cruise phases and achieved ones using the 5th strategy which is the DPWMMAX + FW which has the best results for the cruise phase.

TABLE IV-11. Target and achieved efficiencies during takeoff and cruise

Flight phase	**2025 Target**	**2035 Target**	**DPWMMAX + FW (takeoff)**			
			FC 1st e-motor	**NPC 1st e-motor**	**FC 2nd e-motor**	**NPC 2nd e-motor**
Takeoff	96.5%	99%	98.39%	98.39%	99.02%	99.02%
Cruise	98%	99.5%	98.84%	98.81%	99.09%	99.12%
Global Efficiency	-	-	97.86%	97.76%	97.84%	97.92%

The 2025 efficiency targets were achieved only by using a regular sine PWM and the 1st machine winding configuration. However, for 2035 efficiency objectives, even with the 2nd machine winding configuration and DPWMMAX, the efficiency is lower than the cruise power point objective and for the maximum power point, the objective was reached with the 3-level FC using a DPWMMAX control strategy. Nevertheless, the specific power of the FC topology is significantly lower than the NPC one due to the additional flying capacitors weight.

3. Conclusion

This chapter evaluates the efficiency of the chosen 3-level inverter topologies, which are the FC and NPC, for different modulation strategies during the flight mission so to find the best option to improve the efficiency during the cruise. This study was carried for two electric motor winding configurations.

The first studied strategy was to use the THIPWM during the takeoff and climb so to fully use the sine PWM during the cruise. This strategy enhances the overall inverter efficiency. The second one compares the THIPWM and DPWM both MIN and MAX. The DPWMMAX stands out from this comparison for both inverter topologies and both machine configurations. The third one is using FW for the entire mission profile. In this case, the efficiency is enhanced however, since the FW is a low modulation strategy, the THD is high for low power and frequency phases due to the low harmonic components. To avoid this problem, the 4^{th} and 5^{th} strategies were studied. These strategies use FW in combination with sine PWM for the 4^{th} one and DPWMMAX for the 5^{th} one. This improves efficiency and THD during the low power phases.

For all the modulation strategies, the use of the second machine parameters increases the efficiency of the inverter since for the same power, the used DC bus voltage is higher and therefore the current is lower, which reduces power losses in semiconductors.

So the most interesting strategy would be to size the inverter for the takeoff using the FW and use the DPWMMAX for the other flight mission phases. This strategy makes it possible to achieve the first targets set by HASTECS project in terms of efficiency. However, the cruise 2035 efficiency target (99.5 %) is still not reached (99.12 %).

Another solution to improve the efficiency during the cruise could be to use two or more converters. In the case of two converters, both are operated during take-off. Then, only one is connected to the motor. This solution could be considered to reach the 2035 targets. However, the inverter weight could be increased which will reduce the specific power.

Conclusion & perspectives

The main objective of this manuscript has been to size a highly integrated power electronic inverter that will feed an electric motor connected to an aircraft propeller with a specific power of 15 kW/kg for 2025 target and 25 kW/kg for 2035 target including its cooling system. It takes part in the second work package of HASTECS Clean Sky 2 European project that aims to study the possibility of electric propulsion hybridization in an aircraft which was presented in detail in Chapter I. In this Ph.D. study, power electronics topologies, smart control, and modulation strategies as well as semiconductor technologies were investigated.

As a result of a first simple sizing for a 2-level inverter, the main factor to increase the specific power was identified in Chapter I, decreasing the weight of the cooling system. Two options were conceivable. The first one was decreasing the cooling system mass by optimizing its components which was done by WP4 work. The second one was reducing power losses which is a part of our work package (WP2) tasks.

To size the power converter used to feed the electrical motor for the aircraft propulsion, a pre-design tool was developed. This tool uses *Matlab* object-oriented programming and is based on analytic analysis of the inverter power losses so to evaluate the efficiency and components temperatures to respond to our specification detailed in chapter II. The used power losses and thermal models were also presented in the second chapter. These models need several components such as capacitors and semiconductors parameters that are issued from the available database or generated based on it so to satisfy the current and voltage requirements. These components were validated using several study case scenarios and would help to define the DC bus voltage which is the first task of this work.

The available semiconductors voltage ranges limit the DC bus voltage that could be chosen if the 2-level topology was to be used without allowing direct series association. The high switching frequency represents also a constraint to the large voltage caliber components that were not meant to operate at these frequency levels due to the high switching losses. With all this said, using smaller voltage rating components but with high DC bus voltage to reduce the needed current rating would be more interesting. This could be done by using multilevel topologies.

In Chapter III, the inverter topologies, modulation strategies, and components technologies were presented. As noticed in chapter II, the inverter power losses reduction could be achieved by using small rating components. This was done by using multilevel architectures to avoid the direct series association. The used topologies were 2, 3 and 5 levels ones. They were compared using DC bus voltage sweeps to find the optimal DC bus voltage range for each group of topologies. If the DC bus voltage is between 700 V and 1 kV, the 2-level topology could be used, however, in this case, to withstand the machine current, several components should be associated in parallel which will increase the inverter weight and volume. If the DC bus voltage is between 1 and 2.4 kV, the 3-level topologies have the best efficiencies for this voltage this

range. However, if the DC bus voltage is between 2.4 and 3.5 kV, the 5-level ones must be recommended. This voltage range also depends on the used switching frequency. This parameter is very important especially for the high voltage components that were used and have a great impact on the power losses and therefore the semiconductors maximal junction temperature. The 3-level topologies and the 5-level ANPC seemed to be the most adapted ones to our specification. This study showed also that, so to use some topologies such as 2-level or 3-level ones, they should be used with a low switching frequency so to have an acceptable junction temperature.

This leads to the second covered point of chapter III which was the study modulation strategies. The multilevel modulation techniques could be classified according to switching frequency. High switching frequency modulations have higher switching losses but less impact on the machine current since the high-frequency filtering is better than low-frequency one. Therefore, with low switching frequency methods, efficiency is higher. In this work, four modulation strategies, which are sine PWM, Third Harmonic Injection PWM, Discontinuous PWM MIN and MAX, and Full Wave adapted to 3-level inverter topologies, were studied and compared in terms of efficiency so to find the most performant one. The sine PWM had the lowest efficiency among all the topologies but still close to the others' performances. The DPWMMAX was the one with the highest efficiency for both studied 3-level topologies.

The third tackled point in chapter III was semiconductors technologies. The component choice has a great impact on the inverter performances since the power losses depend on the semiconductor conduction and switching parameters. The market evolution of silicon components seemed to be saturated in recent years. However, with the new Mitsubishi 7^{th} generation IGBT module, this is not the case anymore. These components have fewer losses and come in a compact light-weighted packaging. These components were compared to the previous IGBT generation and also to SiC modules with the same current and voltage calibers and seem to be the best option for our specifications.

Using these components, the DPWMMAX modulation and an optimized cooling system with a 3-level NPC topology, the 15 kW/kg specific power target was exceeded (23.29 kW/kg) but it stills far from the 2035 one which is 25 kW/kg. To reach the second target, a specific power module was designed so to integrate half a phase in a single module. This solution reduced the used bus bar and make it possible to achieve a specific power of 57.59 kW/kg for the 3-phase inverter taking into account only the bus bar, DC bus capacitor, semiconductors, and its cooling system. To have a more accurate estimation, parameters such as drivers, filters and components attaching elements should be included.

In chapter IV, several modulation strategies and sizing points have been studied to find out the best scenario for the 3-level FC and NPC inverters modulation strategies taking into account the flight mission. This study was carried for two electric motor winding configurations.

The first studied strategy was to use the THIPWM during the takeoff and climb so to fully use the sine PWM during the cruise. This strategy enhances the overall inverter efficiency. The second one compares the THIPWM and DPWM both MIN and MAX. The DPWMMAX stands out from this comparison for both inverter topologies and both machine configurations. The third one is using FW for the entire mission profile. In this case, the efficiency is enhanced however, since the FW is a low modulation strategy, the THD is high for low power low-speed phases due to the low harmonic components. To avoid this problem, the 4th and 5th strategies were studied. These strategies use FW in combination with sine PWM for the 4th one and DPWMMAX for the 5th one. This improves efficiency and THD during the low power phases.

So the most interesting strategy would be to size the inverter for the takeoff using the FW and use the DPWMMAX for the other flight mission phases. This strategy makes it possible to achieve the targets set by HASTECS project in terms of efficiency for the takeoff. However, for the cruise, the reached efficiency is 99.12 % with the second machine configuration and the 2035 target was 99.5 %. For all the modulation strategies, the use of the second machine parameters increases the efficiency of the inverter since for the same power, the used DC bus voltage is higher and therefore the current is lower, which reduces power losses in semiconductors.

One way to improve inverter efficiency during the cruise could be to use two or more converters. In the case of two converters, both are operated during takeoff. Then, only one is connected to the motor. This solution could be considered to reach the 2035 targets. However, the inverter weight could be increased which would reduce the specific power. Fig. V-1 represents some ideas that were meant to be explored:

- Possibility to increase the number of converter leg if using a multi-motor (Fig. V-1.D) or “multi stator” (double or more) machine (Fig. V-1.E-F), by dividing the required current to power the motor by the number of phases;
- Possibility to interleave the converter legs by inductors (Fig. V-1.B-C). To reduce the size of the inductors, coupling devices can be used or the stator itself can be used as a coupling device (multi-phase or multi-stator Fig. V-1.E-F-G). In each case, the losses inside the converter will change and due to the change in output waveforms, motor performance and partial discharge effect would be affected;
- Impact of the power splitting on the architecture redundancy and fault tolerance issues.

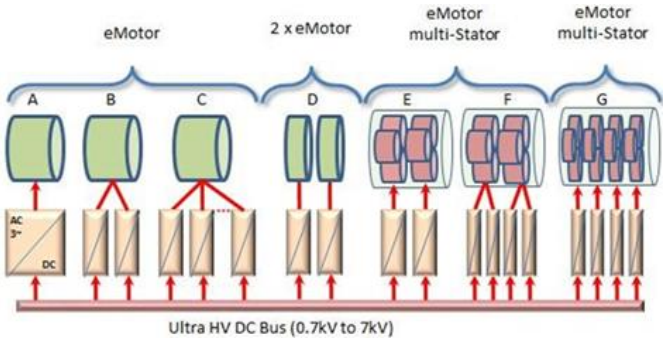


Fig. V-1. Power rating and converter architecture

Appendix

The considered output current (1) absorbed by the electrical motor is supposed to be sinusoidal with a phase shift $\theta$and ω is the electric motor pulsation.

$$I_{out}(x) = \sqrt{2} * I_{rms} * \sin(x - \theta) \text{ with } x = \omega t \quad (1)$$

The command function depends on the used modulation strategy and is as follows:

$$f(x) = \begin{cases} k * \sin(x) & , \quad Sine\ PWM \\ k * \sin(x) + \frac{1}{4} * \sin(3x), & \quad THIPWM \end{cases} \quad (2)$$

With k the modulation index.

1. 3-level FC topology

The considered topology is shown in Fig. VI-1. The switched and conducted average and RMS current expressions are given for the sine PWM and THIPWM modulation strategies. These expressions are deduced from a *Plecs* simulation used to define the switching intervals and the connection function.

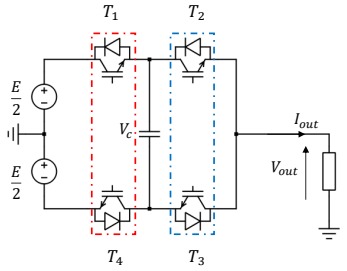


Fig. VI-1. 3-level FC inverter leg

i. PWM

For the sine PWM, the losses are balanced for this topologies so the current are calculated only for one IGBT and one Diode.

TABLE. VI-1. Conduction Mode average and RMS current

Avg	$\bar{I}_{T_1} = \bar{I}_{T_2} = \bar{I}_{T_3} = \bar{I}_{T_4} = \frac{1}{2\pi}\left[\int_{\theta}^{\pi+\theta} I_{out}(x)\,(1 + f(x))dx\right]$ $\bar{I}_{D_1} = \bar{I}_{D_2} = \bar{I}_{D_3} = \bar{I}_{D_4}$ $= \frac{1}{2\pi}\left[\int_{0}^{\theta} I_{out}(x)\,(1 + f(x))dx + \int_{\pi+\theta}^{2\pi} I_{out}(x)(1 + f(x))dx\right]$
RMS	$I_{rms\,T_1} = I_{rms\,T_2} = I_{rms\,T_3} = I_{rms\,T_4} = \sqrt{\frac{1}{2\pi}\left[\int_{\theta}^{\pi+\theta} I_{out}^2(x)(1 + f(x))dx\right]}$ $I_{rms\,D_1} = I_{rms\,D_2} = I_{rms\,D_3} = I_{rms\,D_4} = \sqrt{\frac{1}{2\pi}\left[\int_{0}^{\theta} I_{out}^2(x)\,(1 + f(x))dx + \int_{\pi+\theta}^{2\pi} I_{out}^2(x)(1 + f(x))dx\right]}$

TABLE. VI-2. Switching Mode average current formulas

	Interval Δ^{SW}	Current
Avg	$\frac{1}{2}$	$\bar{I}_{T_1}{}^{SW} = \bar{I}_{T_2}{}^{SW} = \bar{I}_{T_3}{}^{SW} = \bar{I}_{T_4}{}^{SW} = \frac{1}{2\pi}\left[\int_{\theta}^{\pi+\theta} I_{out}(x)\,dx\right]$
	$\frac{1}{2}$	$\bar{I}_{D_1}{}^{SW} = \bar{I}_{D_2}{}^{SW} = \bar{I}_{D_3}{}^{SW} = \bar{I}_{D_4}{}^{SW} = \frac{1}{2\pi}\left[\int_{\theta}^{\pi+\theta} I_{out}(x)\,dx\right]$
RMS	$\frac{1}{2}$	$I_{rms\,T_1}{}^{SW} = I_{rms\,T_2}{}^{SW} = I_{rms\,T_3}{}^{SW} = I_{rms\,T_4}{}^{SW} = \sqrt{\frac{1}{2\pi}\left[\int_{\theta}^{\pi+\theta} I_{out}(x)\,dx\right]}$
	$\frac{1}{2}$	$I_{rms\,D_1}{}^{SW} = I_{rms\,D_2}{}^{SW} = I_{rms\,D_3}{}^{SW} = I_{rms\,D_4}{}^{SW} = \sqrt{\frac{1}{2\pi}\left[\int_{0}^{\theta} I_{out}(x)\,dx + \int_{\theta+\pi}^{2\pi} I_{out}(x)\,dx\right]}$

ii. THIPWM1/4

For the THIPWM, the losses are symmetric so the current are calculated for one upper and one lower IGBT and Diode.

TABLE. VI-3. Conduction Mode average and RMS current

Avg	$\bar{I}_{T_1} = \bar{I}_{T_2} = \frac{1}{2\pi}\left[\int_{\theta}^{\pi} I_{out}(x)\,dx + \int_{\pi}^{\pi+\theta} I_{out}(x)\,(1+f(x))dx\right]$ $\bar{I}_{T_3} = \bar{I}_{T_4} = \frac{1}{2\pi}\left[\int_{\theta}^{\pi} I_{out}(x) * f(x)dx\right]$ $\bar{I}_{D_1} = \bar{I}_{D_2} = \frac{1}{2\pi}\left[\int_{0}^{\theta} I_{out}(x)\,dx + \int_{\pi+\theta}^{2\pi} I_{out}(x)\,(1+f(x))dx\right]$ $\bar{I}_{D_3} = \bar{I}_{D_4} = \frac{1}{2\pi}\left[\int_{0}^{\theta} I_{out}(x) * f(x)dx\right]$
RMS	$I_{rms\,T_1} = I_{rms\,T_2} = \sqrt{\frac{1}{2\pi}\left[\int_{\theta}^{\pi} I_{out}^2(x)\,dx + \int_{\pi}^{\pi+\theta} I_{out}^2(x) * (1+f(x))\,dx\right]}$ $I_{rms\,T_3} = I_{rms\,T_4} = \sqrt{\frac{1}{2\pi}\left[\int_{\theta}^{\pi} I_{out}^2(x) * f(x)\,dx\right]}$ $I_{rms\,D_1} = I_{rms\,D_2} = \sqrt{\frac{1}{2\pi}\left[\int_{0}^{\theta} I_{out}^2(x)\,dx + \int_{\pi+\theta}^{2\pi} I_{out}^2(x) * (1+f(x))\,dx\right]}$ $I_{rms\,D_3} = I_{rms\,D_4} = \sqrt{\frac{1}{2\pi}\left[\int_{0}^{\theta} I_{out}^2(x) * f(x)\,dx\right]}$

TABLE. VI-4. Switching Mode average current formulas

	Interval Δ^{SW}	Current
Avg	$\frac{\theta}{2\pi}$	$\bar{I}_{T_1}{}^{SW} = \bar{I}_{T_2}{}^{SW} = \frac{1}{2\pi}\left[\int_{\pi}^{\pi+\theta} I_{out}(x)\,dx\right]$
	$\frac{\pi-\theta}{2\pi}$	$\bar{I}_{T_1}{}^{SW} = \bar{I}_{T_2}{}^{SW} = \frac{1}{2\pi}\left[\int_{\theta}^{\pi} I_{out}(x)\,dx\right]$
	$\frac{\pi-\theta}{2\pi}$	$\bar{I}_{D_1}{}^{SW} = \bar{I}_{D_2}{}^{SW} = \frac{1}{2\pi}\left[\int_{\pi+\theta}^{2\pi} I_{out}(x)\,dx\right]$
	$\frac{\pi-\theta}{2\pi}$	$\bar{I}_{D_3}{}^{SW} = \bar{I}_{D_4}{}^{SW} = \frac{1}{2\pi}\left[\int_{0}^{\theta} I_{out}(x)\,dx\right]$
RMS	$\frac{\theta}{2\pi}$	$I_{rms\,T_1}{}^{SW} = I_{rms\,T_2}{}^{SW} = \sqrt{\frac{1}{2\pi}\left[\int_{\pi}^{\pi+\theta} I_{out}^2(x)\,dx\right]}$
	$\frac{\pi-\theta}{2\pi}$	$I_{rms\,T_3}{}^{SW} = I_{rms\,T_4}{}^{SW} = \sqrt{\frac{1}{2\pi}\left[\int_{\theta}^{\pi} I_{out}^2(x)\,dx\right]}$
	$\frac{\theta}{2\pi}$	$I_{rms\,D_1}{}^{SW} = I_{rms\,D_2}{}^{SW} = \sqrt{\frac{1}{2\pi}\left[\int_{\pi}^{\pi+\theta} I_{out}^2(x)\,dx\right]}$
	$\frac{\pi-\theta}{2\pi}$	$I_{rms\,D_3}{}^{SW} = I_{rms\,D_4}{}^{SW} = \sqrt{\frac{1}{2\pi}\left[\int_{0}^{\theta} I_{out}^2(x)\,dx\right]}$

2. 3-level NPC topology

The considered 3-level NPC topology is shown in Fig. VI-2. The switched and conducted average and RMS current expressions are given for the sine PWM but are the same for the THIPWM since they don't have the same connection function f.

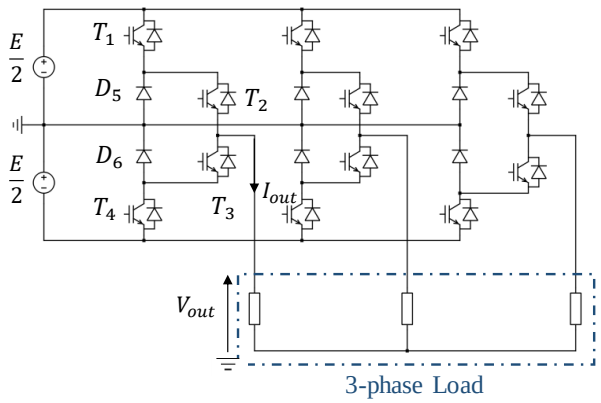


Fig. VI-2. 3-level NPC inverter

TABLE. VI-5. Conduction Mode average and RMS current

Avg	$\bar{I}_{T_1} = \bar{I}_{T_3} = \frac{1}{2\pi}\left[\int_{\theta}^{\pi} I_{out}(x)\, f(x) dx\right]$ $\bar{I}_{T_2} = \bar{I}_{T_4} = \frac{1}{2\pi}\left[\int_{\theta}^{\pi} I_{out}(x)\, dx + \int_{\pi}^{\pi+\theta} I_{out}(x)\,\big(1 + f(x)\big) dx\right]$ $\bar{I}_{D_1} = \bar{I}_{D_3} = \frac{1}{2\pi}\left[\int_{0}^{\theta} I_{out}(x)\, f(x) dx\right]$ $\bar{I}_{D_2} = \bar{I}_{D_4} = \frac{1}{2\pi}\left[\int_{0}^{\theta} I_{out}(x)\, f(x) dx\right]$ $\bar{I}_{D_5} = \bar{I}_{D_6} = \frac{1}{2\pi}\left[\int_{\theta}^{\pi} I_{out}(x)\,(1 - f(x)) dx + \int_{\pi}^{\pi+\theta} I_{out}(x)(1 + f(x)) dx\right]$
RMS	$I_{rms\,T_1} = I_{rms\,T_3} = \sqrt{\frac{1}{2\pi}\left[\int_{\theta}^{\pi} I_{out}^2(x)\, f(x)\, dx\right]}$ $I_{rms\,T_2} = I_{rms\,T_4} = \sqrt{\frac{1}{2\pi}\left[\int_{\theta}^{\pi} I_{out}^2(x)\, dx + \int_{\pi}^{\pi+\theta} I_{out}^2(x) * (1 + f(x))\, dx\right]}$ $I_{rms\,D_1} = I_{rms\,D_3} = \sqrt{\frac{1}{2\pi}\left[\int_{0}^{\theta} I_{out}^2(x) f(x)\, dx\right]}$ $I_{rms\,D_2} = I_{rms\,D_4} = \sqrt{\frac{1}{2\pi}\left[\int_{0}^{\theta} I_{out}^2(x) f(x)\, dx\right]}$ $I_{rms\,D_5} = I_{rms\,D_6} = \sqrt{\frac{1}{2\pi}\left[\int_{\theta}^{\pi} I_{out}^2(x)(1 - f(x))\, dx + \int_{\pi}^{\pi+\theta} I_{out}^2(x) * (1 + f(x))\, dx\right]}$

TABLE. VI-6. Switching Mode average current formulas

	Interval Δ^{SW}	Current
Avg	$\frac{\pi - \theta}{2\pi}$	$\bar{I}_{T_1}^{SW} = \bar{I}_{T_3}^{SW} = \frac{1}{2\pi}\left[\int_{\theta}^{\pi} I_{out}(x)\, dx\right]$
	$\frac{\theta}{2\pi}$	$\bar{I}_{T_2}^{SW} = \bar{I}_{T_4}^{SW} = \frac{1}{2\pi}\left[\int_{\pi}^{\pi+\theta} I_{out}(x)\, dx\right]$
	$\frac{\theta}{2\pi}$	$\bar{I}_{D_1}^{SW} = \bar{I}_{D_3}^{SW} = \frac{1}{2\pi}\left[\int_{0}^{\theta} I_{out}(x)\, dx\right]$
	$\frac{\theta}{2\pi}$	$\bar{I}_{D_2}^{SW} = \bar{I}_{D_4}^{SW} = \frac{1}{2\pi}\left[\int_{0}^{\theta} I_{out}(x)\, dx\right]$
	$\frac{\pi - \theta}{2\pi}$	$\bar{I}_{D_5}^{SW} = \bar{I}_{D_6}^{SW} = \frac{1}{2\pi}\left[\int_{\theta}^{\pi} I_{out}(x)\, dx\right]$

RMS	$\frac{\pi-\theta}{2\pi}$	$I_{rms\,T_1}^{SW} = I_{rms\,T_3}^{SW} = \sqrt{\frac{1}{2\pi}\left[\int_{\theta}^{\pi} I_{out}^2(x)\,dx\right]}$
	$\frac{\theta}{2\pi}$	$I_{rms\,T_2}^{SW} = I_{rms\,T_4}^{SW} = \sqrt{\frac{1}{2\pi}\left[\int_{\pi}^{\pi+\theta} I_{out}^2(x)\,dx\right]}$
	$\frac{\theta}{2\pi}$	$I_{rms\,D_1}^{SW} = I_{rms\,D_3}^{SW} = \sqrt{\frac{1}{2\pi}\left[\int_{0}^{\theta} I_{out}^2(x)\,dx\right]}$
	$\frac{\theta}{2\pi}$	$I_{rms\,D_2}^{SW} = I_{rms\,D_4}^{SW} = \sqrt{\frac{1}{2\pi}\left[\int_{0}^{\theta} I_{out}^2(x)\,dx\right]}$
	$\frac{\pi-\theta}{2\pi}$	$I_{rms\,D_5}^{SW} = I_{rms\,D_6}^{SW} = \sqrt{\frac{1}{2\pi}\left[\int_{\theta}^{\pi} I_{out}^2(x)\,dx\right]}$

3. 5-level ANPC PWM

The considered 5-level ANPC topology is shown in Fig. VI-3. The switched and conducted average and RMS current expressions are given only for the sine PWM.

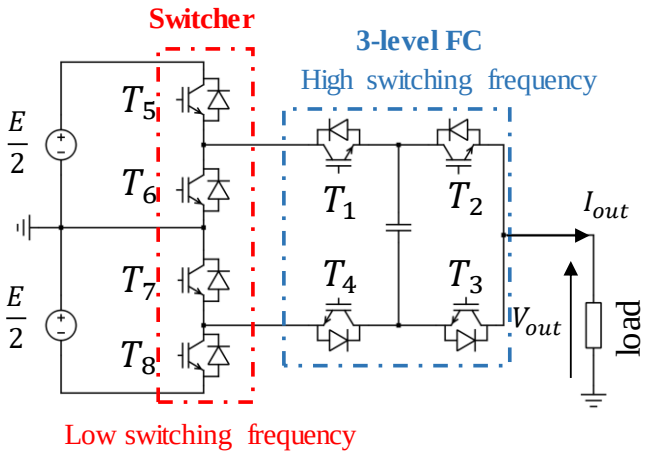


Fig. VI-3. 5-level ANPC topology

TABLE. VI-7. Conduction Mode average current formulas

FC	$\bar{I}_{T_1} = \bar{I}_{T_2} = \bar{I}_{T_3} = \bar{I}_{T_4}$ $= \frac{1}{2\pi}\left[\int_{\theta}^{\pi} I_{out}(x)\,f(x)dx + \int_{\pi}^{\pi+\theta} I_{out}(x)\,(1+f(x))dx\right]$ $\bar{I}_{D_1} = \bar{I}_{D_2} = \bar{I}_{D_3} = \bar{I}_{D_3}$ $= \frac{1}{2\pi}\left[\int_{0}^{\theta} I_{out}(x)\,f(x)dx + \int_{\pi+\theta}^{2\pi} I_{out}(x)(1+f(x))dx\right]$

Switcher	$\bar{I}_{T_5} = \bar{I}_{T_8} = \frac{1}{2\pi}\left[\int_{\theta}^{\pi} I_{out}(x)\,dx\right]$ $\bar{I}_{D_5} = \bar{I}_{D_8} = \frac{1}{2\pi}\left[\int_{0}^{\theta} I_{out}(x)\,dx\right]$ $\bar{I}_{T_6} = \bar{I}_{T_7} = \frac{1}{2\pi}\left[\int_{\pi+\theta}^{2\pi} I_{out}(x)\,dx\right]$ $\bar{I}_{D_6} = \bar{I}_{D_7} = \frac{1}{2\pi}\left[\int_{\pi}^{\pi+\theta} I_{out}(x)\,dx\right]$

TABLE. VI-8. Conduction Mode RMS current formulas

FC	$I_{rms\,T_1} = I_{rms\,T_2} = I_{rms\,T_3} = I_{rms\,T_4} = \sqrt{\frac{1}{2\pi}\left[\int_{\theta}^{\pi} I_{out}^2(x)\,f(x)dx + \int_{\pi}^{\pi+\theta} I_{out}^2(x)(1+f(x))dx\right]}$ $I_{rms\,D_1} = I_{rms\,D_2} = I_{rms\,D_3} = I_{rms\,D_4} = \sqrt{\frac{1}{2\pi}\left[\int_{0}^{\theta} I_{out}^2(x)\,f(x)dx + \int_{\pi+\theta}^{2\pi} I_{out}^2(x)(1+f(x))dx\right]}$
Switcher	$I_{rms\,T_5} = I_{rms\,T_8} = \sqrt{\frac{1}{2\pi}\left[\int_{\theta}^{\pi} I_{out}^2(x)\,dx\right]}$ $I_{rms\,D_5} = I_{rms\,D_8} = \sqrt{\frac{1}{2\pi}\left[\int_{0}^{\theta} I_{out}^2(x)\,dx\right]}$ $I_{rms\,T_6} = I_{rms\,T_7} = \sqrt{\frac{1}{2\pi}\left[\int_{\pi+\theta}^{2\pi} I_{out}^2(x)\,dx\right]}$ $I_{rms\,D_6} = I_{rms\,D_7} = \sqrt{\frac{1}{2\pi}\left[\int_{\pi}^{\pi+\theta} I_{out}^2(x)\,dx\right]}$

TABLE. VI-9. Switching Mode average current formulas

	Interval Δ^{SW}	Average Currents
FC		
T_1, T_4	$\frac{1}{2}$	$\bar{I}_{T_1}^{\ SW} = \bar{I}_{T_2}^{\ SW} = \bar{I}_{T_3}^{\ SW} = \bar{I}_{T_4}^{\ SW} = \frac{1}{2\pi}\left[\int_{\theta}^{\pi} I_{out}(x)\,dx + \int_{\pi}^{\theta+\pi} I_{out}(x)\,dx\right]$
D_1, D_4	$\frac{1}{2}$	$\bar{I}_{D_1}^{\ SW} = \bar{I}_{D_2}^{\ SW} = \bar{I}_{D_3}^{\ SW} = \bar{I}_{D_4}^{\ SW} = \frac{1}{2\pi}\left[\int_{0}^{\theta} I_{out}(x)\,dx + \int_{\theta+\pi}^{2\pi} I_{out}(x)\,dx\right]$

Switcher		
T_5, T_8	$\frac{\pi-\theta}{2\pi}$	$\bar{I}_{T_5}{}^{SW} = \bar{I}_8{}^{SW} = \frac{1}{2\pi}\left[\int_{\theta+\pi}^{2\pi} I_{out}(x)\,dx\right]$
D_5, D_8	$\frac{\theta}{2\pi}$	$\bar{I}_{D_5}{}^{SW} = \bar{I}_{D_8}{}^{SW} = \frac{1}{2\pi}\left[\int_{0}^{\theta} I_{out}(x)\,dx\right]$
T_6, T_7	$\frac{\pi-\theta}{2\pi}$	$\bar{I}_{T_6}{}^{SW} = \bar{I}_{T_7}{}^{SW} = \frac{1}{2\pi}\left[\int_{\theta}^{\pi} I_{out}(x)\,dx\right]$
D_6, D_7	$\frac{\pi-\theta}{2\pi}$	$\bar{I}_{D_6}{}^{SW} = \bar{I}_{D_7}{}^{SW} = \frac{1}{2\pi}\left[\int_{\theta+\pi}^{2\pi} I_{out}(x)\,dx\right]$

TABLE. VI-10. Switching Mode RMS current formulas

	Interval Δ^{SW}	RMS Currents:
FC		$I_{rms\,T_1}{}^{SW} = I_{rms\,T_2}{}^{SW} = I_{rms\,T_3}{}^{SW} = I_{rms\,T_4}{}^{SW}$
T_1, T_4	$\frac{1}{2}$	$= \sqrt{\frac{1}{2\pi}\left[\int_{\theta}^{\pi} I_{out}(x)\,dx + \int_{\pi}^{\theta+\pi} I_{out}(x)\,dx\right]}$
		$I_{rms\,D_1}{}^{SW} = I_{rms\,D_2}{}^{SW} = I_{rms\,D_3}{}^{SW} = I_{rms\,D_4}{}^{SW}$
D_1, D_4	$\frac{1}{2}$	$= \sqrt{\int_{0}^{\theta} I_{out}(x)\,dx + I_{out}(x)dx}$
Switcher		
T_5, T_8	$\frac{\pi-\theta}{2\pi}$	$I_{rms\,T_5}{}^{SW} = I_{rms\,T_8}{}^{SW} = \sqrt{\frac{1}{2\pi}\left[\int_{\theta+\pi}^{2\pi} I_{out}^2(x)\,dx\right]}$
D_5, D_8	$\frac{\theta}{2\pi}$	$I_{rms\,D_5}{}^{SW} = I_{rms\,D_8}{}^{SW} = \sqrt{\frac{1}{2\pi}\left[\int_{0}^{\theta} I_{out}^2(x)\,dx\right]}$
T_6, T_7	$\frac{\pi-\theta}{2\pi}$	$I_{rms\,T_6}{}^{SW} = I_{rms\,T_7}{}^{SW} = \sqrt{\frac{1}{2\pi}\left[\int_{\theta}^{\pi} I_{out}^2(x)\,dx\right]}$
D_6, D_7	$\frac{\pi-\theta}{2\pi}$	$I_{rms\,D_6}{}^{SW} = I_{rms\,D_7}{}^{SW} = \sqrt{\frac{1}{2\pi}\left[\int_{\pi+\theta}^{2\pi} I_{out}^2(x)\,dx\right]}$
T_5, T_8	$\frac{\pi-\theta}{2\pi}$	$\bar{I}_{T_5}{}^{SW} = \bar{I}_{T_8}{}^{SW} = \frac{1}{2\pi}\left[\int_{\theta+\pi}^{2\pi} I_{out}^2(x)\,dx\right]$

Résumé en français

Introduction

L'empreinte environnementale et écologique des systèmes de transport, en particulier des avions, n'a cessé de croître ces dernières années. Les considérations environnementales actuelles poussent donc à réduire leur impact écologique. Des projets tels que le projet Clean Sky 2 apportent une réponse à ce problème, en proposant une réduction des émissions de CO_2 et des nuisances sonores. La mise au point d'un avion hybride à propulsion électrique réduirait ces émissions en réduisant la taille et la masse des systèmes et en utilisant des systèmes électriques plus efficaces. Cela permettrait de réduire la consommation de carburant et donc les émissions polluantes.

Ces travaux s'inscrivent dans le cadre du projet européen HASTECS Clean Sky 2, qui étudie la possibilité d'hybridation de la propulsion d'un avion régional et vise à développer un outil de simulation pour pré-dimensionner les onduleurs destinés à piloter les moteurs électriques connecté aux hélices pour propulser l'avion. Pour ce faire, les topologies de l'électronique de puissance, les stratégies de contrôle et de modulation ainsi que les technologies des semi-conducteurs ont été prises en compte. Le projet HASTECS s'est fixé le défi d'augmenter la densité de puissance de l'électronique de puissance et de son système de refroidissement pour atteindre 15 kW/kg en 2025 puis 25 kW/kg en 2035. Cela permettrait de réduire la masse de l'onduleur ainsi que celle de la chaine de propulsion, ce qui se traduirait par une réduction de la consommation de carburant. Deux objectifs en termes de rendement pour l'électronique de puissance ont été fixés également par les avant-projets. Pour l'objectif de 2025, le rendement devrait être supérieur à 98 % pour la phase de croisière et supérieur à 96.5 % pour le point de puissance maximal. En revanche, pour l'objectif de 2035, le rendement devra être supérieur à 99.5 % pour la phase de croisière et supérieur à 99 % pour le point de puissance maximal.

Pour augmenter la densité de puissance, la masse de l'ensemble du système de conversion de puissance doit être diminué et en particulier la masse du système de refroidissement qui sera validé par le WP4. La réduction des pertes de l'onduleur peut être obtenue en utilisant des composants de faible calibre en tension, en jouant sur les stratégies de modulation ou en utilisant des semi-conducteurs plus performants. La première option pourrait être faite en utilisant des architectures multi-niveaux afin d'éviter l'association série directe. Contrairement à l'association série directe, l'association parallèle est plus facile à gérer en termes de commande de interrupteurs, ce qui a été autorisé dans nos études. Plusieurs topologies d'onduleurs (topologies à 2, 3 et 5 niveaux) et stratégies de modulation (PWM, injection de troisième harmonique, PWM discontinu et pleine onde) ont été comparées en utilisant plusieurs générations de semi-conducteurs pour choisir la solution la plus performante en termes de rendement et de densité de puissance. Pour le profil de mission de vol considéré, l'onduleur peut être dimensionné pour le point de puissance maximum (décollage) ou pour la phase de vol la plus longue (croisière). Une étude comparative des stratégies de contrôle de modulation a été réalisée pour mettre en évidence la structure et la modulation présentant les meilleures performances afin de minimiser

les pertes pour les points de dimensionnement choisis en utilisant les topologies les plus intéressantes pour le profil de mission étudié avec deux configurations de bobinages du moteur (2 et 3 conducteurs par encoche).

Le premier chapitre présente le principal problème lié à l'aviation actuelle et les opportunités offertes par les avions à propulsion hybride électrique. Le principe et la nécessité des avions à propulsion hybride-électrique seront démontrés en raison de l'évolution de l'industrie aéronautique commerciale et des besoins environnementaux, en plus des objectifs du projet européen Clean Sky 2 HASTECS. La problématique et les objectifs de ce travail seront présentés dans ce chapitre ainsi que le modèle de charge utilisé.

Dans le chapitre II, l'organisation du logiciel et les modèles thermiques et de pertes dans les convertisseurs de puissance utilisés seront présentés. La base de données des semi-conducteurs utilisés sera également abordée. Ce travail vise à développer un outil de simulation permettant de pré-dimensionner les convertisseurs. L'outil calcule différents résultats pour différentes architectures de conversion. Ses entrées sont les contraintes de conception, les topologies prévues des convertisseurs, et le choix de la famille de semi-conducteurs ou du fabricant à partir de la base de données des composants disponibles. Les résultats tels que le rendement, le nombre de semi-conducteurs, la température maximale de jonction, les pertes, les fréquences de découpages, les masses des semi-conducteurs, l'échangeur de chaleur, les éléments passifs internes au convertisseur, ainsi que la densité de puissance sont présentés sous forme de figures pour différents paramètres des différents comportements d'architecture.

Les topologies d'onduleurs et les stratégies de modulation étudiées seront présentées au chapitre III. Les performances seront ensuite comparées en utilisant plusieurs semi-conducteurs pour choisir la solution la plus performante en termes de rendement et de densité de puissance.

Dans le chapitre IV, les topologies d'onduleur choisies seront évaluées pour deux configurations de bobinages du moteur électrique pour l'ensemble de la mission de vol. Une étude comparative des stratégies de modulation sera réalisée pour mettre en évidence la structure et la modulation présentant les meilleures performances pour minimiser les pertes.

Chapitre I : Etat de l'art et contexte

Un ciel plus propre est l'objectif des développements récents et des recherches menées par tous les constructeurs aéronautiques. Cependant, les avions commerciaux consomment aujourd'hui plus de 270 millions de tonnes de kérosène par an et produisent donc de plus en plus d'émissions de CO_2.

La propulsion électrique a le potentiel de révolutionner le vol : des voyages plus propres et plus silencieux, les avantages pourraient être énormes. De plus, les estimations prévoient un doublement du trafic aérien tous les 15 à 20 ans. L'organisation internationale ATAG (Air Transport Action Group) s'est fixé des objectifs pour un ciel plus propre. Elle souhaite réduire la consommation de carburant de 1.5 % par an en moyenne entre 2009 et 2020, et plafonner les émissions de CO_2 par une croissance neutre en carbone à partir de 2020, ainsi que réduire de moitié les émissions nettes de CO_2 des activités aériennes d'ici 2050.

Ces objectifs ne peuvent être atteints avec les technologies actuelles. C'est pourquoi plusieurs projets de recherche et développement sur les technologies de propulsion électrique et hybride-électrique sont menés. Outre les avantages évidents de la réduction des émissions de CO_2 et des niveaux sonores, l'électrification permet également de réévaluer complètement la conception d'un aéronef. Différentes gammes de véhicules profiteront ainsi de l'électrification. À plus long terme, Airbus estime que la propulsion hybride-électrique sera probablement installée sur les avions civils de plus grande taille avant de devenir entièrement électrique, car les rapports puissance/masse de la technologie des batteries sont encore loin d'être suffisants.

Récemment, l'idée d'utiliser l'architecture hybride dans la propulsion aéronautique s'est développée. Cette idée est similaire à celle que l'on retrouve dans les véhicules électriques hybrides en automobile (VEH). Trois architectures hybrides différentes existent : hybridation série, parallèle et série/parallèle. Chaque type a ses avantages et ses critères qui diffèrent les uns des autres. Cependant, les trois types partagent l'idée d'utiliser un système de stockage qui sépare le point de fonctionnement du moteur thermique (turbine à gaz, générateur électrique ou groupe auxiliaire de puissance (APU)) de la propulsion, optimisant ainsi le rendement du moteur thermique. Seule l'hybridation série sera prise en compte dans le cadre de cette étude.

1. Présentation du projet HASTECS

Le projet HASTECS étudie la possibilité d'hybridation du système de propulsion d'un avion régional (Figure 1). Outre l'architecture globale, les différents lots de travail (work package WP) visent à augmenter la densité de puissance des différents composants de la chaîne électrique haute puissance. Cette étude conduira à une optimisation de l'ensemble de la chaîne qui proposera des structures intéressantes intégrant toutes les contraintes aéronautiques telles que les décharges partielles pour les équipements électriques placés en zone non pressurisée.

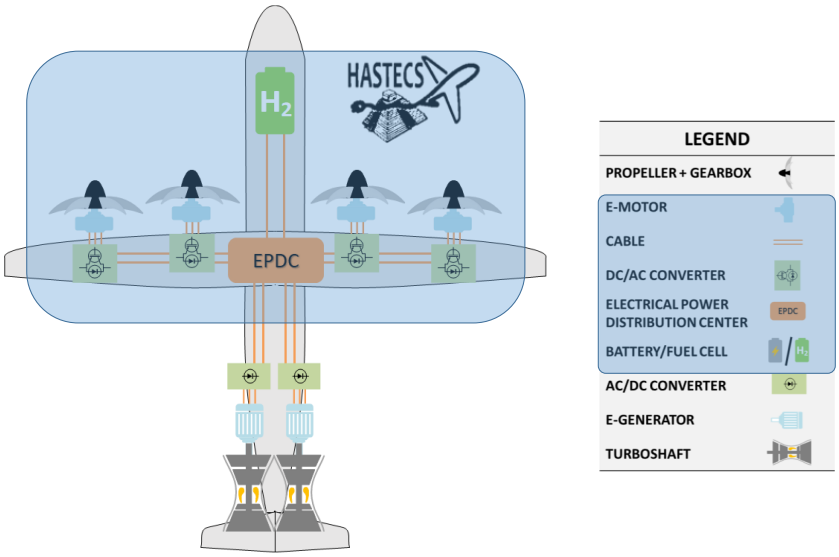


Figure 1. Architecture de base du projet HASTECS

Cette thèse se concentre uniquement sur l'onduleur utilisé pour alimenter le moteur électrique qui entraîne l'hélice (Figure 2). Pour cela, les topologies de l'électronique de puissance, les stratégies de modulation, ainsi que les technologies des semi-conducteurs seront prises en compte. Ceci a pour but de concevoir un onduleur hautement intégré d'une densité de puissance de 15 kW/kg pour la cible de 2025 et de 25 kW/kg pour la cible de 2035, incluant son système de refroidissement. Deux objectifs en termes de rendement pour l'électronique de puissance ont été fixés par le projet HASTECS. Pour l'objectif 2025, le rendement devrait être supérieur à 98 % pour la croisière et supérieur à 96.5 % pour le point de puissance maximal qui correspond au décollage. En revanche, pour l'objectif 2035, le rendement devrait être supérieur à 99.5 % pour la croisière et supérieur à 99 % pour le point de puissance maximal.

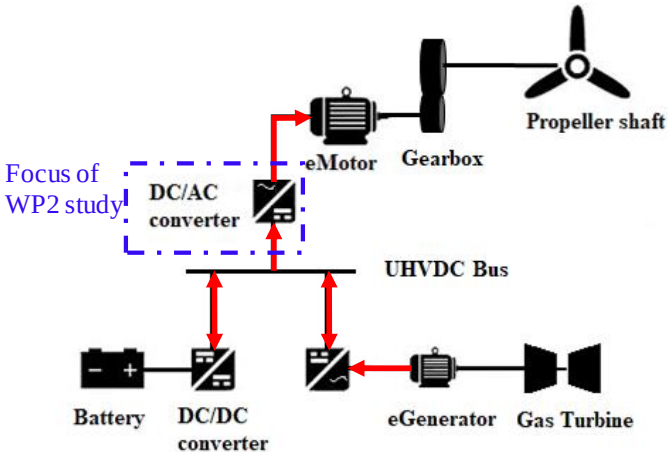


Figure 2. Configuration du système de propulsion hybride électrique

2. Cas de référence

Un onduleur régulier à 2 niveaux avec une PWM sinusoïdal a été dimensionné pour le point de puissance maximal afin de se faire une idée de ce qui pourrait être réalisé en termes de densité de puissance avec une solution basique.

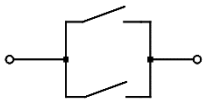
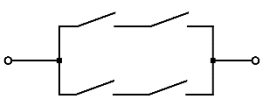
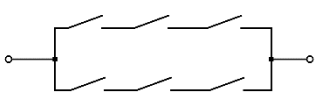
Pour ce cas d'étude, la tension du bus DC est choisie pour fournir la tension maximale nécessaire de la machine électrique ($V_{out_{max}}$) comme dans le Tableau 1. L'onduleur est dimensionné pour le point de puissance maximale avec un bus DC de 2 kV et une fréquence de découpage de 5.8 kHz qui représente environ 11 fois la fréquence nominale PMSM donné par le WP1. Pour estimer la densité de puissance de l'onduleur, y compris le système de refroidissement, on prend en compte un coefficient de 0.34 kW/kg qui traduit directement les pertes en masse du système de refroidissement. Cette valeur est utilisée comme valeur de base issue de l'état de l'art du partenaire Airbus. La masse des composants passifs tels que les condensateurs dans ce cas, sont également pris en compte.

Tableau 1. Paramètres de l'étude

Fréquence fondamentale (Hz)	532.3
$V_{out_{max}}$ (V)	857.3
$I_{out_{RMS}}$ (A)	1054
Indice de modulation	0.86
Facteur de puissance	0.78

Nous proposons de tester l'utilisation de trois calibres de composants différents afin de comparer les performances du convertisseur étudié. Pour ce premier cas d'étude, il est possible d'utiliser deux composants Infineon 3300 V / 800 A associés en parallèle pour s'adapter au niveau de courant imposé par la machine (utilisés à 61 % de leur calibre en tension). Le second utilise deux composants Infineon 1700 V / 600 A associés en parallèle et deux composants en série utilisés à 59% de leur calibre de tension même si l'association directe en série est difficile à réaliser. On suppose dans ce cas que l'on sait résoudre par la commande la problématique de la mise en série. Dans le troisième cas, deux composants Infineon 1200 V / 600 A sont associés en parallèle et trois composants en série utilisés à 56 % de leur calibre de tension. Le Tableau 2 résume les principales performances des onduleurs pour ces trois cas d'étude.

Tableau 2. Performances du convertisseur 2 niveaux

Calibre en tension	3300 V	1700 V	1200 V
η(%)	92.55	98	98.54
Température de jonction (°C)	244	307	98
Densité de puissance (kW/kg)	3.39	8.86	9.23
Associations séries et parallèles (par interrupteur)			
Nombre total de semi-conducteurs par phase	4	8	12

La Figure 3 montre la répartition de la masse de l'onduleur pour les différents cas étudiés. La masse du système de refroidissement, qui est une image directe des pertes en utilisant les composants de puissance à travers le coefficient d'échange initial, est la masse prédominante de l'onduleur. Le bus bar vient alors en deuxième position et sera dominant si la masse de l'échangeur thermique est réduite.

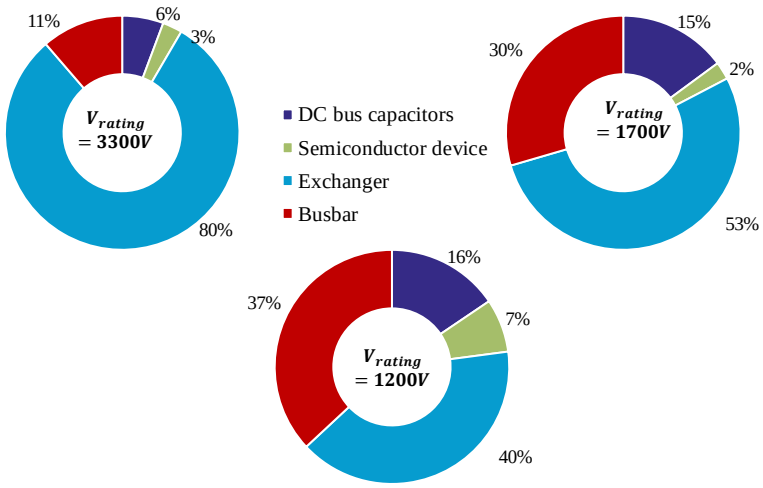


Figure 3. Répartition de la masse de l'onduleur pour les différents composants étudiés

Le convertisseur utilisant les composants possédants un petit calibre en tension a un meilleur rendement mais l'association en séries directe est difficile à réaliser, donc l'utilisation de topologies multi-niveaux pourrait être une solution. À partir de ces exemples, les principaux facteurs d'augmentation de la densité de puissance sont identifiés. Le premier consiste à diminuer la masse du système de refroidissement, en optimisant ses composants ou en réduisant les pertes de puissance. Le deuxième sera donc d'optimiser le bus bar.

Chapitre II : Outil de simulation

Ce chapitre vise à présenter l'outil de simulation développé qui permet de pré-dimensionner les convertisseurs et leurs composants pour un onduleur triphasé. Dans cet outil, les topologies des onduleurs et les stratégies de modulation sont fixées afin que l'utilisateur puisse choisir ses entrées parmi celles disponibles. Il calcule les pertes et la température de jonction pour chaque cas sélectionné selon le modèle qui sera détaillé dans ce chapitre en utilisant les paramètres du semi-conducteur sélectionné. Ce semi-conducteur est sélectionné dans la base de données disponible ou peut être généré de manière à s'adapter aux calibres de courant et tension nécessaires si l'utilisateur le décide, selon le principe de génération qui sera décrit et validé ci-dessous. Le dimensionnement du condensateur sera ensuite expliqué. Les modèles de perte seront ensuite validés à l'aide d'une simulation temporelle sur *Plecs* pour plusieurs topologies d'onduleurs. Ces modèles et les composants générés aideront ensuite à définir la plage de tension du bus DC au chapitre III, qui correspond à la première étape du travail du WP2.

1. Organisation de l’outil

L'outil permet à partir d'un cahier des charges donné de dimensionner le convertisseur en fonction de la topologie choisie. Il permet également de réaliser des études paramétriques en faisant varier la tension du bus DC, la puissance demandée ou l'indice de modulation pour déterminer le point de fonctionnement optimal. Il peut également prendre en compte un profil de mission qui permet de vérifier les performances du convertisseur pour une mission donnée.

Cet outil est réalisé en programmation orientée objet sur *Matlab.* Il est basé sur des calculs analytiques des pertes dans les composants semi-conducteurs pour les différentes architectures multiniveaux intégrées en considérant plusieurs stratégies de modulations. Chaque partie du convertisseur est représenté par un objet ou une classe.

Un objet de type convertisseur, par exemple, peut être caractérisé en topologies multiples (topologie à 2 niveaux, FC, NPC, SMC ou ANPC). Cet objet convertisseur est ensuite relié à un objet de spécification et à un ensemble d'éléments semi-conducteurs et condensateurs. Il est également composé de stratégies de modulation qui utilisent la topologie sélectionnée et les paramètres des dispositifs pour évaluer les pertes de puissance. Chaque bloc peut contenir un ou plusieurs scripts m-file *Matlab*. De plus, chaque script possède des données et des caractéristiques de classes et de leurs propriétés ; les scripts sont nommés comme la classe incluse à l'intérieur. Ces composants du convertisseur seront détaillés au chapitre III.

Pour chaque point de dimensionnement, l’outil sélectionne, à partir de la base de données disponible, les composants semi-conducteurs les plus appropriés qui conviennent le mieux à la tension et au courant désirés. Pour ce faire, un algorithme adapté a été développé. La première étape de cet algorithme consiste à sélectionner le fabricant choisi par l'utilisateur pour extraire les composants correspondants de la base de données. Il est ensuite déterminé si les composants disponibles permettent d'atteindre la tension nominale demandée. Si aucun des composants n'est adapté et que le composant le plus gros est donc trop petit, les composants sont connectés en série pour obtenir la tension souhaitée. Sinon, si plusieurs calibres de composants sont appropriés, le plus petit calibre est choisi parmi ceux qui sont appropriés pour avoir le composant le plus performant comme indiqué au chapitre I. Pour le calibre courant, si le courant requis est supérieur au plus grand calibre en courant, les composants sont associés en parallèle. Sinon, si plusieurs composants sont adaptés, le plus petit est sélectionné.

Ce logiciel permet une grande flexibilité et un grand degré de liberté pour le dimensionnement et l’étude des convertisseurs pour différents scénarios possibles.

2. Modélisations des pertes et de la thermique

Après avoir sélectionné les composants, l'étape suivante consiste à calculer les pertes pour évaluer le rendement de l'onduleur. Elles seront également utilisées pour calculer la température

maximale de jonction. Ces pertes et la température de jonction sont calculées à l'aide des modèles simplifiés présentés ci-dessous.

Pour modéliser les pertes dans le semi-conducteur, nous devons calculer les pertes par commutation et par conduction. Les deux pertes dépendent des paramètres du composant et des courants et tensions appliqués à ce dernier. Afin de simplifier le calcul des pertes dans les semi-conducteurs, un certain nombre d'hypothèses préliminaires ont été formulées qui sont présentées en détail dans le chapitre II. Dans ce cas, les semi-conducteurs utilisés sont uniquement des IGBT et des diodes en silicium.

Les pertes sont calculées à l'aide du produit courant-tension. Pour calculer les pertes par conduction, l'IGBT et la diode peuvent être modélisés par une chute de tension et une résistance interne connectée en série ne considérant qu'un courant positif (eq. (1)).

$$V_{ce} = V_{ce_0} + R_{dson} * I_c \tag{1}$$

$$P_{cond} = \frac{1}{T_{modulation}} \int_0^{T_{modulation}} V_{ce}(t) * I_c(t) dt \tag{2}$$

$$P_{cond} = V_{ce_0} * I_{c_{average}} + R_{dson} * {I_{c_{rms}}}^2 \tag{3}$$

Avec $I_{c_{average}}$ et $I_{c_{rms}}$ sont respectivement les valeurs moyenne et efficace du courant.

Pour calculer les pertes par commutation, on utilise les courbes des pertes d'énergie en fonction du courant pour une tension commutée, présentes dans les fiches techniques. Elles peuvent être approximés par une équation du second ordre avec trois paramètres Ax, Bx et Cx.

$$E_x = A_x + B_x * I + C_x * I^2 \tag{4}$$

$$P_{sw} = \frac{1}{T_{modulation}} \frac{1}{T_{sw}} \int_{t_1}^{t_2} \frac{V_{sw}}{V_{def}} E_{V_{def}}(I_{load}).\, dt \tag{5}$$

$$P_{sw} = f_{sw} * \frac{V_{sw}}{V_{def}} * \left(A \frac{\Delta sw}{T_{modulation}} + B * I_{sw_{average}} + C * {I_{sw_{rms}}}^2\right) \tag{6}$$

Avec f_{sw} la fréquence de découpage, $T_{modulation}$ la période de modulation, $I_{sw_{average}}$ et $I_{sw_{rms}}$ respectivement les courants moyen et efficaces découpés, V_{def} la tension d'utilisation du composants et $\Delta_{sw} = t_2 - t_1$ l'intervalle de commutation.

À partir des pertes dans la diode et l'IGBT, la température de jonction peut être définie. Dans notre architecture, un seul interrupteur de puissance contient un transistor avec une diode antiparallèle qui assure un chemin pour le courant inverse. Le modèle thermique comprendra donc deux résistances thermiques. Chaque résistance a un flux d'énergie thermique causé par les pertes de son composant respectif. Les températures des différents points de l'ensemble de commutation peuvent être déterminées à l'aide des équations suivantes :

$$T_{Transistor} = P_{losses_{transistor}} . R_{th_{jc}T} + T_{case} \quad (7)$$

$$T_{Diode} = P_{losses_{diode}} . R_{th_{jc}D} + T_{case} \quad (8)$$

$$T_{case} = (P_{losses_{transistor}} + P_{losses_{diode}}) . \left(R_{th_{ch}} + R_{th_{ha}}\right) + T_{ambient} \quad (9)$$

3. Base de données des semi-conducteurs

L'outil de simulation utilise une base de données qui résume les paramètres des semi-conducteurs obtenus à partir des fiches techniques des fabricants. Les composants sont classés en familles selon leur fabricant. Dans ce cas, seuls les composants en silicium sont étudiés.

WP2 se concentre sur les convertisseurs statiques et la définition de la tension du bus DC. Pour faciliter le travail des autres groupes de travail du projet, une première étape consiste à déterminer une plage de tension optimale pour le bus DC. À l'aide de l'outil de simulation et de la base de données disponible, le rendement ainsi que les calibres de tension utilisés lors d'une étude paramétrique qui dépendent de la tension du bus DC sont indiqués sur la Figure 4. Les sauts de rendement constatés sont dus au changement des calibres de tension des composants utilisés.

Par conséquent, il est difficile de trouver la tension optimale du bus DC en raison de la discrétisation des tensions nominales disponibles. Pour surmonter ce problème, nous avons créé une base de données continue de composants qui s'adapte aux calibres souhaités en ajustant et en extrapolant les composants existants de la base de données. Bien sûr, ces composants peuvent ne jamais exister, mais cela permet de voir l'effet du choix de l'architecture de conversion statique sur le rendement sur la plage de tension considérée tout en éliminant l'effet dû à la discrétisation.

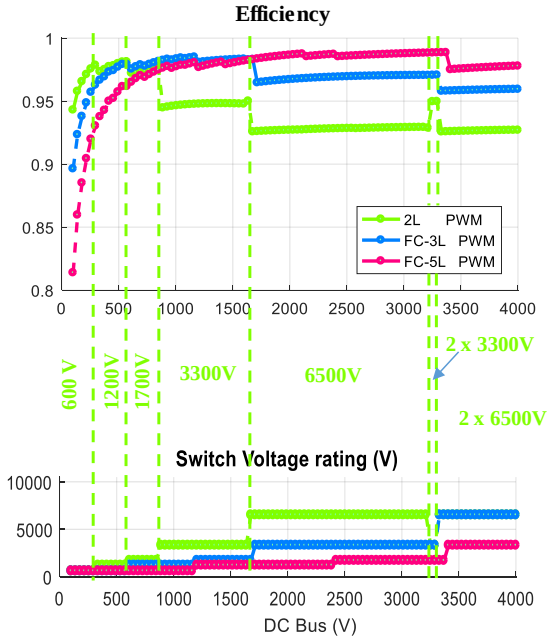


Figure 4. rendement de différentes topologies étudiées en utilisant les composants de la base de données

Pour créer un composant qui n'existe pas dans notre base de données, nous sélectionnons d'abord la famille ou le fabricant auquel le composant créé appartient. Pour cela, tous les paramètres des composants appartenant à cette famille sont extraits du fichier *Matlab*. Les composants de calibre en tension et en courant les plus proches sont sélectionnés pour être utilisés dans l'extrapolation. Une fois les composants sélectionnés, ils seront utilisés pour générer les paramètres du composant désiré. Les lois de variation de tous les paramètres sont ensuite identifiées en fonction du calibre de tension ou du produit calibres tension-courant comme indiqué dans le Tableau 3 et ensuite appliquées aux calibres souhaités.

Tableau 3. Paramètres générés

Paramètres générés	**Dépendance**	**Fonction d'approximation**
Pertes par commutation A_x, B_x and C_x	Calibre en tension	Polynôme du deuxième ordre $f(x) = ax^2 + bx + c$
Pertes par Conduction V_{ce0} R_{dson}, V_d, R_d.	Calibre en tension * Calibre en courant	Polynôme du premier ordre $f(x) = ax + b$
Résistances thermiques R_{th-jc_T}, R_{th-jc_D} and R_{th-ch}	Calibre en tension * Calibre en courant	Polynôme du deuxième ordre $f(x) = ax^b + c$
Surface	Calibre en tension * Calibre en courant	Polynôme du premier ordre $f(x) = ax + b$

4. Condensateurs

Les condensateurs sont des composants clés de l'électronique de puissance. Dans l'état de l'art des onduleurs, les condensateurs sont les plus grands composants et déterminent essentiellement le volume de l'onduleur. Par conséquent, une augmentation de la densité de stockage d'énergie des condensateurs aurait un impact énorme sur la taille et la densité de puissance de l'électronique de puissance.

Pour définir la valeur de la capacité, des informations sur les ondulations de courant, la fréquence et la tension sont nécessaires. Dans cette partie, le courant du condensateur est évalué pour deux types de condensateurs. Le premier est le condensateur de bus DC qui est nécessaire pour toutes les topologies et le second est le condensateur flottant qui est utilisé dans certaines topologies à 3 et 5 niveaux. Ces condensateurs sont sélectionnés à partir d'une base de données disponible selon un processus de sélection détaillé au chapitre II.

5. Nécessité des topologies multiniveaux

En utilisant les calibres en tension de composants disponibles, nous avons estimé les tensions de bus DC possibles pour utiliser pleinement le silicium disponible considéré ici comme 60% de leur calibre en tension. Cette valeur a été choisie de manière à permettre une utilisation optimale des composants 1200 V et 1700 V avec une surtension acceptable. Avec les topologies à 5 niveaux, on peut aller jusqu'à 7 kV mais avec les topologies à 2 niveaux, 2 kV est encore élevé pour les composants disponibles comme on peut le voir sur la Figure 5. Les points floutés ne sont pas réalisables en raison de la fréquence de découpage élevée qui implique une température de jonction élevée.

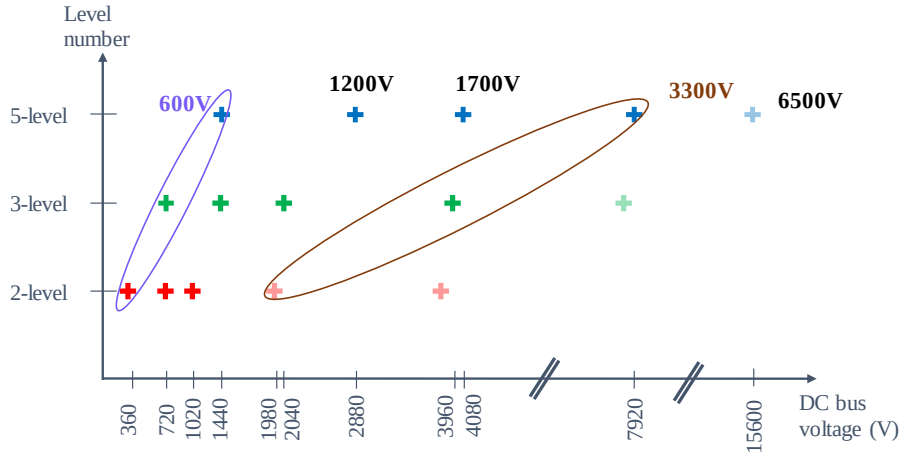


Figure 5. Tension optimale du bus DC en fonction du calibre en tension des composants et du nombre de niveaux de topologies

Les plages de tension des semi-conducteurs disponibles limitent la tension du bus continu qui pourrait être choisie si la topologie à deux niveaux devait être utilisée sans permettre une association directe en série. La fréquence de commutation élevée représente également une contrainte pour les composants de grand calibre de tension qui ne sont pas conçus pour fonctionner à ces niveaux de fréquence en raison des pertes par commutation élevées. Il serait donc plus intéressant d'utiliser des composants de calibre en tension plus petits mais avec une tension de bus DC élevée pour réduire le courant nominal nécessaire. Cela pourrait être fait en utilisant des topologies multi-niveaux. Les topologies sélectionnées seront présentées dans le chapitre III.

Chapitre III : Comparaison des solutions possibles dimensionnées pour le point de puissance maximal

Le principal facteur pour augmenter la densité de puissance identifié au chapitre I est la diminution de la masse du système de refroidissement en optimisant ses composants qui fait partie du travail du WP4 ou en réduisant les pertes. La réduction des pertes de l'onduleur peut être obtenue soit en utilisant de petits composants, soit en jouant sur des stratégies de modulation ou bien en utilisant des semi-conducteurs plus performants (Figure 6). La première option, qui consiste à utiliser de petits composants de tension nominale, pourrait être réalisée en utilisant des architectures multiniveaux pour éviter l'association série directe.

Dans ce chapitre, les topologies d'onduleurs et les stratégies de modulation étudiées sont présentées. Les performances sont ensuite comparées en utilisant plusieurs technologies de semi-conducteurs pour choisir la solution la plus performante en termes de rendement et de densité de puissance. Pour ce chapitre, le point de conception considéré est le point de puissance maximal qui correspond au décollage indiqué dans le profil de mission du chapitre I.

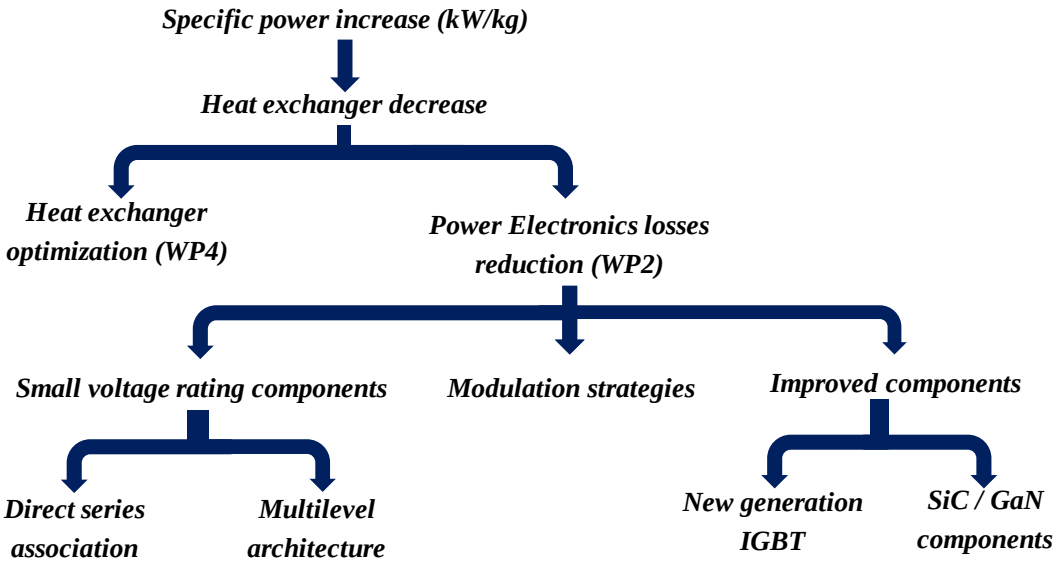


Figure 6. Ligne d'étude d'augmentation de densité de puissance

1. Comparaison des topologies multiniveaux

Dans cette thèse, les topologies de convertisseurs choisies sont des topologies multiniveaux de moyenne tension et de haute puissance. Les topologies étudiées sont le *Neutral Point Clamped* (NPC), le *Flying Capacitor* (FC), le *Stacked Multicellular Converter* (SMC) et *l'Active NPC topology* (ANPC).

Pour vérifier les conclusions antérieures concernant l'utilisation de composants de faible calibre en tension, trois types de topologies sont comparées. En utilisant le composant ABB disponibles dans notre base de données, les performances des topologies à 2, 3 et 5 niveaux ont été estimées

pour un balayage de bus DC de 700 V à 7 kV avec une fréquence de découpage apparente de 5.8 kHz et le point de puissance maximal avec une température de semelle fixée à 80 °C. Les composants générés sont utilisés à 50 % de leur tension nominale et à 100 % de leur courant nominal.

À l'issue de cette étude, les intervalles de tension du bus DC pour chaque topologie ont été définis. L'onduleur à 2 niveaux ne pourrait être utilisé qu'à faible puissance avec une tension de bus DC qui diminue avec la puissance utilisée pour la fréquence de découpage utilisée. Cet onduleur ne semble donc pas être la meilleure option pour notre application comme indiqué précédemment. Les onduleurs à 3 niveaux peuvent être utilisés jusqu'à 2 kV sur toute la gamme de puissance étudiée et ont un rendement optimal entre 1 kV et 2 kV. Cependant, pour les topologies à 5 niveaux, ils ont un rendement optimal entre 3 kV et 4 kV. On peut en conclure que pour ces topologies, à partir des graphiques de rendement, le rendement est optimal pour une tension de bus DC comprise entre 1 kV et 4 kV.

2. Comparaison des stratégies de modulation

Dans ce chapitre, quatre stratégies de modulation ont été étudiées. La modulation à largeur d'impulsion (PWM) sinusoïdale, la PWM avec injection de la troisième harmonique, la PWM MIN et MAX discontinu (DPWM) et la modulation pleine onde (FW) adaptée aux topologies d'onduleurs à 3 niveaux, ont été étudiées et comparées en termes de rendement.

Pour comparer les différentes stratégies de modulation, les résultats topologie pour la FC à 3 niveaux sont présentés ci-dessous. L'onduleur a été dimensionné pour un bus DC de 2 kV, ce qui donne un condensateur de bus DC de 2.5 mF selon la méthode de dimensionnement du chapitre II.

Comme l'indique le Tableau 4, les stratégies DPWM et la FW sont plus intéressantes. Cependant, pour la modulation pleine onde, le condensateur flottant est dimensionné pour la basse fréquence, ce qui donne un condensateur plus gros. Pour la THIPWM et la DPWM, la tension du bus DC a été dimensionnée en tenant compte de 15 % de tension de sortie supplémentaire par rapport au la PWM sinusoïdal et celle du FW a été dimensionnée en tenant compte de 30 % de tension de sortie supplémentaire pour le même point de puissance que la PWM.

Tableau 4. Performances d'un FC à 3 niveaux pour différentes stratégies de modulation

Topologie	**Flying Capacitors 3 niveaux**			
Stratégie de modulation	PWM	THIPWM1/4	DPWMMAX	FW 2
$\boldsymbol{\eta}$ **(%)**	96.54	97.80	97.85	98.09
Température (°C)	122	132	137	112
$\boldsymbol{C_{FC}}$ **(mF)**	1.35			5.7

3. Comparaison des 6ème et 7ème générations d'IGBT et les composants SiC

Le choix des composants a un impact important sur les performances de l'onduleur car les pertes dépendent des paramètres de conduction et de commutation du semi-conducteur. L'évolution du marché des composants en silicium semble avoir été saturée ces dernières années. Cependant, avec le nouveau module IGBT Mitsubishi de 7ème génération, ce n'est plus le cas. Ces composants ont moins de pertes et ont un emballage compact et léger.

Pour comparer la 6ème et la 7ème génération aux modules SiC et choisir la technologie la plus appropriée, l'onduleur est conçu en utilisant des modules 1200 V / 600 A, avec un bus DC de 1.2 kV pour utiliser pleinement le module (50 % du calibre en tension comme indiqué dans la fiche technique). Les résultats sont comparés pour un NPC à 3 niveaux utilisant une stratégie de modulation PWM sinusoïdale et associant deux composantes en parallèle pour satisfaire le niveau de courant imposé. La puissance a été adaptée pour n'utiliser que deux composants en parallèle puisque la tension du bus DC a été réduite.

Tableau. IGBT 1200V/600A de 6ème et 7ème génération vs module SiC 1200V/600A

	6ème génération IGBT	**7ème génération IGBT**	**SiC**
η(%)	98.53	98.84	98.51
Pertes par conduction (kW)	11.4	8.95	14.48
Pertes par commutation (kW)	3.52	2.81	0.679
Température jonction max (°C)	95.6	90.6	111.3

Pour notre spécification, le module 1200 V Full SiC n'est pas pertinent par rapport à notre solution. Même si les pertes par commutation sont faibles, les pertes par conduction restent supérieures aux pertes totales du module de 7ème génération. La fréquence de découpage utilisée est faible car il n'est pas nécessaire d'avoir une fréquence élevée afin de garantir des courants sinusoïdaux dans la machine. Nous ne profitons donc pas pleinement des avantages de la technologie SiC. De plus, la résistance thermique du module SiC est plus élevée, augmentant la température de jonction. En plus, la technologie SiC n'en est qu'à ses débuts et est donc moins avancée que la technologie Silicium et pourrait être une option intéressante à l'avenir.

4. Modèle onduleur en 3D

En utilisant ces composants de 7ème générations, la modulation DPWMMAX et un système de refroidissement optimisé avec une topologie NPC à 3 niveaux, l'objectif de densité de puissance de 15 kW/kg a été dépassé (23.29 kW/kg) mais on est encore loin de celui de 2035 qui est 25 kW/kg.

Pour réduire la masse du bus bar, la création d'un module intégré monophasé enlève le bus bar entre les modules de semi-conducteurs et tout ce qui reste est la connexion entre le module et les condensateurs du bus DC et entre le module et la phase du moteur. Un module de puissance a été conçu pour un NPC monophasé à 3 niveaux (Figure 7) en prenant en compte les contraintes schématiques, dimensionnelles et environnementales.

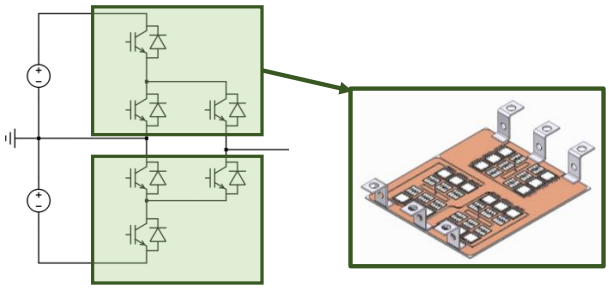


Figure 7. Conception d'un module de puissance pour un onduleur ANPC à 3 niveaux

Le convertisseur complet (3 phases) est représenté dans la Figure 8.

Cette solution a permis de réduire le bus bar utilisé et d'atteindre une densité de puissance de 57.59 kW/kg pour l'onduleur triphasé en ne prenant en compte que le bus bar, le condensateur du bus DC, les semi-conducteurs et son système de refroidissement dont le coefficient considéré est 4.5 kW/kg. Pour obtenir une estimation plus précise, il faut inclure des paramètres tels que les drivers et les éléments de fixation des composants.

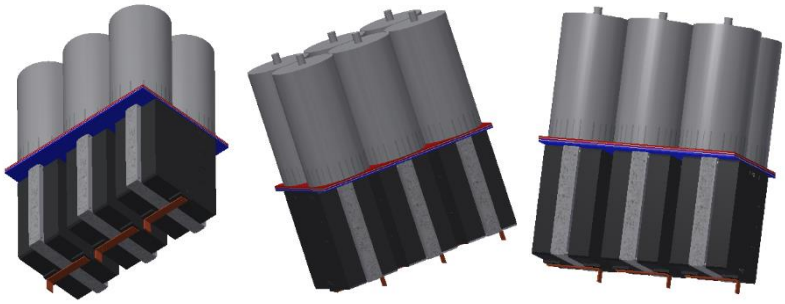


Figure 8. Onduleur NPC triphasé à 3 niveaux avec nouveaux modules de puissance

Chapitre IV : Performances des solutions choisies au cours du profil de mission

Le profil de mission de puissance considéré est illustré à la Figure 9. Trois options de dimensionnement peuvent être prises en compte. La première consiste à dimensionner l'onduleur pour le décollage qui correspond à la puissance maximale du profil. La seconde serait de le dimensionner pour la phase de croisière qui représente la phase la plus longue de la mission de vol. La troisième est de dimensionner pour un point milieu de la phase de montée. La puissance maximale est de l'ordre du MW et, pour des raisons de confidentialité, la valeur exacte ne peut être donnée : toutes les valeurs de puissance ont été normalisées par rapport à la puissance maximale.

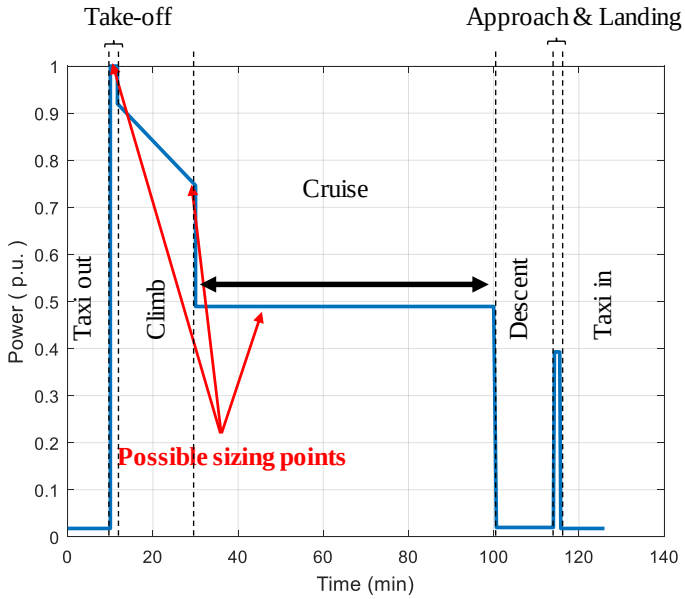


Figure 9. Profil de mission de puissance

Deux objectifs en termes de rendement pour l'électronique de puissance ont été fixés par le projet HASTECS. Pour l'objectif de 2025, le rendement devrait être supérieur à 98 % pour le point de croisière et supérieur à 96.5 % pour le point de puissance maximal. En revanche, pour l'objectif de 2035, le rendement devrait être supérieur à 99.5 % pour le point de croisière et supérieur à 99 % pour le point de puissance maximal.

L'objectif principal de ce chapitre est d'évaluer les topologies d'onduleurs choisies et les stratégies de modulation associées pour alimenter la machine électrique utilisée pour la propulsion de l'avion. Une étude comparative des stratégies de modulation est réalisée pour mettre en évidence la structure et la modulation présentant les meilleures performances afin de minimiser les pertes pour le point de dimensionnement choisi associé aux topologies FC et NPC à 3 niveaux.

Le rendement le plus élevé pour les scénarios étudiés correspond à la 2ème configuration machine (3conducteurs par encoche) avec DPWMMAX+ FW hybride pour les topologies FC 3 niveaux et NPC. La stratégie FW est alors utilisée pour le décollage et la DPWMMAX pour le reste de la mission de vol. Le Tableau 5 résume les objectifs en terme de rendement pendant les phases de décollage et de croisière et ceux obtenus en utilisant la 5ème stratégie qui est la DPWMMAX + FW qui a les meilleurs résultats pour la phase de croisière.

Tableau 5. Cibles et résultats atteints pour le rendement au décollage et en croisière

Phase de vol	**Objectif 2025**	**Objectif 2035**	**DPWMMAX + FW (décollage)**			
			FC 1er e-moteur	**NPC 1er e-moteur**	**FC 2ème e-moteur**	**NPC 2ème e-moteur**
Décollage	**96.5%**	**99%**	98.39%	98.39%	99.02%	99.02%

Croisière	**98%**	**99.5%**	98.84%	98.81%	99.09%	99.12%
Rendement global	-	-	97.86%	97.76%	97.84%	97.92%

Les objectifs de rendement pour 2025 ont été atteints en utilisant simplement la PWM sinusoïdal avec la première configuration de bobinage de la machine. Cependant, pour les objectifs de 2035, même avec la 2ème configuration de bobinage de la machine et la DPWMMAX, le rendement reste inférieur à celui désiré pour la croisière tandis que pour le décollage, l'objectif a été atteint avec le FC 3 niveaux. Néanmoins, la densité de puissance de la topologie FC est nettement inférieure à celle du NPC en raison de la masse supplémentaire des condensateurs flottants.

Conclusion et perspectives

L'objectif principal de ce manuscrit était de dimensionner un onduleur de puissance hautement intégré pour alimenter un moteur électrique d'une densité de puissance de 15 kW/kg pour la cible 2025 et de 25 kW/kg pour la cible 2035, incluant son système de refroidissement. Il fait partie du WP2 du projet européen HASTECS Clean Sky 2 qui vise à étudier la possibilité d'hybridation de la propulsion d'un avion régional et qui a été présenté en détails au chapitre I.

Suite à un premier dimensionnement simple pour un onduleur à 2 niveaux, le facteur principal pour augmenter la densité de puissance a été identifié au chapitre I. Deux options étaient envisageables. La première était de diminuer la masse du système de refroidissement en optimisant ses composants, ce qui a été fait par le WP4. Le deuxième était la réduction des pertes, qui fait partie des tâches du WP2.

Pour dimensionner le convertisseur de puissance, un outil de préconception a été développé. Cet outil est développé à l'aide de la programmation orientée objet sous *Matlab* et est basé sur le calcul analytique des pertes de l'onduleur afin d'évaluer le rendement et les températures des composants. Le calcul des pertes et les modèles thermiques utilisés ont également été présentés dans le deuxième chapitre. Ces modèles ont besoin de plusieurs paramètres de composants semi-conducteurs qui sont issus de la base de données disponible ou générés à partir de celle-ci afin de satisfaire les exigences en courant et en tension. Ces composants générés ont été validés à l'aide de plusieurs scénarios de cas d'étude et ont aidé à définir la tension du bus DC qui est la première tâche de ce travail.

Les calibres en tension des semi-conducteurs disponibles limitent la tension du bus continu qui pourrait être choisie si la topologie 2 niveaux devait être utilisée sans autoriser l'association série directe. La fréquence de découpage élevée représente également une contrainte pour les composants de grand calibre en tension qui ne sont pas conçus pour fonctionner à ces niveaux de fréquence. Ceci dit, il serait plus intéressant d'utiliser des composants de faible calibre en tension mais avec une tension de bus DC élevée pour réduire le courant nécessaire pour le même niveau de puissance. Cela pourrait être fait en utilisant des topologies multiniveaux.

Dans le chapitre III, les topologies d'onduleur, les stratégies de modulation et les technologies des composants semi-conducteurs ont été présentées. Comme indiqué au chapitre II, la réduction des pertes de l'onduleur pourrait être obtenue en utilisant des composants de faible calibre en tension. Ceci a été fait en utilisant des architectures multi-niveaux pour éviter l'association série directe. Les topologies utilisées étaient des topologies à 2, 3 et 5 niveaux. Elles ont été comparées à l'aide de balayages de tension de bus DC pour trouver la plage de tension de bus DC optimale pour chaque groupe de topologies. Si la tension du bus DC est comprise entre 700 V et 1 kV, la topologie à deux niveaux peut être utilisée, mais dans ce cas, plusieurs composants doivent être associés en parallèle pour supporter le courant imposé mais cela augmente la masse et le volume de l'onduleur. Si la tension du bus DC est comprise entre 1 et 2.4 kV, les topologies à 3 niveaux ont les meilleurs rendements pour cette plage de tension.

Cependant, si la tension du bus DC est comprise entre 2.4 et 3.5 kV, les convertisseurs 5 niveaux sont recommandés. Cette plage de tension dépend également de la fréquence de découpage utilisée. Ce paramètre est très important surtout pour les composants de fort calibre en tension et a un grand impact sur les pertes et donc la température maximale de jonction des semi-conducteurs. Les topologies à 3 niveaux et l'ANPC à 5 niveaux semblent être les plus adaptées à notre cahier des charges. Cette étude a également montré que, pour utiliser certaines topologies telles que les topologies à 2 ou 3 niveaux, elles doivent être utilisées avec une faible fréquence de découpage afin d'avoir une température de jonction acceptable.

Cela nous amène au deuxième point abordé au chapitre III, à savoir les stratégies de modulation. Les techniques de modulation multiniveaux pourraient être classées en fonction de la fréquence de découpage. Les modulations à haute fréquence de découpage ont des pertes par commutation plus élevées mais moins d'impact sur le courant de la machine puisque le filtrage haute fréquence est meilleur que celui en basse fréquence. Par conséquent, avec les méthodes à basse fréquence, le rendement est plus élevé. Dans ce travail, quatre stratégies de modulation, qui sont la PWM sinusoïdale, la PWM à injection de troisième harmonique, la PWM MIN et MAX discontinu et la pleine onde (FW) adaptée aux topologies d'onduleurs à 3 niveaux, ont été étudiées et comparées en termes de rendement afin de trouver la plus performante. La PWM sinusoïdale a le rendement le plus faible mais toujours proche des performances des autres. Le DPWMMAX est la meilleure en termes de rendement pour les deux topologies 3 niveaux sélectionnées.

Le troisième point abordé au chapitre III concerne les technologies des semi-conducteurs. Le choix des composants a un impact important sur les performances de l'onduleur car les pertes dépendent des paramètres de conduction et de commutation du semi-conducteur. Les nouveaux modules IGBT Mitsubishi de 7ème génération ont moins de pertes et ont un emballage compact et léger. Ces composants ont été comparés à la génération IGBT précédente ainsi qu'aux modules SiC avec les mêmes calibres de courant et de tension et semblent être la meilleure option pour notre cas.

En utilisant ces composants, la modulation DPWMMAX et un système de refroidissement optimisé avec une topologie NPC à 3 niveaux, l'objectif de densité de puissance de 15 kW/kg a été dépassé (23,29 kW/kg) mais le résultat est encore loin de la cible de 2035 qui est 25 kW/kg. Pour atteindre cette cible, un module de puissance a été conçu pour intégrer une demi phase de l'onduleur NPC 3 niveaux dans un seul boitier. Cette solution a permis de réduire la masse du bus bar utilisée et d'atteindre une densité de puissance de 57.59 kW/kg pour l'onduleur triphasé en ne prenant en compte que le bus bar, le condensateur du bus DC, les semi-conducteurs et le système de refroidissement. Pour obtenir une estimation plus précise, il faut inclure des paramètres tels que les drivers et les éléments de fixation des composants.

Dans le chapitre IV, plusieurs stratégies de modulation et points de dimensionnement ont été étudiés afin de trouver le meilleur scénario pour les stratégies de modulation des onduleurs à 3 niveaux FC et NPC en tenant compte de la mission de vol. Cette étude a été réalisée pour

deux configurations de bobinage du moteur électrique. La première stratégie étudiée était d'utiliser le THIPWM pendant le décollage et la montée afin d'utiliser pleinement le PWM sinusoïdal pendant la croisière. Cette stratégie améliore le rendement global de l'onduleur. La seconde compare la THIPWM et la DPWM MIN et MAX. La DPWMMAX se distingue de cette comparaison pour les deux topologies d'onduleurs et les deux configurations de la machine. La troisième utilise la FW sur tout le profil de mission. Dans ce cas, le rendement est amélioré, puisque la FW est une stratégie à faible fréquence de commutation, le THD est élevé pour les phases de faible puissance en raison de la présence des composantes harmoniques de basse fréquence. Pour éviter ce problème, les 4ème et 5ème stratégies ont été étudiées. Ces stratégies utilisent la FW en combinaison avec la PWM pour la 4ème et DPWMMAX pour la 5ème stratégie. Ceci améliore le rendement et le THD pendant les phases de faible puissance.

La stratégie la plus intéressante serait donc de dimensionner l'onduleur pour le décollage en utilisant la FW et d'utiliser la DPWMMAX pour les autres phases de la mission de vol. Cette stratégie permet d'atteindre les objectifs fixés par le projet HASTECS en termes de rendement pour la phase de décollage. Tandis que pour la croisière, le rendement obtenu est 99.12 % en utilisant un NPC 3 niveaux et la seconde machine alors que la cible de 2035 est 99.5 %. Pour toutes les stratégies de modulation, l'utilisation des paramètres de la seconde machine augmente le rendement de l'onduleur puisque pour la même puissance, la tension du bus DC utilisé est plus élevée et donc le courant plus faible, ce qui réduit les pertes dans les semi-conducteurs.

Pour améliorer le rendement de l'onduleur pendant la croisière, une autre solution peut être envisageable et qui est l'utilisation de deux convertisseurs ou plus. Dans le cas de deux convertisseurs, les deux peuvent être utilisés pendant le décollage. Ensuite, un seul est connecté au moteur pour le reste de la mission de vol. Cette solution pourrait être envisagée pour atteindre les objectifs de 2035. Cependant, la masse de l'onduleur pourrait être augmenté, ce qui réduirait la densité de puissance.

Il y a aussi la possibilité d'augmenter le nombre de bras d'onduleur en cas d'utilisation d'une machine multi moteur ou "multi stator" (double ou plus), en divisant le courant nécessaire pour alimenter le moteur par le nombre de phases. La deuxième option est d'entrelacer les bras du convertisseur par des inductances. Pour réduire la taille des inductances, des dispositifs de de fixation peuvent être utilisés ou le stator lui-même peut être utilisé comme dispositif d'accouplement (multi phase ou multi stator). Dans chaque cas, les pertes du convertisseur changeront et, en raison de la modification des formes d'onde de sortie, les performances du moteur et l'effet des décharges partielles seront affectés.

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