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Self-Heating Characterization of β-Ga_2O_3 Thin-Channel MOSFETs by Pulsed I-V and Raman Nanothermography

Nicholas A. Blumenschein, Neil A. Moser, Eric R. Heller, Nicholas Miller, Andrew J. Green, Andreas Popp, Antonio Crespo, Kevin Leedy, Miles Lindquist, Taylor Moule, Elisha Mercado, Manikant Singh, James W. Pomeroy, Martin Kuball, Gunter Wagner, Tania Paskova, John F. Muth, Kelson D. Chabak, and Gregg H. Jessen

***Abstract*—β-Ga_2O_3 thin-channel metal-oxide-semiconductor field-effect transistors (MOSFETs) were evaluated using both DC and pulsed I-V measurements. The reported pulsed I-V technique was used to study self-heating effects in the MOSFET channel. The device was analyzed over a large temperature range of 23 to 200°C. A relationship between dissipated power and channel temperature was established, and it was found that the MOSFET channel was heating up to 208°C when dissipating 2.5 W/mm of power. The thermal resistance of the channel was found to be 73°C-mm/W. The results are supported with experimental Raman nano-thermography and thermal simulations and are in excellent agreement with pulsed I-V findings. The high thermal resistance underpins the importance of optimizing thermal management in future Ga_2O_3 devices.**

***Index Terms*—Channel temperature, gallium oxide, MOSFET, pulsed I-V measurements**

I. Introduction

RESEARCH efforts on the gallium oxide beta (β-Ga_2O_3) polymorph are continuously growing because of its thermal and chemical stability, optical transparency, and bulk production capabilities using melt growth methods [1]. β-Ga_2O_3 has a lot of promise for high-power device applications because of its wide bandgap (E_g) of ~ 4.9 eV and estimated critical electric field (E_C) of 8 MV/cm, resulting in a Baliga's Figure-of-Merit (BFOM) of 3444 [2]. Following the first Ga_2O_3 transistor demonstrations [3], a report by Green *et al.* validated β-Ga_2O_3 as a high-power semiconductor material by fabricating a MOSFET with a breakdown electric field exceeding 3.8 MV/cm, which was the first demonstration of β-Ga_2O_3 having a higher breakdown field than both GaN (3 MV/cm) and SiC (3.18 MV/cm) [4]. These excellent material properties have allowed for the development of a wide variety of semiconductor devices such as high-voltage Schottky barrier diodes (SBDs) [5]–[7] and transistors with high current density [8]-[11], high breakdown voltage [3], [4], [12]–[15], radio frequency operation [11], [16], and vertical topology [17], [18]. Recently, work by Lv *et al.* demonstrated a source-field-plated Ga_2O_3 MOSFET with a record-setting power figure-of-merit ($V_{br}^2/R_{on,sp}$) of 50.4 MW/cm^2 [19].

One concern with β-Ga_2O_3 is its low anisotropic thermal conductivity [20], [21], posing additional challenges in designing high-power Ga_2O_3 devices with capability to extract enough heat to prevent thermal-related failures such as oxide breakdown. It has been proposed that effective heat extraction in β-Ga_2O_3 will likely require a combination of top-side and back-side thermal solutions [2], [22], [23]. To evaluate these methods of heat removal, it is imperative to quantify the channel temperature of Ga_2O_3 devices during operation independent of the thermal solution. Previous reports have shown success measuring channel temperature using methods such as Raman thermography [22], thermo-reflectance imaging [24], and electrical measurements [25]. Pulsed I-V characterization of β-Ga_2O_3 FETs has been reported at higher power operation by suppressing trapping and thermal effects [9]. Joh *et al.* reported on a simple pulsed I-V method that showed the ability to accurately measure the channel temperature of GaN high-electron mobility transistors (HEMTs) [26]. This method is beneficial because it does not require any special device layout or geometry, it can be used to measure packaged devices, and provides the channel temperature rather than a spatially averaged temperature. In this work, we apply the pulsed I-V measurement technique to Ga_2O_3 MOSFETs and prove its capability as a universal method to estimate the channel temperature. Raman nano-thermography was used to validate these results. This is the first report of Ga_2O_3 MOSFET channel temperature measurement that was verified using two separate

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N. A. Blumenschein, T. Paskova, and J. F. Muth are with the Department of Electrical and Computer Engineering, North Carolina State University, Raleigh, NC 27695 USA. (e-mail: nablumen@ncsu.edu).

N. A. Moser, E. R. Heller, N. Miller, A. J. Green, A. Crespo, K. Leedy, M. Lindquist, K. D. Chabak, and G. H. Jessen are with the Sensors Directorate, Air Force Research Laboratory, Wright-Patterson AFB, OH 45433 USA.

A. Popp and G. Wagner are with the Leibniz-Institut für Kristallzüchtung, Berlin, Germany.

T. Moule, E. Mercado, M. Singh, J. W. Pomeroy, and M. Kuball are with the Centre for Doctoral Training in Condensed Matter Physics, University of Bristol, Bristol, United Kingdom.

experimental methods.

II. EXPERIMENTAL DETAILS

A. Device Details

Metal-organic chemical vapor phase epitaxy (MOVPE) was used for homoepitaxial growth of a Si-doped β-Ga_2O_3 thin film channel on a (010) Fe-doped Ga_2O_3 substrate. The channel thickness and donor concentration was 65 nm and 2×10^{18} cm^{-3}, respectively. Ohmic contacts were formed by depositing a Ti/Al/Ni/Au (20/100/50/50 nm) metal stack, followed by rapid thermal annealing (RTA) for one minute at 470 °C in a N_2 atmosphere. The ohmic contact resistance was estimated to be ~ 11 Ω·mm using TLM test structures. From Hall measurements, the sheet concentration and mobility of the film were found to be 1.33×10^{13} cm^{-2} and 90 cm^2/V-s, respectively. A 20 nm Al_2O_3 gate dielectric was deposited by atomic layer deposition (ALD). A 90 nm SiO_2 layer was deposited using plasma-enhanced chemical vapor deposition (PECVD) to serve as a field oxide layer in the ungated access regions. A 0.14 µm gate length (L_G) was formed in the SiO_2 layer by etching a trench with CF_4 reactive ion etching (RIE) with the ALD Al_2O_3 serving as an etch stop. A 0.7 µm wide Ni/Au metal stripe was evaporated over the trench to form a T-shaped gate electrode. The Au pad layer was electroplated to a thickness of ~5 µm to serve as a heat sink. Fig. 1 shows an illustration of the depletion-mode MOSFET structure with source-to-drain (L_{SD}) and gate-source (L_{GS}) length of 8 µm and ~0.5 µm, respectively.

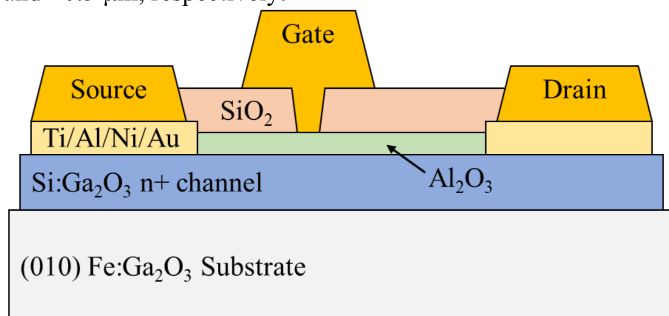

Fig. 1. Thin-channel β-Ga_2O_3 MOSFET device schematic.

B. Pulsed I-V Measurement Technique

Pulsed I-V measurements were performed at temperatures ranging from 23°C to 200°C using a DiVA D265 dynamic IV analyzer equipped with a gold-plated thermal baseplate. Simultaneous control of gate/drain voltage switching times were possible for sub-µs pulsewidths. This capability allowed the use of previously reported pulsed IV method that showed the feasibility in gathering transistor channel temperature information through pulsed IV measurements [26]. The technique involves a calibration step and measurement step. The goal of the calibration step is to gather temperature-dependent IV data without self-heating effects. To ensure that this was the case, we pulsed from zero quiescent gate/drain voltage conditions (V_{GSQ}, V_{DSQ} = 0V) and minimized the time in which the non-quiescent voltages (V_{GS}, V_{DS}) were active using a 200 nanosecond pulse width and 0.02% duty cycle. Previous experiments on GaN HEMTs showed that these pulsewidth and duty cycle conditions resulted in channel temperature measurements where an error of approximately 6°C was observed [26]. This error was reduced to ~ 0.5°C when shortening the pulsewidth to 100 ns. Unfortunately, we were unable to use a shorter pulsewidth because of equipment limitations. However, we observed no self-heating effects when using a 200 ns pulsewidth, indicated by the complete linearity of the pulsed I_D-V_{DS} curves up to a 15 V bias. By complying with these measurement conditions, we could assume that power dissipation did not affect the device temperature; thus, the temperature of the transistor channel was the same as that of the baseplate ($T_{CH} = T_{Baseplate}$). The IV characteristic was measured by applying a V_{GS} = 0 V and sweeping the drain voltage from 0 to 15 V. The on-resistance (R_{ON}) was determined at each temperature from the I_D-V_{DS} curve slope. Another key parameter used in this work was the maximum drain current ($I_{D,max}$), which we have chosen to define as I_D at V_{DS} = 15 V. Once these calibration measurements were complete, a temperature-dependent relationship was identified for both R_{ON} and $I_{D,max}$. The second part of the measurement technique required the use of non-zero quiescent drain bias conditions to induce self-heating in the channel while keeping $T_{Baseplate}$ at a constant 23°C. Here, V_{DSQ} and V_{DS} were both varied from 0 to 15 V. Since T_{CH} was unknown, the dissipated power ($P_D = V_{DSQ} \times I_{DQ}$) was calculated for each V_{DSQ} and used to create a relationship similar to that in the calibration step (P_D vs. R_{ON}, $I_{D,max}$). Thus, by using the T_{CH}-dependent data of the calibration step, the channel temperature was estimated using the P_D-dependent data of the measurement step.

C. Raman Thermography Measurement Technique

Peak temperature in the MOSFET channel was extracted using Raman nano-thermography. Titanium dioxide (TiO_2) nanoparticles with a 30 nm diameter were used to measure the temperature at four distinct locations on the MOSFET surface above the channel. The nanoparticles were distributed onto the device using a suspension of 99.98% pure TiO_2 particles mixed in methanol. Sonication of this suspense ensured a uniform density of particles throughout the methanol. The particle-ethanol suspense was drop cast onto the channel. The low density and small size of the TiO_2 particles minimize their effect on channel temperature. During device operation, owing to their low heat capacity, TiO_2 particles reach thermal equilibrium with the device channel almost instantaneously. The Raman peak shift of the particles is used to extract channel temperature. The temperature calibration method used has been previously described elsewhere [27]–[30]. During these measurements the wafer was mounted to an electrically grounded baseplate at a temperature of 25°C. Self-heating effects were evaluated in the device using DC bias conditions (V_G = 0 V, V_{DS} = 2 – 8V in steps of 2V). Experiments were carried out using a 532 nm Ar+ laser and 0.5 NA objective lens with a 0.64 µm spot size on the sample surface.

III. Results

A. Pulsed I-V Characterization

Fig. 2(a) shows the MOSFET DC I-V characteristic of a representative device when varying V_{DS} from 0 to 10 V and V_G from -16 to 0 V in 2 V increments. Fig. 2(b) shows the corresponding transfer characteristic while biasing the device at V_{DS} = 10 V. The inset shows the I_D transfer characteristic plotted on a log scale. A peak g_m of 12.8 mS/mm was observed at V_{GS} = - 13.2 V. A threshold voltage of -15.1 V was found through linear extrapolation of the I_D–V_G curve. Fig. 3(a) shows the I_D-V_{DS} characteristic when using a bias pulsewidth of 200 µs and varying $T_{Baseplate}$ from 23 to 100°C. Immediately observed was an expected temperature dependence where R_{ON} increased and $I_{D,max}$ decreased with T_{CH}. However, it can be seen that the slope of the curve does not remain linear up to V_{DS} = 15 V, and instead begins to saturate as it should if a DC bias were applied. This is due to the large 200 µs pulsewidth and 20% duty cycle, where unwanted power dissipation is

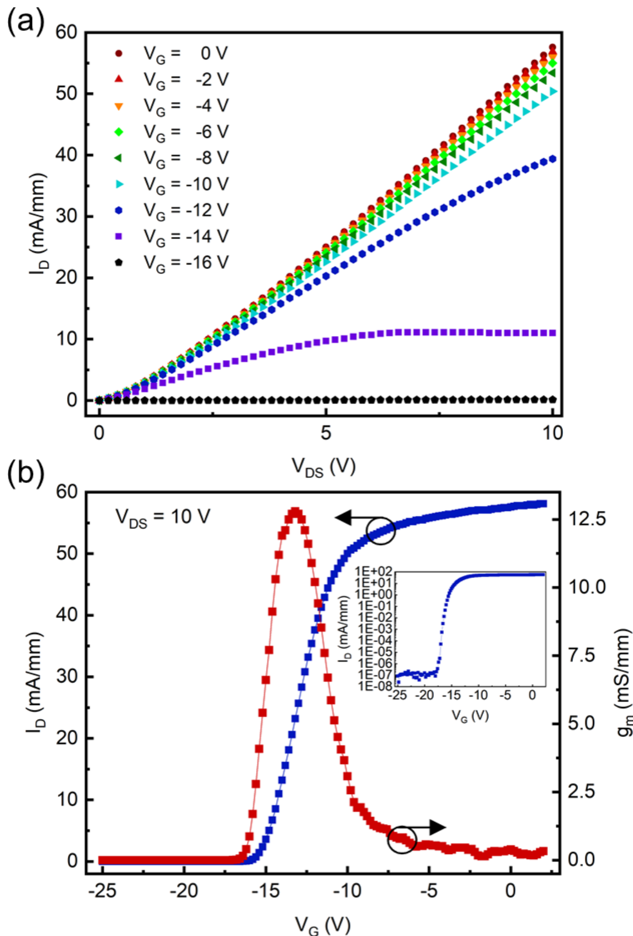

Fig. 2. (a) DC I_D-V_{DS} characteristic while varying V_G from -16 to 0 Volts and (b) Transfer characteristic when applying a 10V V_{DS}. Inset shows I_D plotted on a log scale.

causing heat to build up in the channel. Reducing the pulsewidth into the sub-µs range has the benefit of minimizing T_{CH} self-heating, as has been previously demonstrated for AlGaN/GaN devices [31]. For these reasons, as shown in Fig. 3(b), a 200 ns pulsewidth (0.02% duty cycle) was chosen for I_D-V_{DS} characteristic measurements. The desired linear IV relationship for the entire temperature range was observed. The R_{ON} had an RT value of 67.9 Ω-mm that increased to 84 Ω-mm at 200°C (24% increase) whereas $I_{D,max}$ had an RT value of 215.2 mA/mm that decreased to 176.4 mA/mm at 200°C (22% decrease). Figure 3(c) shows a plot of R_{ON} and $I_{D,max}$ versus T_{CH}.

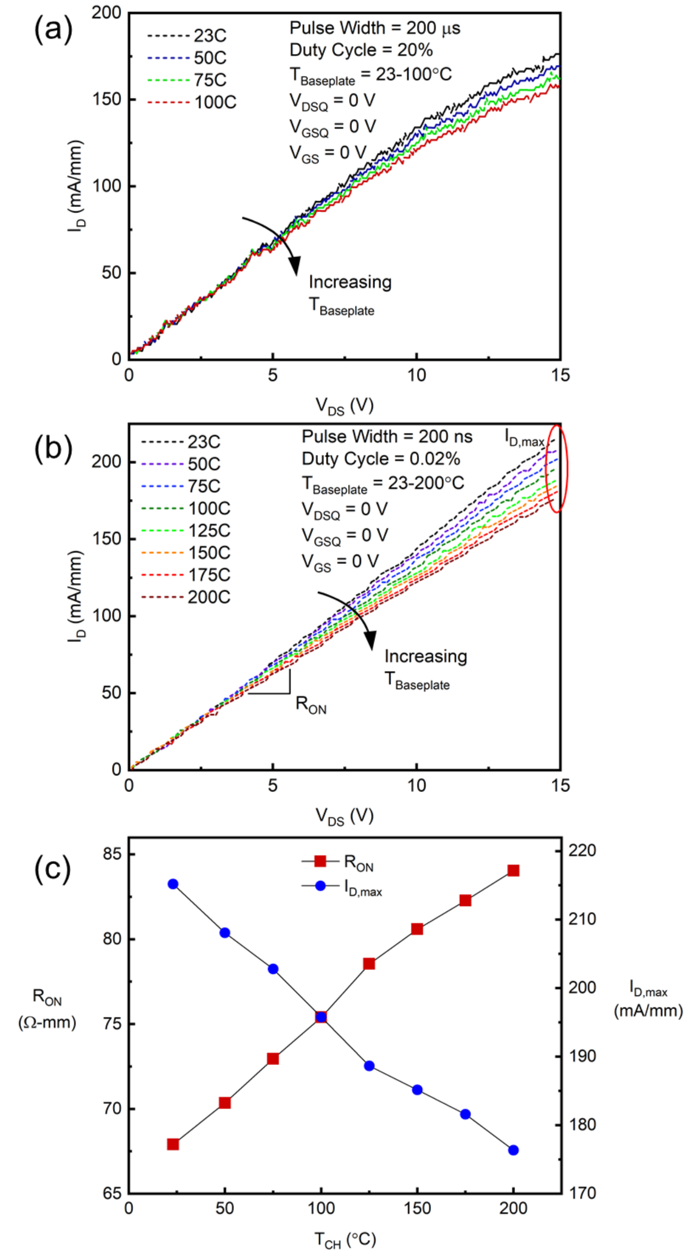

Fig. 3. Pulsed I_D-V_{DS} characteristic with varying $T_{Baseplate}$ when using a pulsewidth of (a) 200 µs and (b) 200 ns. (C) R_{ON}, $I_{D,max}$ parameters obtained from I_D-V_{DS} characteristic and plotted versus T_{CH}.

In the measurement step we used the same pulse conditions of 200 ns and 0.02% duty cycle, but also set the baseplate temperature to 23°C and used a non-zero V_{DSQ} to dissipate increasing amounts of power in the device. Fig. 4(a) shows the

I_D-V_{DS} characteristic under these conditions for a V_{DSQ} ranging from 2 to 15 V. The dissipated power was calculated for each V_{DSQ} condition using $P_D = V_{DSQ} \times I_{DQ}$ then plotted versus R_{ON} and $I_{D,max}$ as shown in Fig. 4(b). Using the R_{ON}–T_{CH} and $I_{D,max}$–T_{CH} data from Fig. 3(c), along with the R_{ON}–P_D and $I_{D,max}$–P_D data from Fig. 4(b), we were able to extract a family of equations [(1) - (4)]. From (1) – (4) we then obtained (5) and (6), which relate P_D and T_{CH}. Interestingly, (5) and (6) were nearly identical even though they were obtained separately using R_{ON} and $I_{D,max}$. Fig. 5 shows the estimated T_{CH} as a function of P_D as obtained from (5) and (6). The thermal resistance (R_{TH}) was extracted from the slope of the two T_{CH}–P_D curves using a least squares fit over the whole dataset, and estimated as the average value of 73 °C-mm/W.

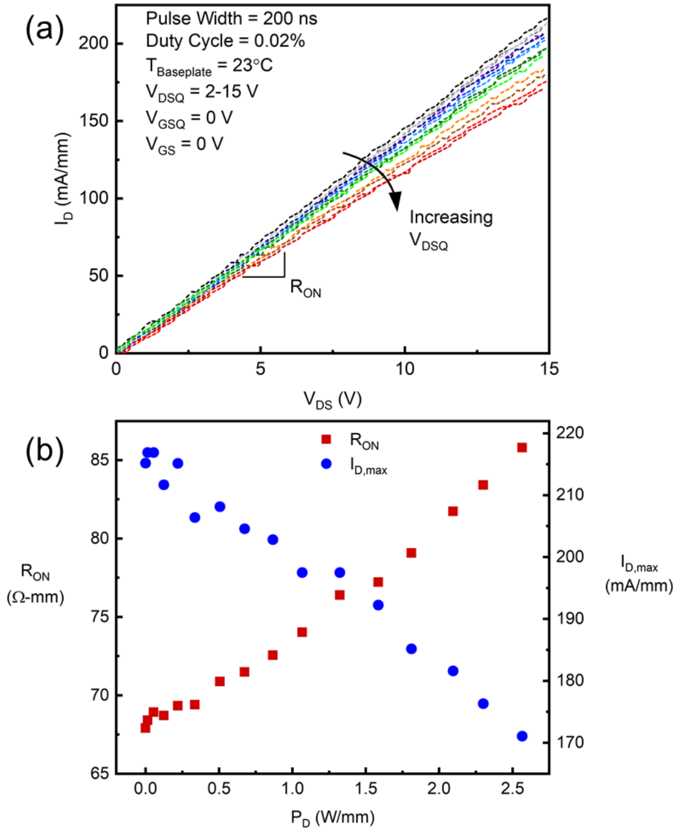

Fig. 4. (a) Pulsed I_D-V_{DS} characteristic when V_{DSQ} = 0 – 15 V and (b) resulting R_{ON}, $I_{D,max}$ versus P_D data.

$$R_{ON} = 0.09 \cdot T_{CH} + 65.96 \tag{1}$$

$$I_{D,\max} = -0.22 \cdot T_{CH} + 218.86 \tag{2}$$

$$R_{ON} = 6.64 \cdot P_D + 67.63 \tag{3}$$

$$I_{D,\max} = -16.87 \cdot P_D + 216.33 \tag{4}$$

$$T_{CH} = 70.63 \cdot P_D + 17.73 \tag{5}$$

$$T_{CH} = 76.78 \cdot P_D + 11.52 \tag{6}$$

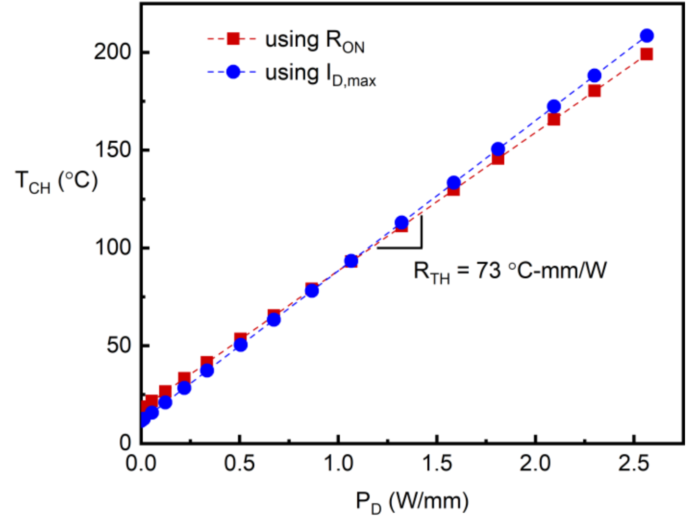

Fig. 5. Two independent estimations of T_{CH} that were found through R_{ON} and $I_{D,max}$. The resulting thermal resistance of 73°C-mm/W was found from the T_{CH}-P_D slope.

B. Raman Thermography

Fig. 6(a) shows the four locations of TiO_2 nanoparticles on the device surface during Raman thermography measurements. The Raman spectra of the TiO_2 particles was measured at each distinct location as a function of P_D. Four varying amounts of P_D were used (0.228, 0.517, 0.698, and 0.904 W/mm). Fig. 6(b) shows the resulting T_{CH} data as a function of TiO_2 nanoparticle location. The source, gate, and drain locations have also been denoted here using black arrows. The maximum T_{CH} was observed on the drain-side of the gate at a distance of 2.46 μm from the edge of the source contact for every amount of P_D. This is consistent with previous thermal characterization reports on Ga_2O_3 MOSFETs [22]. The T_{CH} measured at distances of 0.20 and 3.47 μm were all relatively similar in comparison for every P_D.

The pulsed I-V technique described in this work results in an average T_{CH} (and R_{TH}), whereas the Raman thermography measurement technique provides spatial information laterally across the channel. To better understand these two separate T_{CH}-P_D datasets the spatial T_{CH} information in Fig. 6(b) was plotted as a function of P_D as shown in Fig. 6(c). The R_{TH} found at each TiO_2 nanoparticle location is shown on the figure, and varies from 47 – 66 °C-mm/W. Colored lines show the linear fits for each TiO_2 nanoparticle location and their slopes were used to estimate R_{TH}.

Fig. 7 shows comparative T_{CH}-P_D data measured using the two techniques. The pulsed I-V data shown is an average of the two datasets shown in Fig. 5, where an R_{TH} of 73 °C-mm/W is observed. An average T_{CH} was taken for each TiO_2 particle to study how the Raman nano-thermography technique might vary from the pulsed I-V method. Taking this average resulted in an R_{TH} of 59 °C-mm/W, which is 19.2% lower than the value found when using pulsed I-V. It is likely that these two R_{TH} values would converge if more TiO_2 nanoparticles were used in the Raman measurements in areas underneath the drain-edge of the gate where the majority of thermal effects are

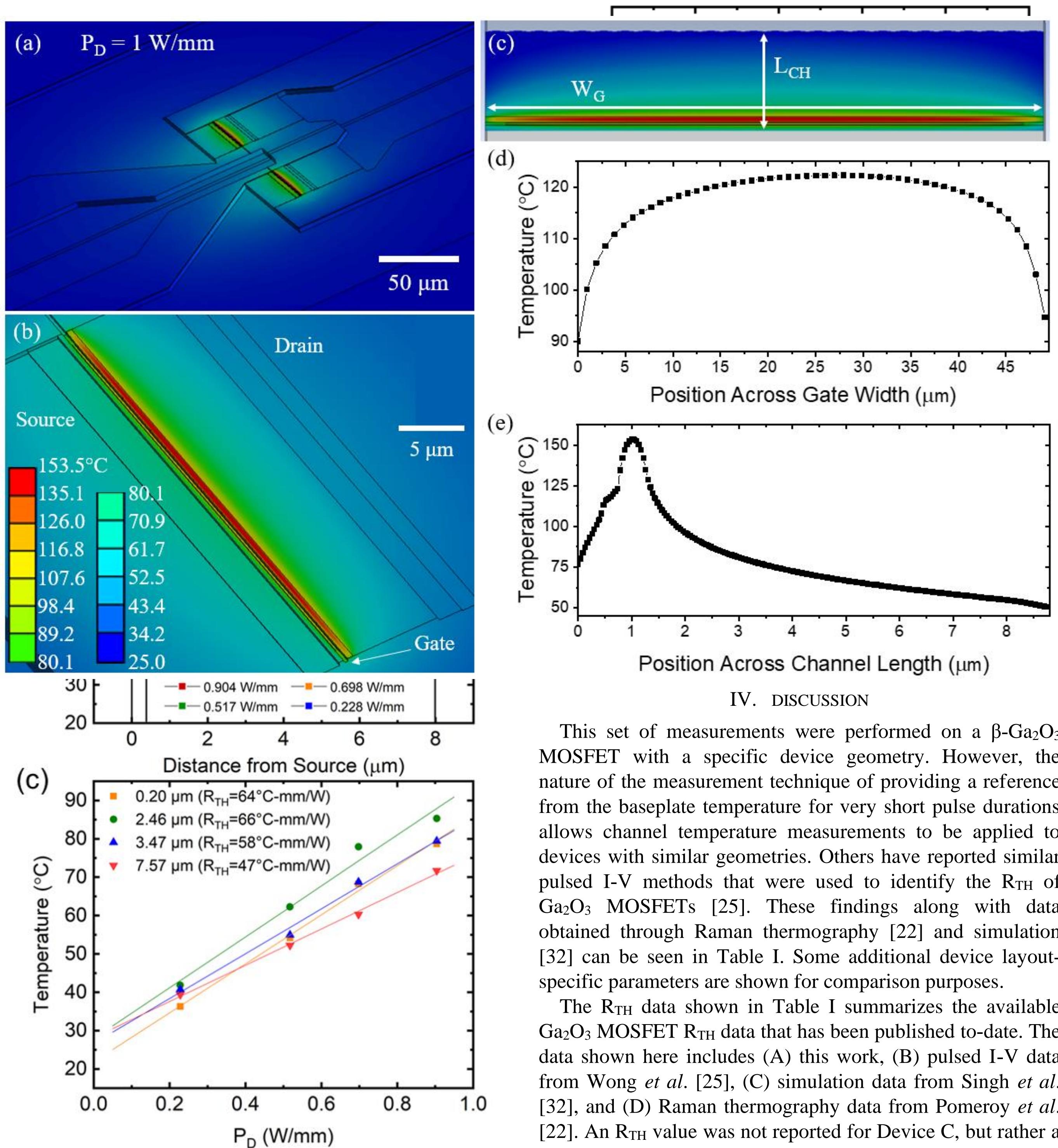

Fig. 6. (a) Position of TiO_2 particles on device surface indicated by red X, (b) T_{CH} data found by Raman thermography measurements using four different amounts of dissipated power at each distinct TiO_2 particle position, and (c) T_{CH}-P_D data at each TiO_2 location. Colored lines show linear approximations used to find R_{TH} for each TiO_2 location on the device surface.

observed. This point is further proven when looking at the thermal simulations in Fig. 8. Fig. 8(a)-(c) shows thermal simulations at varying levels of resolution with P_D = 1 W/mm. Fig. 8(d) shows the temperature profile along the gate width of the device centered at the drain-edge of the gate. This result

IV. DISCUSSION

This set of measurements were performed on a β-Ga_2O_3 MOSFET with a specific device geometry. However, the nature of the measurement technique of providing a reference from the baseplate temperature for very short pulse durations allows channel temperature measurements to be applied to devices with similar geometries. Others have reported similar pulsed I-V methods that were used to identify the R_{TH} of Ga_2O_3 MOSFETs [25]. These findings along with data obtained through Raman thermography [22] and simulation [32] can be seen in Table I. Some additional device layout-specific parameters are shown for comparison purposes.

The R_{TH} data shown in Table I summarizes the available Ga_2O_3 MOSFET R_{TH} data that has been published to-date. The data shown here includes (A) this work, (B) pulsed I-V data from Wong *et al*. [25], (C) simulation data from Singh *et al*. [32], and (D) Raman thermography data from Pomeroy *et al*. [22]. An R_{TH} value was not reported for Device C, but rather a plot of channel temperature as a function of power dissipation at an ambient temperature of 25°C. To compare the results for these four devices, we used the method described in this work to find the R_{TH} of Device C. Interestingly, this resulted in an R_{TH} of 116°C-mm/W, which was significantly higher than that reported by the other three papers. There are many variables that can alter R_{TH} (e.g. channel dimensions, substrate, ambient temperature, etc.). However, it appears that Devices B and C had a near-identical device layout, a (010)-oriented Fe-doped Ga_2O_3 substrate, and only a minor 5°C ambient temperature

Fig. 8. (a)-(c) Thermal simulations at varying resolutions while applying a P_D = 1 W/mm. Temperature profiles are plotted (d) across the gate width and (e) across the channel length.

TABLE I

Parameter	A [this work]	B [25]	C [32]	D [22]
R_{TH} (°C-mm/W)	73 / 59	48 / 56	116*	88
$T_{Ambient}$ (°C)	23 / 25	20 / 125	25	25
Meas. Tech.	PIV / Raman	PIV	Sim.	Raman
Substrate	(010) Fe-doped Ga_2O_3 with 650 μm thickness			
d_{CH} (nm)	65	300	300	300
N_D (cm^{-3})	2E18	3E17	3E17	3E17
L_{SD} (μm)	8	22	22	44
L_G (μm)	0.14	2	2	4
L_{GD} (μm)	7.36	15	15	30
L_{GS} (μm)	0.5	5	5	10
W_G (μm)	50	-	500	200
# of Fingers	2	1	-	1
d_{Al2O3} (nm)	20	20	20	20
H_{FP} (nm)	90	-	400	400

Comparison of this work (Device A) with previously reported β-Ga_2O_3 MOSFET thermal resistance values and corresponding device fabrication properties. H_{FP} represents the field-plate height.
* R_{TH} not reported; estimated here by linear fitting of T_{CH}-P_D data.

difference. Device B used a similar approach to that first reported by Joh *et al.*, but since a linear I_{DS}-T_{CH} relationship was not observed, they instead altered the technique by using a V_{DS}-dependent I_{DS}-T_{CH} calibration. From this calibration data,

they were able to obtain a relationship between channel temperature and DC power density, resulting in an R_{TH} of 48 °C-mm/W at 20°C. The data for Device C was found using single pulse thermal simulations where the channel temperature transient was evaluated at various amounts of power dissipation. The R_{TH} of 88°C-mm/W reported for Device D is similar to what was found in this work, despite some major device fabrication differences.

As seen in Table I, the devices tested in this work are more tightly scaled than those previously examined elsewhere, with smaller L_G and higher channel doping leading to a smaller and more tightly confined depletion region. During Ga_2O_3 MOSFET operation the majority of heat will be generated below the gate on the drain-side of the channel, and we expect that the physically small region for this thermal load will contribute to a larger temperature gradient and larger differences overall. As shown in Fig. 6(b), this is where we observed the highest T_{CH}. We believe this is one reason for the significant R_{TH} difference observed between the pulsed I-V results of this work and those from Device B in Table I. Device B had channel dimensions that were quite large in comparison to the MOSFET analyzed here, and since the pulsed I-V method provides an average R_{TH} of the channel, the heat created at the drain-side below the gate region has a lessened impact on R_{TH}.

V. CONCLUSION

Pulsed I-V measurements were performed to evaluate self-heating effects in β-Ga_2O_3 thin-channel MOSFETs. Characterization was performed within a wide temperature range of 23 to 200°C using sub-μs pulsewidths. The $I_{D,max}$ and R_{ON} were measured at each temperature, then used to identify a T_{CH}-P_D relationship. The T_{CH} was found to have a linear dependence on P_D, and a maximum T_{CH} of 208°C was observed for a P_D of 2.56 W/mm. The MOSFET channel was found to have a R_{TH} of 73°C-mm/W, which is in agreement with previous reports that analyzed channel temperature in β-Ga_2O_3 MOSFETs. Additional self-heating characterization was performed using Raman nano-thermography, which resulted in an average R_{TH} of 59°C-mm/W. Further reducing the R_{TH} in Ga_2O_3 devices by developing more efficient thermal management approaches will be important for improving performance. This work describes one possible thermal characterization method that can be used to evaluate new heat extraction concepts.

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