5-2018

Software Defined Radio for CubeSat Communication

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SOFTWARE DEFINED RADIO FOR CUBESAT COMMUNICATION

by

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**Capstone submitted in partial fulfillment of
the requirements for graduation with**

UNIVERSITY HONORS

with a major in

**Electrical Engineering
in the Department of Electrical and Computer Engineering**

**UTAH STATE UNIVERSITY
Logan, UT**

Spring 2018

Acknowledgements

Dr. Jacob Gunther - Faculty Mentor

Dr. Don Cripps - Design Course Instructor

Jolynne Berrett - Communications Course Instructor

Reggie Smith - Harris Corporation

Steve Meeker - ECE Tech Lead

Heidi Harper - ECE Store Coordinator

Software Defined Radio for CubeSat Communication

Final Report

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May 3, 2018

Revision History

Date	Revision	Description
4/5/2018	1	Initial Draft
4/21/2018	2	Revised Draft
5/3/2018	3	Final Draft

Executive Summary

Cube satellites, more commonly referred to as CubeSats, are small satellites that have become increasingly popular for academic, amateur, commercial, and scientific applications over the past five to ten years. These satellites provide a fairly inexpensive and compact platform for deploying many different types of equipment. While CubeSats do not allow for housing large, complex instruments, some organizations have begun to explore the possibility of deploying networks, or clusters, of CubeSats. Satellites in these clusters could theoretically be tied together via radio frequency communications to accomplish more than a single CubeSat could alone.

This report summarizes the preliminary design and development of a CubeSat software defined radio system for Harris Corporation. This system aims to facilitate communication between cube satellites using a compact, yet dynamic architecture. It is anticipated that the preliminary design of this project, described in this report, will be continued by future student design teams.

The preliminary design of this system has focused on two main components of the radio design. The first component is the electronic and programming design of the actual radio software and components. The second is the mechanical packaging that will encase the radio chip-set and mount within the satellite. The design and development of these components was performed concurrently.

Design of the electronic and software components included the design of two main subsystems: a transmitter and a receiver. The transmitter subsystem deals with receiving, modulating, and then transmitting incoming data. The receiver system involves demodulation, phase recovery, timing recovery, and error detection to then properly receive transmitted information. For this preliminary design, an image was captured using a camera and was then transmitted and received by the developed software defined radio system to demonstrate functionality.

Mechanical components for the radio packaging were developed to meet physical and thermal loading requirements. The mechanical packaging was designed to meet random vibration, shock, and equivalent dynamic loads. The thermal load requirements of the electrical components were taken into account to determine the thermal design needs of the packaging.

Expenses for this preliminary design fall well within the sponsor's provided budget of $10,000. Conceptual designs for the electrical and mechanical components of this preliminary design were completed during the first semester. Machining, programming, and testing took place during the second semester of the project.

Contents

1 Introduction

1.1 Overview

Cube Satellite systems (CubeSats) are small satellites that are based off a standard 10 cm by 10 cm base chassis design. This base chassis is often referred to as a one-unit, or 1U, chassis. CubeSat designs requiring larger chassis simply build off the base size by adding more units to the chassis. A 1.5U CubeSat, for example, would have a 10 cm by 10 cm by 15 cm chassis. A 3U CubeSat would have a 10 cm by 10 cm by 30 cm chassis. This modular architecture makes it easy to have a standardized sizing system that is simple to understand and design around.

Many commercial, educational, and research institutions have begun using CubeSats for space-based research and development projects. Applications include defense, communications, and commercial and scientific research. Many of these institutions are exploring the deployment of swarm and cluster missions of CubeSats to increase likelihood of mission success and to lower the cost compared to deploying a large satellite.

Software defined radios are a class of radio that implements components using software instead of hardware. These radios are preferred over traditional hardware radios for space-borne applications because they offer more flexibility in changing the operating parameters via software. They are much easier to update and reprogram from the ground without having to replace hardware components.

1.2 Problem Definition

With the increase in swarm and cluster missions of CubeSats, the communication needs of satellite missions have changed. For one satellite to communicate with another satellite in the mission, communication typically goes through ground, rather than directly between CubeSats. This causes unnecessary traffic in communication channels and is less efficient and reliable than direct communication.

This projects aims to solve this problem by designing a low-powered software defined radio to allow CubeSats to communicate reliably and effectively between each other in order to reduce mission risk and enable future mission capability. The radio is designed with capabilities of operating at frequencies from 70 MHz to 6 GHz, data rates from 100 Kbps to 20 Mbps, and bit error rates below 10^{-6}. This will allow much greater flexibility in transferring information at variable frequencies and data rates.

2 Materials and Methods

2.1 Electrical and Software Design

The system is designed around two key hardware components, the Analog Devices AD9361 Radio Frequency Integrated Circuit (RFIC) chip and the Xilinx ZYNC-7000 FPGA development board (ZC706). Most of the digital processing will be done in the FPGA, and the analog signal conversion and creation will be handled by the RFIC chip with data provided by the FPGA. Once the configurations are set, the RFIC chip will operate without any further commands.

The system will implement a QPSK (Quadrature Phase Shift Keying) digital modulation scheme for data transmission. Digital data, with the bits separated into symbols, will be input into the system and shaped into the outgoing waveform. Figure 1 shows the symbol interpretation of the data bits.

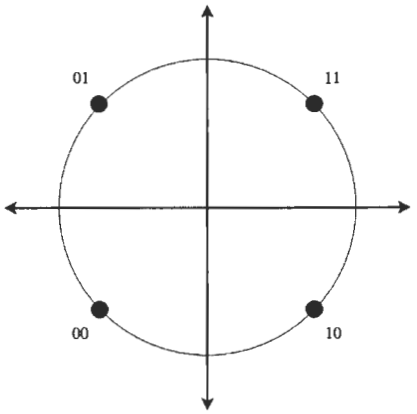

Figure 1: QPSK constellation diagram

The points on the diagram represent phase offsets of the sent waveform. If the bits that are to be sent are "1 1", then a transmission signal with a phase offset of 90° will be sent. To create these phase offsets the input data used to create in-phase (real) and quadrature (imaginary) components of the waveform. If the waveform was purely in-phase, there would be no phase offset. By adding together the two components the differing phases can be created.

Using this scheme allows for wide compatibility with current satellite systems and is simpler to implement than other modulation schemes. The system will operate with both transmit and receive capabilities as shown in Figure 2. This is necessary for use in swarm and cluster missions as described in Section 1.

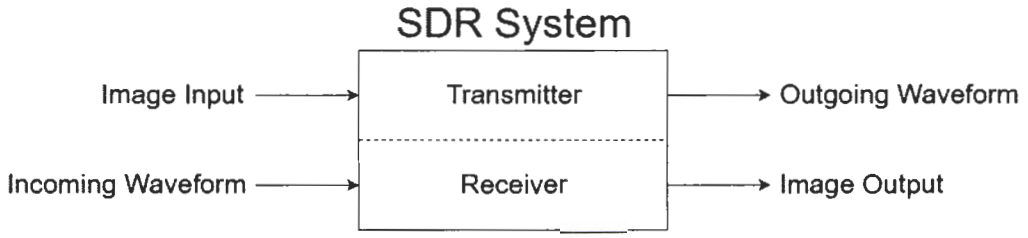

Figure 2: High level functional diagram

2.1.1 Data Transmission

Modulation converts digital data into an analog waveform for transmission. The steps to implement a modulator are shown in Figure 3.

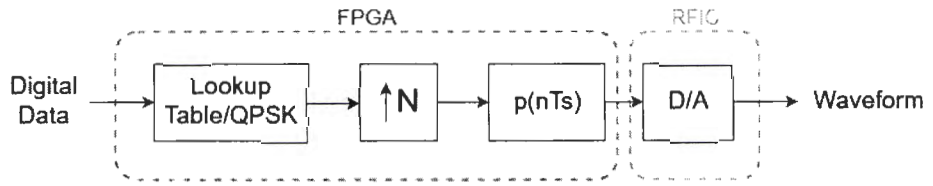

Figure 3: Transmitter subsystem diagram

Digital data entering the system is converted to QPSK symbols via a lookup table (LUT) as described in Section 2.1. The symbols are then upsampled ($\uparrow N$) to separate the QPSK symbols with additional data points. By doing this, a smooth sinusoidal output wave can be produced without the symbols mixing together in the consecutive stages.

After upsampling, a pulse shaping filter, ($p(nT_s)$), is applied. Pulse shaping, along with upsampling, separates the symbols so that the transmission of one symbol does not affect other symbols and limits the bandwidth of the signal to stay within federally allocated bands.

The processes from data input through pulse shaping are implemented on the FPGA. The output from the pulse shaping filter is sent directly to the RFIC to create the output signal.

This process of waveform creation is done for both the in-phase and quadrature components of the signal. Those components are added together and mixed to create the total output waveform. Mixing take the signal from baseband frequencies to the desired carrier frequency. This combination and mixing is also performed in the RFIC.

2.1.2 Data Reception and Recovery

The demodulator recovers symbols from the received analog waveform. At a high level, this process involves sampling, filtering, and aligning the received data points with those designated by the QPSK constellation. The receiver system also has to compensate for frequency and phase offset and ensure that samples

are taken at the appropriate time in the symbol. The output digital data will match that which was sent by the transmitter. This process is shown in Figure 4.

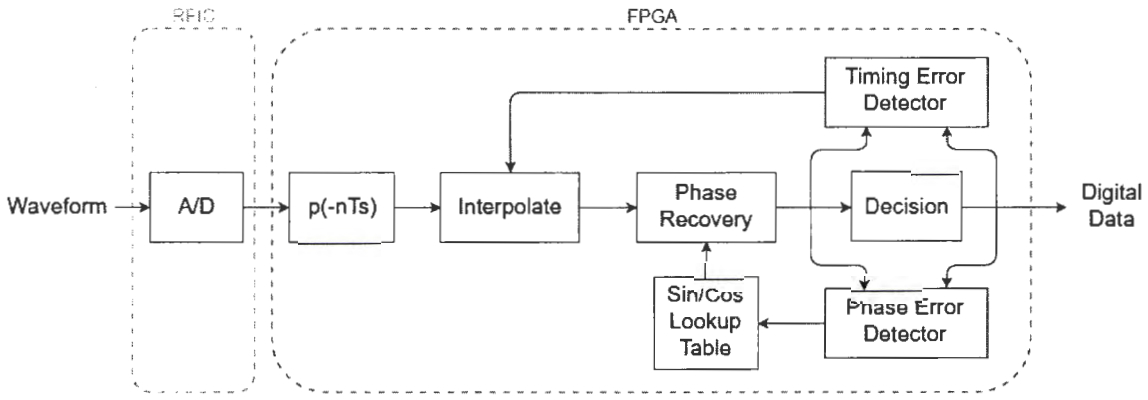

Figure 4: Receiver subsystem diagram

The received signal is sampled, de-mixed to baseband, and separated into in-phase and quadrature components by the RFIC. These separated data samples are then sent to the FPGA.

Once the data is received it goes through a set of matched and derivative matched filters. The matched filter is the reverse of the pulse shaping filter in Figure 3, hence the name matched. The characteristics of the pulse shaping and matched filter make symbol recovery a matter of keeping the filter output at the correct time. If the timing is correct the sample should be exactly on top of one of the constellation points and easily recovered. These kept symbols are sent to the decision block to convert the data point into a symbol. The decision block will compensate for quantization noise and noise from other signal sources in the received signal. The decision block may not, however, be able to compensate for other errors such as phase offset at the de-mixing stage and sample timing offset. To adjust for these offsets, timing and phase recovery subsystems are included in the demodulation system.

Design of the modulator with subsystem details is shown in Figure 5.

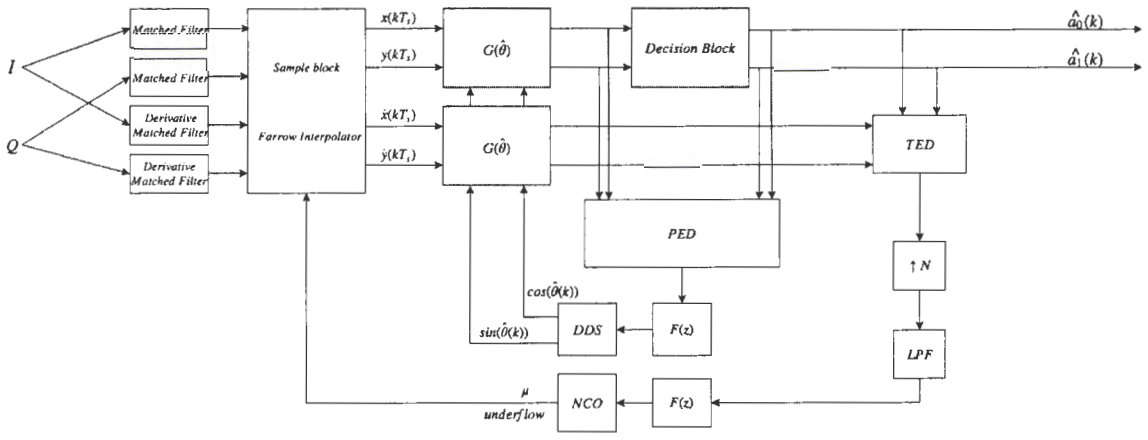

Figure 5: Detailed Demodulation System

The phase recovery subsystem is needed to detect and resolve offsets that appear after the received signal is de-mixed sinusoid. The system is able to correct for the detected offset as well as for small differences in frequency. This is accomplished primarily by the use of a Givens Rotator. The rotator uses input sine and cosine values at a given angle and rotates the received symbols by that angle. In order to find this rotation angle a filtered feedback system uses the received symbols and the decision output of those symbols. These received and decided symbols are used in a Phase Error Detector (PED).

When a phase error is detected, the output will be filtered and used to find the necessary rotation angle to correct the error. The filters prevent any sudden changes that may occur in the phase offset. The most common source of these changes is noise found in the input signal. Even in the presence of high noise, the filters will allow the rotation angle to settle to a consistent value.

This implementation of the phase recovery will potentially lock in at phase offsets other than zero. The reason for this is because the phase error is determined by the difference in the received symbol and the decided symbol instead of the true symbol. For example if the received signal is sampled with a phase offset of 180° the decision block will decide that the received symbol is correct and the PED will find zero phase error. There will be no rotation of these symbols even though they have been improperly received. To combat this, differential encoding will be implemented to encode the transmitted data in symbol changes instead of the symbols themselves. By doing this the data at the output will be correct even if the phase recovery system locks on to the wrong phase.

The timing recovery system is needed to compensate for differences in the sample timing in the send and receive systems. These differences can be caused by error in the sampling frequency or by sampling before of after the optimal time at the receiver. The timing recovery system as implemented can compensate for both types of timing error.

The timing recovery system is centered around an interpolator that approximates what the received sample would have been without any timing error. The interpolator uses four previous input samples and a fractional interval. The interpolator fits the received samples to a third order polynomial and uses the fractional interval as the time value at which to compute the estimated sample. The timing recovery system also computes when to save the interpolator output as the received symbol. The symbol timing calculated by the timing system is labeled as underflow in Figure 5.

To compute the timing error, the decided symbols are used along with the output of a derivative matched filter. The timing error is filtered and used to compute the fractional interval and create the underflow signal.

2.1.3 MATLAB Implementation and Simulink Model

The initial design was implemented in MATLAB to verify functionality and to demonstrate understanding of the components in the system. Each component was programmed individually and tested to ensure that the outputs were correct and each piece was functioning appropriately. This allowed the system to be modularized and also enabled better understanding of each piece and its design and function.

Components were then pieced together to run higher-level system simulations and ensure system functionality. Once these simulations were verified and the complete system was built, the system modules were implemented using a block diagrams in Simulink. This modular design simplified the implementation and verification process by allowing individual modules to be tested and debugged before system integration.

A few plots from that simulation are seen in Figures 6 and 7. Figure 6 is a plot of received symbols without any phase or timing error. Using these data points would result in many errors and cause the received data to be almost unusable. Figure 7 shows the same symbols after passing through the phase and timing recovery systems. There are a few symbols that would result in error, but they are some of the first symbols to be transmitted. Once the system has locked into the needed phase and timing changes the received

symbols are group tightly around the constellation decision points.

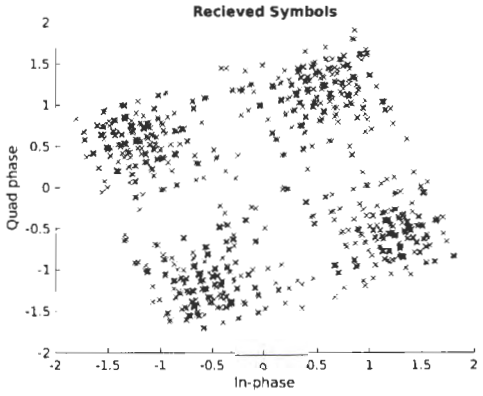

Figure 6: Received Symbols - no phase or timing recovery

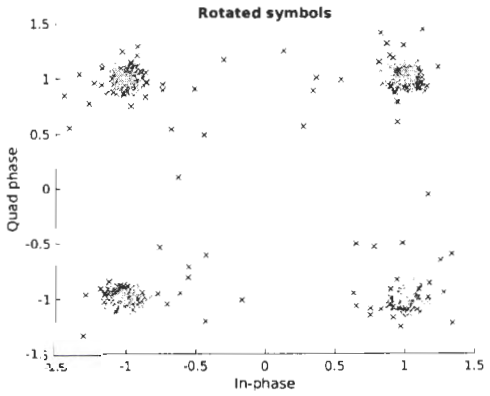

Figure 7: Received Symbols after phase and timing recovery

2.1.4 HDL Code Blocks and Vivado Project

Simulink's HDL Coder was used to convert the blocks from Simulink into HDL code. Any blocks that were not easily implemented in Simulink were coded by hand using Verilog or using included functional blocks(IPs) in Vivado.

HDL code blocks were then packaged as IP blocks and imported into a project in Vivado, where they were connected together into the final system implementation to be loaded onto the FPGA.

The simulation design was converted to digital logic by converting all of the numerical calculations to Q15 binary fixed point format with saturation overflow. Q15 format is a binary representation of fractional numbers that uses one sign bit and 15 bits to represent a decimal value. By using Q15 the system can perform calculations with a precision of 0.0000305. This precision should introduce less error into the signal than is already present from noise making the fixed point representation essentially the same as a full precision representation. These calculations were kept to a Q15 format by rounding all of the computation outputs.

Saturation at overflow is used to prevent the received signal from wrapping around from positive to negative or vice versa if the computations overflow. To implement saturation the system checks if the number has wrapped around, and if it has set the value to the most positive or negative value depending on what the value was before overflowing.

2.2 Mechanical Design

2.2.1 Conceptual design

CubeSat internal components, such as boards and electronic hardware, usually conform to the PC/104 form-factor. This form-factor or standard specifies the dimensions that boards should use so that they can be stacked as shown in Figure 8. Because of this, it was decided that the final packaging design should conform to this form-factor so that the package could be fairly universal.

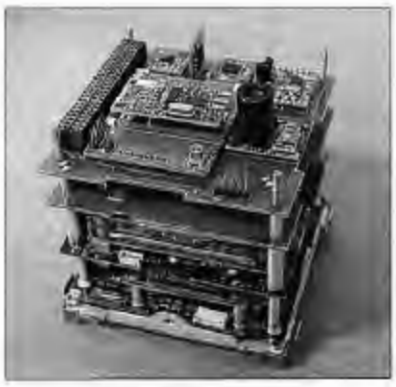

Figure 8: Typical CubeSat board stack

To protect the radio components from electromagnetic interference, the packaging was designed to enclose the SDR chip-set and board entirely. The final packaging houses the FPGA and board as shown in Figure 9. This way, it should be possible to mount this packaging as desired within a stack. However, it should be noted that this packaging will interfere with the traditional pin stack used to tie together PC/104 boards.

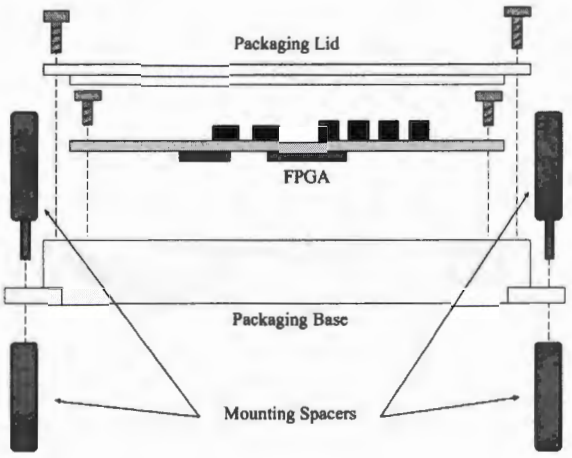

Figure 9: Final packaging concept illustration

2.2.2 Material Selection

Four different types of metal were considered for the mechanical packaging of the SDR system: 304 stainless steel, 304L stainless steel, 2024 T4 aluminum alloy, and Grade 1 titanium. These metals were considered for their strength, their frequent use in aerospace-grade designs, and their resistance to out-gassing in zero-atmosphere environments. Figure 10 shows the decision matrix used to compare these metals. The strength-to-weight ratio for each metal was calculated by dividing the yield strength of the metal by its density.

	Weight	304 Stainless Steel	304L Stainless Steel	2024 T4 Aluminum	Grade 1 Titanium
Strength-to-weight Ratio	25	26.88	26.25	100.72	37.69
Thermal Conductivity (W/m-K)	25	16.2	16.2	121	16
Machinability	25	Poor	Poor	Good	Poor
Price	25	Medium	Medium	Medium	High
Total	100	150	150	250	150

Yield Strength (MPa)		215	210	280	170
Density (g/cm^3)		8	8	2.78	4.51

Exceeds = 3 Points
Meets = 2 Points
Questionable = 1 Point
Does Not Meet = 0 Points

Figure 10: Decision matrix used to recommend and select a metal for the mechanical packaging

From this matrix, 2024 T4 aluminum was selected for its superior strength-to-weight ratio, great thermal conductivity, and cost. While the T4 temper was specifically examined in this decision matrix, the T3 and T351 tempers were used to produce our metal prototype. This was done because these tempers are more readily available from suppliers than 2024 T4 aluminum. The properties of these tempers are very similar to those of 2024 T4. See Table 1 for a comparison of these different tempers.

Table 1: Aluminum Association listed properties for 2024 Aluminum

Temper	Yield Strength	Ultimate Strength	Modulus of Elasticity
T3	345 MPa	483 MPa	73.1 GPa
T351	324 MPa	469 MPa	73.1 GPa
T4	324 MPa	469 MPa	73.1 GPa

2.2.3 Preliminary Design and Analysis

Initial calculations were performed to determine the minimum thickness of the packaging per the safety factors listed in requirement 4.3.7. The maximum mass of 0.3 kg listed in requirement 4.3.2 and the equivalent dynamic loading of 60g listed in 4.3.5 were used to calculate a maximum equivalent load of 176 N.

Using the maximum equivalent load, calculations were then performed to analyze a tensile load. A 'beam width' of 7 cm was assumed for these calculations to establish a conservative initial width. A bending moment analysis was conducted, modelling a single wall of the packaging as a simply supported beam. A width of 7 cm was used again for these calculations.

Using these initial calculations as a baseline, a preliminar. model of the packaging was then created in SolidWorks. The initial packaging design was set to be 80 mm wide by 80 mm long to fit inside the maximum dimensions described in requirement 4.3.1 and to provide room for connectors. In designing with these dimensions, an upper bound for the mass of the packaging was estimated with a rough over-design of the SDR packaging. This initial design is shown in Figure 11.

Figure 11: CAD model of initial packaging design

Using this initial design, three static load analyses were performed to roughly gauge the performance of the packaging design. A static load of 200 N was applied individually to each face as shown in these analyses. A 200 N load was chosen as an over-estimation of the equivalent load for the initial design.

With a general idea of how the packaging would perform under stress, the packaging design was then iterated to reduce the mass of the packaging while providing as much space as possible for the PCB board and chip-set. The location and dimensions of the mounting holes were also redesigned to conform with the PC/104 standard as specified in the PC/104 Specification Version 2.6 released by the PC/104 Embedded Consortium (see Appendix D for mechanical drawings and dimensions for the PC/104 standard). It was decided to have three mounting pads for the PCB board so as to provide sufficient wall space for RF and data connectors.

A plastic, 3D printed prototype of the semifinal packaging base, shown in Figure 12, was created to provide a visual item to inspect before machining the metal prototype. This prototype was presented to the electrical engineering students for feedback. The prototype was then taken to the student prototype lab to make sure that the design conformed with the requirements of available CNC bits and machinery. Small revisions were made to the fillet radii of the design so that the metal prototype would be easy to machine. The final design for the packaging, with these revisions, is shown in Figure 13.

Figure 12: 3D printed packaging prototype created to finalize design

Figure 13: CAD model of final packaging base

The final packaging design fits completely within the form factor of the PC/104 standard. This means that the packaging should easily fit within a standard CubeSat chassis. Since the packaging was designed according to the PC/104 mounting standard, the packaging should also be easily usable within existing CubeSat standards and mounting architecture. As can be seen in Figure 13, this design does not include holes for connectors or for venting. The locations and dimensions of these features have been left for future teams to determine once the location of electronic components is better defined. These features should be fairly easy to incorporate into this design, as sections of the walls have been left free to account for these future additions. The mounting holes for the lid and PCB board were sized for 8-32 threads (see Appendix B for mechanical drawings of the packaging).

The lid for the main packaging was designed with an inset which fits into the main packaging. This inset

performs two main functions. First, it helps to align the lid with the packaging. Second, the inset help provide electromagnetic shielding. These features can be seen in Figure 14.

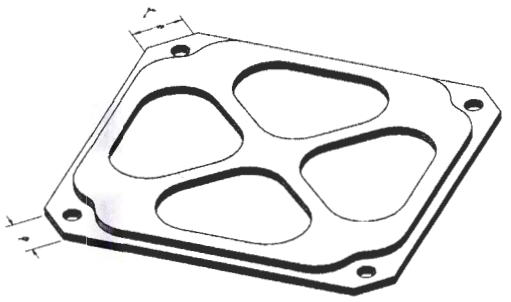

Figure 14: CAD model of final packaging lid

2.2.4 Static and Dynamic Load Analysis

Several different analyses were performed to ensure that the final packaging design meets the project requirements. Acceleration stress tests were conducted on the final package design to determine the minimum safety factor of the final design with an acceleration load of 60g applied along the major axial directions. This same analysis was performed on the lid, however only in the direction normal to the lid face.

With the SolidWorks CAD models finalized and the acceleration, modal, and random vibration analyses complete, a metal prototype was developed to use for physical vibration testing. The base of the packaging was machined out of 2024 T351 aluminum and the lid was created using 2024 T3 aluminum. To provide results consistent with the prototype, all SolidWorks analyses were conducted assuming using these tempers. The properties used in SolidWorks are listed in Table 2.

Table 2: SolidWorks listed properties for 2024 Aluminum

Temper	Yield Strength	Ultimate Strength	Modulus of Elasticity
T3	345 MPa	485 MPa	72.4 GPa
T351	325 MPa	470 MPa	72.4 GPa

2.2.5 Random Vibration and Modal Analysis

A modal analysis was conducted on the packaging assembly to identify the natural frequencies of the mechanical packaging. The entire assembly was analyzed together to identify the possible natural frequencies of the packaging when assembled. This was done by mating the lid to the packaging with a fixed mating. Recognizing that this assumption does not represent how the lid is actually attached to the base, the base and lid were then analyzed separately to determine if their natural frequencies overlap.

The final analysis performed on the SolidWorks model of the final packaging was a random vibration study. This study was performed according to the random vibration requirements detailed in GSFC Standard 7000, revision A, as specified by requirement 4.3.3. For this analysis, the base and lid of the packaging were tested together as if they were one unit. It is acknowledged that this assumption does not allow for very accurate analysis of how the packaging components would interact with one another under random vibration loads. However, this study was conducted this way because: the natural frequencies of the packaging components lie above the range of frequencies tested, time constraints did not allow for a more detailed analysis in

SolidWorks, and set of physical vibration tests were to be conducted. The physical vibration tests, along with a mass-model test of the system, have been left for the next phase of design.

2.2.6 Thermal Analysis

The mechanical packaging is required to transfer heat from the power generating circuits to the CubeSat frame, which is connected to a separate thermal regulation system. A thorough study of the thermal regulation of a CubeSat similar to what this radio will be implemented on is given in a study by Soo-Jin Kang and Hyun-Ung Oh [1]. Because every CubeSat is not the same, and all components are not known, a system-wide analysis like what is shown in this study is impossible. As such, the temperature values from the aforementioned study will be used.

The packaging is required to fit into a 1U CubeSat using mounting screws on the four corners. In this thermal analysis, it is assumed that the mounting screws will never exceed the temperature bounds shown in the study by Soo-Jin Kang. It is also assumed 3 W will go through the contact area of the FPGA and 0.75 W will go through the contact area of the RFIC. An important aspect of thermal analysis is that there is never perfect contact between two surfaces. As such, a thermal gel or paste is often used to improve the thermal contact of two surfaces. In analysis, a thermal resistor must be accounted for at each interface. For this analysis, a 60 mil (1.524 mm) thick coating of thermal gel with a thermal conductivity of 2.8 $W/(m \cdot K)$ was used wherever the packaging was in contact with an integrated circuit. The contact resistance of the screws was estimated by a 10 mil (0.254 mm) thick resistor with a thermal conductivity of 1.0 $W/(m \cdot K)$.

Additionally, the surface temperature is not the temperature that determines whether a chip fails. Thus, the junction temperature is calculated for each chip using values provided by the manufacturer. These values are 0.23 °C/W for the FPGA [2] and 9.6 °C/W for the RFIC [3]. The maximum allowable junction temperatures are 125 °C for the FPGA [2] and 110 °C for the RFIC [3].

3 Results

Table 3 summarizes the method and status of verification for the requirements as identified and described in the Specifications Document for this project. In Progress denotes that the requirement is not yet fully met and will be completed in subsequent phases of the project.

Table 3: Verification Status

Requirement ID	Description	Method of Verification	Status
4.2.1	System is an implementation of a Software Defined Radio capable of transmitting and receiving waveforms.	Inspection	Passed
4.2.2	System shall demonstrate transmit and receive capabilities by sending or receiving an image.	Inspection	In Progress
4.2.3	System shall demonstrate transmit and receive operations at a distance of at least 3 ft.	Inspection	In Progress
4.2.4	System shall be able to output a symbol constellation diagram to demonstrate the QPSK modulation scheme.	Test	In Progress
4.2.5	System shall operate between 10. Kbps and 20 Mbps and shall demonstrate at least 4 steps of adjustability in between these bounds.	Test	In Progress
4.2.6	System shall operate at a nominal frequency 2.45 GHz, which is allocated in the ISM band by the FCC. System shall be adjustable in the RF frequency range.	Test	In Progress
4.2.7	System shall use less than 4 watts of power.	Test	In Progress
4.2.8	System shall make use of the Analog Devices AD9361 RFIC chip.	Inspection	Passed
4.2.9	Syste. shall include a user interface that is capable of changing basic parameters and reporting system status.These parameters shall include, but shall not be limited to, the operating frequency and the data rate.	Test	In Progress
4.2.10	System shall include a waveform lock indicator.	Test	In Progress
4.2.11	Dynamic BER test shall be implemented such that it can test with an added noise signal or with no added noise.	Test	In Progress
4.2.12	System shall demonstrate operation with a BER at or below 10^{-6}.	Test	In Progress
4.2.13	System will be laid out on a PCB.	Inspection	Passed
4.2.14	System shall operate in half duplex for transmit and receive.	Test	In Progress
4.2.15	System will have a link budget as stated in Specifications.	Analysis	In Progress
4.3.1	System and packaging shall have maximum dimensions of 100 mm by 100 mm by 50 mm.	Inspection	Passed
4.3.2	System shall have a maximum mass of 0.3 kg.	Inspection	Passed
4.3.3	System shall meet random vibration qualifications in the frequency range of 20-2000 Hz as specified in GSFC standard 7000, revision A, section 2.4.2.5 and Table 2.4-3.	Test & Analysis	In Progress
4.3.4	System shall withstand steady-state loads of 8.5g.	Analysis	Passed
4.3.5	Cantilevered components of the system shall withstand a static and dynamic equivalent load of 60g.	Analysis	Passed
4.3.6	The packaging shall maintain the electronic components between temperature of -40° C and 85° C.	Analysis	Passed
4.3.7	All packaging components shall meet the following safety factors: Yield - 1.25, Ultimate - 1.50, No Test - 2.0.	Analysis	Passed

3.1 Electrical and Software Results

3.1.1 Simulation Results

The full software system was successfully simulated in MATLAB. These results demonstrated the correct operation of the system and its components before converting to HDL code for implementation on the FPGA. The correct frequencies and data rates were simulated with verified QPSK modulation. The algorithms for timing and phase error detection and recovery were also verified.

3.1.2 Hardware Results

Hardware results are currently in progress and will be continued in subsequent phases of the project. HDL code is nearly complete and will be synthesized, debugged, and implemented on the FPGA, after which hardware testing will commence as outlined in the Specifications Document.

Following the hardware implementation of the software on the FPGA, a custom PCB board will be designed. The mechanical packaging will be refined to fit this board and will also undergo further testing. Final results for the project will include a fully packaged prototype for Harris Corporation.

3.2 Mechanical Results

3.2.1 Static and Dynamic Analysis Results

Figures 15 through 17 depict the results of the static load simulations performed on the initial packaging model. These loads were applied in the three axial directions, with the inside of the mounting holes set as fixed faces. The overall minimum safety factor for these analyses was found to be 22.

Figure 15: Stress distribution for the x-axis static loading study of the initial packaging base

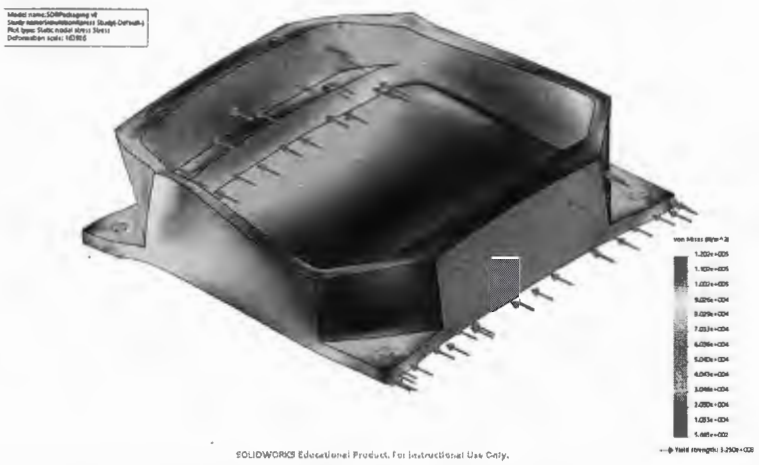

Figure 16: Stress distribution for the y-axis static loading study of the initial packaging base

Figure 17: Stress distribution for the z-axis static loading study of the initial packaging base

Images of the acceleration stress analyses can be seen in Appendix C. The minimum safety factors against yield found from these analyses for the base and lid are shown in Table 3. The fixture conditions for these analyses were the same as those used for the static tests of the initial packaging design, where the inside faces of the mounting holes were fixed in place.

3.2.2 Random Vibration and Modal Analysis Results

Table 4 shows the first five natural frequencies of the mechanical packaging as found by performing a SolidWorks frequency analysis. Images of the deflections and modal shapes for each of these modes are shown in Appendix C. These analyses were conducted by fixing the inside faces of the mounting holes for each model.

The results of the random vibration analysis can be seen in Figure 18. For this analysis, the inside faces of the mounting holes were fixed. The model was then vibrated using a uniform base excitation matching the

Table 4: Minimum safety factors found for an acceleration load of 60g

Part	Direction of Applied Load	Minimum Safety Factor
Base	Y+	66.79
Base	Y-	66.79
Base	X+	244..
Base	X-	244.8
Base	Z+	229.5
Base	Z-	229.5
Lid	Z+	49.53
Lid	Z-	49.53

Table 5: Natural frequencies of the mechanical packaging components and assembly

Part	Mode 1 (Hz)	Mode 2 (Hz)	Mode 3 (Hz)	Mode 4 (Hz)	Mode 5 (Hz)
Base	2369	4133	4658	5244	6584
Lid	1987	3456	3705	3801	6403
Base + Lid Assembly	3127	3539	5021	5342	6668

specifications of GSFC Standard 7000, revision A, Table 2.4-3.

Figure 18: Stress distribution for the random vibration study of the packaging base and lid assembly

3.2.3 Thermal Analysis Results

Using a fixed temperature of 30 °C on all four corners and a fixed power output of 3 W on the FPGA and 0.75 W on the RFIC, the temperature of the FPGA surface at steady state is 47.45 °C, and the temperature of the RFIC is 46.55 °C. These are acceptable values for an on-orbit level qualification. Using values provided by the manufacturer, the actual junction temperatures of the chips are calculated to be 48.14 °C for the FPGA and 53.75 °C for the RFIC. For flight qualification level conditions, an additional 21 °C is required to be added to the ambient temperature. Accordingly, another analysis with a fixed temperature of 51 °C at the corners shows surface temperatures of 68.45 °C on the FPGA and 67.55 °C on the RFIC. The actual junction temperatures are 69.14 °C on the FPGA and 74.75 °C on the RFIC. A visualization of the temperature distribution in the packaging is shown in Fig 19.

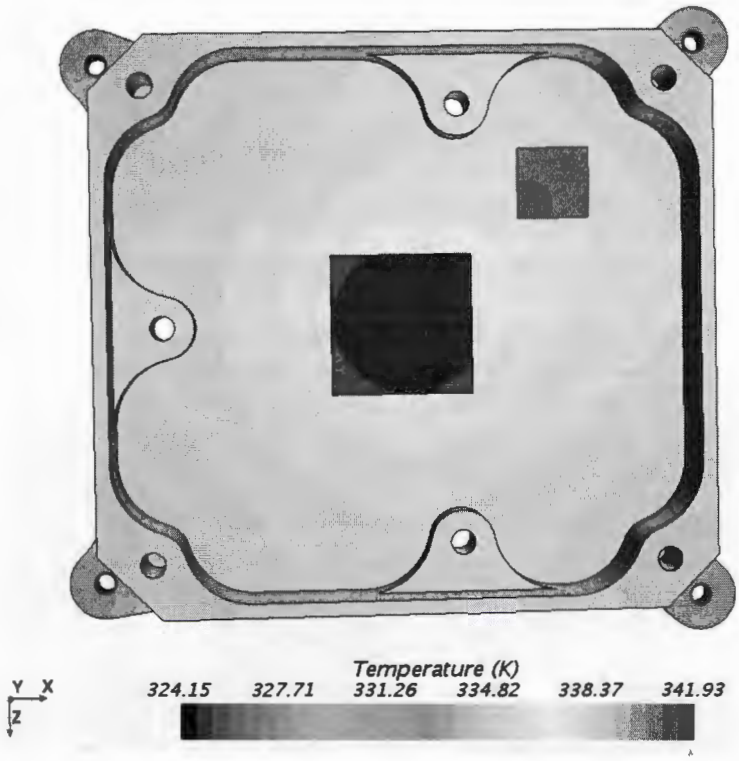

Figure 19: Temperature distribution in steady state thermal load

4 Conclusion

This project detailed the design for a software defined radio capable of transmitting and receiving images for use in communication between CubeSats. The first phase included the software design of the radio, including a modulator and demodulator with timing and phase error detection and recovery, implementation on an FPGA, and design of the mechanical packaging. Results of this phase yielded working simulations of the complete software design, working HDL code for implementation on an FPGA, and a fully machined metal packaging prototype.

The project will be continued in subsequent phases by students in the design course to create a working, packaged prototype for Harris Corporation. These phases will include custom design of a PCB, further development and testing of the software and user interface, and the final packaging.

References

[1] S.-J. Kang and H.-U. Oh, "On-orbit thermal design and validation of 1 u standardized cubesat of step cube lab," *International Journal of Aerospace Engineering*, vol. 2016, 2016.

[2] Xilinx, *Zynq-7000 All Programmable SoC Packaging and Pinout Product Specification*, 2018.

[3] I. Analog Devices, *AD9361 Data Sheet, Ref. F.*, 2017.

[4] G. E. V. Standard and A. Revision, "Nasa goddard space flight center," tech. rep., GSFC-STD-7000, 2005.

[2] PC/104 Specification Version 2.6. (2018). [ebook] PC/104 Embedded Consortium, pp.3, A-2, A-3, D-2. Available at: http://pc104.org/hardware-specifications/pc104/ [Accessed 28 Apr. 2018].

Appendix A: Additional Resources

This appendix contains several resources that were helpful in learning about the hardware and software tools used in implementing and testing this project.

"AD9361," AD9361 Datasheet and Product Info — Analog Devices. [Online]. Available: http://www.analog.com/en/products/rf-microwave/integrated-transceivers-transmitters-receivers/wideband-transceivers-ic/ad9361.html. [Accessed: May-2018].

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W. L. I. Agency, "Product Detail," USRP B210 USB Software Defined Radio (SDR) - Ettus Research. [Online]. Available: https://www.ettus.com/product/details/UB210-KIT. [Accessed: May-2018].

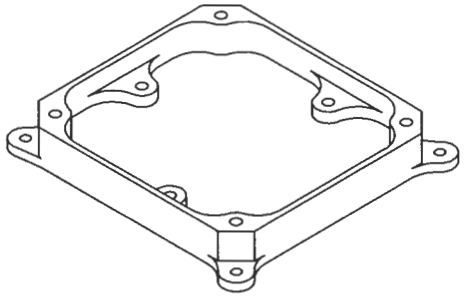
"Guided Tutorial Hardware Considerations," GNU Radio Wiki. [Online]. Available: https://wiki.gnuradio.org/index.php/Guided_Tutorial_Hardware_Considerations. [Accessed: May-2018].

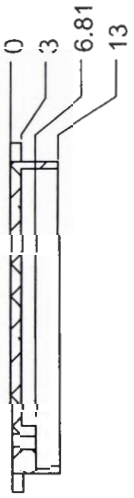
"SoCs with Hardware and Software Programmability," Zynq-7000 Programmable SoC. [Online]. Available: http://www.xilinx.com/products/silicon-devices/soc/zynq-7000.html. [Accessed: May-2018].

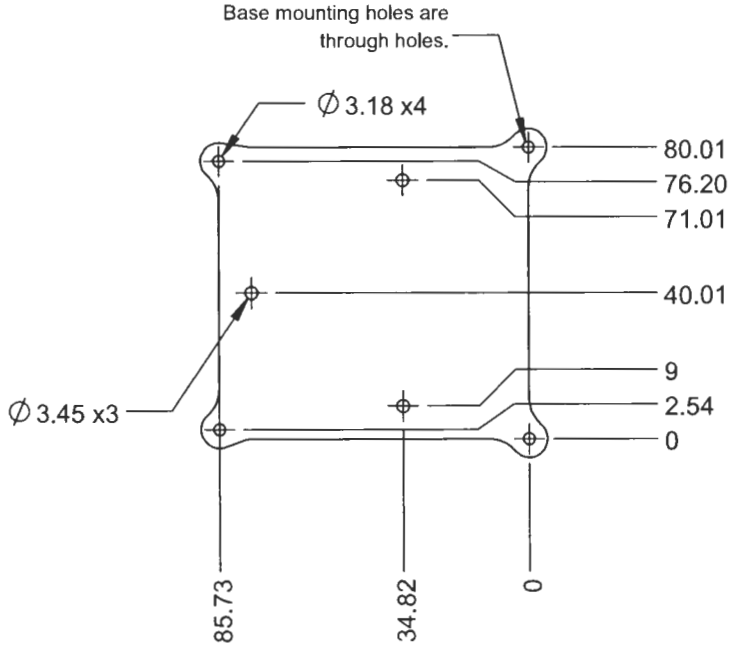
Appendix B: Mechanical Drawings and Calculations

Appendix Contents:

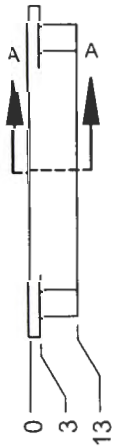
Drawings of Packaging Base - Metric
Drawings of Packaging Lid - Metric
Drawings of Packaging Base - Standard
Drawings of Packaging Lid - Standard
Rough Analysis and Bolt Analysis Calculations

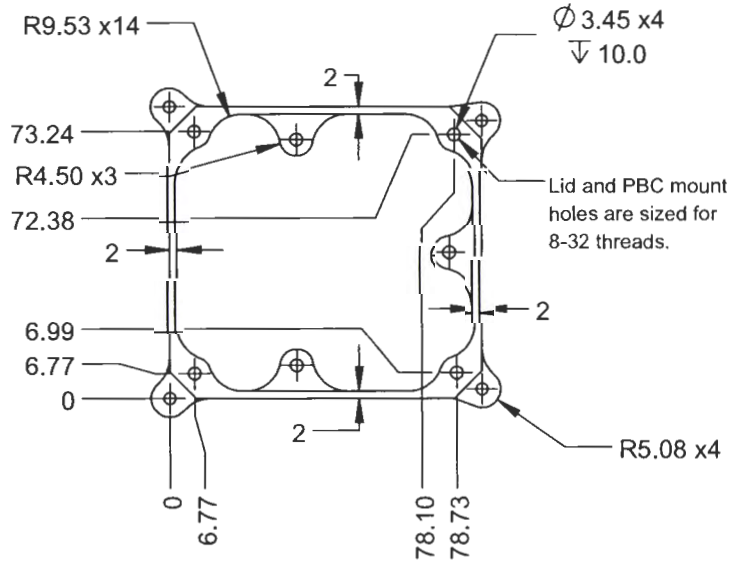




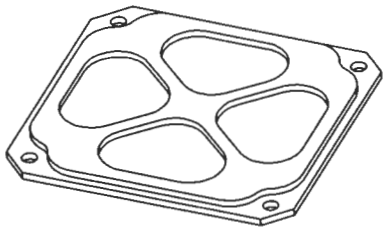


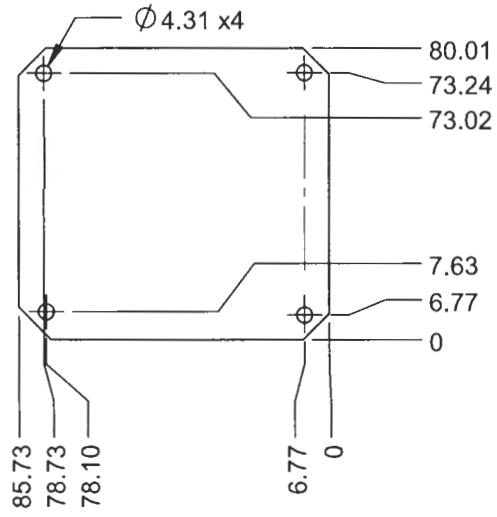
SECTION A-A

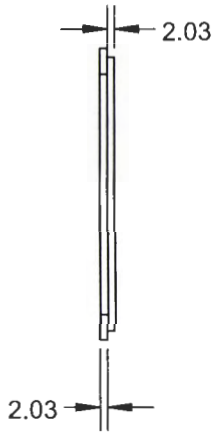


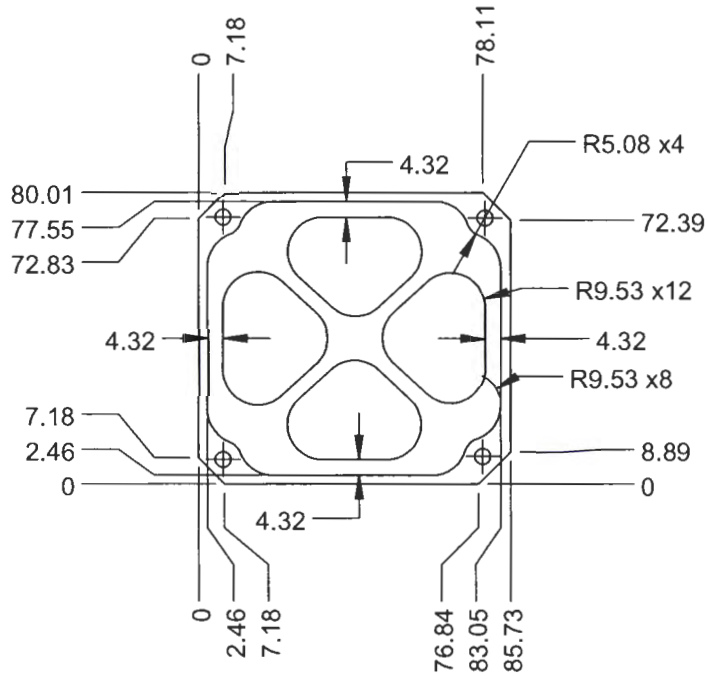


	Mechanical & Aerospace ENGINEERING UtahState University	**PROJECT** Harris Corporation CubeSat SDR
SPECIFICATIONS AND TOLERANCES UNLESS OTHERWISE NOTED DRAWING ARE CREATED IN ACCORDANCE TO ASME Y14.5-2009 DEFAULT DIMENSIONAL TOLERANCES: LINEAR DIMENSIONS [mm]: X±.5, X.X±.1, X.XX±.03, X.XXX±.005 ANGULAR DIMENSIONS [degrees]: X±3, X.X±.5, X.XX±.1 MINIMUM SURFACE FINISH: 25 micrometers		DRAFTED BY: Tyler Gardner
	PART/ASSEM NAME: Packaging Base	CHECKED BY: YOUR CHECKER
	PART/ASSEM NUMBER: HARRIS-01	APPROVED BY: YOUR SUPERVISOR
	MATERIAL: 2024-T3	DATE APPROVED: 4/17/2018
	FINISH: Machined	SHEET SCALE: 1:2 / SHEET NUMBER: 1 of 1

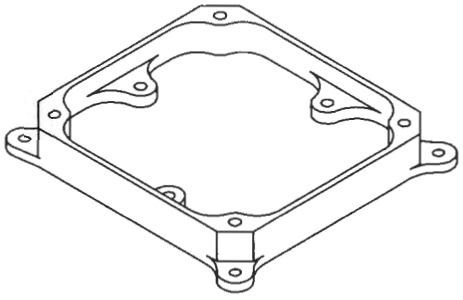


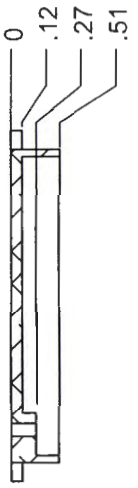






SPECIFICATIONS AND TOLERANCES UNLESS OTHERWISE NOTED DRAWING ARE CREATED IN ACCORDANCE TO ASME Y14.5-2009 DEFAULT DIMENSIONAL TOLERANCES: LINEAR DIMENSIONS [mm]: X±.5, X.X±.1, X.XX±.03, X.XXX±.005 ANGULAR DIMENSIONS [degrees]: X±3, X.X±.5, X.XX±.1 MINIMUM SURFACE FINISH: 25 micrometers	Mechanical & Aerospace ENGINEERING UtahState University	PROJECT Harris Corporation CubeSat SDR	
	PART/ASSEM NAME: Packaging Lid	DRAFTED BY: Tyler Gardner	
	PART/ASSEM NUMBER: HARRIS-02	CHECKED BY: YOUR CHECKER	
	MATERIAL: 2024-T3	APPROVED BY: YOUR SUPERVISOR	
	FINISH: Machined	DATE APPROVED: 4/17/2018	
		SHEET SCALE: 1:2	SHEET NUMBER: 1 of 1





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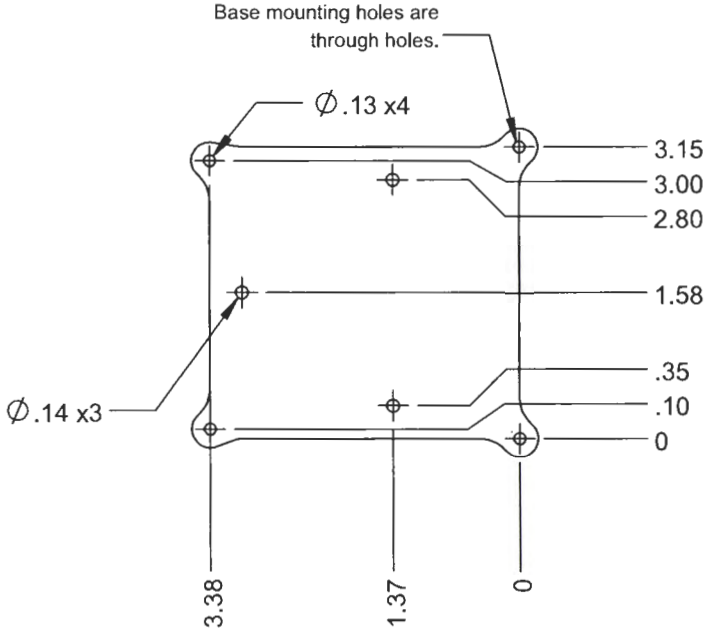

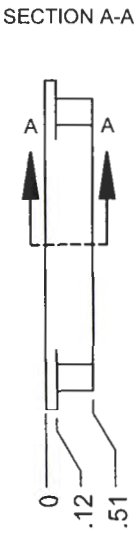

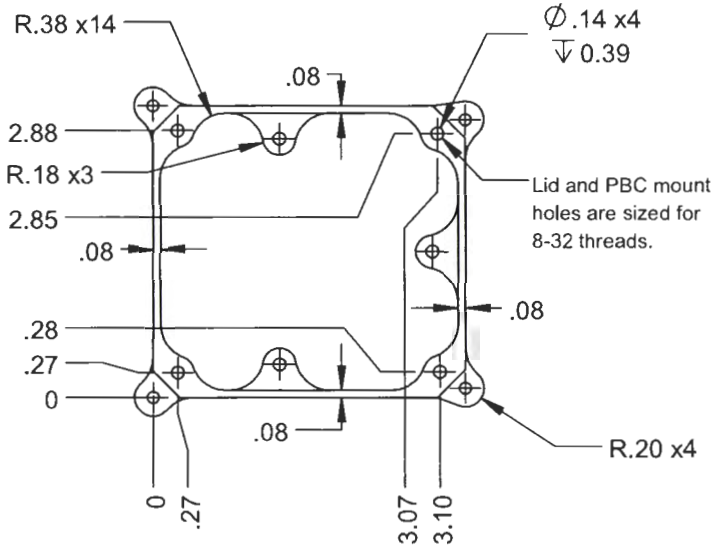

Mechanical & Aerospace ENGINEERING — UtahState University		PROJECT: Harris Corporation CubeSat SDR
		DRAFTED BY: Tyler Gardner
SPECIFICATIONS AND TOLERANCES	PART/ASSEM NAME: Packaging Base	CHECKED BY: YOUR CHECKER
UNLESS OTHERWISE NOTED DRAWING ARE CREATED IN ACCORDANCE TO ASME Y14.5-2009	PART/ASSEM NUMBER: HARRIS-01	APPROVED BY: YOUR SUPERVISOR
DEFAULT DIMENSIONAL TOLERANCES: LINEAR DIMENSIONS (in): X±.5, X.X±.1, X.XX±.03, X.XXX±.005 ANGULAR DIMENSIONS (degrees): X±3, X.X±.5, X.XX±.1 MINIMUM SURFACE FINISH: 25 micrometers	MATERIAL: 2024-T351	DATE APPROVED: 4/18/2018
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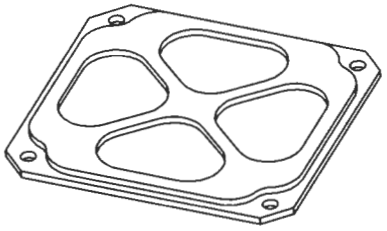
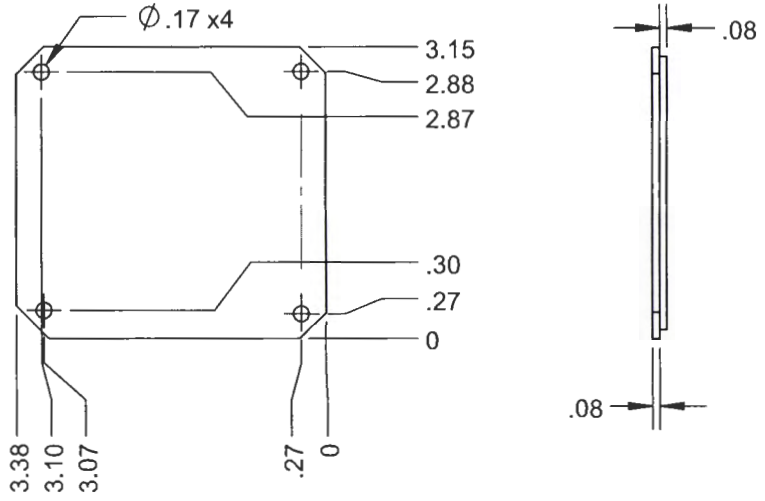
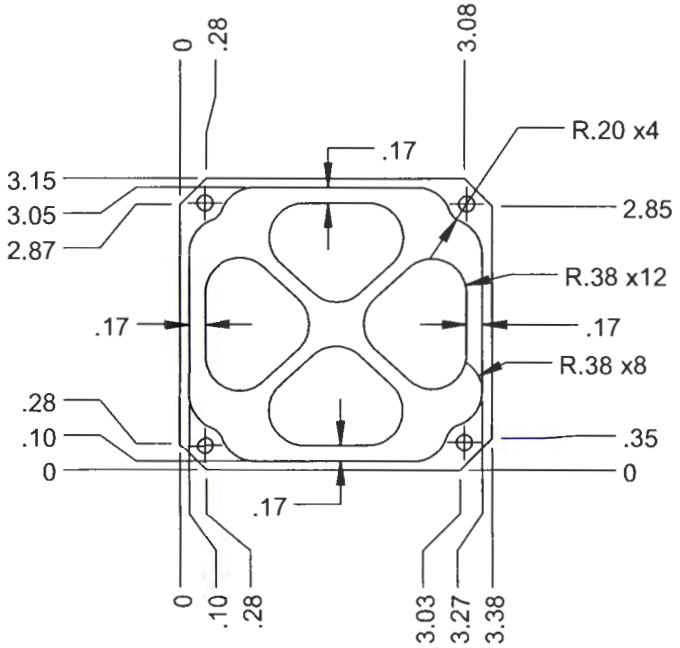


Dimensions in inches





Mechanical & Aerospace ENGINEERING — UtahState University		PROJECT: Harris Corporation CubeSat SDR	
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UNLESS OTHERWISE NOTED DRAWING ARE CREATED IN ACCORDANCE TO ASME Y14.5-2009	PART/ASSEM NUMBER: HARRIS-02	CHECKED BY: Arden Barnes	
DEFAULT DIMENSIONAL TOLERANCES: LINEAR DIMENSIONS [in]: X ±.5, X.X ±.1, X.XX ±.03, X.XXX ±.005 ANGULAR DIMENSIONS [degrees]: X ±3, X.X ±.5, X.XX ±.1 MINIMUM SURFACE FINISH: 25 micrometers	MATERIAL: 2024-T3	APPROVED BY: YOUR SUPERVISOR	
	FINISH: Machined	DATE APPROVED: 4/19/2018	
		SHEET SCALE: 1:2	SHEET NUMBER: 1 of 1

Material Properties:

2024 T4 Aluminum

$S_Y := 280MPa$ $S_U := 420MPa$ $S_F := 138MPa$

$E := 73.1GPa$ $G_{shear} := 28GPa$

$k := 121\frac{W}{m \cdot K}$ $C_{sh} := 0.875\frac{J}{g \cdot C}$ $rho := 0.00278\frac{kg}{cm^3} = 2.78 \times 10^{-6}\frac{kg}{mm^3}$

Properties found at:

Project Requirements and Specifications:

Physical Characteristics:

$m_{max} := 0.3kg$ $W_{max} := 100mm$ $L_{max} := 100mm$ $H_{max} := 50mm$

Structural Requirements:

Factors of Safety:

$FS_Y := 1.25$ $FS_U := 1.40$ $FS_{NOTEST} := 2.0$

Limit Loads:

$L_{DYN} := 58 \cdot g \cdot m_{max} = 170.636N$

Frequency Modes:

$FM1_{min} := 100Hz$

Ascent Pressure Decay:

$dP_{ascent} := 1.5\frac{psi}{s}$

Shock and Random Vibration:

See curves

Analysis:

Basic Analysis:

Tensile loading

$$A_Y := \frac{FS_Y \cdot L_{DYN}}{S_Y} = 0.762\,mm^2 \qquad Tmin_Y := \frac{A_Y}{7cm} = 0.011\,mm$$

$$A_U := \frac{FS_U \cdot L_{DYN}}{S_U} = 0.569\,mm^2 \qquad Tmin_U := \frac{A_U}{7cm} = 8.126 \times 10^{-3}\,mm$$

Bending Moment Loading

Assume center loading of equivalent dynamic load on bottom plate. This is the largest surface, and therefore most vulnerable to bending.

$b := 7cm \quad h := 2mm \quad Y := 1mm \qquad I := b \cdot h^3 = 560\,mm^4$

$$M := L_{DYN} \cdot \frac{7cm}{2} = 5.972 \cdot N \cdot m$$

$$I_Y := \frac{FS_Y \cdot M \cdot Y}{S_Y} = 26.662 \cdot mm^4 \qquad Tmin_Y := \left(\frac{I_Y}{b}\right)^{\frac{1}{3}} = 0.725\,mm$$

$$I_U := \frac{FS_U \cdot M \cdot Y}{S_U} = 19.907 \cdot mm^4 \qquad Tmin_U := \left(\frac{I_U}{b}\right)^{\frac{1}{3}} = 0.658\,mm$$

Bolt Analysis

Bolt size: 8-32

$d := 0.1640in \quad t_1 := 0.1in \quad t_2 := 0.3937in$

No washer so: $h := t_1 = 0.1 \cdot in$

From Table 8-7: $l := h + \frac{d}{2} = 0.182 \cdot in$

Min. bolt length: $L_{min} := h + 1.5 \cdot d = 0.346 \cdot in$

Round up: $L := \frac{3}{8}in = 0.375 \cdot in$ (smallest available from McMaster)

Threaded length: $L_T := L = 0.375 \cdot in$

Length of unthreaded portion: $l_d := L - L_T = 0\,mm$

Length of threaded portion to the effective "nut":

$l_t := l - l_d = 0.182 \cdot in$

From Table 8-2:

$A_t := 0.0140 in^2$

$A_d := \frac{\pi \cdot d^2}{4} = 0.021 \cdot in^2$

From inside front cover:

$E := 30 \cdot 10^6 psi$

Eqn 8-17

$k_b := \frac{A_d \cdot A_t \cdot E}{A_d \cdot l_t + A_t \cdot l_d} = 2.308 \times 10^6 \cdot \frac{lbf}{in}$

Eqn 8-22

$k_m := \frac{0.5774 \cdot \pi \cdot E \cdot d}{2 \ln\left[5 \frac{(0.5774 \cdot l + 0.5d)}{(0.5774 \cdot l + 2.5d)}\right]} = 7.479 \times 10^6 \cdot \frac{lbf}{in}$

Assumed load: $P_{total} := 45 lbf$ Number of bolts: $N := 4$

From table 8-9: $S_P := 120 ksi$

$C := \frac{k_b}{k_b + k_m} = 0.236$ $P := \frac{P_{total}}{N} = 11.25 \cdot lbf$

$F_i := 0.5 \cdot A_t \cdot S_P = 840 \cdot lbf$

Yielding FS (eqn 8-28):

$n_P := \frac{S_P \cdot A_t}{C \cdot P + F_i} = 1.994$

Overload FS (eqn 8-29):

$n_L := \frac{S_P \cdot A_t - F_i}{C \cdot P} = 316.643$

Joint separation FS: (eqn 8-30)

$n_0 := \frac{F_i}{P \cdot (1 - C)} = 97.707$

$F_{max} := S_P \cdot A_t = 1.68 \times 10^3 \cdot lbf$

$F_{min} := P \cdot (1 - C) = 8.597 \cdot lbf$

$F_{avg} := \frac{F_{max} + F_{min}}{2} = 844.299 \cdot lbf$

$K_{torque} := 0.2$ $T_{preload} := K_{torque} \cdot F_{avg} \cdot d = 27.693 \cdot lbf \cdot in$

Appendix C: Stress Distributions and Modal Shapes

Appendix Contents:

Acceleration Load Stress Distributions
Modal Shapes

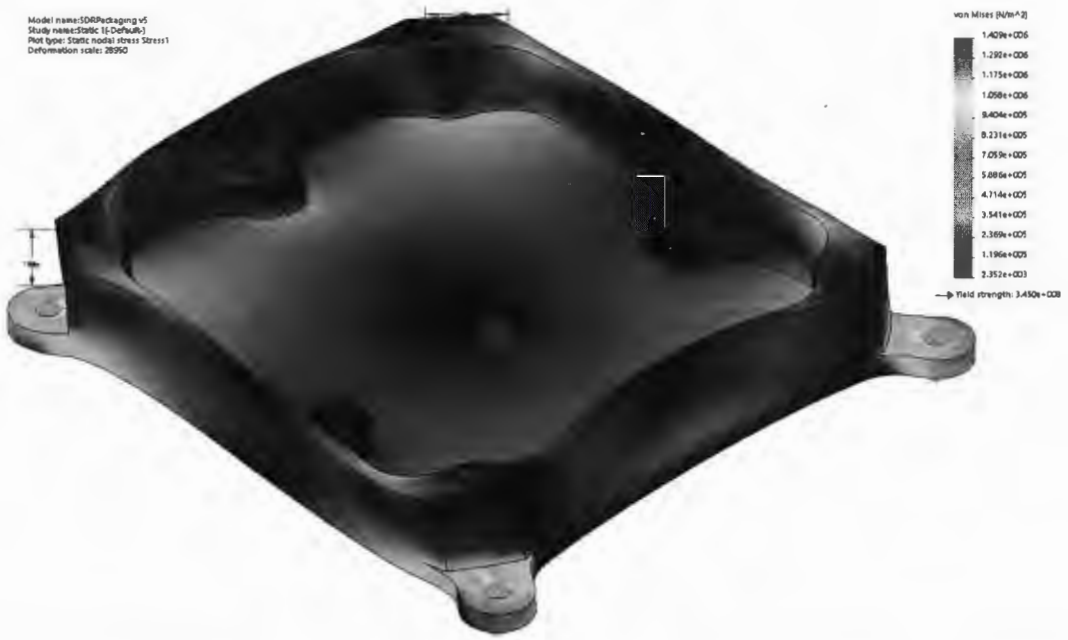


Figure 20: Stress distribution in the packaging base for a 60g acceleration load applied in the positive x direction

Figure 21: Stress distribution in the packaging base for a 60g acceleration load applied in the negative x direction

Figure 22: Stress distribution in the packaging base for a 60g acceleration load applied in the positive y direction

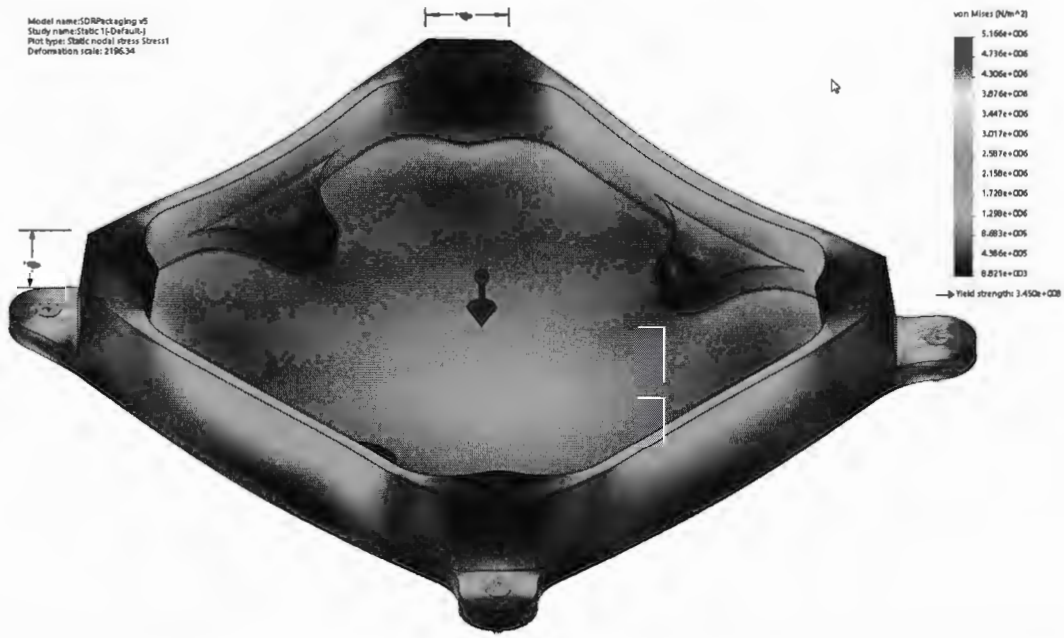


Figure 23: Stress distribution in the packaging base for a 60g acceleration load applied in the negative y direction

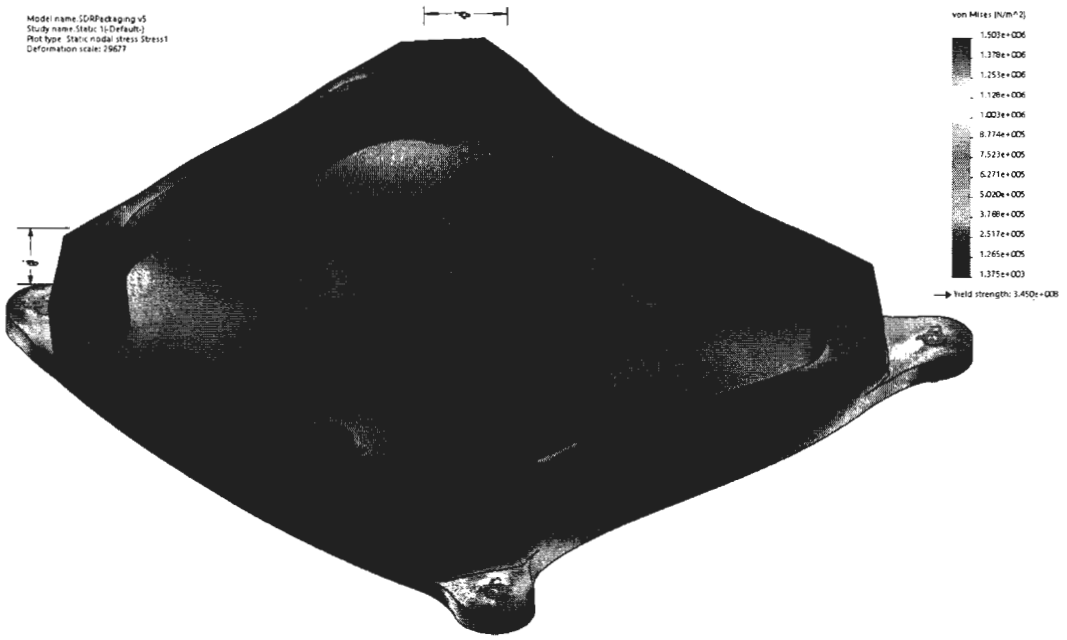


Figure 24: Stress distribution in the packaging base for a 60g acceleration load applied in the positive z direction

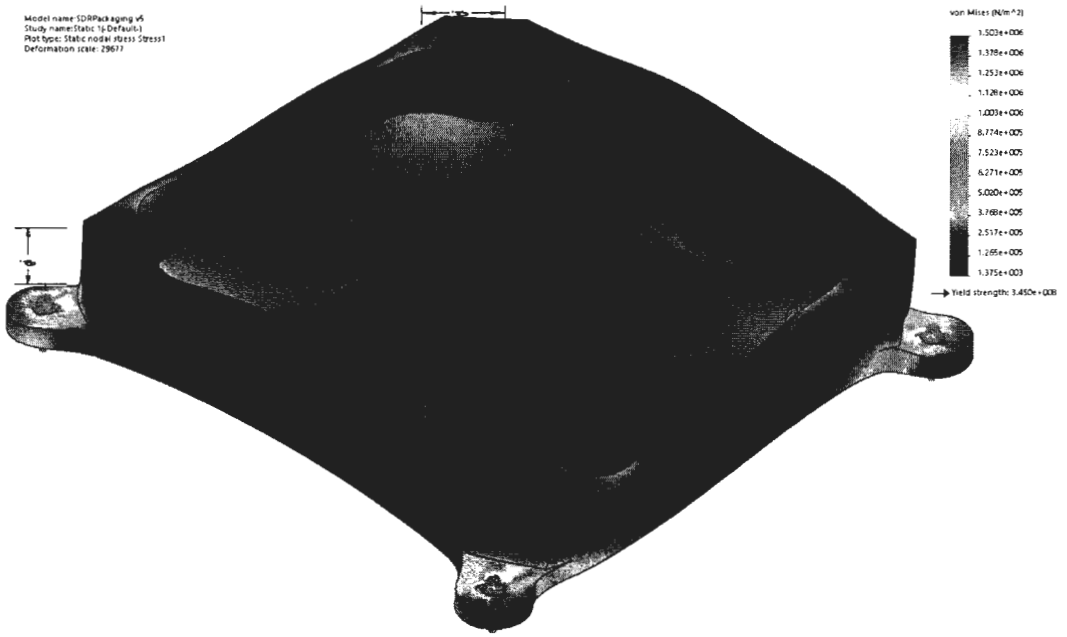


Figure 25: Stress distribution in the packaging base for a 60g acceleration load applied in the negative z direction

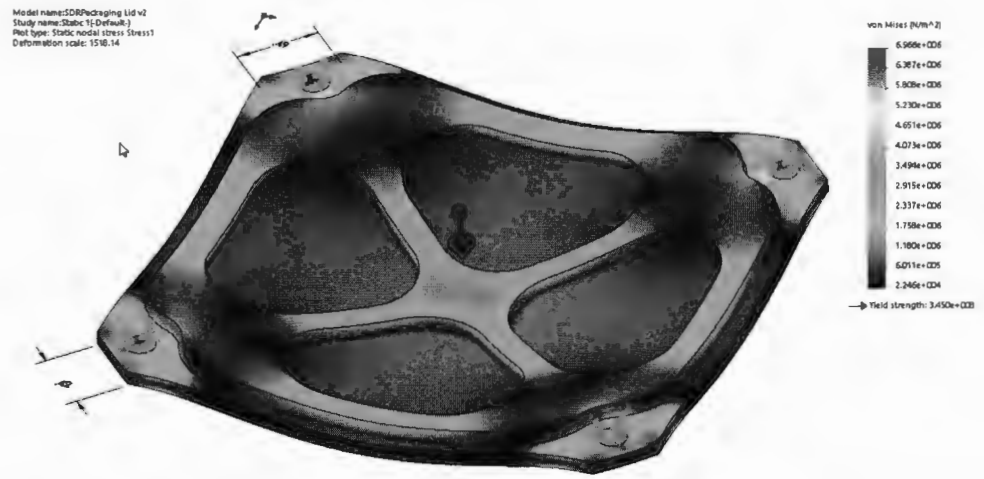


Figure 26: Stress distribution in the packaging lid for a 60g acceleration load applied in the positive z direction

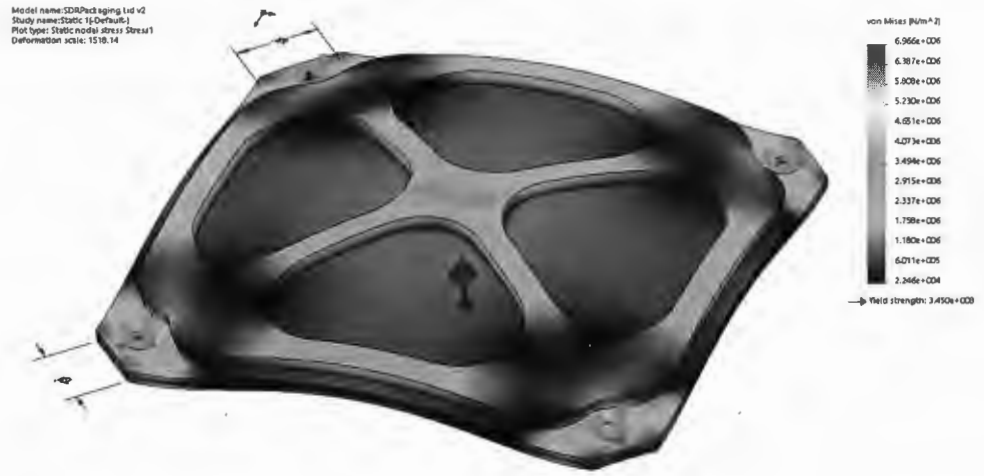


Figure 27: Stress distribution in the packaging lid for a 60g acceleration load applied in the negative z direction

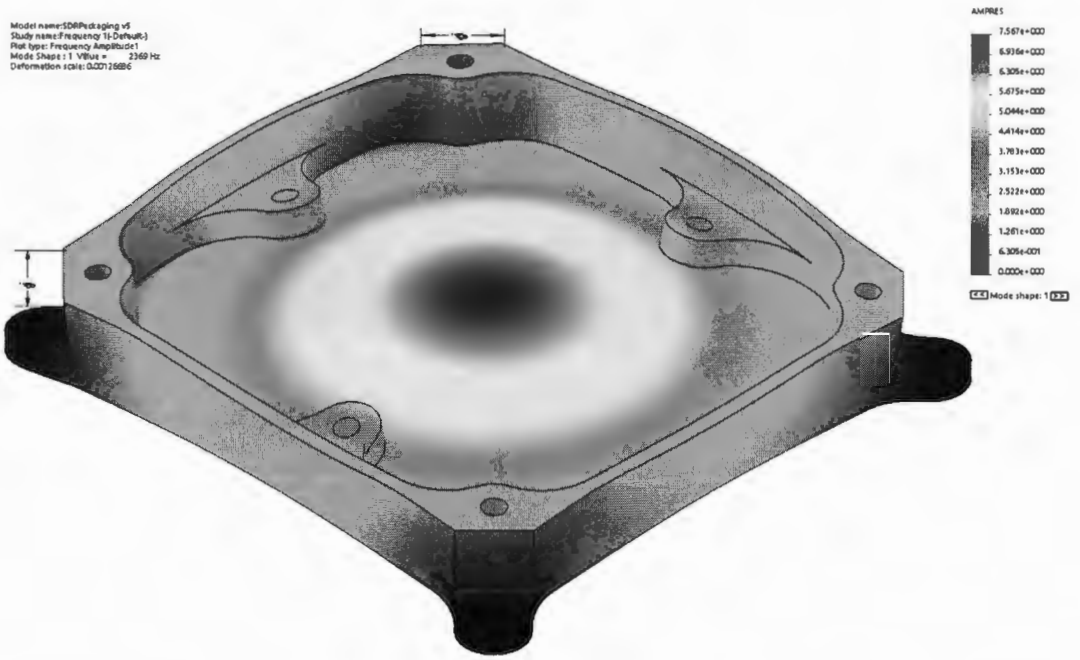


Figure 28: First modal shape for the packaging base

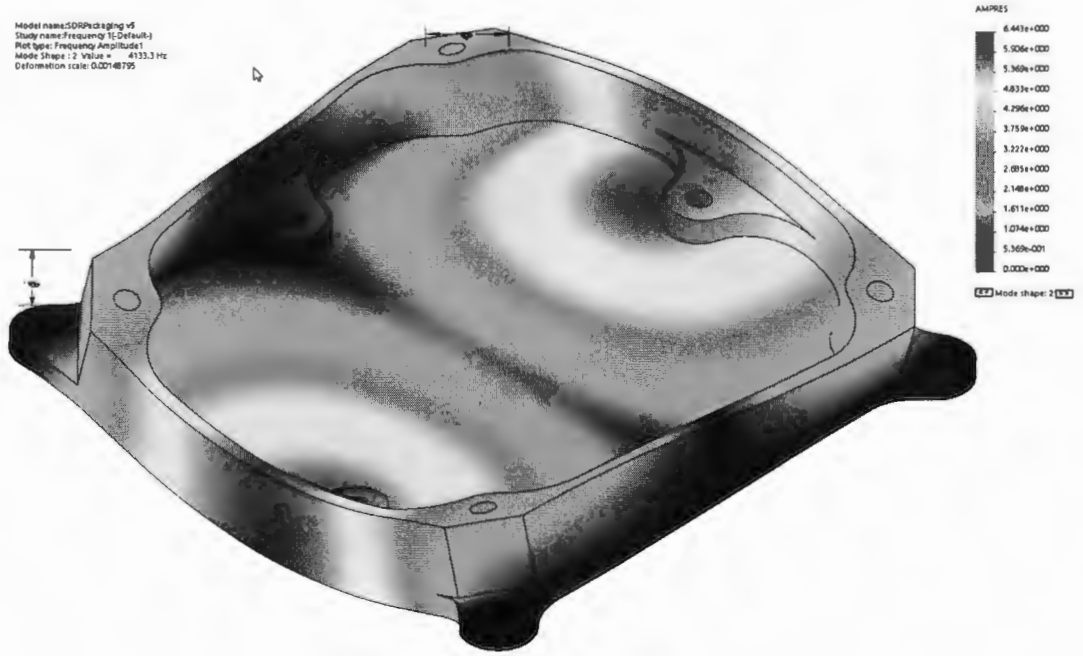


Figure 29: Second modal shape for the packaging base

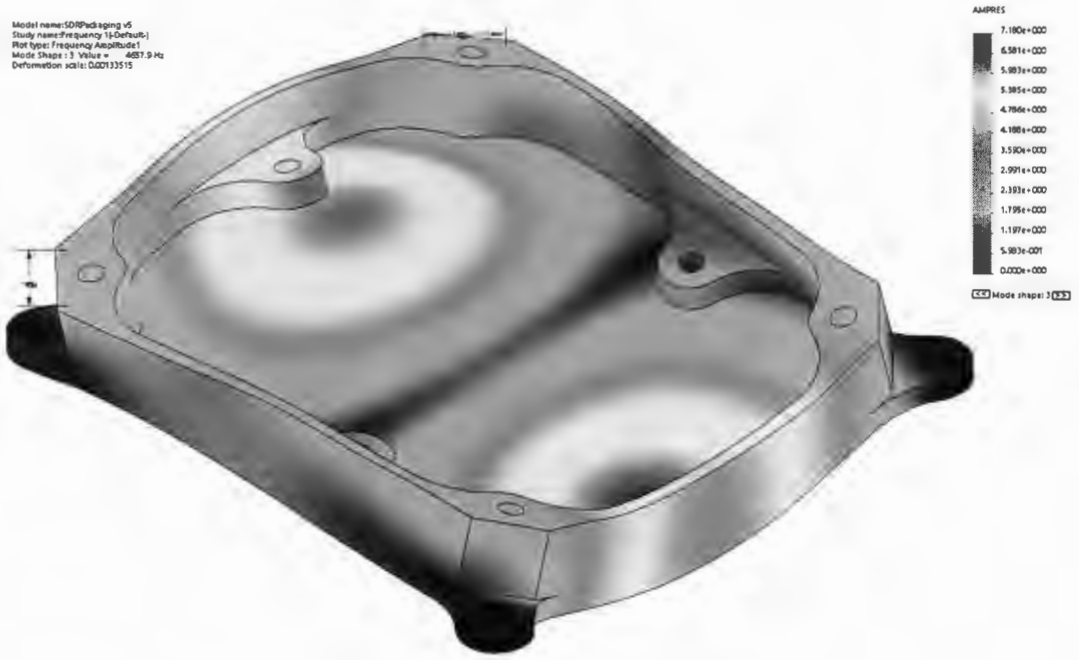


Figure 30: Third modal shape for the packaging base

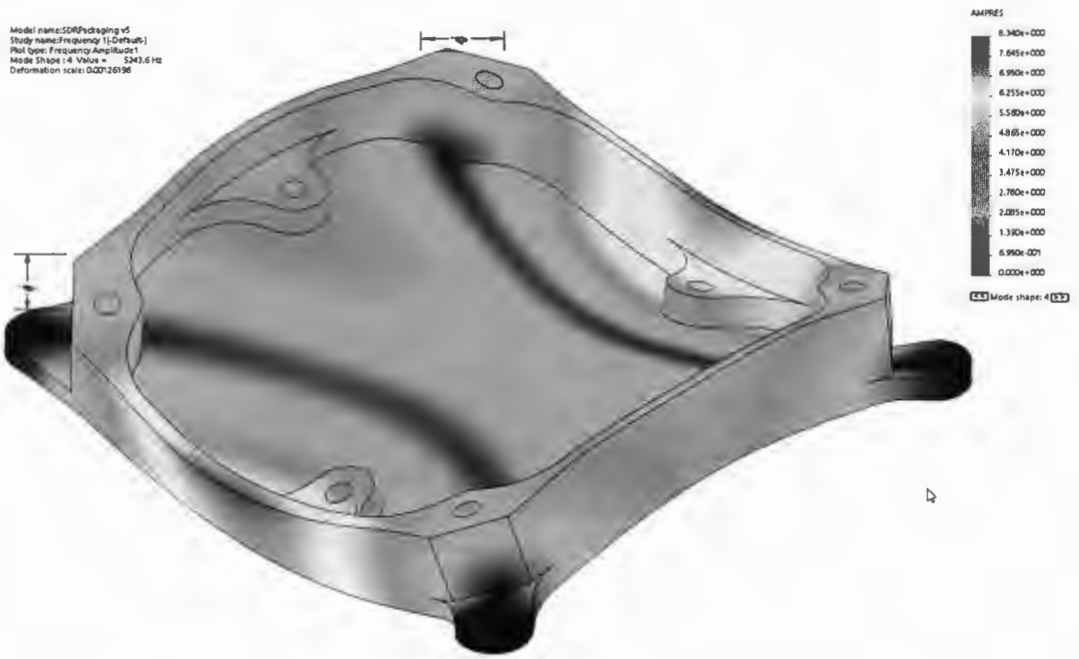


Figure 31: Fourth modal shape for the packaging base

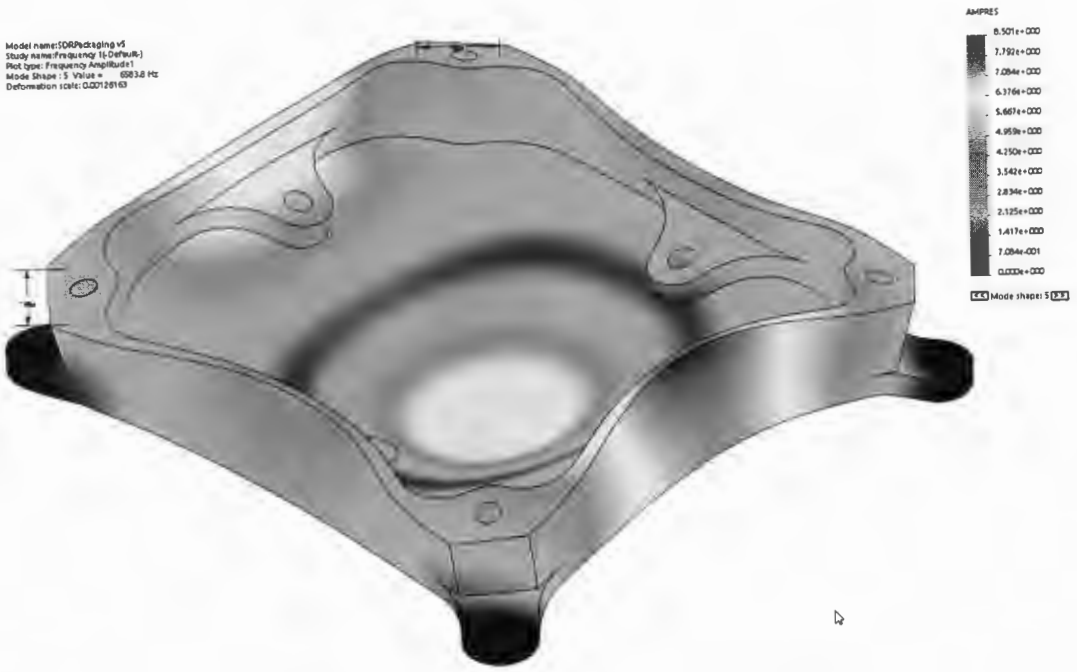


Figure 32: Fifth modal shape for the packaging base

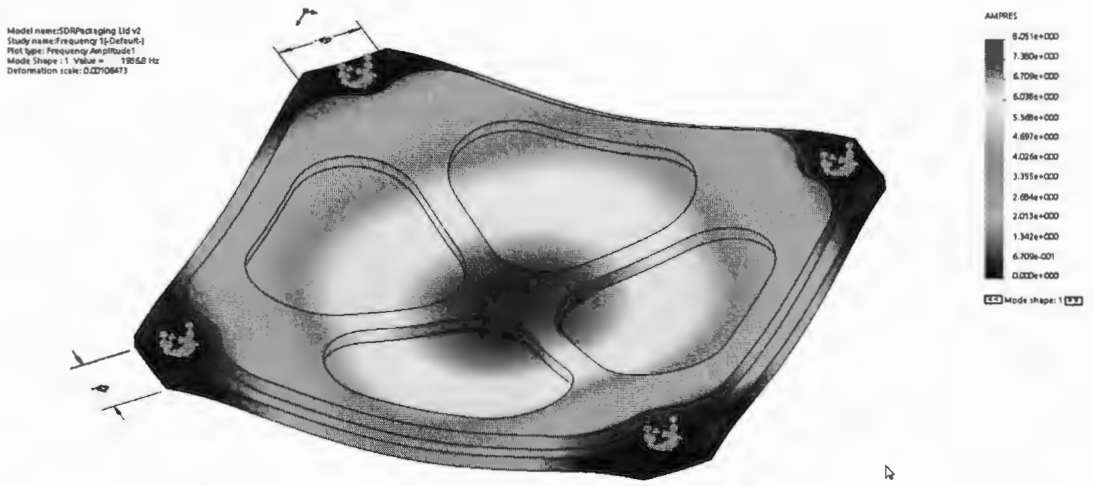


Figure 33: First modal shape for the packaging lid

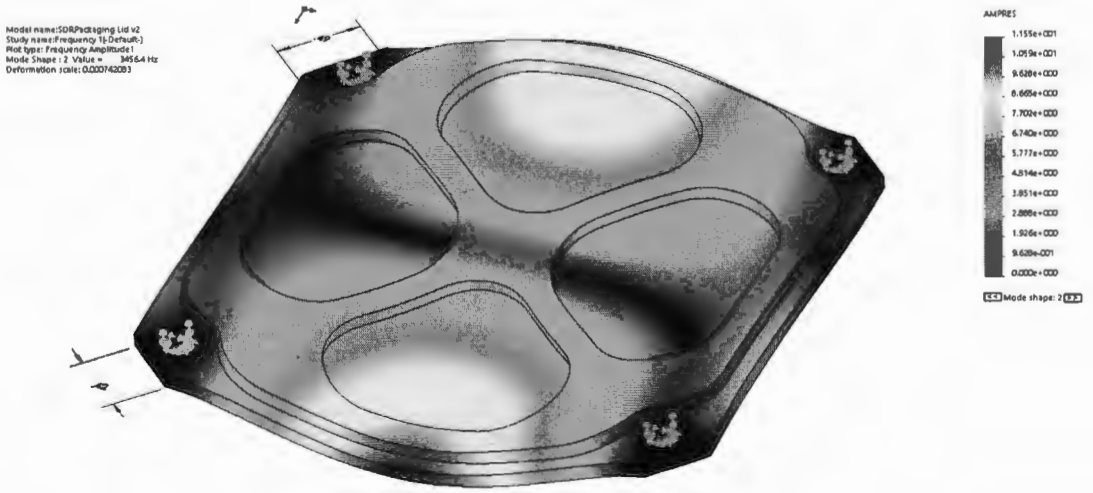


Figure 34: Second modal shape for the packaging lid

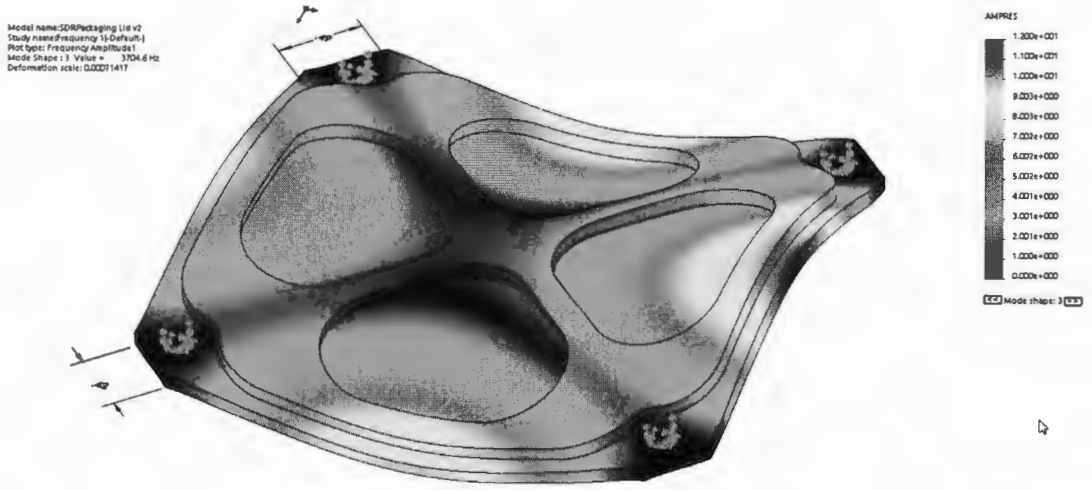


Figure 35: Third modal shape for the packaging lid

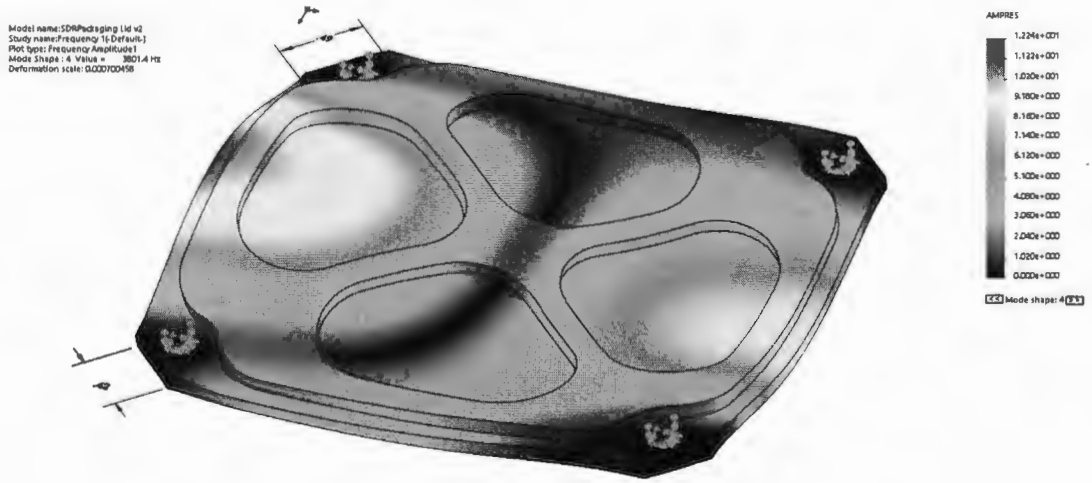


Figure 36: Fourth modal shape for the packaging lid

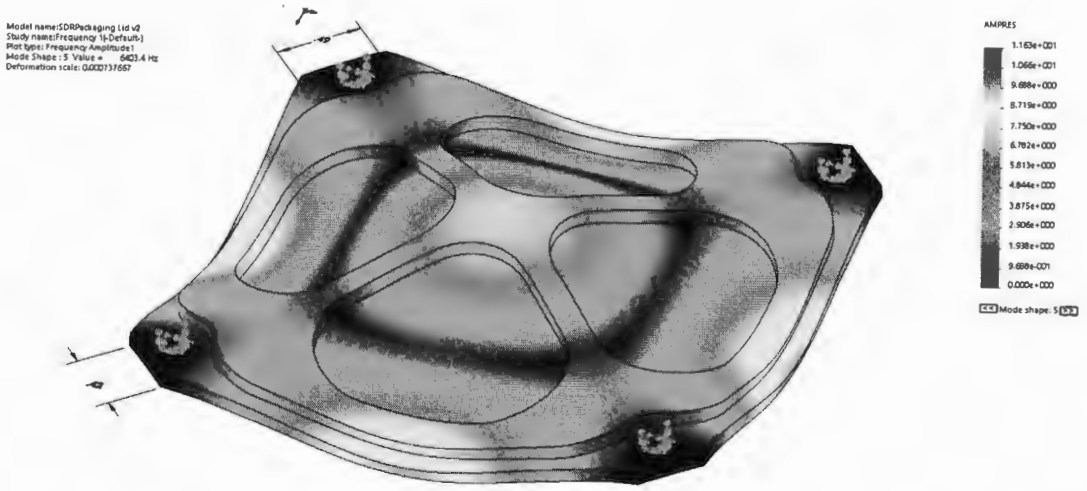


Figure 37: Fifth modal shape for the packaging lid

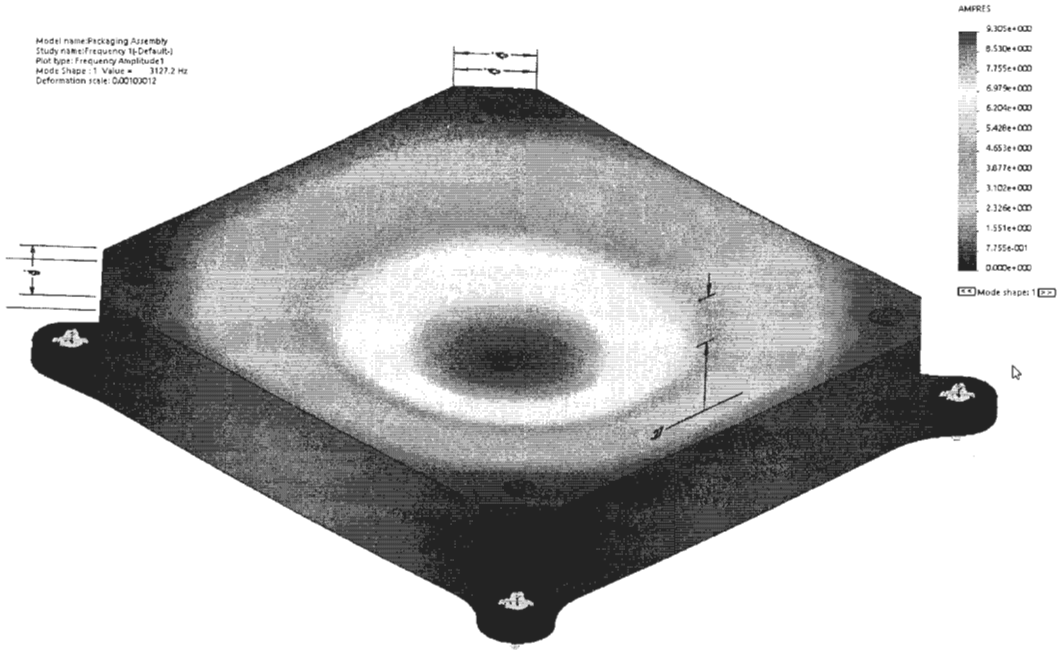


Figure 38: First modal shape for the packaging assembly

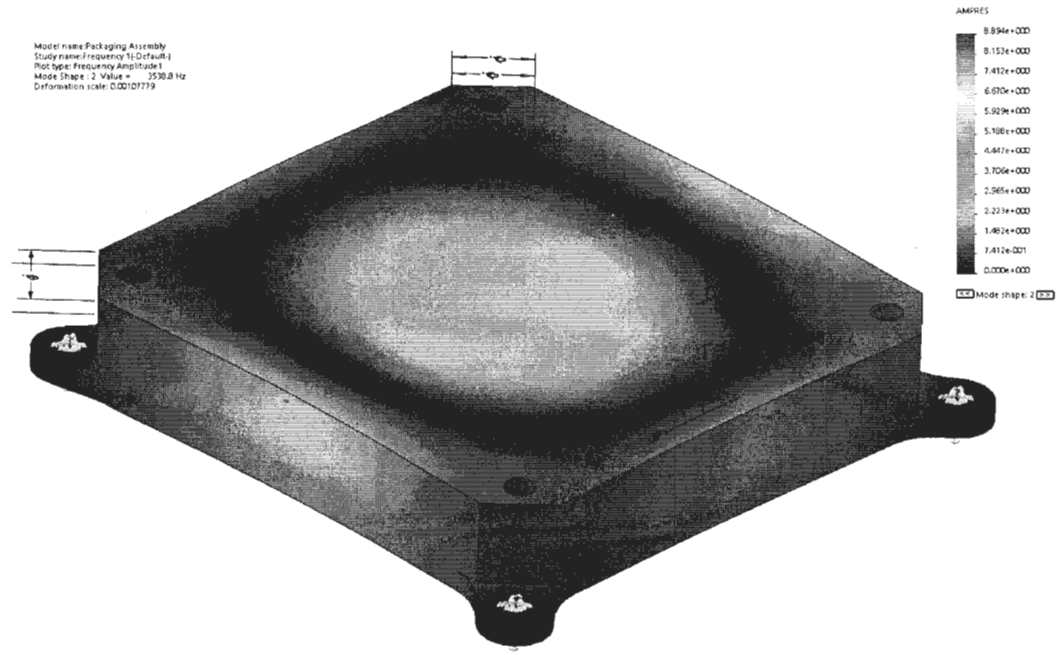


Figure 39: Second modal shape for the packaging assembly

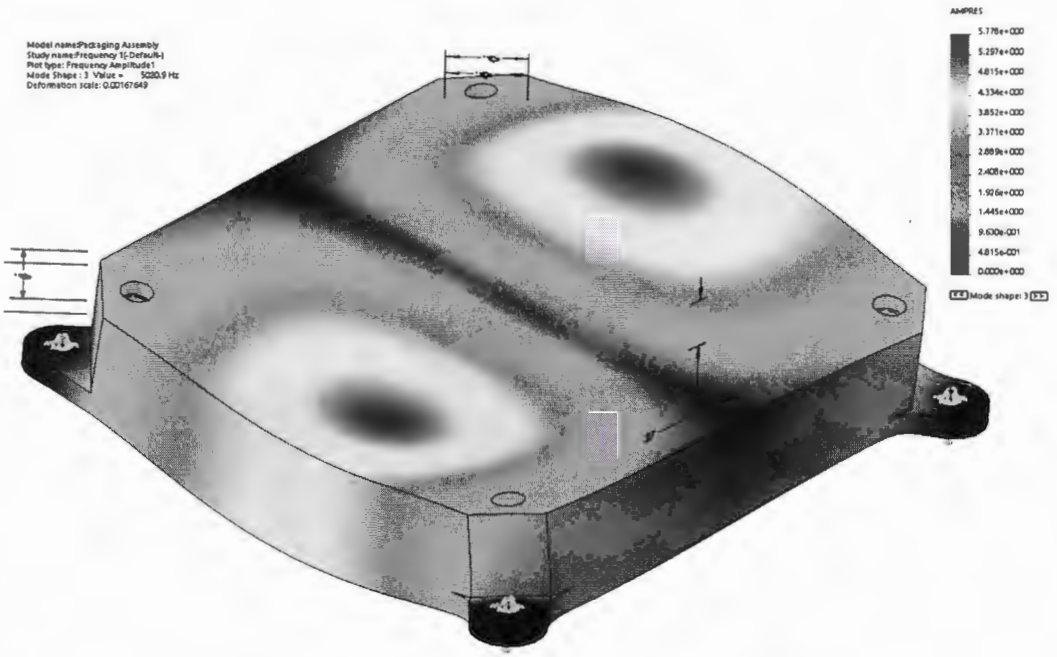


Figure 40: Third modal shape for the packaging assembly

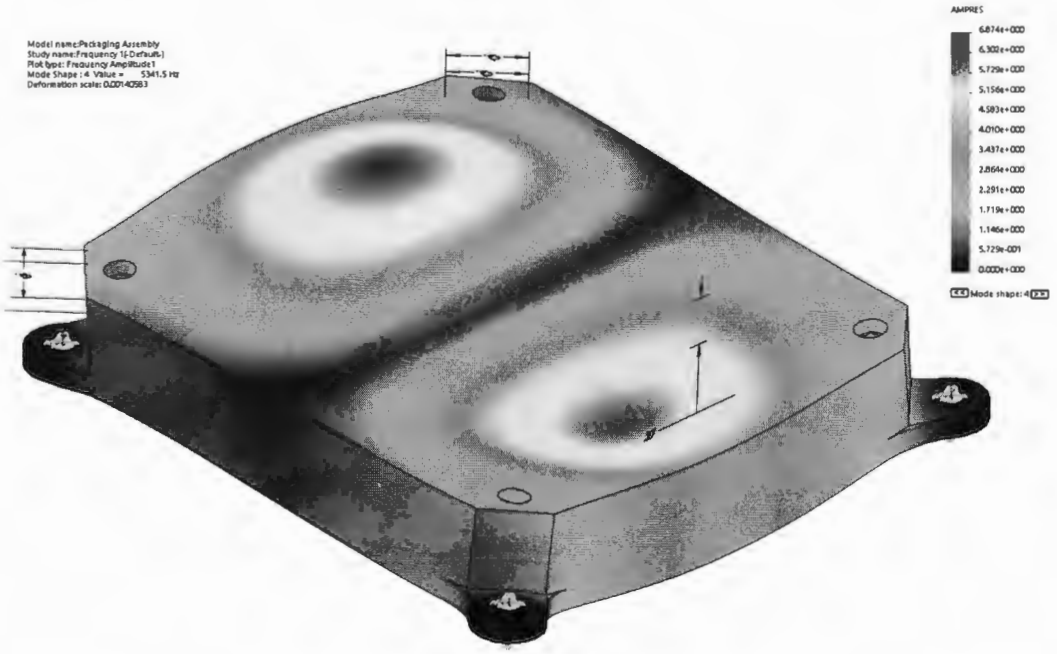


Figure 41: Fourth modal shape for the packaging assembly

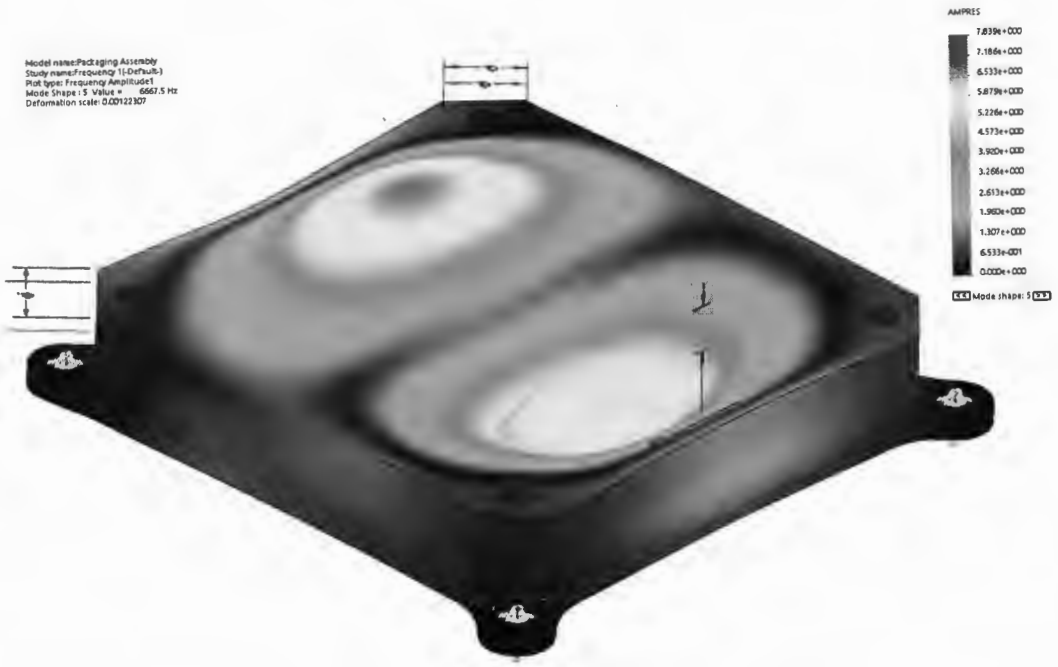


Figure 42: Fifth modal shape for the packaging assembly

Appendix D: GSFC-STD-7000A

Appendix Contents:

Relevant Sections from GSFC-STD-7000A

GSFC-STD-7000A
4/22/2013
Supersedes
GSFC-STD-7000

GENERAL ENVIRONMENTAL VERIFICATION STANDARD (GEVS)
For GSFC Flight Programs and Projects

Approved By:

Original Signed by:
Chief Engineer
Goddard Space Flight Center

Original Signed by:
Director of Applied Engineering and Technology
Goddard Space Flight Center

Original Signed by:
Director of Flight Projects
Goddard Space Flight Center

Original Signed by:
Director of Safety and Mission Assurance
Goddard Space Flight Center

NASA GODDARD SPACE FLIGHT CENTER
Greenbelt, Maryland 20771

Changes to

GENERAL ENVIRONMENTAL VERIFICATION STANDARD

Change No.	Date	Nature of Change
Baseline	April 2005	
A	4/22/2013	Major update - STS references removed; Reference to Office of Mission Success removed; Added definition of anomaly; Significant updates to the following sections: 1.13; 2.2.5; 2.4.1.2; 2.4.1.4.1; 2.4.2.2; 2.4.2.6; 2.4.4.1; 2.4.4.2; 2.6.2.4; Section 1.14 added; Section 2.5 rewritten; Section 2.7 rewritten CCR Number CCR-D-0071

wavelength of the lowest frequency of interest is recommended. It is recognized that this cannot be achieved in some facilities, particularly when noise levels are specified to frequencies as low as 25 Hz. In such cases, the microphones shall be located in positions so as to be affected as little as possible by surface effects.

The preferred method of preparing for an acoustic test is to preshape the spectrum of the acoustic field with a dummy test item. If no such item is readily available, it is possible to preshape the spectrum in an empty test area. In that case, however, a low-level test should be performed after the test item has been placed in the test area to permit final adjustments to the shape of the acoustic spectrum.

Acoustic testing may be performed in a reverberant chamber or may be performed as a direct-acoustic field (DAF) test in which the acoustic pressure field is generated by banks of speakers. The preferred method for performing acoustic testing on flight hardware is with a reverberant chamber test. Comparison of data from test articles subjected to both reverberant and current state-of-the art DAF testing showed that the pressure field and measured responses from DAF testing can differ significantly from a reverberant field test even if the control microphones are kept within the test tolerances specified in Section 1.13. Because of the non-uniformity that may exist in the acoustic field generated by DAF testing, care must be taken when performing this type of test to have sufficient instrumentation on the test article to prevent exceeding hardware capability as the test level is increased and have an adequate number of microphones in place during the test to monitor the pressure field generated near critical items. It should also be noted that variability in the acoustic field generated by a DAF test may result in under-testing as well as over-testing in specific frequency bands and all efforts should be made to map the acoustic field relative to acoustically sensitive hardware to ensure that an adequate test can be achieved.

b. Test Setup - The boundary conditions under which the hardware is supported during test shall duplicate those expected during flight. When that is not feasible, the test item shall be mounted in the test chamber in such a manner as to be isolated from all energy inputs on a soft suspension system (natural frequency less than 20 Hz) and a sufficient distance from chamber surfaces to minimize surface effects. During test, the test item should be in an operational configuration, both electrically and mechanically, representative of its configuration at lift-off.

c. Performance - Before and after the acoustic exposure, the payload shall be examined and functionally tested. During the test, performance shall be monitored in accordance with the verification specification.

2.4.2.3 Payload Random Vibration Tests - At the payload level of assembly, protoflight hardware shall, when practicable, be subjected to a random vibration test to verify its ability to survive the lift-off environment and also to provide a final workmanship vibration test. For small payloads (<454 kg or 1000 lb), the test is required; for larger payloads the need to perform a random vibration test shall be assessed on a case-by-case basis. Additional qualification tests may be required if expected environments are not enveloped by this test. The acoustic environment at lift-off is usually the primary source of random vibration; however, other sources of random vibration must be considered. The sources include transonic aerodynamic fluctuating pressures and the firing of retro/apogee motors.

a. Lift-Off Random Vibration - Protoflight hardware shall be subjected to a random vibration test to verify flightworthiness and workmanship. The test level shall represent the qualification level (flight limit level plus 3 dB).

The test is intended for payloads (spacecraft) of low to moderate weight and size. For small payloads, such as Pegasus-launched spacecraft, the test should cover the full 20-2000 Hz frequency range. In such cases, the project should assess and recommend a random vibration test, acoustic test, or both, depending on the payload. For larger ELV payloads, the test is not required unless there is a close-coupled, direct structural load path to the launch vehicle external skin. In that case, both lift-off and transonic random vibration must be considered.

The payload in its launch configuration shall be attached to a vibration fixture by use of a flight-type launch-vehicle adapter and attachment hardware. Vibration shall be applied at the base of the adapter in each of three orthogonal axes, one of which is parallel to the thrust axis. The excitation spectrum as measured by the control accelerometer(s) shall be equalized such that the acceleration spectral density is maintained within ±3 dB of the specified level at all frequencies within the test range and the overall RMS level is within ±10% of the specified level.

Prior to the payload test, a survey of the test fixture/exciter combination shall be performed to evaluate the fixture dynamics, the proposed choice of control accelerometer locations, and the control strategy. If a mechanical test model of the payload is available it should be included in the survey to evaluate the need for limiting.

If a random vibration test is not performed at the payload level of assembly, the feasibility of doing the test at the next lower level of assembly shall be assessed.

b. Performance - Before and after each vibration test, the payload shall be examined and functionally tested. During the tests, performance shall be monitored in accordance with the verification specification.

2.4.2.4 Subsystem/Instrument Vibroacoustic Tests - If subsystems are expected to be significantly excited by structureborne random vibration, a random vibration test shall be performed. Specific test levels are determined on a case-by-case basis. The levels shall be equal to the qualification level as predicted at the location where the input will be controlled. Subsystem acoustic tests may also be required if the subsystem is judged to be sensitive to this environment or if it is necessary to meet delivery specifications. A random vibration test is generally required for instruments.

2.4.2.5 Component/Unit Vibroacoustic Tests - As a screen for design and workmanship defects, components/units shall be subjected to a random vibration test along each of three mutually perpendicular axes. In addition, when components are particularly sensitive to the acoustic environment, an acoustic test shall be considered.

a. Random Vibration - The test item is subjected to random vibration along each of three mutually perpendicular axes for one minute each. When possible, the component random vibration spectrum shall be based on levels measured at the component mounting locations during previous subsystem or payload testing. When such measurements are not available, the levels shall be based on statistically estimated responses of similar components on similar structures or on analysis of the payload. Actual measurements shall then be used if and when they become available. In the absence of any knowledge of the expected level, the generalized vibration test specification of Table 2.4-3 may be used.

As a minimum, all components shall be subjected to the levels of Table 2.4-4, which represent a workmanship screening test. The minimum workmanship test levels are primarily intended for use on electrical, electronic, and electromechanical hardware.

The test item shall be attached to the test equipment by a rigid fixture. The mounting shall simulate, insofar as practicable, the actual mounting of the item in the payload with particular attention given to duplicating the mounting contact area. In mating the test item to the fixture, a flight-type mounting (including vibration isolators or kinematic mounts, if part of the design) and fasteners should be used. Normally sealed items shall be pressurized during test to their prelaunch pressure.

For components mounted on isolators, flexures, or other highly compliant mounting structure, adequate workmanship testing may not be achieved in the flight configuration. In this case, it may be necessary to test the component hard-mounted to the shaker to achieve sufficient input levels to verify workmanship. The hard-mounted test would be run in addition to testing the component with flight-like mounting hardware. The component must be assessed for the hard-mounted test configuration to ensure that the hardware can survive the test without damage.

In cases where significant changes in strength, stiffness, or applied load result from variations in internal and external pressure during the launch phase, a special test shall be considered to cover those effects.

Prior to the test, a survey of the test fixture/exciter combination shall be performed to evaluate the fixture dynamics, the proposed choice of control accelerometer locations, and the control strategy. The evaluation shall include consideration of cross-axis responses. If a mechanical test or engineering model of the test article is available it should be included in the survey.

For very large components the random vibration tests may have to be supplemented or replaced by an acoustic test if the vibration test levels are insufficient to excite internal hardware. If neither the acoustic nor vibration excitation is sufficient to provide an adequate workmanship test, a screening program should be initiated at lower levels of assembly; down to the board level, if necessary. The need for the screening program must be evaluated by the project. The evaluation is based on mission reliability requirements and hardware criticality, as well as budgetary and schedule constraints.

If testing is performed below the component level of assembly, the workmanship test levels of Table 2.4-4 can be used as a starting point for test tailoring. The intent of testing at this level of assembly is to uncover design and workmanship flaws. The test input levels do not represent expected environments, but are intended to induce failure in weak parts and to expose workmanship errors. The susceptibility of the test item to vibration must be evaluated and the test level tailored so as not to induce unnecessary failures.

If the test levels create conditions that exceed appropriate design safety margins or cause unrealistic modes of failure, the input spectrum can be notched below the minimum workmanship level. This can be accomplished when flight or test responses at the higher level of assembly are known or when appropriate force limits have been calculated.

b. Acoustic Test - If a component-level acoustic test is required, the test set-up and control shall be in accordance with the requirements for payload testing.

c. Performance - Before and after test exposure, the test item shall be examined and functionally tested. During the test, performance shall be monitored in accordance with the verification specification.

2.4.2.6 Acceptance Requirements - Vibroacoustic testing for the acceptance of previously qualified hardware shall be conducted at flight limit levels using the same duration as recommended for protoflight hardware. As a minimum, the acoustic test level shall be 138 dB, and the random vibration levels shall represent the workmanship test levels.

The payload is subjected to an acoustic test and/or a random vibration test in three axes. Components shall be subjected to random vibration tests in the three axes. Additional vibroacoustic tests at subsystem/instrument and component levels of assembly are performed in accordance with the environmental verification plan or as required for delivery.

Hardware that has beryllium, composite (including metal matrix), ceramic, or bonded joints in the structural load path and whose strength margins are driven by vibro-acoustic loading shall be tested to protoflight levels for random and/or acoustic testing even if the design has been previously qualified on a valid prototype or protoflight unit. Protoflight vibro-acoustic testing ensures that structure whose strength is workmanship or fabrication dependent is adequately screened to preclude failure at higher levels of assembly. Protoflight testing should be performed at the lowest level of assembly practical for the hardware.

During the test, performance shall be monitored in accordance with the verification specification.

Table 2.4-3
Generalized Random Vibration Test Levels
Components (ELV)
22.7-kg (50-lb) or less

Frequency (Hz)	ASD Level (g^2/Hz)	
	Qualification	Acceptance
20	0.026	0.013
20-50	+6 dB/oct	+6 dB/oct
50-800	0.16	0.08
800-2000	-6 dB/oct	-6 dB/oct
2000	0.026	0.013
Overall	14.1 G_{rms}	10.0 G_{rms}

The acceleration spectral density level may be reduced for components weighing more than 22.7-kg (50 lb) according to:

	Weight in kg	Weight in lb	
dB reduction	= 10 log(W/22.7)	10 log(W/50)	
$ASD_{(50\text{-}800\ Hz)}$	= 0.16•(22.7/W)	0.16•(50/W)	for protoflight
$ASD_{(50\text{-}800\ Hz)}$	= 0.08•(22.7/W)	0.08•(50/W)	for acceptance

Where W = component weight.

The slopes shall be maintained at + and - 6dB/oct for components weighing up to 59-kg (130-lb). Above that weight, the slopes shall be adjusted to maintain an ASD level of 0.01 g^2/Hz at 20 and 2000 Hz.

For components weighing over 182-kg (400-lb), the test specification will be maintained at the level for 182-kg (400 pounds).

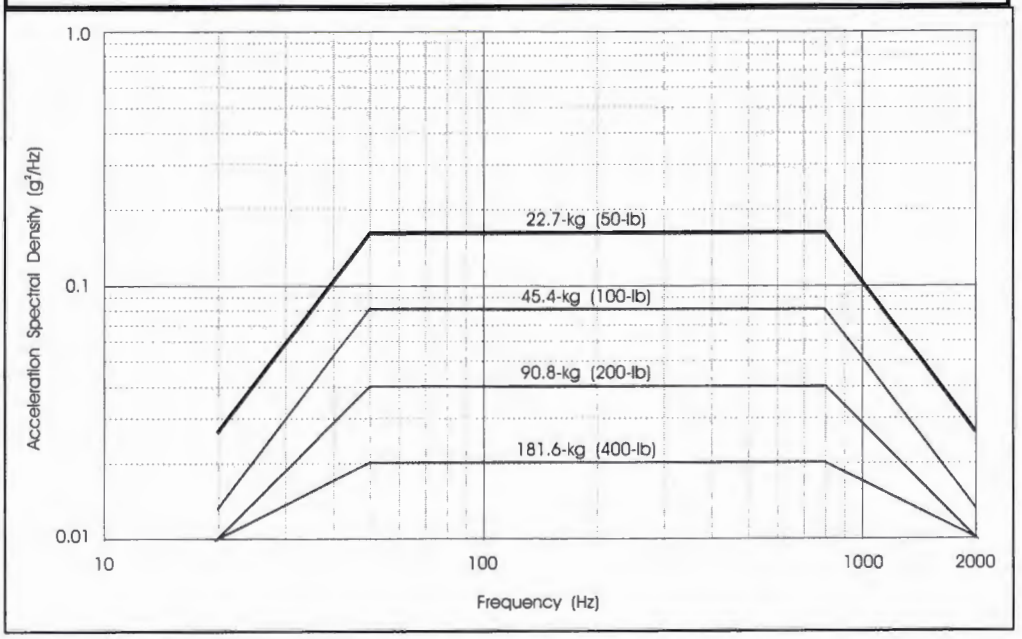


Table 2.4-4
Component Minimum Workmanship
Random Vibration Test Levels
45.4-kg (100-lb) or less

Frequency (Hz)	ASD Level (g^2/Hz)
20	0.01
20-80	+3 dB/oct
80-500	0.04
500-2000	-3 dB/oct
2000	0.01
Overall	6.8 g_{rms}

The plateau acceleration spectral density level (ASD) may be reduced for components weighing between 45.4 and 182 kg, or 100 and 400 pounds according to the component weight (W) up to a maximum of 6 dB as follows:

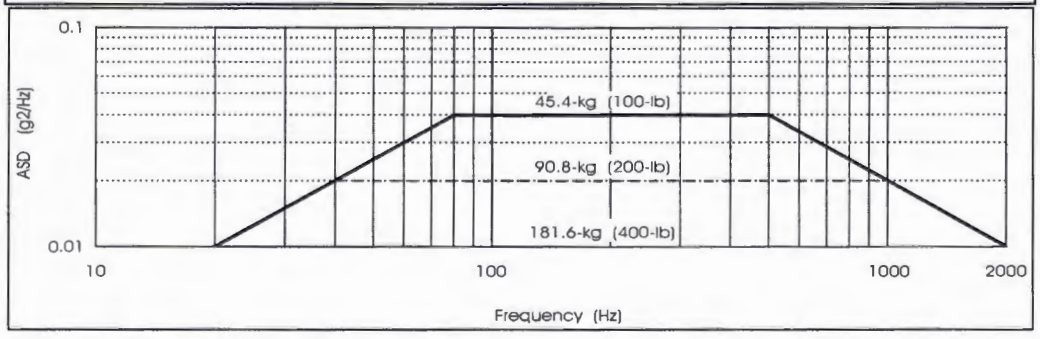
	Weight in kg	Weight in lb
dB reduction	= 10 log(W/45.4)	10 log(W/100)
$ASD_{(plateau)}$ level	= 0.04•(45.4/W)	0.04•(100/W)

The sloped portions of the spectrum shall be maintained at plus and minus 3 dB/oct. Therefore, the lower and upper break points, or frequencies at the ends of the plateau become:

F_L = 80 (45.4/W) [kg] = 80 (100/W) [lb] F_L = frequency break point low end of plateau

F_H = 500 (W/45.4) [kg] = 500 (W/100) [lb] F_H = frequency break point high end of plateau

The test spectrum shall not go below 0.01 g^2/Hz. For components whose weight is greater than 182-kg or 400 pounds, the workmanship test spectrum is 0.01 g^2/Hz from 20 to 2000 Hz with an overall level of 4.4 g_{rms}.



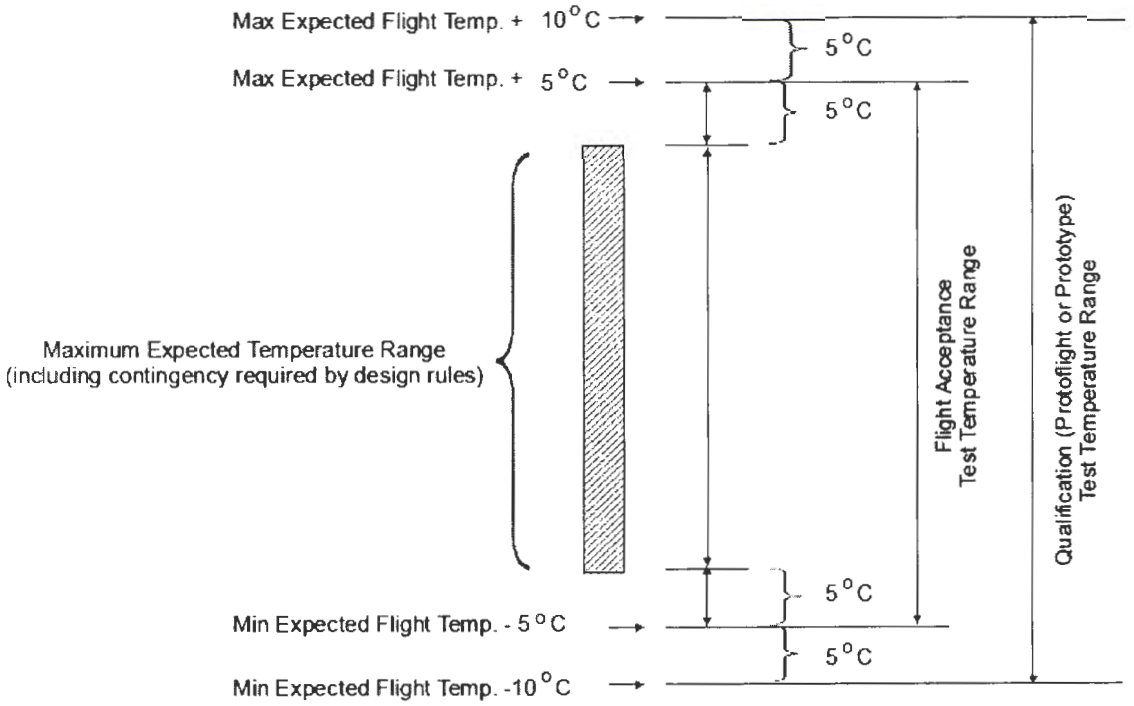


Figure 2.6-2 Qualification (Protoflight or Prototype) and Flight Acceptance Thermal-Vacuum Temperatures

Appendix E: PC/104 Specification

Appendix Contents:

Relevant Sections from PC/104 Specification

PC/104 Embedded Consortium

www.pc104.org

PC/104 Specification

Version 2.6

October 13, 2008

Please Note

This specification is subject to change without notice. While every effort has been made to ensure the accuracy of the material contained within this document, the PC/104 Embedded Consortium shall under no circumstances be liable for incidental or consequential damages or related expenses resulting from the use of this specification. If errors are found, please notify the PC/104 Embedded Consortium.

REVISION HISTORY

Version 1.0, March 1992 - Initial release.

Version 2.1, July 1994 - Revised specification incorporating changes to conform with IEEE P996.1 draft version D1.00:

a. Changed bus options. Eliminated the "option 2" configurations having right-angle P1 and P2 connectors. Created new "option 2" configurations similar to "option 1," but without the stackthrough pins. Added a statement indicating that a P2 connector may be included on 8-bit modules, if desired.
b. Added two additional mounting holes to 8-bit bus versions, making the mounting hole patterns of both 8- and 16-bit modules identical.
c. Added an I/O connector region along the bus edge of the module.
d. Increased widths of I/O mating-connector regions from 0.4" to 0.5".
e. Changed lengths of I/O mating-connector regions so that their edges align with the outer edges of the annular rings of adjacent mounting holes.
f. Reduced the bus drive requirement on the signals that had been specified at 6 mA to 4 mA.
g. Added specification of module power requirements.
h. In Appendix C, Section 3, changed minimum value of pullup resistance on shared interrupt line from 10K to 15K ohms.
i. Added a section defining levels of PC/104 conformance.

Version 2.2, September 1994

a. Added correction sheet showing revised schematic for Appendix C.

Version 2.3, June 1996

a. Incorporated correction to Appendix C schematic.
b. Changed P2 connector Pin 1 designation in 16-bit module dimension drawings.
c. Added metric dimensions, including metric versions of module dimension drawings.
d. Minor formatting changes.

Version 2.4, August 2001

a. Added Appendix D Connector Specifications.
b. Removed all specific company references.
c. Corrected Consortium address and phone numbers
d. Added new reference for ISA specification
e. Cleaned up mechanical drawings

Version 2.5, November 2003

a. Reformatted and updated
    1. New Chapter 2 "ISA Signal Definition" has been added
    2. Chapter 3 "Electrical Specification" is now Chapter 4.
    3. Chapter 4 "Levels of Conformance" is now Chapter 5.
    4. Appendix D "Connector Specifications has been combined with Appendix A
b. Signal names have been updated to reflect the names referenced in Edward Solari's book "ISA & EISA Theory & Operation"
    1. IOCHCHK* relabeled to IOCHK*
    2. RESETDRV relabeled to RESET
    3. ENDXFR* relabeled to SRDY*
    4. SYSCLK relabeled to BCLK
    5. MASTER* relabeled to MASTER16*
c. Mechanical drawings have been redone in AutoCAD showing both English and Metric units.
d. Contact finish female interface has been changed from 20 microinches minimum to 15 microinches in Figure 5
e. Mechanical performance withdrawal force has been change from 1 ounce minimum average to 1 ounce per pin minimum in Figure 5

Version 2.6, October 13, 2008

a. Added logo to cover and updated copyrights
b. Cleaned up reference section. Added Mindshare book as a reference.
c. Fixed dimensions in Figure 1. Standoff height is 0.600" (15.24mm).
d. Added standoff mechanical drawing in Appendix D.
e. Fixed page numbers in Table of Figures and Table of Tables

Figure 1: A Possible Module Stack Configuration

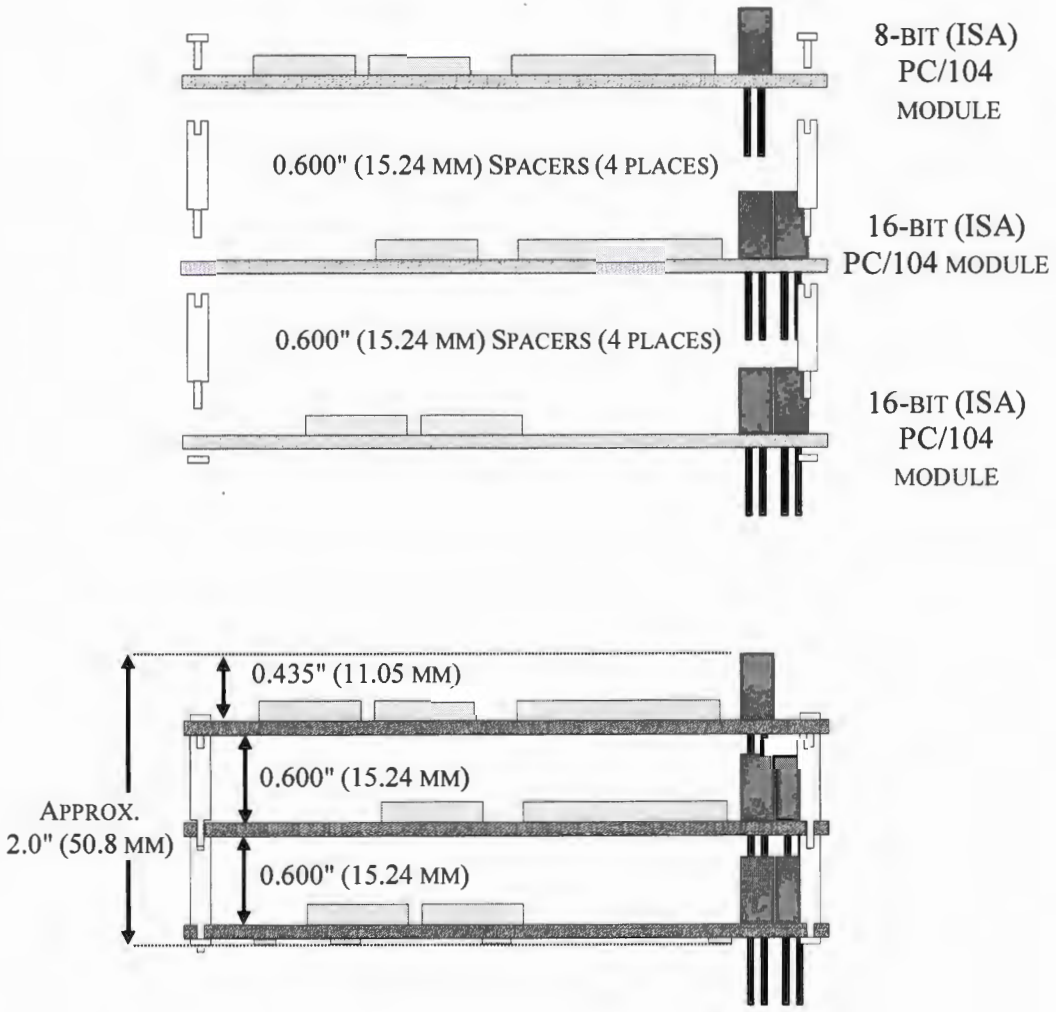


Figure 2: PC/104 8-bit Module Dimensions

Dimensions are in inches / (millimeters)

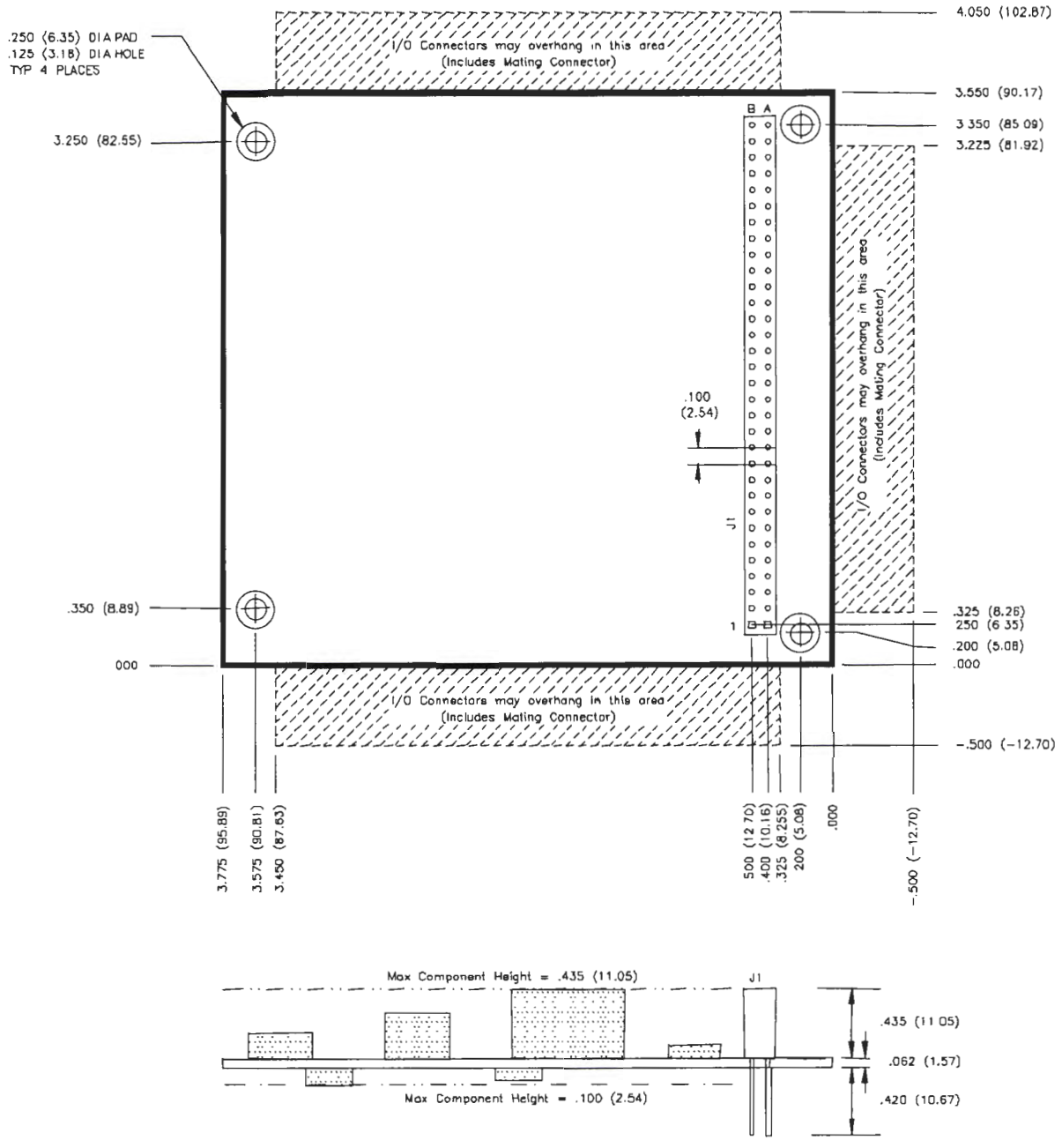
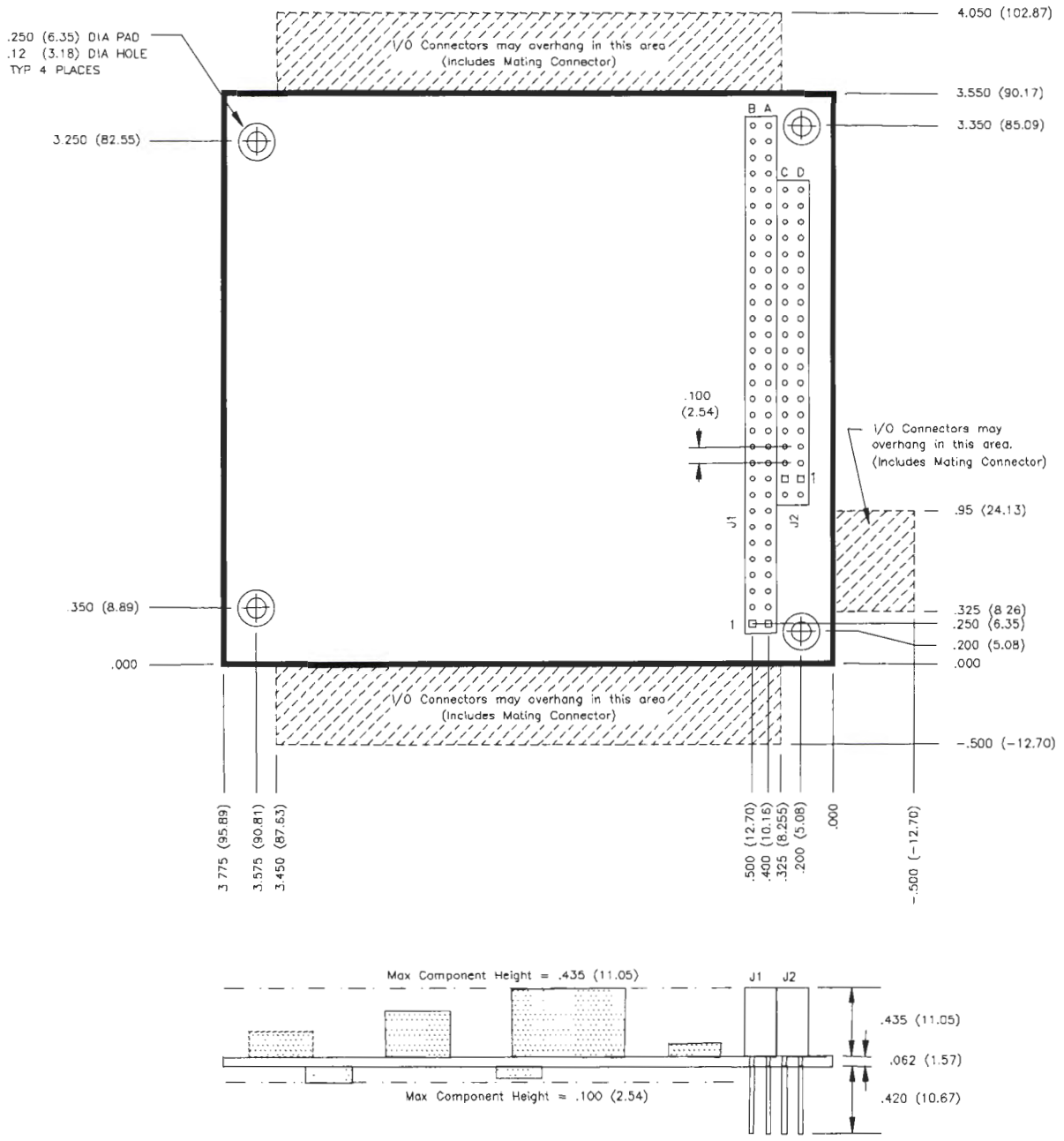


Figure 3: PC/104 16-bit Module Dimensions

Dimensions are in inches / (millimeters)



Standoffs are used to ensure stacked boards retain their connectivity. The standoffs are preferably made from stainless-steel to provide for maximum strength and height tolerance. Pads must be provided for the standoffs, with the same plating as the pads for the connectors.

All critical dimensions are listed. It is up to the user to define the thread typed. The height of the standoff shall be 0.600" +/- 0.005". The width of the standoff must be able to fit on the Standoff pad called out on the Board Layout & Dimensions Section. The width of the threaded section must be able to fit into the standoff pad hole called out in the Board Layout & Dimensions Section.

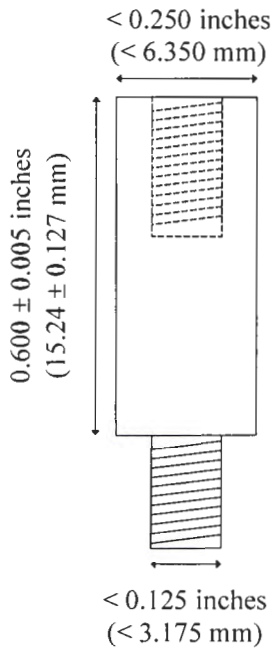


Figure 7: Standoff Mechanical Dimensions

Software Defined Radio for CubeSat Communication

Honors Capstone Reflection

Sarah Watkins

May 3, 2018

The process of completing this Honors Capstone project was an extremely valuable learning experience for me in ways that I did not expect. My project was to design a software defined radio to be used for CubeSat communication. This project was commissioned and sponsored by Harris Corporation, a defense contractor based in Florida. It involved learning about signal processing, programming an FPGA using HDL code, new software programs to enable the implementation, writing professional documents, and working closely with a professional organization to meet their specifications and report on our progress. In addition to these things, I learned more about myself, my work styles, and my field of interest.

This capstone project greatly broadened my experience in my field. Most of my previous experience fell within a power systems emphasis. I did several internships in this field, with very positive results. However, this project dealt largely with signal processing. This allowed me to utilize my knowledge from signal processing classes and apply it in a different environment. I learned during this experience that signal processing is not my main field of interest.

Learning about what I do not want to do in my career is nearly as valuable as learning about what I do want to do. This has enabled me to focus my coursework on learning concepts that deal more with my preferred emphasis. It has also enabled me to make decisions regarding my plans upon graduation with my undergraduate degree. Due to this experience, I have decided not to immediately pursue a graduate degree, but to accept a job in power systems for the time being, with eventual plans to get an MBA and transition to more business-related pursuits.

I have greatly enjoyed working with my team and with our mentors for this project, including Dr. Jake Gunther, Dr. Don Cripps, and Jolynne Berrett. Dr. Gunther was our faculty mentor. He met with us

every few weeks and offered much of his time and resources to helping us succeed with this project. His investment in his students as individuals is inspiring, especially given his responsibilities as the department head. Dr. Cripps was our design course instructor. He gave us guidance and advice about how to approach projects, mitigate stress, and how to deal with people in the workforce. Jolynne Berrett assisted us with the documentation for our project. She helped us revise, edit, and format reports, specifications, presentations, and posters.

I learned a great deal about the design process in general. It is difficult to estimate the scope, time commitment, and difficulty of a project as an undergraduate, even with work experience. The importance of setting weekly goals and regularly reporting on our progress became evident very quickly. Doing these things helped me realize how to better stay on schedule, and how to manage my time more wisely. I also learned about the difficulty of working on too many major projects at once. Doing so caused my attention to be divided, and ended up putting me behind on my capstone.

This experience taught me more about my work styles. I generally prefer to work on my own, particularly when I feel comfortable with the tasks I am given. In this case, I did not have as much experience with the subject matter, and I did not feel very comfortable approaching some of the work. I would have had a more positive experience if I had been able to work more closely and collaboratively with my team. I could have used their expertise to begin to understand the problems, rather than putting them off or wallowing in confusion. In the future, I will make more of an effort to reach out for help when I need it, and to ask questions about things I don't feel comfortable with or don't understand.

Another interesting aspect of the project was working closely with Harris Corporation. Due to the distance, most of our communication was done remotely through conference calls and emails. It was intimidating at times, because we felt more pressure as a team to present our progress and go above and beyond in our dealings with the company. I learned more about how to present things professionally, and I learned the importance of being prepared for every foreseeable question that might be asked about the design, the concepts, and the decisions we made. Fortunately, I had a positive experience working with Harris Corporation.

Most of the major problems we ran into during the design of this project related to software issues. We had to make sure we not only had the correct software and versions installed, we had to install additional packages and hardware drivers to ensure compatibility with the other software and hardware we were working with. Unfortunately, we were delayed on the project due to software licensing issues, and a naming convention that prevented us from using our current operating system to run some of our software and

compile our code. It was difficult to foresee those particular issues, but we were able to solve most of them eventually.

The other major problems we ran into were typical to working in a group. Most of them related to time management, division of labor, and working out scheduling. However, I loved working with my team. We made an effort to be supportive of each other and continue to contribute to the project.

The most important lesson I learned from this project was how to be proud of the work that I accomplished. I realized towards the end of the project that I have an inherent tendency to believe that all my projects are failures. I somehow feel as if I have not done enough, no matter how much I have accomplished. I made a conscious decision to start being proud of how hard I have worked and the things I have learned. I also decided to worry less about what other people think, and to stop overly catering to what I perceive their demands to be. I am grateful for the experience I have had here at Utah State University, and the lessons I have learned from this project.

Author Bio

Sarah Watkins is from Salt Lake City, UT, and followed in the steps of her parents and grandparents in attending Utah State University. She studied Electrical Engineering and was selected as the Outstanding Junior in the Department of Electrical and Computer Engineering in 2017. She enjoyed participating in the USU Symphony Orchestra and studying cello and piano during her time at USU.

Sarah has completed several internships, including working for Envision Engineering, ETC Group, and the California Independent System Operator. She plans to move to Salt Lake City to work for the Western Electricity Coordinating Council.