STUDY OF CHOPPER STABILIZATION IN SINGLE ENDED AMPLIFIERS

BY

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THESIS

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Abstract

Chopper stabilization is one of the prominent techniques used to overcome low-frequency noise and DC offset errors in CMOS amplifiers. This thesis presents a detailed analysis of this approach. The fundamentals of chopping, followed by the design and underlying tradeoffs of a chopper stabilized amplifier, are included. A chopper stabilized, single ended amplifier in closed loop unity gain configuration is designed using the folded cascode topology in 180 nm CMOS process. This design is verified for functionality by a thorough comparison with its non-stabilized counterpart. Simulation results, including the benefits obtained in terms of reduced flicker noise and an amplified output voltage independent of input DC offsets, are discussed.

To Maa, Paa and Bhai.

Acknowledgments

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List of Abbreviations

1/f	Flicker Noise
AC	Alternating Current
ADC	Analog-to-Digital Converter
AZ	Auto-zeroing
CDS	Correlated Double Sampling
CHS	Chopper Stabilization
CMOS	Complementary Metal Oxide Semiconductor
CMRR	Common-Mode Rejection Ratio
DC	Direct Current
IC	Integrated Circuits
LPF	Low-Pass Filter
MOSFET	Metal Oxide Semiconductor Field-Effect Transistor
nMOS	n-channel MOSFET
OpAmp	Operational Amplifier
pMOS	p-channel MOSFET
Pnoise	Periodic Noise (Analysis)
PSS	Periodic Steady State (Analysis)

Chapter 1

Introduction

This thesis describes the design of a differential input, single ended output, chopper stabilized operational amplifier in CMOS ICs. Despite the wide ranging use of operational amplifiers and temperature sensors in numerous applications, their inherent non-idealities and design tradeoffs make them prone to DC offset voltage errors and low-frequency (1/f, or flicker) noise. Chopper stabilization, as hinted by the name, is a technique used to mitigate the effect of such non-idealities. Such mitigation of DC offsets and low-frequency errors is essentially achieved by up-modulating the aforementioned non-idealities, thereby allowing them to be filtered out, or "chopped".

This chapter provides an introduction to the work presented. Section 1.1 focuses on the motivation behind this work. Section 1.2 outlines the thesis.

1.1 Motivation

This section provides underlying reasons for conducting this thesis work. First, the demand for precision of data values is studied. This is followed by an overview of the operational amplifier and what it aims to achieve. The non-idealities in the OpAmp that give rise to the need of using chopper stabilization are discussed thereafter.

1.1.1 Resolution Accuracy of Data in Analog Signal Chains

The world today stands on pillars of sound technical advancement enabled by various engineering marvels. Different fields have been supported by innovations in the engineering domain that enable machines to work the way we want them to. Be it healthcare with X-rays, ultrasound, CT scans, etc., all of which employ digitization techniques, or be it communication with the 5G technology requiring receivers that allow for low-strength signals to be captured without much complexity, or be it art that utilizes software that poses the need for high-speed microprocessors to handle heavy data processing, all domains are built upon pillars of IC design that enables the hardware and software to grow. It is vital to see that these applications require

huge amounts of analog-to-digital data conversion at very high speeds and with minimal errors.

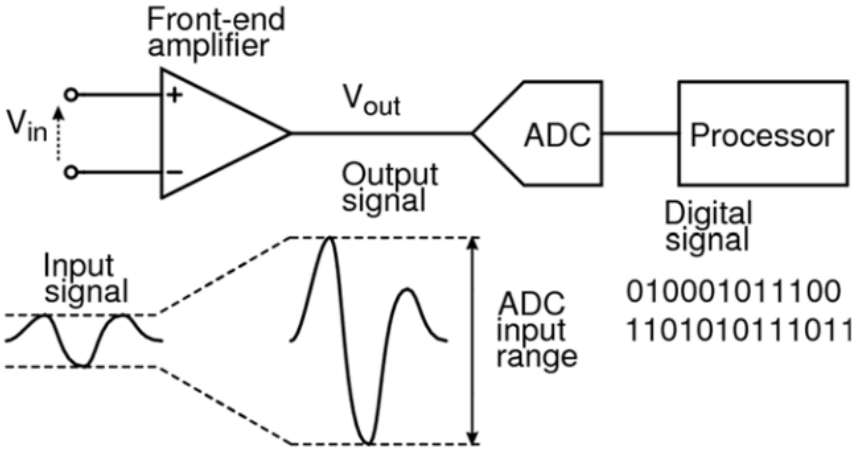


Figure 1.1: Precision Data Acquisition Signal Chain [1]

Fig. 1.1 depicts the precision data acquisition signal chain from [1], which consists of a front-end amplifier, an ADC and a digital processor. Since the resolution targeted in such chains is 16 bits or more, an input signal with a small amplitude is amplified to an amplitude to utilize the full range of the ADC. Thus, it is of utmost importance to rid this front-end amplifier of any input errors that may dominate the amplified output, thereby resulting in errors even before the analog signal is digitized. With the power supplies scaling down as CMOS technologies are advancing, even 1 μV of input offset can vary the output of the amplifier enough to produce an erroneous quantized ADC output, resulting in incorrect processing of the input.

Hence, with increasing demand for optimum use of every bit of power and with the imminent technology scaling, the need for precision has been reaching an all-time high. Modern data acquisition signal chains put a stringent specification on the upper limit for tolerance of dc offsets. With such precise accuracy requirements comes a challenge to the optimal functioning of amplifiers, wherein small, previously insignificant offsets are now rendered absolutely unacceptable.

1.1.2 The Operational Amplifier

Operational amplifiers are the backbone of numerous circuit applications. They are a key component in voltage regulation, rectification and analog-to-digital conversion and digital-to-analog conversion, to name a few. These applications have been rendered possible due to significant advancements in circuit design over the past decades. OpAmps are one of the standard circuit designs that stand out as having wide ranging applications across multiple domains. In order to better use OpAmps for such wide ranging applications, it is vital to comprehend how they function.

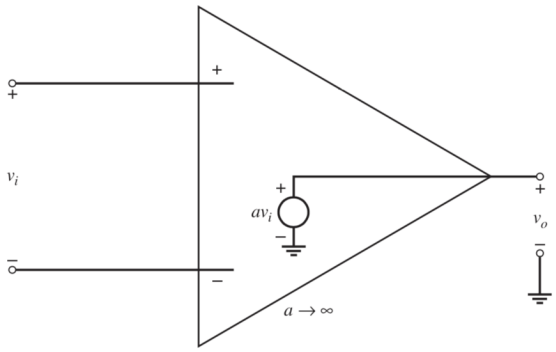
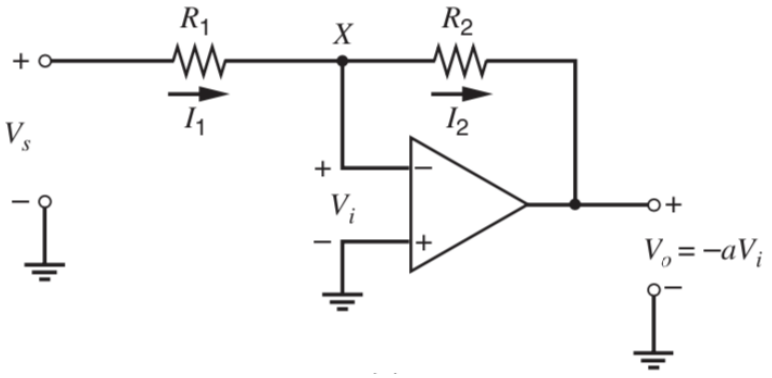
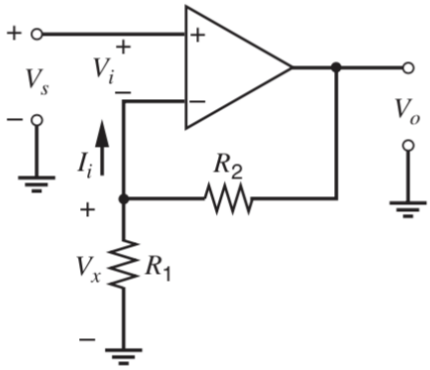


Figure 1.2: Ideal Single Ended Operational Amplifier [2]

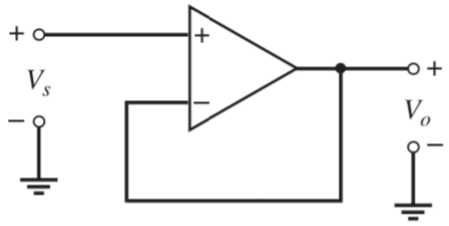
As shown in Fig. 1.2 [2], the ideal OpAmp with differential input and single ended output has infinite voltage gain, infinite input resistance and zero output resistance.



(a) Inverting Amplifier Configuration



(b) Non-inverting Amplifier Configuration



(c) Unity Gain Buffer Configuration

Figure 1.3: OpAmp in Feedback [2]

The OpAmp used in feedback, in both inverting and non-inverting configurations, is depicted in Fig. 1.3.

Its gain in such closed loop inverting configuration in Fig. 1.3a can be computed to be:

$$\frac{V_o}{V_s} = -\frac{R_2}{R_1}\left[\frac{1}{1+\frac{1}{a}\left(1+\frac{R_2}{R_1}\right)}\right] \tag{1.1}$$

where a is the gain of the amplifier and R_1 and R_2 are as depicted in Fig. 1.3a. If the gain of the OpAmp is large enough so that

$$a\left(\frac{R_1}{R_1+R_2}\right) \gg 1 \tag{1.2}$$

then the closed loop gain becomes

$$\frac{V_o}{V_s} = -\frac{R_2}{R_1} \tag{1.3}$$

In the non-inverting configuration, the gain of the closed loop amplifier as shown in Fig. 1.3b becomes

$$\frac{V_o}{V_s} = \left(1+\frac{R_2}{R_1}\right)\frac{\frac{aR_1}{R_1+R_2}}{1+\frac{aR_1}{R_1+R_2}} \simeq \left(1+\frac{R_2}{R_1}\right) \tag{1.4}$$

The approximation in equation 1.4 is valid if equation 1.2 holds.

The OpAmp is said to be in unity gain configuration if it is connected as shown in Fig: 1.3c where it acts as a voltage follower. This is a variant of the non-inverting amplifier configuration with $R_1 \to \infty$ and $R_2 = 0$. The gain is close to one, i.e., unity, if $a \gg 1$.

1.1.3 The Need for Chopper Stabilization

OpAmps have deviations from ideality [2] including errors induced by input bias current mismatch, input offset current, input offset voltage, limited common mode input range, finite common mode rejection ratio, finite power supply rejection and finite input and output resistances. The problem is magnified due to the presence of noise in MOSFETs, as can be seen in Fig. 1.4 [1]. While thermal noise exists at all frequencies, at low frequencies, amplifier noise is dominated by flicker noise that causes undesired distortion, thereby necessitating techniques to reduce such adverse effects.

The aforementioned low-frequency imperfections in OpAmps result in issues in circuit design such as:

- High-precision industrial, automotive and medical applications rely on the accuracy of outputs produced by OpAmps.
- Typical (1/f) noise is greatest right in the area of sensor bandwidth.
- Such non-ideal factors limit ADC resolution which ripples through to damage the processor output,

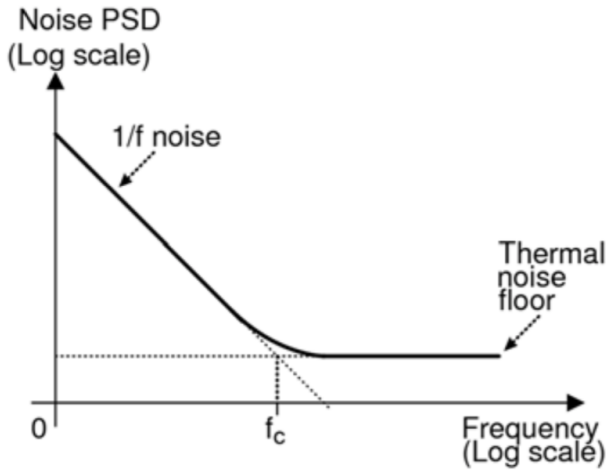


Figure 1.4: Noise PSD of a Typical CMOS OpAmp [1]

thereby distorting functionality.

- Some types of signals that need amplifying can be so small that they need an incredibly high gain, but very high gain DC amplifiers are very hard to build with low offset, (1/f) noise and reasonable stability and bandwidth.

Despite these non-ideal effects, CMOS OpAmps find wide usage due to their ready integrability with circuits such as ADCs that are also realized using CMOS ICs. CMOS OpAmps are also cheaper to build and fabricate on a large scale than BJTs. Since CMOS realizations of circuits also consume very low static power due to easy switching activity that further assists digital-to-analog and analog-to-digital conversion, CMOS OpAmps become the first choice to design circuits that fulfill such functionality constraints. Hence, there is a need to use such OpAmps while using other techniques to combat their non-idealities. Chopper stabilization is one such technique which is simple and offers many benefits in terms of helping designers achieve near-ideal functionality in their circuits. Chopper stabilized amplifiers compensate for low-frequency errors such as input offset voltage, input bias current, temperature drift and (1/f) noise. They are therefore vital building blocks that must be properly understood and implemented to fully reap the benefits of many analog circuits, most importantly, CMOS amplifiers.

1.2 Outline

This thesis is organized into six chapters. This chapter serves as background explaining why chopper stabilization is worth studying and integrating into CMOS amplifier IC design. The remaining chapters provide deeper understanding about how to rid OpAmps of their non-ideal input DC offsets and (1/f)

noise. Chapter 2 focusses on the theory behind chopper stabilization and how it is accomplished. Chapter 3 describes the circuit designed to verify the functionality of the chopper stabilized, single ended amplifier. Performance results of the amplifier are included both with and without chopper stabilization, in order to compare. The process of combating input DC offset with chopper stabilization is presented in chapter 4, along with simulation results. Chapter 5 gives a comparative analysis regarding noise reduction in the chopper stabilized amplifier and results obtained from simulation. The thesis work is concluded in chapter 6.

Chapter 2

Chopper Stabilization

This chapter discusses in detail the theory behind chopper stabilization and how it works. Section 2.1 includes a discussion of the fundamental idea behind chopper stabilization. Other techniques used to combat low-frequency noise and dc offset voltage variations are covered in section 2.2. A comparative study between the possible techniques is presented in section 2.3. Section 2.4 includes a literature review of chopper stabilization being used in amplifier design to date.

2.1 Fundamental Idea behind Chopping

Fig. 2.1 [1] depicts a functional diagram of a chopper amplifier comprising of an input chopper CH_{IN}, an amplifier A_1, an output chopper CH_{OUT}, and a low-pass filter LPF. Suppose that the amplifier, A_1, has an undesired input DC offset voltage depicted by the DC source V_{os1}. The switch set CH_{IN} comprising four switches $S1 - S4$ is responsible for up-modulating the input. This modulated input along with the DC offset is amplified by A_1. Demodulation is performed by switch set CH_{OUT} comprising four switches: $S5 - S8$. The switches are driven by complementary clocks ϕ_{CH} and $\overline{\phi_{CH}}$ both of which operate at a frequency f_{CH}, the chopping frequency.

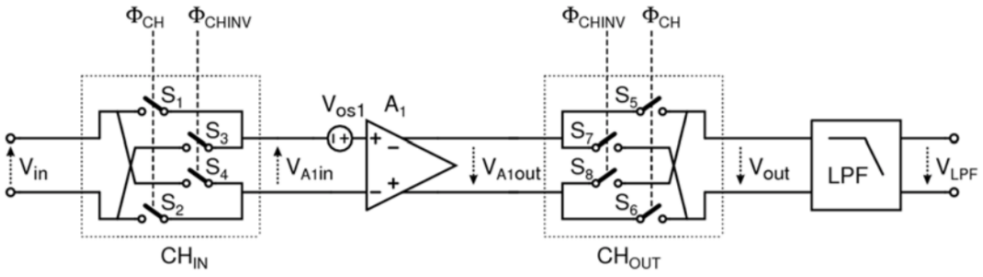


Figure 2.1: Functional Diagram of Chopping [1]

Fig. 2.2 tracks the input signal as it goes through the amplification process via a chopper stabilized amplifier. Time and frequency domain plots are included for every differential node that the signal traverses on its way to getting amplified. It is important to note that the final output produced after such amplification

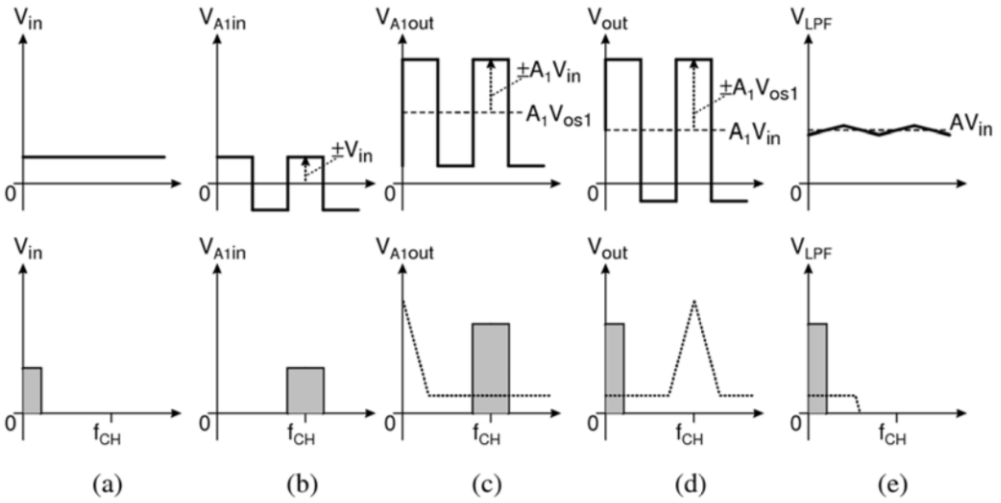


Figure 2.2: Signal, Offset, and Noise in the Time and Frequency Domains [1]

is AV_{IN} in place of $A(V_{IN}+V_{OS})$, which would have been the case if chopper stabilization was not employed. Following is a series of steps involved in the process:

1. CH_{IN} up-modulates the applied low-frequency input signal V_{in} as shown in Fig. 2.2 (a), to f_{CH}, thereby producing the signal shown in Fig. 2.2 (b).

2. This up-modulated signal then gets hit by the amplifier input offset, V_{OS}. This combined signal is then amplified by A_1 to produce an output as shown in Fig. 2.2 (c). The MOSFETs in the circuit implementation of the amplifier add to significant $(1/f)$ noise at low frequencies and thermal noise at higher frequencies, as depicted by the dashed line in the frequency domain part of the same figure.

3. Demodulation back to baseband is then performed by CH_{OUT} on the amplified output signal and the thermal noise around the chopping frequency f_{CH}. At the same time, this also works as up-modulation of the amplified DC input offset and the (1/f) low-frequency noise to f_{CH}. This is depicted by Fig. 2.2 (d).

4. Finally, the LPF attenuates high-frequency composition of the signal, so that only the thermal noise floor interferes with the intended amplifier response (Fig. 2.2 (e)).

Hence, using the fundamental idea behind this technique, chopper stabilization works to eradicate the input DC offset and $(1/f)$ noise. However, when a circuit implementation is done for this idea, it is important to note that F_{LPF} must be less than F_{CH} in order to accurately remove ripple at the output [3]. This sets

an upper limit on the usable bandwidth range of the amplifier. This is the reason that chopper stabilization is employed in techniques that can work with limited output signal bandwidth, which is true for usage of OpAmps in ADCs or the front end amplifiers for temperature sensors.

2.2 Other Techniques for Reducing Amplifier DC Offset

- Auto-zeroing (AZ)

  The AZ technique samples the unwanted quantity (noise and offset) and then subtracts it from the instantaneous value of the contaminated signal [4]. The circuit describing a generalized auto-zero amplifier implementation [5] is shown in Fig. 2.3.

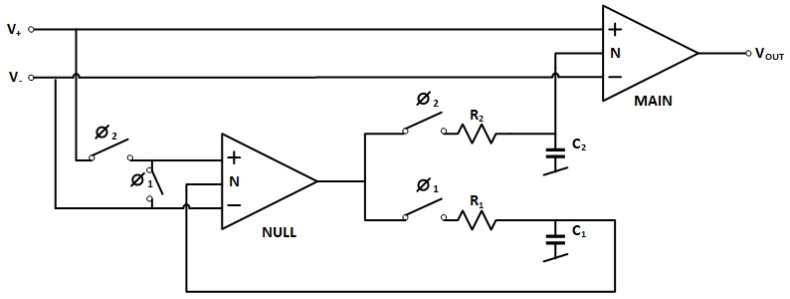


Figure 2.3: Feed-forward Amplifier Design [5]

There are two amplifiers used: main and null (aux). The circuit functions such that at high frequencies, the response of the system is dictated by that of the main amplifier alone, which is error-free since the low-frequency errors and DC offsets do not interfere with the input signal at high frequencies. At low frequencies, two clock phases govern the system operation. During the first clock phase, the effective offset is given by:

$$V_{os(eff)} = \left(\frac{1}{1+A_n}\right) V_{osN} \tag{2.1}$$

where $V_{os(eff)}$ is the effective offset voltage, which is reduced from the offset voltage of the nulling amplifier, V_{osN}, by the open loop gain of the amplifier, A_n. In the second clock phase, the system output voltage, V_{out}, is set to:

$$V_{out} = A_m A_n \left[V_+ - V_- + \frac{V_{osM} + V_{osN}}{A_n}\right] \tag{2.2}$$

where A_m and V_{osM} are the open loop gain and the offset voltage of the main amplifier. Hence, using the AZ technique, overall offset of the system is given by a sum of individual offsets of the two amplifiers, divided by the open loop gain of the nulling amplifier. Since the gain of the nulling amplifier

is large, the resultant offset value is rendered very small.

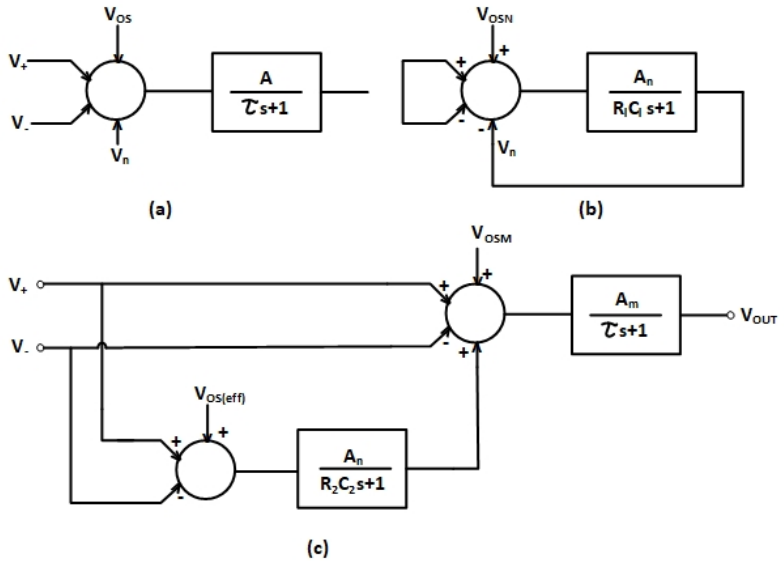


Figure 2.4: (a) Internal Amplifier Model (b) Null Amplifier Block Diagram during Clock Phase 1 (c) System Block Diagram During Clock Phase 2 [5]

Even the lowest power auto-zero amplifiers require hundreds of microamperes of quiescent current in order to suppress the in-band noise caused by folding which results from sampling [6]. They have a very modest 200 kHz bandwidth with broadband noise nearly 150 nV/$\sqrt{\text{Hz}}$ at 1 kHz. In contrast, some standard CMOS and bipolar amplifiers offer about the same bandwidth, with lower noise, on less than 10 μA of quiescent current [7].

- Correlated-Double Sampling (CDS)

  The CDS operation comprises an auto-zero operation followed by a S/H circuit. CDS seeks to reduce low-frequency noise circuits by means of high-pass filtering. It is inherently a sampled method [4]. CDS can be utilized to improve the effective gain of OpAmps used in areas such as digital signal processing. In applications that require sampled data circuits such as switched capacitor stages, CDS techniques are used predominantly [4].

2.3 Comparison between Chopper Stabilization and Other Techniques

Since CHS is based on modulation rather than sampling in auto-zero amplifiers, CHS seems the preferable option for continuous-time signals. If the chopping frequency is much larger than the noise corner frequency,

Table 2.1: Comparison between Techniques used to Mitigate Low-Frequency Errors [6]

Auto-Zero	Chopper Stabilized	Chopper Stabilized and Auto-Zero
Very low offset, TC_{VOS}	Very low offset, TC_{VOS}	Very low offset, TC_{VOS}
Sample/hold	Mod/demod	Sample/hold plus mod/demod
Higher low-frequency noise due to aliasing	Similar noise to flat band (no aliasing)	Combined noise shaped over frequency
Higher power consumption	Lower power consumption	Higher power consumption
Wide bandwidth	Narrow bandwidth	Widest bandwidth
Lowest ripple	Higher ripple	Lower ripple level than chopping
Little energy at auto-zero frequency	Lots of energy at chopping frequency	Little energy at auto-zero frequency

then the baseband white noise in the output is only very slightly larger (due to noise folding) than it was without CHS. However, noise folding is more significant in CDS related schemes.

One disadvantage of using the CHS technique is that a continuous-time CHS system causes the OpAmp to amplify a higher frequency signal and hence its effective gain is usually reduced. In contrast to this, CDS can often be employed to enhance gain of the OpAmps in the signal path [4]. Also, using chopper stabilization, the cutoff frequency of the LPF needs to be set lower than f_{CH} which, as hinted in section 2.1, limits the usable signal bandwidth.

Choppers are therefore a good choice for low-power, low-frequency applications (< 100 Hz), whereas auto-zero amplifiers are better for wide-band applications. A combination of auto-zero and chopping techniques is ideal for applications that require low noise, no switching glitch, and wide bandwidth. Table 2.1 [6] summarizes the aspects of auto-zeroing, chopper stabilization and a combination of both, with respect to each other.

2.4 Literature Review

This section briefly reviews the progress in the area of chopper stabilization.

Among the first few circuits to be designed utilizing chopper stabilization was that presented in [8], where a fifth-order low-pass switched capacitor filter is implemented using chopper stabilization. The filter output noise reduced from around 10 μV without chopper stabilization to 2 μV with the same. Individual amplifier equivalent noise reduced to 40 nV/$\sqrt{\text{Hz}}$ with 128 kHz chopping frequency, from its original value of 800 nV/$\sqrt{\text{Hz}}$. This was implemented in 15 μm CMOS process with a $\pm$7.5 V supply and 20 MW power dissipation. In 1987, C. Enz et al. designed a second-order LPF [9] using chopper stabilization in 3 μm CMOS, consuming 34 μW power. The equivalent input noise is said to be reduced to 63 nV/$\sqrt{\text{Hz}}$ with 200

Hz chopping frequency and the offset is less than 5 μV .

In 2002 Tang [10] presented a 3 μV-offset operational amplifier with 20 nV/$\sqrt{\text{Hz}}$ input noise PSD at DC employing both chopping and auto-zeroing. The auto-zero designed by Kugelstadt [11] in 2005 uses a quiescent current of 300 μA and provides typical values of 1 μV of input offset and 20 nV/°C of offset drift over temperature. In 2009, Analog Devices came up with a product, MT055 [12] for chopper stabilized auto-zero OpAmps with 22 nV/$\sqrt{\text{Hz}}$ input voltage noise at 1 KHz, 1 μV input offset voltage and 0.002 μV/°C input offset voltage drift.

A 21 nV/$\sqrt{\text{Hz}}$ chopper-stabilized multi-path current-feedback instrumentation amplifier [13] with 2 μV offset was presented in 2010 by Fan et al. In 2011, Y. Kusuda presented a 5.9 nV/$\sqrt{\text{Hz}}$ chopper amplifier [14] with 0.78 μV maximum offset and 28.3 nV/°C offset drift. Then came the era of employing chopper stabilization for biomedical sensors, $\Delta\Sigma$ADCs, instrumentation amplifiers, etc. In 2018, Xu and Moon [15] presented a chopper-stabilized source follower coupling based low-pass filter implemented in 0.18 μm CMOS process. The circuit achieved output noise density of 9.4 nV/$\sqrt{\text{Hz}}$ over the filter bandwidth of 20 MHz.

Such widespread use of chopper stabilization techniques was instrumental in this study of chopper stabilization with the aim to understand stand-alone, chopper stabilized, single ended amplifiers and how they function better than their non-stabilized counterparts. In this domain, two papers were found that employed chopper stabilization in a single ended amplifier. Peng et al. [16] introduce a single ended, chopper stabilized amplifier to build a low-noise voltage reference. Using 3.7 V power supply and 0.5 μm CMOS process, they achieve a low-noise voltage of 0.121 μV for their output reference voltage. Yang et al. [17] propose a low-power chopper amplifier without the need for an external low-pass filter. This circuit simulated using 0.18 μm CMOS technology achieves equivalent input noise voltage of 73 nV/$\sqrt{\text{Hz}}$ at 1 Hz.

Chapter 3

Design of a Single Ended Chopper Stabilized Amplifier

This chapter covers the design and verification of the proposed chopper stabilized amplifier. It has been broken into two sections. Section 3.1 covers the challenges faced in design and tradeoffs therein. Section 3.2 focuses more on the results obtained from the design, comparing responses between the regular amplifier and a chopper stabilized configuration for the same design.

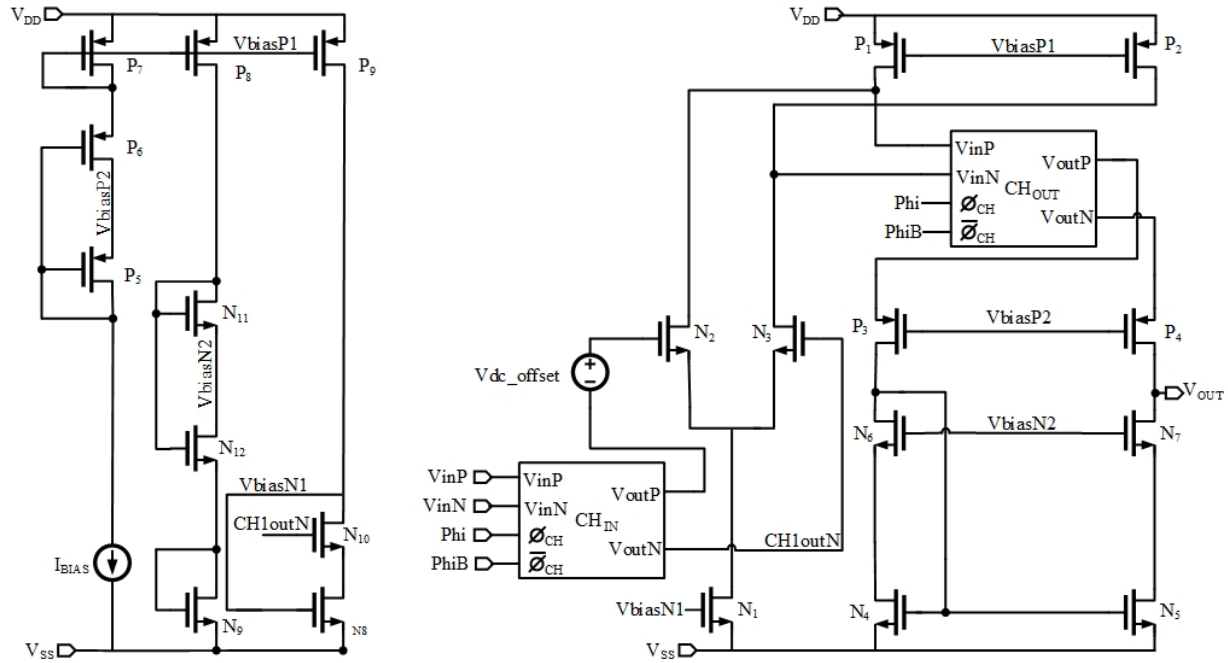
3.1 Implementation

The design proposed in this thesis provides freedom to choose any amplifier topology based on convenience. The choice is therefore between a two-stage amplifier, a telescopic cascode or a folded cascode. Given that it is desired that the amplifier be single stage in order to investigate whether chopper stabilization yields any benefits in that configuration, the inclination is toward the folded cascode topology.

One of the main reasons behind this choice is the fact that, because of the way a chopper switch is structured, there have to be "two paths". The traditional use of chopper stabilization in fully differential amplifiers was particularly beneficial since the amplifier had differential inputs and differential outputs. To create a single ended counterpart, a design has to be conceived that enables down-modulation before producing the actual single ended output. Hence, a folded cascode is a clear choice since it enables up-modulation before the differential input pair and easy demodulation, thanks to the two arms at the folding node. The reduced output swing in a telescopic cascode does not make it a favorable topology since chopper stabilization is used more in a cascaded design targeting applications such as a voltage reference, building offset invariant temperature sensors, etc., rather than just in stand-alone amplifier usage. A two-stage amplifier lacks the freedom to use another arm as in the folded topology, for demodulation. Fully differential, two-stage, chopper stabilized amplifiers are commonly used because demodulation can occur on the differential output.

The amplifier shown in Fig. 3.1b was designed in 180 nm CMOS technology using Cadence Virtuoso, in order to evaluate the performance of a chopper stabilized amplifier in single ended configuration. A supply

voltage of 1.8 V was chosen. The folded cascode topology chosen is an nMOS-input differential pair which is passed to a pMOS folded stage. Here, as seen in Fig. 3.1b, the input is up-modulated using a chopper switch and then sent to the differential input pairs of the amplifier. This modulated input is amplified by the gain of this stage, after which, at the folding node, demodulation occurs. Once the amplified input has been demodulated, a common gate cascode produces the single ended output at its drain.



(a) Biasing Network

(b) Folded Cascode Amplifier

Figure 3.1: Proposed Chopper Stabilized Amplifier Circuit Diagram

The biasing for this proposed amplifier configuration is shown in Fig. 3.1a. A pMOS current mirror is used to bias the current to the folding nodes of the amplifier. Fig. 3.2 shows the connection for switches within the CH_{IN} and CH_{OUT} specified in Fig. 3.1b.

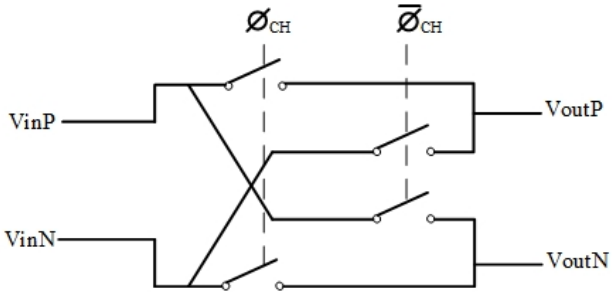


Figure 3.2: Chopper Switch Sets: CH_{IN} and CH_{OUT}

The MOSFETs are sized based on optimal gain constraints set using $g_m I_D$ methodologies discussed in

[18]. Table 3.1 provides information regarding DC operation of the circuit designed including the device transistor sizes, bias currents, g_m values and Δ values. Table 3.2 gives additional specifications such as the value of the ideal current source used and the supply voltages.

Table 3.1: Device Metrics (I) for the Chopper Stabilized Amplifier of Fig. 3.1

MOSFET Name	Width[μm]	Length[nm]	Bias Current[μA]	g_m[μS]	$\Delta[V] = \frac{2}{g_m/I_D}$
N1	30.015	180	149.00	2724.00	0.109
N2	14.985	180	74.59	1413.00	0.106
N3	14.985	180	74.41	1410.00	0.106
N4	4.950	360	10.45	192.70	0.108
N5	4.950	360	10.48	193.50	0.108
N6	4.950	360	10.45	200.90	0.104
N7	4.950	360	10.48	201.50	0.104
N8	4.950	180	25.03	457.90	0.109
N9	4.950	360	22.76	355.50	0.128
N10	4.950	180	25.03	468.00	0.106
N11	4.950	360	22.76	366.60	0.124
N12 (linear)	1.665	360	22.76	143.90	0.316
P1	40.005	360	85.04	1003.00	0.169
P2	40.005	360	84.89	998.90	0.169
P3	9.990	360	10.45	168.30	0.124
P4	9.990	360	10.48	168.30	0.124
P5	9.990	360	23.33	274.60	0.169
P6 (linear)	3.330	360	23.33	88.22	0.529
P7	9.990	360	23.33	281.90	0.165
P8	9.990	360	22.76	276.40	0.164
P9	9.990	360	25.03	295.89	0.169

Table 3.2: Device Metrics (II) for the Chopper Stabilized Amplifier of Fig. 3.1

Other Components	Value
I_{BIAS}	70μA
V_{dc_offset}	0 V
V_{DD}	1.8 V
V_{SS}	0 V

3.2 Performance Results

It is important in order to verify accuracy that the gain of the amplifier designed can be successfully predicted, so that the ripple at the output is verified. Hence, for the sake of simplicity in design, the amplifier is put in unity gain buffer configuration, as depicted in Fig. 3.3, such that if the loop gain is high enough, the output voltage is almost the same as the voltage applied at the positive input terminal of the amplifier. The clocks ϕ and $\overline{\phi}$ are the two non-overlapping clocks that work as clocks to chopper switches used to

modulate/demodulate. The buffer output is passed through a third-order low-pass filter in order to reduce output ripple. An input sine wave of frequency $F_{in} = 50$ Hz and amplitude 100 μV is applied over a common mode DC input of 800 mV to the positive input of the amplifier. The clocks ϕ and $\overline{\phi}$ have a chopping frequency $F_{CH} = 10$ kHz. Based on the inequality $F_{in} < F_{low-pass\_filter} < F_{CH}$, the values for the allowed ranges for resistance and capacitance of the third-order RC low-pass filter can be calculated. These values are chosen to be $R = 160$ MΩ and $C = 1$ pF.

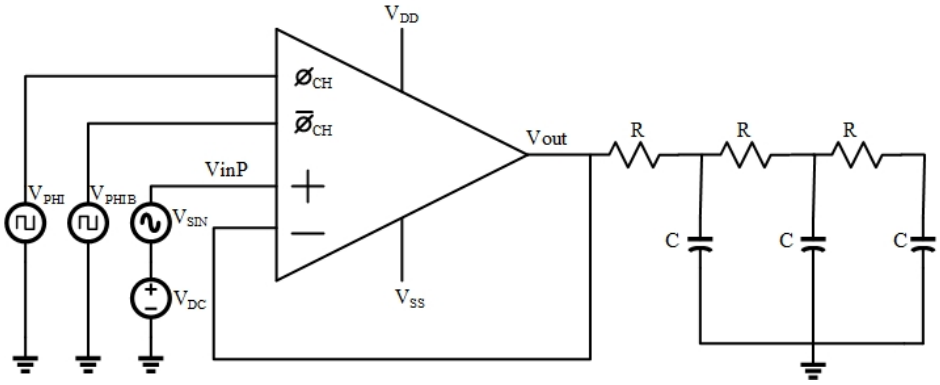


Figure 3.3: Amplifier Unity Gain Buffer Configuration for Design Verification

3.2.1 AC Response

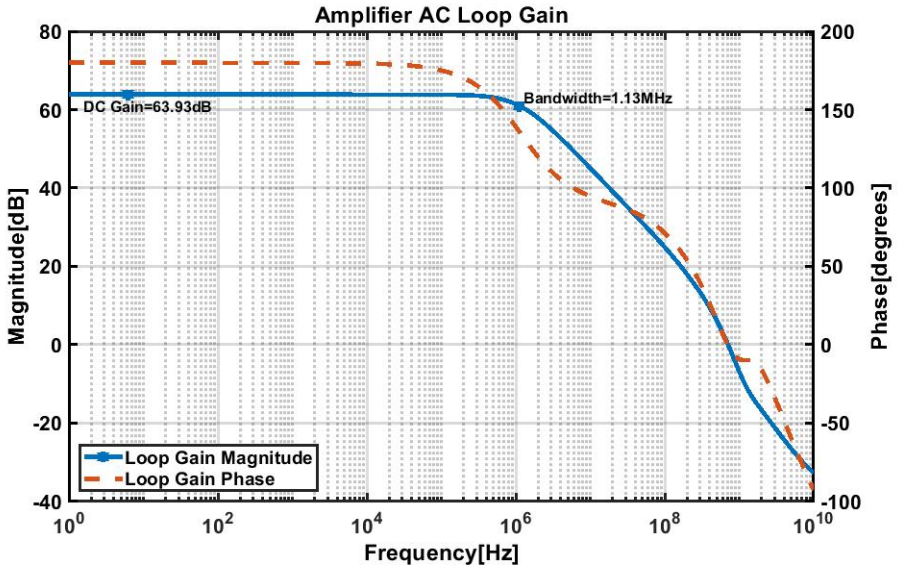


Figure 3.4: Amplifier AC Loop Gain

The designed amplifier in its closed loop unity gain configuration was simulated using Cadence Analog Design Environment (ADE) with Spectre analysis tools. Negative feedback is ensured in order to maintain

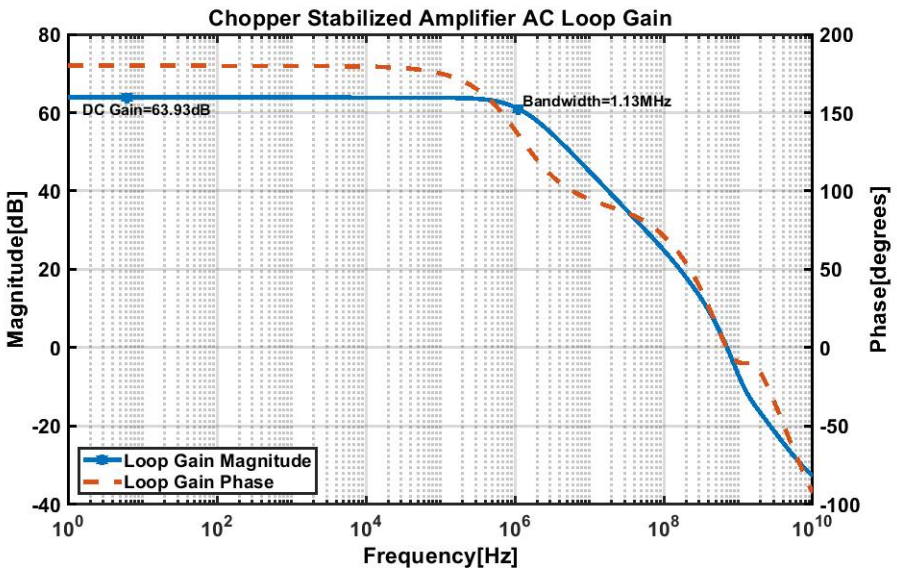


Figure 3.5: Chopper Stabilized Amplifier AC Loop Gain

stability. An stb analysis was run in order to check the AC closed loop gain, after accurate probe placement that allows Cadence to correctly break the loop. Fig. 3.4 depicts the desired loop gain for the regular amplifier, without chopper stabilization. It is important to note that the regular amplifier is essentially the chopper stabilized amplifier with $\phi = 1$ and $\overline{\phi} = 0$. Sixty (60) dB of DC gain is obtained. Since the AC gain with chopper stabilization is none other than the gain for $\phi = 0$ and $\overline{\phi} = 1$, the chopper stabilized amplifier loop gain was found by interchanging the clocks to satisfy the desired constraint. Fig. 3.5 depicts the AC loop gain of the chopper stabilized amplifier. As can be seen from both the figures, the AC loop gains show a matching for the regular amplifier and the chopper stabilized amplifier. Hence, it can be concluded that the two agree in terms of AC loop response.

3.2.2 Transient Response

In order to measure the transient response of the amplifier, a transient analysis is run for approximately 10 input clock cycles. This run on the regular amplifier provides a unity gain as shown in Fig. 3.6. It can be seen that the voltage observed at the output of the amplifier is slightly less than that applied at the input since the amplifier has a finite gain of 60 dB. This drop vanishes for a gain of about 115 dB which is obtained by simulating an ideal amplifier; however, in order to avoid unnecessary complexity in design in order to achieve a 115 dB gain, it is important to keep in mind the aim of this study, which is to investigate the effects of chopper stabilization on single ended amplifiers.

Therefore, we can overlook the 0.0005 V difference between the input and output in the designed unity

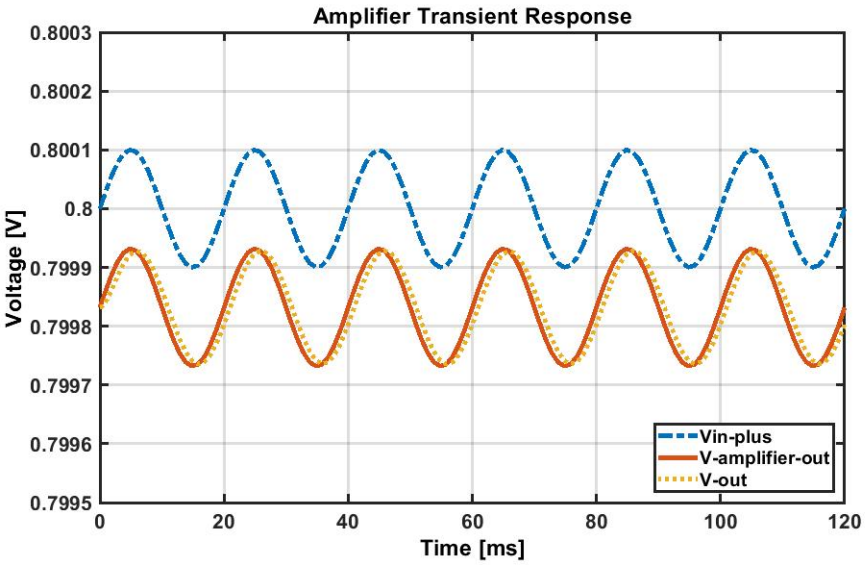


Figure 3.6: Amplifier Transient Response

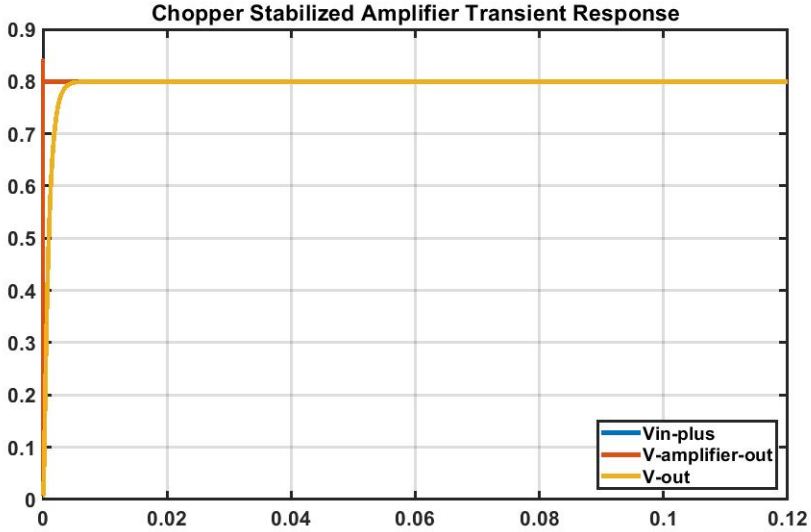


Figure 3.7: Chopper Stabilized Amplifier Transient Response

gain buffer amplifier. As can be seen from Fig. 3.6, the final voltage obtained after low-pass-filtering the amplified output is just a delayed version of the amplified output itself.

When the same experiment is performed on the chopper stabilized amplifier, the response shown in Fig. 3.7 is obtained. Here, the amplified output initially spikes due to the first switching action, an overshoot less than 0.5 V. The final output after low-pass-filtering is shown to rise from 0 V as the nose gets charged, based on a time constant set by the R and C of the third-order filter. A zoomed plot as shown in Fig. 3.8 is obtained, from which it is confirmed that the chopper stabilized amplifier obtains the same characteristic

response as was obtained by the regular amplifier shown previously. Hence, there exists a match between the transient characteristics of the regular amplifier and the chopper stabilized amplifier.

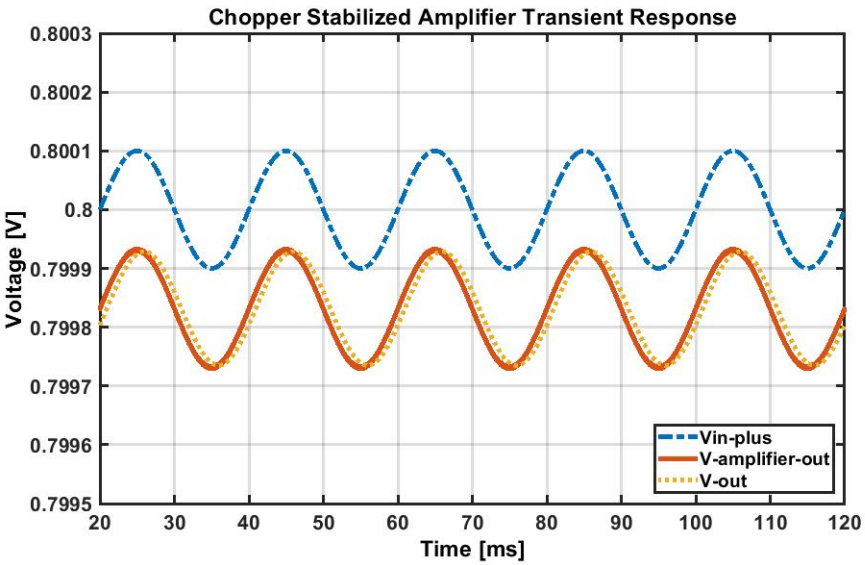


Figure 3.8: Chopper Stabilized Amplifier Transient Response (Magnified)

Thus, along with the aforementioned simulations in this section, the functionality of the chopper stabilized circuit is verified. A match is obtained in terms of both AC loop response and transient response among the two topologies of the designed single ended amplifier, with and without chopper stabilization.

Chapter 4

Effect of DC offset on Amplifier Performance

One of the most beneficial advantages of using chopper stabilization is its ability to combat DC offsets in the amplifier design so as to make it invariant to such mismatches. This chapter investigates the differences between amplifier performance in the present of a DC offset, with and without chopper stabilization.

4.1 Propagation of DC Offset

With the advancement of technology scaling, the precision of amplifiers needs to adhere to strict values. Such requirements are essential in order to build comparators in analog-to-digital converters, temperature sensors that are invariant to offset changes with temperature, etc. In the absence of any stabilization technique, an input offset at the differential pair propagates to the output and results in a change in the average amplified output voltage. Chopper stabilization works to counteract this effect by introducing modulation, demodulation and filtering, as discussed in section 2.1. It is important to remember that DC offsets are deterministic DC variations that occur as a result of systematic and random mismatch within the devices during the design process [1].

4.2 Performance Results

In order to compare amplifier performance with and without chopper stabilization, the simulation was prepared in much the same way as in section 3.2. Here too, a 100 μV input sine voltage was applied to the input positive node over a common mode of 800 mV. A 10 mV DC offset is applied to the positive input nMOS from the differential pair. It is beneficial to refer to Fig. 2.1 and Fig. 2.2 in order to ensure that the offset is applied at the right node, after up-modulating the input and before reaching the amplifier input nodes. A parametric sweep of DC offset is also performed on both the topologies where the DC offset is swept from 0 mV to 20 mV in linear steps of 5 mV each.

4.2.1 Without Chopper Stabilization

In the case of the regular amplifier, the application of a 10 mV DC offset results in a 10 mV change in the output voltage, as depicted in Fig. 4.1.

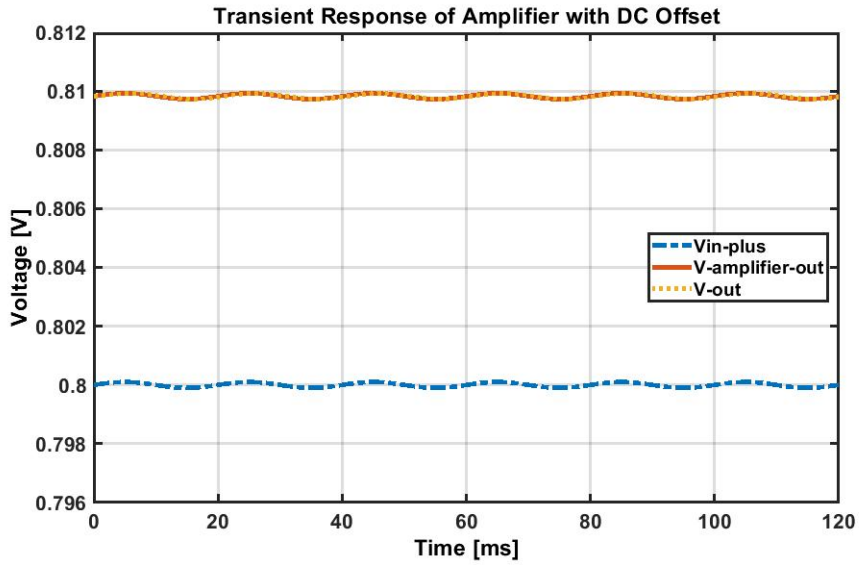


Figure 4.1: Transient Response of Amplifier with DC Offset

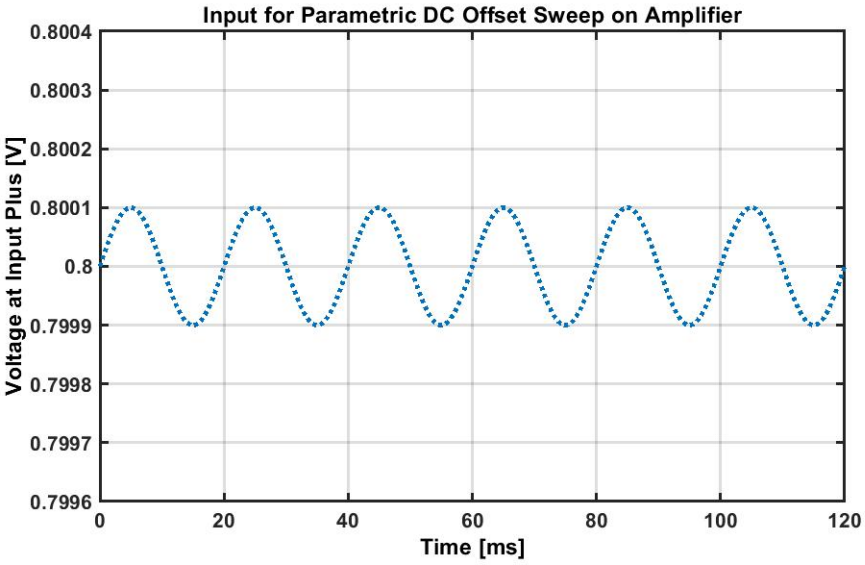


Figure 4.2: Input for Parametric DC Offset Sweep on Amplifier

When the above mentioned parametric sweep is applied at the input pair of the amplifier, the resulting outputs are produced in Fig. 4.3. For all these outputs, it is vital to note that the input never actually changed, as shown in Fig. 4.2. Hence, any DC offset applied to the inputs of a regular amplifier directly

propagates to the amplifier outputs. The amplifier with a gain A, offset voltage V_{OS} and for an input voltage of V_{in} produces an output given by $A(V_{in} + V_{OS})$, instead of just $A(V_{in})$. Since in the unity gain buffer configuration, the closed loop gain, A, is unity, it is justified for the output voltage to be shifted up to $(V_{in} + V_{OS})$, thereby shifting the average output by the applied DC offset voltage.

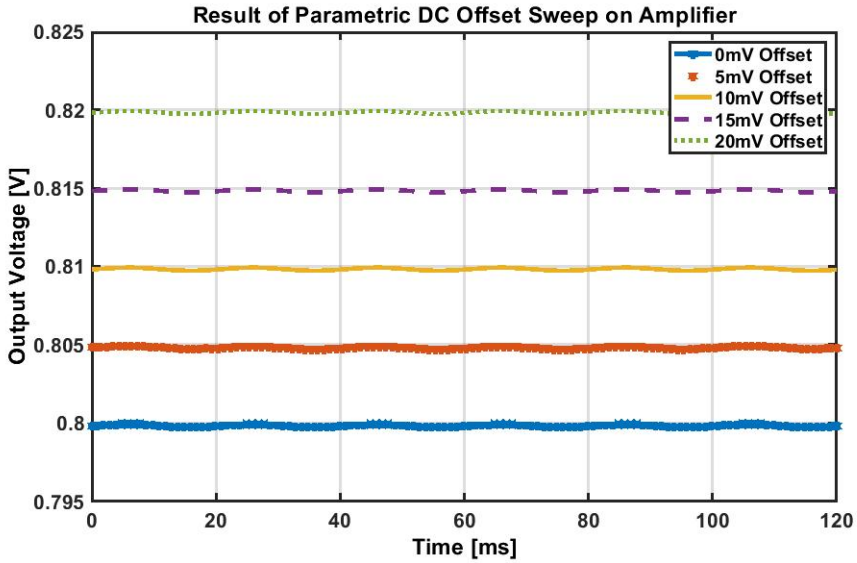


Figure 4.3: Result of Parametric DC Offset Sweep on Amplifier

4.2.2 With Chopper Stabilization

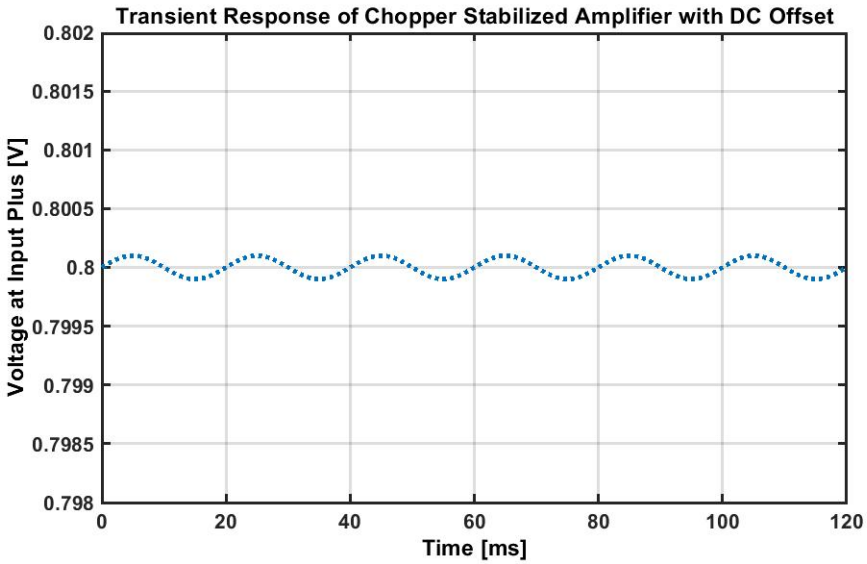


Figure 4.4: Transient Response of Chopper Stabilized Amplifier with DC Offset (Input)

For the case of the chopper stabilized amplifier the same simulation tests as done in the previous section yield different results. First, a 10 mV DC offset is applied to the input of the amplifier in a similar way as in the case of the regular amplifier. The input voltage to the chopper switch for up-modulation is depicted in Fig. 4.4, the same as the case before with an average of 800 mV. The resulting output obtained is shown in Fig. 4.5. It can be seen that the amplifier output produces a similar overshoot as in the transient case discussed in section 3.2.2. The final low-pass-filtered output too rises from 0 mV toward the final value.

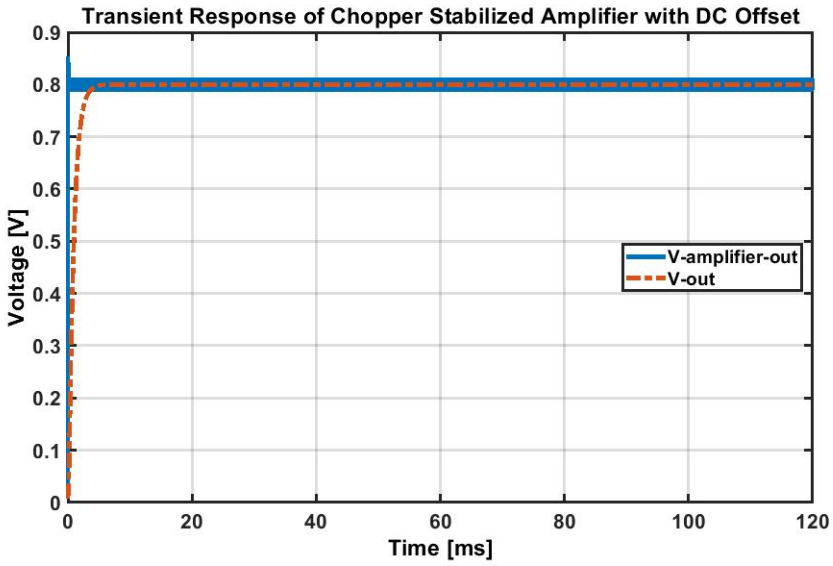


Figure 4.5: Transient Response of Chopper Stabilized Amplifier with DC Offset (Output)

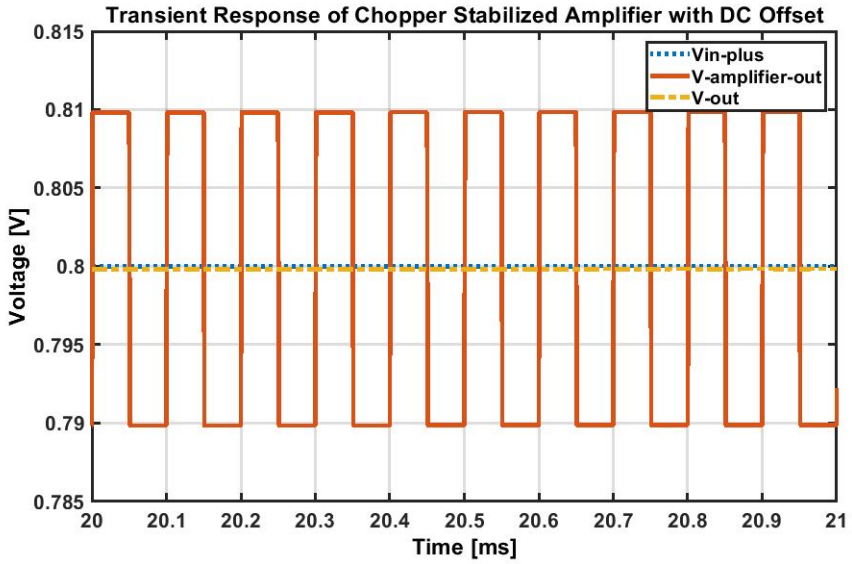


Figure 4.6: Transient Response of Chopper Stabilized Amplifier with DC Offset (Magnified)

Fig. 4.6 shows that the amplifier output obtained has a 10 mV ripple which is in sync with the demodulated output ripple given by AV_{OS} in section 2.1, where $A = 1$ in the designed closed loop unity gain configuration and $V_{OS} = 10$ mV, the applied DC input offset. It is important to note that despite the application of a 10 mV DC offset, the average output voltage of the chopper stabilized amplifier is maintained at 800 mV, as in the case of no offset. The ripples produced at this amplified output node can be filtered out using the same third-order low-pass filter as before, in order to obtain an output sine wave that mimics the input.

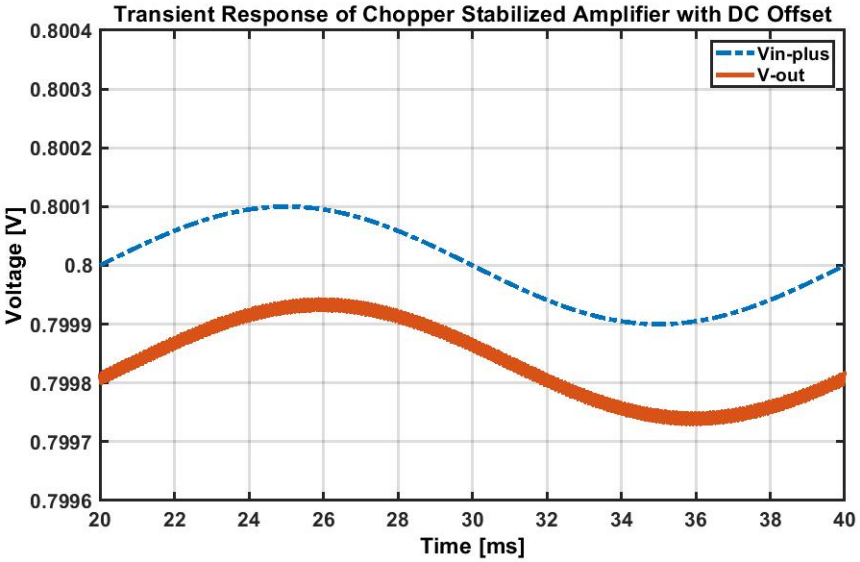


Figure 4.7: Transient Response of Chopper Stabilized Amplifier with DC Offset (Depicting Input and Output)

Fig. 4.7 shows the low-pass-filtered output voltage with respect to the applied input voltage. It can be seen that this agrees with the results depicted in Fig. 3.8 where the DC offset was 0 V. The final output voltage in Fig. 4.7 is independent of the 10 mV DC offset applied. Next, a parametric sweep is performed on the chopper stabilized amplifier. The DC offset is swept from 0 mV to 20 mV in linear steps of 5 mV. The input to the amplifier is kept constant for the entirety of the parametric sweeps and is depicted in Fig. 4.8. It is the same 100 μV sine wave over a common 800 mV DC, as used for the previous simulations.

Fig. 4.9 shows the output of the parametric sweep performed. It can be noted that the final low-pass-filtered voltage rises from 0 mV until 800 mV and maintains a constant average of 800 mV thereafter, the same as the input voltage applied, irrespective of the DC offset.

A closer look at these obtained output voltages in Fig. 4.10 shows how the sinusoids at the output overlap with each other around the constant DC input voltage, thereby seeming to be a single output waveform. This is in stark contrast to the results obtained from Fig. 4.3, where the average output voltage is dependent

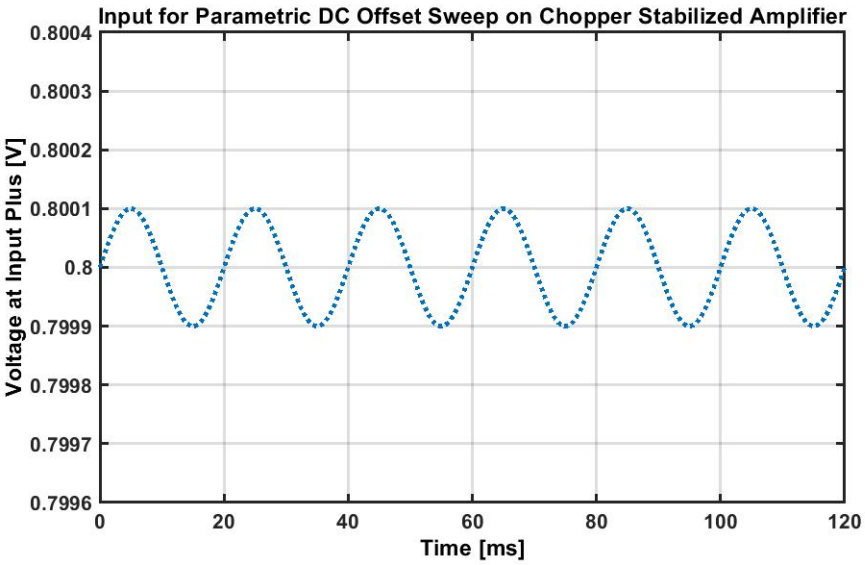


Figure 4.8: Input for Parametric DC Offset Sweep on Chopper Stabilized Amplifier

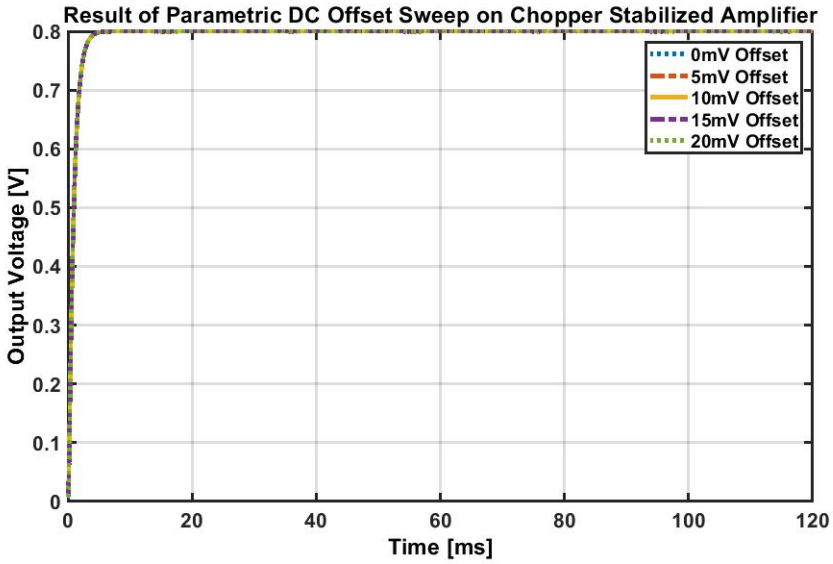


Figure 4.9: Result of Parametric DC Offset Sweep on Chopper Stabilized Amplifier

on the DC offset of the amplifier. This hints at the fact that no matter how much DC offset there is, the chopper stabilized amplifier output voltage produced comprises a ripple with magnitude equal to the gain of the amplifier times the DC offset. If this ripple is properly filtered out, an error-free amplified sine wave is obtained, as desired.

This section therefore verifies the claim that chopper stabilization works in the designed single ended amplifiers to combat any DC offsets that may be present at the amplifier input terminals. The final low-pass-filtered output is invariant to such DC offsets, hence justifying the wide-ranging applications of chopper

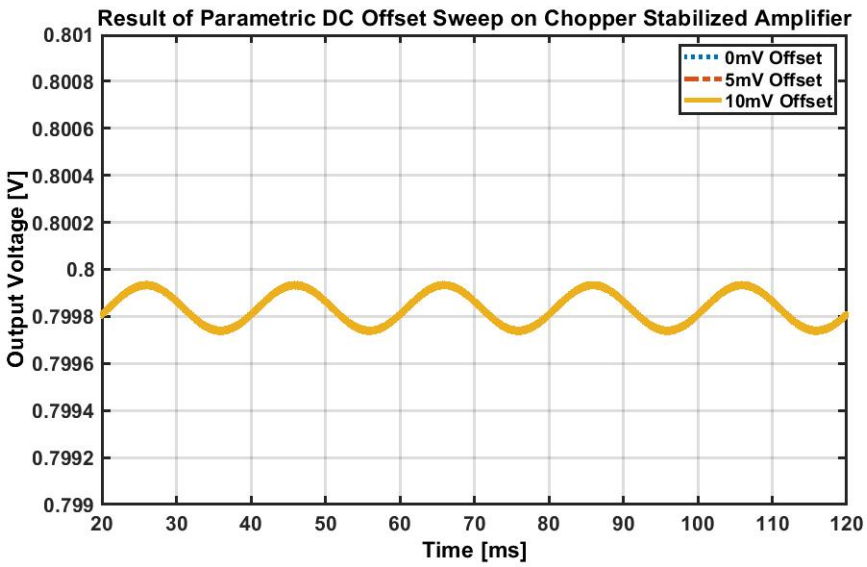


Figure 4.10: Result of Parametric DC Offset Sweep on Chopper Stabilized Amplifier (Magnified)

stabilization to reduce amplifier dependencies on DC offsets. It is important to note that the designed chopper stabilization based, single ended amplifier is fully functional in eradicating DC offsets and in preventing their propagation to the amplifier output voltages, just like in its existing differential counterparts.

Chapter 5

Effect of Noise on Amplifier Performance

5.1 Factors that Contribute to Noise

Noise, in contrast to offsets, occurs completely due to random errors. The flicker noise of a MOSFET at drain terminal is given by [18]

$$\overline{i_{nd,fn}^2} = \frac{K_f}{C_{ox}WL}\frac{g_m^2}{f} \tag{5.1}$$

which is the same as modeling it as a voltage source such that

$$\overline{v_{nd,fn}^2} = \frac{K_f}{C_{ox}WL}\frac{1}{f} \tag{5.2}$$

where C_{ox} is the oxide capacitance, and K_f is a process parameter whose value depends on the dimensions—width W and length L—of the transistor. The thermal noise in MOSFETs can be modeled as the drain current as shown in equation 5.3.

$$\overline{i_{nd,th}^2} = 4kT\gamma g_m \tag{5.3}$$

The same thermal noise can also be modeled as gate voltage, given by equation 5.4

$$\overline{v_{ng,th}^2} = \frac{4kT\gamma}{g_m} \tag{5.4}$$

The noise at the output of the chopper stabilized unity gain buffer can be calculated based on the noise contribution from individual devices. Assuming that the symmetric devices along branches are matched, the output noise can be written as shown in [16] by

$$\overline{v_{n,out}^2} = \overline{v_{n,out,th}^2} + \overline{v_{n,out,fn}^2} \tag{5.5}$$

$$\overline{v_{n,out,th}^2} = A_{DM}^2\left(\frac{16kT}{3g_{mN2}}\left[1 + \frac{g_{mP2}}{g_{mN2}} + \frac{g_{mN5}}{g_{mN2}}\right]\right) \tag{5.6}$$

$$\overline{v_{n,out,fn}^2} = A_{DM}^2 \left(\frac{2K_{fP}T}{(WL)_{N2}f} \left[1 + \frac{K_{fN}}{K_{fP}} \frac{(WL)_{N2}}{(WL)_{P2}} (\frac{g_{mP2}}{g_{mN2}})^2 + \frac{(WL)_{N2}}{(WL)_{N5}} (\frac{g_{mN5}}{g_{mN2}})^2 \right] \right) \tag{5.7}$$

where $K_{fN} = \frac{K_f}{C_{ox,N}}$ and $K_{fP} = \frac{K_f}{C_{ox,P}}$. A_0 refers to the differential gain of the folded cascode topology, as given by

$$A_{DM} \approx -g_{mN2} \left[g_{mN5} r_{dsN5} r_{dsN7} \parallel (g_{mP4} r_{dsP4} (r_{dsN2} \parallel r_{dsP2})) \right] \tag{5.8}$$

Similarly, the common-mode gain, A_{CM}, can be given as:

$$A_{CM} \approx - \left(\frac{2g_{mN2}}{1 + 2g_{mN2} r_{ds,N1}} \right) \left(\frac{1}{2g_{mN5}} \right) \tag{5.9}$$

Assuming matching between the symmetric devices, $CMRR$ of the folded cascode amplifier can therefore be written as:

$$\begin{aligned} CMRR &= \frac{A_{DM}}{A_{CM}} \\ &= \frac{1}{2} (g_{mN5}^2 r_{ds,N5} r_{ds,N7})(1 + 2g_{mN2} r_{ds,N1}) \end{aligned} \tag{5.10}$$

5.2 Performance Results

In the proposed implementation of chopper stabilization, as shown in Fig. 3.1b, an insight regarding the main contributors to noise can be obtained. Tables A.1 and A.2 include a noise summary of the individual noise contributors to the integrated output noise, without and with chopper stabilization, respectively. They are obtained by performing periodic steady state analysis and periodic noise analysis on the circuit from Fig. 3.3.

As anticipated, the most significant source of noise is the input pair of transistors ($N2$ and $N3$ from Fig. 3.1b). Table A.1 shows that they contribute 86.74% of the total integrated output noise in a regular amplifier. This is because any low-frequency errors or systematic mismatches seen at the input pair of the amplifier directly propagate through to its output, being further amplified by the gain.

The effect of the most significant amplifier noise contribution by the input pair is seen to be eradicated using chopper stabilization, as shown in Table A.2, where the noise contributed by the same differential input pair is now almost 0%. This is due to the fact that chopper stabilization works to reduce flicker noise of the input pair by modulating and demodulating the input, thereby allowing us to chop the low-frequency flicker noise of the input pair, added during the amplification process. Chopper stabilization also works to remove the flicker noise contribution of the pMOS transistors at the folding node.

It can be seen from the tables that the next big contributors to noise, after the differential input pair, are transistors $N5$ and $N4$. This is due to the current mirror flicker noise contributed by the two transistors which, as per Table A.2, contribute 88.92% of the remaining noise seen at the output. If this noise is removed, the next big contributors would be on the scale of thermal noise, which is too small to adversely affect the functioning of an amplifier.

The next big source of error is the transistors N4 and N5 from Fig. 3.1b. Since they form the current mirror that is directly connected to the output node, it is logical that after the input differential pair, these two transistors contribute the most noise to the output of the chopper stabilized amplifier. However, chopper stabilization can be put to use beyond the folded nodes in Fig. 3.1b.

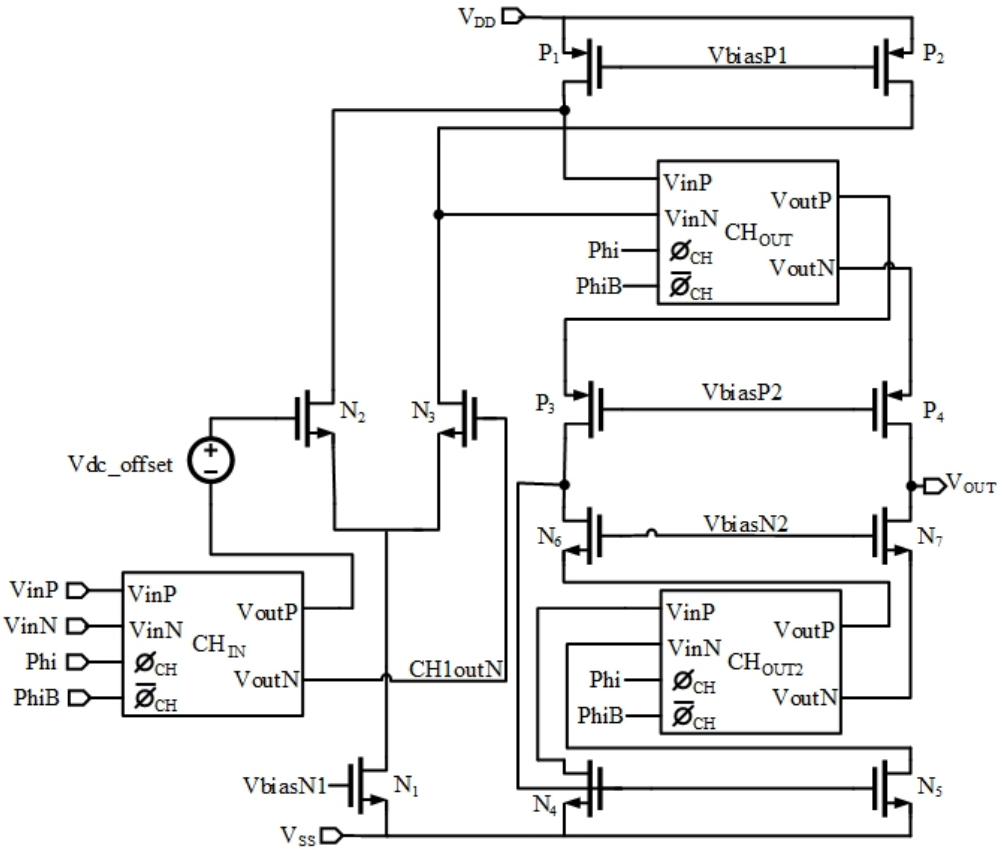


Figure 5.1: Circuit Diagram for Chopper Stabilized Amplifier with Three Chopper Switch Sets

Using guidance from [17], we can create a circuit as depicted in Fig. 5.1. This circuit too was verified for its functionality in the same way that the circuit from Fig. 3.1b was verified in Chapter 3 using transient and stability analysis. After successful verification, noise from this amplifier can be simulated using PSS and Pnoise analysis. Table A.3 shows the noise summary when the circuit from Fig. 5.1 is used in place of the circuit from Fig. 5.1. It is important to note that the biasing is kept the same, as shown in Fig. 3.1a.

It is evident from Table A.3 that the noise contribution due to the nMOS current mirror formed by N4 and N5 reduces to 0% when using two output chopper switches rather than just one. This means that N4 and N5 have 0% contribution to the overall integrated output noise from 1 Hz to 100 kHz.

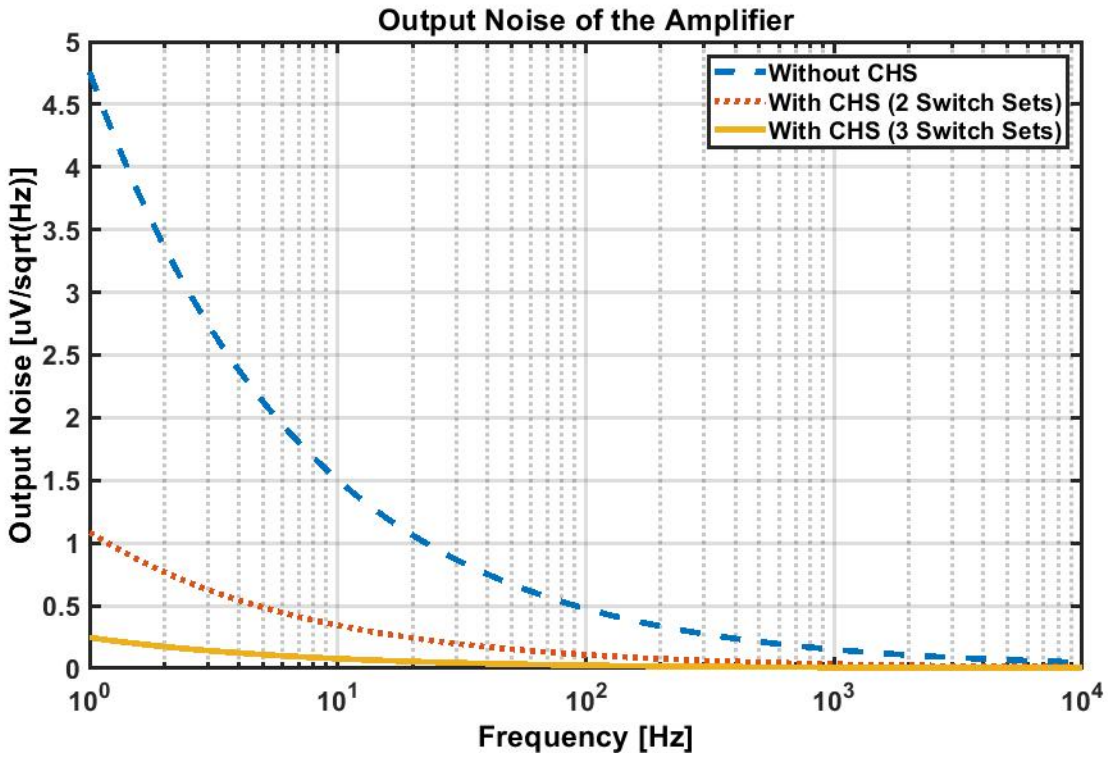


Figure 5.2: Output Noise of the Amplifier With and Without Chopper Stabilization

After performing PSS and Pnoise analysis on the proposed folded cascode amplifier unity gain buffer, it is possible to plot the integrated output noise. This experiment is performed for all three modes: (1) without chopper stabilization, (2) with chopper stabilization using two chopper switches, using the circuit shown in Fig. 3.1b, and (3) with chopper stabilization using three chopper switches, using the circuit shown in Fig. 5.1. The result of this simulation is shown in Fig. 5.2. It can be seen that the total noise at the output is 4.6 μV at DC when chopper stabilization is not employed. The shape is similar to that obtained when $(1/f)$ noise is dominant at low frequencies, and then it decays with increase in frequency until it hits the crossing frequency where the total noise is dictated thereafter by thermal noise.

It can be seen that the total noise at the output decreases to 1.1 μV when the same experiment of PSS and Pnoise analysis is performed on the chopper stabilized amplifier to obtain the second response shown in Fig. 5.2. This is a 76% decrease from the value obtained without chopper stabilization. This is a significant decrease caused by the reduction of flicker noise and DC mismatch contribution mainly due to the differential input pair.

Finally, it can be observed that the overall integrated noise at the output also decreases to 250 $\text{nV}/\sqrt{\text{Hz}}$ where the output noise with respect to frequency is plotted in Fig. 5.2, for third case, i.e., with chopper stabilization using three chopper switches. This is a reduction of 77.27% from the value with chopper stabilization using two chopper switches. When this result is compared to the output noise without chopper stabilization, as seen in the first case, a 94.5% decrease is observed.

It is therefore possible to conclude that chopper stabilization proves useful in order to reduce the flicker noise contribution of MOSFETs in single ended operational amplifiers. The simulations reported above verify that the overall integrated output noise reduces by 94.5% when chopper stabilization is used. Hence, the technique is recommended to combat the non-idealities caused by MOSFET flicker noise when designing ICs.

Chapter 6

Conclusion

This thesis describes a detailed study of chopper stabilization. It seeks to answer three vital questions about chopper stabilization: what it is, why it is needed and how it aims to achieve improved amplifier functionality. A chopper stabilized, single ended OpAmp is designed and verified for its output responses, against the non-stabilized amplifier in the same device configuration. It is established that the designed chopper stabilized, single ended amplifier generates an output voltage which is independent of the DC offsets at the input. Results from PSS and Pnoise simulations help conclude that chopper stabilization can eradicate the flicker noise contribution of MOSFETs to output noise, which itself is the most significant noise contributor of all individual devices that constitute the amplifier. Various noise-contributing devices have been discussed and attempts to combat their noise contribution are presented. Overall a 94.5% reduction in output noise is obtained by employing the technique of chopper stabilization, thereby justifying its widespread use in the world of analog IC design. Hence, this technique can be readily employed to build reliable single ended amplifiers that are immune to DC offsets and flicker noise, thereby finding use in a variety of ADC designs, temperature sensors and many other analog blocks.

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Appendix A: Noise Summary

This appendix contains the noise summary tables obtained during Pnoise analysis which is carried out to obtain performance results discussed in Chapter 5.

The 'parameter' values in Tables A.1-A.3 refer to the following individual noise contributors in a MOSFET:

- fn: flicker noise
- id drain-source resistance thermal noise
- rs: source parasitic thermal noise
- rd: drain parasitic resistance thermal noise

Table A.1: Noise Summary of Integrated Output Noise of Amplifier

Device	Parameter	Noise Contribution	Percentage of Total
/I0/N3	fn	1.03288e-10	43.38
/I0/N2	fn	1.03245e-10	43.36
/I0/P1	fn	7.6144e-12	3.20
/I0/P2	fn	7.36501e-12	3.09
/I0/N5	fn	5.91071e-12	2.48
/I0/N4	fn	5.90721e-12	2.48
/I0/N3	id	9.62298e-13	0.40
/I0/N2	id	9.61396e-13	0.40
/I0/P1	id	7.77675e-13	0.33
/I0/P2	id	7.52839e-13	0.32
/I0/N4	id	2.97586e-13	0.12
/I0/N5	id	2.97301e-13	0.12

Table A.1 Continued

/I0/P4	fn	2.54327e-13	0.11
/I0/P3	fn	2.44089e-13	0.10
/I0/N8	fn	8.9516e-14	0.04
/I0/P4	id	3.30682e-14	0.01
/I0/P3	id	3.18155e-14	0.01
/I0/N1	fn	1.52715e-14	0.01
/I0/N6	fn	1.41344e-14	0.01
/I0/N7	fn	1.25822e-14	0.01
/I0/P9	fn	6.05787e-15	0.00
/I0/N8	id	8.27181e-16	0.00
/I0/N6	id	7.06641e-16	0.00
/I0/N7	id	6.27955e-16	0.00
/I0/P9	id	5.88228e-16	0.00
/I0/N1	id	1.40722e-16	0.00
/I0/P6	fn	1.29033e-16	0.00
/I0/N10	fn	9.00512e-17	0.00
/I0/P7	fn	4.18098e-17	0.00
/I0/N12	fn	3.86799e-17	0.00
/I0/N9	fn	2.88271e-17	0.00
/I0/P8	fn	2.72292e-17	0.00
/I0/P5	fn	1.30766e-17	0.00
/R1	rn	1.1102e-17	0.00
/I0/P6	id	7.42682e-18	0.00
/I0/N11	fn	6.20087e-18	0.00
/I0/P7	id	4.15208e-18	0.00
/I0/P8	id	2.72267e-18	0.00
/I0/P5	id	1.20477e-18	0.00
/I0/N9	id	1.17853e-18	0.00
/I0/N12	id	1.07937e-18	0.00
/I0/N10	id	8.35156e-19	0.00

Table A.1 Continued

/I0/N11	id	2.50524e-19	0.00
/R3	rn	7.34402e-20	0.00
/R4	rn	3.40736e-21	0.00

Table A.2: Noise Summary of Integrated Output Noise of Chopper Stabilized Amplifier

Device	Parameter	Noise Contribution	Percentage of Total
/I0/N5	fn	4.53346e-12	44.48
/I0/N4	fn	4.52947e-12	44.44
/I0/N4	id	2.92825e-13	2.87
/I0/N5	id	2.92657e-13	2.87
/I0/P4	fn	1.94223e-13	1.91
/I0/P3	fn	1.86676e-13	1.83
/I0/N8	fn	6.18434e-14	0.61
/I0/P4	id	3.2458e-14	0.32
/I0/P3	id	3.12702e-14	0.31
/I0/N1	fn	1.05228e-14	0.10
/I0/N6	fn	1.02958e-14	0.10
/I0/N7	fn	9.21331e-15	0.09
/I0/P9	fn	4.19179e-15	0.04
/I0/N8	id	7.31095e-16	0.01
/I0/N6	id	6.6062e-16	0.01
/I0/N7	id	5.90173e-16	0.01
/I0/P1	fn	5.459e-16	0.01
/I0/P9	id	5.20722e-16	0.01
/I0/P2	fn	2.08312e-16	0.00
/I0/N1	id	1.23964e-16	0.00
/I0/P6	fn	9.13399e-17	0.00
/I0/P1	id	7.09963e-17	0.00
/I0/N10	fn	6.54446e-17	0.00

Table A.2 Continued

/I0/N3	fn	4.75234e-17	0.00
/I0/P7	fn	2.82485e-17	0.00
/I0/N2	fn	2.65709e-17	0.00
/I0/N12	fn	2.5538e-17	0.00
/I0/P2	id	2.39352e-17	0.00
/I0/N9	fn	1.90328e-17	0.00
/I0/P8	fn	1.79778e-17	0.00
/R1	rn	1.13304e-17	0.00
/I0/P5	fn	9.25672e-18	0.00
/I0/P6	id	6.72596e-18	0.00
/I0/N11	fn	4.09405e-18	0.00
/I0/P7	id	3.5889e-18	0.00
/I0/P8	id	2.29973e-18	0.00
/I0/N3	id	1.44758e-18	0.00
/I0/P5	id	1.09108e-18	0.00
/I0/N9	id	9.95461e-19	0.00
/I0/N12	id	9.117e-19	0.00
/I0/N10	id	7.76414e-19	0.00
/I0/N2	id	5.98583e-19	0.00
/I0/N11	id	2.11607e-19	0.00
/R3	rn	6.46656e-20	0.00
/R4	rn	3.51334e-21	0.00

Table A.3: Noise Summary of Integrated Output Noise of Chopper Stabilized Amplifier with Three Chopper Switch Sets

Device	Parameter	Noise Contribution	Percentage of Total
/I0/P4	fn	2.32397e-13	36.20
/I0/P3	fn	2.23344e-13	34.79
/I0/N8	fn	7.50977e-14	11.70

Table A.3 Continued

/I0/P4	id	3.29522e-14	5.13
/I0/P3	id	3.17441e-14	4.95
/I0/N6	fn	1.28955e-14	2.01
/I0/N1	fn	1.28047e-14	1.99
/I0/N7	fn	1.15274e-14	1.80
/I0/P9	fn	5.09013e-15	0.79
/I0/N8	id	7.56557e-16	0.12
/I0/N6	id	7.02931e-16	0.11
/I0/N7	id	6.27317e-16	0.10
/I0/P9	id	5.38858e-16	0.08
/I0/P2	fn	4.35265e-16	0.07
/I0/P1	fn	4.35265e-16	0.07
/I0/N1	id	1.28623e-16	0.02
/I0/P6	fn	1.10409e-16	0.02
/I0/N10	fn	7.94655e-17	0.01
/I0/P2	id	4.60468e-17	0.01
/I0/P1	id	4.60468e-17	0.01
/I0/P7	fn	3.39856e-17	0.01
/I0/N12	fn	3.28012e-17	0.01
/I0/N9	fn	2.44459e-17	0.00
/I0/P8	fn	2.30909e-17	0.00
/R1	rn	1.13778e-17	0.00
/I0/P5	fn	1.11892e-17	0.00
/I0/P6	id	6.92685e-18	0.00
/I0/N11	fn	5.25843e-18	0.00
/I0/P7	id	3.67949e-18	0.00
/I0/P8	id	2.51705e-18	0.00
/I0/P5	id	1.12367e-18	0.00
/I0/N9	id	1.08953e-18	0.00
/I0/N12	id	9.97855e-19	0.00

Table A.3 Continued

/I0/N3	fn	9.11355e-19	0.00
/I0/N2	fn	9.11354e-19	0.00
/I0/N10	id	8.03469e-19	0.00
/I0/N11	id	2.31603e-19	0.00
/I0/N5	fn	2.05944e-19	0.00
/I0/N4	fn	2.05943e-19	0.00
/R3	rn	8.13487e-20	0.00
/I0/N3	id	4.76169e-20	0.00
/I0/N2	id	4.76169e-20	0.00
/I0/N4	id	9.68682e-21	0.00
/I0/N5	id	9.68674e-21	0.00
/R4	rn	3.63285e-21	0.00