MICROMACHINING OF SINGLE CELL ARRAY FOR OXYGEN CONSUMPTION RATE ANALYSIS

A Thesis

by

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ABSTRACT

The Oxygen Consumption Rate of biological cells is an important parameter of cellular metabolism. In order to study the behaviour of cell populations, it becomes necessary to capture and store them in one location for analysis. Individual cell analysis within a cell group can provide useful information about the average response of the cell group, as well as identify outliers. Such analysis can be used to identify different groups of cells based on their oxygen levels. However, characterizing the individual cell response within a cell group is challenging since cell dimensions are on the order of a few micrometers. Conventional techniques, such as microtiter plates and flow cytometery, are unable to offer both the high temporal and the high spatial resolution that is required to characterize individual cells. Modern micromachining and microfabrication techniques, on the other hand, allow for the creation of devices that have dimensions that are on the order of a few micrometers. Through a series of thin film deposition, photolithography and thin film etching techniques, it is possible to create single cell trapping structures whose dimensions are only slightly larger than that of individual cells. The aim of this thesis is to create a process flow in order to fabricate such structures on a single crystalline silicon substrate using available micromachining techniques.

DEDICATION

I would like to dedicate this thesis to my family who have constantly motivated and supported me throughout the course of my studies.

ACKNOWLEDGEMENTS

I would like to express my deepest gratitude to my advisor, Dr. Jun Zou, for all his guidance and motivation throughout my study at Texas A and M University. I would like to thank him for providing me with the opportunity to be a part of his research group and work in his research laboratory. I would also like to thank all of my committee members, Dr. Kamran Entesari, Dr. C.B Su, and Dr.Tony Hsieh for their guidance and support throughout the course of this research. I also want to thank past and present members of Dr. Zou's research group for all of their advice, help and friendship during these years. Thanks also go to my friends and colleagues, and the department faculty and staff for making my time at Texas A and M University a great experience. Finally, thanks to my mother, father and sister for all of their encouragement and support throughout my life.

TABLE OF CONTENTS

Page

ABSTRACT ii

DEDICATION iii

ACKNOWLEDGEMENTS iv

TABLE OF CONTENTS v

LIST OF FIGURES vii

LIST OF TABLES ix

1. INTRODUCTION 1

   1.1 Micro-well Arrays for Single Cell Analysis 1
   1.2 Characterization of Oxygen Consumption Rate of Cells 2
   1.3 Motivation for Single Cell Array Fabrication for OCR Measurements . . . 3

2. OVERVIEW OF SILICON ETCH PROCESS 6

   2.1 Wet Etching 8
   2.2 Dry Etching 10
   2.3 Reactive Ion Etching 11
   2.4 Bosch Process 12
   2.5 Cryogenic Etching 14

3. OPTIMIZATION OF THE CRYOGENIC ETCH PROCESS 17

   3.1 Primary Etching Parameters 17
   3.2 Etch Sample Fabrication 20
      3.2.1 Silicon Acoustic Delay Lines 20
      3.2.2 Fabrication Process 21
   3.3 Etch Experiments and Results 23
   3.4 Conclusions 32

4. FABRICATION OF SINGLE CELL ARRAY ON SILICON SUBSTRATES . . 35

   4.1 Design 35

4.2 Fabrication Process Development 36
4.3 Fabricated Devices 39
4.4 Conclusion 46

5. CONCLUSION AND FUTURE WORK 47

REFERENCES 48

LIST OF FIGURES

FIGURE Page

1.1 Microwells that Trap Cell Groups on a Glass Plate with Built in Fluorescence Sensors for OCR Measurements. 3

1.2 Schematic of a Single Cell Array Substrate. 4

2.1 Wet Etching. 8

2.2 Tapering of Structures Due to Use of KOH Etchant. 9

2.3 Etch Steps. 10

2.4 RIE Chamber. 12

2.5 Bosch Process. 13

2.6 Room Temperature Bosch Process. Reprinted from [1] with Permission from Elsevier. 14

2.7 Cryogenic Process. 16

3.1 Oxford PlasmaLab RIE System. 18

3.2 Etch DOE. 19

3.3 Delay Line Receiving System : (a) Delay Line with a Single Receiving Transducer, (b) Signal before Entering the Delay Lines, (c) Ultrasound Signal with a Delay Time, (d) Ultrasound Signal Received by the Transducer: Reproduced from 'Micromachined Silicon Acoustic Delay Lines for Ultrasound Applications' by Zou et al, Used under CC BY Licence[27]. 21

3.4 Delay Line Fabrication. 24

3.5 Effect of Temperature on Etch Selectivity. 25

3.6 Effect of SF_6 sccm on the Etch Rate of Silicon. 27

3.7 Effect of O_2 on the Etch Rate of Silicon. 28

3.8 High Forward Power of 70 Watts Damaging the Hard Mask. 29

3.9 Varying Widths Due to Poor Sidewall Passivation. 30

3.10 Low Anisotropy Due to Poor Thermal Passivation. 32

3.11 High Anisotropy Obtained by Addition of Helium Backing. 33

3.12 High Anisotropy for Smaller Features. 33

3.13 Etch Profiles of Delay Lines Fabricated: (a) Second Set of Delay Lines with Varying Anisotropy, (b) Third Set of Delay Lines with Anisotropy 0.72, (c) Fourth Set of Delay Lines with Anisotropy 0.84, (d) Fifth Set of Delay Lines with Anisotropy 0.9. 34

4.1 Microwell Layers. 36

4.2 Microwell Design. 39

4.3 100 um Through Etched Features. 40

4.4 100 um Features with 1 um Thick Aluminum Deposited as a Base for Vertical Stacking. 41

4.5 Issues Faced During Fabrication. 42

4.6 Well Developed Features with Conformal Thickness for 10 um and 50 um SU8 Features. 44

4.7 First Stage of Alignment. 45

4.8 Final Device Structure with Aligned Features. 45

LIST OF TABLES

TABLE Page

3.1 RIE Recipe Table 1 27

3.2 RIE Recipe Table 2 31

3.3 RIE Recipe Table 3 31

1. INTRODUCTION

1.1 Micro-well Arrays for Single Cell Analysis

The Oxygen Consumption Rate (OCR) is used for the diagnosis of cellular meta-bolic status. OCR of cell populations can be used in medical screening, cancer research, drug developement and genetic studies among many others [2]. For instance OCR plays an imporatant role in identifying hypoxic tumor cells which are known to have a low oxygenation content (pO2 $<$ 10 mmHg). Hypoxia causes these cells to be resistant to radiation and drug treatment as well as known to cause metastasis [3]. Thus, finding out the OCR of cancer cells is a key tool in identifying different groups of cancer cells.

Typically cells have dimensions that are on the order of the few micrometers and the latest MEMS fabrication technologies can help create cell trappment structures for monitoring the activities of cell populations. Conventional techniques use mircrotiter plates and flow cytometry. Microtiter plates consist of an array of wells or tubes that are embedded in a plate. Each tube can hold a few milliters of liquid which contains a sample set of a cell group. Flow cytometery consists of a funnel like structure that allows cells to flow through a narrow channel. A laser beam or an electromagnetic wave is used to irradiate the a cell at a given instant in time and based on the spectral response the cell can be categroized into different groups. While microtitter plates can be used to monitor cells over extended periods in time it is difficult to monitor the cell to cell variations. Flow cytometry monitors indivdual cells but is not suitable for obtaining vaild statistical data since only one data point is available from a cell at a given time [4]. Hence it becomes imperative to create live cell arrays that can combine the spatial resolution of flow cytometry and the temporal resolution of microtitter plates so as to allow continous monitoring of indivdual cells [5]. These cell arrays can also be used for visual examination of the cells under a

microscope. Microwell structures fabricated on glass plates or polysterene can be used to create cell catchment areas using microfabrication techniques. Microwells consists of two vertically stacked chambers where the upper chamber is tapered for cell trapping and the a lower chamber is used to supply oxygen or nutrients to the trapped cells. These trapped cells can then be characterized for their OCR.

1.2 Characterization of Oxygen Consumption Rate of Cells

Current methods for measuring the overall OCR of a cell population are either electrical or optical.The OCR content of cells has been measured using numerous methods such as:

1. Oxygen flux in environment of cells
2. Optically detecting singlet of oxygen form its phosphorescence
3. Measuring pO2 using a CMOS based sensor
4. OCR Measurement Using Fluorescence Life Time via imaging.

Traditional electrical methods are widely used but have low sensitivity and face problems such as signal drift [6]. Recently optical methods have become more popular by using platinum based fluorophores whose fluorescence life time (FLT) can be altered by oxygen molecules [7]. The partial pressure of oxygen can be monitored by the FLT measurements [8] [9].

The cell population can be estimated by using a mircowell array. OCR measurements can be performed by creating a cell array substrate consisting of an array of microwells. Inside each microwell is an FLT sensor to measure oxygen. The cell arrays act as catchments or trapping structures. After capturing one or more cells the cover glass plate is placed on top of the substrate which holds the cells and the FLT of oxygen is monitored

by a microscope to estimate the OCR. Unlike the other methods mentioned above the FLT imaging method can be be performed in an oxygen depletion environment so that more accurate data can be obtained from individual cells[8] [9]. Fig 1.1 shows a traditional setup of microwells on a glass subsrate that is used to trap a group of cells.

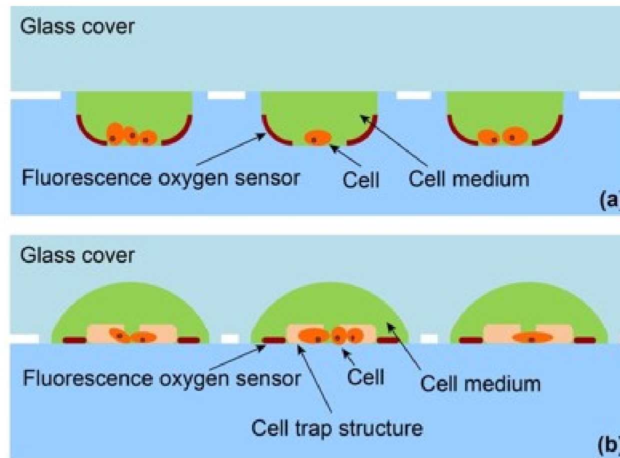


Figure 1.1: Microwells that Trap Cell Groups on a Glass Plate with Built in Fluorescence Sensors for OCR Measurements.

1.3 Motivation for Single Cell Array Fabrication for OCR Measurements

So far OCR measurements were performed on bulk cell populations. Recent studies have shown increasing evidence of cell to cell heterogeneity that need to be identified and hence measuring the average response of a cell population stimulus may not reflect well on single cell responses [10] [11]. Therefore conducting OCR measurements of single cells is critical to provide accurate graphical information about the cellular functioning in order to get more information about single cells as well as for gathering information about the entire cell population. To enable high throughput single cell OCR measurements a single cell array substrate suitable for OCR measurement needs to be developed. The array

should have a high density of cell placement which provides for a larger sample set while minimizing the overall chip size which makes the device compact and also reduces data acquisition time for the device. A high filling ratio of single cells minimizes voids. Single cell substrates can be developed to achieve good OCR measurements by isolating the FLT sensor from the cell trap thus ensuring good oxygen sealing capability. The single cell array can provide an oxygen limited diffusion environment that can be used to achieve high accuracy in OCR measurements. The single cell array can be fabricated using microfabrication processes which allow them to be manufactured in high volumes at lower costs. Fig 1.2 depicts single cell array arrays on a substrate. Each well has an upper chamber for cell trappment which is separated from a lower chamber for oxygen supply.

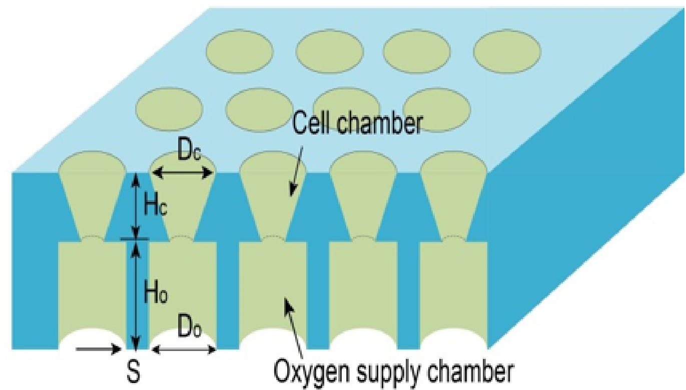


Figure 1.2: Schematic of a Single Cell Array Substrate.

Currently there are two ways of creating single cells - settling and trapping [12]. The settling approach is preferred since it has a high filling ratio and high density array of microwells. The dimensions of each microwell are such that the cells settle into the wells by themselves and the extra cells are washed away. It is possible to isolate single cells using this technique [13][14]. The trapping method is more versatile when it comes to trapping

different types of cells but its drawbacks include low density and higher chance of multi-cell trappment. Therefore, the cell settling method using a high density of microwells is gaining more traction when it comes to adopting a design technique for creation of single cell arrays. The goal of the thesis is to investigate and develop a process flow to fabricate a high density of single cell arrays onto a single crystalline silicon substrate using existing microfabrication and micromachining techniques.

2. OVERVIEW OF SILICON ETCH PROCESS

Silicon is the primary substrate material used in microelectronics and MEMS Devices [15].The etch processing techniques have been throughly developed for silicon and can be used to create a variety of devices such as pressure senors, accelerometers and micropumps using a number of different electrical and mechanical properties such as the piezoresistive effect or the resonance in single crystalline silicon [16] [17]. Bulk and Surface Micromachining are processes used to create microstructures in MEMS Devices. Bulk Micromachining is used to create microfeatures and membranes by selectively removing material from a substrate while surface micromachining is used to build microstructures by deposition and etching of different layers on top of a substrate [18] [19]. Bulk Micromachining refers to etching through the wafer from the back side in order to form desired structures and makes used of a hard mask to define the features while surface micromachining uses a suitable sacrifical layer that is eventually removed to create free standing structures. Many devices are fabricated using both technologies. Bulk micromachining is primarily used to create an array of features inside a silicon substrate by etching thorough and removing layers of silicon that make up the substrate.A hard mask is created on top of the silicon substrate inorder to define the features that need to be etched. Mask patterns created after photolithography can be used as an etch mask. These masks have to be resistant to the etchant that attacks silicon. The mask is generally made from photoresist, a thin film of metal or insulating material. Photoresist masks are known to have a limited temperature range and high and low temperatures are known to harm the resist. Also thicker photoresist is prone to cracking and not suitable for high aspect ratio structures. Thus it becomes imperative to use a hard mask during the etching of Silicon. Silicon Dioxide, Silicon Nitride, Aluminum and Chromium are some of the materials that are common hard mask

materials that can be grown or deposited on top of Silicon using standard micromachining techniques. Etching techniques are categorized as either wet etching or dry etching depending on the phase of the etchant. The etch processing and quality of the etched profile can be evaluated on the following three parameters.

1. **Etch Rate**: The Etch Rate is defined as the amount of time it takes to chemicall or physically remove layers of material or materials from a surface of a wafer during fabrication. Precise control of the widths of etched lines is required for a good etch profile. A fast etch rate achieves a desirable throughput of wafers that is needed for batch processing.It also lowers the risk of contamination that occurs when gases flow for a prolonged period of time inside a vaccum chamber [20].

$$Rate = \frac{Thickness\ before\ etch - Thickness\ after\ etch}{Etch\ Time} \tag{2.1}$$

2. **Selectivity**: Selectivity is the ratio of the etch rate of the target material being etched to the the etch rate of other materials above and below the target [20].

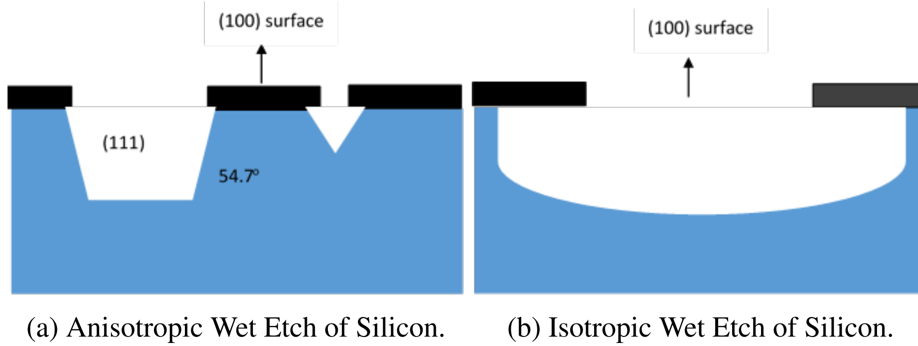
$$Selectivity = \frac{Etch\ Rate\ Material\ 1}{Etch\ Rate\ Material\ 2} \tag{2.2}$$

3. **Anisotropy**: Anisotropy of an etch is defined as uniformity of the etch in a particular direction. A number of MEMS structures require deep etching of Silicon to obtain high aspect ratio structures. Hence it becomes necessary to characterize the impact of etchants on the the materials being etched. Isotropic etchants attack the material in every direction while anisotropic etchants selectively attack the substrate in one direction in particular thus allowing the creation of high aspect ratio features [20].

$$Anisotropy = 1 - \frac{Bias}{2h}\ where\ Bias = \ d_{bottom} - \ d_{top} \tag{2.3}$$

2.1 Wet Etching

Wet etching is a liquid phase etching where the substrate is immersed in a bath of etchant and agitated in order to create features in the substrate. Wet etching is generally isotropic and has a selectivity depending on the crystallographic direction. It is often used in surface micromachining to remove sacrificial layers to create free standing structures. Anisotropic Silicon etchants such as KOH etch faster in one particular direction (1100 nm/min for (100) oriented wafer) while isotropic etchants attack the material in all directions at a slower rate (150 nm/min for (100) oriented wafer) [21] as depicted in Fig 2.1.



(a) Anisotropic Wet Etch of Silicon. (b) Isotropic Wet Etch of Silicon.

Figure 2.1: Wet Etching.

For KOH the etching plane the order of etch rate is given by (100) $>$ (110) $>$ (111) for the mentioned crystal plane orientations. When etching in the (100) direction the KOH etchant forms a 54.7^o angle with the base (intersection of the (100) and (111) planes) as the etch is not perfectly anisotropic. KOH is a non-toxic, economical and commonly used metal hydroxide silicon etchant that provides high Silicon etch rate and moderate Silicon Dioxide etch rate [22]. The rate of etching of Silicon Dioxide in standard KOH solution is around 15 nm/min which is significantly smaller in comparison to the Silicon

etch rate. However, KOH attacks Aluminum very rapidly (greater than 12000 nm/min) and this impedes its use in microfabrication processes [21]. TMHA is another anisotropic etchant that is widely used in the semiconductor industry. The etching rate of TMAH is comparable to KOH but the etching rate of the masking materials silicon dioxide and aluminum is considerably smaller [22]. The etch plane selectivity in the (100) direction is better in KOH than TMAH but TMAH provides better material selectivity with respect to Silicon and is hence very suitable for MEMS technologies.

Wet Etching however cannot create highly anisotropic structures that is required for certain MEMS devices like comb drives. In wet etching undercutting takes place at the extruded corners and curved edges of the mask pattern on the wafer surface due to the intersection of different crystalographic planes. Fig 2.2 depicts a profile obtained if KOH etchant were to be used to create 100 um features by etching through a silicon wafer with a thickness of 220 um. The features sizes at the start of the etch would have to nearly 4 times larger in order to obtain the desired 100 um features on the backside after the through etch. Thus the 54.7^o degree angle is detrimental to the formation of a dense vertical array of bulk etched features.

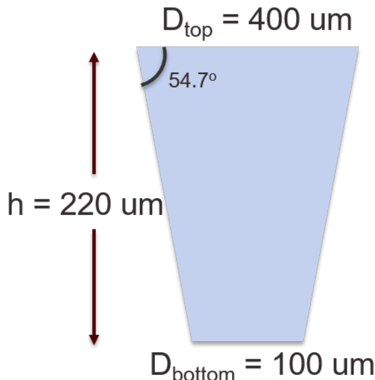


Figure 2.2: Tapering of Structures Due to Use of KOH Etchant.

While this is advantageous for creating suspended structures in a bulk etch it becomes detrimental to the creation of grooves and V shaped structures thus limiting the resolution [23]. Hence wet etching is typically not used while creating structures with small feature sizes. In the micro-electronics industry dry etching is generally used to create small feature sizes which require a higher degree of anisotropy.

2.2 Dry Etching

Dry etching is mainly a plasma based etching technique. The substrate is introduced into a chamber whose pressure is typically between 10 mT to 100 mT. Etch gases are passed into the chamber and their flow rate is controlled by a mass flow controller. These gases are then ionized to produce ions and free radicals which are then directed towards the substrate for etching.The reactants are transported through a boundary layer to the surface that is to be etched. The mass transport to the surface being etched is followed by a reaction between reactants and films to be etched. The by products that are formed are then diffused past the boundary layer and passed out of the etching chamber. Fig 2.3 depicts the dry etching steps.

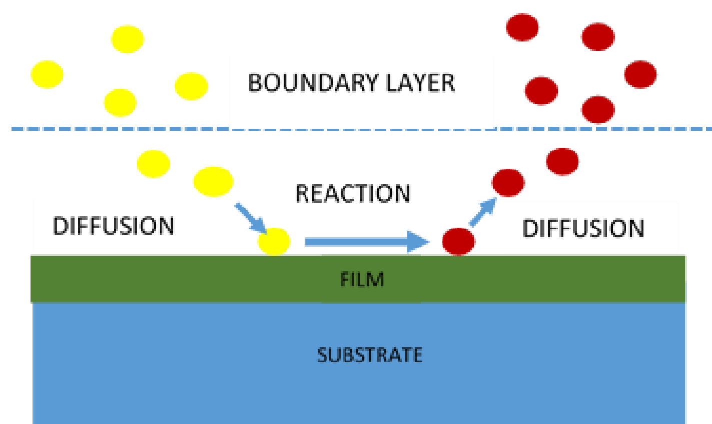


Figure 2.3: Etch Steps.

Plasma etching can be either isotropic or anisotropic. Anisotropy can be enhanced using a plasma technique known as Reactive Ion Etching.

2.3 Reactive Ion Etching

Reactive Ion etching is used to create vertical anisotropic structures by using a combination of Physical and Chemical etching mechanisms. It achieves directional etching by the reaction between active gas phase species and ion sputter etching [24]. A typical RIE system, as shown in Fig 2.4, consists of a vacuum chamber with a wafer plate attached to the bottom electrode. Gas is flown into the chamber and its flow rate is controlled with the help of mass flow controllers. A strong RF (Radio Frequency) field is applied to the wafer plates and this creates an oscillating electric field by ionizing the gas molecules and converting them to plasma by stripping away the electrons. The plasma develops a strong positive charge and is directed towards the bottom electrode during the negative half cycle. The oscillating field ensures that charge build up does not take place on any one electrode. Gases such as SF_6 and CHF_4 selectively attack one material in particular mimicking a chemical wet etch with the byproducts transferred away past the boundary layer. On the other hand gases such as Argon attack all materials present in the chamber once ionized and thus create a physical etching mechanism. In order to ensure that structures obtained are mechanically strong with near vertical sidewalls it is necessary to take selectivity, etch rate and anisotropy into consideration while formulating the recipe. The RF power creates Ions with high energy and the ICP system increases the Plasma Density. SF_6 is used commerically to etch away silicon. SF_6 gas on ionization creates Fluorine Free Radicals and Fluorine Ions. As mentioned previously RIE systems have two etching mechanisms - a reactive type and a physical type. The Fluorine Radicals react with Silicon to form the byproduct SiF_4. The Fluorine Ions on the other hand are responsible for a physical etch. High RF power causes the Flourine ions to bombard the hard mask which protects the

pattern, thus reducing selectivity and anisotropy. Also reactive ion etching is not very suitable for deep etching of Silicon since it creates ballooning and trenching problems which make it impossible to create high aspect ratio structures with smooth side wall profile [25]. Hence it becomes imperative to create a process that can etch through silicon to create high aspect ratio structures.

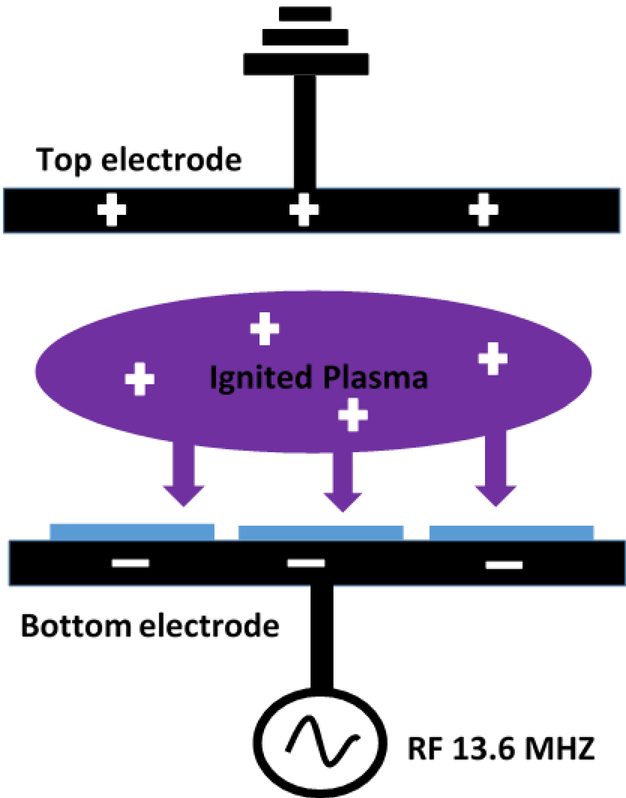


Figure 2.4: RIE Chamber.

2.4 Bosch Process

Deep Etching in MEMS Fabrication is obtained through two processes - Bosch Process and Cryogenic Etching. The Bosch Process uses sidewall passivation inorder to protect the sidewalls while plasma chemistry is used to etch the bottom layers to create vertical

anisotropic structures. The Bosch process, as depicted in Fig 2.5, can be described as consisting of sequential etching and passivation steps using C_4F_8 for passivation and SF_6 for etching [26].

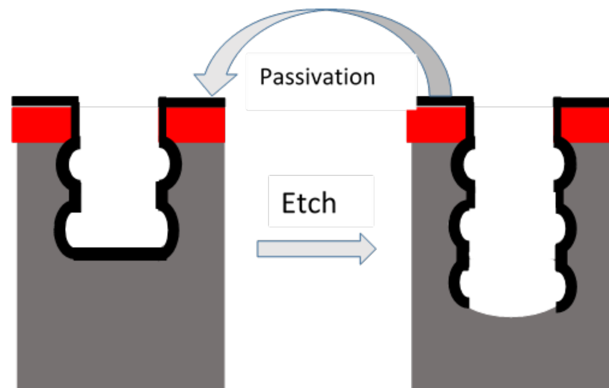
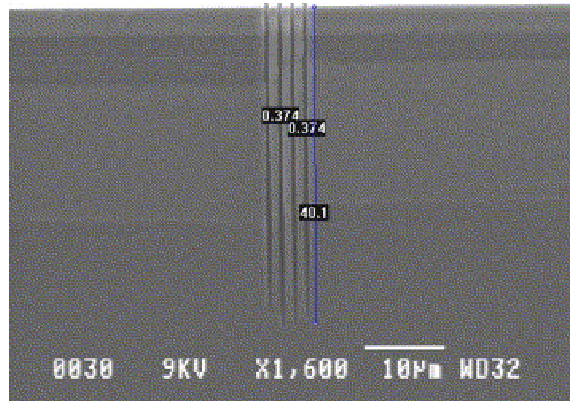


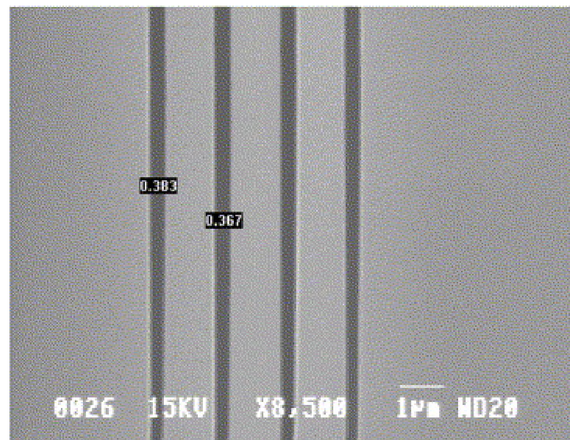
Figure 2.5: Bosch Process.

The Bosch Process can help fabricate structures with aspect ratios as high as 107:1. Fig 2.6 depicts the quality of a bosch etch. The problems associated with deep etching are mitigated and high aspect ratio structures can be obtained. It can be used to create vertical comb drive structures for capacitive sensing in accelerometers, gyroscopes and microscanners. The Bosch Process creates high aspect ratio microstructures with a high flexibility of wiring while having an etch rate greater than 17 um/min [27]. However a major drawback is its limited etch uniformity [28] and though it's surface roughness of features is better than isotropic wet etchants [29] there are still notches that are formed on the sidewall that can impede device performance. High aspect ratio structures that require a deep etch through a Si wafer require an etch depth of 300 um or more. The etch rate reduction for high aspect ratio structures results in buildup of polymer since the attack of ions on the sidewalls due to ion bombardment reduces. This results in negative profiles that increase roughness. Additionally the Bosch process requires control of alternating gas

flow into the chamber which increases the complexity of the system and requires expensive equipment for process control. [30].



(a) Deep Etch of Silicon.



(b) Detailed View Showing Aspect Ratio of 107.

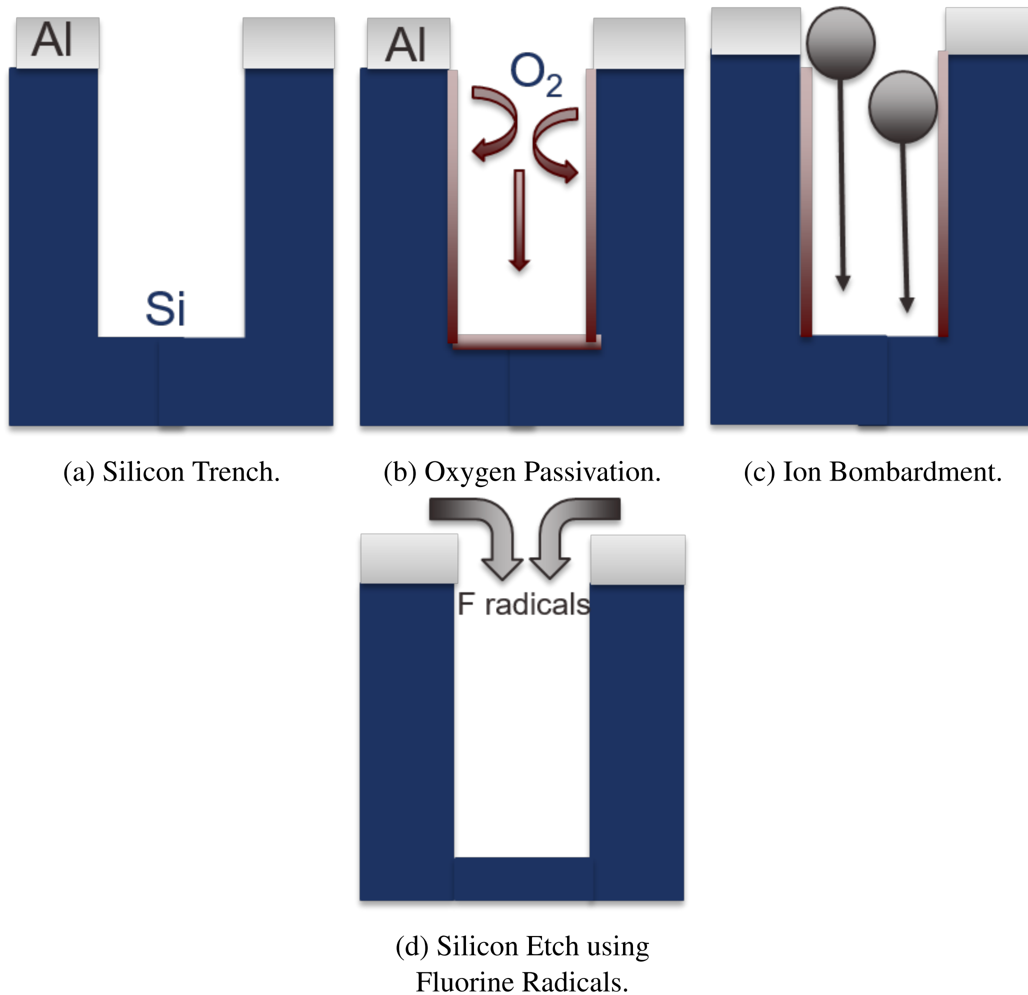
Figure 2.6: Room Temperature Bosch Process. Reprinted from [1] with Permission from Elsevier.

2.5 Cryogenic Etching

Though the Bosch Process is the most popular method to create high aspect ratio vertically etched structures in silicon it is an expensive process that is complicated due to the need of controlling the etching and polymer passivation in an alternate manner. A viable

alternative is the use of a cryogenic process to obtain good profile control at moderate etch rates. This can be done using an RIE chamber with ICP backing. As mentioned earlier the presence of an ICP system helps produce a large number of free radicals without generating ions that will produce high energy. Cryogenic cooling improves the selectivity of Silicon etching with respect to the mask material. The etch rate of Silicon remains constant at low temperatures while that of the mask materials such as Silicon Dioxide, Photoresist and Aluminum reduces significantly. Tachi et al showed that the temperature dependancies on the etch rate of a Siilcon and Silicon Dioxide changes drastically at -100 ^oC. They observed that the etch selectivity of Silicon was more than 30 over an AZ 1350J film mask or Silicon Dioxide film mask. [31] In order to get vertical anisotropic structures O_2 gas in added to the SF_6 mixture. The O_2 gas passivates the sidewalls and the bottom surface since O_2 reacts readily with Silicon to form Silicon Dioxide. The Fluorine ions that are created by the RF system attack the bottom surface of the structure physically etching away the Silicon Dioxide at the bottom. Since these Ions have high Kinetic Energy and the mean free path of the system is high, these Ions move towards the substrate (bottom electrode) in a vertical manner and leave the Silicon Dioxide on the side walls intact. Once the Silicon Dioxide on the bottom surface is eroded by the physical etch the Fluorine radicals take over and etch away the Silicon selectively leaving the sidewalls intact. Thus a cryogenic Bosch process can be developed to create through holes in silicon that have a high anisotropy without the complexity of alternating gas flow that is needed for polymer passivation at room temperature. Also the sidewalls are smoother and contouring and notching is much less than a standard Bosch process, though the etch rate is considerably smaller.

Equations 2.4 2.5 2.6 below describe the etch chemistry while Fig 2.7 gives a description of the Cryogenic Process.



(a) Silicon Trench. (b) Oxygen Passivation. (c) Ion Bombardment.

(d) Silicon Etch using Fluorine Radicals.

Figure 2.7: Cryogenic Process.

$$Si + O_2 = SiO_2 \tag{2.4}$$

$$SF_6 + e = SF_5 + F + e \tag{2.5}$$

$$Si + 4F = SiF_4 \tag{2.6}$$

The goal of etch processing to create anisotropic structures in silicon devices in order to fabricate a high density of bulk etched arrays in a silicon substrate.

3. OPTIMIZATION OF THE CRYOGENIC ETCH PROCESS

In order to micromachine a dense array of structures onto a silicon substrate it becomes necessary to optimize the dry etch process in order to create small feature sizes (less than 150 um) that possess a high anisotropy after etching through a silicon substrate. In order to test and optimize the etch processes silicon delay lines with widths ranging from 500 um down to 80 um were fabricated using a single crystalline silicon substrate. This section explores the developement of an optimized etch process to fabricate the Silicon Delay Lines. Special emphasis is laid on selectivity and anisotropy since vertical silicon sidewalls are essential for the delay line to pass the pulsed ultrasound signals without much attenuation. The etch process developed for the delay line fabrication can be used as proof of concept to bulk etch the silicon substrate with a large number of small circular features that possess a high degree of anisotropy which is a requirement for the creation of a high density of single cell arrays.

3.1 Primary Etching Parameters

Texas A and M's fabrication facility - Aggie Fab has a dry etching bay with an Oxford PlasmaLab ICP 100 ICP Unit shown in Fig 3.1. The system provides seperate RF and ICP generator which provide seperate control over ion energy and ion density thus allowing for high process flexibility. The system has a vacuum load lock and a process chamber which are isolated from each other. A roughing pump is used to adjust the process pressure between 10 mT -100 mT. A number of gases are provided for etch purposes. $SF6$, $CHF3$ are the gases that are involved in a chemical etch mechanism while Argon and Oxygen are known for their physical etch characteristics.

The RF power which is used to generate kinetic energy in Ions can be varied between 10 Watts - 150 Watts while the ICP which is used to increase ion density can be varied

Figure 3.1: Oxford PlasmaLab RIE System.

between 0 Watts - 2000 Watts. The RIE system can be cooled down to -150 ^oC using liquid nitrogen. The wafer chuck inside the system also provides for helium assisted backing for the sake of better thermal distribution. The creation of the delay lines requires a clean repeatable etch with good structural stability. Hence it becomes important to characterize the system with respect to the three important etching parameters - etch rate, selectivity and anisotropy. The thermal passivation, ion energy and ion directionality, the surface passivation and the formation of free radicals are the intermediate factors that control the etch quality. Thus the gas flow through the chamber, the pressure, the system temperature and the RF/ICP power are knobs that can be controlled and modified by a process engineer in order to get desired etch results.

Each one of these paramters affects the etch performance as explained in Fig 3.2.

The Fluorine free radicals attack the substrate in the manner of a chemical etch. The SF_6 gas flow through the system and the Inductively Coupled Plasma that creates a high

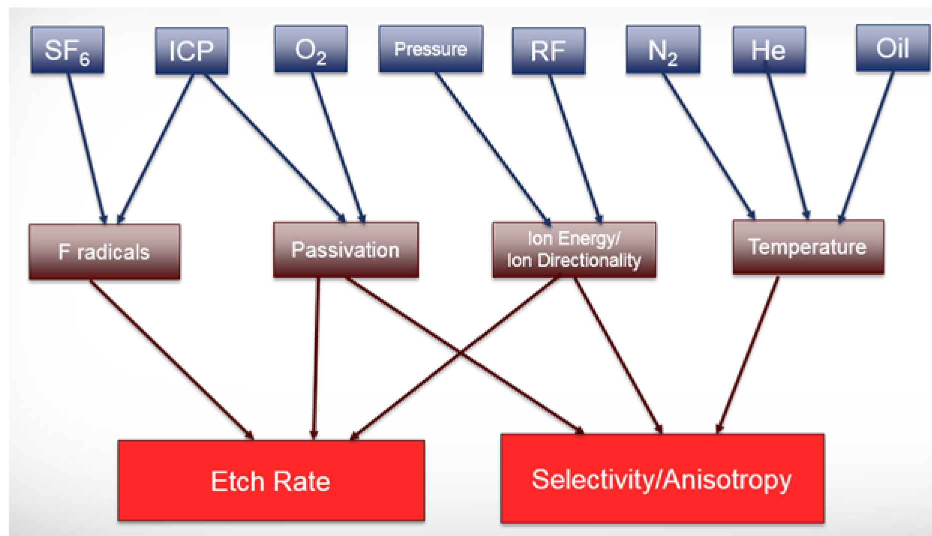


Figure 3.2: Etch DOE.

density of ions are the parameters that are responsible for the creation of the Fluorine free radicals that etch away silicon. The passivation layer creates silicon dioxide around the sidewalls and the base of the etched profile. Thus the amount oxygen that flows through the system plays the most crucial role in the formation of the passivation layers. The Ion Directionality and Ion Energy are dependent on the Process Pressure and the RF Power. The RF power ignites the plasma and creates the ions with kinetic energy stored in them. The greater the kinetic energy, more is the directionality of the physical etch. The process pressure should ideally be as low as possible to increase the mean free path which will cause the ions to move vertically downwards without bouncing off other atoms that might be present in the chamber. However there is tradeoff with the etch rate. A lower process pressure would be more directional but the etch rate would be low. The Nitrogen gas cools down the system to desired temperatures which affects the selectivity and anisotropy of the etch while the helium backing and the use of oil between the substrate and the carrier wafer causes the heat that builds up due to excessive ion bombardment to dissipate around the substrate creating uniform temperatures around the wafer chuck. Each of these process

parameters has to be characterized for the Oxford PlasmaLab system inorder to obtain a good etch profile.

3.2 Etch Sample Fabrication

3.2.1 Silicon Acoustic Delay Lines

In order to achieved high imaging resolution and speed large transducer arrays and Data Acquisition Systems are needed which create a complex and expensive Ultrasound Imaging Setup. To address this issue ultrasound receiving systems using acoustic delay lines can be created in order to replace the array of transducer elements. Each delay line receives a signal and introduces an appropriate delay into the signal. A single transducer at the end of the channel receives these time delayed signals sequentially. Thus, a delay line system converts parallel signals into single channel serial signals and thus reduces complexity of the system. Fig 3.3 shows the manner in which the delay lines converts the parallel signals into a serial form by introducing a time delay which can be analyzed by a single transducer [32].

Silicon is used for delay line material since it has extremely low attenuation in the MHz range, is mechanically strong and can be easily fabricated using micromachining. The dimensions of the delay line affect the transmission of the signal. In order to operate at center frequency of 2.25 MHz the dimension of the delay line would have to be less than 3.7 mm. Since the acoustic velocity of silicon is high the delay lines also have to be long inorder to achieve sufficient delay time in each channel. Hence curved or coiled structures have to be fabricated to satisfy the length requirements as well as remain compact in size. The delay lines fabricated in this work have dimensions between 500 um to 80 um and substrate thicknesses between 250 um -100 um. In order to maintain signal fidelity through the delay line it is essentail that the edges of the structure remain consistent and whole, and are not jagged or broken. Also the profile width needs to be consistent and the

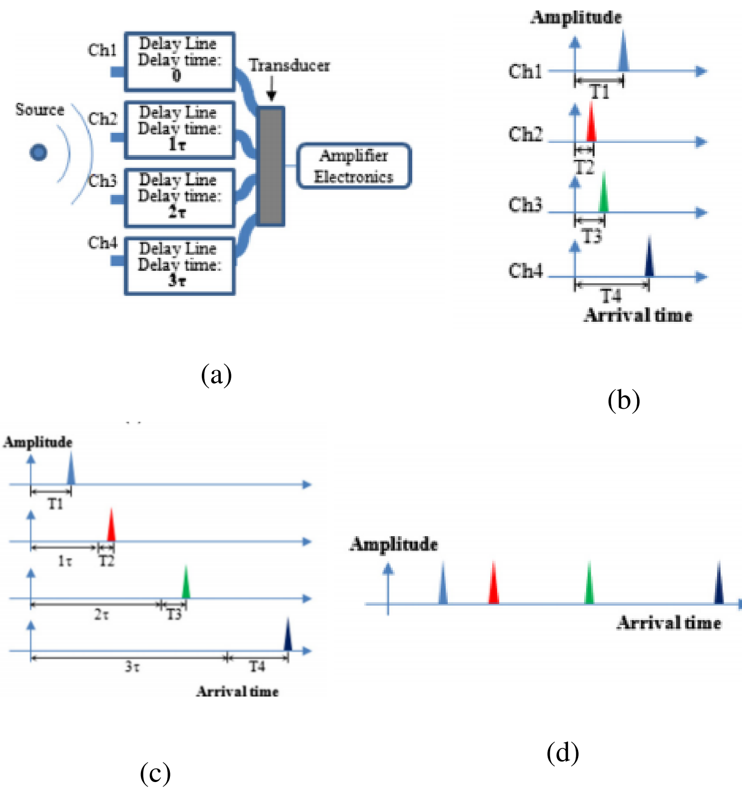


Figure 3.3: Delay Line Receiving System : (a) Delay Line with a Single Receiving Transducer, (b) Signal before Entering the Delay Lines, (c) Ultrasound Signal with a Delay Time, (d) Ultrasound Signal Received by the Transducer: Reproduced from 'Micromachined Silicon Acoustic Delay Lines for Ultrasound Applications' by Zou et al, Used under CC BY Licence[27].

top and bottom sufaces should remain intact. Thus it becomes essential to obtain a good anisotropic etch profile with high selectivity in order to achieve desired results. The motivation of the fabrication process was to create coiled and straight structures with smooth vertical side walls using dry etching.

3.2.2 Fabrication Process

Selecting the right type of silicon substrate is also critical to the fabrication process. It was decided to use undoped, double side polished silicon that is either 3 or 4 inches in diameter. The thickness of the silicon used was between 200 - 250 um to propagate a 2.2

MHz ultrasound signal through the channel. The thickness of the wafer can be reduced to propagate signals with higher frequency.

1. The first step involves cleaning a Double Side Polished silicon wafer in a Piranha solution to remove contaminants on the surface and obtain a clean hydrophobic surface. Piranha is a mixture of sulfuric acid(H_2SO_4) and Hydrogen Peroxide in a 3:1 ratio. The wafers are immersed in this bath and soaked for 15 minutes. They are then rinsed in DI water and dry baked in a convection oven for 5 minutes.

2. The wafer samples were placed in an e beam evaporator to deposit a 400 nm of Aluminum. E beam evaporation was chosen for growing the thin Aluminum film since it creates good quality film at thicknesses greater than 100 nm.

3. Deposition process is then followed by a patterning process. Photoresist AZ 5214 is spin coated onto the substrate. The spin speed is around 4000 rpm and the spin speed time is 40 seconds. The film thickness obtained is close to 1.4 um. The substrate and photoresist are then softbaked at 120 ^oC for 2 minutes on a hot plate. An L-line MA6 Karl Suss mask aligner is used to expose the photoresist to Ultra Violet light at an intensity of $90mJ/cm^2$. The film is then immersed in AZ 1:1 Developer solution and gently shaken for 40 - 45 seconds to reveal the pattern.

4. The regions that were exposed to the UV light were developed to reveal the underlying Aluminum pattern while the non exposed regions are unaffected. The patterned photoresist is then hardbaked in an oven at 135 ^oC . A few nanometers of residual resist often remains at the bottom of the exposed region. An O_2 ashing recipe is used to the remove the resist polymer in a Reactive Ion Etching chamber.

5. The Aluminum coating is now patterned by immersing the substrate in Aluminum etchant. The etchant attacks Aluminum selectively leaving the photoresist and sil-

icon unaffected [21]. Some undercutting of Aluminum is observed but that can mitigated by adjusting the mask design to take such factors into consideration. The Aluminum etchant is heated slightly on a hotplate to facilitate faster etching. However it should be ensured that the etchant does not start bubbling due to excessvie heating since it can cause the film to start peeling. If heated properly it takes around 4 minutes to reveal the underlying Silicon layer.

6. The pattern is observed under a microscope to ensure that there is no residual Alumimum. During the developement process care should be taken to ensure no scratches appear on the surface of the Aluminum film, especially in regions where the pattern is being created. This will cause the structure to be comprimised while etching and should thus be avoided at any cost. Once the Aluminum has been patterened the substrate is then placed in the RIE chamber. SF_6 gas is used to etch away the exposed silicon substrate while Aluminum acts as a hard mask during the fabrication process.

Fig 3.4 depicts the process flow for the fabrication of the delay lines.

3.3 Etch Experiments and Results

In order to obtain vertically etched coiled structures for the delay lines it was imperative that a thorough process characterization of the mask materials and silicon be performed in the RIE chamber. The aim of this process characterization was to select a suitable hard mask which would transfer the pattern onto a silicon substrate without being affected by the etch recipe that was being used to etch away silicon. Silicon was introduced into the chamber at room temperature and the effect of SF_6 and O_2 gas plasma was observed on potential mask materials such as Silicon Dioxide, Aluminum and Chromium at different temperatures. The forward power was kept at 60 Watts and ICP at 1000 Watts which are the recommended values according to the Lab manual for the Oxford PlasmaLab

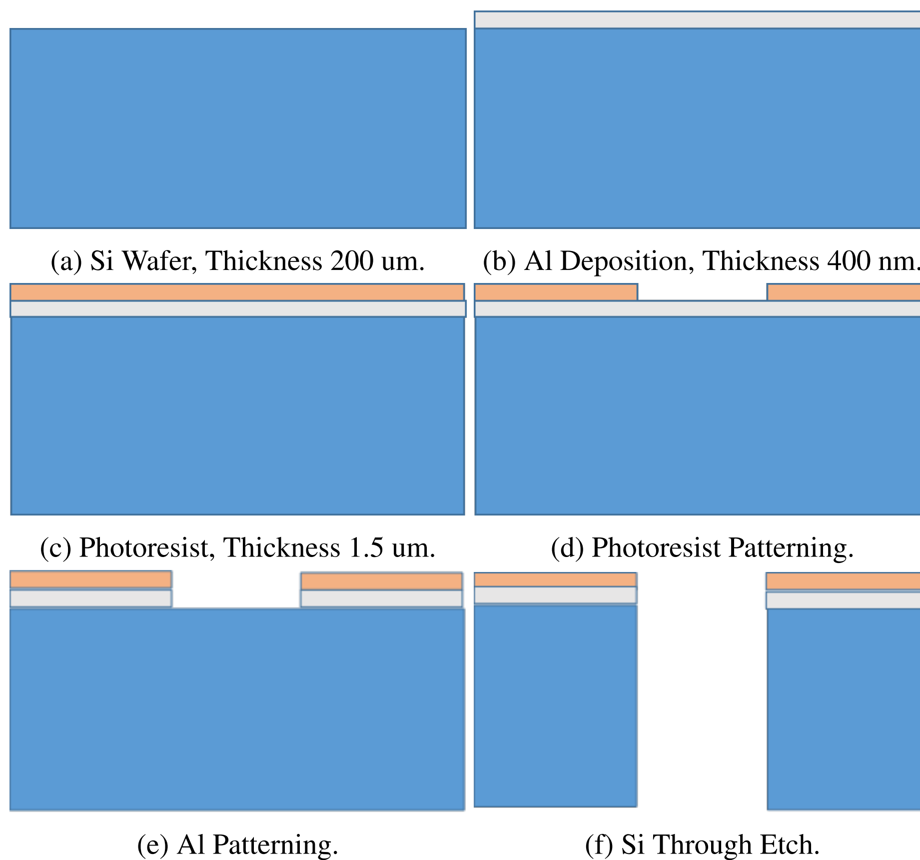


Figure 3.4: Delay Line Fabrication.

100 machine. Aluminum, Silicon Dioxide and Chromium were deposited onto a silicon substrate and introduced into the chamber to observe the effect of the temperature on the etch rates. Silicon Dioxide was deposited using a PECVD machine. The maximum thickness upto which a conformal consistent Silicon Dioxide film can be obtained from the system is around 1.5 um. We deposited around 1.2 um of the same. An e beam evaporator was used to deposit Aluminum and Chromium on a sample of Single crystalline Silicon wafers. The thicknesses for the Aluminum were 400 nm and 200 nm respectively since characteritzation of the e-beam's deposition showed that consistent good quailty conformal film can be obtained at the mentioned thicknesses for the two films. The samples of Bare silicon, Silicon with Silicon Dioxide, Silicon with Aluminum and Silicon with

Chromium were introduced into the RIE chamber and the thicknesses were monitored using a Dektak Profilometer which offers a vertical resoultion of 5 Angstrom if the step size is greater that 0.1 um wide though previous experiments have shown that the accuracy is more consistent at the order of a few nanometers. Pieces of Tape 2 mm x 2 mm in dimension were plastered at different locations on the samples so as to protect the underlying layers from the etch. It had been previously observed that the tape holds well for extended periods of time during the etch mechanism and is often used to hold the sample wafer inplace over a carrier wafer. The samples were introduced in to the chamber at different process temperatures. The process would run at intervals of 5 minutes in order to observe if any change in thickness had taken place. If there was no observable change then the process time would be increased gradually so as to observe the change in thickness.

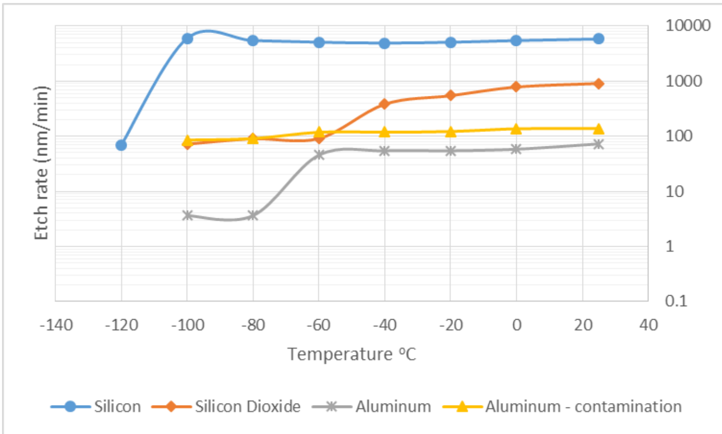


Figure 3.5: Effect of Temperature on Etch Selectivity.

It was observed that while the etch rate of silicon remains constant at around 5.8 um/min while there is a noticeable drop in the etch rates of silicon dioxide and aluminum. Chromium would easily crack due to the ion bombardment and hence is not a suitable material for a hard mask. The selectivity of Silicon over Silicon Dioxide increased by a factor

of 12 from 25 ^oC to -100 ^oC while the selectivity of Silicon over that of Aluminum was even better and increased by a factor of 20. The 400 nm of Aluminum held well and the surface did not look contaminated and was etched only a few nanometers. However care must be taken to ensure that the RIE chamber is cleaned with oxygen ions before starting every etch cycle using a O_2 plasma chamber clean. The Aluminum's selectivity degrades considerably if the chamber is unclean and it gives away much faster. Since we wish to etch away at least 250 um of silicon it would take nearly an hour to do so and even an etch rate of a few nanometers per minute (around 80 nm/min in the case of a contaminated chamber) would erode the thin Aluminum hard mask in a matter of a few minutes. The Fig 3.5 indicates that given a clean RIE chamber a 400 nm layer of aluminum acts as a good hard mask and can withstand an etch time of greater than 60 minutes.

The SF_6/O_2 ratio plays an important role in creating the vertical sidewalls. The O_2 provides sidewall passivation by readily combining with the Silicon to form Silicon Dioxide. The Ions that are formed during the etch process have a high kinetic energy and attack the surface of the carrier in an anisotropic manner. Thus the bottom of the trench gets plowed away while the sides remain intact. The Fluorine radicals that etch away the silicon selectively can now attack the exposed layer. If the O_2 gas flow is too high then the thickness of the passivation Silicon Dioxide layer being formed will increase. This will increase the etch time considerably. Hence it was imperative to obtain a SF_6/O_2 gas flow ratio that gives a good etch rate along with high anisotropy. Coiled structures around 500 um wide were patterned onto an aluminum hard mask. These structures were then introduced into an RIE chamber, first to observe the effect of forward power and SF_6 gas flow rate on the etch rate of silicon, and then to observe the effect of the introduction of oxygen into the gas feed.

Fig 3.6 shows that the increasing the forward power from 10 Watts to 60 Watts increases the etch rate but the effect of the SF_6 concentration on the etch rate is much more

prominent. A gas flow rate of 90 sccm can give a good etch rate at lower forward Power. We desire the forward power to be as low as possible since the ions would have lower energy and not bombard the hard mask or sidewalls as strongly as they would with a higher forward power.

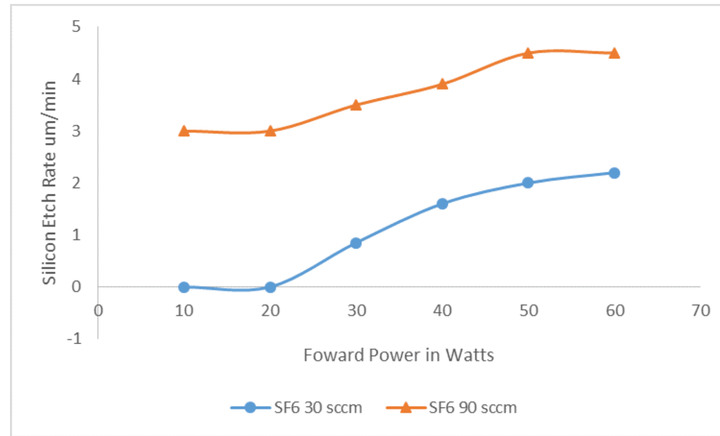


Figure 3.6: Effect of SF_6 sccm on the Etch Rate of Silicon.

Fig 3.7 shows the effect of the amount of oxygen in the gas feed. The aim of the process characterization was to obtain the highest possible O_2 content in the feed without drastically affecting the etch rate of silicon. Fig 3.7 shows that an $SF_6 : O_2$ ratio is around 3:1 ensures a good etch rate of silicon is obtained for a forward power of 30 Watts and an ICP of 1000 Watts.

Table 3.1: RIE Recipe Table 1

Parameter	Values
SF6/O2	75/10 sccm
RF/ICP	70/1000 W
Process Pressure	15 mT
Temperature	-100 C

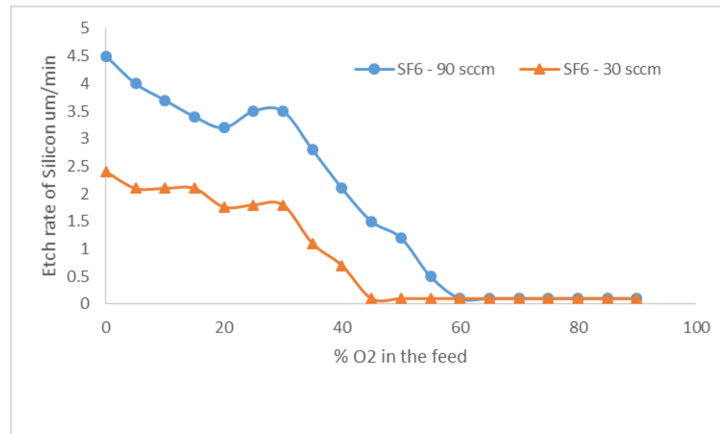


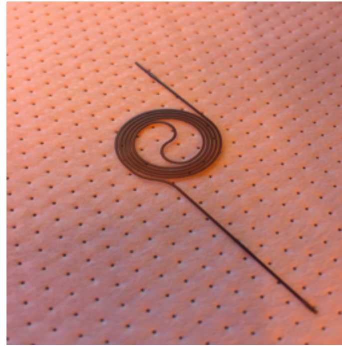
Figure 3.7: Effect of O_2 on the Etch Rate of Silicon.

The first set of delay lines that were fabricated used a forward power of 70 Watts and an SF_6 : O_2 ratio of 7:1. It was observed that the hard mask was damaged due the high forward power. Fig 3.8 shows the aluminum hard mask being damaged by excessive forward power while Table 3.1 mentions the RIE recipe used to obtain the first set of coiled structures.

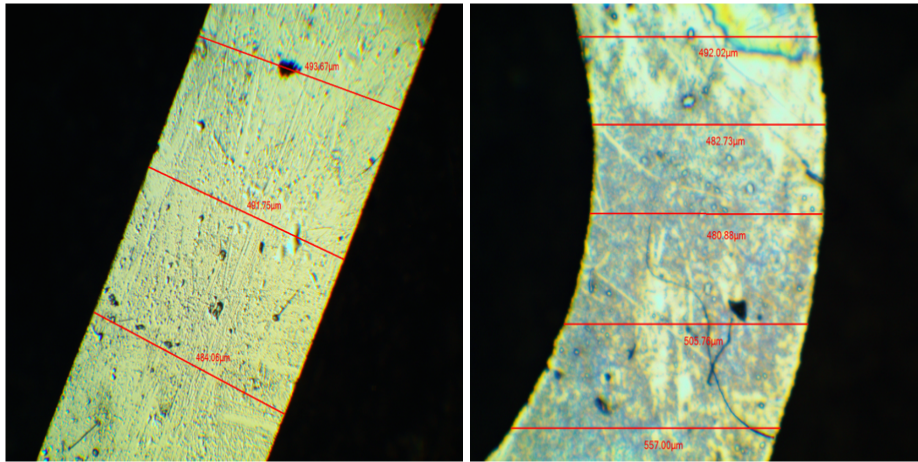
The damage caused to the hard mask was clearly due to the physical etching caused by ions with excessive kinetic energy. Cracks were formed in the hardmask which would cause unwanted patterns in the silicon substrate.

The forward power was then reduced to 30 Watts while the ICP remains constant at 1000 Watts while fabricating the second set of coiled delay line structures. The lowering of the forward power resulted in the hard mask staying intact as shown in Fig 3.9c. However, the spacing between the silicon lines and the widths of the silicon lines was found to vary considerably. This inconsistency creates line structures with varying anisotropy. The edges were jagged and inconsistent. Table 3.2 mentions the RIE recipe that was was used to obtain the second set of coiled structures.

The lack of consistency in these structures was due to the poor passivation since the



(a) Delay Line 1.



(b) Straight Region.

(c) Curved Region.

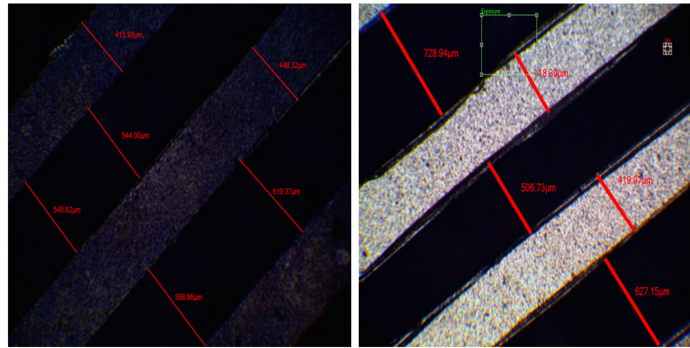
Figure 3.8: High Forward Power of 70 Watts Damaging the Hard Mask.

ratio of $SF_6 : O_2$ was not commensurate with the necessary ratio required to create a good side wall passivation.

As shown in Fig 3.7 the $SF_6 : O_2$ ratio should be 3:1 in the gas feed to give a good etched profile while maintaining a good etch rate. The $SF_6 : O_2$ ratio was modified to a 3:1 ratio while fabricating the next set of delay lines. It was observed that the width and spacing of the fabricated delay lines was consistent as compared to the previous set of delay line structures. However the anisotropy was observed to be only 0.72 and edges were not very consistent. Fig 3.10 depicts the third set of fabricated delay lines.

It was hypothesized that the low anisotropy and inconsistent edges were due to the Sil-

(a) Delay Line 2.



(b) Bottom View. (c) Top View.

Figure 3.9: Varying Widths Due to Poor Sidewall Passivation.

icon Dioxide and Aluminum layers being attacked by the SF_6 gas. The selectivity drops when the temperature around the substrate increases as show by the process characterization carried out in Fig 3.5.

This occurs due to heat generated by ion bombardment over a long period in time. Thus our recipe needed the addition of some thermal passivation inorder to ensure conformal cooling around the substrate. The OxfordPlasma Lab ICP 100 allows for the chuck to be backed with Helium which can cool down the substrate. This allows the heat around the substrate to be dissipated and the temperatures around the substrate to be consistent.

Table 3.3 shows the recipe that was used to obtain coiled delay structures of desired anisotropy. The low RF forward power ensures the aluminum mask holds well while the

Table 3.2: RIE Recipe Table 2

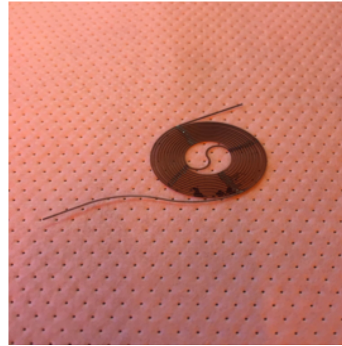
Parameter	Values
SF6/O2	75/10 sccm
RF/ICP	30/1000 W
Process Pressure	15 mT
Temperature	-100 C

Table 3.3: RIE Recipe Table 3

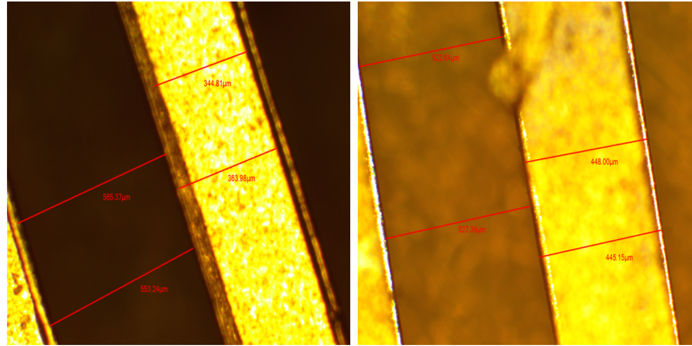
Parameter	Values
SF6/O2	90/30 sccm
RF/ICP	30/1000 W
Process Pressure	15 mT
He Backing	35.5 sccm
Temperature	-100 C

nitrogen cooling ensures greater selectivity of silicon etching over that of the aluminum hard mask. The percentage of O_2 in the feed was also modified to obtain a good passivation layer while simultaneously maintaining a good etch rate. Fig 3.11 shows that a coiled delay line structure was obtained with anisotropy of 0.84. The Aluminum hard mask holds well and edges are consistent. The top and bottom layers do not vary in spacing by more than 80 um unlike in Fig 3.10 where the edges were inconsistent and the top and bottom widths varied by more than 100 um.

The recipe was then test on delay line widths with feature sizes that were less that 100 um to observe if the anisotropy results held for smaller features. Fig 3.12 shows that the anisotropy of greater than 0.9 was obtained for widths and features that were 80 um apart while performing a through etch on a silicon wafer that is 110 um thick. The reduced thickness of the silicon substrate contributed to a higher anisotropy since tapering is not at as narrow as it would has been for wafers that are 220 um thick. The Aluminum once



(a) Delay Line 3.



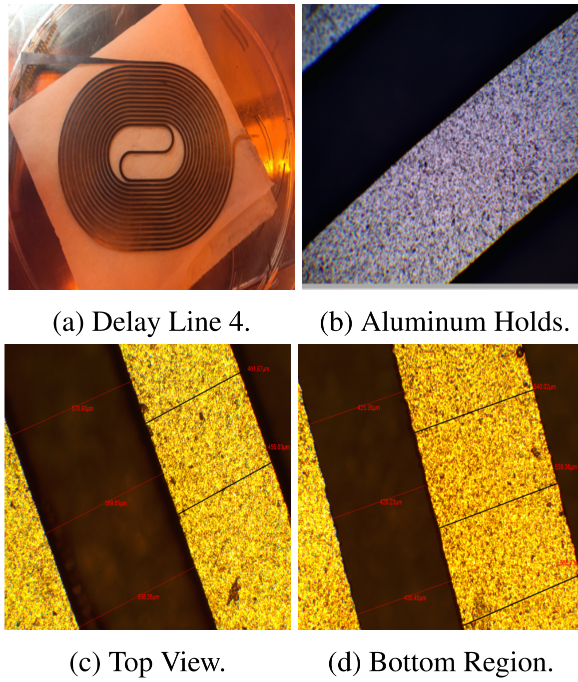
(b) Top View. (c) Bottom Region.

Figure 3.10: Low Anisotropy Due to Poor Thermal Passivation.

again holds well and edges are sharp and consistent.

3.4 Conclusions

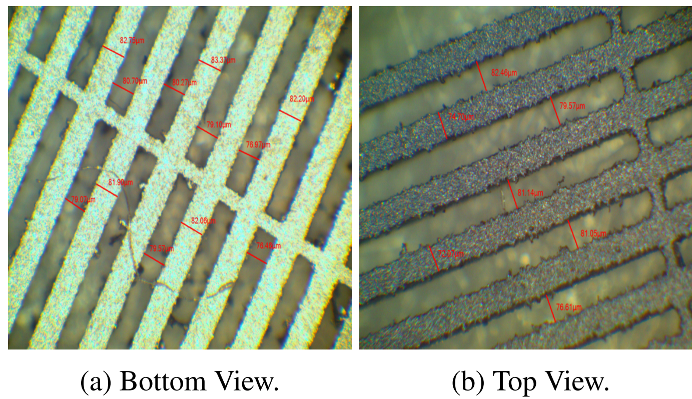
Thus the dry etch process was optimized by creating straight and coiled delay line structures on a Silicon substrate with feature sizes varying between 500 um to 80 um. The Aluminum hard mask held well and an anisotropy of 0.84 and greater was obtained for the fabricated devices with feature sizes as large as 500 um for silicon substrates with a thickness of 220 um. An anisotropy of greater than 0.9 for feature sizes as small as 80 um on 100 um thick Silicon substrates. Thus crygoenic etching can be used to created high aspect ratio, vertically through etched structures in Silicon. The etch profiles of the fabricated devices is shown in Fig 3.13. The recipe developed in the fabrication of the



(a) Delay Line 4. (b) Aluminum Holds.

(c) Top View. (d) Bottom Region.

Figure 3.11: High Anisotropy Obtained by Addition of Helium Backing.



(a) Bottom View. (b) Top View.

Figure 3.12: High Anisotropy for Smaller Features.

delay line structures can now be used to create a high density of micromachined arrays on a Silicon substrate .

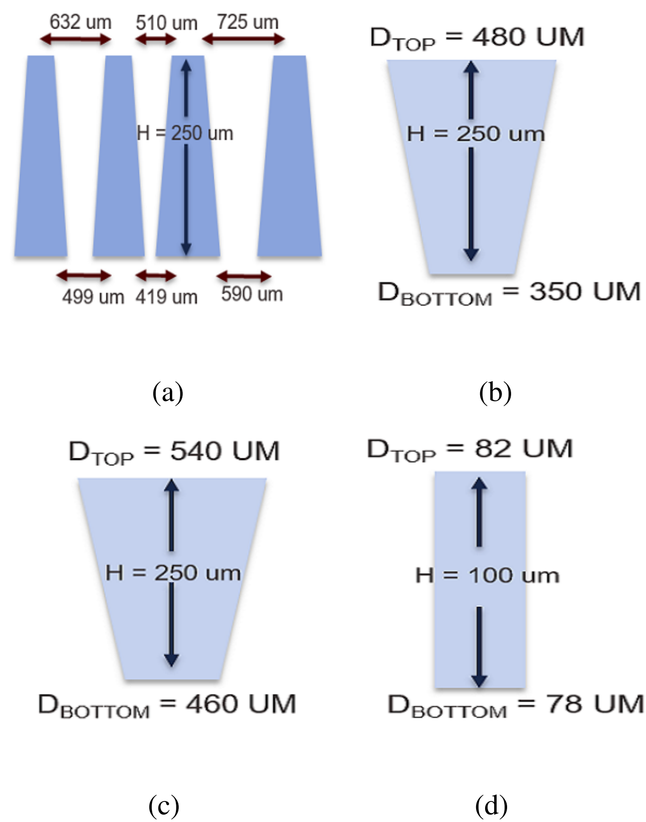


Figure 3.13: Etch Profiles of Delay Lines Fabricated: (a) Second Set of Delay Lines with Varying Anisotropy, (b) Third Set of Delay Lines with Anisotropy 0.72, (c) Fourth Set of Delay Lines with Anisotropy 0.84, (d) Fifth Set of Delay Lines with Anisotropy 0.9.

4. FABRICATION OF SINGLE CELL ARRAY ON SILICON SUBSTRATES

4.1 Design

The methods and techniques developed during the creation of the delay lines were applied to create single cell arrays for cell trapping on silicon substrates. A dense array of microwells is fabricated by etching through a silicon wafer. The anisotropic nature of the cryogenic etch process developed in the previous chapter will be used to create oxygen supply chambers. An upper chamber consisting of two vertically stacked layers has one opening large enough to allow a cell to enter microwell and a smaller opening at the bottom above the oxygen supply chamber to keep the cell in place. This two layered structure positions the cell more precisely while controlling the oxygen supply to the cell. The lateral size and height of the cell chamber is determined based on the average size of the cells being measured. Normal blood cells have an average diameter of 12- 25 um, hence it was decided that the bottom layer will have a hole size of 10 um. The top layer should be large enough to allow a cell to pass through it and the diameter was chosen to be around 50 um. SU8 polymer was used to create the vertically stacked sections since it provides high aspect ratio structures. It is a negative photoresist which can cover a range of thicknesses from 1 um to 200 um while giving good dimensional control over the feature sizes. It is a good material for the creation of microfluidic channels since it is a soft material but still provides structural stability. It also provides excellent chemical resistance to attacks from several acids and bases and these properties make SU8 a very attractive material for making devices for cell handling, mixing and transport.

The Fig 4.1 shows the layered approach to creating the structure.

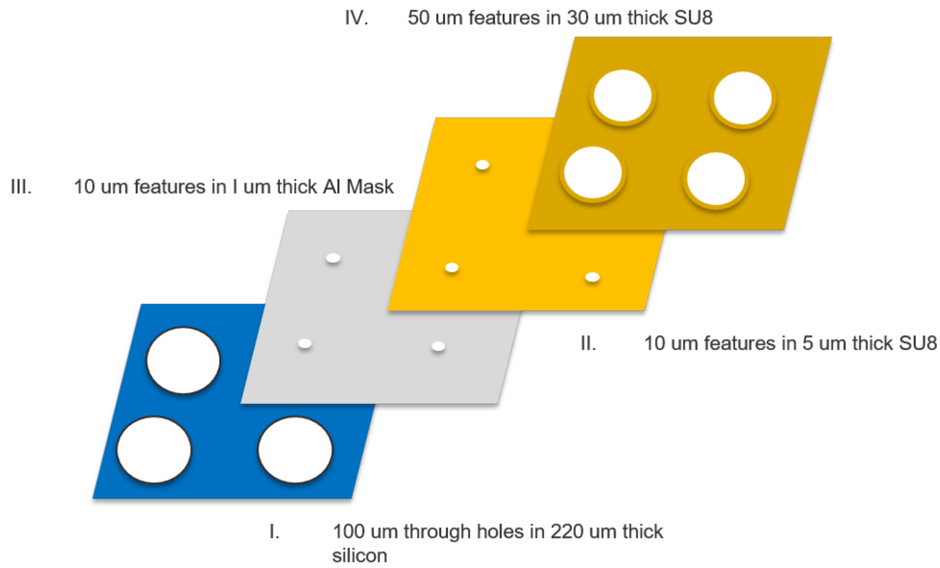


Figure 4.1: Microwell Layers.

4.2 Fabrication Process Development

Single crystalline silicon substrate is used to fabricated an array of etched holes which forms the bottom chamber through which oxygen can be supplied to the cell while SU8 polymer is processed in order to create the top chamber for cell trappment. The fabrication process flow that creates the high density of vertically stacked single cell arrays is described below.

1. **Creation of 100 um through holes in the silicon substrate:** In order to get a highly dense array of structures, (nearly 2500 microwells), within a 2 inch substrate it becomes necessary to create through holes in silicon that are 100 um in diameter on either side of the substrate. The cryogenic etch recipe that was used to create anisotropic silicon delay lines was employed in order to create the dense array of bulk etched through holes. Aluminum was coated on either side of the substrate before etching . The Aluminum surface with the 400 nm thickness is patterned and

will act as the hard mask during the bulk etch. The Aluminum on the opposite surface is 1 um thick and is the base on which the SU8 layers will be fabricated. The Aluminum film should be conformal and should hold firm while not bending inwards.

2. **Deposition of SU8-5 on the 1 um thick Aluminum surface:** SU8 is fabricated onto the 1 um thick Aluminum surface. In the fabrication of the microwell SU8-5 is spun on top of the Aluminum surface in order to create a film that is 5 um thick. The spin speed for the fabrication is 2450 rpm and the spin time is 30 seconds at an acceleration and de-acceleration rate of 400 rpm/second. The film is then placed on a hot plate at room temperature for two minutes in order to allow the polymer to reflow and settle. The hotplate is ramped up to 70 ^{o}C and the substrate is allowed to sit on the hot plate for 2 mins at 70 ^{o}C . The hot plate is then ramped up to 100 ^{o}C and the substrate sits at this temperature for 2 more minutes. The ramping is done to ensure that the film is gradually heated and doesn't suffer from a thermal shock. Also sudden heating causes bubbles on the surface of the film which makes it very uneven.

3. **Creation of 10 um wide features in SU8-5 film:** Once the substrate is cooled down to room temperature the film is exposed using UV light via an MA6 mask aligner. The exposure intensity for a film that 5 um thick is around 90 mJ/cm^2. A mask with 10 um feature sizes is used to create a pattern on the film and is aligned so that it is formed over the 100 um through holes. The film is then post exposure baked in convection ovens at that are at 65 ^{o}C and 95 ^{o}C for 2 mins each. This causes cross linking in the polymer which hardens the exposed regions while causing a faint pattern in the soft unexposed regions. The substrate in then introduced into a beaker containing SU8 developer and agitated vigorously to develop the structures.

Once the film is developed the susbstrate is dipped in a beaker filled with acetone to remove residue. The film is inspected under a microscope to check for proper development. The 10 um features will form the base on which the cells that enter the microwell will rest since the feature size is less than the cell diameter.

4. **Creation of 10 um wide through holes in the 1um thick Aluminum surface:** The SU8-5 film also acts as a hard mask for wet etching the Aluminum on which it rests. Aluminum etchant is used to create 10 um holes in the Aluminum film. A small amount of under cutting will take place as wet etchants are isotropic in nature. This hole will be used to supply oxygen to the cell in a diffusion limited environment.

5. **Creation of the 50 um wide features using SU8-50:** SU8-50 polymer is spin coated on top of the SU8 -5 structure. A spin speed of 4000 rpm for 40 seconds creates a film that is 30 um thick. The film is heated in convection ovens at 70 ^oC for 30 minutes before being transferred to a convection oven at 100 ^oC where it is allowed to be heated for 2 hours. After cooling down to room temperature the substrate in exposed to UV light and the MA6 is once again used for aligning the 50 um features on the mask with the 10 um and 100 um features on the substrate. The exposure intensity for the 30 um features is around 200 mJ/cm^2. The film is then placed in the convection ovens for a post exposure bake with bake times of 8 minutes in the 70 ^oC oven and 12 minutes in the 100 ^oC oven. Once the cross linking takes place the film is placed in the developer and agitated for one minute to reveal the structures. Acetone is used to clean away residues and obtain a clean well developed film.

The Fig 4.2 shows the design and dimensions of the microwell.

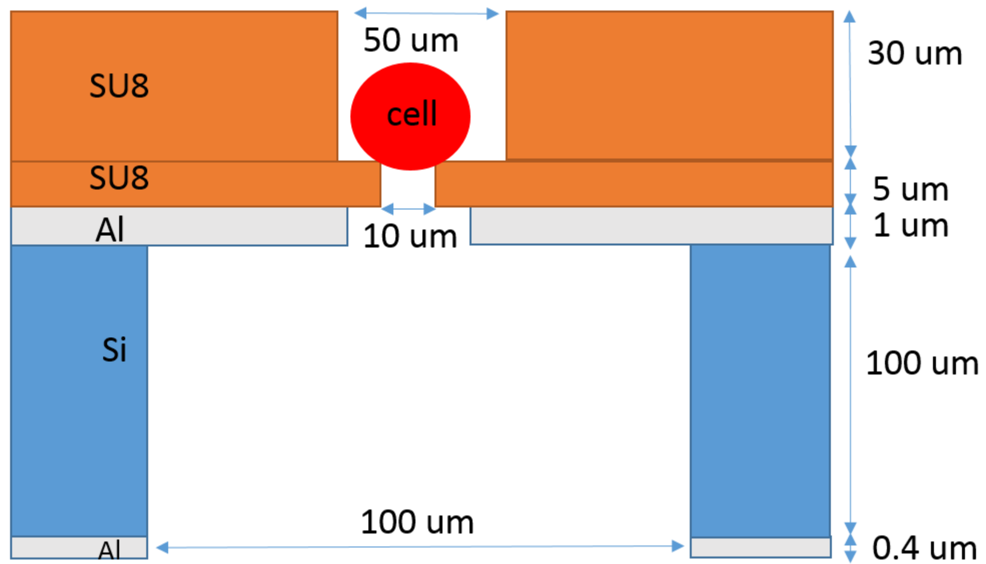
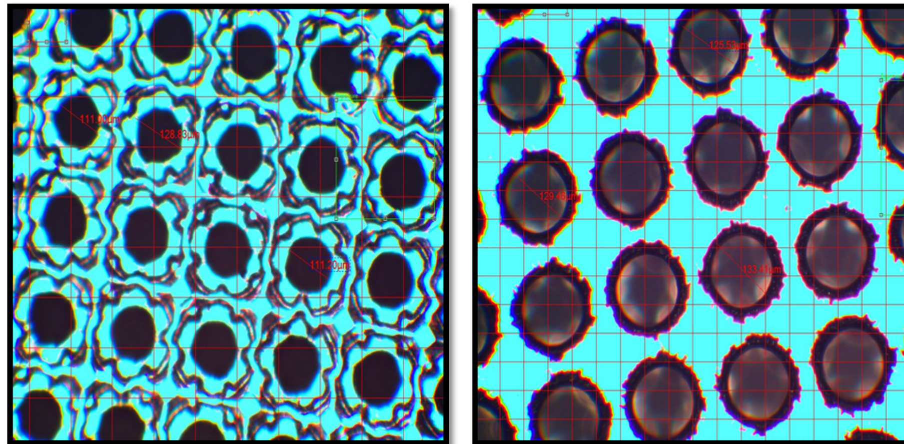


Figure 4.2: Microwell Design.

4.3 Fabricated Devices

Fig 4.3a and Fig 4.3b show the top and bottom surfaces of a through etched silicon wafer with the 100 um features. The 1 um of Aluminum that is an integral part of our device was not deposited intially inorder to characterize the through etch. This allows the use of a simple confocal microscope for characterizing the anisotropy. The figures show that it is possible to create highly anisotropic through etched holes in silicon.

The features on the top surface had a diameter of 120 um to 130 um while the holes on the bottom surface had feature diameters ranging from 110 um to 120 um. The Aluminum hard mask that is 400 nm holds well though there are square shaped cracks that border around the top surface. This is due to some of the photoresist sticking to the transparency mask during the lithography process. This causes the pattern to be transferred onto the aluminum surface. However the border cracks weren't etched through and did not hamper the circular features that we desired to etch away to create our bottom chamber.

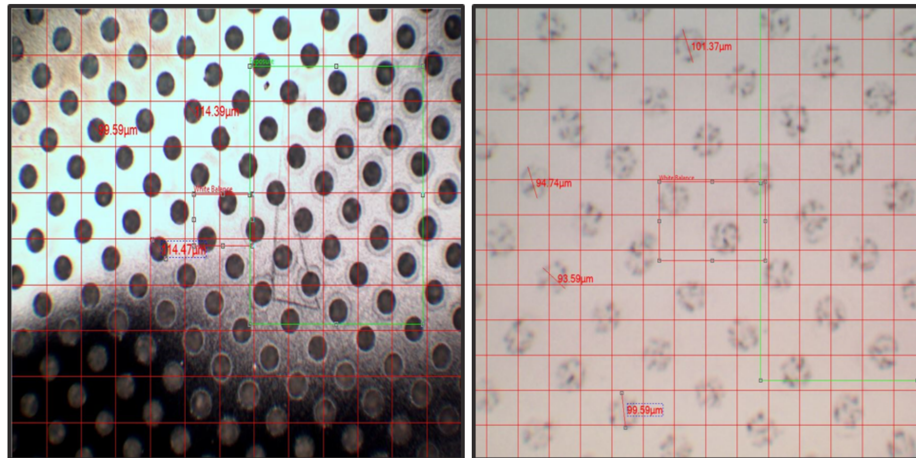


(a) Bottom View. (b) Top View.

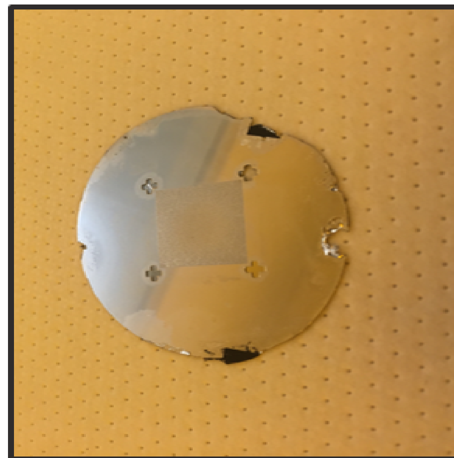
Figure 4.3: 100 um Through Etched Features.

Once it was verified that a highly dense array with anisotropic structures could be fabricated onto a silicon subsrtate using cryogenic etching, 1 um of aluminum was deposited on the opposite surface of the wafer. E beam evaporator was used to deposit the aluminum. The deposition rate was kept as low as possible inorder to get a film that a good amount of intrinsic stress since it internal stress helps create a conformal film that doesn't shrivel up due to tension or compression. A small amount of photoresist was spun onto the back surface of the aluminum inorder to protect the surface from contamination due to fomblin oil. The substrate is introduced into the reactive ion etching chamber with the 400 nm aluminum hard mask facing upwards while the thin film of photoresist is in contact with the carrier wafer. A few drops of fombin oil were added for better thermal passivation. The cryogenic etch processing was carried out as before and the results of the etch are shown in Fig 4.4a and Fig 4.4b.

The view from the hard mask side shows that the features were etched through and that the aluminum pattern doesn't get eroded. The photoresist on top of the 1 um thick aluminum was stripped away and gently blow dried using a nitrogen gun. The microscopy



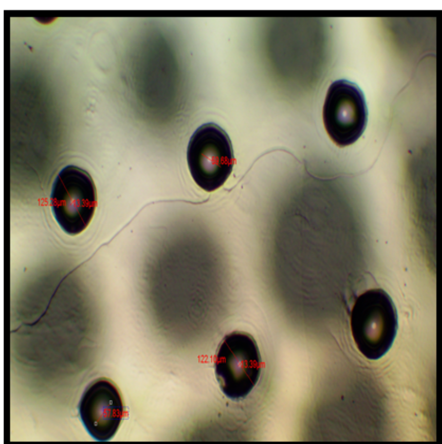
(a) Bottom View. (b) Top View.



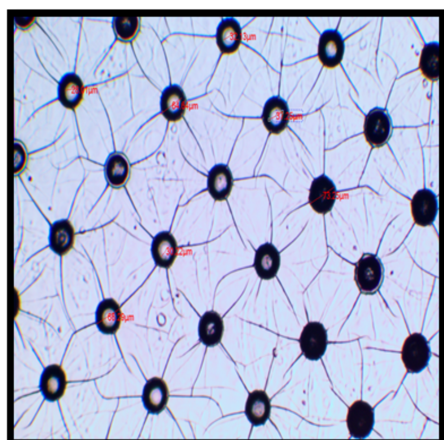
(c) Micromachined Array.

Figure 4.4: 100 um Features with 1 um Thick Aluminum Deposited as a Base for Vertical Stacking.

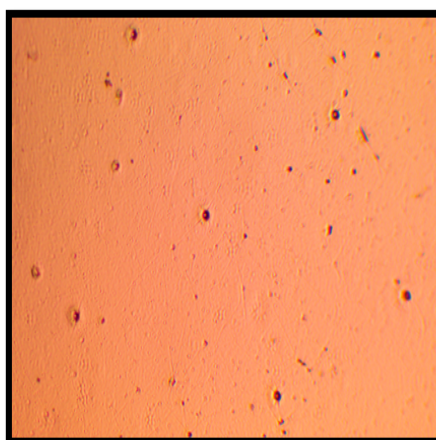
results show that the aluminum surface holds well and a faint outline of the etched holes can observed. The anisotropy of greater than 0.9 is maintained. Fig 4.4b shows the highly dense bulk etched array from the hard mask side. The four crosses at the corners are present for alignment purposes. The next stage of the fabrication process involved creation of the 10 um and 50 um features on top of the 1 um Aluminum surface while ensuring that the vertically stacked layers align their feature sizes properly.



(a) Misalignment of features.



(b) Cracking of SU8 due to Excessive Baking



(c) Under Development of 10 um Features.

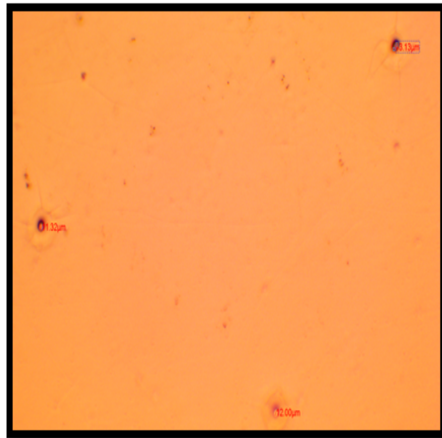
Figure 4.5: Issues Faced During Fabrication.

The processing techniques developed for SU8 polymer were employed to create the vertically stacked cell holding chambers on top of the 1 um thick aluminum film. However there were many issues that were faced in creating these structures. Fig 4.5 depicts some of the issues that impeded the fabrication of the vertically stacked layers. While some layers would align others would not as shown in Fig 4.5b. This is due to some offset that is created if the mask and wafer are not parallel to each other. Alignment can be improved

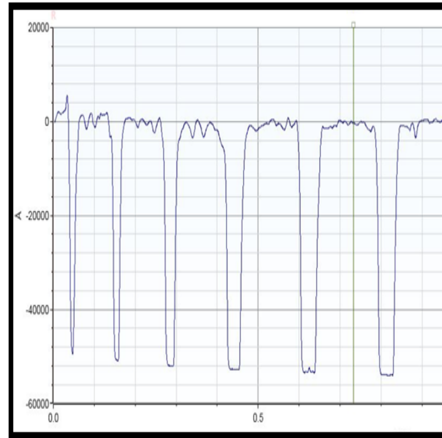
by making the array more dense and the alignment marks closer together. Excessive pre exposure and post exposure baking causes the film to crack and create inconsitencies in the features being developed as shown in Fig 4.6c. Certain features are developed while others remain undeveloped. This is due to uneven leveling of the hot plates which causes the film to cross link differently thus causing variation in the feature profile during development. This can be avoided by ensuring that the film is not heated excessively by following the baking times mentioned in the data sheet for the SU8 film of a particular thickness. Also the wafers should be placed on a even surface during baking. Fig 4.5c shows the effects of under developement of the 10 um features. If the either the exposure time or the post exposure bake time is insufficient, the features do not cross link properly, especially near the bottom surface. This causes the film to either peel away or not develop through the required thickness. Thus, it comes important to calibrate the right exposure time and right baking time for the SU8 features. This is even more important for the 10 um features which face a lot of development issues if not processed properly.

Fig 4.6 depicts the 10 um and 50 um features when properly developed. The patterns are consistent and the film is smooth on the surface and etched in a consistent profile in the valleys. The valleys in Fig 4.6d will form the cell catchment areas while the top region of the valleys in Fig 4.6b will form the base on which the cell rests.

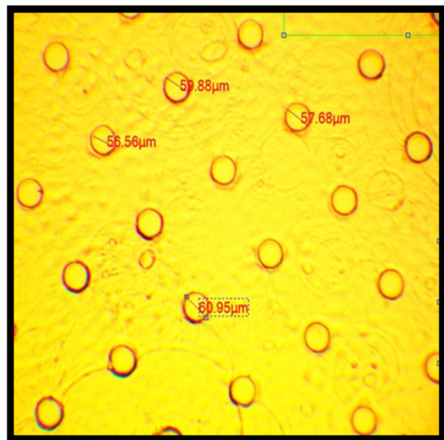
Fig 4.7 shows the proper alignment of the 10 um features on top of the 100 um through holes. Though the centering is not perfect the huge difference in the two feature sizes enables a large number of aligned structures. Fig 4.8 shows the final device with the vertically stacked layers on top of each other. Fig 4.8c shows a top view of the 3 types of features being aligned and stacked on top of one another. The outline of the 100 um through holes are seen at the bottom of the substrate. A small circular ring 10 um wide is observed at the center of each the pattern. This is the 10 um hole formed in the Al mask through the 5 um thick SU8-5 polymer. These features form the base on which the cell



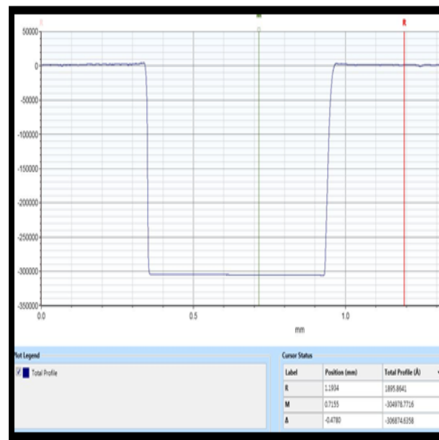
(a) Well Developed 10 um Features.



(b) 5 um Film Thickness.



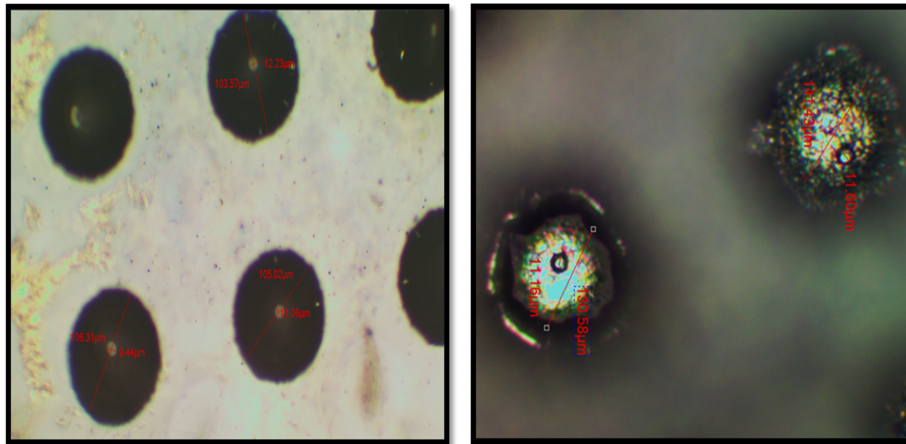
(c) Well Developed 50 um Features.



(d) 30 um Film Thickness.

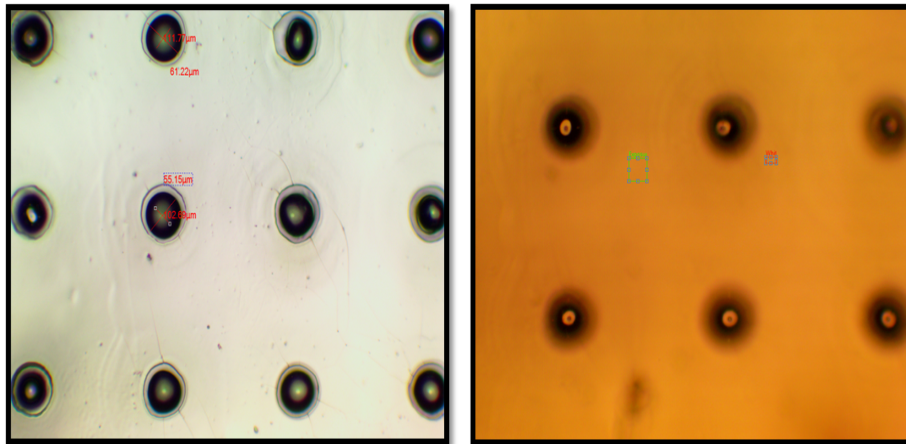
Figure 4.6: Well Developed Features with Conformal Thickness for 10 um and 50 um SU8 Features.

rests while providing an oxygen supply route through the 10 um hole in the aluminum. The circular orange features within the 100 um patterns as shown in Fig 4.8b are the 50-60 um SU8-50 structures that are 30 um thick. These structures form the entrance of the single cell array. The feature sizes obtained were consistent throughout the array. The substrate can now be tested for its cell trapping ability and single cell filling ratio as well as for measuring the OCR content of cells.

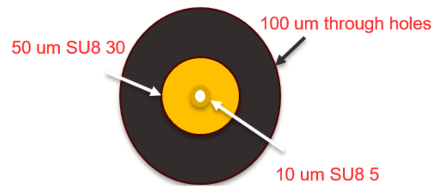


(a) Bottom View. (b) Top View.

Figure 4.7: First Stage of Alignment.



(a) Bottom View. (b) Top View.



(c) Top View.

Figure 4.8: Final Device Structure with Aligned Features.

4.4 Conclusion

This section of the thesis covered the fabrication of the single cell array on a single crystalline silicon substrate. The etch processing techniques that were developed for the fabrication of the silicon delay lines were successfully applied to create high density (around 2500 cell wells) of micromachined arrays in silicon. SU8 polymer was used to create vertical chambers on top of the silicon substrate. The 50 um opening at the top of the well is wide enough to allow cells to enter while the 10 um opening at the bottom is small enough to prevent the cell from falling through and acts as a base on which the cell can rest. The vertical dimensions of the upper chamber of the well is around 35 um which is compact and will allow for a high filling ratio of single cells. The 100 um through etched features at the bottom can be used to provide oxygen to the cell in a diffusion limited environment for OCR analysis.

5. CONCLUSION AND FUTURE WORK

Micromachining techniques were used to fabricate 2500 single cell arrays on a single crystalline silicon substrate. Initially Silicon delay lines with widths varying from 500 um to 80 um were fabricated to characterize and optimize the dry etch process. Special emphasis was laid on obtaining highly anisotropic structures and process paramteres were modified till an anisotropy of greater than 0.85 was obtained using an Oxford PlasmaLab 100 ICP reactive ion etching system. Thus, an optimized dry etch process at cryogenic temperatures was developed to create a dense array of anisotropic through hole structures in the silicon substrate which were only a hundred micrometers in diameter. This would form the lower chamber of the microwell through which oxygen can be supplied to the cell. SU8 polymer was used to fabricate the upper chamber. The feature sizes of around 50 um forms an opening for the chamber while a 10 um opening at the bottom forms the base on which the cell rests. The cell can now enter the microwell through the larger opening while the smaller opening supplies oxygen to the trapped cell from the bottom in a diffusion limited environment.

The next stage involves testing the cell array and observing the filling ratio of the cells. Ideally each array should trap only one cell which will help identify outliers in a cell group while giving a better indication of the average cell group parameters. Oxygen can be supplied to the cell from the lower chamber and the oxygen consumption rate of the cell can be obatined for different types of cells. Improvements can also me made in the process flow of the micromachining of the single cell array to obtain a higher throughput of successfully fabricated arrays. Additionally glass can be used as a substrate for micromachining in place of silicon. This would open the array system up to optical analysis techniques thereby enhancing the capabilities of the cell array system.

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