COMMUTATION TECHNIQUE FOR HIGH FREQUENCY LINK INVERTER WITHOUT OPERATIONAL LIMITATIONS AND DEAD TIME

A Thesis

by

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ABSTRACT

An improved commutation technique for the ac-ac output converter circuit of a pulse width modulated high frequency link (HF-link) inverter has been investigated. The high frequency link inverter converts a DC input voltage into line frequency AC output voltage using a high-frequency transformer for voltage step-up and galvanic isolation, without an intermediate rectification and DC bus. In this topology, there is a direct ac-ac converter, which processes the HF-link square-wave voltage into the desired sinusoidal ac output voltage. To do this requires a commutation method to prevent shoot-through when output current changes direction or commutates from one switch to the next. Conventionally, dead time is used but this adds distortion to the output waveform. Previously a commutation technique without dead time was introduced, but it required a number of assumptions on the inverter load impedance and link voltage characteristics that made it useful for a stand-alone R-L load but not practical for grid connection. The commutation method in this paper does not require dead time and does not impose any limitation on the output inductance and link voltage magnitude and frequency. Simulations, results experimental results and detailed analysis of output current THD values are presented.

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All work for the thesis was completed by the student, under the advisement of Professor Balog of the Department of Electrical and Computer Engineering.

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1. INTRODUCTION[*]

1.1 Introduction

Of the numerous inverter topologies and controls studied in the research literature [1-5], the high frequency link (HF-link) inverter, which is shown in Figure 1, converts DC input volt age, such as from fuel cells or photovoltaic arrays, into line frequency AC voltage without needing an internal DC bus. It has practical advantages because it contains a high-frequency transformer to provide galvanic isolation for safety and voltage step-up [6]. It also has the potential to be more efficient than a DC-link topology, which is shown in Figure 2, because the output of the link transformer is not rectified, eliminating a power conversion step.

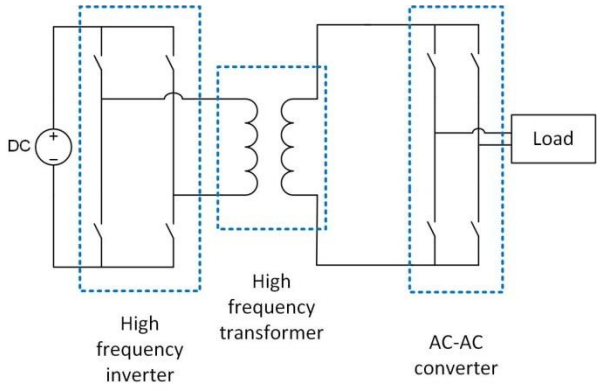

Figure 1. High frequency link inverter

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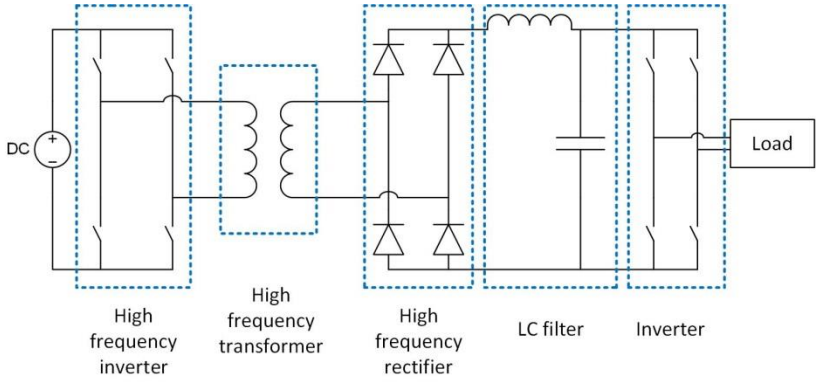

Figure 2. DC-link inverter

In Figure 2, the topology changes the input DC voltage into high frequency AC voltage which may be in the form of a square wave. Then the high frequency AC voltage goes through a high frequency transformer and a rectifier so it becomes DC voltage again. Then the inverter changes it to line frequency AC voltage.

This high frequency DC link converter topology has been studied with various applications and control methods [7- 15]. Active clamp in high frequency DC link converter allows the use of low voltage stress diodes so it helps to achieve optimum efficiency [7-8]. A maximum power point tracking (MPPT) method for this converter is introduced in [9]. Optimal Sequence-Based-Controller (OSBC) for this topology realizes MPPT for better efficiency for this topology [10]. Soft-switching techniques for this topology reduce switching losses [11-13]. In the high frequency DC link topology, bulky DC-capacitor can be removed if hybrid-modulation is implemented [14-16]. This topology is investigated for wind Energy conversion systems as well [17-18].

However, in Figure 1, the topology changes the DC voltage to high frequency link voltage. The AC voltage goes through a high frequency link voltage and the AC-AC converter changes the high frequency link voltage into line frequency AC voltage. Therefore, the topology in Figure 1 has fewer steps than the DC-link topology and it also removes the necessity of LC filter in the middle.

This AC link converter has been studied widely with various applications and control methods [19-27]. This topology can be extended to bidirectional inverter [19]. Soft-switched high frequency AC link converter improves the efficiency of the converter [22-25].

The output inverter topology, shown in Figure 1, may have the appearance of a cycloconverter, but it is controlled very differently by using pulse width modulation (PWM) methods, which create high-quality voltage and current waveforms. The topology has only two power stages: the primary side of the HF-link transformer, where DC input voltage is converted into high frequency square wave, and the secondary side, where the square wave voltage is converted into the desired sinusoidal voltage without an intermediary rectification step. The rectifier diodes and LC filter are eliminated, reducing cost, power loss, mass \ volume, and reliability problems [26].

In the secondary side of the inverter, shown in Figure 3, Vlink is the square wave generated by the input stage converter and the load is grid-connected. It was thought that such an AC-AC converter requires complicated control and modulation [26-33] and generated significant harmonic distortion. However, it was previously shown that thyristors could be used in this topology along with a PWM method to produce high-

quality current waveforms with natural current commutation to reduce losses instead of requiring hard-switched IGBT or MOSFETS [6]. The double frequency ripple, usually handled by capacitance at the dc-link is managed separately [34].

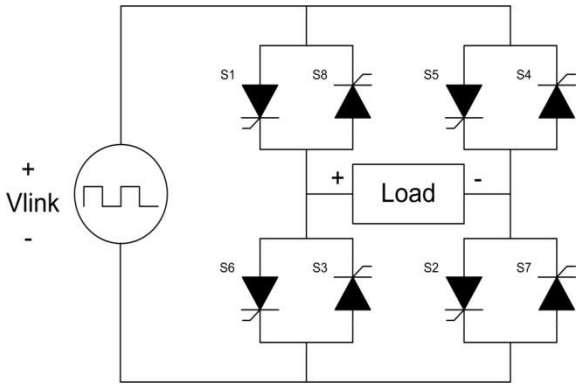

Figure 3. High frequency link inverter ac-ac converter

Dead time can prevent shoot-through in a cycloconverter, matrix converter, or other topologies with totem pole switches but lowers efficiency and introduces zero-cross distortion, which requires compensation [35-38]. Figure 4 shows how the shoot through current can flows in the AC-AC converter. In the Figure, the input voltage is positive and S1 and S6 are on at the same time. This can happens if S6 is supposed to be on and S1 is supposed to be off but before S1 is off, S6 is already on. Therefore, to prevent this kind of shoot-through current, certain amount of time when all the switches are off is typically inserted between switch transitions and the time is called dead time. The process of switching current is called commutation and commutation method is

critical not only to provide the desirable output voltage and current, but also to prevent any shoot-through current and commutation failures.

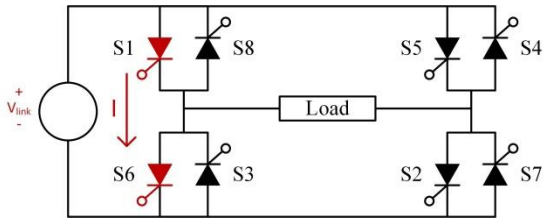

Figure 4. Possible shoot-through current

As a safe commutation method, 4-step switching method is also developed for AC-AC converter [39-40]. Figure 5 shows the AC-AC converter where the 4 step switching can be applied. Figure 6 shows how the four step switching works. The 4-step switching method in AC-AC converter is one of the methods that can be applied to remove the dead time but provides safe commutation.

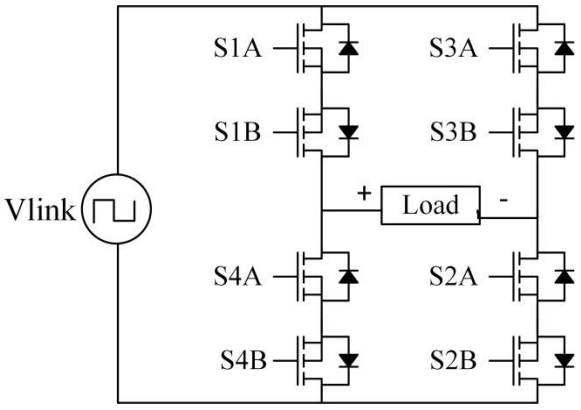

Figure 5. AC-AC converter with four step switching method

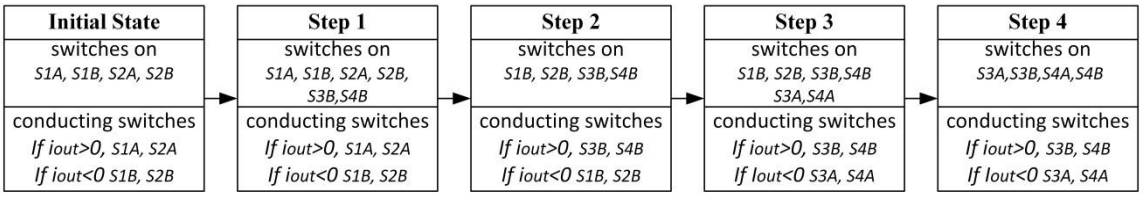

Figure 6. Four step switching method

A commutation technique, which did not use dead time was previously introduced for the topology in Figure 3 [30]. However, this method required some assumptions.

1) Switching occurs once per HF link commutation.
2) The threshold current value is higher than the thyristor's holding current and the latching current values.
3) While the magnitude of the current is lower than the selected threshold current value, the link voltage's polarity stays the same.
4) The minimum value of the output current during one HF link commutation occurs while the output current freewheels through the switches which were gated during previous HF voltage interval.
5) For every transition in HF link, a unique switching pair is gated.

The third assumption requires that the amount of the current changes during one HF link commutation is big enough. To meet these assumptions, the link voltage frequency must be low enough; the output inductance must be high enough; and the link voltage magnitude must be high enough. If these assumptions are not valid then the output current will not properly commutate and commutation failure will occur.

1.2 Thesis outline

This thesis develops a new method that overcomes these limitations. The outline of this thesis is as follows.

Chapter 2 explains the details of the previous commutation method and three possible failures cases. The previous method is based on a state machine which has four states. Each state represents one unique switching pair and the inputs for the state machine are the polarity of the link voltage and the direction of the load current. The previous method successfully commutates the switch pairs if the assumptions are met. However, if voltage changes its polarity while current is near the zero crossing points, there are three different possible failure cases and distortions will be added to the output current.

In chapter 3, the new commutation method and the three operation cases of the new method will be introduced. Just like the previous method, the new method is based on a state machine. However, the new state machine has 12 states and it requires not only the link voltage polarity and the magnitude of the output current but also PWM values and the direction of the output current. Unlike the previous method, the new method does not produce distortions to the output current even if the link voltage changes its polarity while the current is near the zero crossing point.

In chapter 4, simulation and experiment results are presented and the analysis of the results is discussed. Both the previous method and the new method are simulated and tested through. The results of the new method show that the new method removes the distortions which were presented during the previous method simulations and

experiments. THD analysis results of the output current during both the previous method and the new method are presented.

2. NECESSITY OF NEW COMMUTATION TECHNIQUE[*]

2.1 Introduction

The commutation technique based on a state machine is previously presented. The state machine decides which switching pair to turn on depending on the magnitude of the load current and the link voltage polarity and it does not insert any dead time when the load current changes its direction. However, the method assumes that when the output current is near the zero crossing point, the link voltage does not change its polarity. To meet this assumption, the current magnitude change during one HF link voltage should be large enough. Therefore, to implement the previous method without any distortion, there are limitations on the link voltage magnitude, switching frequency and the load inductance.

If the assumption which was mentioned above is not met, the commutation process would be different from what is expected so distortions would be inserted to the output current. This chapter discusses three commutation failures that can occur with the previous technique. All of the three cases occur because the link voltage changes its polarity while the load current is near the zero crossing point. However, each case starts to be distorted at different points. The detail failure process of each case will be discussed in this chapter.

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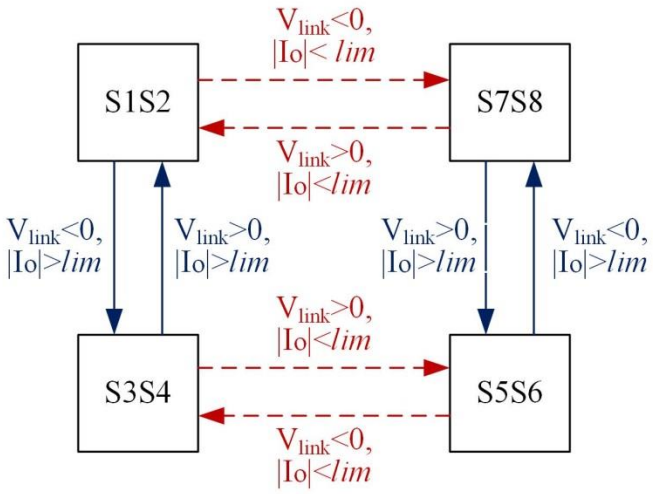

Figure 7. State machine for commutation technique from previous work

2.2 Previous method and its operation

Figure 7 illustrates the prior commutation technique, which is based on a state machine where each state represents a pair of switches from Figure 3. For example, state S1S2 represents switch pair (S1,S2) on and all other switches off. As shown, a change in switch-state (state transition) occurs when the high frequency square wave link voltage (Vlink) changes polarity or the magnitude of the output current (Io) value drops below a predetermined value (lim). In Figure 7, the commutations, which occur when the link voltage changes its sign, are presented using blue color arrows and the commutations, which occur when the output current magnitude is lower than the limit value, are presented using dashed red color arrows.

The state machine initiates a change in switch configuration between (S1,S2) and (S3,S4) or between (S5,S6) and (S7,S8), depending on the polarity of output current

when the link voltage changes polarity. These commutations make sure that the switches, which are supposed to be on, are turned on when the load current is higher than the lim value. Table 1 shows which switches are supposed to be on while the load current higher than the limit value.

Table 1. Switching pairs depending on link voltage and output current polarity

	Link voltage	Output current
S1S2	positive	positive
S3S4	negative	positive
S5S6	positive	negative
S7S8	negative	positive

If the output current magnitude is less than the threshold limit (lim) value, the method assumes that the current is nearing the zero-cross and hence about to change polarity. For positive link voltage, if the output current magnitude becomes less than lim, the switch-state changes from (S3,S4) to (S5,S6) or (S7,S8) to (S1,S2). If the output current magnitude becomes lower than lim value when link voltage is negative, switch-state changes from (S1,S2) to (S7,S8) or from (S5,S6) to (S3,S4). To prevent shoot-through current, direct switch-state transition between (S1,S2) and (S5,S6) and between (S3,S4) and (S7,S8) are prohibited from occurring.

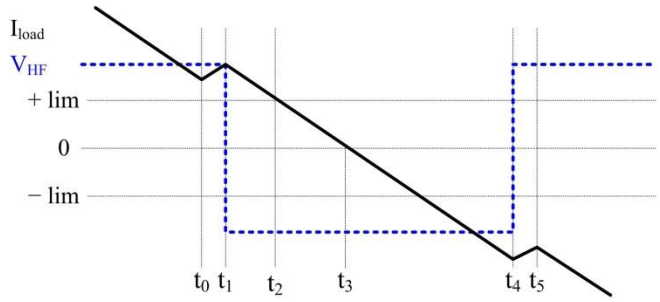

Figure 8. Commutation from positive current to negative current while link voltage is negative

Table 2 : Commutation from S1S2 to S7S8 as shown in Figure 8

Time	Switches
~t_0	Freewheeling through S3S4
t_0~t_1	S1S2 turned on
t_1~t_2	Freewheeling through S1S2
t_2~t_3	S7S8 gated, freewheeling through S1S2
t_3~t_4	Freewheeling current commutates to S7S8
t_4~t_5	Freewheeling through S7S8
t_5~	Freewheeling current commutates to S5S6

Figure 8 and table 2 show the process of current zero-cross from the technique. The output current (Iload) is changing polarity from positive to negative while the high frequency square wave link (VHF) voltage is negative. Prior to t_0, both the link voltage and output current are positive. Current freewheels through switch pair (S3,S4), resulting in negative output voltage, and the current decrease in magnitude. From t0 to t1, (S1, S2) is on, output current is positive and the link voltage is positive so the output voltage is also positive and both current value and the magnitude of current increase. From t1 to t2, the link voltage is negative, output current positive; the current freewheels through

(S1,S2) resulting in negative output voltage and both current value and the magnitude of the current decrease. At t2, the current magnitude reaches the threshold limit value. The switch state changes from S1S2 to S7S8 so (S7,S8) is on. However, current still flows through (S1,S2) because the output current is not yet negative. At t3, the current changes direction and current starts to flow through (S7,S8). From t3 to t4, the link voltage is negative, the output current is negative and current flows through (S7,S8) so output voltage is negative and current decreases, but the magnitude of the current increases. From t4 to t5, link voltage is positive, current is negative and current flows through (S7,S8) so output voltage is positive and current increases but the magnitude of the current decreases. At t5, (S5,S6) is on and current magnitude starts increasing.

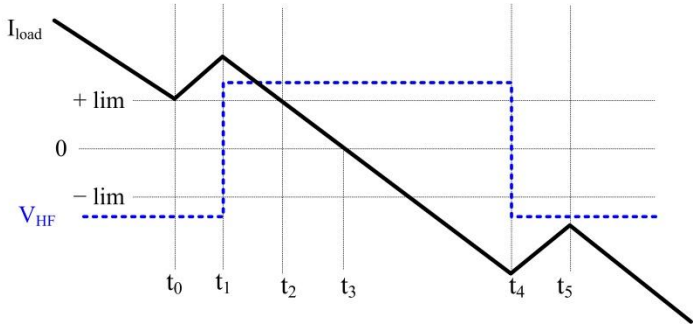

Figure 9. Commutation from positive current to negative current while link voltage is positive

Similarly, if the load current changes from positive to negative when input voltage is positive, (S5,S6) is turned on when current magnitude is lower than the limit value, so a path for the current after current sign transition is provided. Figure 9 and

Table 3 show more detail switch transition from (S3,S4) to (S5,S6). The procedure is the same with Figure 8, but since the commutation occurs when voltage is positive, (S3,S4) is on instead of (S1,S2) and (S5,S6) is on instead of (S7,S8).

Table 3. Commutation from S3S4 to S5S6

Time	Switches
~t_0	Freewheeling through S1S2
t_0~t_1	S3S4 turned on
t_1~t_2	Freewheeling through S3S4
t_2~t_3	S5S6 gated, freewheeling through S3S4
t_3~t_4	Freewheeling current commutates to S5S6
t_4~t_5	Freewheeling through S5S6
t_5~	S7S8 turned on

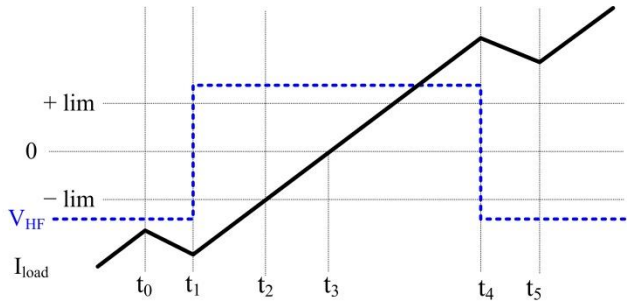

Figure 10. Commutation from negative current to positive current while link voltage is positive

Figure 10 and Table 4 show the commutation from (S7,S8) to (S1,S2) when the load current transitions from negative to positive while the link voltage is positive. (S1,S2) is on when current magnitude is lower than limit value at t2 but current freewheels through (S7,S8) until the magnitude of the current changes its direction.

Figure 11 and Table 5 show the commutation when the load current changes from negative to positive while the input voltage is negative. (S5,S6) is on before the current magnitude is lower than the limit value and when the current magnitude is lower than the limit value, (S3,S4) is on. The current still flows through (S5,S6) and when the current changes its direction, current flows through (S3,S4).

Table 4. Commutation from S7S8 to S1S2

Time	Switches
~t_0	Freewheeling through S5S6
t_0~t_1	S7S8 turned on
t_1~t_2	Freewheeling through S7S8
t_2~t_3	S1S2 gated, freewheeling through S7S8
t_3~t_4	Freewheeling current commutates to S1S2
t_4~t_5	Freewheeling through S1S2
t_5~	S3S4 turned on

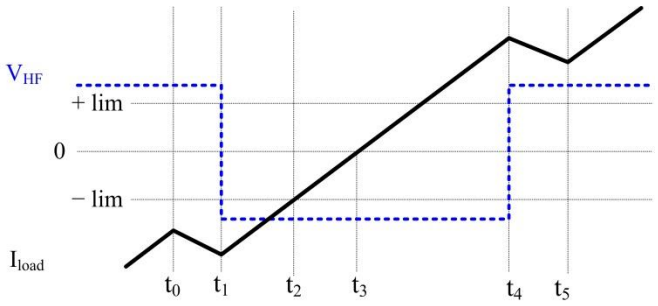

Figure 11. Commutation from negative current to positive current while link voltage is negative

Table 5. Commutation from S5S6 to S3S4

Time	Switches
~t_0	Freewheeling through S7S8
t_0~t_1	S5S6 turned on
t_1~t_2	Freewheeling through S7S8
t_2~t_3	S1S2 gated, freewheeling through S7S8
t_3~t_4	Freewheeling current commutates to S3S4
t_4~t_5	Freewheeling through S3S4
t_5~	S1S2 turned on

Therefore, in this commutation technique, while the direction of the current changes, the pair of thyristors that will provide the path for the current are on in advance so a path for the current is always provided. At the same time, direct switch transitions between (S1,S2) and (S7,S8) and between (S3,S4) and (S5,S6) are prohibited to prevent shoot-through current.

2.3 Failure case 1 from the previous method

This commutation technique is very useful because it does not require dead time but also prevent shoot-through current from commutation failure. However, this method assumes that current changes from +limit to –limit or –limit to +limit within one voltage commutation interval, so this method assumes that while the load current changes from +limit to –limit or while current changes from –limit to +limit, voltage sign remains the same. However, it is possible that while the output current magnitude is lower than the limit value, the link voltage changes its polarity. If this occurs, the commutation procedure is different from what we expect and the output current will be distorted.

There are three different commutation failure cases which happen if the assumption is not met.

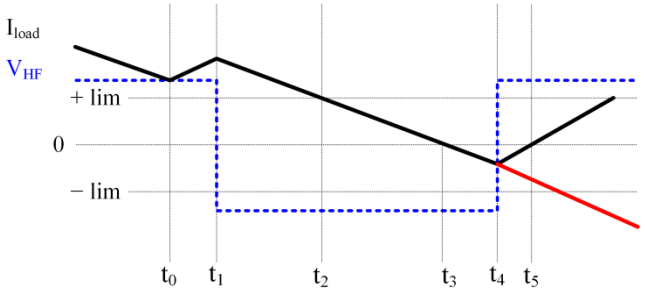

Figure 12. Failure case 1 during commutation from S1S2 to S7S8, Previous method (black), desirable result (red)

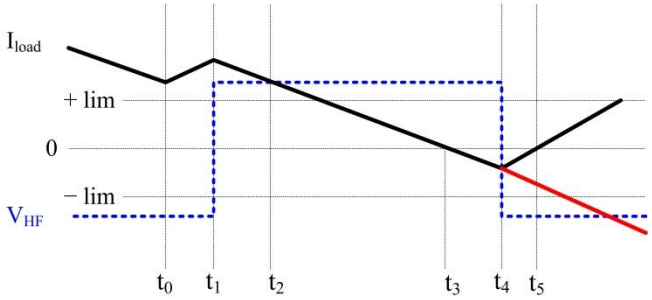

Figure 13. Failure case 1 during commutation from S3S4 to S5S6, Previous method (black), desirable result (red)

Figure 12, Figure 13, Figure 14 and Figure 15 show the first commutation failure case. Black lines show what happens if this assumption is not met and the red lines show the desirable output current result. This failure case represents the case that the link

voltage changes its polarity when the output current already changed its direction but the magnitude of the current is not yet the limit value.

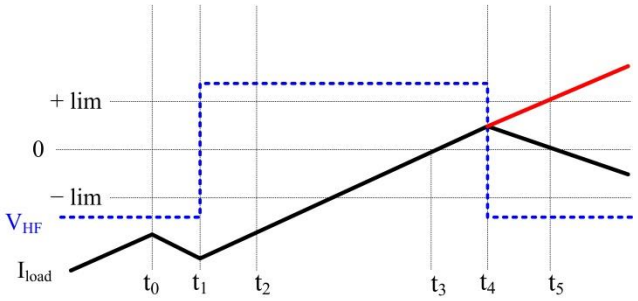

Figure 14. Failure case 1 during commutation from S5S6 to S3S4, Previous method (black), desirable result (red)

In Figure 12, the black line shows this commutation failure case. The current changes polarity from positive to negative while the link voltage is negative, therefore at t2, (S7,S8) is on. However, if the voltage polarity changes when in state S7S8 and current has not reached –lim, commutation from (S7,S8) to (S1,S2) occurs even though current is supposed to be negative and (S5,S6) is supposed to be on at this time. As a result, at t4 (S1,S2) is gated again and the current still flows through (S7,S8). From t4 to t5 the current freewheels through (S7,S8) so the current magnitude decrease even though it is supposed to increases. Then after t5, the current flows through (S1,S2) and becomes positive again.

In Figure 13, the black line represents failure case 1 during commutation from (S3,S4) to (S5,S6). Before t0, the current flows through (S1,S2). From t0 until t1, (S3,S4)

is on. At t2, the magnitude of the current lower than the limit value and (S5,S6) is gated but the current still freewheels through (S3,S4) until t3. From t3 to t4, the current flows through (S5,S6) but at t4, the link voltage becomes negative and (S3,S4) is gated again because the current magnitude is lower than the limit value even though (S3,S4) should not be gated and the current still has to flow through (S5,S6).

In Figure 14, the current changes its direction from negative to positive while the link voltage is positive. From t0 to t1, (S5,S6) is gated and from t1 to t3, current freewheels through (S5,S6) and from t3 to t4, current flows through (S3,S4). However, the voltage changes from positive to negative before the magnitude of the current becomes higher than the limit value and (S5,S6) is gated again even though it is not supposed to be gated and current should flows through (S1,S2).

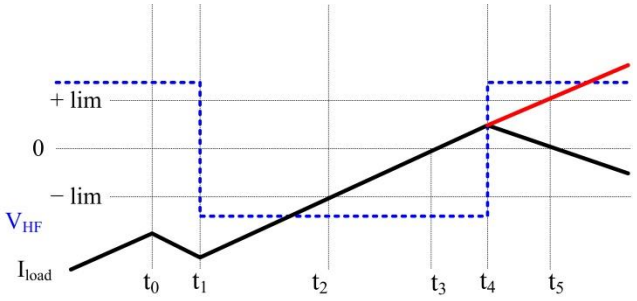

Figure 15. Failure case 1 during commutation from S7S6 to S3S4, Previous method (black), desirable result (red)

Figure 15 shows the failure case 1 during the commutation from (S7,S8) to (S1,S2). Similar to the previous figures, before t3 current flows through (S7,S8) and

from t3 to t4 current flows through (S1,S2). At t4, the link voltage changed its direction but the current magnitude is less than the limit value. Therefore, even though (S3,S4) is supposed to be gated for the right commutation, (S7,S8) is gated again so the output current will be distorted.

2.4 Failure case 2 from the previous method

Figure 16 shows another failure during commutation from (S1,S2) to (S7,S8). In this case, when current changes from +limit to –limit, the voltage polarity remains the same so the commutation is successful until t4. However, after the load current drops below –lim, during this freewheeling period from t4 to t5, current increases above the –lim value so state changes from S7S8 to S1S2 again. In Figure 8, from t4 to t5, current is always lower than –limit value so after t5, state changes to S5S6 but in Figure 16 in the state machine, state changes from S1S2 again and current increases even though current is supposed to decrease at this time. Thus, current becomes positive again since after t5, (S1,S2) is on instead of (S3,S4).

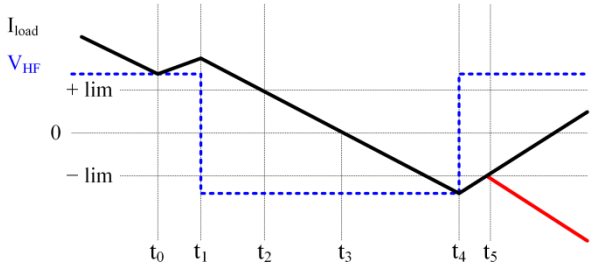

Figure 16. Failure case 2 during commutation from S1S2 to S7S8, Previous method (black), desirable result (red)

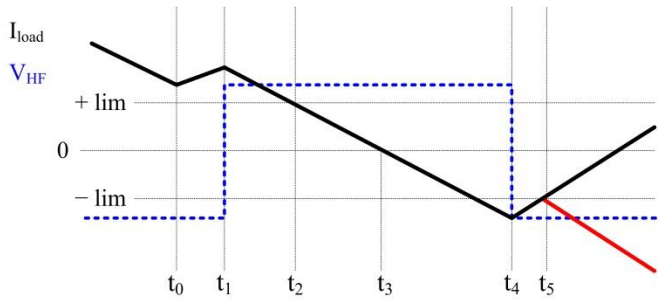

Figure 17. Failure case 2 during commutation from S3S4 to S5S6, Previous method (black), desirable result (red)

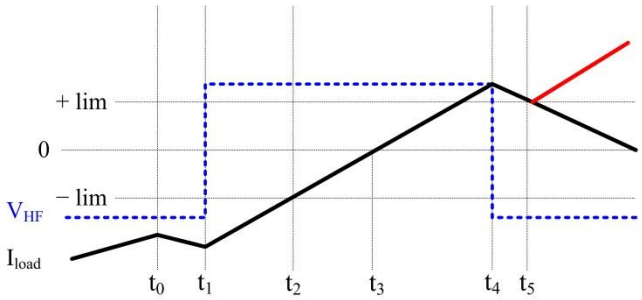

Figure 18. Failure case 2 during commutation from S5S6 to S3S4, Previous method (black), desirable result (red)

Figure 17, Figure 18 and Figure 19 show the failure case 2 during commutation from (S3,S4) to (S5,S6), from (S5,S6) to (S3,S4) and from (S7,S8) to (S1,S2), respectively. Just like Figure 16, before t4, the commutation is successful and there is no difference from Figure 9, Figure 10 and Figure 11. However, while the current freewheels before the PWM signal, the current magnitude becomes less than the limit value. Then according to the state machine, the switch pair which was gated from t0 until t1 is gated again even though it is not supposed to be on again. Therefore, the

commutation procedure is different from what we expected and distortion is inserted to the output current waveform.

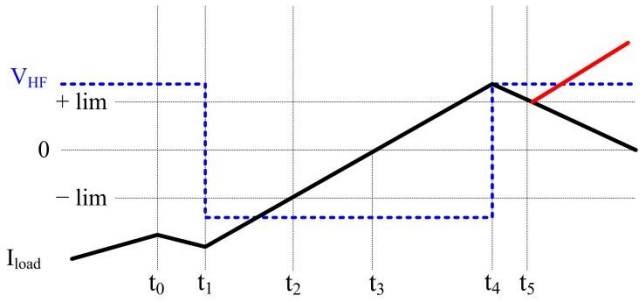

Figure 19. Failure case 2 during commutation from S7S8 to S1S2,

Previous method (black), desirable result (red)

2.5 Failure case 3 from the previous method

In Figure 20, at t2, the gate signal for (S7,S8) is given but from t1 to t4, current freewheels through (S1,S2). At t4, link voltage polarity changes and the magnitude of the current is less than the limit value so commutation from (S7,S8) to (S1,S2) occurs. From t4 to t6, current flows through (S1,S2) and since link voltage is positive, output voltage is also positive and the magnitude of the current increases. Then from time t6 to t7, like the commutation from t1 to t4, the gate signals for (S7,S8) will be asserted. Then at t7, like t4, commutation from (S7,S8) to (S1,S2) occurs and this procedure repeats forever in the previous technique. The difference between failure case 1 and 3 is that in Fig. 9, the state transition from S7S8 to S1S2 occurs when current polarity has already changed so current flows through (S7,S8) then flows back to (S1,S2). However, in

Figure 20, state transition from S7S8 to S1S2 occurs when current polarity is still positive so current flows only through (S1,S2).

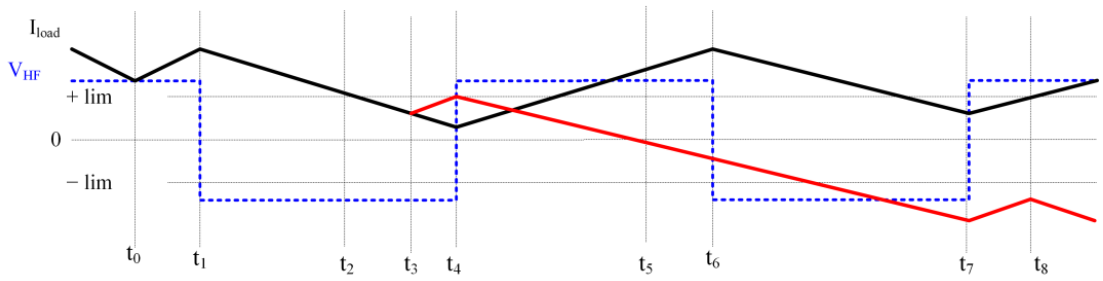

Figure 20. Failure case 3 during commutation from S7S8 to S1S2, Previous method (black), desirable result (red)

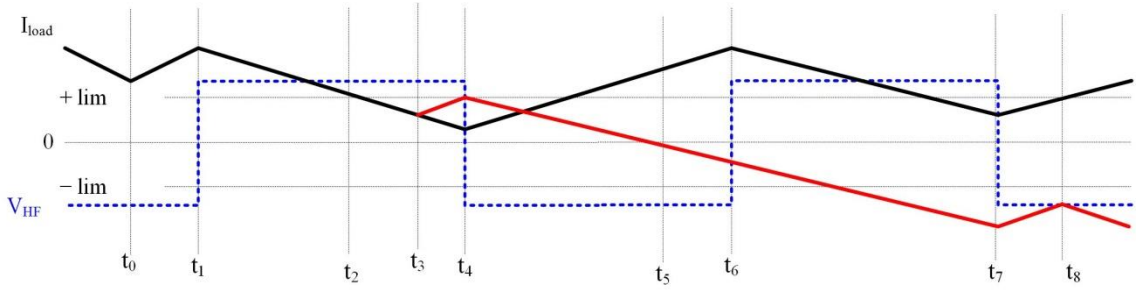

Figure 21. Failure case 3 during commutation from S3S4 to S5S6, Previous method (black), desirable result (red)

Figure 21, Figure 22 and Figure 23 show the failure case 3 during the commutations from (S3,S4) to (S5,S6), from (S5,S6) to (S3,S4) and from (S7,S8) to (S1,S2), respectively. At t4, the current direction is not yet changed but the voltage

polarity changes. Then, the switch pair which was gated from t0 to t1 is gated again from t4. Therefore, even though the magnitude of the current is supposed to decrease, it increase and distortion is caused to the output current.

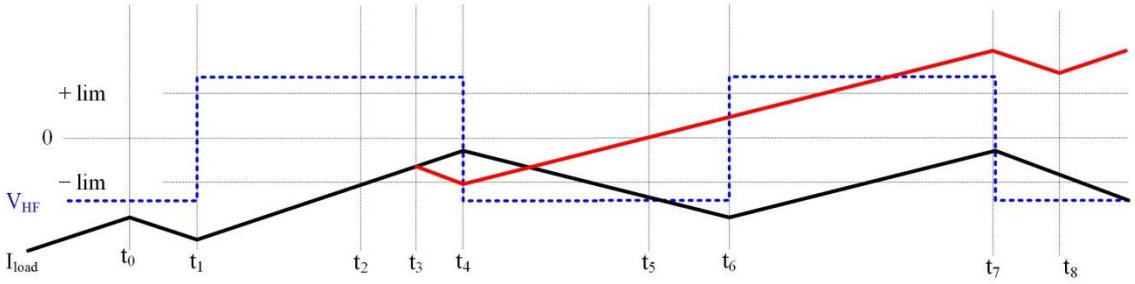

Figure 22. Failure case 3 during commutation from S5S6 to S3S4, Previous method (black), desirable result (red)

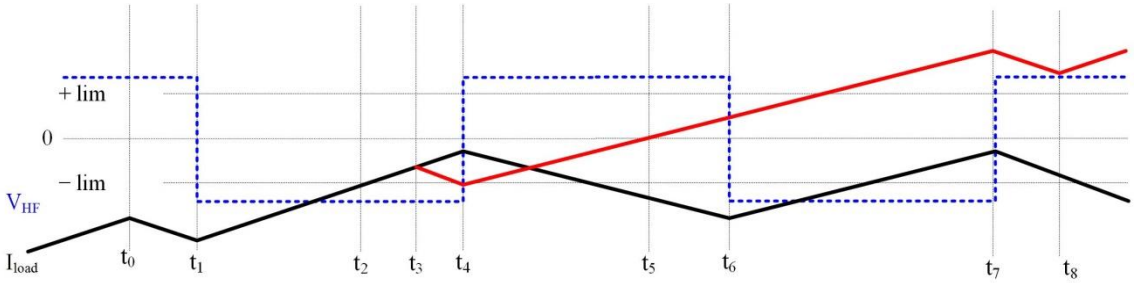

Figure 23. Failure case 3 during commutation from S7S8 to S1S2, Previous method (black), desirable result (red)

In all three cases, if current changes its direction from positive to negative when voltage is negative, commutation failure occurs in which the state machine toggles between S1S2 and S7S8 instead of properly transitioning to S5S6. If the current changes from negative to positive while the link voltage is negative, the state machine toggles

between S1S2 and S7S8 rather than properly transitioning to S3S4. Similarly, if the current changes from positive to negative when the link voltage is positive the state machine toggles between S3S4 and S5S6 rather than properly transitioning to S7S8. If the current changes from negative to positive when the link voltage is positive the state machine toggles between S3S4 and S5S6 rather than properly transitioning to S1S2.

To prevent from these failure cases, current changes during one voltage interval must be big enough or predetermined limit value must be big enough. However, we cannot choose any small number as our limit value to remove the failures cases because the limit value must be higher than the latching current of the thyristors in the circuit. If load current is lower than latching current, the thyristor turns off and current cannot freewheel through the thyristors. Therefore, it is assumed that current magnitude change for half of the link voltage period is higher than two times of the thyristor latching current value so the introduced failure cases do not happen. To meet this condition, it is assumed that link voltage is high enough, link frequency is low enough and output inductance is small enough so current magnitude change is high enough. However, these conditions limit the applications of the topology and thus the commutation technique. Therefore, it is necessary to develop an enhanced commutation technique which also does not require dead time but which is not limited by the constraints of the original assumptions. The proposed method removes all the cases that cause commutation failure.

2.6 Conclusion

In this chapter, the previous commutation technique, which is based on a state machine with four states, is investigated. The commutation technique commutates the

switching pairs well if the link voltage polarity does not change while the current is near the zero-crossing point. However, if the link voltage changes its polarity while current is near the zero crossing point, there are three possible failure cases. Each failure case is studied and the link voltage and the output current figures show three different failure cases in four different conditions. Each failure case is explained four times because during the failure process, the link voltage can be positive and negative and the current direction can change from positive to negative or from negative to positive. It is concluded that it is necessary to develop a new commutation method which can eliminate these three failure cases so we can eliminate the switching frequency limitation, the link voltage magnitude limitation and the load inductance limitation.

3. NEW COMMUTATION TECHNIQUE[*]

3.1 Introduction

In this chapter, the new commutation technique will be introduced and its detail operation process will be discussed. The new commutation technique is based on a state machine with 12 states and the state machine needs information regarding the magnitude and the direction of the output current, the polarity of the link voltage and the PWM values. There are four switching pairs so three states represent one switching pair. While the current is not near the zero crossing point, the commutation process is the same as the previous method. However, to prevent distortions which can occur during the previous method commutation technique process, when the magnitude of the load current is lower than the limit value which we set, the commutation technique is different from the previous method. The new state machine, the inputs for the state machine will be discussed in chapter 3.2.

The detail operation cases of the new method will be investigated in this chapter. There are three different operating cases. The operation case 1, which will be presented in section 3.3, has the same commutation process as the previous method. Therefore, case 1 is the case when the link voltage does not change its polarity while the output current magnitude is lower than the limit value. The operating case 2, which will be discussed in chapter 3.4, removes the failure case 1 and 2 in the previous method.

[*] © 2016 IEEE. Reprinted, with permission, from M. Kim and R.S. Balog, "Commutation technique for high frequency link inverter without operational limitations and dead time," 8th Annual IEEE Energy Conversion Congress and Exposition (ECCE), September, 2016.

Although they are different failure cases, the same commutation process can solve these two failure cases' problems. The operation case 3, which will be discussed in chapter 3.5, show how the new commutation method can remove failure case 3 from the previous method. Each method will be explained using the link voltage and the output current figures and state machine figures.

3.2 New state machine

Figure 24 shows the enhanced commutation technique state machine which can overcome the failure cases in the previous method. There are three states which represent one switching pair. For example, S1S2, S1S2', S1S2" all represent the state to turn on (S1,S2). The states which are denoted as S1S2, S3S4, S5S6, S7S8 are the states for when the current polarity is not changing and current magnitude exceeds the limit values. The other states are the states during the current sign transition. The difference between states are that if the state is S1S2', S3S4', S5S6' or S7S8', the switches are always on regardless of the PWM value. In other states, switches are on when only PWM value is '1'.

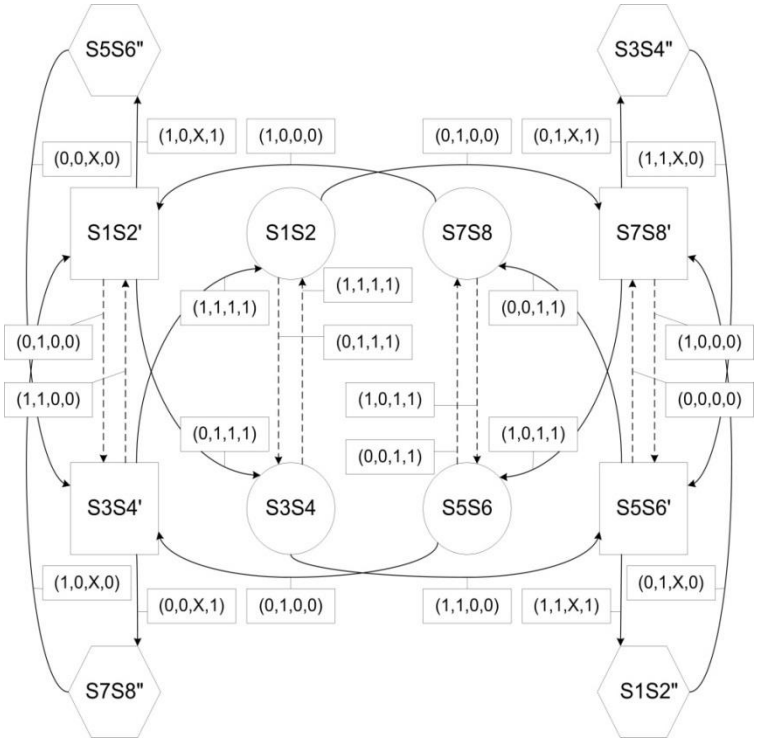

Figure 24. State machine for the new commutation method

Table 6. Inputs of new state machine

	1	0
Input 1	Link voltage > 0	Link voltage < 0
Input 2	Output current > 0	Output current<0
Input 3	|Output current|>limit	|Output current|<limit
Input 4	Incoming switches PWM =1	Incoming switches PWM =0

There are four inputs in this state machine. Table 6 shows how input values are chosen. The first input is the sign of link voltage; the second the output current polarity; the third is the magnitude of the output current; and the fourth input is the incoming

PWM value of incoming switches. The term “incoming switches” mean the switches that are about to turn on. Since the multi-carrier PWM method [7] is used, there are two PWM signals created in the usual sine-sawtooth modulation way. The two different PWMs are generated by the same carrier function but the modulation functions for the PWMs are 180 degree phase shifted to each other. The PWM signal used for (S1,S2) and (S3,S4) is denoted PWM1 and the PWM signal for (S5,S6) and (S7,S8) is PWM2. In the state machine, in Figure 24, ‘x’ means “don’t care”.

3.3 New method operation case 1

Table 7. New commutation intervals from Figure 8

Time	Switches	state
~t0	Freewheeling through S3S4	S3S4
t0~t1	S1S2 turned on	S1S2
t1~t2	Freewheeling through S1S2	S1S2
t2~t3	S7S8 gated, freewheeling through S1S2	S7S8’
t3~t4	Freewheeling current commutates to S7S8	S7S8’
t4~t5	Freewheeling through S7S8	S7S8’
t5~	Freewheeling current commutates to S5S6	S5S6

Table 7 shows the state and turned on switches during the commutation which is shown in Figure 8. In this condition, since current changes during one voltage interval are the same, both the previous state machine and the new state machine work fine. In Figure 8 before t0, through (S3,S4), current is freewheeling. Then at t0, voltage direction

is positive, output current is positive, current magnitude value is higher than the limit value and the PWM value for the incoming switch pair which is (S1,S2) becomes 1 so the input for the state machine is (1,1,1,1). Therefore the state changes from S3S4 to S1S2 and current flows through (S1,S2) and the magnitude of the current increases. From t1 to t2, (S1,S2) is on but since the link voltage is negative, current freewheels through (S1,S2). At t2, the current magnitude becomes less than the limit value, input voltage is negative, current direction is positive and the PWM value of the incoming switch that is (S7,S8) is -1. Therefore the input for the state machine is (0,1,0,0) and the state becomes S7S8' and the gate signal is given to (S7,S8). Since the current value is small, regardless of PWM values, gate signals are given to (S7,S8). At t3, current changes its direction and current flows through (S7,S8) from t3 to t4. At t4, input voltage sign changes so current magnitude starts decreasing but the state is still S7S8'. At t5, input voltage is positive, current is negative and its magnitude is higher than the limit value and the PWM value for incoming switches is 1 so input for the state machine is (1,0,1,1) and (S5,S6) is turned on.

Table 8. New commutation intervals from Figure 9

Time	Switches	state
~t0	Freewheeling through S1S2	S1S2
t0~t1	S3S4 turned on	S3S4
t1~t2	Freewheeling through S3S4	S3S4
t2~t3	S5S6 gated, freewheeling through S3S4	S5S6’
t3~t4	Freewheeling current commutates to S5S6	S5S6’
t4~t5	Freewheeling through S5S6	S5S6’
t5~	Freewheeling current commutates to S7S8	S7S8

Table 9. New commutation intervals from Figure 10

Time	Switches	state
~t0	Freewheeling through S7S8	S7S8
t0~t1	S5S6 turned on	S5S6
t1~t2	Freewheeling through S5S6	S5S6
t2~t3	S3S4 gated, freewheeling through S5S6	S3S4’
t3~t4	Freewheeling current commutates to S3S4	S3S4’
t4~t5	Freewheeling through S3S4	S3S4’
t5~	Freewheeling current commutates to S1S2	S1S2

Table 8, 9 and 10 show operation case 1 during commutation from (S3,S4) to (S5,S6), from (S5,S6) to (S3,S4) and from (S7,S8) to (S1,S2) respectively.

Table 10. New commutation intervals from Figure 11

Time	Switches	state
~t0	Freewheeling through S5S6	S5S6
t0~t1	S7S8 turned on	S7S8
t1~t2	Freewheeling through S7S8	S7S8
t2~t3	S1S2 gated, freewheeling through S7S8	S1S2’
t3~t4	Freewheeling current commutates to S1S2	S1S2’
t4~t5	Freewheeling through S1S2	S1S2’
t5~	Freewheeling current commutates to S3S4	S3S4

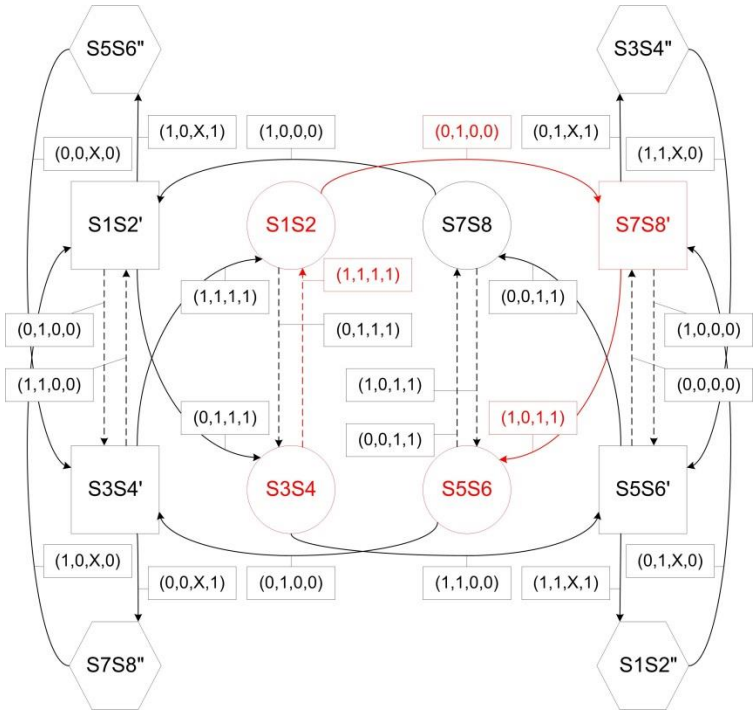

Figure 25. New commutation state transitions for the commutation in Figure 8

Even though the previous commutation technique and the new technique lead to the same result, the new technique is more reliable because in the new state machine,

there is S7S8’ state and if current is higher than the limit value and PWM is 1, the state becomes S5S6. Therefore, there is no possibility that state becomes S1S2 again and toggles between S7S8 and S1S2. In Figure 25, the red lines show how the state changes during this commutation. Figure 26 presents the commutation which is described in Figure 8 and Figure 25.

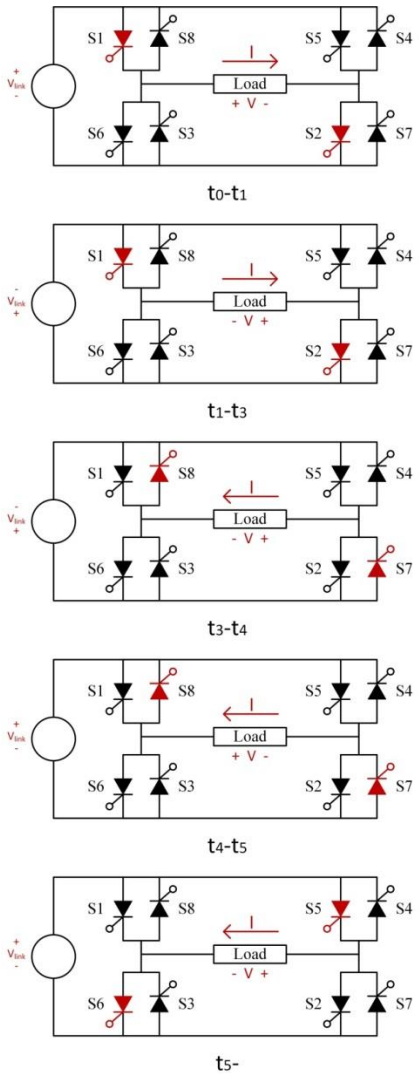

Figure 26. Operation case 1, commutation between (S1,S2) and (S7,S8)

3.4 New method operation case 2

Table 11. New commutation intervals from Figure 9

Time	Switches	state
~t0	Freewheeling through S3S4	S3S4
t0~t1	S1S2 turned on	S1S2
t1~t2	Freewheeling through S1S2	S1S2
t2~t3	S7S8 gated, freewheeling through S1S2	S7S8’
t3~t4	Freewheeling current commutates to S7S8	S7S8’
t4~	Current commutates to S5S6	S5S6'

Figures from Figure 12 to Figure 23 describe the three cases when only the new commutation method can work without trouble. Failure case 1 and 2 can be considered as the same operation case because how the state machine changes is the same for both failure cases. Table 11 shows how the new state machine works in Figure 12. Before t4, there is no difference between Figure 8 and Figure 12 but at t4, input voltage changes its sign when current magnitude is still between +limit and –limit. At this time, voltage is positive, current is negative and current magnitude is lower than the limit value so the input for the state machine is (1,0,0,0). Thus, the state changes from S7S8’ to S5S6’ and (S5,S6) is on regardless of the PWM value so current magnitude increases. Then after the magnitude of the current is high enough the state will change from S5S6’ to S7S8. Figure 27 shows the state changes during this commutation case and Table 11 shows the case in Figure 12. Figure 28 presents more details about how the commutation occurs. Table 12, 13 and 14 show operation case 2 and previous method failure case 1 during

commutation from (S3,S4) to (S5,S6), from (S5,S6) to (S3,S4) and from (S7,S8) to (S1,S2) respectively.

Table 12. New commutation intervals from Figure 10

Time	Switches	state
~t0	Freewheeling through S1S2	S1S2
t0~t1	S3S4 turned on	S3S4
t1~t2	Freewheeling through S3S4	S3S4
t2~t3	S5S6 gated, freewheeling through S3S4	S5S6’
t3~t4	Freewheeling current commutates to S5S6	S5S6’
t4~	Current commutates to S7S8	S7S8'

Table 13 New commutation intervals from Figure 11

Time	Switches	state
~t0	Freewheeling through S7S8	S7S8
t0~t1	S5S6 turned on	S5S6
t1~t2	Freewheeling through S5S6	S5S6
t2~t3	S3S4 gated, freewheeling through S5S6	S3S4’
t3~t4	Freewheeling current commutates to S3S4	S3S4’
t4~	Current commutates to S1S2	S1S2'

Table 14. New commutation intervals from Figure 12

Time	Switches	state
~t0	Freewheeling through S7S8	S5S6
t0~t1	S5S6 turned on	S7S8
t1~t2	Freewheeling through S7S8	S7S8
t2~t3	S1S2 gated, freewheeling through S7S8	S1S2’
t3~t4	Freewheeling current commutates to S1S2	S1S2’
t4~	Current commutates to S3S4	S3S4'

Table 15. New commutation intervals from Figure 16

Time	Switches	state
~t0	Freewheeling through S3S4	S3S4
t0~t1	S1S2 turned on	S1S2
t1~t2	Freewheeling through S1S2	S1S2
t2~t3	S7S8 gated, freewheeling through S1S2	S7S8’
t3~t4	Freewheeling current commutates to S7S8	S7S8’
t4~t5	Freewheeling through S7S8	S7S8'
t5~	Freewheeling current commutates to S5S6	S5S6’

Table 15 illustrates the enhanced PWM for the case in Figure 13. Before t5, it works like Figure 5 or Figure 9. However, at t5, the current magnitude becomes less than limit value, input voltage is positive, current direction is negative and PWM is still -1. Then the input for the state machine is (1,0,0,0) so the state becomes S5S6’ from S7S8’ and gate signal for (S5,S6) is always given regardless of PWM values. Since current flows through (S5,S6) and the input voltage is positive, current magnitude increases. The state transition flow is the same with Figure 12 so Figure 19 shows how the state

machine works for this case. The difference between this case and the case in Figure 8 is that in Figure 12, the state changes from S7S8’ to S5S6’ at t4 and in Fig. 8, the transition occurs at t5. However, since how the states in the state machine changes is the same with failure case 2, both failure case 1 and 2 are new method operation case 2. Table 16, 17 and 18 show operation case 2 and previous method failure case 2 during commutation from (S3,S4) to (S5,S6), from (S5,S6) to (S3,S4) and from (S7,S8) to (S1,S2) respectively.

Table 16. New commutation intervals from Figure 17

Time	Switches	state
~t0	Freewheeling through S1S2	S1S2
t0~t1	S3S4turned on	S3S4
t1~t2	Freewheeling through S3S4	S3S4
t2~t3	S5S6 gated, freewheeling through S3S4	S5S6’
t3~t4	S5S6 turned on	S5S6’
t4~t5	Freewheeling through S5S6	S5S6'
t5~	Freewheeling current commutates to S7S8	S7S8’

Table 17. New commutation intervals from Figure 18

Time	Switches	state
~t0	Freewheeling through S7S8	S7S8
t0~t1	S5S6turned on	S5S6
t1~t2	Freewheeling through S5S6	S5S6
t2~t3	S3S4 gated, freewheeling through S5S6	S3S4’
t3~t4	S3S4 turned on	S3S4’
t4~t5	Freewheeling through S3S4	S3S4'
t5~	Freewheeling current commutates to S1S2	S1S2’

Table 18. New commutation intervals from Figure 19

Time	Switches	state
~t0	Freewheeling through S5S6	S5S6
t0~t1	S7S8turned on	S7S8
t1~t2	Freewheeling through S7S8	S7S8
t2~t3	S1S2 gated, freewheeling through S7S8	S1S2’
t3~t4	S1S2 turned on	S1S2’
t4~t5	Freewheeling through S1S2	S1S2'
t5~	Freewheeling current commutates to S3S4	S3S4’

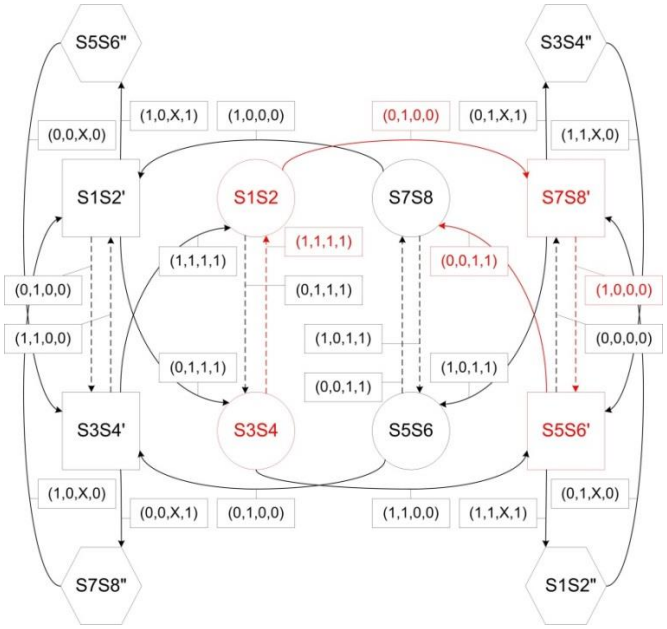

Figure 27. New commutation state changes for the commutation in Figure 12 and Figure 16

In Figure 27, the red lines show how the state changes during this commutation. Figure 28 presents the commutation which is described in Figure 12, Figure 16 and Figure 27.

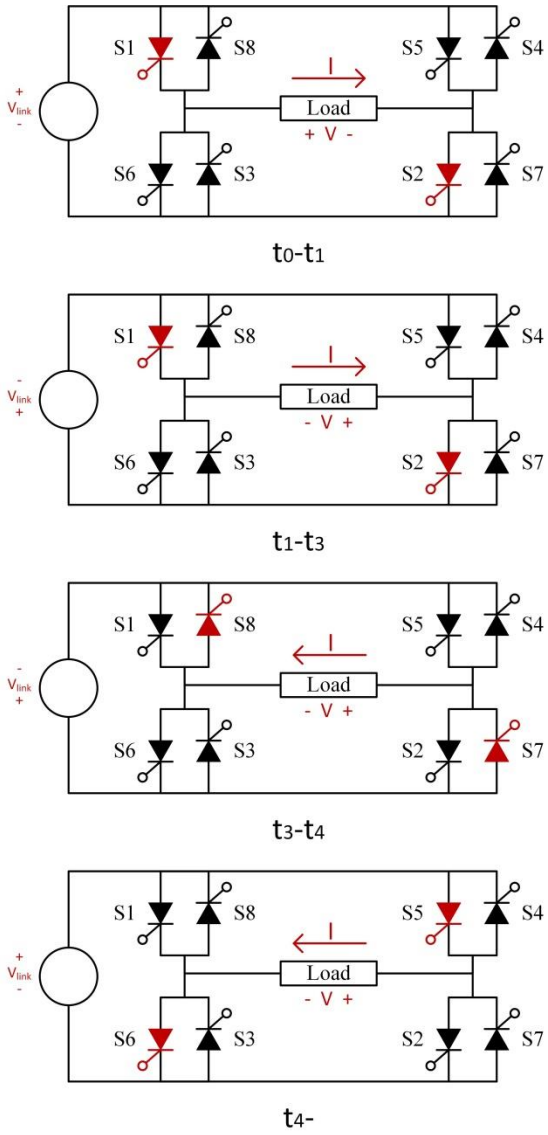

Figure 28. Operation case 2, commutation between (S1,S2) and (S7,S8)

3.5 New method operation case 3

Table 19. New commutation intervals from Figure 20

Time	Switches	state
~t0	Freewheeling through S3S4	S3S4
t0~t1	S1S2 turned on	S1S2
t1~t2	Freewheeling through S1S2	S1S2
t2~t3	S7S8 gated, freewheeling through S1S2	S7S8’
t3~t4	Freewheeling current commutates to S3S4	S3S4”
t4~t5	S5S6 gated, freewheeling through S3S4	S5S6’
t5~t6	Freewheeling current commutates to S5S6	S5S6’
t6~t7	Current commutates to S7S8	S7S8’
t7~t8	Freewheeling through S5S6	S5S6
t8~	Freewheeling current commutates to S5S6	S5S6

Table 19 shows the case in Figure 20. This case is similar to Figure 12 because when current magnitude is lower than limit value, voltage changes its polarity. However, in Figure 17 when voltage changes its sign, current is positive and in Figure 12 when voltage changes its sign, current is negative. In Figure 20 case, at t3, the PWM value becomes 1, while input voltage is negative, current is positive. The input for the state machine is (0,1,0,1) so (S3,S4) is turned on and the state changes from S7S8’ to S3S4”. When the current state is S3S4”, when voltage becomes positive, the state changes from S3S4” to S5S6’. Therefore, at t4 S5S6 is gated and regardless of the PWM value, gate signals are given to (S5,S6) but before t5 current freewheels though (S3,S4). At t5, current changes its direction and (S5,S6) is on. At t6, input voltage becomes negative, current is negative and current magnitude is lower than the limit value so the input for the state machine is (0,0,0,0) so the state changes from S5S6’ to S7S8’. From t6 to t7,

gate signal for (S7,S8) is given so current flows through (S7,S8) and current magnitude increases. At t7, state does not change but voltage becomes positive so current freewheels through (S7,S8). At t8, input voltage is positive, output current is negative, current magnitude is higher than the limit value and the PWM is 1. Therefore, the input for the state machine is (1,0,1,1) so the state becomes S5S6 and (S5,S6) is turned on. Unlike operation case 1 and 2, this case also uses the double prime state, S3S4".

Table 20. New commutation intervals from Figure 21

Time	Switches	state
~t0	Freewheeling through S1S2	S1S2
t0~t1	S3S4 turned on	S3S4
t1~t2	Freewheeling through S3S4	S3S4
t2~t3	S5S6 gated, freewheeling through S3S4	S5S6'
t3~t4	Freewheeling current commutates to S1S2	S1S2"
t4~t5	S7S8 gated, freewheeling through S1S2	S7S8'
t5~t6	Freewheeling current commutates to S7S8	S7S8'
t6~t7	Current commutates to S5S6	S5S6'
t7~t8	Freewheeling through S7S8	S7S8
t8~	Freewheeling current commutates to S7S8	S7S8

Table 20, 21 and 22 show operation case 3 and previous method failure case 3 during commutation from (S3,S4) to (S5,S6), from (S5,S6) to (S3,S4) and from (S7,S8) to (S1,S2) respectively.

Table 21. New commutation intervals from Figure 22

Time	Switches	state
~t0	Freewheeling through S7S8	S7S8
t0~t1	Freewheeling current commutates to S5S6	S5S6
t1~t2	Freewheeling through S5S6	S5S6
t2~t3	S3S4 gated, freewheeling through S5S6	S3S4’
t3~t4	S7S8 turned on	S7S8”
t4~t5	S1S2 gated, freewheeling through S7S8	S1S2’
t5~t6	Freewheeling current commutates to S1S2	S1S2’
t6~t7	Current commutates to S3S4	S3S4’
t7~t8	Freewheeling through S3S4	S1S2
t8~	Freewheeling current commutates to S1S2	S1S2

Table 22. New commutation intervals from Figure 23

Time	Switches	state
~t0	Freewheeling through S5S6	S5S6
t0~t1	Freewheeling current commutates to S7S8	S7S8
t1~t2	Freewheeling through S7S8	S7S8
t2~t3	S1S2 gated, freewheeling through S7S8	S1S2’
t3~t4	S5S6 turned on	S5S6”
t4~t5	S3S4 gated, freewheeling through S7S8	S3S4’
t5~t6	Freewheeling current commutates to S3S4	S3S4’
t6~t7	Current commutates to S1S2	S1S2’
t7~t8	Freewheeling through S3S4	S3S4
t8~	Freewheeling current commutates to S3S4	S3S4

In Figure 29, the red lines show how the state changes during this commutation.

Figure 30 presents the commutation which is described in Figure 20 and Figure 29.

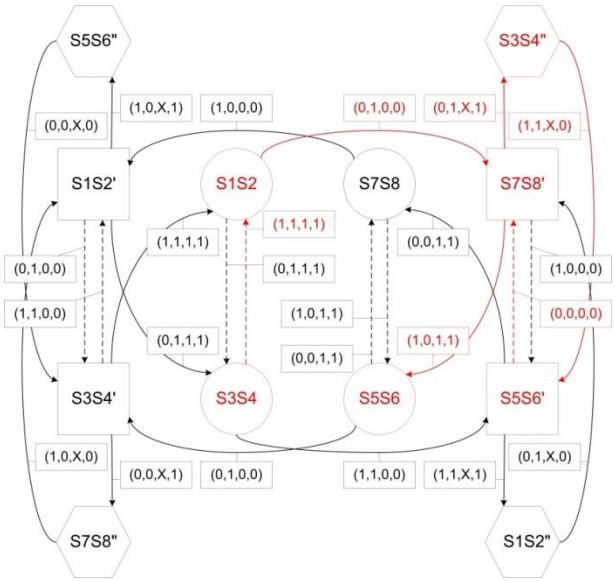

Figure 29. New commutation state changes for the commutation in Figure 20

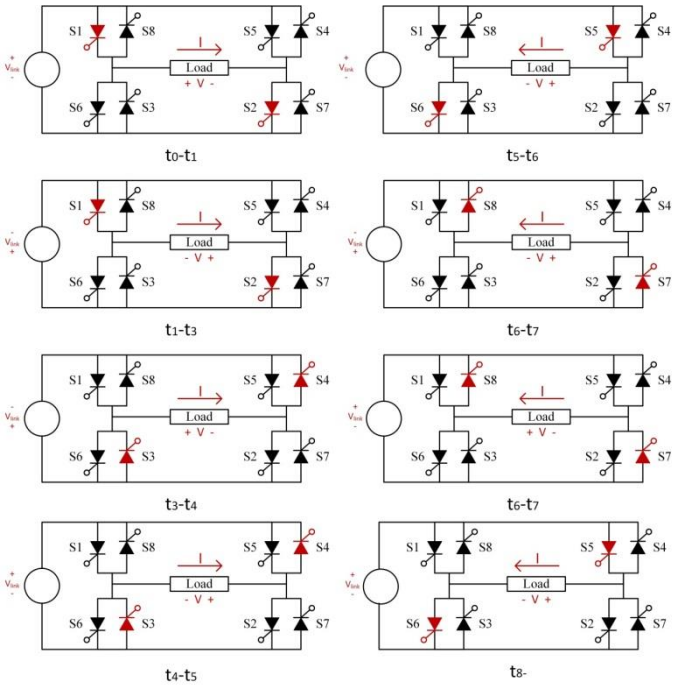

Figure 30. Operation case 3, commutation between (S1,S2) and (S7,S8)

The cases show how the new state machine removes all the possible failures that can possibly happen in the previous technique when current changes its direction from positive to negative while the link voltage is negative. This new commutation technique also works when current changes its direction from negative to positive and when the current direction change occurs while voltage is positive.

3.6 Conclusion

The new state machine is investigated in this chapter. The key idea of this new state machine is that we have four states that are steady state and the other eight states are transition states. The states for steady states are represented as S1S2, S3S4, S5S6 and S7S8 and these states are only for when the current is higher than the limit value. The other eight states are only used when the load current is changing its direction; these transition states prevent the state from being one of the steady states when current is not higher than limit value. Therefore, by adding eight transition states to the previously suggested state machine the assumption it had is removed.

4. RESULT AND DISCUSSION[*]

4.1 Introduction

In this chapter, both the previous commutation method and the new commutation method are simulated and experimented on. The results of both methods will be compared and analyzed. Large number of data will be collected with various switching frequencies, the load inductance, the load resistance and the link voltage magnitude. The collected results reveal that in some cases, the previous method and the new method show the same results but in other cases, distortions are inserted to the previous method results so the THD of the output current of the previous method is worse than the new method results.

4.2 Simulation results

Both the previous commutation technique and the new technique are implemented using Simulink/Matlab. Figure 31 shows output current and the input voltage when the new method is implemented if the link voltage magnitude is 35V, output load has 10 Ω resistance and 20mH inductance and the switching frequency is 2kHz. Figure 32 shows the state changes during the simulation. In this figure, S1S2, S3S4, S5S6 and S7S8 states are indicated as 1, S1S2', S3S4', S5S6' and S7S8' states are indicated as 2 and S1S2",S3S4", S5S6" and S7S8" states are indicated as 3. Figure 32 presents that this simulation case describes figure 8 and previous technique can be used

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for this simulation case so the results of the previous technique will be the same with the new technique.

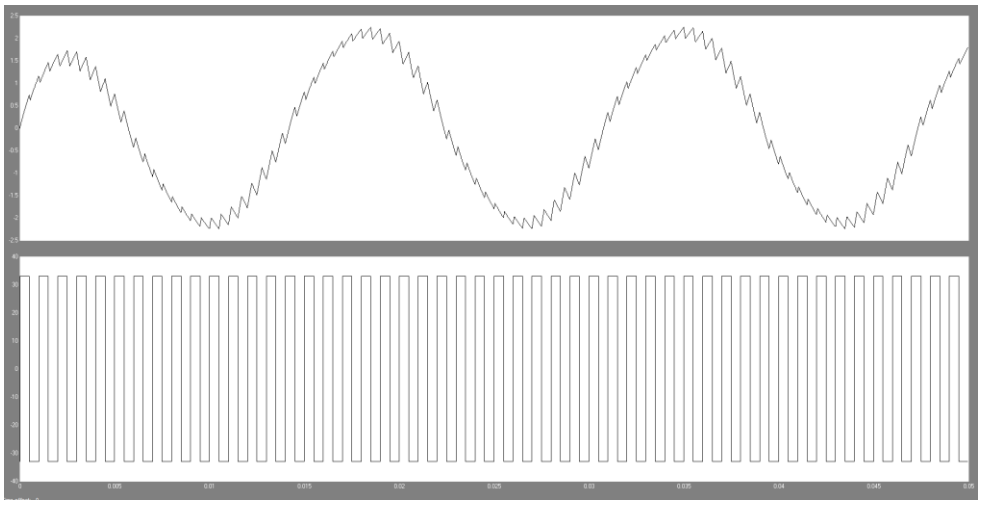

Figure 31. Simulation result describing operation case 1: output current (top) and output voltage (Bottom)

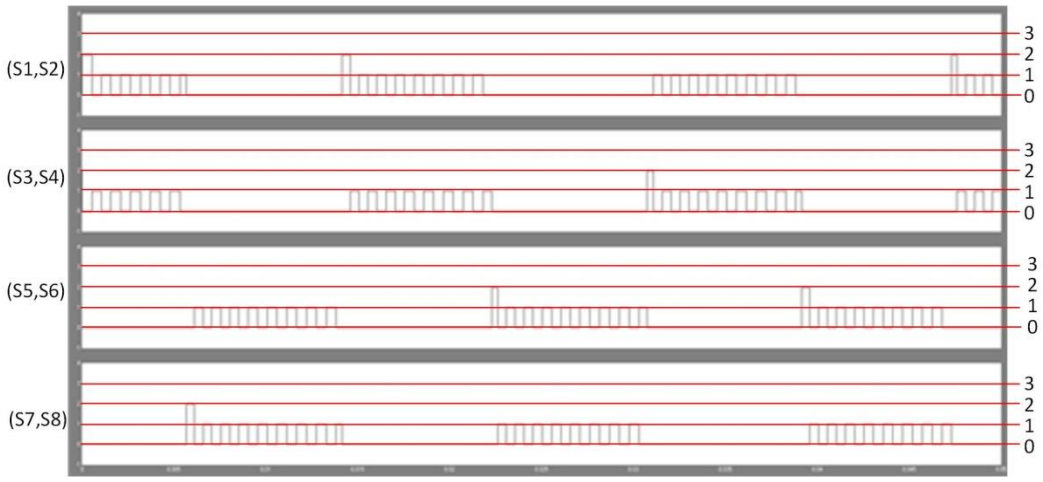

Figure 32. State changes during operation case 1: (S1,S2)(top), (S3,S4)(middle1), (S5,S6)(middle2) and (S7,S8)(Bottom)

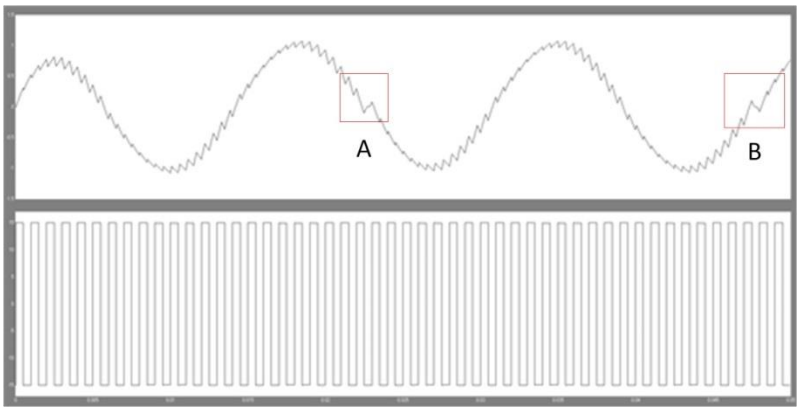

Figure 33. Simulated case 1 and 2 failed commutation: output current (top) and output voltage (Bottom)

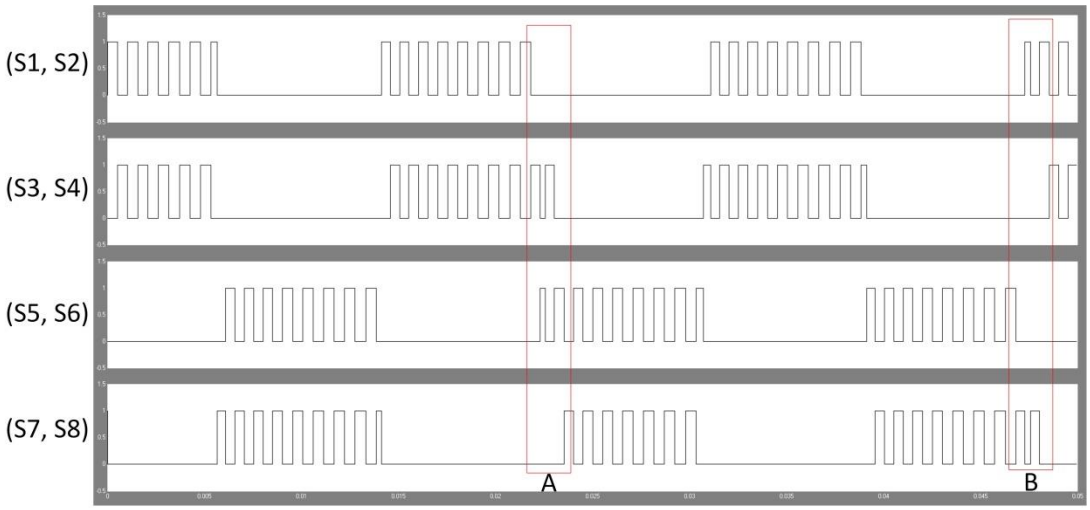

Figure 34. State-changes during failure case 1 and 2: (S1,S2)(top), (S3,S4)(middle1), (S5,S6)(middle2) and (S7,S8)(Bottom)

Figure 33 shows the simulation results of the previous technique and Figure 34 shows the switch pairs during the operation in Figure 33. Figure 34 shows that during A period in the figure, it is supposed to switch its state from S3S4 to S5S6 but the state

toggles a few times. During the period B, the state is supposed to change from S7S8 to S1S2 but the two states toggle so distortion is added to the load current.

Figure 35 shows the simulation results of the new technique if the link voltage magnitude is 17V, output load has 10 Ω resistance and 20mH inductance and the switching frequency is 2kHz . Figure 33 and Figure 35 show that during this simulation, only new method works well.

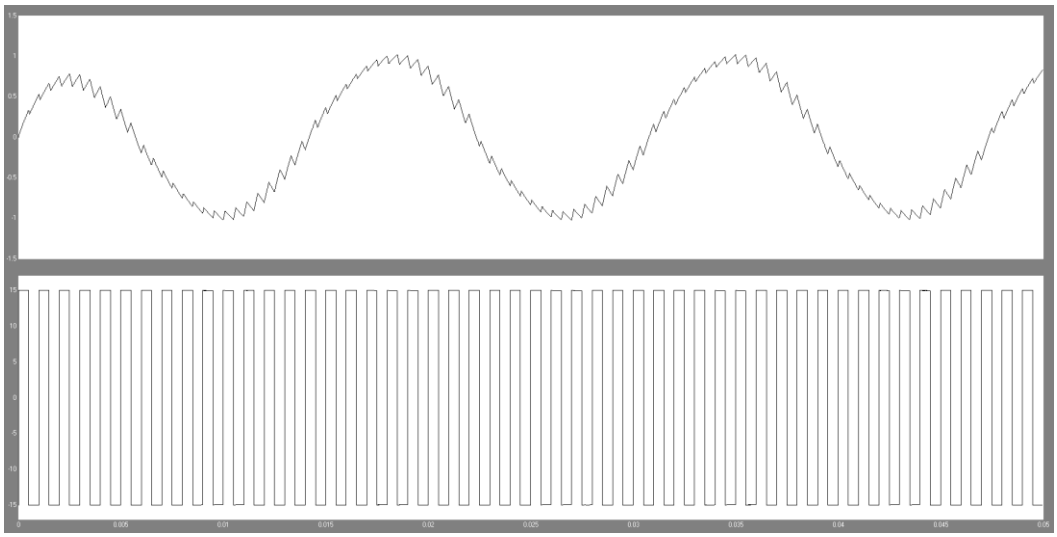

Figure 35. Simulation result describing operation case 2 : output current (top) and output voltage (Bottom)

Figure 36 shows the state changes during the simulation and the figure points out that this simulation case describes operation case 2.

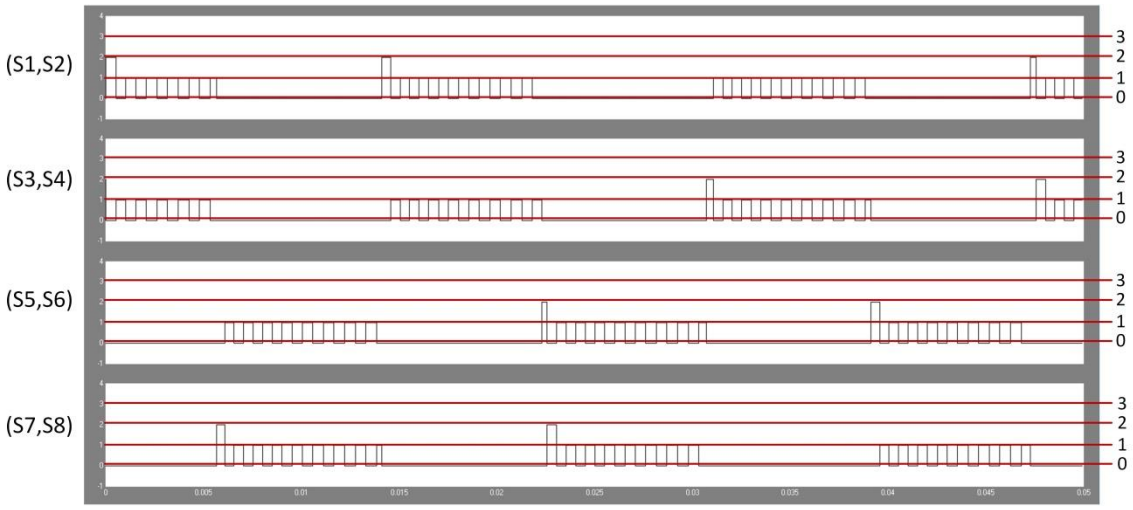

Figure 36. State-changes during operation case 2: (S1,S2)(top), (S3,S4)(middle1), (S5,S6)(middle2) and (S7,S8)(Bottom)

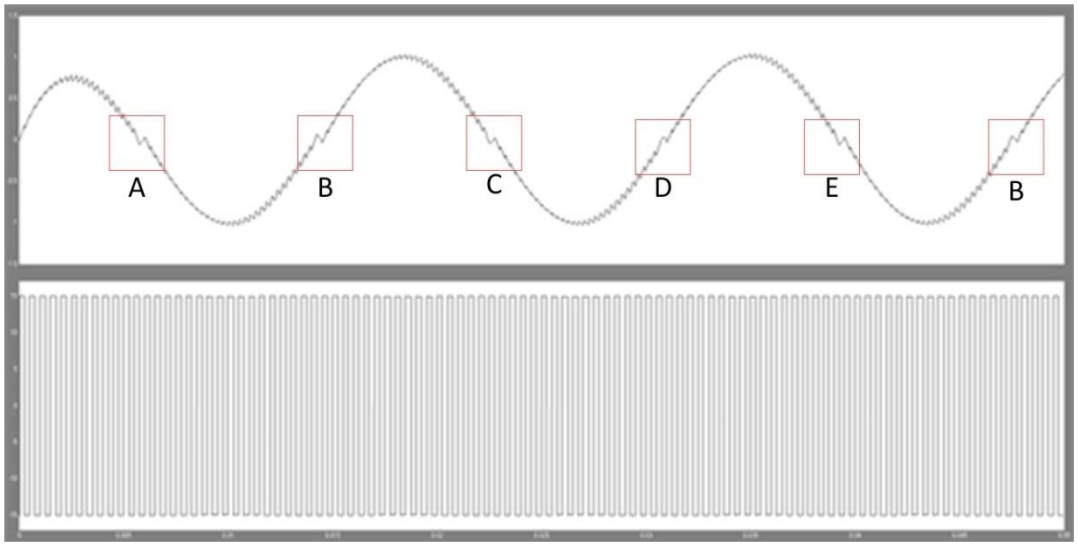

Figure 37. Simulated case 3 failed commutation: output current (top) and output voltage (Bottom)

Figure 37 shows the simulation results of the previous technique and Figure 38 show which switch pair is on. Figure 39 shows the simulation results of the new technique when if the link voltage magnitude is 17V, output load has 10 Ω resistance and 20mH inductance and the switching frequency is 4kHz . Figure 37 and Figure 39 show that during this simulation, only new method works well but the previous method causes some troubles when the current changes its direction.

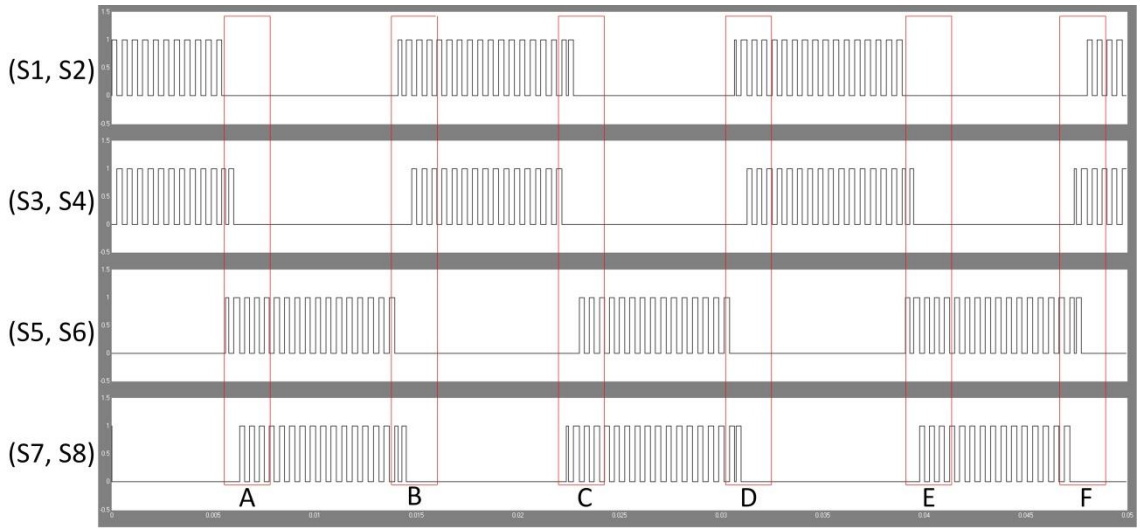

Figure 38. state-changes during failure case 1 and 2: (S1,S2)(top), (S3,S4)(middle1), (S5,S6)(middle2) and (S7,S8)(Bottom)

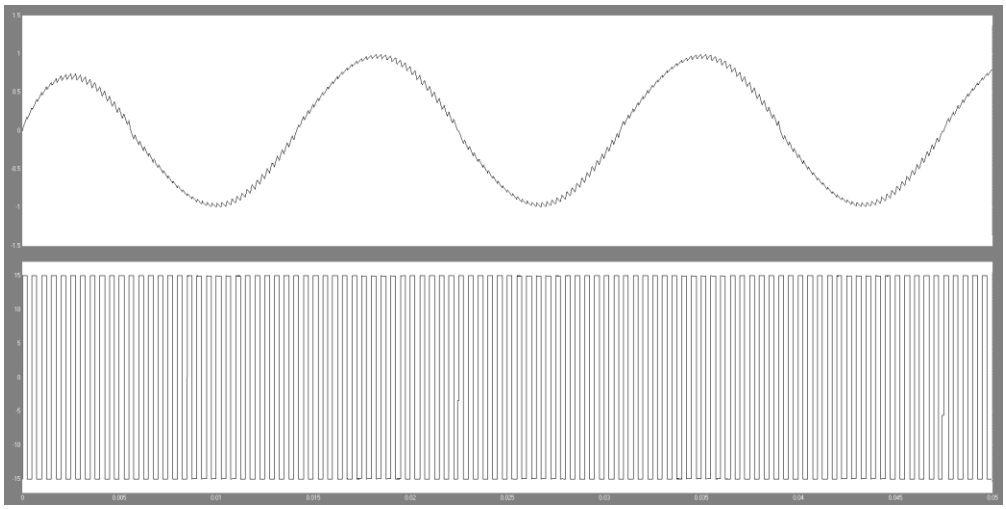

Figure 39. Simulation result describing operation case 3: output current (top) and output voltage (Bottom)

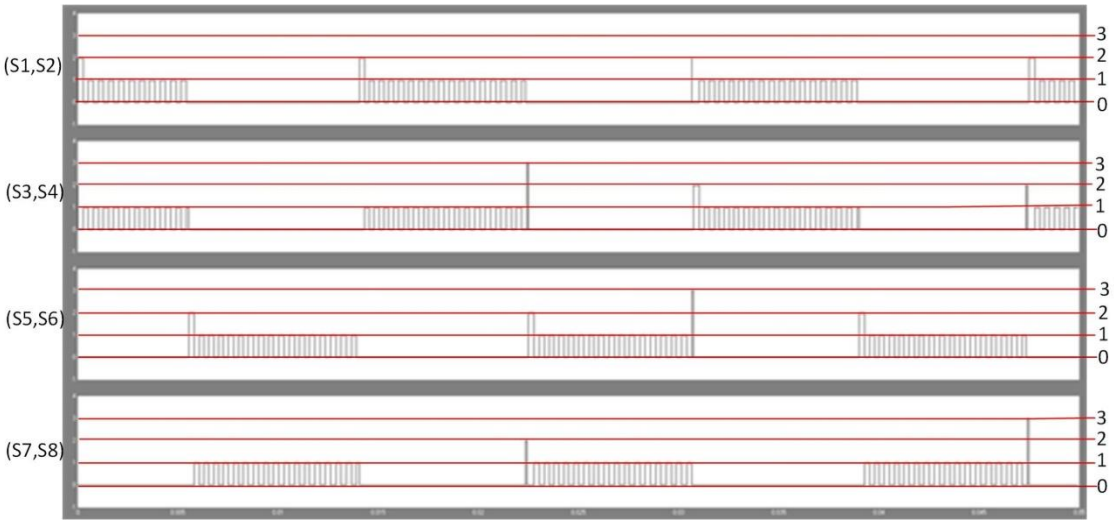

Figure 40. State-changes during operation case 3: (S1,S2)(top), (S3,S4)(middle1), (S5,S6)(middle2) and (S7,S8) (Bottom)

Figure 40 shows the state changes during the simulation. The figure points out that this simulation describes the operation case 3, because when current changes its direction the figure shows the state goes to S1S2", S3S4", S5S6" or S7S8" during the commutation process.

4.3 Experiment results

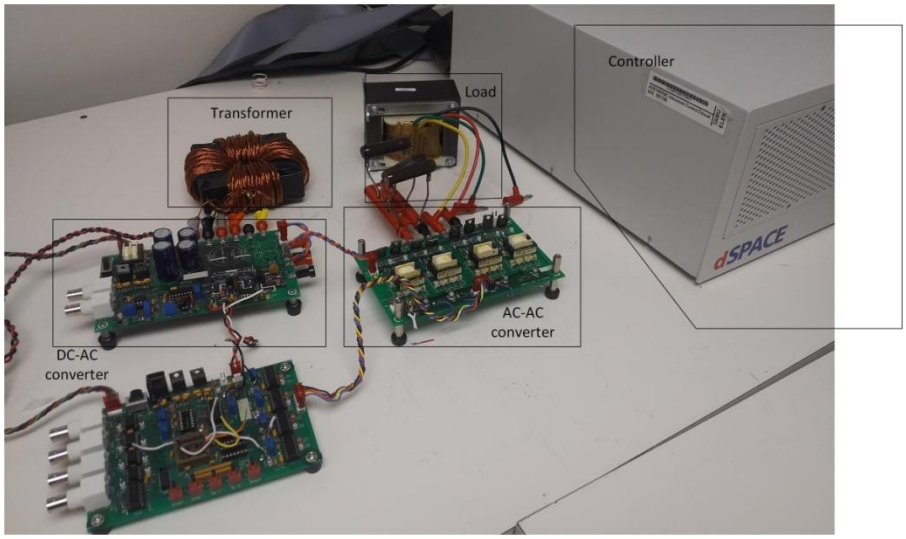

Figure 41. Hardware setup for experiments

Figure 41 is a picture of the hardware for this experiment. The hardware includes a controller, DC-AC inverter, which change a DC voltage to square wave AC voltage, AC-AC converter, which is composed of eight thyristors and a transformer, which provides the galvanic isolation between DC-AC converter and the AC-AC converter.

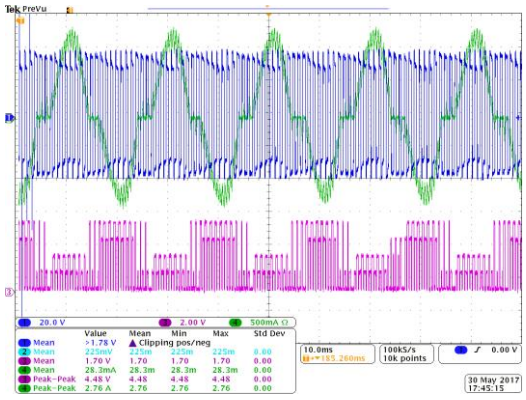

Figure 42. Experiment result, previous method, 5 periods

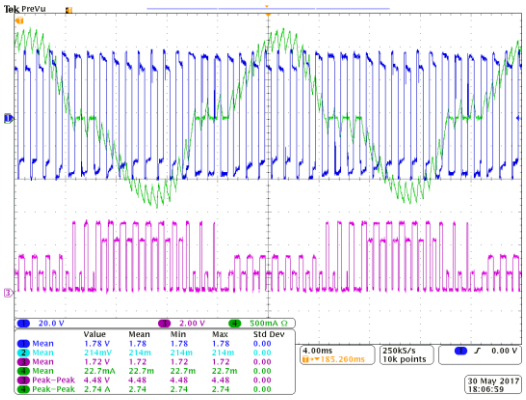

Figure 43. Experiment result, previous method, 2 periods

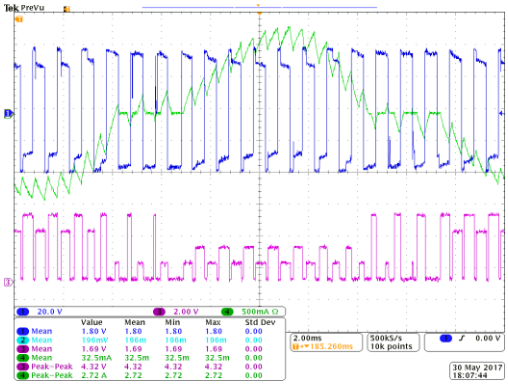

Figure 44. Experiment result, previous method, a period

Figure 42, 43 and 44 show the previous method experiment results and Figure 45, 46 and 47 show the new method experiment result. During the experiment, the magnitude of the link voltage was 18V, the output resistance was 0.78Ω, the output inductance was 32mH and the switching frequency was 1kHz.

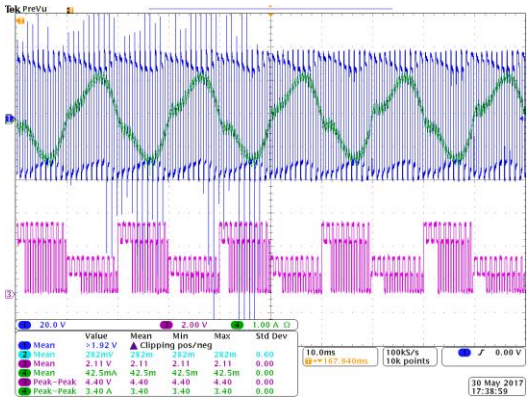

Figure 45. Experiment result, new method, 5 periods

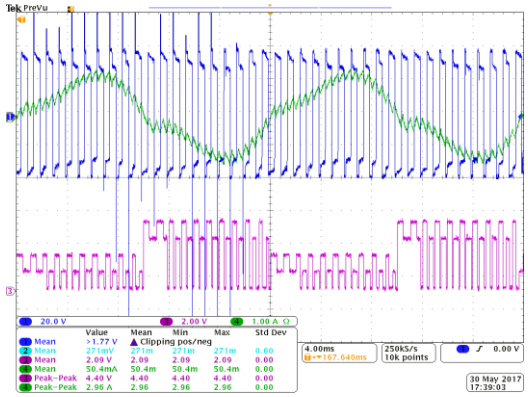

Figure 46. Experiment result, new method, 2 periods

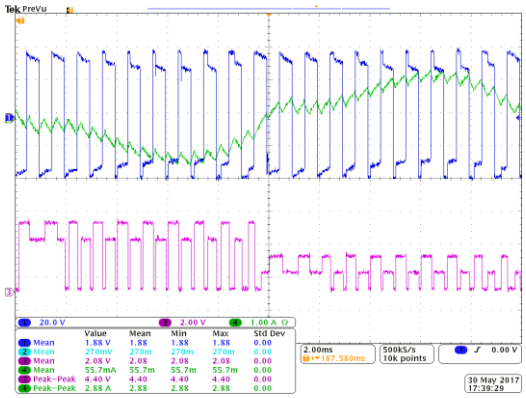

Figure 47. Experiment result, new method, a period

In the figures, channel 1 and 4 show the link voltage and the output current respectively. Channel 3 shows which switching pair is on. If (S1,S2) is gated, the value of channel 3 is 1, if (S3,S4) is gated, the value of channel 3 is 2, if (S5,S6) is gated, the value of channel 3 is 3, if (S7,S8) is gated, the value of channel 3 is 4, if no switching pair is on, the value is 0. The experiment results also show that the new method reduces distortion in the output current.

In the previous method experiment results, channel 3 shows that when the magnitude of the output current is not big enough, switch pairs (S1,S2) and (S7,S8) toggle a few time before the load current becomes larger than the limit value. However, in the new method results, once (S7,S8) is on, (S5,S6) and (S7,S8) toggle and (S1,S2) are not turned on again.

The experiment results show double line frequency ripple on the load current. It increases the THD value and also the power loss in the components. Double line frequency ripple is an inherent feature single phase inverter [41]. Removing these ripples

can be one of the future works. Furthermore, the experiment results also show some voltage notches. Developing better control methods to cancel the voltage notches will be one of the future works too.

4.4 THD analysis

In the previous section, simulation and experiment results are presented and those results show that during operation case 2 and 3, previous methods have some distortions when the magnitude of the output current is close to 0. Therefore, it is expected that more harmonics are included in the output current results from the previous method than the results from the new method. In this section, the THD analysis results of the output current will be presented and these results support that the new method improves the quality of the output current.

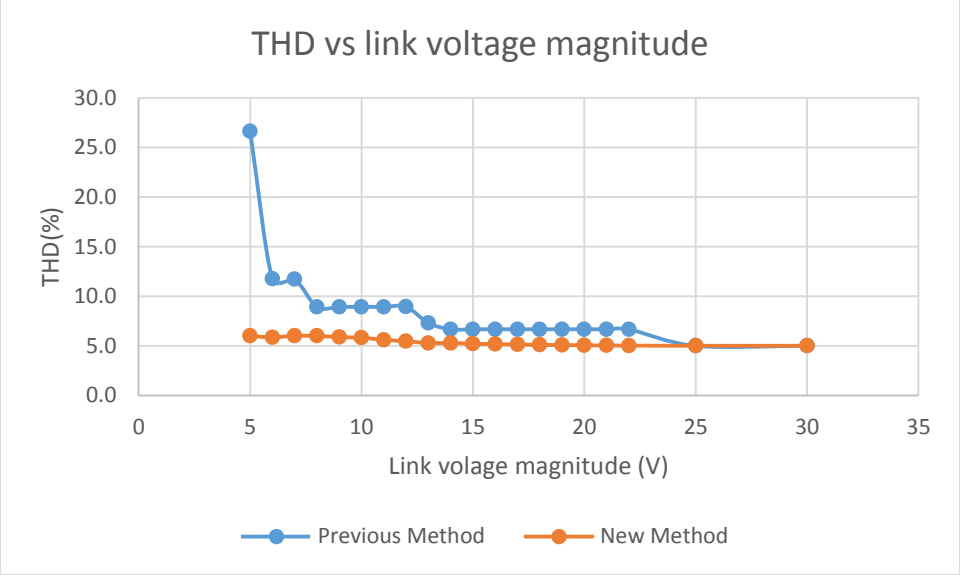

Figure 48. THD vs Vlink

The commutation failures occur from the previous technique because while the current is changing its direction, the link voltage changes its polarity. Therefore, if the current magnitude changes slowly, it is more likely that the previous method produces more distorted output current. Thus, when the magnitude of the link voltage is smaller, the THD difference between the new method and the previous method will be larger. Figure 48 shows THD of output current results from both the new method and the previous method while the link voltage magnitude increases from 5V to 30V. During these simulations, switching frequency was 2kHz, output resistance was 10Ω and the output inductance was 20mH. In this figure, when the link voltage is higher than 25V, there is almost no THD difference between the previous method and the new method but the difference increases when the link voltage decreases.

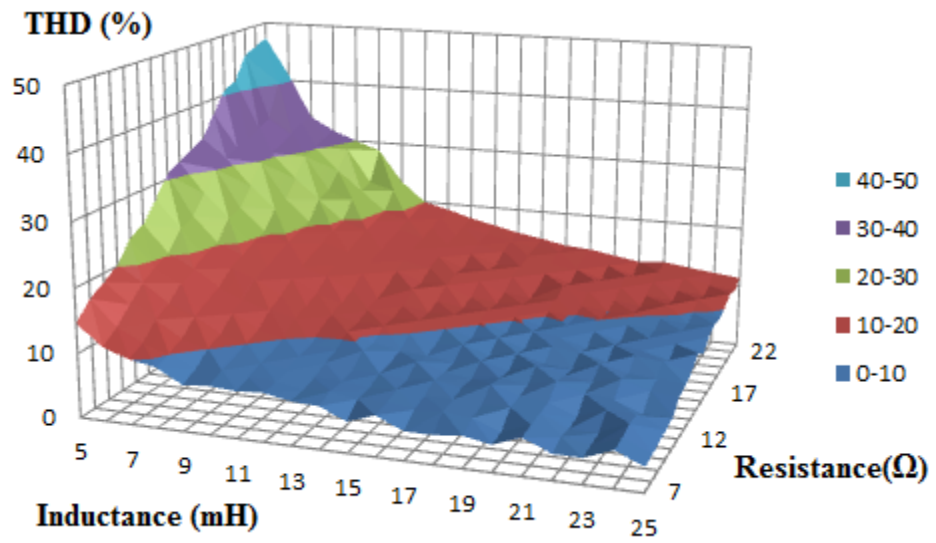

Figure 49. THD, L, R, Previous method

Figure 49 and 50 show how THD values, the load resistance and the load inductance are related. During the simulations for these figures, the link voltage magnitude was 20V and the switching frequency was 2kHz. Figure 43 show THD of the output current of the previous method while the output resistance and the output inductance change. Figure 50 shows the THD analysis results while the new method is applied and the output resistance and the output inductance change. In these two figures, it is common that when the inductance increases and the resistance decreases, the THD values decrease. However, figure 49 which represents the THD values of previous method has more higher values than figure 50 and figure 50 which represents the THD values of the new method has more lower values than figure 49. Therefore, it is observed that the new method lowers the THD values and improves the quality of output current.

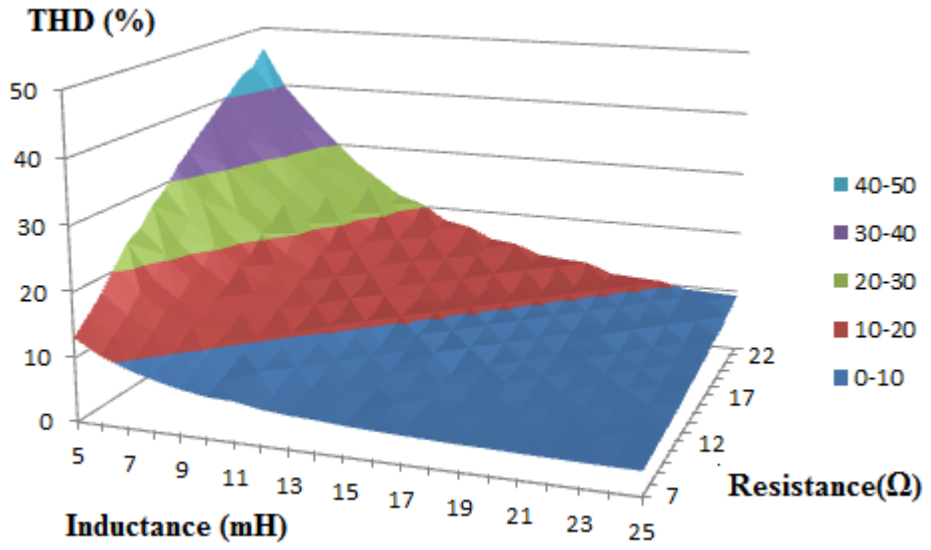

Figure 50. THD, L, R, New method

Figure 51 is the graph which shows the relationship between load inductance and the output current THD values. Figure 51 is when the output resistance is 50Ω and the switching frequency is 1kHz, the voltage magnitude is 120V and the predetermined current limit value is 50mA. In the figure, if the inductance increases, the THD difference between the previous method and the new method also increases. If the output inductance is higher, the current changes more slowly and it is more likely that voltage toggles while current value is between +limit to –limit. The previous method assumes that the voltage polarity stays the same while current changes from –limit to +limit or +limit to –limit. The new method does not have that assumption. Therefore, it is more likely that the previous method has some failures in commutations.

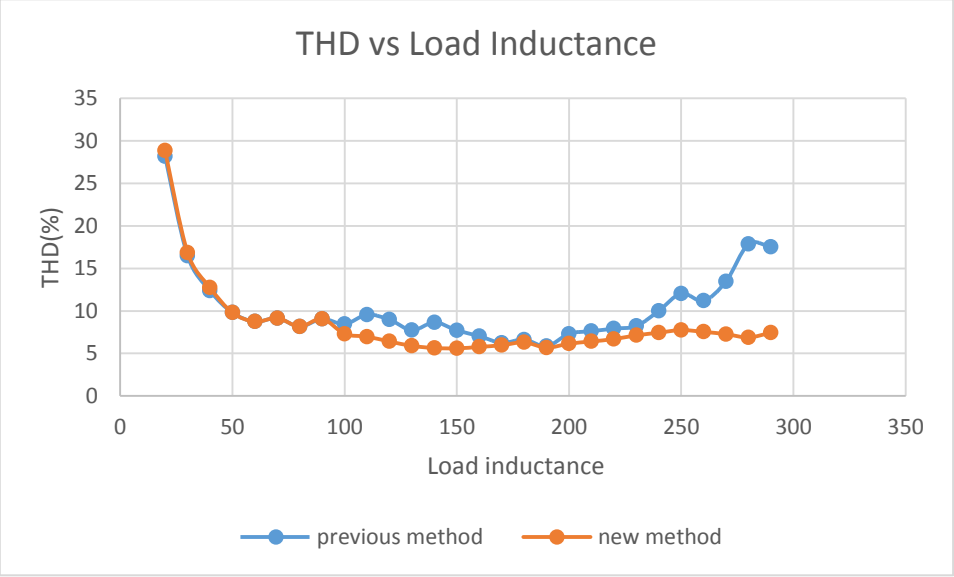

Figure 51. THD vs Load inductance

However, as Figure 51 shows, it is possible that even though the inductance is higher, the assumption is not broken so the previous method has almost the same THD value as the new method. In figure 51, when the load inductance is 180mH and 190mH, the THD values of the previous method are almost the same with the new method THD values. This explains that increasing the output inductance increases the probability that the assumption in the previous method is not met. However, increasing the load inductance is not directly related to the THD value of the output current.

Furthermore, in Figure 51, if the load inductance is 20mH, the new method THD value is higher than the previous method value. The reason is that the new method does not follow the PWM signals if the magnitude of the current is lower than the limit value but the previous method does. Therefore, if it is guaranteed that the current change during one switching interval is high enough, it is possible that the new method has higher THD values because it does not follow the PWM signals.

Figure 52 shows how the THD value changes if the switching frequency changes from 2kHz until 8.5kHz. If switching frequency is higher, the current change during one switching interval is smaller because the period is reduced. Therefore, if the switching frequency is higher, it is more likely that there is commutation failure in the previous method. Figure 46 shows that when the frequency is lower than 3.5kHz, the previous method and the new method show similar THD values. From 3.5kHz, previous method has higher THD values. From 6.5kHz, the THD difference between the previous method and the new method becomes larger.

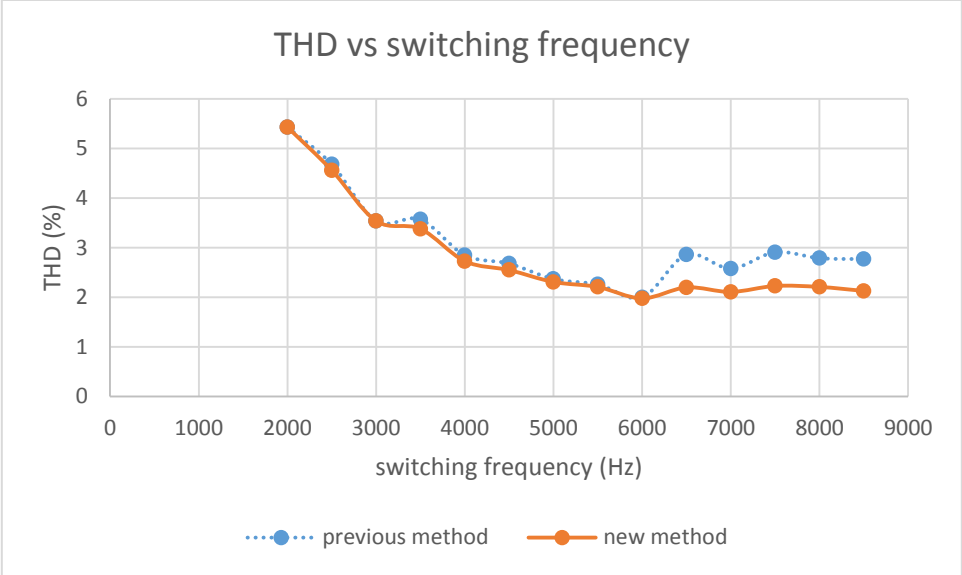

Figure 52. THD vs Switching frequency

As the graphs of THD values and other factors show, at some points, the new method and the previous method show the same result. However, if the current change during one switching interval is not enough so the assumption in the previous method is not met, distortions are added to the previous method output current and the THD values are higher in the previous method. Furthermore, since the new method does not follow the PWM values if the current magnitude is not high enough, at some points the previous method has lower THD values than the new method.

4.5 Conclusion

In this chapter, the simulation results and the experiment results prove that the new method improves the quality of the output current. Both methods are simulated numerous times and three conditions that can show the different operating cases and failure cases are chosen and the output current and the link voltage waveforms are

shown in this chapter. Furthermore, the THD analysis of the load current is presented with different variables such as the link voltage magnitude. The experiment was conducted and its results point out that the new method improves the quality of the output current.

5. CONCLUSIONS*

A new commutation technique based on a state machine method is proposed for a high frequency AC-link, PWM controlled inverter. This method does not require dead time to prevent shoot-through when the current changes polarity or commutates in response to the grid voltage zero cross or PWM command. It also removes the operational limitations that a previous technique placed on the link voltage magnitude, link frequency and output inductance. Simulation results and experiment results have been carried out.

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