A MILLIMETER-WAVE COEXISTENT RFIC RECEIVER ARCHITECTURE IN 0.18-μm SiGe BiCMOS FOR RADAR AND COMMUNICATION SYSTEMS

A Dissertation

by

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ABSTRACT

Innovative circuit architectures and techniques to enhance the performance of several key BiCMOS RFIC building blocks applied in radar and wireless communication systems operating at the millimeter-wave frequencies are addressed in this dissertation. The former encapsulates the development of an advanced, low-cost and miniature millimeter-wave coexistent current mode direct conversion receiver for short-range, high-resolution radar and high data rate communication systems.

A new class of broadband low power consumption active balun-LNA consisting of two common emitters amplifiers mutually coupled thru an AC stacked transformer for power saving and gain boosting. The active balun-LNA exhibits new high linearity technique using a constant gm cell transconductance independent of input-outputs variations based on equal emitters' area ratios. A novel multi-stages active balun-LNA with innovative technique to mitigate amplitude and phase imbalances is proposed. The new multi-stages balun-LNA technique consists of distributed feed-forward averaging recycles correction for amplitude and phase errors and is insensitive to unequal paths parasitic from input to outputs. The distributed averaging recycles correction technique resolves the amplitude and phase errors residuals in a multi-iterative process. The new multi-stages balun-LNA averaging correction technique is frequency independent and can perform amplitude and phase calibrations without relying on passive lumped elements for compensation. The multi-stage balun-LNA exhibits excellent performance from 10 to 50 GHz with amplitude and phase mismatches less than 0.7 dB and 2.86º,

respectively. Furthermore, the new multi-stages balun-LNA operates in current mode and shows high linearity with low power consumption. The unique balun-LNA design can operates well into mm-wave regions and is an integral block of the mm-wave radar and communication systems.

The integration of several RFIC blocks constitutes the broadband millimeter-wave coexistent current mode direct conversion receiver architecture operating from 22-44 GHz. The system and architectural level analysis provide a unique understanding into the receiver characteristics and design trade-offs. The RF front-end is based on the broadband multi-stages active balun-LNA coupled into a fully balanced passive mixer with an all-pass in-phase/quadrature phase generator. The trans-impedance amplifier converts the input signal current into a voltage gain at the outputs. Simultaneously, the high power input signal current is channelized into an anti-aliasing filter with 20 dB rejection for out of band interferers. In addition, the dissertation demonstrates a wide dynamic range system with small die area, cost effective and very low power consumption.

DEDICATION

To my family, Hiyam and Daher Geha, and Rana Nouaime and her family, Rami and Reem Nouaime

For all their love, prayers, and unwavering support

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CHAPTER I

INTRODUCTION

1.1 Background and Motivation

With the ever growing consumers' demands for high data rate wireless communications and high resolution high accuracy sensing and detection, communication and radar networks have congested the low-end frequency spectrum infrastructure. To cope with users end strains, the Federal Communications Commission (FCC) has allocated some unlicensed bands at the microwave and millimeter wave frequency spectrum [1]-[2]. Transceivers targeting microwave and millimeter-wave (mm-wave) applications based on the wireless metropolitan area network standards (802.16) ranging from 10-66 GHz, ultra-wideband short range radar vehicular sensor from 22-29 GHz, and military radar for unmanned aerial vehicle (UAV) from 35-37 GHz [3], etc. are essential to achieve the users end demands. This frequency spectrum allocation still encounters adjacent as well as coexistence channels, similar to lower frequency spectrums, like radio astronomy at 23.6-24 GHz, industrial-scientific-medical (ISM) at 24.05-24.25 GHz, local multipoint-distribution system (LMDS) at 31 GHz, and cloud radar at 35 GHz [4]. In fact, the frequency spectrum presents a dilemma for some sensitive frequency bands where overlapping exists. For that reason, the FCC regulates the effective isotropic radiated power (EIRP) for the ultra-wideband (UWB) devices to limit the radiated emissions and noise on the spectrum. In literature, many transceivers are reported for microwave and mm-wave applications with limited agility using single-

band approach [5]-[13], dual-band design [14]-[15], and lastly wideband RF front-end receivers [16]-[18].

Dedicated transceivers for mm-wave targeting specific applications have come to light in recent years. A 0.18-μm 24 GHz CMOS RF front end was reported in [5]. An automotive short-range and long-range radar sensor for *Ka*- and *W*- bands application with its FCC regulations was addressed in [6]-[7]. Various broadband architectural transceivers designs for the 60 GHz wireless communications are reported in [8]-[10]. Such receivers with single-balanced RF mixers tend to suffer from local oscillator (LO) leakage; thus causing receiver desensitization. Fully integrated using 4 and 8 elements phased array receivers in CMOS for 24 GHz ISM band are reported in [11]-[12]. Further, a fully integrated 77 GHz BiCMOS phased array receiver with dipole antenna on chip for long-range automotive radar sensor is reported in [13].

To increase versatility and functionality, dual-band transceivers/receivers are demonstrated in [14]-[15]. Adding more passive components to achieve dual-bands resonance introduces high signal loss and increases chip area; and hence, increases the power consumption. The dual-bands 24/31 GHz based sub-harmonic receiver architecture in [13] requires fine tuning for the quadrature phases generation schemes as well for amplitude mismatches to improve bands rejection. An automotive dual-bands direct conversion transceiver for collision avoidance is reported in [15]. The large frequency spread of the transceiver frequency planning causes two dedicated local oscillators running at 22 and 77 GHz to be integrated on a single chip. The drawback is more power consumption, larger chip area, and more complex layout floor planning not

to mention the phase noise issues. As we can see; single-band or dual-bands transceivers as reported have limited flexibility and hence creating urgent needs to address these problems.

A more desired approach targets wideband RF front-end transceivers to increase functionality and have the capabilities to support multiple standards simultaneously suffers from limited linearity and high noise figure [16]-[18], thus limiting the receiver dynamic range.

A millimeter-wave coexistent wideband direct conversion receiver for multi-standard multi-band radar and communication systems translates simultaneously the entire frequency spectrum and provides more capabilities and numerous advantages as compared to the single and non-optimized dual-band counterparts. More functionality can be clearly seen in the fact that more information is transmitted and received, and more remote targets are sensed simultaneously on coexistent multiple channels system. Working on wideband spectrum makes the systems more robust to the fluctuation of the propagation environment such as severe multi-path fading, urban settings, and mountainous terrains or frequency-dependence attenuation. Coexistent multi-standards multi-band operations can be implemented using a single system leading to substantial benefits including reduced die area, high density IC integration, low cost, and low power consumption. However, the design of multi-mode multiband system is challenging and requires new techniques to design the circuits' blocks efficiently with optimized performances.

In order to meet the high demands for short-range radar and communication

systems in the future, we need to develop miniaturized, highly integrated SoC (System on Chip), low-cost, low-power mm-wave receivers capable of high-resolution, precise and fast location detection, and high data rate wireless communication. The proposed coexistent multi-mode multi-band system should effectively utilize the newly opened mm-wave spectrum, exploit the unique characteristics of UWB and work under various standards constraints simultaneously.

This dissertation proposes and develops a wideband current mode millimeter r-wave coexistent receiver for multi-standards multi-bands working in K/Ka bands (18-27 GHz/26.5-40 GHz) and V band (40-75 GHz) for short-range high-resolution radar and high data rate wireless communication systems. The proposed receiver is designed using 0.18 μm SiGe BiCMOS technology. The coexistent receiver architecture works to support all standards within the range 22-44 GHz simultaneously resulting in low-cost, miniature, and low-power consumption systems. The developed mm-wave multi-standard multi-band coexistent receiver can be used for numerous cost-effective and multi-functionality applications such as short-range high-data-rate wireless communications, sensing, imaging, tracking, and automotive radar.

1.2 Millimeter-Wave Short Range Radar System

As early as 1886, German physicist Heinrich Hertz experimentally demonstrated that radio waves reflected from solid objects can be used for detection and ranging, thus the name Radar (Radio Detection and Ranging) [21]. Shortly after that, radar systems were developed independently and simultaneously in the naval academies of various

countries. Nowadays, radar systems are being used in various aspects of life for military and commercial purposes such as locating targets at sea, air, and ground.

1.2.1 Radar System Overview

The main purpose of a radar system is to detect accurately the position, range and property for a specific target. To accomplish this task a radar system must consists of 3 sub-systems: a transmitter, an antenna, and a receiver. Fig. 1.1 illustrates the concept.

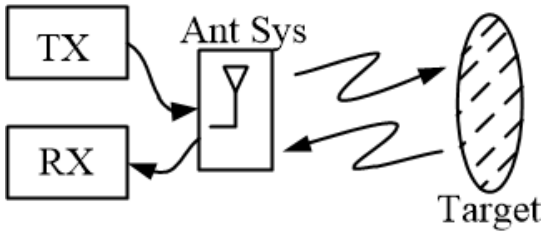

Fig. 1.1 Radar consists of subsystems: a transmitter, an antenna system, and a receiver.

1.2.1.1 Transmitter

Radar systems operate over an extremely wide range of frequencies from low RF, to microwave and millimeter-wave regimes, up to 300 GHz [21] and beyond. Radar systems have various architectures for antennas, transmitters and receivers. For instance, the transmitter architecture of an ultra-wideband short range vehicle sensor is characterized mainly into 3 different categories, which are: 1) pseudorandom noise (PN) coded continuous wave (CW) transmitters; 2) frequency chirped transmitters systems; and 3) gated pulsed transmitters [21].

All of the previously described transmitters systems can deploy a traditional

process technique known as pulse compression to enhance the radar systems performances. Furthermore, some of the reported systems encompass hybrid structure of various techniques at a greater system design complexity [18]. The PN coded continuous wave (CW) transmitter system is essentially a frequency spread spectrum type system resilient to interferences, but it lacks the necessary dynamic range due to high leakage from transmitter to receiver. As for frequency-chirped transmitters, they are difficult to implement for UWB bandwidth in excess of 1 GHz due to the challenge of generating a wideband low phase-noise chirp in CMOS technologies [22].

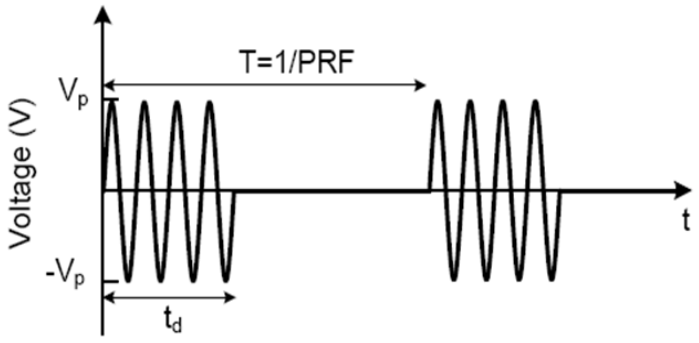

Fig. 1.2 RF pulse signal.

A pulsed transmitter radiates an RF train of pulses or (loosely speaking) impulses with a system-defined carrier frequency, pulse repetition frequency (PRF), and duty cycle. The PRF is the frequency at which the RF pulses or impulses are transmitted, and is inversely proportional to T, where T is the time between transmitted pulses, as shown in Fig. 1.2. The duty cycle of RF pulses is defined as the ratio of t_d/T, where t_d is the transmitted pulse width. In a gated pulse system, the transmitter and receiver operate in a

time duplex fashion (TDD) meaning one of them is on at a time, hence achieving a high dynamic range and making it easier to detect a returned signal at the expense of increased hardware and signal complexity. A pulsed radar signal can be incoherent or coherent. To be coherent, there must be a deterministic phase relationship for the carrier from pulse to pulse. This can be accomplished by switching a CW carrier on and off.

The waveform modulation can be introduced into all types of transmitters systems. Various types of modulation schemes can be used including phase, frequency and amplitude modulation, or a combination of modulation types. For pulsed systems, the modulation can be applied within each pulse over the time period t_d. In the case of adding signal modulation functionality, the transceiver in radar systems can be used in communication systems.

1.2.1.2 Antenna System

Radar antenna systems consist of various types of antennas as follow: 1) single antenna shared between transmitter and receiver; 2) a pair of independent antennas for transmission and reception; 3) an array of antennas.

Fig. 1.3 shows the block diagram of all types of radar antenna systems configurations. A single antenna type of configuration is more suitable for the gated pulse radar type due to the time division duplexing operation of the system. Such configuration setup is established using a circulator and or a T/R switch to select the path of operation. Note that in either operational mode, transmitting or receiving, it is important to maintain high isolation between ports to minimize the leakage spectrum. If

separate transmit and receive antennas are used, the high intrinsic isolation between the antennas minimizes the leakage from the transmitter to the receiver through the antenna system.

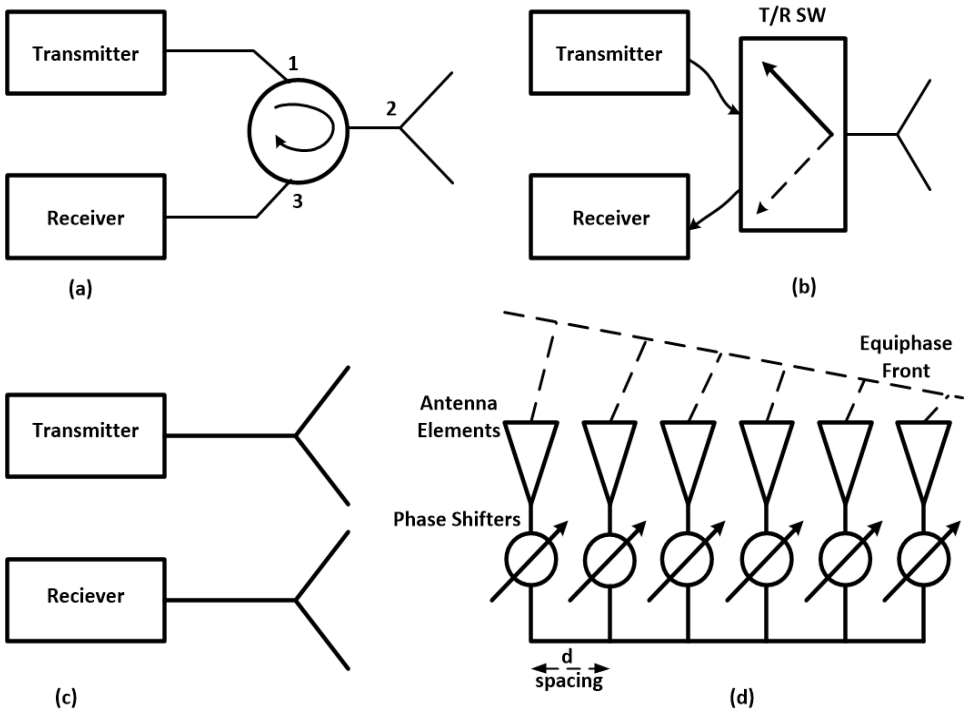

Fig. 1.3 Antenna systems can consist of one antenna using (a) circulator, (b) T/R switch, (c) two separate antennas, and (d) antenna array such as phased array.

Finally, a radar array antenna system with high gain and high directivity is desirable, especially at mm-wave frequencies. The transmitter and receiver can share an antenna array or use separate arrays. Antenna arrays are used extensively in radio astronomy at 23.6-24 GHz and at 44 GHz for synthetic aperture radar (SAR) applications [21].

1.2.1.3 Receiver

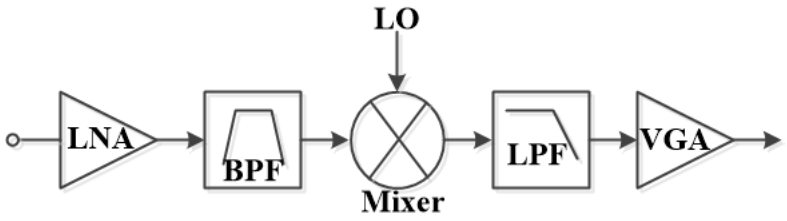

Fig. 1.4 Conventional radar receiver architecture.

The conventional radar receivers amplify, filter, and correlate the received signal to an intermediate frequency (IF) or baseband signal, from which the target can be correctly characterized. Fig. 1.4 shows the basic radar receiver architecture consisting of a low noise amplifier (LNA), a linear phase band pass filter (BPF), mixer, low pass filter and variable gain amplifier (VGA). As the first stage in the receiver, the LNA should exhibit high gain and a low noise figure to maintain a low noise figure for the whole receiver chain. The band pass filter sets the RF band select of the receiver and limits the receiver noise. The mixer correlates the received signal frequency to the IF band or DC by cross correlating the received signal with the local oscillation (LO) signal. In a coherent radar system, the receiver's LO is synchronized with the transmitter LO; coherent systems are common in modern radar systems. Upon down-conversion to the IF band, the signal is filtered and amplified. The IF low pass filter (LPF) sets the final noise bandwidth for the receiver and the VGA sets the receiver dynamic range based on the analog to digital converter (ADC) full scale range. The output of the receiver is then digitized, and digital signal processing is applied.

1.2.2 Short Range Pulse Radar System

The architecture for the short range radars is constrained by the requirements of high range resolution as low as 5 cm, close range detection accuracy for static and moving target, and high dynamic range. Pulsed radar solution is perhaps the most suitable architecture given the time duplex mode of operation, thus high isolation is achieved between transmit and receive side at the expense of complex timing and pulse gated delay circuitry. Hence, a wide dynamic range is attained that helps improve range resolution. Other functionalities include good range accuracy, clutter reduction, and multipath resolution. Pulsed radar is also perhaps one of the simplest architectures to implement, thus potentially making it the most cost effective [18].

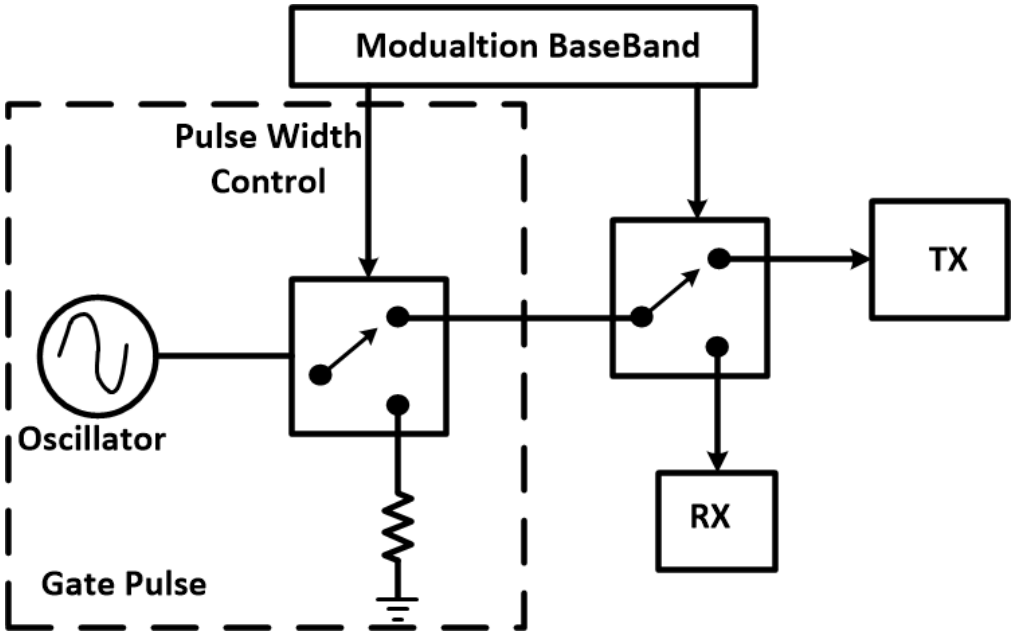

Fig. 1.5 Conventional pulse radar system architecture [18].

The pulsed radar architecture is shown in Fig. 1.5 [18]. A baseband impulse gates the sinusoid from an oscillator to generate a high frequency gated RF pulse signal transmitted by the TX. The resulting RF-pulse signal, as shown in Fig. XX, occupies a bandwidth of approximately $1/t_d$, where t_d is the width of the baseband impulse; the precise bandwidth will depend on the shape of the impulse envelope [21]. The transmission of gated RF pulse triggers a baseband delay circuitry, which waits certain time for a second trigger event to take place. Before the second trigger is activated, the TX/RX select switch is toggled between the TX antenna and the LO ports of the receiver. At the second trigger, the second switch is changed from the TX to RX. The RX then samples its output at this instant and stores it for processing. Thus, the input from the RX antenna is multiplied with a replica of the transmitted pulse. If the two pulses do not overlap in time, the output will be zero, whereas if they are coincident, the output will be a maximum. The delay between the two triggers determines the range gate being scanned at the time. Thus, by changing this delay, objects at varying distances can be detected [18], [22].

1.2.2.1 Radar Interferers and Solutions

The pulsed radar sensor suffers from various interferers that tend to degrade its effective cross sectional radar target detection accuracy as well increases false alarm rate. The most harmful interferers affecting the sensor receivers' detection process and dynamic range are listed as follow: 1) interferers emitted by the radar sensor and radiated as blockers on the frequency spectrum; 2) interferers emitted in-band due to

limited TX/RX isolation; 3) interferers in-band or jammers radiated from similar sensor systems [18].

For the regulatory commissions, the first interferes type are of worrisome due to spurious emissions generated from the radar sensors. Those emissions must be filtered in accordance the regulatory spectral emission limits. For instance, the transmit power and its vertical antenna gain directivity for a short range radar sensor is limited to 35 dB below the -41.3dB$_m$/MHz for a maximum 30 degree elevation with the horizontal plane due to certain sensitive passive test equipment - e.g., astronomy radio equipment at 23.6-24 GHz and 24.05-24.25 GHz ISM band [4].

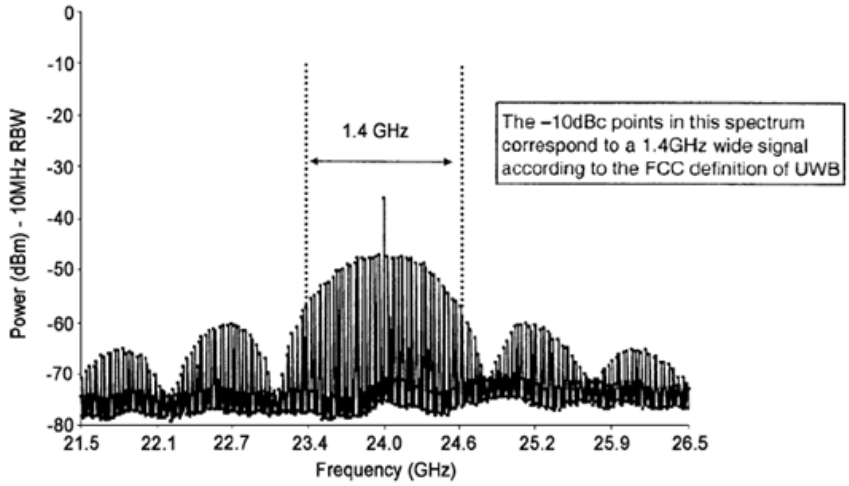

Fig. 1.6 CW LO leakage at 24.15 GHz [18].

In addition, the finite switch isolation in the pulsed radar sensor leaks spurious emissions into the radar receiver's due to CW transmit signal, thus affecting the radar sensor detection accuracy and receiver sensitivity and dynamic range. Fig. 1.6 illustrates

the CW leakage into the receiver's spectrum [18]. The last spurious emissions radiated in-band and/ or jammers are caused by CW transmit signals appearing in the pulsed radar receiver spectrum. This artifact is mainly due to UWB frequency modulated continuous wave (FM-CW) transmitter radar sensor operating at 26 GHz in the vicinity of the pulsed radar receiver. Those interferes can potentially saturates the radar receiver and desensitizes it, thus increasing the receiver down time. However, a careful design can alleviate this problem through a coherent radar approach where carrier frequency is being changed from pulse to pulse and also employ a randomization concept. A further benefit of this randomized pulsing is in meeting the spectral emission limits of the FCC by spreading the radiated energy more evenly across the operating bandwidth [18].

1.2.2.2 Radar Equations

The received power at the input of the radar receiver is calculated using radar equation

$$P_r = \frac{P_t G_{tx} G_{rx} \lambda^2 \sigma}{(4\pi)^3 R_{\max}^4} \tag{1.1}$$

where P_{rx} is the power at the input of the receiver, P_{tx} is the power at the output the transmitter, G_{tx} is the transmit antenna gain, G_{rx} is the receive antenna gain, λ is the wavelength of the carrier frequency, σ is the radar cross section (RCS) of the target, and R is the range to the target [21].

The maximum range of the radar system correlated the with the resolution accuracy is derived from (1.1)

$$R_{\max} = \left(\frac{P_t G_{tx} G_{rx} \lambda^2 \sigma}{(4\pi)^3 P_{r,\min}} \right)^{1/4} \tag{1.2}$$

where R_{max} is the maximum target range and $P_{r,min}$ is the minimum detectable power at the input of the receiver. The expression demonstrates the relationship between the target range, transmitted power, and minimum detectable received power. Increasing the transmitted power and/or decreasing the minimum detectable received power increases the maximum range of the radar.

The minimum signal to noise ratio for a single pulse at the output of the receiver, $SNR_{o,min}$ is calculated as

$$SNR_{o,\min} = \frac{SNR_{in,\min}}{NF} \tag{1.3}$$

where $SNR_{in,min}$ is the minimum signal to noise ratio for a single pulse at the input of the receiver and NF is the noise figure of the receiver. Manipulating equations (1.1) and (1.3), $SNR_{o,min}$ is calculated as

$$SNR_{o,\min} = \frac{EIRP_{pk} G_{rx} \lambda^2 \sigma}{(4\pi)^3 R_{\max}^4 K T_a (NF)(BW)} \tag{1.4}$$

where $EIRP_{pk}$ is defined as the peak effective isotropic radiated power, K is the Boltzmann constant ($1.38e^{-23}$J/K), T_a is the antenna temperature, and BW is the receiver bandwidth.

1.2.3 Radar Pulse Compression

Radar pulse compression is a general term used to describe a waveform shaping process produced by a modified propagating waveform through electrical network properties of a medium. The pulse compression technique consists of a CW source with dispersive delay line through a rectangular function on the transmit side whilst the echoed signal is filtered through a surface acoustic wave (SAW) pass band filter to generate a pulse compression before post processing. The purpose of the pulse compression concept is to combine the high energy of a long pulse width with the high resolution of a short pulse width. Thus, this pulse compression technique improves the signal to noise ratio for less power transmission. The pulse compression concept is a frequency modulated pulse method that consists of two classes; 1) frequency modulation or FM modulation; 2) phase modulation or PM modulation.

1.2.3.1 Linear Frequency Modulation Pulse Compression

Linear frequency modulation (LMF) pulse compression radar or (Chirping) is the practical implementation of a matched-filter system. The transmit pulse signal can be described either by the frequency response $H(\omega)$ or as an impulse response $h(t)$ of the modulated filter. The received echo is fed into a matched filter whose frequency response is the complex conjugate $H^*(\omega)$ of the modulating filter. The output of the matched filter is the compressed pulse which is just the inverse Fourier transform of the product of the signal spectrum. A filter is also matched if the signal is the complex

conjugate of the time inverse of the filter's impulse-response. This is often achieved by applying the time inverse of the received signal to the pulse-compression filter. The output of this matched filter is given by the convolution of the signal h(t) with the conjugate impulse response h*(-t) of the matched filter. In essence, the matched filter results in a correlation of the received signal with a delayed version of the transmitted signal as shown in Fig 1.8 below. For this chirp pulse compression example, the output of the matched filter is a sinc function with problematic time side-lobes. An amplitude weighting function is used at the output of the match filter to suppress the time side-lobes to less than 30 dBs.

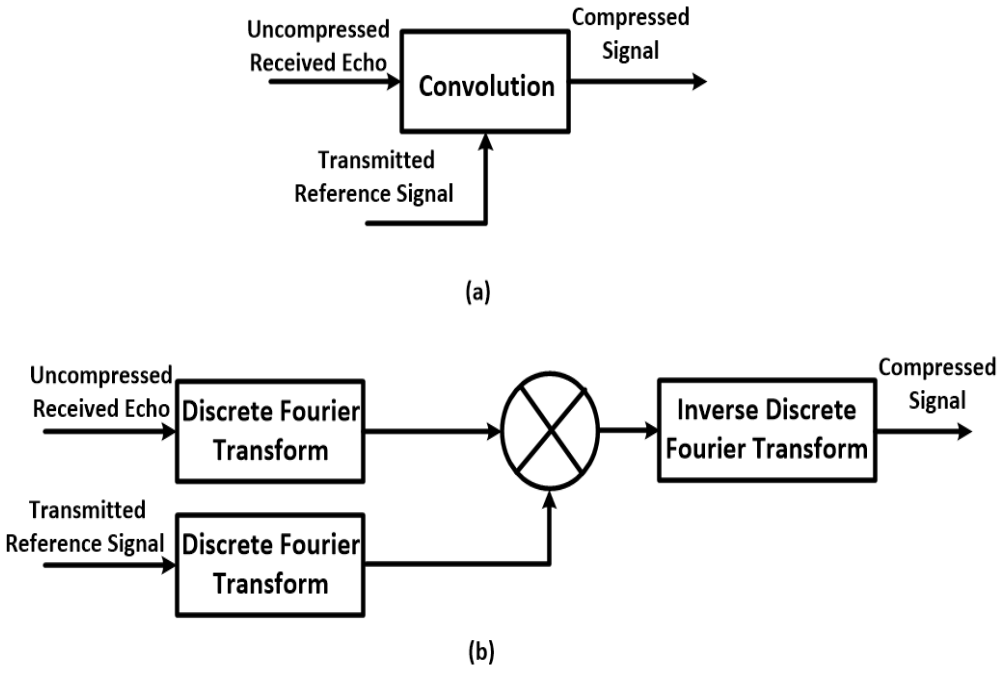

Fig. 1.7 Linear frequency modulation pulse compression implementation methods (a) time domain, (b) frequency domain.

1.2.3.2 Phase-Coded Pulse Compression

Phase-coded pulse compression based on the binary phase shift keying (BPSK) modulation technique sub-divides a long transmitted pulse into equally timed short pulses with a particular phase. The phase of each sub pulse is selected in accordance with the phase code modulation sequence (BPSK) which is either positive +1 or negative -1. The phase of the transmitted pulse alternates between 0 and π in accordance with the

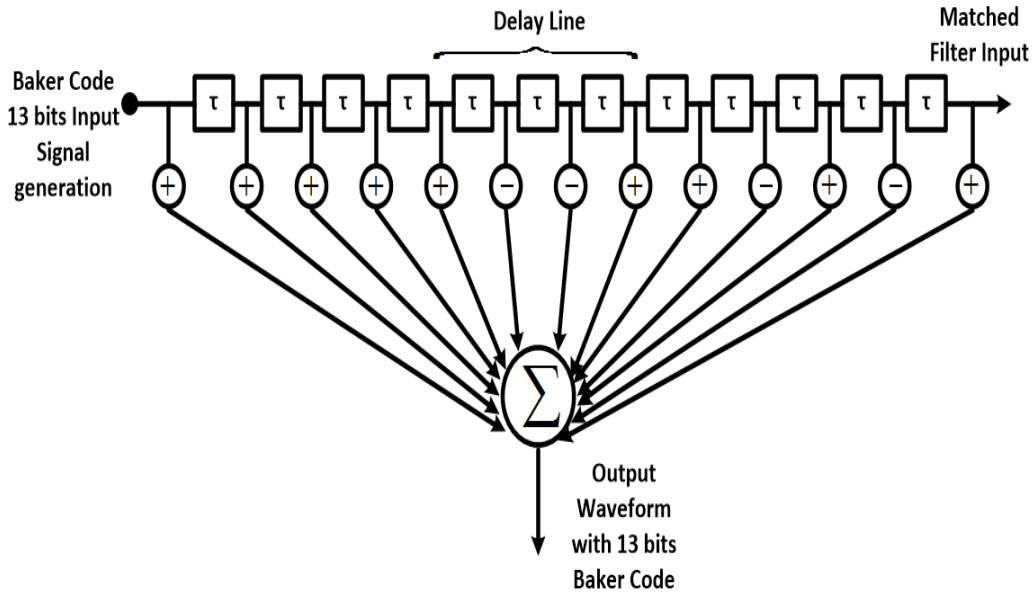

Fig. 1.8 Phase-coded pulse compression using 13 bits Baker code.

transmitted pulse coded sequence of elements as illustrated in Fig. 1.8. Since the transmitted frequency is not a multiple of the reciprocal sub-pulse width, the coded signal is discontinuous at the phase-reversal point. In fact, the phase 0, π random selection is critical. To overcome the side-lobes limitations, optimum binary codes known as Baker codes have been developed to suppress this artifact.

1.2.4 Signal Modulation

Signal modulation schemes can be implemented in pulsed radar systems to support the data communication. On-Off-Key modulation (OOK), Pulse Position Modulation (PPM), Pulse Amplitude Modulation (PAM) and Bi-phase modulation (BPM) are the most widely used for this objective; the transmitted information can be coded by changing its pulse position, shape or polarity [23].

1.2.4.1 On-Off Key Modulation (OOK)

OOK denotes the simplest form of amplitude-shift keying (ASK) modulation that represents digital data as the presence or absence of a carrier wave. In its simplest form, the presence of a carrier for a specific duration represents a binary "1", while its absence for the same duration represents a binary "0". The main disadvantage of OOK modulation system is that it is more prone to noise, interference, and multipath fading. Thus, it will be more difficult for the receiver/demodulator to distinguish between fading/noise and data pulse transmission.

1.2.4.2 Pulse Position Modulation (PPM)

PPM is a form of signal modulation in which M message bits are encoded by transmitting a single pulse in one of 2^M possible required time-shifts. Such transmission is periodic every T seconds, and the bit rate is M/T bit per second. The advantage of PPM is that the pulse position will appear to be random on the time domain, which

translates into a smoothly spread spectrum on the frequency domain.

1.2.4.3 Pulse Amplitude Modulation (PAM)

PAM is a form of signal modulation where the message information is encoded in the amplitude of a series of signal pulses. It is an analog pulse modulation scheme in which the amplitudes of a train of carrier pulses are varied according to the sample value of the message signal. PAM supports multi-level amplitude modulation which is suitable for high data rates. However, the pulses will be very close to each other and more susceptible to noise and interference while larger pulses will require more power for amplification.

1.2.4.4 Bi-Phase Modulation (BPM)

BPM is RF transmitted pulse signal that alternates between 0 and π to represent the bit sequence of elements "1" or "0". BPM is less sensitive to noise compared to AM modulation schemes; and the requirement for accurate timing control is also not as stringent as PPM. Furthermore, BPM supports wide range of digital data transmission from WiFi to satellite television.

1.3 Transceivers Architecture for Short Range Radar and Radio Communications Systems

The system architecture reported in [24] holds dual mode functionalities for short range radar and communications systems. As for the communication system mode of operation, modulated RF train pulses are transmitted using any of the modulation

schemes from section 1.2.4. The receiver generates a series of RF pulses with exactly the same shape and intervals, called template signal, to correlate with received pulses in order to detect the transmitted information [23]. Time delay is expected between the two users end, and loop synchronization is in place to align the template train pulse and the received signal.

In radar system mode configuration, the transmitter sends RF gated pulses periodically with lower pulse repetition frequency (PRF). The receiver operates in similar fashion as mentioned in the communication mode mechanism. That is, the received signal is correlated to the very same transmitted signal acting as template signal on the receiver end with known time delay measured as multiple of the time gated pulse which is equal to the pulse width.

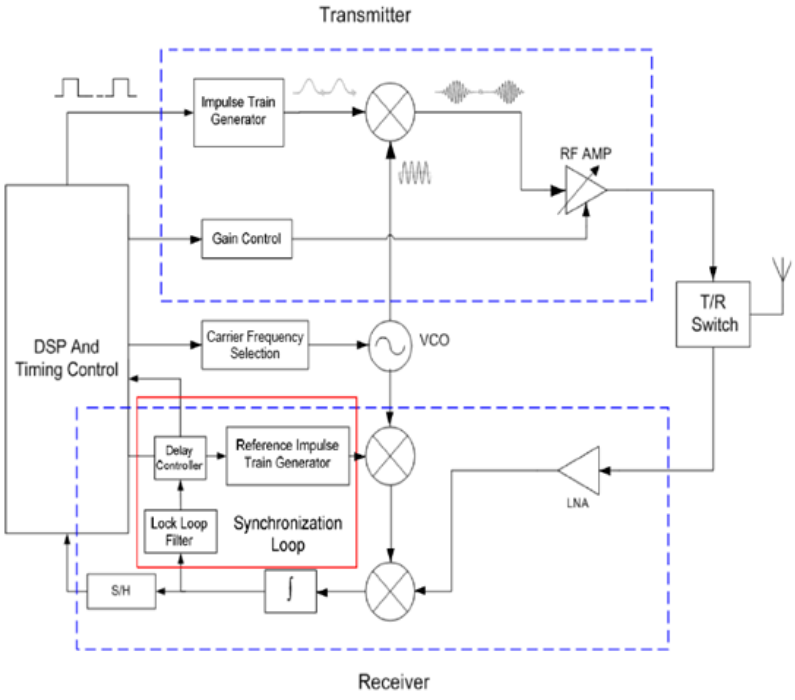

Fig. 1.9 System architecture for both radar and communication systems [24].

1.4 Dissertation Organization

This dissertation presents several new circuit architectures and techniques to improve performance of some key CMOS and SiGe/BiCMOS RFIC circuits operating at RF, microwave and millimeter-wave frequencies, and the development of a new millimeter-wave coexistent current mode direct conversion receiver for multi-standards multi-bands operating at K/Ka and V bands and not limited to short range radar and communication systems.

Chapter II discusses system architecture level and design specifications for short range radar and wireless communication systems at millimeter-wave frequency. Chapter III presents a new low power consumption active balun-LNA for millimeter-wave application using SiGe BiCMOS technology. Analysis design procedure, parameter trade-off, simulation and measurement results, and layout issues are discussed. In Chapter IV, a novel 2 stages low power balun-LNA with phase and gain mismatches cancellation technique independent of frequency is presented. The cancellation technique is frequency independent and do not rely on passive components for neutralization and compensation. The active balun-LNA is well-balanced over a wide frequency range from DC up to millimeter-wave regimes and detailed analysis is provided. In Chapter V, a new coexistent millimeter-wave system and circuits level architecture using SiGe BiCMOS current mode direct conversion receiver is presented. An auxiliary path for high power jamming interferers for military unmanned aerial vehicular (UAV) radar system at 35-37 GHz is considered as well. The detailed design of some building blocks including fully balanced quadrature passive mixer and phase

shifter, trans-impedance amplifier (TIA), and out of band interferers rejection filter known as anti-aliasing filter is presented. Finally, chapter VI summarizes the contribution of this dissertation.

CHAPTER II

SICS COEXISTENT RECEIVER ARCHITECTURE AND SYSTEM SPECIFICATIONS

2.1 MMW Receivers History

Most microwave and mm-wave receivers' designs reported in literature are dedicated to serve single or dual bands applications. Some of these applications involve short range high resolution vehicular radar at 22-29 GHz to wireless high data rate metropolitan area network from 10.6-66 GHz. However, various types of receivers' architectures are reported to serve these applications based on homodyne approach, heterodyne designs, and phased array types as well. We will provide a small window into each receiver's design approach highlighting its proponents and drawbacks.

2.1.1 Heterodyne Receiver

MM-wave heterodyne type receiver architecture design consists of multi-mixing stages to bring about the spectrum to an intermediate frequency (IF) followed through with some filtering made ready after A/D converter for digital processing. However, polyphase filters are needed to suppress LO images after each mixing stage. The design of RF polyphase filter is not trivial and not to mention the need for gain compensation stage to maintain SNR level at the expense of power and die area. Until recently, a new concept of mm-wave heterodyne receiver's considered [8], [9] shown in Fig. 2.10 below. The architecture consists of RF mixing followed by direct mixing stage to alleviate the

image problem and resolve some complex issues related to high in-band phase noise associated with LO frequency planning and layout floor designs.

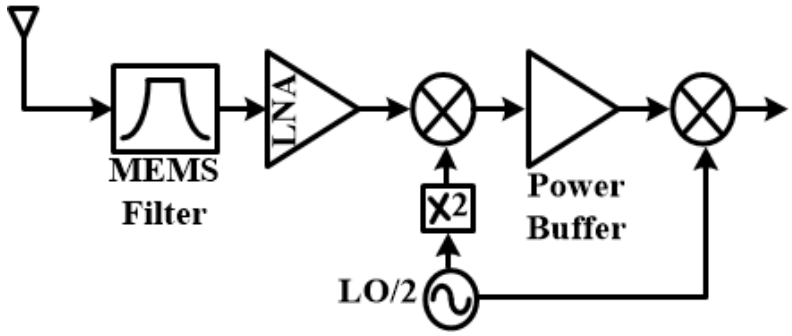

Fig. 2.10 Heterodyne receiver architecture.

2.1.2 Phased Array Receiver Principles and Architecture

A phased array receiver consists of several signal paths, each connected to a separate antenna. The radiated signal arrives at spatially-separated antenna elements at different times. An ideal phased-array compensates the time delay difference between the elements and combines the signals coherently to enhance the reception from the desired direction(s) while rejecting emissions from other directions [25]. Fig. 2.11 shows a one dimensional n-elements linear array hit by a plane wave. The arrival incident signal to each antenna element is progressively time delayed by τ. This time delay difference between two adjacent antenna elements is related to their separation distance (*d)* and their angle of incidence (θ) with respect to the normal. The governing relationship is given by

$$c\tau = d\sin\theta \tag{2.1}$$

where c is the speed of light. The incident signal at the kth antenna element can be expressed as

$$S_k(t) = A(t - k\tau)\cos\left(\omega_c t - k\omega_c \tau + \varphi(t - k\tau)\right) \tag{2.2}$$

where the amplitude of the kth element is defined by $A(t - k\tau)$; the carrier frequency is defined by ω_c; and the phase delay is defined by $\varphi(t - k\tau)$. The equal spacing of the

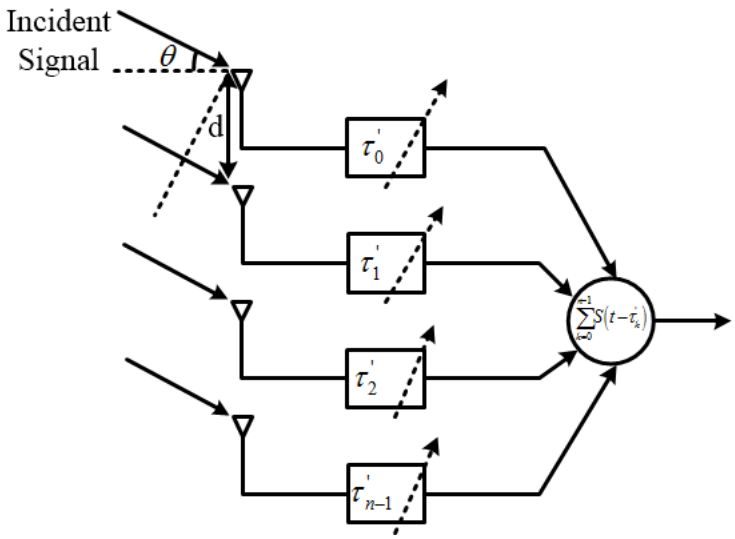

Fig. 2.11 General concept of phased array system architecture.

antenna elements is reflected in (2.2) as a progressive phase difference $\omega_c\tau$ and a progressive time delay τ in A(t) and φ(t). Adjustable time delay elements (τ'_n) can compensate the signal delay and phase difference simultaneously [25]. The combined signal summation $S_s(t)$ can be expressed as

$$S_s(t) = \sum_{k=0}^{n-1} S\left(t - \tau_k^{'}\right)$$
$$= \sum_{n=0}^{n-1} A\left(t - k\tau - \tau_k^{'}\right) \cdot \cos\left[\omega_c t - \omega_c \tau_k^{'} - k\omega_c \tau + \varphi\left(t - k\tau - \tau_k^{'}\right)\right] \quad (2.3)$$

For $\tau_k^{'} = -k\tau$ the total output signal power is given by:

$$S_s(t) = nA(t)\cos\left(\omega_c t + \varphi(t)\right) \quad (2.4)$$

For a narrowband phased array design the time delay between antenna elements is translated into an adjustable phase delay elements in the RF path. Note that in a narrowband signal the relative slow change in amplitude A(t) and phase φ (t) compared to the carrier frequency ω_c necessitate only the need to compensate for the progressive phase difference $\omega_c\tau$. The time delay element can be replaced by a phase shifter which provides phase-shift Φ_k to the kth receiver signal path. To add the power signal coherently, Φ_k should be given by:

$$\Phi_k = k\omega_c \tau \quad (2.5)$$

The phase compensation for a narrow band signal can be made at various locations in the receiver chain, i.e, RF path, LO, Baseband, or digital domain. For the broadband type of phased array architecture, the only suitable structure is limited to passive RF phase shifting architecture. In this approach, antennas elements are directly

followed by passive phase shifters or time delays elements fed into a combiner to coherently add signals into the LNA input. A single path receiver is suitable for this approach as shown in Fig. 2.12. The main drawbacks of this design are the lack of amplitude control as well as the limited receiver dynamic range and sensitivity due to passive phase shifter and combiner losses [25], [26]. As a single-path receiver, the phased array receiver can be realized using various known down conversion schemes such as

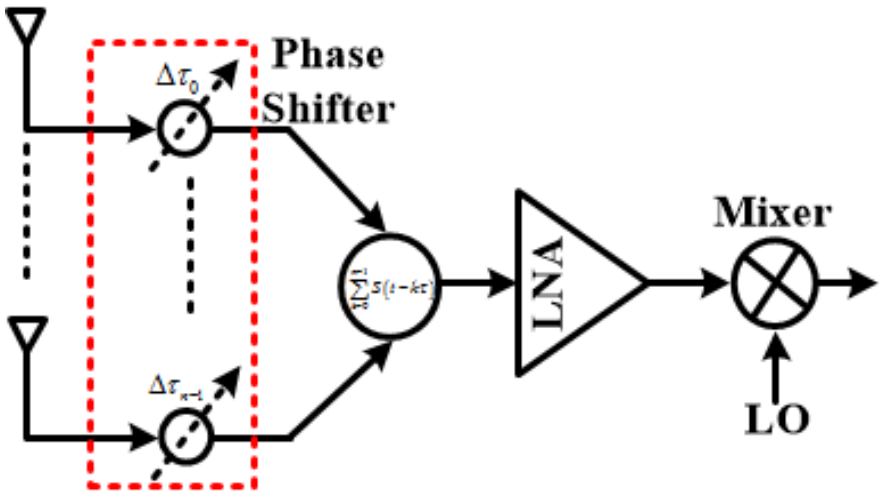

Fig. 2.12 Passive RF phased array architecture.

heterodyne, direct conversion, wide-band IF, and low-IF. The design trade-offs are dictated according to each signal-path receiver type. One important factor in a phased array system is its ability to attenuate the incident interference power from other directions. Thus, the spatial filtering is applied. Furthermore, a spatial processing technique can be considered by changing the nulls location and the side lobes levels by changing the weight signal power factor of each element in the phased array system.

Hence, the spatial filtering and processing techniques help improve the signal to noise and interferers' ratio for the phased array receiver chain.

2.1.3 Homodyne Receiver

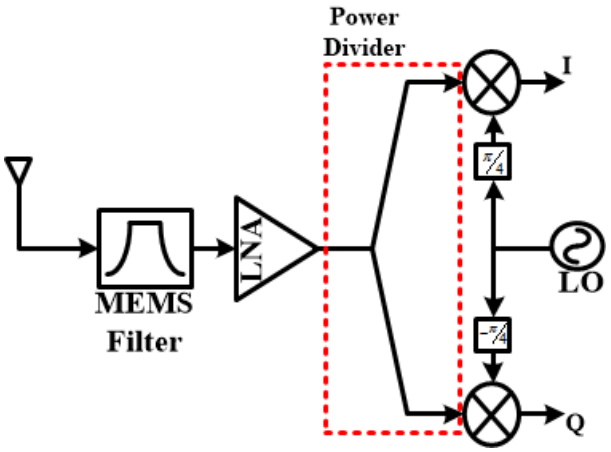

Fig. 2.13 Homodyne receiver architecture at mm-wave.

An alternative approach to the previously mentioned receiver architectures is the homodyne receiver structure also known as direct down conversion receiver. At mm-wave, all interconnects have to be simulated in a 3D EM simulator to see the effects of inductance loading and coupling parastics to substrate. In this spirit, the mm-wave homodyne receivers reported in [16], [18], [22], consist of a LNA followed by a power divider fed into in-phase/quadrature single balanced mixers. The cross correlated outputs, mixers outputs, is fed into a wideband variable gain amplifier (VGA). The baseband signal is integrated and dumped before being digitally processed. Fig. 2.13 shows the system receiver architecture. For instance, this approach was dedicated to the short range vehicular radar system from 22-29 GHz application. The main disadvantage

of this single balanced mixer design scheme is subject to LO power feed-through causes receiver desensitization that can lead to noise figure increase. Also, the integration and dump block on the baseband side is very vague and doesn't present a real solution.

2.2 SICS Coexistent Receiver Definition

In May 1995, J. Mitola proposed "The Software Radio Architecture", [27], that is transmit/receive *multiple channels simultaneously* completely eliminating the Analog Front-End (AFE). However, such a system probably is an over reach at mm-wave frequencies and is bounded by advancement in technology not foreseen in the near future. Razavi's proposed Cognitive Radio design approach [28]. The main idea stems from intelligently sensing the frequency spectrum and makes allocation of freed up channels for reuse. The system design entails many challenges from the AFE design and technology aspects and may not be applicable any time soon. A more practical approach that copes with industry needs based on multi stacked systems integrations on a single die also known as System on Chip (SOC) [29]-[30]. However, the rapid increase in systems integration becomes impractical not to mention the die size and its power consumption and I/O complexity. Our portrayal of coexistent receiver architecture is based on a configurable, agile platform supporting any predefined single channel bandwidth with any modulation scheme located anywhere on a defined broad spectrum.

2.3 Coexistent RX for Radar and Radio Terminals

Our System presents the challenge of designing an mm-Wave coexistent radio and radar receiver architecture (CRRA) supporting multi-standards multi-bands applications. The current mode coexistent receiver architecture is based on configurable agile platform supporting any predefined single channel bandwidth with any modulation. If multiple bands requested simultaneously then parallel structure is needed with possible blaun-LNA block being shared. The system will be operating from 22- 44 GHz sustaining short range vehicle radar receiver from 22-29 GHz, Industrial-Scientific-Medical (ISM) band from 24.05-24.25 GHz, military radar receiver for reconnaissance missions using unmanned aerial vehicular at 35-37 GHz, ultra-wideband (UWB) wireless application from 10-66 GHz known as Metropolitan Access Area Network (WiMAN) for 802.16a standard, and 44 GHz for satellite communication. This is just to list few applications, it should be able to support all channels receivers operating within the frequency band; given we have a wideband tunable local oscillator (LO) with a good phase noise and a wideband phase shifter with minimum insertion loss as well as low amplitude and phase mismatches. For a system to be considered CRRA, it has to meet certain criteria:

- No RF pre-filter right after antenna e.g. (SAW Filter or BAW Filter), providing the necessary flexibility.
- Having a reconfigurable ADC combined with a VGA.
- Having a reconfigurable current mode RF-Front End.
- Limit power consumption for possible wireless support.

- Having out of band harmonics and interferers' rejection.

In general, all RF-Front End circuits including RF pre-filter and base-band (BB) blocks are conditioning signals for the analog to digital conversion (ADC) to provide accurate digital representations for the demodulated signals. That being said, the receiver has to have a robust linearity to IN/OUT of band interferers, cross modulation, and amplitude modulation (AM) detection. Some aspects of these interferers are subject to the type of receiver architecture. For example, a second order intermodulation product (IP2) is very important for direct conversion approach although a differential structure is supported. Therefore, designing a receiver involves paramount tradeoffs between sensitivity and linearity.

2.4 Signal Conditioning Functions in Low Power Wideband Receiver

Mitola's main idea concept presents the ADC as the only interface between the analog domain and the digital world. With simple calculations, it is immediately concluded that Mitola's concept is impossible to be implemented at mm-wave frequencies considering the ADC sampling frequency and its power consumption requirements. In general, the ADC is a low pass filter shaping the signal in its simplest form. Note that the ADC dynamic range has to be larger than incoming signal dynamic range including interferers and blockers. It is important for the incoming signal to be down converted, filtered, and amplified prior to the ADC. Fig. 2.14 shows the signal conditioning blocks for the wideband receiver architecture where LO frequency planning

and layout floor plays a major role in the structure design. The assumption here is the LO is provided externally supporting wideband differential signal as stated in the section 2.3.

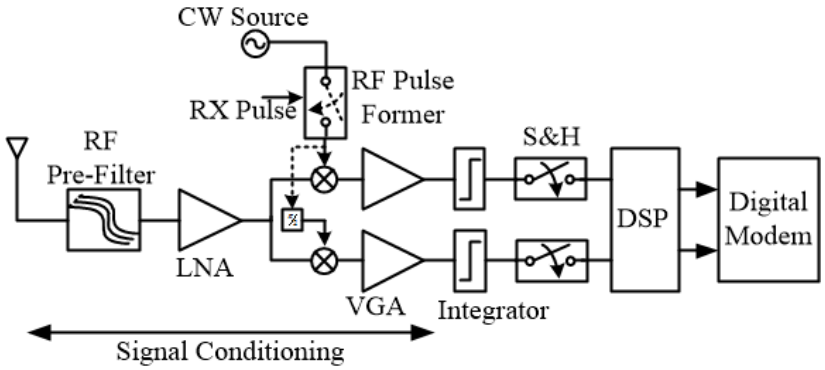

Fig. 2.14 SRR wideband receiver architecture with front-end signal conditioning blocks.

The architecture scheme shows a homodyne type approach also known as direct conversion with zero IF which is easier to achieve wideband operation with the least signal blocks path, hence reducing power and losses. The receiver first block consists of RF preselect filter using MEMS technologies. A low noise amplifier (LNA) is followed where the signal is amplified with minimum added noise. After the LNA block, the signal is down converted to baseband using in-phase/quadrature mixers making the receiver more robust to frequency image spectrum. Ideally, the in-phase/quadrature operation is image free, however in practice the image rejection ratio (IRR) is limited by the amplitude and phase mismatches between the I and Q paths [31], [32].

The simple frequency planning and low IRR requirements makes the direct conversion zero IF receiver an attractive choice at mm-wave. For narrow band receivers, the rejection of interferers and blockers are established through cascaded filtering

functions from the RF pre-filter, LNA output LC tank, and baseband low pass filter. However, wideband receivers experience a little or no filtering up till the VGA block where a first order low pass in its natural form is expected. For that reason the FCC limits the transmit power on the spectrum in some cases so the background noise spectrum and interferers are low for some sensitive passive radar applications. Chapter I addresses the interferers and blockers mitigations mainly after the demodulation section in the receiver chain. However, the filter needs to be applied as early as possible in the receiver chain so the receiver down time is very small.

2.5 Low Power Coexistent Receiver Architecture Fundamentals

Starting from the receiver back end where digital Modem is followed by the DSP block for demodulation and constellation recovery. The analog to digital interface is based on the availability of low power reconfigurable ADC with finite resolution and more reasonable sampling frequency to preserve the low power wideband receiver concept for radar and radio terminals. In some operational domains, the coexistent receiver is wired and in other operational mode has limited power access for wireless and surveillance applications. The ADC is preceded with the AFE circuits for filtering and amplification.

This means that the selected channel, and adjacent channels, is sampled with minimal filtering and amplification consistent with low power ADCs. To preserve the wideband operational mode, the AFE circuits should remain as simple as possible with the least parasitic losses. Most of the filtering operation is pushed further down the

receiver chain into the digital and demodulation section. The VGA is lumped into the ADC block, and a continuous feed-forward poly-phase high pass anti-aliasing filter is selected to deal with interferers and harmonics rejections. A current mode RF front-end is considered to maintain high in-band linearity and low noise figure followed by a trans-impedance amplifier providing I-V conversion.

Similar to homodyne wideband RX, it is clear that from the upstream ADC it is most beneficial that the channel of interest is down-converted to zero-IF. This is because of the low-pass nature of all analog circuits and the most efficient in power consumption. Although in principles these circuits can be transformed into any filters or amplifications types, the power consumption, circuits' complexity, and losses make it undesirable approach.

2.5.1 Low Power ADC at Baseband

The power budget for the ADC is limited to less than 32 mW designed in advanced CMOS technologies. According to FCC regulations; a minimum of 500 MHz bandwidth is needed for UWB systems including mm-wave based UWB systems and their transmitters and receivers. A simple literature review shows that a 10 bits pipeline ADC with up to 1 GS/s is possible [33]. For example, this ADC can be used for short range vehicular radar application. Based on 802.16-SC standard for single wireless carrier for WiMAN between 10-66 GHz, a local multipoint-distribution system (LMDS) at 31 GHz with 500 MHz bandwidth including 19-20 channels bandwidth up to 25/28 MHz with QPSK modulations are targeted with readily available 10 bits ADCs' using

pipeline architecture with 100 MS/s and consumes less than 5 mW. More advancement in CMOS technologies can reduce the power/conversion-step for the ADCs' and improve the bits resolutions thus increases the ADC signal bandwidth.

2.5.2 Merging Variable Gain Amplifier (VGA) into ADC

According to the FCC regulations, a UWB receiver requires a minimum of 500 MHz channel bandwidth. For a wideband receiver, it is more reasonable to shift the gain control of the high dynamic range signal from the programmable gain amplifier (PGA) or VGA or the combination of both to the RF front-end. Shifting the programmable gain functions completely to the DSP forces the ADC power consumption to become excessively high. In reality, it is a tradeoff between ADC power consumption, and the RF front-end. The incoming signal dynamic range needs to be lower than the ADC dynamic range so that all analog values are mapped, digitized, and normalized properly. Due to advancement in CMOS digital technologies, we assume greater role for the AGC. Let us study the effect of the AGC behavior on the short range vehicular radar (SRR) sensor.

According to SRR transmit standard [1]-[2]; the specifications for transmit emissions EIRP mean power density is regulated to -41.3 dBm/MHz with an additional 35 dB attenuation for passive radar applications, 23.6-24 GHz, with antenna sidelobes elevation above 30º with the horizontal plane. The peak transmit EIRP power density is limited to -17 dBm/MHz for 50 MHz bandwidth. From these specifications, we can determine the receive strength signal at the receiver antenna side to be between -77 dBm

to -15 dBm. This is a 62 dB dynamic range. We assume that the receiver architecture is based on pulsed radar design approach, thus the benefit of higher receiver dynamic range compared to its counterpart's structures. Further, the TX/RX mode of operation is based on time duplex, hence reducing the TX/RX leakage. Given the design requirements for the *prf, probability of target detection and probability of false alarm a minimum* $(SNR_0)_{min}$ *is required.* The minimum SNR is 1.1 dB and 10 pulses are integrated to reach the required SNR target of 11 dB based on RX NF of 8 dB.

Starting with the ADC, we used a 10 bits pipeline ADC. Such ADC is readily available with Full Scale (FS) output of 0 dBm (1.2 V peak to peak) and a sampling frequency of 1 GS/s and supporting bandwidth up to the Nyquist rate. The ADC only consumes 32 mW from a 1.2V power supply using 65 nm CMOS process. Then, the ADC quantization noise is at -60 dBm; so all signal conditioning circuits are required to amplify input signals above the ADC noise floor plus the modulation scheme SNR. All RF front-end circuits, anti-aliasing and anti-blocking filter are required to amplify input signal by 28 dB. Also, we have to consider the SNR degradation mainly due thermal noise, quantization noise, and clock jitter. To limit our SNR degradation to 0.1 dB due to noise quantization, we need to add 16 dB as a safety margin. For large input, gain must be lowered from 44 to 9 dB leaving 6 dB margins below full scale output for envelope variations and AGC gain setting error. Fig. 2.15 shows the frequency planning for the programmable variable gain amplifier. It is really important to emphasize the sharing between the VGA and the DSP part instead of using higher resolution ADC, thus

increasing the power consumption. Note that an increase in signal bandwidth requirement may set higher gain requirements on the AFE and VGA.

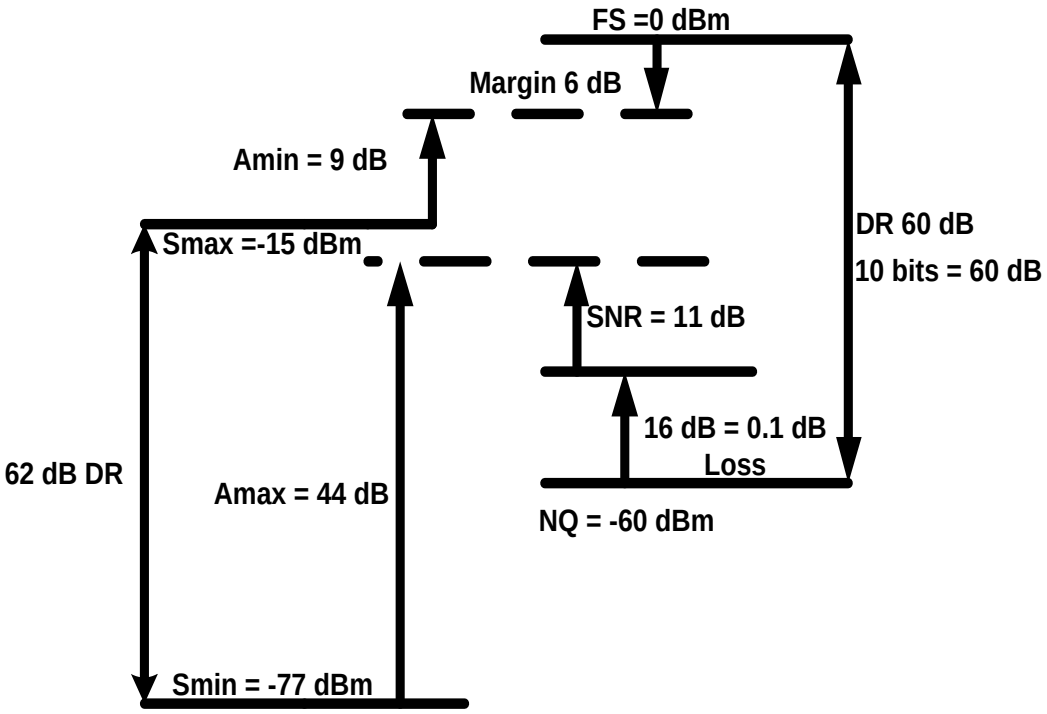

Fig. 2.15 Programmable variable gain amplifier specification for SRR application.

Similarly, the 802.16-SC for the WiMAN standard with 25/28 MHz bandwidth operates from -85 dBm to -15 dBm. At high data rate transfer, the minimum receiver sensitivity floor is set at -75 dBm. A larger dynamic range is expected due to smaller bandwidth. To digitize 28 MHz bandwidth, a 10 bits pipeline ADC with 100 MS/s is expected within the power budget of 5mW [34] from a 1V power supply using 90 nm CMOS process. Allowing for the 15 dB SNR for proper signal detection at an acceptable bit error rates; the RF/analog front-end variable gain is expected to vary from

41 dB to 9 dB. A lower ADC dynamic range due to wider system bandwidth requirements forces the RF front-end to carry higher burden in terms of power consumption.

2.5.3 Anti-Aliasing and Anti-Blockers Filters

Anti-aliasing and anti-blockers filters are part of the RF pre-filter, LNA output matching load, and baseband filters. However, in a wideband mm-wave receiver design approach the earliest filtering takes place at baseband. RF pre-filters are not so effective at mm-wave frequencies trading insertion loss for out of band attenuation and lack the necessary flexibility to support multi-standards. A recent attempt is made to improve insertion loss through MEMS filters [35]; however such filters are technology specific and expensive to use and not easily integrated on chip.

Removing the RF pre-filter and having wideband matching LNA load pushes the filtering to baseband and DSP. For the current mode coexistent mm-wave receiver, the baseband partially present some attenuation to the out of band blockers and the rest is handled by the DSP to mitigate the linearity requirements. In reality, the FCC regulations limit the emissions EIRP at mm-wave frequencies particularly where overlapping standards exists.

In our attempt to present the dilemma of linearity requirements, we will show the anti-aliasing and anti-blockers filter mask for the SRR and the LMDS standards.

2.5.3.1 SRR Filter Specification

The increase in ADC dynamic range helps reduce the anti-blockers filtering requirements and off load most of the channel selection to DSP at the expense of ADC power consumption increase. According to the FCC regulations, a UWB receiver has to maintain a minimum of 500 MHz channel bandwidth with emissions limitations at certain sensitive frequency bands. EIRP emissions at 23.6-24 GHz and at 29-31 GHz are limited to -41.3 dBm/MHz and furthermore, antenna sidelobes above 30 degrees with the horizontal plane are attenuated an additional 35 dB. One proposed solution to the restriction on elevation sidelobes is to center the spectrum of the transmitted signal above 25 GHz so that the first null of the sinc(x) spectrum falls at the restricted band, thus reducing some of the demands upon antenna design [18]. None the less, anti-aliasing and anti-blockers filters are designed based on analog filters.

In the presence of a blocker, the sensitivity requirement is reduced by 3 dB. This 3 dB margin, compared to maximum sensitivity requirement, should be used properly to relax the linearity demands and nonidealities on key circuit blocks.

2.5.3.1.1 SRR Anti-Aliasing Requirements

Removing the RF pre-filter from the receiver chain exposes the AFE to all sorts' of spectrum non-idealities and makes the anti-aliasing filter specifications very difficult to meet. Note the main concern for the SRR is the spurious emissions generated from the radar sensor and radiated as radio frequency interference. Chapter 1 shows various

interferers types that affect the SRR spectrum and its mitigated DSP solutions. However our approach is to provide a join solution between the analog filter and the DSP.

The assumption here is for 1 dB SNR degradation from aliasing blocker due to RF pre-filter removal. This means that the total generated distortion from aliasing blocker is limited to 6 dB below the SNDR of the receiver. Furthermore, the aliasing blocker bandwidth is limited to the desired channel bandwidth. The anti-aliasing blocker attenuation factor referred to the antenna for a given sampling ADC frequency, $f_{s,ADC}$, is given by:

$$\alpha_{AAF} = P_{bk} - 10\log\left(BW_{bk}/BW\right) - \left(P_{sig} - SNR - 6\right) \tag{2.6}$$

where, P_{bk} and BW_{bk}, are the aliasing blocker power and its bandwidth, respectively, and P_{sig} is the received signal power referred to the antenna. For a higher blocker bandwidth, the attenuation factor is a bit more relaxed. Considering the SRR example, the P_{sig} is set to -74 dBm after 3 dB budget for filter interferers profiling, SNR equal to 11 dB, and assuming the blocker bandwidth equal to the desirable channel of 500 MHz. The attenuation factor needed at 1 GHz offset from selected frequency channel based on a given sampling ADC frequency, $f_{s,\,ADC}$ equal to 1GS/s, is 74 dB. However, the blocker can be as close as 25 MHz away from the desirable channel. In that case, no analog filter can provide any rejection or attenuation and we are completely relying on DSP approach. For the worst case scenario, considering the ISM band at 24.05-24.25 GHz for

short range pulsed communication system, the anti-aliasing attenuation factor needed is 108 dB. Fig. 2.16 shows the anti-aliasing filter profile based on interferers power levels.

2.5.3.1.2 SRR Anti-Blocker Specifications

To prevent in-channel distortion due to the nonlinearities generated from subsequent blocks particularly the ADC, an anti-blocking filter is needed to enhance the attenuation factor. An IIP3 test measures the ADC true linearity based on injecting two tones signals with equal amplitudes and spaced a Δf frequency. ADC nonlinearity is specified by defining the effective number of bits (ENOB), looking into the spurious free dynamic range (SFDR), and its IIP3 is calculated from:

$$IIP_{3,ADC}(dBm) = P_{in}(dBm) - \frac{IMD_3(dBc)}{2} \tag{2.7}$$

where P_{in} is the input signal power and IMD_3 is the third-order intermodulation distortion. In general, a 7 dB below full scale input ADC seems a common practice [36] (-7 dBFS). IMD_3 is related to the ENOB of the ADC, thus (2.7) can be rewritten as:

$$IIP_{3,ADC} = (FS - 7) + \frac{(6b_{ENOB} + 1.7 - 20\log_{10}(7))}{2} \tag{2.8}$$

Assuming that the ADC has 8.6 bits linear (ENOB) and dominated by the third order nonlinearity, then

$$IIP_{3,ADC} = 11.4 \text{ dBm} \tag{2.9}$$

Note that it is important for the incoming signal plus distortion to have a dynamic range less than the ADC dynamic range. Therefore, the incident signal will not experience any clipping due to ADC limitation. The ADC is at the backend of the receiver chain, and to calculate the anti-blocking filter requirements; the receiver's gain of 44 dB should be accounted for. If only 0.1 dB degradation budget is allocated for the intermodulation test, then the IMD_3 specified at the ADC input should be:

$$IMD_3 \le P_{sig} - SNR - 16dB + A \tag{2.10}$$

where A is the RX gain under the interferers test setup conditions with 1 dB interferers degradation budget. For the SRR standard, the IM_3 intermodulation power test translates into (-61) dBm at the ADC input. The two tones blockers power at the ADC input should be

$$P_{b,ADC} = \frac{IM_3}{3} + \frac{2}{3} IIP_3 \tag{2.11}$$

where $P_{b,ADC}$ is the tolerable 2 tones power blockers at the ADC input. From (2.11) we can determine that the maximum $P_{b,ADC}$ = -20 dBm. The attenuation factor for anti-blocking 2 tones blockers at the ADC input is specified as

$$\alpha_{ABF,2tones} = P_b - \left(P_{b,ADC} - A\right) \tag{2.12}$$

Where, P_b, the 2 tones input power blockers test set at -58 dBm. The 2 tones attenuation factor, $\alpha_{ABF,2tones}$, sets the anti-blocking requirements to 4 dB.

In the case the input ADC is driven by a single tone test whose peak is at full scale (FS), the third harmonic spur level H_{3S} is determined based on the following:

$$H_{3S} = FS - 7 - (6b_{ENOB} + 1.7) \tag{2.13}$$

From (2.13) H_{3S} *is -60 dBm* for the SRR application. Considering only 1 dB degradation for the ADC SNDR (signal noise plus distortion ratio) while a P_{sig} received at the antenna is -74 dBm requires that the maximum allowable third harmonic level H_{3f} *< -54 dBm.* The third harmonic tone, H_{3f}, is generated due to a down converted blocker to intermediate frequency located at $f_{if} \le n.\frac{f_{s,ADC}}{3}$ experiences ADC third order nonlinearity. H_{3f} is the third harmonic tone that sits on top of the wanted channel after being sampled at $f_{s,ADC}$. The maximum Allowable blocker power at the ADC input is gen by:

$$P_{b,ADC,H3} = FS - 7 - \frac{\left(H_{3S} - H_{3f}\right)}{3} \tag{2.14}$$

Inserting H_{3S} *and* H_{3f} into (2.14) results in the maximum allowable blocker power into the ADC input at $f_{if} \le n.\frac{f_{s,ADC}}{3}$. $P_{b,ADC,H3}$ is at -5 dBm. This sets the anti-blocking requirement of

$$\alpha_{ABF,H3} = P_b - \left(P_{b,ADC,H3} - A\right) = P_b + 47 \tag{2.15}$$

for the SRR mode of operation, ADC sampling frequency $f_{s,ADC}$, is selected at 1GS/s. In this case, the blocker fundamental tone falls inside the channel band selection. Thus a minimum ADC sampling requirement which is 3 times the SRR bandwidth has to be maintained at the expense of higher power consumption. Assume that $f_{s,ADC}$ is 1.5 GS/s, the suppression required according to (2.15) for an -17 dBm/MHz blocker is 30 dB. Fig. 2.16 shows the anti-blocking filter requirements.

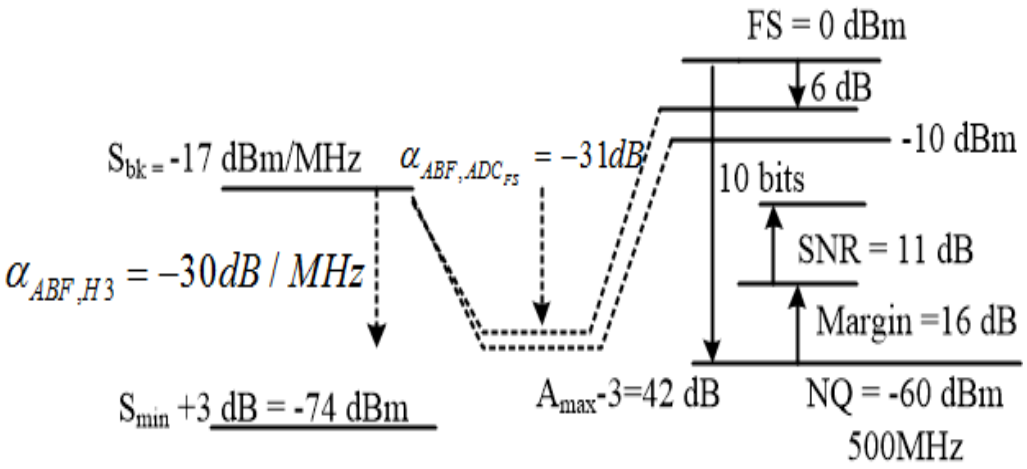

Fig. 2.16 SRR anti-blocker filter level diagram.

All blockers experience the receiver gain chain, and they should be attenuated to a level at least equal to their total power average power ratio (PAPR) below the ADC full scale [37]. This ensures that the incident signal level is below the ADC dynamic range and it's not going to be clipped. Hence, the anti-blocker filter attenuation factor based on ADC full scale is defined as:

$$\alpha_{ABF,ADC_{FS}} = P_b + A - (FS - PAPR - M) \tag{2.16}$$

where the $\alpha_{ABF,ADC_{FS}}$ has to be suppressed by 31 dB for a -17 dBm/MHz blocker with 6 dB PAPR. This requirement can be higher due AGC gain error setting and higher PAPR for out-of-band blockers.

2.5.3.2 IEEE 802.16-SC Filter Specifications

2.5.3.2.1 LMDS Anti-Aliasing Requirements

From previous section, equation (2.6) fits the need for the Local Multipoint-Distribution System (LMDS) standard and the attenuation factor for anti-aliasing is derived as

$$\alpha_{AAF} = P_{bk} - 10\log\left(BW_{bk} \big/ BW\right) + 106 \tag{2.17}$$

(2.17) assumes an SNR higher than 15 dB for the 802.16-SC due to high data rate of operation. The sensitivity level for the LMDS system is set at -85 dBm and its power level budgeted an additional 3 dB for desensitization purposes to -82 dBm with a 20/25/28 MHz bandwidth. The filter must provide 95 dB of anti-aliasing attenuation for an SRR blocker with -17 dBm/MHz power level which has a minimum bandwidth of 500 MHz. The suppression must be maintained over 28 MHz bandwidth for a multiple sampled ADC frequency, $f_{s,ADC}$ (100 MHz).

2.5.3.2.2 LMDS Anti-Blocker Requirements

The fact that 802.16-SC standard has a large bandwidth channel (28 MHz) compared to the existing ISM bands and sensitive passive devices (EECS), then most blockers falls out of band and are not considered. Under these circumstances, we took the liberty to assume multiples individual blockers with high PAPR are present, and a constant 20 dB attenuation from full scale seems logical. Based on equation (2.16), we can derive the following

$$\alpha_{ABF,ADC_{FS}} = P_b + A - (FS - 20) \tag{2.18}$$

The requirement on this blocker suppression can be met in conjunction with the DSP signals post processing and thus limit the delay response as well as the receiver's turn down time. Our proposed filter solution is an integral part of the current to voltage trans-impedance amplifier.

2.6 SICS Feed-forward Anti-Aliasing Filter

The anti-aliasing anti-blocking filter approach is based on a continuous time feed-forward polyphase high pass filter to suppress all out of band harmonics and its intermodulation products. The benefits of the feed-forward approach are to limit the power consumption compared to feedback counterpart system implementation and its non-evasive nature affecting the input current buffer impedance. A more detailed analysis will be addressed in Chapter V.

2.7 CRRA Non-idealities and System Specifications

The SICS coexistent receiver architecture and its auxiliary path is based on direct down conversion approach. Thus like any homodyne system, the CRRA suffers from various known problems similar to narrow band design from DC offset, AM detection, and low RF/IF isolation to IP2 limitation. However, these nonidealities to a certain extent are at ease in an mm-wave wideband system due to FCC regulation on power emissions and limited robustness to out of band harmonics and interferers. Hence, receiver's turn down time is expected. In the next section we will address concerns associated with receiver's linearity and limitations.

2.7.1 Limits to AM Detection

Zero IF Receiver architecture experiences AM Detection problems due to second order nonlinearity from receiver RF front-end and base-band circuits [37]. The unwanted AM power signal that falls in band after down-conversion is defined as $X_{bb}(t)$. The latter

consists of two portions where the first part experiences DC offset from zero frequency; and the second portion is time varying around DC which occupies twice the required bandwidth. The in band signal to noise ratio (SNR) between desirable power signal and power of unwanted AM signal leads to IIP2 as a function of modulation signal type.

2.7.2 Limits to Cross Modulation

Frequency cross modulation is due to third order nonlinearity of the unwanted AM modulated signal envelope; cross modulation appears on a wanted channel at a different frequency. Consider having two input signals:

$$\begin{aligned} x_1(t) &= A\cos(w_1(t)+\phi_1(t)) \\ x_2(t) &= a(t)\cos(w_2(t)+\phi_2(t)) \end{aligned} \tag{2.19}$$

where A is amplitude of $x_1(t)$ and $a(t)$ is the time varying amplitude of $x_2(t)$ respectively. Now, these two inputs are used into a nonlinear system where the output is modeled as third order polynomial as in equation (2.20):

$$\begin{aligned} y(t) &= \alpha_1 x_1(t) + \alpha_3 (x_1(t)+x_3(t))^3 + \ldots \\ y(t) &= \alpha_1 A\left[1+\frac{3}{4}\frac{\alpha_3}{\alpha_1}(A^2+2a^2(t))\right]\cos(w_1 t+\phi_1(t))+\ldots. \end{aligned} \tag{2.20}$$

where α_1, α_3 are nonlinear coefficients of the polynomial. From equation (2.20) we can see the envelope detection of unwanted AM signal which consists of two parts (A^2,

$a^2(t)$). The first parameter, A^2, is purely DC component while the latter is proportional to the time varying portion. The DC part decreases only the effective gain which increases the noise. If the blocker is not an amplitude modulated signal, it only decreases the gain. In the case of amplitude modulation, the time varying portion creates a distortion at the same frequency as the wanted signal as determined in the equation below;

$$d(t) = 3\alpha_3(\frac{a_2^2(t)}{2} - P_2)A\cos(w_1 t + \phi_1(t)) \tag{2.21}$$

equation (2.21) can be translated into a specification to determine the IIP3 which is function of the blocker power and its modulation scheme (SNR). Cross modulation is very important in receivers' using frequency division duplexing (FDD) where power leaks takes place due low T/R switch isolation particularly in SRR application. But, a more important factor in terms of receiver linearity is present in case of 2 dB RX gain compression due to undesirable high power blocker signal. In this case, gain desensitization will take precedent over the cross modulation because it becomes the limiting factor of the receiver linearity.

2.7.3 Harmonic Distortion

The SICS coexistent wideband receiver amplifies from 22 to 44 GHz where in many instances blockers harmonics caused by RF front-end nonlinear circuitry land in-band on a wanted channel signal. If there are strong blockers located at ($BW_1/2$ and

$BW_1/3$) of the desired channel frequency, through circuit nonlinearity, harmonics of those blockers will fall on the desirable wanted signal. Then, the linearity requirements for such a case are very high, but fortunately enough there are exceptions set by the FCC and allowable turn down time. Generally, the signal to distortion is calculated as:

$$IIP2 = 2P_{bk} - P_{sig} + SNR + M + 10\log(\frac{BW_{sig}}{BW_{bk}})$$
$$IIP3 = \frac{3P_{bk}}{2} - P_{sig} + \frac{1}{2}\left[SNR + M + 10\log(\frac{BW_{sig}}{BW_{bk}}) \right] \quad (2.22)$$

SNR and M are based on the modulation scheme, and VGA margin respectively. Also, blockers harmonics bandwidths are two to three times wider compared to the main blocker. The assumptions here are the worst case scenario, detectable wanted signal at the minimum detectable level, and the blocker power at -15 dBm for SRR application.

2.7.4 Harmonic Downconversion

In order to achieve the fundamental maximum gain from a mixer circuit, it must commutate its RF input signal. This will effectively correlate the RF signal by a square wave LO in time domain. In frequency domain, the RF spectrum convolves series of monotonically decreasing LO harmonics impulses compared to the fundamental. In a narrow band receiver, blockers around LO harmonics impulses (3rd and 5th harmonics) are sufficiently filtered out and may not cause much problems. But, in the case of a broadband receiver; these blockers are not attenuated and get down converted by the 3rd

and 5th LO harmonics. The down converted harmonics have substantial power compared to the fundamental. This problem is only a concern at lower end frequency spectrum, mainly for wideband receivers operating from MHz range to GHz. However, in our spectrum range from 22-44 GHz; we can foresee some problems at lower bound where LO second harmonic can affect the 44 GHz desirable channel. We can only tell more after testing if some blockers from lower spectrum are being up converted to fall in frequency band of interest.

2.8 Receiver Specifications

2.8.1 SRR Receiver Specifications

We are using a 10 bits nyquist ADC @ 1GS/s with 16 mW power consumption using 45nm CMOS [33]. The receiver specifications show a BER of 10^{-3} and an SNR of 11 dB. More importantly, the receiver recovery times is set to less than 5 ns in case of receiver saturation due to out of band harmonics or even gain compression that could cause receiver desensitization. One important measure of the receiver agility and flexibility is to have different gain and linearity settings to support multiple standards. Table 2.2 reflects the high gain settings with low noise figure. The receiver front-end has a gain higher than 50 dB and a cumulative noise figure roughly 8.6 dB. Also, the receiver requirement is sensitive enough to detect the presence of a -77 dBm signal in the presence of in band or out of band blocker. However, given the nature of wideband receiver, the blockers requirements are relaxed due to FCC regulations.

Table 2.1 Automotive radar receiver specifications

SRR RX Summary	
Range detection	0.05-40m
Range Resolution	0.2m
Range Accuracy	0.05m
PD	0.9
PFA	10^{-3}
BER	10^{-3}
Sensitivity max	-15 dBm
Sensitivity min	-77 dBm
NF	8 dB
SNR	11 dB
BW	0.5 GHz
SNRmin	1.1 dB
RX Recovery	< 5 ns

Table 2.2 RF Front-End Specifications for high gain high sensitivity mode.

	2 stages Balun/LNA	Passive Mixer	TIA/Filter	ADC
Gain	21	-15	54	-
NF	5	4.5	6	-
Cum NF	5	8.6	11	11.1

For the high linearity settings, the receiver system has a 30 dB gain and a noise figure equal to 11 dB. Although those results specifications are based on calculations, the real measurements would expect higher noise figure by 1 to 2 dB. It is also important to notice the contribution of the mixer to the overall NF. Mixer's NF more noticeable due to low LNA gain settings. It would be to our desire to have a wideband mixer with low noise figure and a high linearity. Table 2.3 shows receiver specifications for linearity settings. Although, the NF in high linearity settings can approach the original design specs, we can use a high end digital modem in DSP where it can detect a 3 dB lower SNR, reserving 16 dB NF tolerances.

2.8.2 Mini-UAV SAR Radar Receiver

Most synthetic aperture radars SAR are operating in the X-band due to lower atmospheric attenuation. However, our SAR system will be operating in the Ka band at 35-37 GHz. Our bandwidth will be specified based on the sensitivity level desired in a

clutter environment. But, before moving into the specifications of the SAR radar; the SAR radar is split into two segments. One segment makes the TX/RX implemented on

Table 2.3 RF front-end specifications for high linearity mode settings.

	2 stages Balun/LNA	Passive Mixer	TIA/Filter	ADC
Gain	18	-26	54	-
NF	5.5	4	7	-
Cum. NF	5.5	9.5	11	11.1

unmanned aerial vehicular (Mini-UAV) board with a data link. The second segment conforms of the A/D and the signal processing engine and is placed on the ground next to the operator. Size, weight, and power are the name of the game for a UAV. Making Ka band frequency of operation is based on the following: 1) miniaturized block components due to higher frequency which is very suitable for SWP; 2) it can provide a good outline and surface texture for human man-made objects; 3) image exploitation is easily compensated due to motion of UVA platform. But, the only drawback is the high atmospheric loss. Now, based on similar setup from previous design, and using an ADC with 100 MS/s for 12 bits of resolution with very reasonable power dissipation, the VGA has to operate between 58 to 10 dB gain settings. Following the previous approach, we shared part of the power dissipation between the front-end system and the DSP. Table 2.4 shows UAV receiver targeted specifications and the benefits of operating in Ka band.

Table 2.4 SAR RX specifications for UAV

SAR Radar RX	
Flight altitude	(300- 2000)m
Velocity relative to ground	(10-40) m
Image resolution	0.5x0.5 m
SAR mode(s)	Stripmap Mode
Swath	(500-1000)m
Max. onboard power consumption	200 mW
Datalink type	Analog
Datalink bandwidth	100 MHz
Alpha Angel	18-30(degree)
Max Sensitivity	-15
Min Sensitivity	-105
SNR	11 dB
NF	8 dB
BW	100 MHz
SNRmin	1.1 dB
Modulation	PD

Note that most of the specifications for the RX of the UAV are set according to [3]. One aspect of this system is for positing object and target detection for military use, like ground army forces for enemy's detection and tracking using very light weight UAV. Now, as far as jamming the radar on board of the UAV, most solutions provided are thru signal manipulations and using different modulation schemes; more of a DSP solution. Furthermore, having a low phase noise VCO with accurate frequency tuning at such high frequency is very challenging. So, any frequency drift by more than 0.5 % and we are out of frequency band of SAR radar. This could be a very serious problem at such high frequency band.

2.9 SICS Coexistent Receiver System Architecture

The overall system consists of multiple blocks based on wideband approach with reconfigurable/programmable RF front-end. In brief, we are planning on implementing a variable gain LNA with high linearity at small expense of higher noise figure. Also, having variable second gain stage based on class AB transconductance AC coupled to passive mixer thus reducing the 1/f noise. The class AB Gm driving stage prevents I/Q crosstalk without degrading linearity. A current gain buffer stage for high linearity IIP2 based on trans-impedance amplifier follows the passive mixer. Given the current mode output mixer, a trans-impedance amplifier is needed to convert current mode RF to voltage mode baseband. Up until the mixer output, no filtering has taken place yet due to wideband LNA output matching network and no RF pre-filter. A feed-forward high pass

polyphase filter is implemented to provide cancellation for all intermodulation products and generated LO harmonics.

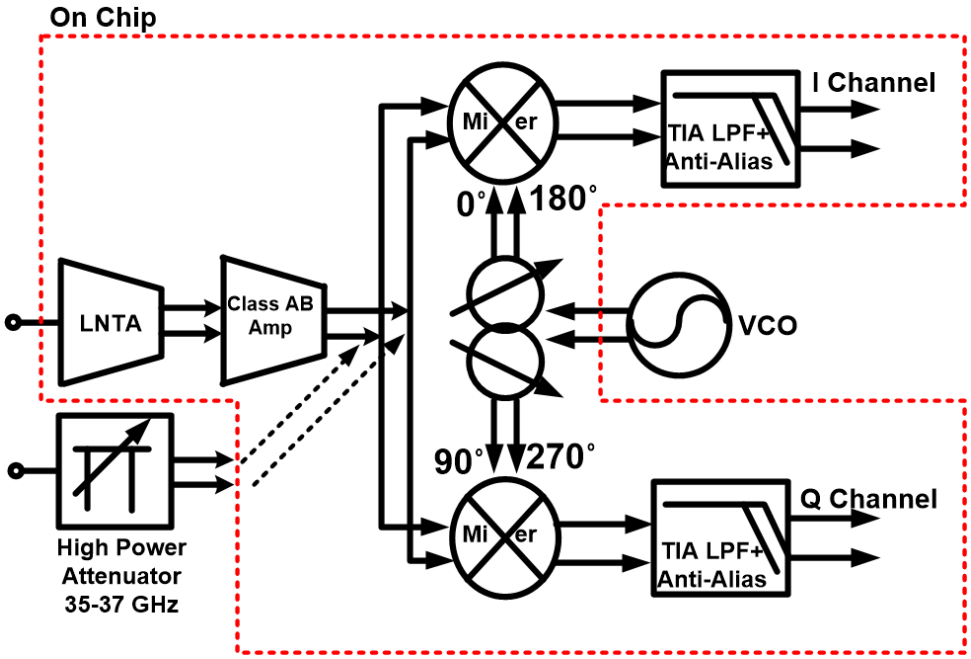

Fig. 2.17 SICS coexistent receiver architecture.

Fig. 2.17 shows the system structure design level for the coexistent receiver's architecture and its auxiliary path to support UAV radar application. The next following dissertation chapters will describes receiver circuits' implementation.

CHAPTER III

A WIDEBAND LOW POWER CONSUMPTION 22-35 GHZ ACTIVE BALUN-LNA

3.1 Introduction

Low-noise amplifier (LNA) plays a crucial role in achieving high gain and linearity over wide operating frequency ranges for these receivers. Active balun-LNAs are LNAs capable of providing differential outputs from a single-ended input and are important component in receivers. Various wideband active balun-LNAs on silicon at low frequencies, which implement active and passive feedback mechanisms to improve linearity, gain and phase errors mismatches, have been reported [38],[39]. However, employing active feedback comes at the expense of power and nonlinearity rendering the harmonics cancellation ineffective [39]. A linearization technique based on derivative superposition and its improved derivative version tend to provide impressive input referred third order intercept point (IIP_3) [45], [47]. The derivative superposition methods use auxiliary N/PMOS path in weak inversion to cancel the third-order nonlinear current of the main transconductance gain-stage path, thus enhancing IIP_3. Nonetheless, this improvement is subject to deter the second inter-modulation product (IP_2) due to nonlinear cross terms between the two paths [45]. Further, current-mode balun-LNA based common-gate common-source structures with bias control and output conductance kept constant show optimum behavior for both noise and linearity [41], [46]. Such constrain across wideband is costly in terms of power consumption and

subject to process, voltage, and temperature variations. Another approach is making third inter-modulation IM3 cancellation independent of frequency in bipolar junction transistor (BJT) [42]-[44]. A second-harmonic control with fully differential mode configuration using BJT devices facilitates frequency independent IM3 cancellation [42]. In [43]-[44], IM3 cancellation happens due to current hyperbolic tangent behavior from dual gated BJT devices in differential and pseudo-differential modes added to the output. However, the cost is doubled in noise and power consumption. All of these techniques were implemented in designs operating below 2.4 GHz. A 20 GHz balun-LNA using 0.25μm SiGe BiCMOS technology was reported in [40]. This balun-LNA consists of a common-emitter gain stage followed by a single-to-differential output buffer stage using a common-emitter common-base (CE-CB) structure with ac current source. This design suffers from very high phase and gain mismatches, thus limiting the bandwidth. These works show a tradeoff between linearity, power consumption, and gain.

In this Chapter, a 0.18μm SiGe BiCMOS 22-35 GHz active balun-LNA with high linearity and low power consumption is presented. The linearity improvement is attained using a new linearity technique based on a constant Gm-cell transconductance that forms the balun-LNA structure. The constant Gm-cell transconductance is established through equal emitters' area ratios of the balun-LNA. The constant small-signal Gm-cell transconductance remains independent of input and output variations under large-signal behavior and provides second-order intermodulation (IM_2) cancellation, resulting in improved linearity. The low power consumption is due in part

to the coupled inductors used between cascaded stages. The balun-LNA targets multi-standard multi-channel receivers' applications ranging from 22-35 GHz that require high linearity. Many microwave and mm-wave applications not only coexist, but also overlap each other on the same frequency spectrum, making the linearity the bottle neck for the receiver's dynamic range.

3.2 Proposed Architecture and Circuit Analysis

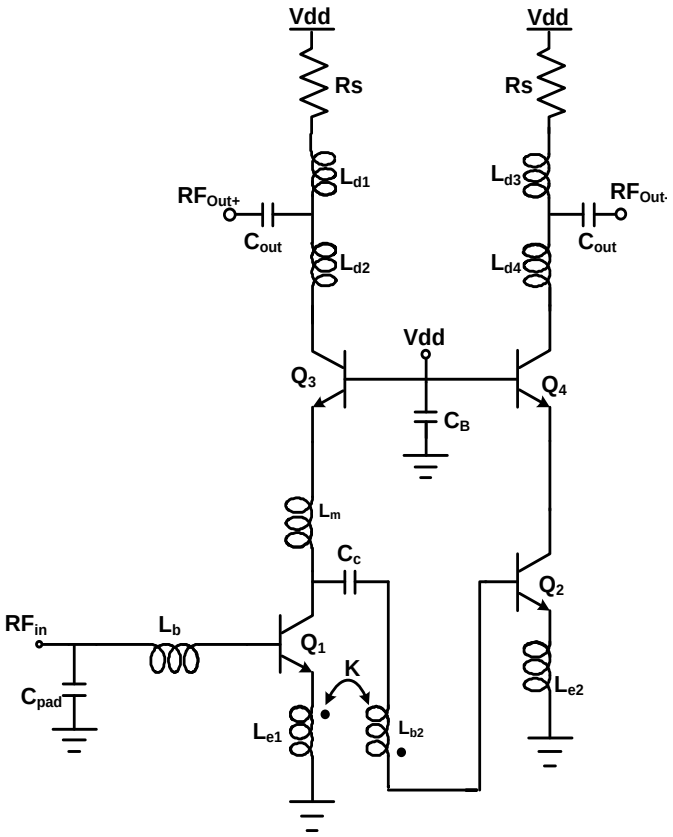

Fig. 3.18 Proposed Balun-LNA architecture.

Figure 3.18 shows the schematic of the 22-35 GHz (single-to-differential) wideband active balun-LNA with high gain, high linearity, and low power consumption. The proposed balun-LNA architecture consists of a main transconductance gm gain stage, Q_1, coupled to an auxiliary gain path, Q_2, through a transformer. The coupled transformer increases the signal swing at the input of the second stage, thus boosting the Gm transconductance, hence gain, and reducing the power consumption. The composite Gm cell defined by transistors Q_1, Q_2, and Q_3 plays a major role in improving the linearization of the structure. The stipulated total Gm stays constant even in the presence of variations in gm_1 of Q_1 and gm_2 of Q_2 due to high input power. As the collector currents of transistors Q_1 and Q_2 vary from their quiescent bias under large voltage swing; the gm's dependency on equal emitters' area (A_e) ratios keeps the overall Gm-cell constant. The overall Gm's constant and frequency-independent characteristic behavior with IM2 cancellation results in linearity enhancement. A simple wideband input matching network is established using inductors L_b and L_{e1} similar to [48]. The effect of the coupling transformer (L_{e1}, L_{b2}) on the input matching is considered thoroughly in the following section. Inductive shunt peaking is used at the output loads to extend the matching bandwidth of the balun-LNA. Finally, the noise due to the cascode transistor Q_3 is reduced by adding an inductor L_m to resonate away the parasitic capacitance at the emitter, thus reducing the output noise. Table 3.5 shows all design components parameters to achieve the desirable balun-LNA performance where emitter area is defined by $WxL_{Q1,\ Q2,\ Q3,\ and\ Q4}$ and is equal to 0.2x10.16 μm^2. All of these design techniques are implemented to design the 22-35-GHz active balun-LNA.

Table 3.5 Circuit components values of the implemented balun-LNA.

Emitter WxL_{Q1} 0.2x10.16 μm^2	Emitter WxL_{Q2} 0.2x10.16 μm^2	Emitter WxL_{Q3} 0.2x10.16 μm^2	Emitter WxL_{Q4} 0.2x10.16 μm^2
C_{be1} = 105 fF	L_{d3} = 240 pH	L_{b2} = 120pH	C_{pad} = 60fF
C_{be2}= 62 fF	L_b = 300 pH	K = 0.34	L_{e1}/L_{e2} = 80pH
C_c = 300fF	L_m = 120pH	L_{d2}/L_{d4} = 90pH	L_{d1} = 260pH

3.2.1 Input Matching

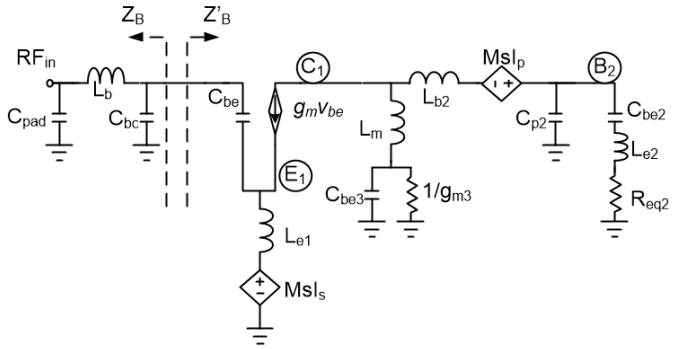

Fig. 3.19 Small signal model of the balun-LNA's input impedance. gm is the small signal transconductance of Q1. Req2 is defined as ωTLe2 of Q2. Ip and Is are the primary and secondary currents of the transformer.

Fig. 3.19 shows the small-signal input impedance of the balun-LNA derived from its schematic in Fig. 3.18. To keep the analysis simple; the input impedance of the balun-LNA is split into two sections Z_B and $Z_B^{'}$, which represent the input impedances looking into the respective networks. Under the perfect matching condition, $Z_B = Z_B^{*}$. Z_B forms a pi-network with wideband matching characteristics, whose quality factor (Q) reduces

due to the loading of the network represented by $Z_B^{'}$. For the ac coupled transformer (L_{e1} and L_{b2}) in $Z_B^{'}$, the coupling coefficient *K* and the number of turn *n* can cause the optimum matching point to shift; yet keeping wideband impedance matched to the input port. To study this effect, an expression for the complex conjugate impedance Z_B^{*} is derived. Z_B^{*} is found using the small-signal model in Fig. 3.2 whereas the adapted transformer model is similar to that in [49]. Applying Kirchhoff current law (KCL) at nodes E_1, C_1, and B_2, where M is the mutual inductance; $K = \frac{M}{\sqrt{L_P L_S}}$ is the coupling coefficient, and $n = \sqrt{L_S / L_P}$ is the turn ratio of the ac coupled transformer, can lead to Z_B^{*}. C_{pad} is defined as the parasitic capacitance due to RF pad on chip. C_{be}, C_{be2}, and C_{be3} are the parasitic capacitances at the base-emitter junctions of transistors Q_1, Q_2, and Q_3, respectively. Additionally, C_{bc}, and C_{p2} are the capacitances at the base-collector junction of transistors Q_1 and Q_2. The KCL equations yield, after several manipulations:

$$V_B^{'}(s) = i_B^{'}(s)\left(1 + \frac{1}{sC_{be}}\left(1 + sg_m L_{e1}\right)\right) - MsI_s \tag{3.1}$$

where $V_B^{'}(s)$ is the base voltage looking into $Z_B^{'}$ network port, and $i_B^{'}(s)$ is its current defined as

$$i_B^{'}(s) = sC_{be}v_{be} \tag{3.2}$$

The secondary current I_s of (1) can be derived as

$$I_s = i_B^{'}(s)\left[\frac{g_m Z_1 - sM\left(sC_{be} + g_m\right)}{sC_{be}\left(Z_1 - sL_{b2} - Z_2\right)}\right] \tag{3.3}$$

where

$$Z_1 = sL_m + \frac{1}{g_{m3} + sC_{be3}} \tag{3.4}$$

and $$Z_2 = \frac{\left(\frac{1}{sC_{be2}} + sL_{e2} + R_{eq2}\right)}{1 + \frac{1}{sC_{p2}}\left(\frac{1}{sC_{be2}} + sL_{e2} + R_{eq2}\right)} \tag{3.5}$$

Substituting I_s into $V_B^{'}(s)$ and taking the ratio between (3.1) and (3.2) gives

$$Z_B^{'}(s) = 1 + \frac{1}{sC_{be}}\left[1 + sL_{e1}\left(g_m - \frac{s(Kn)g_m Z_1}{Z_1 - sL_{b2} - Z_2} + \frac{s^2(Kn)^2 sL_{e1}\left(g_m + sC_{be}\right)}{Z_1 - sL_{b2} - Z_2}\right)\right] \tag{3.6}$$

$Z_B^{'}(s)$ shows that any changes in the coupling coefficient K or the number of turn ratio n for the coupled transformer can affect the poles and zeros alike; thus causing the matching to shift into higher frequency; yet maintaining the wideband characteristics due to poles-zeros cancellation effect. Fig. 3.20 shows the schematic level simulation for the magnitude of $Z_B^{'}(s)$ with and without the transformer. It is clear that the wideband matching characteristic is maintained with only small variation less than 2Ω in the worst case.

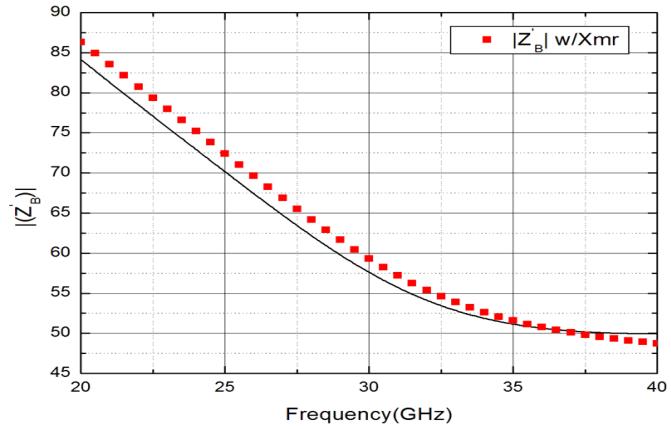

Fig. 3.20 Comparison of magnitudes of Z'B with and without transformer.

3.2.2 Linearity

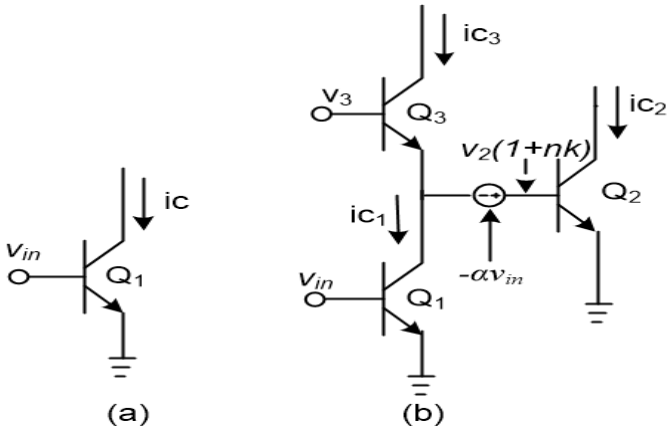

Fig. 3.21 Linearity model analysis: (a) Conventional CE stage and (b) Proposed Gm stage.

Fig. 3.21 shows the linearity model analysis for the conventional common-emitter gm stage as well the proposed balun-LNA Gm structure including the effect of the transformer. Using Taylor series expansion approximation, the output collector current for the CE stage shown in Fig. 3.21 (a) is given by

$$i_C \cong gm\left[\sum_{q=1,2,\ldots}^{\infty} \frac{V_T}{q!}\left(\frac{v_{in}}{V_T}\right)^q\right] \tag{3.7}$$

where $gm = I_{Q1} / V_T$, with I_{Q1} being the quiescent current of Q_1 and V_T being the thermal voltage, is the voltage to current conversion also known as the small signal transconductance *gm;* and v_{in} is the input voltage. From (3.7), taking the q^{th} order derivatives of *gm* with respect to v_{in} encompasses all nonlinearities for the CE stage. Assuming $v_{in} = V_a \cos \omega t$ and taking the ratio between the second and the fundamental harmonic amplitude in a CE stage gives the second-order harmonic distortion as

$$HD_2 = \frac{1}{4}\left[\frac{V_a}{V_T}\right] \tag{3.8}$$

The collector currents in the proposed Gm stage for the balun-LNA as shown in Fig. 3.21(b) can be derived using (3.7) as

$$\begin{aligned}
i_{C1} &\cong I_{Q1}\left[\frac{v_{in}}{V_T} + \frac{1}{2!}\left(\frac{v_{in}}{V_T}\right)^2 + \frac{1}{3!}\left(\frac{v_{in}}{V_T}\right)^3 + \cdots\right] \\
i_{C2} &\cong I_{Q2}\left[\frac{v_2(1+nK)}{V_T} + \frac{1}{2!}\left(\frac{v_2(1+nK)}{V_T}\right)^2 + \frac{1}{3!}\left(\frac{v_2(1+nK)}{V_T}\right)^3 + \cdots\right] \\
i_{C3} &\cong I_{Q3}\left[\frac{-v_2}{V_T} + \frac{1}{2!}\left(\frac{-v_2}{V_T}\right)^2 + \frac{1}{3!}\left(\frac{-v_2}{V_T}\right)^3 + \cdots\right]
\end{aligned} \tag{3.9}$$

Using (3.9), we find the differential output current $i_{Out} = i_{C3} - i_{C2}$ with respect to the input voltage v_{in}, *a*ssuming $i_{C1} = i_{C3}$ and using the fact that $-v_2/v_{in} = -gm_1/gm_3 = -$

A_{e1}/A_{e3}, where A_{e1} and A_{e3} represent the emitter Area for Q_1 and Q_3; respectively, as

$$i_{Out}=\left\{\begin{array}{l} I_{Q3}\left[\frac{-\left(A_{e1}/A_{e3}\right)v_{in}}{V_T}\right]\left[1+\frac{I_{Q2}\left(1+nK\right)}{I_{Q3}}\right]+\frac{I_{Q3}}{2}\left[\frac{\left(A_{e1}/A_{e3}\right)v_{in}}{V_T}\right]^2\left[1-\frac{I_{Q2}\left(1+nK\right)^2}{I_{Q3}}\right] \\ +\frac{I_{Q3}}{6}\left[\frac{-\left(A_{e1}/A_{e3}\right)v_{in}}{V_T}\right]^3\left[1+\frac{I_{Q2}\left(1+nK\right)^3}{I_{Q3}}\right]+\cdots \end{array}\right\} \tag{3.10}$$

Substituting $v_{in}=V_a\cos\omega t$ into (3.10) results in

$$i_{Out}=\left\{\begin{array}{l} \left[I_{Q3}\left(\frac{-(A_{e1}/A_{e3})V_a}{V_T}\right)\right]\left[\begin{array}{l}\left(1+\frac{I_{Q2}(1+nK)}{I_{Q3}}\right)- \\ \frac{1}{8}\left(\frac{(A_{e1}/A_{e3})V_a}{V_T}\right)^2\left(1+\frac{I_{Q2}(1+nK)^3}{I_{Q3}}\right)\end{array}\right]\cos\omega t \\ +\frac{I_{Q3}}{4}\left(\frac{(A_{e1}/A_{e3})V_a}{V_T}\right)^2\left(1+\cos 2\omega t\right)\left(1-\frac{I_{Q2}(1+nK)^2}{I_{Q3}}\right) \\ +\frac{I_{Q3}}{24}\left(\frac{-(A_{e1}/A_{e3})V_a}{V_T}\right)^3\left(\cos 3\omega t\right)\left(1+\frac{I_{Q2}(1+nK)^3}{I_{Q3}}\right)+\cdots \end{array}\right\} \tag{3.11}$$

From (3.11), considering the ratios between the second, and the fundamental amplitude harmonics as well between the third and the fundamental amplitude harmonics for the proposed Gm stage gives $HD_{2,Gm}$ and $HD_{3,Gm,}$ respectively, as

$$HD_{2,Gm} = \left| \frac{\left(\frac{1}{4}\right)\left[\frac{(A_{e1}/A_{e3})V_a}{V_T}\right]\left[1-\frac{I_{Q2}(1+nK)^2}{I_{Q3}}\right]}{\left[\left(\frac{1}{8}\right)\left(\frac{(A_{e1}/A_{e3})V_a}{V_T}\right)^2\right]\left[1+\frac{I_{Q2}(1+nK)^3}{I_{Q3}}\right]-\left[1+\frac{I_{Q2}(1+nK)}{I_{Q3}}\right]} \right| \tag{3.12}$$

$$HD_{3,Gm} = \frac{\left(\frac{1}{24}\right)\left[\frac{(A_{e1}/A_{e3})V_a}{V_T}\right]^2\left[1+\frac{I_{Q2}(1+nK)^3}{I_{Q3}}\right]}{\left\{\left[1+\frac{I_{Q2}(1+nK)}{I_{Q3}}\right]-\left(\frac{1}{8}\right)\left[\frac{(A_{e1}/A_{e3})V_a}{V_T}\right]^2\left[1+\frac{I_{Q2}(1+nK)^3}{I_{Q3}}\right]\right\}} \tag{3.13}$$

As can be seen from (3.12), the cancellation of the nonlinearity factor generated due to $HD_{2,Gm}$ is obtained under the condition $I_{Q2}(1+nK)^2 = I_{Q3}$, which means $g_{m2} = \frac{g_{m3}}{(1+nK)^2}$ and, in turn, $V_{BE3} \approx V_{BE2}$ and $A_{e2} = A_{e3}$. Hence, the overall Gm stays constant even in the presence of variations in gm_1 and gm_2 due to large input voltage signal. As the collector currents differ from their quiescent bias under large input power; the gm's dependency on the emitter area ratios keeps the overall Gm constant. This large signal constant gm characteristic results in linearity improvement. As $HD_{3,Gm}$ from (3.13) cannot be cancelled, equation (3.13) dictates the linearity limitation for this proposed architecture. However, there is a clear tradeoff between gain and linearity for this balun-LNA architecture. Keeping the aspect ratios $A_{e2} = A_{e3} = A_{e4}$ and $g_{m2} = \frac{g_{m3}}{(1+nK)^2} = g_{m4}$ between Q_2, Q_3, and Q_4 maximize the linearity at the expense of

gain due to $G_m = \left[g_{m1} + \left(\frac{g_{m1}}{g_{m3}} + nK \right) g_{m2} \right]$.

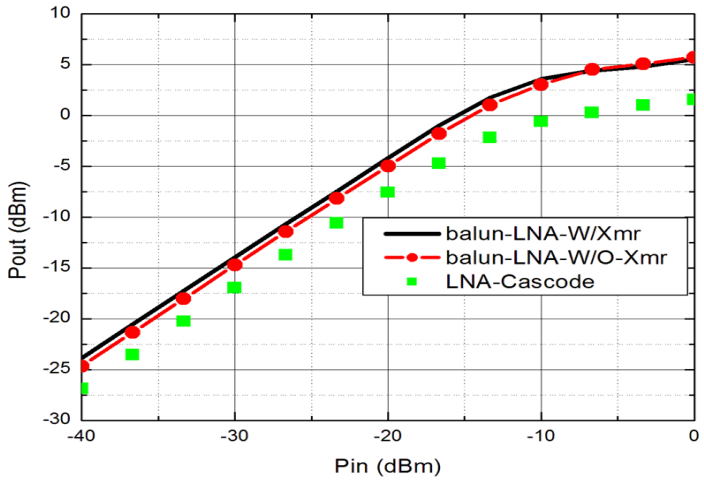

Fig. 3.22 Compression curves for (a) Cascode LNA, (b) balun-LNA with transformer, (c) balun-LNA without transformer.

Also, the gm_2 transconductance increases due to the transformer's product nK which help boost the gain for less dc current. However, given the transformer inductors' sizes and the limited *n*K value the linearity degradation is very small as depicted in Fig. 3.22. The latter shows the simulation results of the input referred 1dB gain compression for a cascode LNA and the proposed balun-LNA with and without transformer. All circuits consume 6.4 mA current from a 1.8V supply and achieve 16-dB power gain. The P1dB for the regular cascode LNA and the proposed balun-LNA with and without transformer are -17.9 dBm, -13.37 dBm and -13.26 dBm, respectively. The linearity improvement of the balun-LNA with transformer as compared to the cascade LNA is better than 4.53 dB.

3.2.3 Noise Analysis

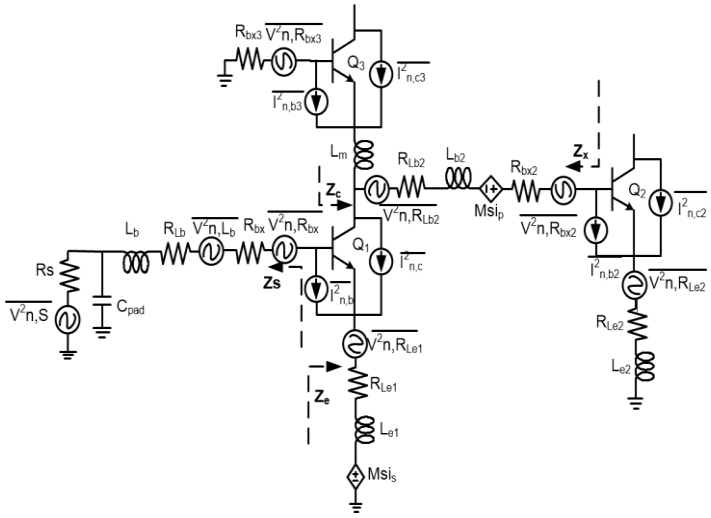

Fig. 3.23 Noise sources model of the proposed balun-LNA.

The noise of the proposed balun-LNA is dominated by the input stage including the matching network and its auxiliary path. Fig. 3.23 shows the circuit's main noise sources for the proposed balun-LNA. The noise sources include base and collector noise currents of Q_1 and Q_2. Noise due to the parasitic base resistances R_{bx} and R_{bx2} of Q_1 and Q_2, respectively, and noise due losses of L_b, R_{Lb}, and coupling transformer L_{e1} and L_{b2}, R_{Le1} and R_{Lb2}, is considered in the noise model. The noise due to the cascode transistor Q_3 is considerably reduced due to inductor L_m rendering the degenerated impedance high at resonance, thus making its noise contribution negligible [48]. Furthermore; noise in the auxiliary path due to cascode transistor Q_4 is neglected due to multi-cascaded transconductance gain stages and, as a result, all cascode transistors are neglected in the

following analysis.

The equivalent input-referred noise due to the base and collector current shot noise of Q_1, Q_2, and its base parasitic resistance R_{bx2} are given by the Appendix equations (A8) - (A12). According to (A8) and (A9) from the Appendix, the input referred noises of Q_1 increases proportionally with L_b inductor's loss. This is because the signal to noise ratio (SNR) between the input and the emitter-base junction is inversely proportional to L_b. It is clear that there is a tradeoff between the input matching requirement for power transfer and the noise figure for this balun-LNA structure. However, equations (A8)-(A9) reflect the effect of the coupling transformer on the emitter impedance Z_e of Q_1. A higher Z_e helps improve the collector current noise at the expense of lower (SNR) at the emitter-base junction. Similarly, equations (A10-A12) show an increase in the SNR at the base-emitter junction of Q_2 raising the voltage gain through the coupling transformer by *(nk)* factor. The collector shot noise of Q_2 and its parasitic base resistance noise R_{bx2} are improved by the same factor.

The total input referred voltage noise due to Q_1 and Q_2, $\overline{v^2_{ni,Q_{1,2}}}$, normalized to the noise voltage source impedance is given by

$$\frac{\overline{v^2_{ni,Q_{1,2}}}}{4kTR_S\Delta f} \approx \frac{\Psi_1(\omega)}{g_{m1}} + \left(\Psi_2(\omega)\right) g_{m1} + \frac{\Psi_3(\omega)}{\left[\frac{g_{m1}}{g_{m3}} + nK\right]} + \left(\Psi_4(\omega)\right)\left[\frac{g_{m1}}{g_{m3}} + nK\right] g_{m2} + \frac{\Psi_5(\omega)}{\left[\frac{g_{m1}}{g_{m3}} + nK\right] g_{m2}} \tag{3.14}$$

$\Psi_1(\omega) - \Psi_5(\omega)$ is given by the Appendix equations (A13) - (A17). This result shows that the collector current shot noise of Q_1 and Q_2 can be improved by increasing gm_1, gm_2, and transformer's product nK, respectively. However, such improvement comes at the expense of degrading the base current shot noise. Hence, there is an optimum value for gm_1 and gm_2 to minimize the total input-referred noise voltage due to Q_1 and Q_2. Differentiating the first two terms and the last two terms of (3.14) with respect to gm_1 and gm_2 respectively and equating the resultant expressions to zero, results in $gm_{1,opt}$ and $gm_{2,opt}$, given by

$$g_{m1,opt} = \sqrt{\frac{\Psi_1(\omega)}{\Psi_2(\omega)}} \tag{3.15}$$

and

$$g_{m2,opt} = \sqrt{\frac{\Psi 5(\omega)}{\Psi 4(\omega)}} \frac{1}{\left[\frac{g_{m1}}{g_{m3}} + nk\right]} \tag{3.16}$$

The third term in (14) is due to the parasitic base resistance noise, R_{bx2}, is limited by $g_{m1,\ opt}$, A_{e2} emitter area of transistor Q_2, and the transformer coupling factor (nK). The total input referred noise figure of the proposed balun-LNA structure is given by

$$NF_{tot}(\omega)\Big| \approx 1+\frac{R_{L_b}+R_{bx}}{R_S}\left(1+\omega^2 C_{pad} R_S\right)+2\sqrt{\Psi_1(\omega)\Psi_2(\omega)}$$
$$+\frac{\Psi_3(\omega)}{\left[\frac{1}{g_{m3}}\sqrt{\frac{\Psi_1(\omega)}{\Psi_2(\omega)}}+nk\right]}+2\sqrt{\Psi_4(\omega)\Psi_5(\omega)} \qquad (3.17)$$

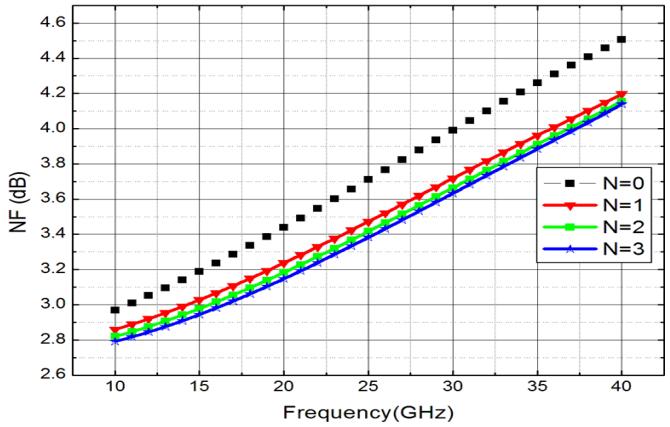

Fig. 3.24 NF for the differential output balun-LNA with ideal coupling coefficient; K; and transformer multiple turns n.

Fig. 3.24 shows the noise figure simulations for the differential output of the balun-LNA. From (3.17); it is clear that signal to noise ratio (SNR) degradation between the source generator and the base-emitter junction capacitance is due to matching inductance loss L_b, R_{Lb}, the parasitic base resistance, $R_{bx,}$ and pad capacitance, C_{pad}. Furthermore; an increase in the turn ratio of the coupling transformer could improve the noise figure. However, the turn ratio cannot be increased randomly considering the coupling transformer non-idealities [50]. Losses associated with parasitic resistances and capacitances at the base of Q_2 measures quadratically compares to the secondary

inductance of the transformer. Hence, the self-resonance frequency of the inductance suffers as well as the magnetic coupling, M, reflecting higher noise. Ultimately, there are practical limits for the voltage gain boosting effect and the optimal turn ratio *n*; thus achieving the lowest noise figure.

3.2.4 Stability and Power Efficiency

The effects of capacitors C_{bc} and C_{p2} on both channels are reduced due to the cascode structure. The added transistors, Q_3 and Q_4, transform the input impedances of the driving stages from negative impedances into a capacitive one; hence the stability is maintained. The transformer is designed in inverting configuration to provide gain boosting without compromising the balun-LNA stability.

The proposed balun-LNA structure having dual g_m output from a single-ended input combines the LNA characteristic with the balun behavior into a single block. The inverting coupling transformer boosts g_{m2} by *(nK)* factor. This topology has two properties: *1)* it can further boosts the voltage gain at the base-emitter junction, thus reducing the dc bias point for a specific gain target which means less dc power consumption, and *2)* by controlling the coupling coefficient polarity, *K*, through proper layout of the stacked transformer, the voltage gain can be increased (with positive K) or remains the same with bandwidth extended (for negative K).

3.3 Transformers and Inductors Layouts

The presence of the parasitic capacitors and resistive losses generated from routing paths in integrated circuits causes lower quality factor in passive components, which could be significant at millimeter-wave frequencies. To accurately account for such effects, all inductors are simulated using electromagnetic (EM) simulator IE3D [51]. Inductors L_{d1}, L_{d3}, and L_b are designed using spiral inductor due to their relatively large inductances. However; a careful consideration is being assigned for the metal width trading off the resistive loss, parasitic coupling to the substrate, quality factor and inductors self-resonance frequencies. To guarantee inductors behaviors at mm-wave frequencies; it is important to achieve the quality factor peak beyond the frequency of interest. To reduce all type of losses the top metal M6 is chosen for all inductors. Furthermore; inductors L_m, L_{e2}, L_{d2}, L_{d4}, and the coupling transformer L_{e1}, L_{b2}, are all implemented using microstrip transmission lines.

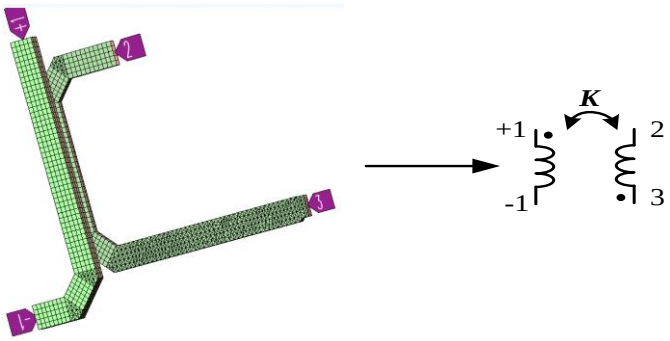

Fig. 3.25 Stacked transformer layout structure and its schematic. Port (1,-1): M6; Port (2, 3): M5

The stacked coupling transformer is shown in Fig. 3.25 where L_{e1} and L_{b2}

consists of primary and secondary inductors; respectively. The transformer inverting configuration is implemented to form a feed-forward path boosting the transconductance gm_2 input stage. All electromagnetic effects from eddy current substrate loss to frequency dependent metal loss are considered in the design process of the transformer.

In order to reduce the parasitic loss effects at high frequency; the stacked transformer is realized with the top metal layers M6 and M5 which are the thickest and farthest from the substrate, thus reducing losses. The quality factor and self-resonance frequency for both L_{e1} and L_{b2} remain almost identical. A high quality factor (Q) for the transformer inductances is needed to reduce its noise contribution into the balun-LNA structure.

For the optimal magnetic coupling between transformer conductors; the metal width for the microstrip transmission lines forming the transformer are set to the smallest possible ($7.5\ \mu m$) constrained by the ohmic losses, the dc current, and the quality factor. The narrower the conductor dimensions width the higher the magnetic coupling between the transformers' turns. However; increasing the metal width leads to higher parasitic capacitance losses to the substrate.

The coupling coefficient, K, for the stacked transformer is limited by the process technology due to metal thickness and minimum layers spacing as well as the optimal turn's ratio at mm-wave frequency. Section II-C states clearly the benefits and limitations of increasing the turn ratios for the stacked transformer. Thus, the stacked transformer is designed with 1:1 turn's ratio. L_{e1} and L_{b2} inductances are 82pH and 120pH, respectively. A coupling coefficient; K equal to 0.34 is achieved in the band of

interest. Fig. 3.26 shows the EM simulations results of the transformer inductances and the coupling coefficient. These parameters remain almost constant in the frequency range of interest. This is because the self-resonance frequency of the transformer is at higher frequency.

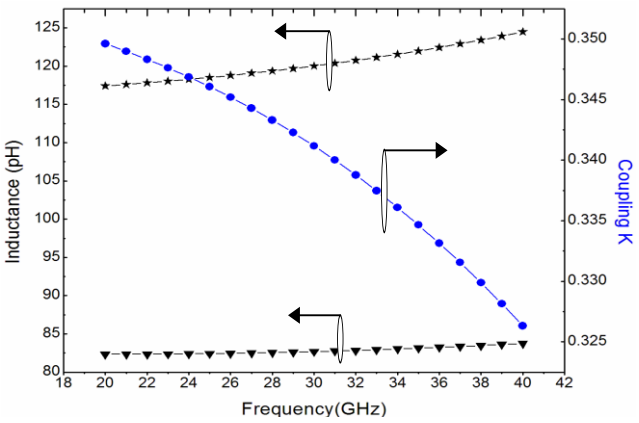

Fig. 3.26 Inductance values; Le1, Lb2, and coupling coefficient, K, for stacked transformer using IE3D.

3.4 Active Balun-LNA Perfomance

The wideband Balun-LNA was fabricated using 0.18 μm BiCMOS technology from Tower Jazz Semiconductor [52]. Fig. 3.27 shows the die micrograph of the balun-LNA, where the total area is 0.46mm^2 excluding the RF and DC pads. On-wafer measurements were done using RF differential probes (G-S-G-S-G) for input and outputs. The use of RF differential input probe is necessary for calibration purposes using Cascade Microtech Impedance Standard Substrate (ISS) [53]. Although an RF differential probe is used at the input, the input signal is fed into only one port. Also, a 6-

pin DC probe is used to provide the DC biasing. The balun-LNA core consumes 5 mA from 1.8V supply.

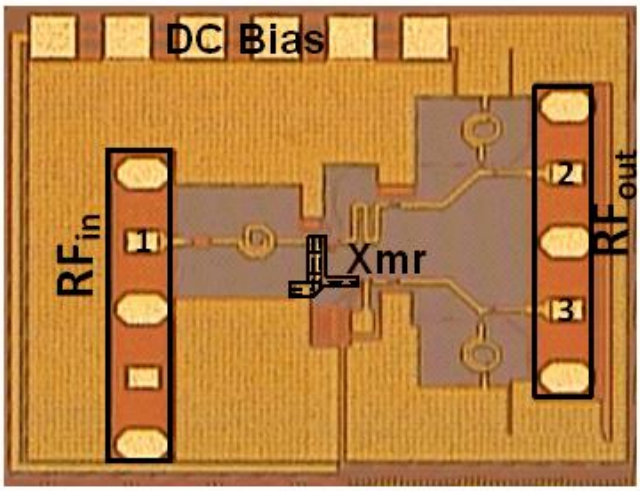

Fig. 3.27 Die photograph of the balun-LNA.

Fig. 3.28 shows the measured and simulated input return losses (S_{11}) for the balun-LNA. Measured S_{11} is larger than 8.7 dB for the entire operating frequency range of 22-35 GHz and up to 40 GHz. Fig. 3.29 displays the measured and simulated output return losses S_{22} and S_{33}. Measured S_{22} is better than 9 dB from 22-29 GHz and S_{33} is larger than 7.5 dB from 23.5-27.4 GHz. The shifting of the return loss responses at the outputs of the balun-LNA is mainly due to the variations of the small metal insulator metal (MIM) output capacitances as well as the parasitic inductances coupling to the substrate. Consequently, the measured power gains for the balun-LNA (S_{21} and S_{31}) shift to 26.8 GHz and 27 GHz, respectively, as seen in Fig. 3.30, which shows S_{21} and S_{31} achieving a gain of 15.6 and 15.4 dB, respectively. This represents a measured differential gain boost of 2.0 dB and 2.4 dB for S_{31} and S_{21} compared to simulations. The

measured 3-dB bandwidths for S_{21} and S_{31} are 7.6 GHz and 11.5 GHz, respectively. A 3.9 GHz bandwidth difference between S_{21} and S_{31} is mainly due to asymmetric signal path from input to outputs and unequal parasitic capacitances to the substrate. The former is related to the unbalanced design structure from the input signal path to the differential outputs; hence the capacitive signal loading and substrate losses are different. Fig. 3.31 shows the measured stability of the proposed balun-LNA in term of the stability parameter μ [54], which is derived from the measured S-parameters. The balun-LNA is unconditionally stable for both channels across the 22-35 GHz bandwidth according to $\mu(s) > 1$. The measured noise figures for both channels are shown in Fig. 3.32, where the noise figures between input port 1 and output port 3 (NF_{31})and input port 1 and output port 2 (NF_{21}) vary from 4.5 dB to 5.8 dB and from 4.6 dB to 7.09 dB, respectively. NF_{21} experiences higher noise figure particularly due to channel gain drop. In the case of a differential to single ended balun with (100:50) Ω impedance ratio applied at the output of the proposed balun-LNA, a 3-dB differential gain increase is possible and a much lower noise figure can be achieved due to common mode noise cancellation. The measured gain and phase imbalances are shown in Fig. 3.33. The gain and phase mismatches from 20-30 GHz are 1.8 dB and 12º, respectively. However, the gain mismatch can reach 5.5 dB at 35 GHz. The measurements of the 1-dB power compression points ($P1dB_{21}$ and $P1dB_{31}$) and the input referred third order intercept points ($IIP3_{21}$ and $IIP3_{31}$) for both channels for the frequency range of 22-35 GHz are shown in Fig. 3.34. P1dB and IIP3 higher than -14.8 and -6dBm across 22-35 GHz are achieved for both channels, respectively. The performance of the proposed wideband

balun-LNA is shown in Table 3.6 in comparison with other LNA designs operating in the same frequency spectrum. These results confirm that the balun-LNA exhibits good differential property, high power gain, low noise figure, very competitive linearity, and the lowest power consumption in the *K/Ka*-band of operation.

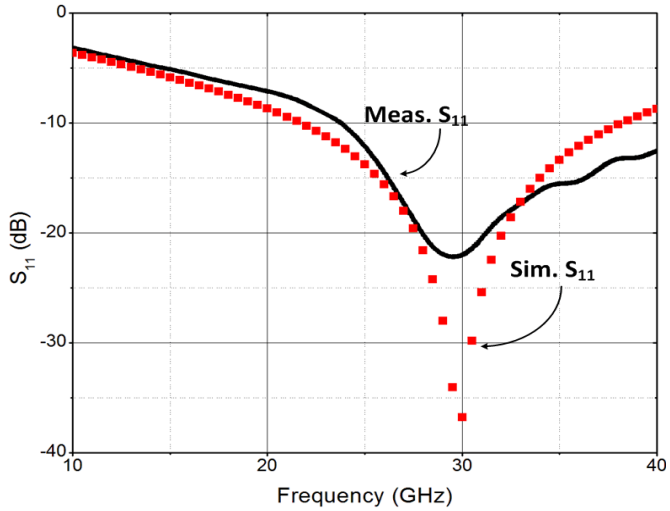

Fig. 3.28 Measured and simulated S11 of the proposed balun-LNA.

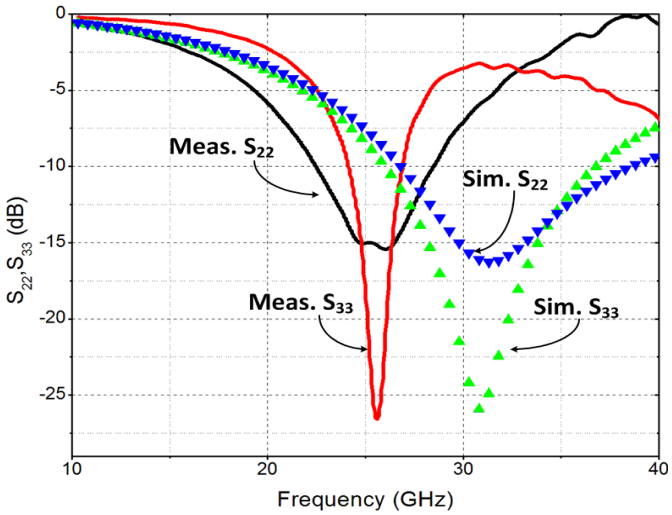

Fig. 3.29 Measured and simulated S22 and S33 of the proposed balun-LNA.

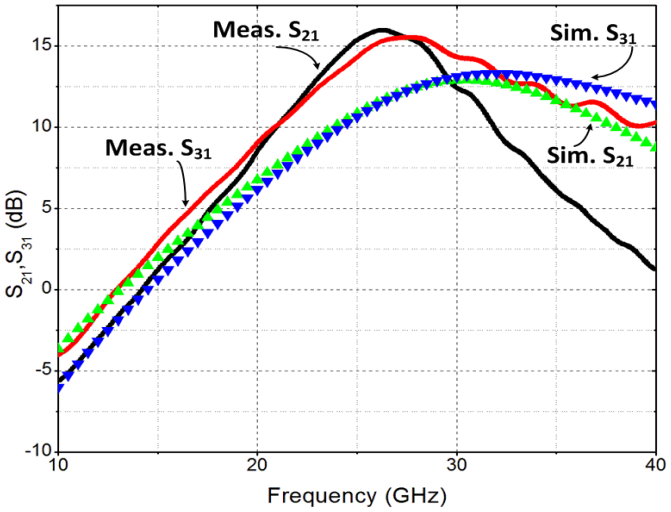

Fig. 3.30 Measured and simulated S21 and S31 for the balun-LNA.

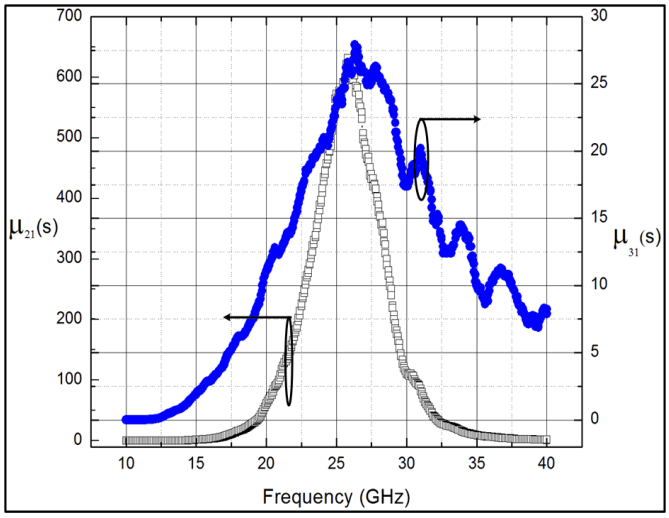

Fig. 3.31 Stability factor of the proposed balun-LNA.

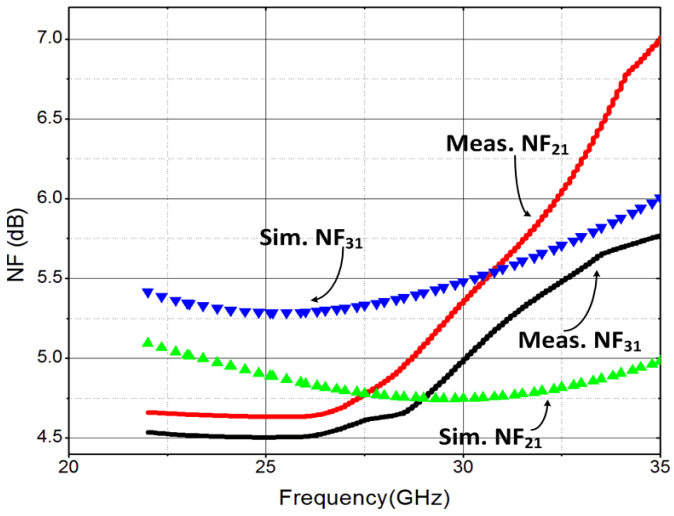

Fig. 3.32 Measured and simulated noise figures of the proposed balun-LNA.

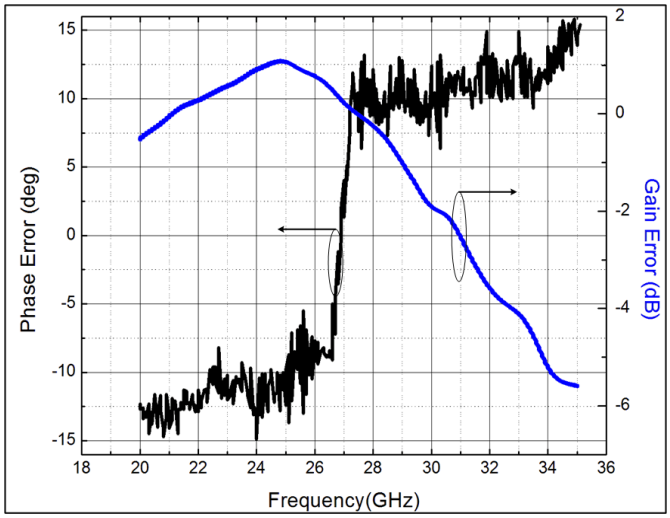

Fig. 3.33 Measured gain and phase mismatches.

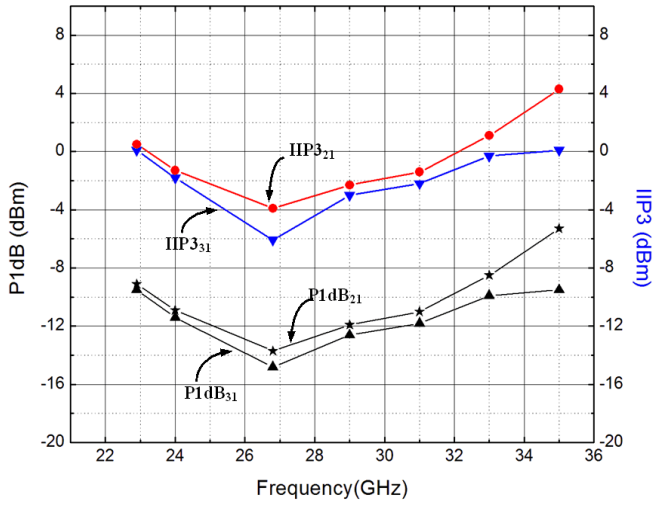

Fig. 3.34 Measured P1dB and IIP3 for the proposed balun-LNA.

Table 3.6 Proposed Balun-LNA comparison to existing balun/LNA designs

Ref.	Topology LNA/Balun	Gain (dB)	Freq Range (GHz)	NF (dB)	P_{1dB} (dB_m)	IIP_3 (dB_m)	S_{11} (dB)	P_{DC} (mA)	Imbalance gain/Phase
[40]	Yes/Yes	6.3/6.7*	20.5	4.9/5.9	0	9	-16.9	14	0.4/39
[55]	Yes/No	8.9	23-27.5	6.93-8	-10.2	2.8	<-14	30	NA
[56]	Yes/No	18	22-29	4.5-6	NA	NA	<-15	8.4	NA
[48]	Yes/No	12*	23-32	4.5-6.3	NA	-6.5	<-12	8.7	NA
[57]	No/Yes	-10	20-30	10	5	NA	<-6.1	48.5	1.8/20
[58]	No/Yes	1	2-40	NA	-6	NA	>-5	31	1/20
This Work	**Yes/Yes**	**15.6/ 15.4**	**22-35**	**4.5-5.8/ 4.6-7.09**	**-13.7/- 14.8**	**-3.9/-6**	**<-8.7**	**5**	**1.8/12 @ 20-30 GHz**

CHAPTER IV

A HIGHLY LINEAR MULTI-STAGES ACTIVE BALUN-LNA WITH DISTRIBUTED FEED-FORWARD AVERAGING RECYCLES CORRECTION TECHNIQUE

4.1 Introduction

Receivers' RF front-ends with differential input ports rely heavily on balun-LNA (single input to differential outputs) to interface with a single port antenna. Various balun design configurations are available from passive to active types. At millimeter wave (mm-wave) frequencies, broadband passive balun tends to suffer from high insertion loss due to limited quality factor on chip and have greater impact on the total receiver's system noise figure. For that reasons, active balun-LNA structures gained popularity due its differential gain benefits, common mode noise cancellation, and second order intermodulation rejections [38]-[41], [46],[55]-[60]. Active balun-LNAs' are classified under 2 frequency domain modes of operation : a) the low frequency balun-LNA type based on noise cancellation structure mainly known as common-gate common-source (CG-CS) approach and its derivatives [38]-[41], [46]; b) millimeter wave designs related to parasitic compensation techniques to alleviate the amplitude and phase errors [55]-[60]. The former approach works well to provide differential outputs at low frequency up to 6 GHz where parasitics are less pronounced. However, in the latter design methods the unequal capacitive coupling parasitics associated with asymmetric signal paths from input to outputs which is mainly due to unbalanced balun-LNA design

structures at millimeter-wave (mm-wave) frequency play a major role in amplitude and phase error variations from the ideal differential conditions. Consequently, various techniques are implemented particularly to resolve the imbalance amplitude and phase dilemmas related to parasitic through neutralization of the junction capacitance at the gate-drain (C_{gd}) and gate-source capacitance (C_{gs}) [58], [60]. In addition, some works in literature propose variations in the output differential loads to compensate for the signal parasitic losses from input to outputs [58]. Such optimization technique only works for narrow band frequency approaches and suffers from amplitude and phase errors as the bandwidth requirement increases.

The proposed distributed feed-forward phase and amplitude averaging recycle correction technique is neither parasitic signal paths dependent nor adherent to any frequency dependent compensation techniques. The averaging recycle correction technique is frequency independent and can minimize the amplitude and phase errors through balanced loads at the differential outputs. Furthermore, the proposed distributed design correction technique can realize successive amplitude and phase calibrations through multi-iteration steps for the active balun-LNA operating at mm-wave frequency. Additionally, the multi-stages active balun-LNA operates in current mode due to low second stage input impedance based on Gilbert class AB gm cell transconductance [67], thus no RF voltage amplification and system linearity is preserved. Note the importance of electromagnetic (EM) simulations to account for all parasitics from input to outputs in the design of active balun-LNA at mm-wave frequency so any compensation techniques can be effective in mitigating the phase and amplitude errors.

4.2 Distributed Feed-Forward Averaging Recycles Correction Technique

Fig. 4.35 shows various conventional balun-LNA structures. These circuit structures experience amplitude and phase imbalances due to asymmetrical signal paths between the input and differential outputs. Furthermore, the baluns' –LNA signal paths exhibit unequal capacitive coupled parasitics to the substrate, hence the gain and phase errors. To alleviate this dilemma, a proposed distributed feed-forward averaging recycles amplitude and phase imbalances correction technique is addressed and analyzed in the following section.

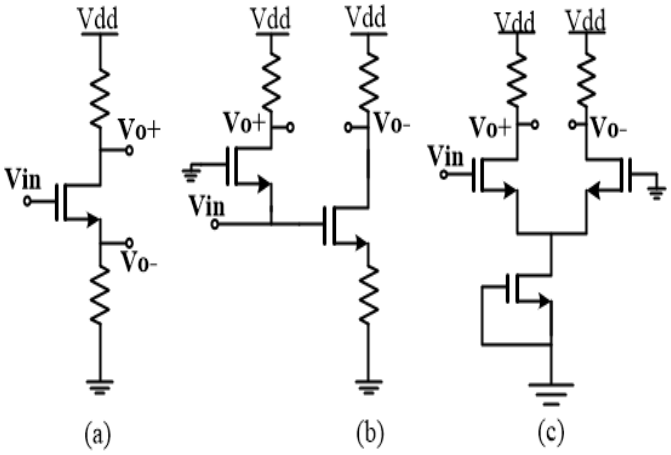

Fig. 4.35 Conventional balun-LNA structures.

4.2.1 Main Idea

Baluns'-LNA circuits are inherently asymmetric structures as shown in Figs. 4.35a, 4.35b, and 4.35c. The signal paths between the input and the differential outputs are unequal and prone to unmatched parasitic capacitances particularly at the signals node splitting. At mm-wave frequency, the impedance at the signals node splitting junction into each signal path is dominated by unequal parasitic capacitances, hence the

gain and phase errors even under balanced outputs loads. Although various passive compensated calibration techniques were in place to correct for the gain and phase imbalances, the process, voltage, and temperature (PVT) and mm-wave gradient process variations prove its ineffectiveness particularly for broadband operation [57]-[60].

The proposed distributed feed-forward averaging recycles amplitude and phase error correction technique is insensitive to unequal signal paths parasitic capacitances and hence the frequency independent type of behavior. The multi-stages feed-forward averaging recycles technique iteratively correct for the amplitude and phase errors by translating the average residues errors within the circuit stages into the same phase delay and equal amplitude variation at each output path. The distributed averaging technique establishes a built-in gain and phase errors calibration without relying on passive compensation techniques [60].

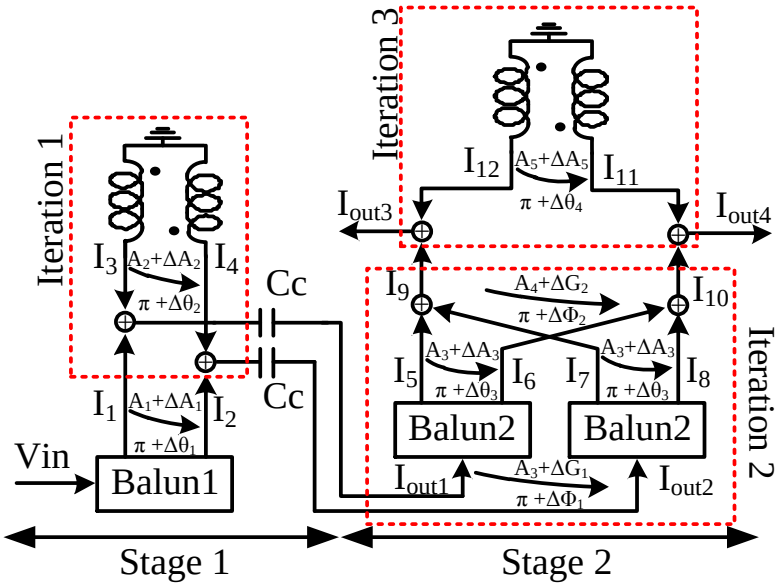

Fig. 4.36 Proposed balun-LNA architecture with distributed averaging correction technique.

Fig. 4.36 shows the conceptual system level diagram of the proposed multi-stages distributed feed-forward averaging recycles amplitude and phase errors correction technique. The system level averaging correction technique consists of two successive active balun-LNAs' stages with 3 residuals' sub-iterations. Stage 1 "Balun1" can consists of any conventional active balun-LNA design structures combined with fully balanced differential load. The fully balanced differential inductor merged with the coupling capacitances, Cc, constitutes the balun-LNA differential load where the first averaging amplitude and phase errors residues are resolved. This process is known as "Iteration1". The current waves traveling thru the differential inductor surface and in each path of the balun-LNA are described as in (4.1) where the amplitude and phase residual errors are, (ΔA_1, ΔA_2, $\Delta\theta_1$, $\Delta\theta_2$), respectively. In addition, K_1 is the coupling coefficient between the differential inductor windings. The current combination of these current waves provides the differential current output as in (4.2). The first stage balun-LNA amplitude and phase imbalances errors, (ΔG_1, $\Delta\Phi_1$), are defined in equations (4.3) and (4.4) respectively.

$$\begin{cases} I_1 = A_1 \sin(\omega t) \\ I_2 = -(A_1 + \Delta A_1)\sin(\omega t + \Delta\theta_1) \\ I_3 = A_2 \sin(\omega t) \\ I_4 = (A_2 + \Delta A_2)(1 + K_1)\sin(\omega t + \Delta\theta_2) \end{cases} \tag{4.1}$$

$$I_{Out1} = (I_3 + I_1) = \left[(A_1 + A_2)\sin(\omega t) \right]$$

$$I_{Out2} = (I_2 + I_4) = \begin{bmatrix} (A_2 + \Delta A_2 + A_2K_1 + \Delta A_2K_1 - A_1 - \Delta A_1)\sin\left(\omega t + \frac{\Delta\theta_1 + \Delta\theta_2}{2}\right)\cos\left(\frac{\Delta\theta_2 - \Delta\theta_1}{2}\right) \\ +(A_2 + \Delta A_2 + A_2K_1 + \Delta A_2K_1 + A_1 + \Delta A_1)\sin\left(\frac{\Delta\theta_2 - \Delta\theta_1}{2}\right)\cos\left(\omega t + \frac{\Delta\theta_1 + \Delta\theta_2}{2}\right) \end{bmatrix} \quad (4.2)$$

$$\begin{aligned} \Delta\Phi_1 &= \angle I_{Out2} - \angle I_{Out1} - 180° \\ &= \tan^{-1}\left(\frac{(A_2 + \Delta A_2 + A_2K_1 + \Delta A_2K_1 + A_1 + \Delta A_1)}{(A_2 + \Delta A_2 + A_2K_1 + \Delta A_2K_1 - A_1 - \Delta A_1)} \tan\left(\frac{\Delta\theta_2 - \Delta\theta_1}{2}\right) \right) \end{aligned} \quad (4.3)$$

$$\Delta G_1 |_{dB} = 20\log\left(\frac{|I_{Out2}|}{|I_{Out1}|} \right) \quad (4.4)$$

Note that from (4.3) the averaged residual phase error is amplitude dependent and may be possible to have $\Delta\Phi_1$ to be zero if $\Delta\theta_1 = \Delta\theta_2$. In case $\Delta\Phi_1$ is not zero, the 180º differential operation can still be performed due to the same phase terms, $\frac{\Delta\theta_1 + \Delta\theta_2}{2}$, in accordance with (4.2). Furthermore, assume the residual phase errors $\Delta\theta_1$ and $\Delta\theta_2$ are zeros; the amplitude error, ΔG_1, is limited to $20\log\left| \left(\frac{(A_2 + \Delta A_2 + A_2K_1 + \Delta A_2K_1 - A_1 - \Delta A_1)}{A_1 + A_2} \right) \right|$ according to (4.4).

In the second stage balun-LNA, the feed-forward averaging recycles amplitude and phase correction technique is designed based on two identical parallel active balun-LNAs' structures as depicted in Fig. 4.36. The averaging recycles correction technique

assumes an equal amplitude and phase residual errors split, (ΔA_3, $\Delta\theta_3$), between the two balun-LNAs'. The current flowing into each path of the active balun-LNAs' can be defined as in (4.5). These currents combination form the differential output currents as labeled in equations (4.6) and (4.7). The second iterative amplitude and phase errors residuals, (ΔG_2, $\Delta\Phi_2$), are defined in equations (4.8) and (4.9) respectively.

$$\begin{cases} I_5 = A_3 \sin \omega t \\ I_6 = -\left(A_3 + \Delta A_3\right)\sin\left(\omega t + \Delta\theta_3\right) \\ I_7 = -\left(A_3 + \Delta G_1 + \Delta A_3\right)\sin\left(\omega t + \Delta\theta_3 + \Delta\Phi_1\right) \\ I_8 = \left(A_3 + \Delta G_1\right)\sin\left(\omega t + \Delta\Phi_1\right) \end{cases} \tag{4.5}$$

$$I_9 = I_7 + I_5 = \begin{bmatrix} -\left(\Delta A_3 + \Delta G_1\right)\times\sin\left(\omega t + \dfrac{\Delta\theta_3 + \Delta\Phi_1}{2}\right)\cos\left(\dfrac{\Delta\theta_3 + \Delta\Phi_1}{2}\right) \\ -\left(2A_3 + \Delta A_3 + \Delta G_1\right)\times\sin\left(\dfrac{\Delta\theta_3 + \Delta\Phi_1}{2}\right)\cos\left(\omega t + \dfrac{\Delta\theta_3 + \Delta\Phi_1}{2}\right) \end{bmatrix} \tag{4.6}$$

$$I_{10} = I_6 + I_8 = \begin{bmatrix} \left(-\Delta A_3 + \Delta G_1\right)\times\sin\left(\omega t + \dfrac{\Delta\theta_3 + \Delta\Phi_1}{2}\right)\cos\left(\dfrac{\Delta\theta_3 - \Delta\Phi_1}{2}\right) \\ -\left(2A_3 + \Delta A_3 + \Delta G_1\right)\times\sin\left(\dfrac{\Delta\theta_3 - \Delta\Phi_1}{2}\right)\cos\left(\omega t + \dfrac{\Delta\theta_2 + \Delta\Phi_1}{2}\right) \end{bmatrix} \tag{4.7}$$

$$\Delta\Phi_2 = \angle I_{10} - \angle I_9 - 180°$$
$$= \begin{bmatrix} \tan^{-1}\left(\dfrac{-\left(\Delta A_3 + 2A_3 + \Delta G_1\right)}{\left(-\Delta A_3 + \Delta G_1\right)} \tan\left(\dfrac{\Delta\theta_3 - \Delta\Phi_1}{2} \right) \right) \\ -\tan^{-1}\left(\dfrac{\left(\Delta A_3 + 2A_3 + \Delta G_1\right)}{\left(\Delta A_3 + \Delta G_1\right)} \times \tan\left(\dfrac{\Delta\theta_3 + \Delta\Phi_1}{2} \right) \right) \end{bmatrix} \tag{4.8}$$

$$\Delta G_2 \,|_{dB} = 20\log\left(\left| \frac{I_{10}}{I_9} \right| \right) \tag{4.9}$$

Assume in (4.8) that the amplitude coefficients ratios for both tangents functions are equals where orthogonal terms in (4.6) and (4.7) are nulled; $\Delta\Phi_2$ can be cancelled completely. Through the second iteration averaging recycles correction technique; a perfect phase calibration can be achieved without passive lumped elements compensation. However, the orthogonally terms introduced in (4.6) and (4.7) are mainly due to amplitude error in each balun-LNA and force small phase variation. Even if the phase error $\Delta\Phi_2$ is not zero, the differential operation of 180º can still be maintained due to the same output phase term in each balun-LNA when orthogonal terms are not set to zeros in (4.6) and (4.7). It is important to note that the first averaged residual phase error, $\Delta\Phi_1$, is being averaged for the second time under the second iterative process.

Finally, the third iteration is established through another differential load inductor at the outputs of the two identical balun-LNAs'. Intuitively, the amplitude and phase errors are $\frac{1}{2^n}$ smaller compared to the original differential signals errors before the first averaging iteration takes place where *n* is the order of the entire distributed network of iterations. The analytical work is similar to the previous two residuals iterations

analyses. Equations (10)-(13) show the final amplitude and phase residual errors outputs defined as (ΔG_3, $\Delta\Phi_3$), after the third iteration.

$$\begin{cases} I_9 = A_4 \sin \omega t \\ I_{10} = -\left(A_4 + \Delta G_2\right)\sin\left(\omega t + \Delta\Phi_2\right) \\ I_{11} = \left(A_5 + \Delta A_5\right)\left(1 + K_2\right)\sin\left(\omega t + \Delta\theta_4\right) \\ I_{12} = A_5 \sin \omega t \end{cases} \tag{4.10}$$

$$I_{Out3} = I_9 + I_{12} = \left[\left(A_4 + A_5\right)\sin\left(\omega t\right)\right] \tag{4.11}$$

$$I_{Out4} = I_{10} + I_{11} = \begin{bmatrix} \left[\left(A_5 + \Delta A_5\right)\left(1 + K_2\right) - \left(A_4 + \Delta G_2\right)\right]\sin\left(\omega t + \dfrac{\Delta\Phi_2 + \Delta\theta_4}{2}\right)\cos\left(\dfrac{\Delta\theta_4 - \Delta\Phi_2}{2}\right) \\ + \left[\left(A_5 + \Delta A_5\right)\left(1 + K_2\right) + \left(A_4 + \Delta G_2\right)\right]\sin\left(\dfrac{\Delta\theta_4 - \Delta\Phi_2}{2}\right)\cos\left(\omega t + \dfrac{\Delta\Phi_2 + \Delta\theta_4}{2}\right) \end{bmatrix} \tag{4.12}$$

$$\begin{aligned} \Delta\Phi_3 &= \angle I_{Out4} - \angle I_{Out3} - 180° \\ &= \tan^{-1}\left(\frac{\left[\left(A_5 + \Delta A_5\right)\left(1 + K_2\right) + \left(A_4 + \Delta G_2\right)\right]}{\left[\left(A_5 + \Delta A_5\right)\left(1 + K_2\right) - \left(A_4 + \Delta G_2\right)\right]}\tan\left(\frac{\Delta\theta_4 - \Delta\Phi_2}{2}\right)\right) \end{aligned} \tag{4.13}$$

$$\Delta G_3\,|_{dB} = 20\log\left(\frac{\left|I_{Out4}\right|}{\left|I_{Out3}\right|}\right) \tag{4.14}$$

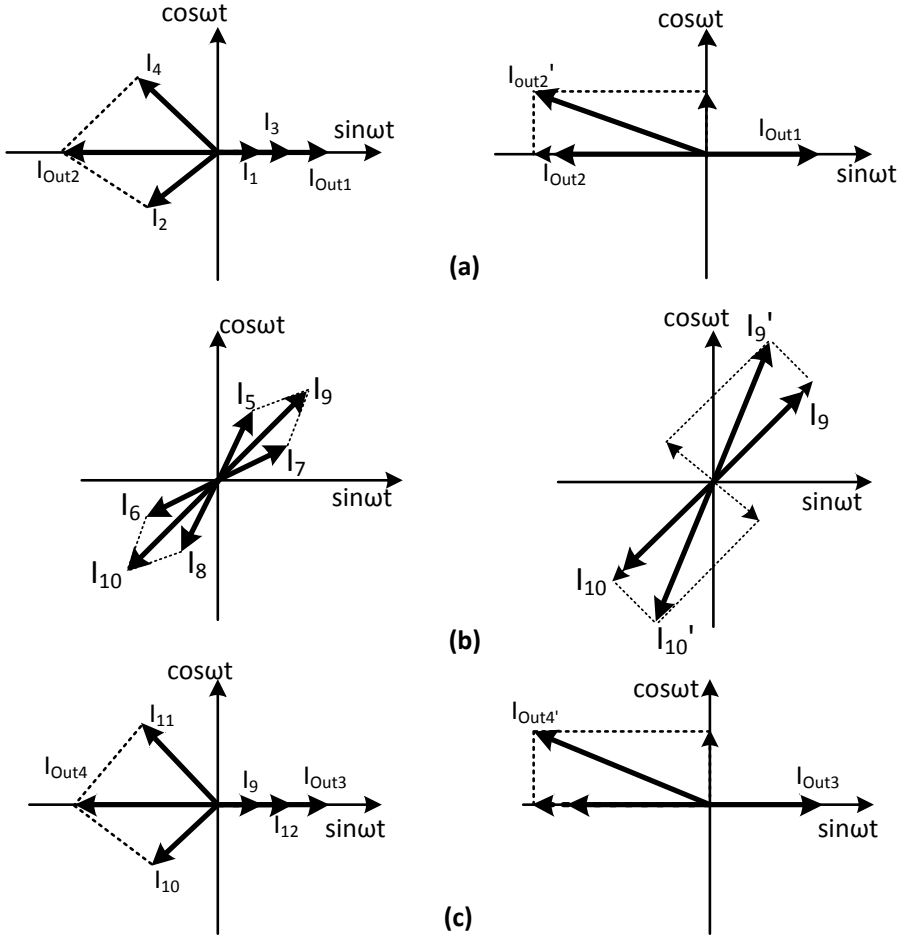

Fig. 4.37 Vector magnitude representation of the averaging recycles correction technique (a) output iteration 1 with and without orthogonal terms (b) output iteration 2 with and without orthogonal terms (c) output iteration 3 with and without orthogonal terms.

To illustrate the averaging recycles correction technique concept, the currents equations can be translated into vectors with magnitudes and polar phase coordinates as shown in Fig. 4.37. The vector currents I_1 through I_4 encompass the differential current of the first stage balun-LNA. Fig. 4.37a shows the orthogonal term effects from amplitude error in (4.2) that limits the averaging phase error correction. The vector combinations, I_{out1} and I_{out2}, are formulated through the vector sums of I_1, I_3, and I_2, I_4,

respectively. Consequently, the current vectors I_9 and I_{10} are generated through vector summations I_5 to I_8. Fig. 4.37b shows the perfect phase error cancellation when the orthogonal terms of equations (4.6) and (4.7) are zeros. According to (4.8), $\Delta\Phi_2$ can be zero even if $\Delta\Phi_1$ and $\Delta\theta_1$ are not. Furthermore, Fig. 4.37c shows the vector currents I_{out3} and I_{out4} after the third averaging iteration due to the differential load inductor.

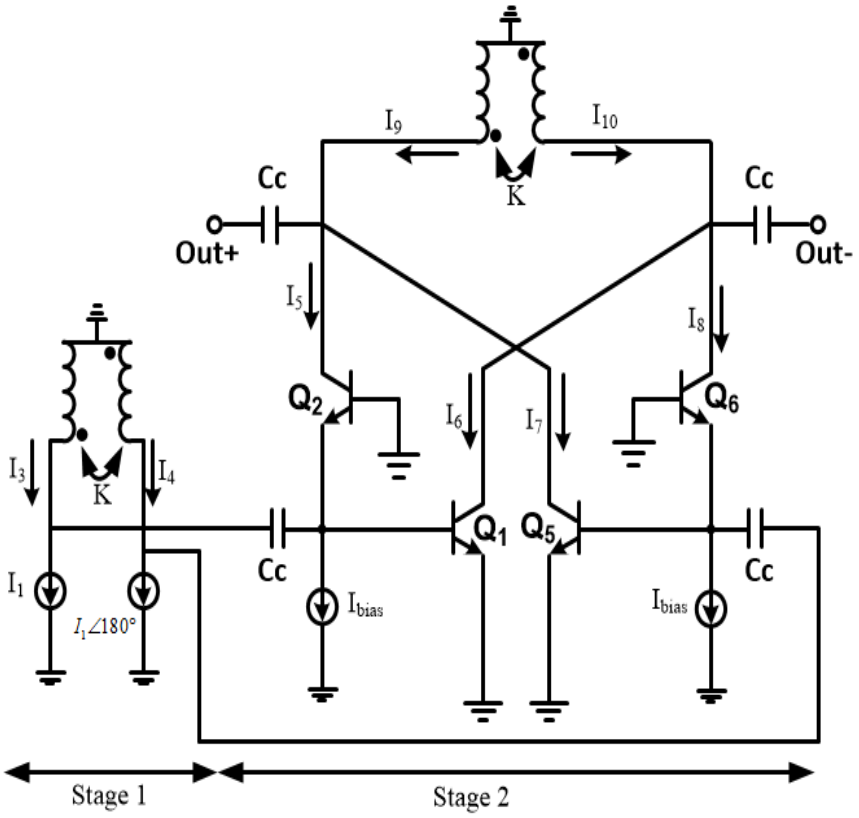

Fig. 4.38 Transistor model of the multi-stages balun-LNA.

The mathematical analysis is verified compared to the 2 stages active balun-LNA transistor level model. Fig. 4.38 shows the 2 stages balun-LNA model. The first stage balun-LNA consists of variable RF current sources with a differential output load

inductor. The two identical balun-LNAs are modeled using HBT transistors, Q_1 to Q_6, similar to Gilbert gm cell transconductance [67]. Consequently, the two identical gm cells are terminated with a differential load inductor which is used as the third iteration to resolve further the amplitude and phase residuals. The simulations demonstrate that for an amplitude error of ± 2 dB and phase error of ±25º injected into the first stage balun-LNA; the amplitude and phase residuals from one iteration to another are tested to demonstrate rectification. Simultaneously, the mathematical analyses strongly agree with the reported results from the model simulations to prove that the distributed averaging recycles amplitude and phase errors correction technique works.

4.2.2 Active and Passive Devices Mismatches

To evaluate the practical performance of the proposed balun-LNA with distributed network averaging recycles correction technique, circuit mismatches need to be considered to account for gradient process variations. A σ variance is specified in the simulator circuit design model to emulate actual physical variations on active and passive devices. Both differential loads inductors are mismatched by 20% from their center taps. Furthermore, each stage of the balun-LNA exhibits a 20% increase in the active device emitters' areas compared to its original counterpart design model. Fig. 4.39 shows the proposed model architecture where active and passive devices mismatches parameters are included. The simulations of the outputs amplitude and phase errors are limited to less than 4º and 1 dB, respectively. Ultimately, the distributed averaging network correction technique is bit degraded when mismatches are considered

compared to the previous results. However, the robustness of the proposed technique to suppress the gain and phase errors even in the presence of mismatches proves that the performance of the mm-wave broadband balun-LNA is still intact.

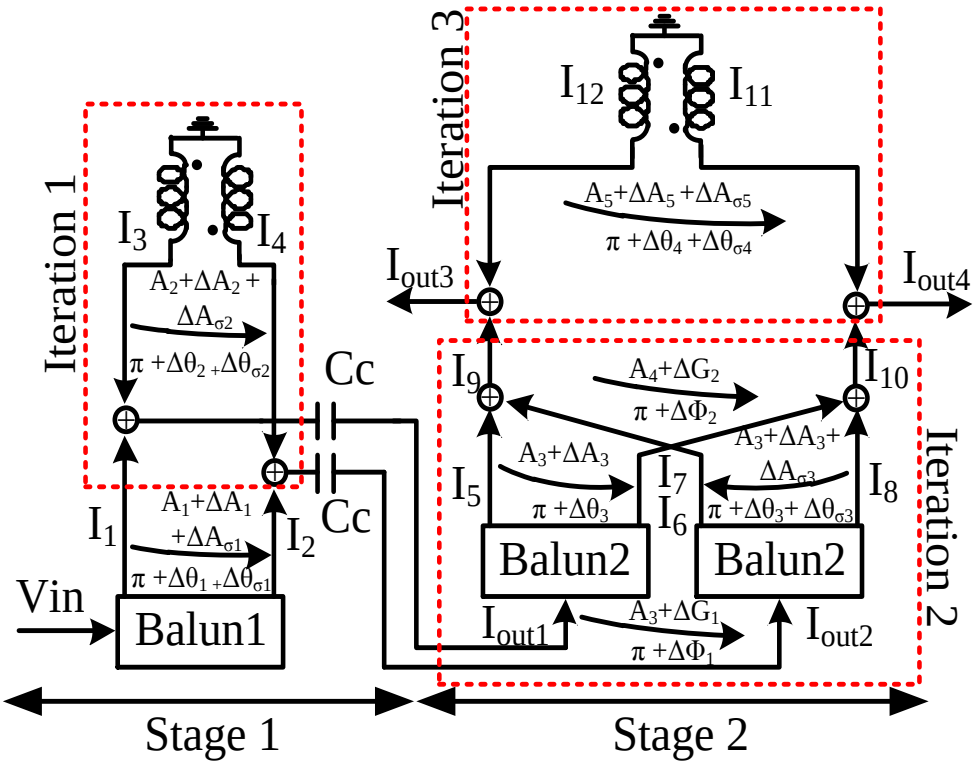

Fig. 4.39 Proposed model architecture of the multi-stages balun-LNA including active and passive mismatches parameters.

The impact of the circuit mismatches can also be represented into the mathematical model analyses derived previously. The variance parameters of amplitude and phase errors due to active and passive device mismatches are defined as $(\Delta A_{\sigma n}, \Delta\theta_{\sigma n})$, respectively. The mismatch model variance σn for $n = 1, 2, 3\ldots$ is assigned to each resolved stage of residual iteration. Equations (4.15)-(4.17) present the newly added

mismatch non-idealities into the mathematical derivations. These non-idealities slightly deteriorate the performances of the balun-LNA. The benefits of the multi-stages distributed averaging correction technique limit the mismatches impact on the output amplitude and phase errors. This suggests that the mismatches are not directly reflected on the outputs and the averaging correction technique helps maintain the balun-LNA characteristics at mm-wave frequency.

$$\begin{aligned}\Delta\Phi_{1/\sigma n} &= \angle I_{Out2/\sigma n} - \angle I_{Out1/\sigma n} - 180^\circ \\ &= \tan^{-1}\left(\begin{array}{l}\left[\dfrac{\left(A_2+\Delta A_2+\Delta A_{\sigma 2}+A_2K_1+\Delta A_2K_1+A_1+\Delta A_1+\Delta A_{\sigma 1}\right)}{\left(A_2+\Delta A_2+\Delta A_{\sigma 2}+A_2K_1+\Delta A_2K_1-A_1-\Delta A_1-\Delta A_{\sigma 1}\right)}\right] \\ \times\tan\left(\dfrac{\Delta\theta_2+\Delta\theta_{\sigma 2}-\Delta\theta_1-\Delta\theta_{\sigma 1}}{2}\right)\end{array}\right)\end{aligned} \tag{4.15}$$

$$\begin{aligned}\Delta\Phi_{2/\sigma n} &= \angle I_{10/\sigma n} - \angle I_{9/\sigma n} - 180^\circ \\ &= \left[\begin{array}{l}\tan^{-1}\left(\dfrac{-\left(\Delta A_3+2A_3+\Delta G_1\right)}{\left(-\Delta A_3+\Delta G_1\right)}\tan\left(\dfrac{\Delta\theta_3-\Delta\Phi_1}{2}\right)\right) \\ -\tan^{-1}\left(\dfrac{\left(\Delta A_3+\Delta A_{\sigma 3}+2A_3+\Delta G_1\right)}{\left(\Delta A_{\sigma 3}+\Delta A_3+\Delta G_1\right)}\times\tan\left(\dfrac{\Delta\theta_3+\Delta\Phi_1}{2}+\dfrac{\Delta\theta_{\sigma 3}}{2}\right)\right)\end{array}\right]\end{aligned} \tag{4.16}$$

$$\begin{aligned}\Delta\Phi_{3/\sigma n} &= \angle I_{Out4/\sigma n} - \angle I_{Out3/\sigma n} - 180^\circ \\ &= \tan^{-1}\left(\begin{array}{l}\dfrac{\left[\left(A_5+\Delta A_5+\Delta A_{\sigma 5}\right)\left(1+K_2\right)+\left(A_4+\Delta G_2\right)\right]}{\left[\left(A_5+\Delta A_5+\Delta A_{\sigma 5}\right)\left(1+K_2\right)-\left(A_4+\Delta G_2\right)\right]} \\ \times\tan\left(\dfrac{\Delta\theta_4+\Delta\theta_{\sigma 4}-\Delta\Phi_2}{2}\right)\end{array}\right)\end{aligned} \tag{4.17}$$

4.2.3 Linearity

The linearity associated with the multi-stages balun-LNA is based on the analysis shown in chapter V. Generally speaking, in a receiver system with multiple gain stages the linearity of the second gain stage is the bottleneck of the entire system. For this reason, we implemented a class AB gm cell transconductance to overcome this limitation. Furthermore, the input impedance into the class AB gm cell is very low over the entire system broadband operation, hence no RF voltage gain which in turn provides very low distortion. The multi-stages balun-LNA operates in current mode; hence the system linearity is preserved.

4.3 Circuit Implementation

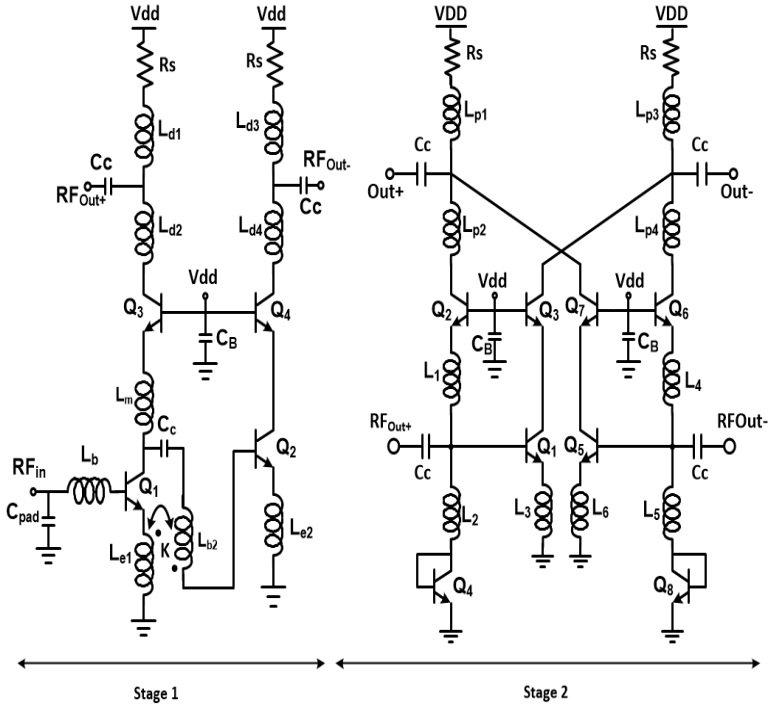

Fig. 4.40 Proposed multi-stages balun-LNA circuit implementation

Fig. 4.40 shows the circuit schematic of the proposed multi-stages balun-LNA where circuits biasing are not shown for simplicity. Stage 1 consists of common emitter design structure AC coupled to an auxiliary common emitter path with AC coupled stacked transformer for power saving. The detailed design tradeoffs and structure analyses are reported in [65] and chapter III. Note that the differential load is fully balanced with equally single balanced inductors in each output path. The reason for this approach instead of differential inductor at the output is to preserve the gain without sacrificing the performance of iteration 1 of the recycles averaging correction technique. Furthermore, stage 2 consists of two identical balun-LNAs' structures with low input impedances; hence the system linearity is maintained. Each balun-LNA path employs a current buffer in parallel to a common source structure with beta helper current source. For a positive or negative excursion, the common source structure on one end with the current buffer from the 180 out of phase second balun-LNA structure are added in phase at the output to produce the second iteration for amplitude and phase errors recycles averaging correction technique. Note that the calibration happens within the built-in circuits without the need for passive lumped elements for compensation or neutralization of the capacitive parasitic. In addition, a fully balanced differential load is used at the output of the second stage where iteration 3 is deployed to refine further the amplitude and phase residual errors. A single balanced inductor in each path is used instead of differential one for gain purposes as well similar to stage 1. Note, all inductors designs are simulated using IE3D electromagnetic simulator to account for all interconnects resistive losses, and capacitive coupling parastics to the substrate. The design of each

inductor is based on coplanar waveguide (CPW) structure where a bit lower inductor quality factor is sacrificed for higher self-resonance. The simulations of the proposed broadband design show effective amplitude and phase errors correction based on distributed recycles averaging correction technique from 10-50 GHz with gain and phase mismatches less than 0.7 dB and 2.8 degree, respectively.

4.4 Simulations and Measurements

The power gain results of the proposed multi-stages balun-LNA with recycles amplitude and phase errors correction technique are reported in Fig. 4.41. The 3-dB bandwidth of the proposed balun-LNA architecture is 21-45 GHz with 17.4 dB as maximum power gain for both channels (S_{21}, S_{31}), respectively. Furthermore, the broadband balun functional design structure can work from 10-50 GHz with very low amplitude and phase errors. Fig. 4.41 and Fig. 4.43 show amplitude and phase mismatches less 0.7 dB and 2.86°, respectively. Fig. 4.42 shows the noise figure results of both balun-LNA channels, S_{21} and S_{31}, where NF_{21} and NF_{31} are 4.4-4.9 dB and 5.8-6.4 dB, respectively. Note the importance of maintaining fully balanced differential operation for the proposed balun-LNA, hence the common mode noise cancellation is very high. The differential noise figure matches well with the minimum noise figure NF_{min}. Fig. 4.44 addresses the 1 dB input referred gain compression. The $P_{in}1dBs$' for both channels are better than -15.6 dBm across the entire bandwidth of interest. The estimated input referred third order intermodulation IIP_3 for both channels is better than -2.6 dB across the frequency range 21-45 GHz. Fig. 4.45 shows the die micrograph of

the proposed balun-LNA architecture with active area 1mm x 1.2 mm including RF and DC bias pads. The performance of the proposed broadband multi-stages balun-LNA is shown in Table 4.7 in comparison with other existing balun-LNA designs operating in the same frequency spectrum 21-45 GHz and 10-50 GHz. These results confirm that the balun-LNA exhibits excellent differential properties, high power gain, low noise figure, very high linearity, and very competitive power consumption in the *K/Ka- and V* bands of operation. The total power consumption is less than 28.8mW drawn from 1.8V power supply using 0.18 µm SiGe BiCMOS technology from Jazz semiconductor.

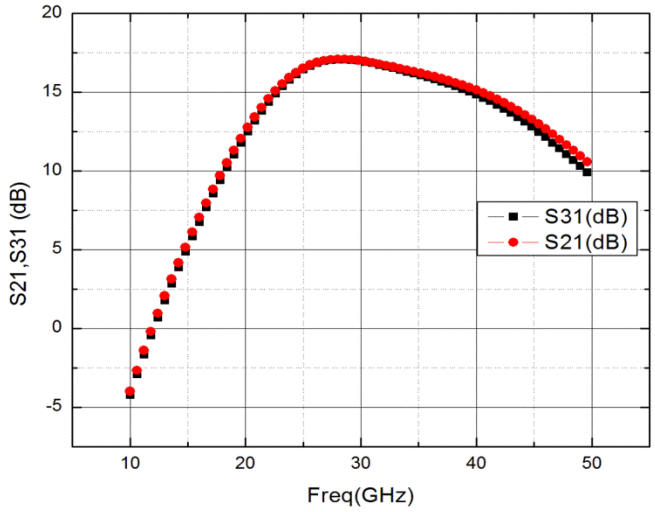

Fig. 4.41 S21, and S31 power gains of the proposed multi-stages balun-LNA.

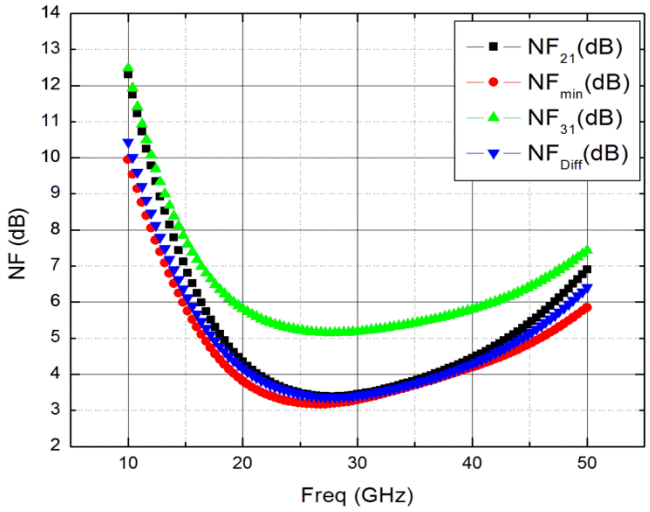

Fig. 4.42 Noise figure simulations of the proposed multi-stages balun-LNA.

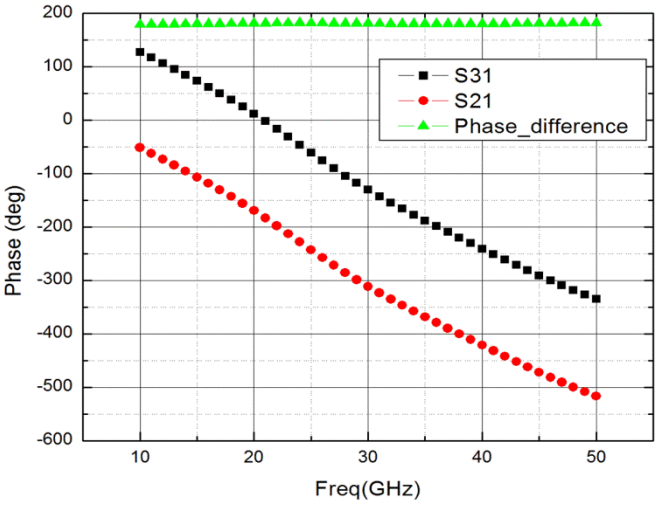

Fig. 4.43 Phase balance and phase difference of the proposed multi-stages balun-LNA.

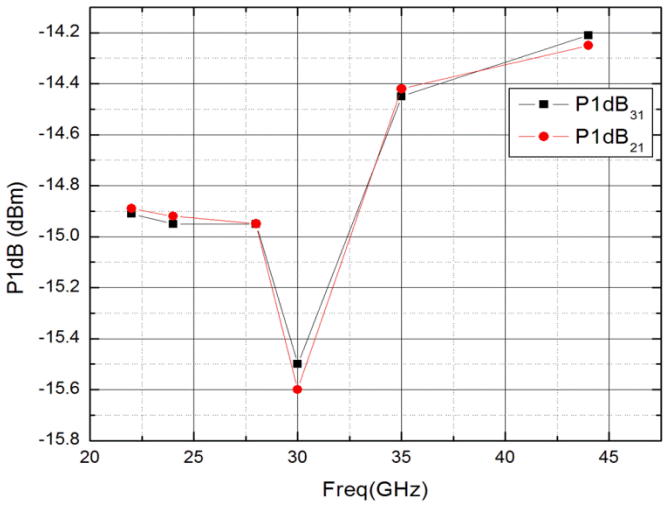

Fig. 4.44 Input referred 1 dB gain compression of the proposed multi-stages balun-LNA.

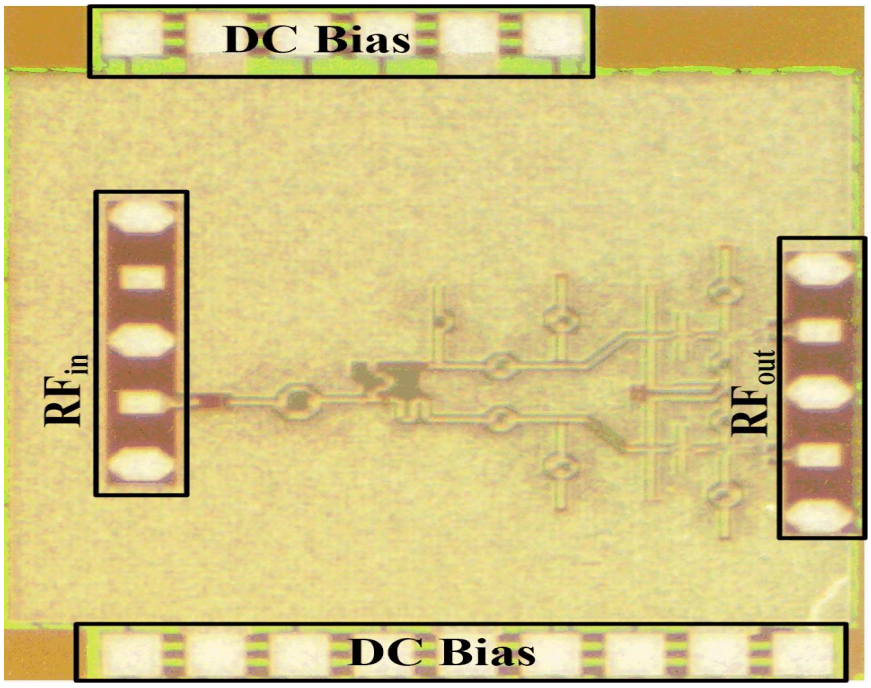

Fig. 4.45 Micrograph die of the proposed multi-stages balun-LNA

Table 4.7 Proposed multi-stages balun-LNA comparison to existing designs

Ref.	Topology LNA/Balun	Gain (dB)	Freq Range (GHz)	NF (dB)	P_{1dB} (dB_m)	IIP_3 (dB_m)	S_{11} (dB)	P_{DC} (mA)	Imbalance gain/Phase
[40]	Yes/Yes	6.3/6.7*	20.5	4.9/5.9	0	9	-16.9	14	0.4/39
[55]	Yes/No	8.9	23-27.5	6.93-8	-10.2	2.8	<-14	30	NA
[56]	Yes/No	18	22-29	4.5-6	NA	NA	<-15	8.4	NA
[48]	Yes/No	12*	23-32	4.5-6.3	NA	-6.5	<-12	8.7	NA
[57]	No/Yes	-10	20-30	10	5	NA	<-6.1	48.5	1.8/20
[58]	No/Yes	1	2-40	NA	-6	NA	>-5	31	1/20
[68]	Yes/Yes	10/8.5	60-67	8.6	-16.6	-7	<-10	13.6	1.7/10
[69]	Yes/Yes	4	>60	N/A	-2**	N/A	<-10	15	1/10
This Work	**Yes/Yes**	**17.5/ 17.4**	**21-44/ 10-50**	**4.4-4.9/ 6.5-10**	**-15.5/ -15.6**	**-2.6/-2.5**	**<-8.7**	**16**	**0.7/2.86**

CHAPTER V

A 22-44 GHZ MILLIMETER-WAVE COEXISTENT RECEIVER ARCHITECTURE AND CIRCUITS DESIGN

5.1 Proposed Receiver Architecture

A wideband versatile multi-standards multi-bands direct conversion receiver chain for microwave and mm-wave coexistent applications from 22-44 GHz is shown in Fig. 5.46. The receiver architecture consists of a main path; and an auxiliary one dedicated to high power jamming blocker for military unmanned aerial vehicle (UAV) radar application 35-37 GHz. The latter one is designed to have an attenuator first block with linear phase characteristics and is expected to be off chip for less design layout complexity. A receiver signal strength indicator block (RSSI) senses the incoming antenna signal power level and controls path selectivity. The main path consists of a wideband active balun-LNA reported in [65] followed by a low input impedance class AB amplifier. The differential current mode outputs of the two successive gain stages are down-converted by an ac coupled doubly-balanced passive mixers through the correlation of differential In-phase/quadrature signals using quadrature all pass filter (QAP) design fed externally from a differential local oscillator (LO). The cross-correlated current output is converted to voltage using a feed-forward trans-impedance amplifier (TIA) with low input impedance. Furthermore; a feed-forward high-pass polyphase filter provides cancellation mechanism at the output TIA node and immune the receiver from out of band interferers (OBI), blockers, and reduce the effect of in-

band aliasing. Note that the noise contribution of this high-pass polyphase cancellation filter is minimal owing to its low

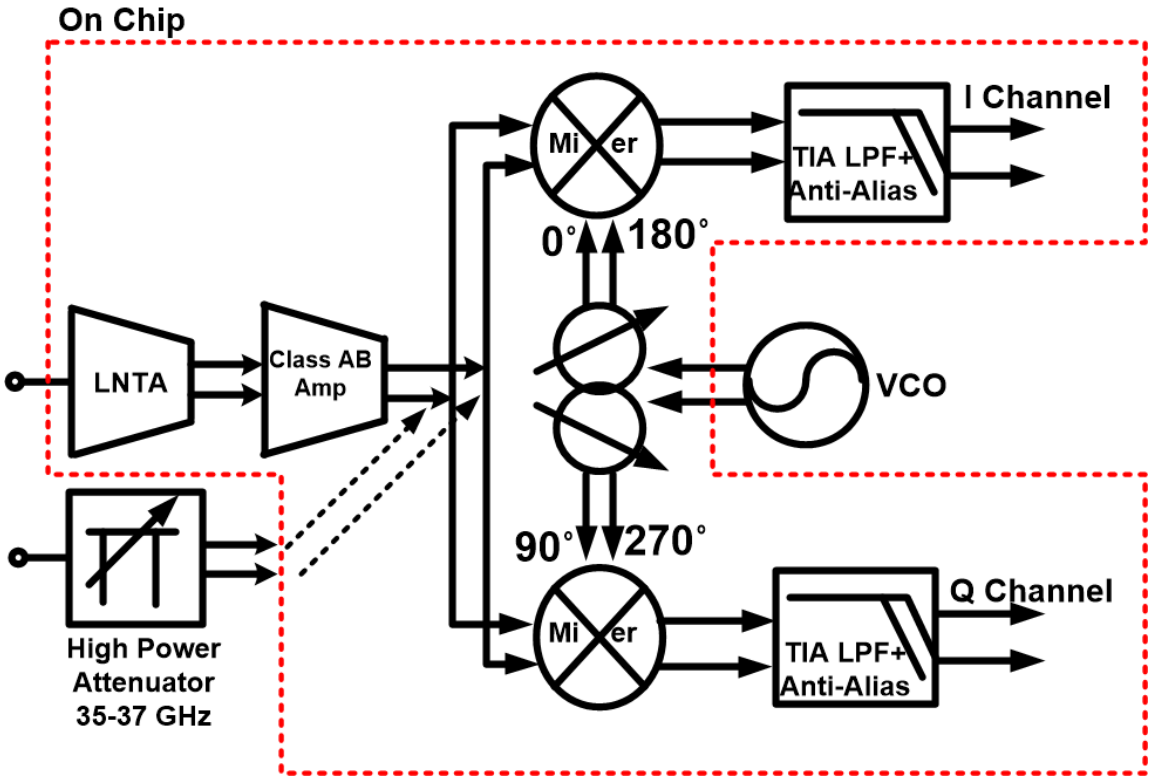

Fig. 5.46 Proposed millimeter-wave coexistent receiver architecture.

gain frequency response in band. This design method increases receiver flexibility and functionality and reduces its dependency on external duplexers and bulky MEMS filter as in [14]. Hence, the bill of materials (BOM) is reduced. The proponents of the proposed receiver architecture including both paths are as follows: *1)* Utilizing current mode amplification in the RF front-end, *no RF voltage gain*. Thus, low noise figure (NF) and high in-band linearity for the RF front-end is maintained. *2)* Class AB amplifier with low input impedance preceded by a highly linear balun-LNA bolsters the current amplification mode without degrading the linearity compared to [37]; [61]; where

regular common source transconductance gm stages are used. *3)* Having successive low input impedance throughout the multi-gain stages of the RF front-end helps preserve the wideband operation across the frequency band of interest, and leads to less distortion in the mixer and the nonlinear output impedances of the multi-gain current mode blocks. Hence, the out of band interferers' (OBI) experience no voltage gain amplifications and the first voltage gain happens only at baseband after the low pass filter, which provides channel filtering selectivity to mitigate the OBI. *4)* The addition of second gain stage amplification alleviates problems associated with using 50% duty cycles control signals for mixers operations where at any point in time in such design approach 2 mixers switches for I/Q channels are turned on simultaneously causing both channels to be short, thus the receiver suffers from *I/Q channels crosstalk*/*interactions* [62]. *5)* Having an active wideband single to differential balun-LNA with asymmetric paths from input to outputs can causes amplitude and phase mismatches due to unequal capacitive parasitics between the two paths. To resolve this dilemma; single to differential passive transformer is being used as part of the matching network for a fully differential LNA [63]-[64]. However, a large insertion loss (< -4 dB) due to passive transformer is inevitable hence, the noise figure is degraded. The alternative approach is placing a differential class AB gain stage after the balun- LNA to improve the common mode rejection through a fully balanced differential output load, and cancel any amplitude and phase mismatches due to unequal capacitive parasitic paths between the input and the outputs without linearity limitation. Furthermore; the class AB amplifier has built in amplitude and phase mismatches cancellation scheme independent of frequency where

no passive lumped elements are required for compensation. The architectural design advantages for this mm-wave receiver are ubiquitous. A more detailed analysis of these benefits will be addressed in the next section on the circuit implementation level.

5.2 Circuits Implementation

5.2.1 Balun-LNA

A single to differential highly linear active wideband balun-LNA is designed to amplify the signal in the frequency range 22-44 GHz. The active balun-LNA structure stems from similar design approach addressed in chapter III. The proposed active wideband balun-LNA architecture is shown in Fig. 5.47 and all components values are reported in table 5.1 [65]. Table 5.8 lists all design parameters of the acive balun-LNA including the transistors Q_1, Q_2, Q_3, and Q_4 emitters' area defined as $WxL_{Q1,2,3,4}$.The architecture of the active balun-LNA has a wideband input matching network consisting of base inductance; L_b; ac coupled transformer between L_{e1} and L_{b2} , and coupling parasitic capacitances to the substrate as losses. The input matching response behavior is dependent on the coupling coefficient; *K*; and the turn ratios between the transformer windings. A resonance frequency shift is adjusted with the base inductance L_b. A wideband performance is maintained due to low quality factor of the matching network through its poles and zeros cancellations. Yet, each inductor must have a high quality factor with high self-resonance frequency (SRF) to keep the noise figure low. It is important for an inductor design to have not only high quality factor, but also high SRF. The reason for that is to guarantee the inductor quality factor is achievable at particular

frequency of interest. The rule of thumb is to have SRF 3 times higher than the operating frequency with inductor quality factor peaking higher than the desired frequency of interest; thus the inductor contribution to the system noise figure is kept at a minimum. The output matching network consists of inductive peaking capacitively coupled to the class AB amplifier with low input impedance.

The balun-LNA architecture consists of two paths as follows; a main transconductance gm gain stage path coupled to an auxiliary one using transformer. The benefits of adding this transformer translates into an increase in the signal to noise ratio (SNR) at the base-emitter junction of the auxiliary path. Hence, a gain boost for less static dc power is achieved. Furthermore; a lower input referred noise is seen in the auxiliary path due to the transformer benefits. Fig.5.3 shows the post-layout simulations of the proposed balun-LNA.

The 3-dB differential power gain S_{21} is 15 dB and the bandwidth is determined according to the return loss S_{11} < -10 dB across the entire frequency band of interest. A linearity improvement technique is based on a constant G_m-cell transconductance behavior for the balun-LNA structure. The constant G_m-cell transconductance is established through equal emitters' area (A_e) ratios and proper base-emitter junction biasing. The constant small signal G_m-cell transconductance remains independent of input and output variations under large signal behavior. The proposed structure achieves a second order intermodulation (IM_2) cancellation, and the measured input referred third order intermodulation (IIP_3) and differential NF are > -1 dB_m and < 3.5 dB; respectively.

The gain and phase mismatches are kept to a minimum. The total power consumption is less than 18mW drawn from a 1.8V power supply.

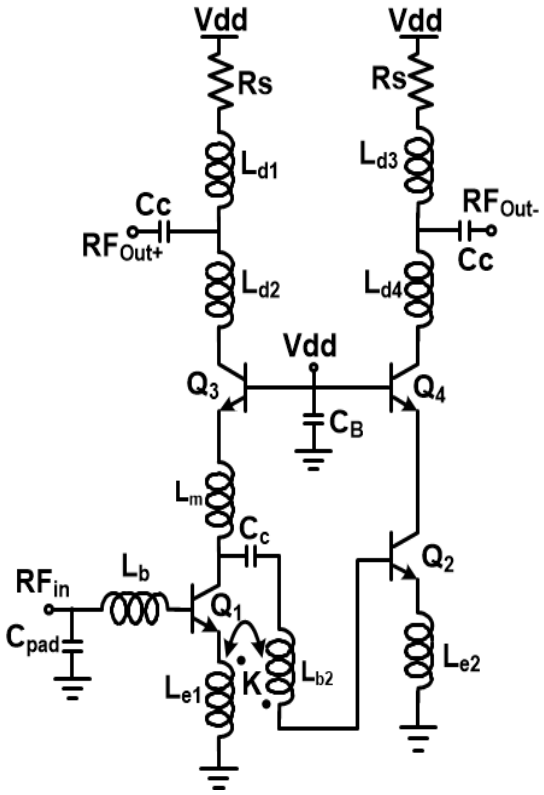

Fig. 5.47 Active balun-LNA circuit implementation.

Table 5.8 Circuit components values for the implemented balun-LNA.

Emitter W x L_{Q1} 0.2 x 10.16 μm^2	Emitter W x L_{Q2} 0.2 x 10.16 μm^2	Emitter W x L_{Q3} 0.2 x 10.16 μm^2	Emitter W x L_{Q4} 0.2 x 10.16 μm^2
C_{be1} = 105 fF	L_{d3} = 245 pH	L_{b2} = 120 pH	C_{pad} = 60fF
C_{be2}= 62 fF	L_b = 300 pH	K = 0.34	L_{e1}/L_{e2} = 80 pH
C_c = 300fF	L_m = 120 pH	L_{d2}/L_{d4} = 90 pH	L_{d1} = 245 pH

5.2.2 Class AB Amplifier

The class AB amplifier is preceded with a highly linear current mode balun-LNA. Note that to maintain receiver chain linearity and suppress the passive mixer noise contribution; a highly linear second gain stage amplifier is required. Fig. 5.48 shows the architecture circuit level design of the class AB amplifier. Current mode operation in RF front-end entails numerous benefits from noise to linearity associated with each RF building block exhibiting low output impedance; *hence no RF voltage gain but RF current gain* [37]-[62]; [63]-[64]. The low output impedance at each RF block limits the voltage swing at that particular node and thus the low distortion and noise levels behavior. To keep the voltage swing to a minimum at the input of the class AB amplifier; a low differential input impedance has to be maintained across the bandwidth of interest. Fig. 5.49 shows the small signal model to the input impedance, $Z_{in,\,AB}$, which consists of the parallel combination of two sections. The first part is made of the diode connected bipolar device Q_4 junction in series with inductor L_2. The second part consists of the common base device Q_2 in series with inductor L_1. The impedance looking into the base of $Q_1$is very high and is ignored for simplicity. The derived input impedance of the class AB amplifier is based on the small signal model shown in Fig. 5.49. Equation (5.1) shows the derived input impedance below;

$$Z_{in,AB}(s) = \left(\frac{\left(1 + Z_1 Z_{comp}\right) Z_2}{1 + Z_{comp}\left(Z_2 + Z_1\right)} \right) \tag{5.1}$$

$$Z_1 = sL_1 + r_{e2} \tag{5.2}$$

$$Z_{comp} = \left(\frac{gm}{1 + r_{bx} sC_\pi} + \frac{1}{r_o} \right) \left(\frac{\frac{r_o}{sL_{p2}} \left(1 + s^2 L_{p2} C_{cs2} \right)}{1 + \frac{r_o}{sL_{p2}} \left(1 + s^2 L_{p2} C_{cs2} \right)} \right) + \frac{r_{bx}}{1 + r_{bx} sC_\pi} \tag{5.3}$$

$$\begin{aligned} Z_2 = {} & sL_2 + \frac{1}{sC_{cs4}} + \frac{\left(1 + sC_{\pi 4} r_{bx4} \right)}{\left(gm + sC_{\pi 4} \right)} \\ & - \frac{\left(r_o + r_{e4} \right) \left(1 + sC_{\pi 4} r_{bx4} \right) \left(1 + r_o r_{e4} gm \right)}{\left[r_{e4} \left(1 + sC_{\pi 4} r_{bx4} \right) + r_o r_{e4} gm \right] \left(sC_{\pi 4} \left(r_o + r_{e4} \right) + gmr_o \right)} \end{aligned} \tag{5.4}$$

where (5.1) can be simplified into ($Z_1 \| Z_2$) with the assumption that $Z_1 Z_{comp} >> 1$. Note that at mm-wave frequencies, V1=V2=0 for $C_{\pi 2} = C_{\pi 4} >> C_{cs2} = C_{cs4}$ and $r_{bx2} = r_{bx4} \approx 0$, which leads to $Z_{in,AB}(s) = ½(sL) + ½ (V_T/(I_c + V_T sC_{cs}))$. We made the assumption that $I_{C4} = I_{C2} = I_C$, $L_1 = L_2 = L$ due to the differential symmetry of the class AB structure and equal device sizes with equal biasing junctions, and V_T is the thermal voltage. We also assumed the devices Q_4 and Q_2 emitter' area sizes are equal, hence $C_{\pi 2} = C_{\pi 4} = C_\pi$. The benefit of having low input impedance relative to the linearity of the receiver chain is demonstrated in Chapter IV. As the class AB input impedance, $Z_{in,AB}$, decreases by increasing the gm transconductance of devices Q_2 and Q_4 ; the receiver system linearity improves and the second gain stage becomes less of a bottleneck linearity problem.

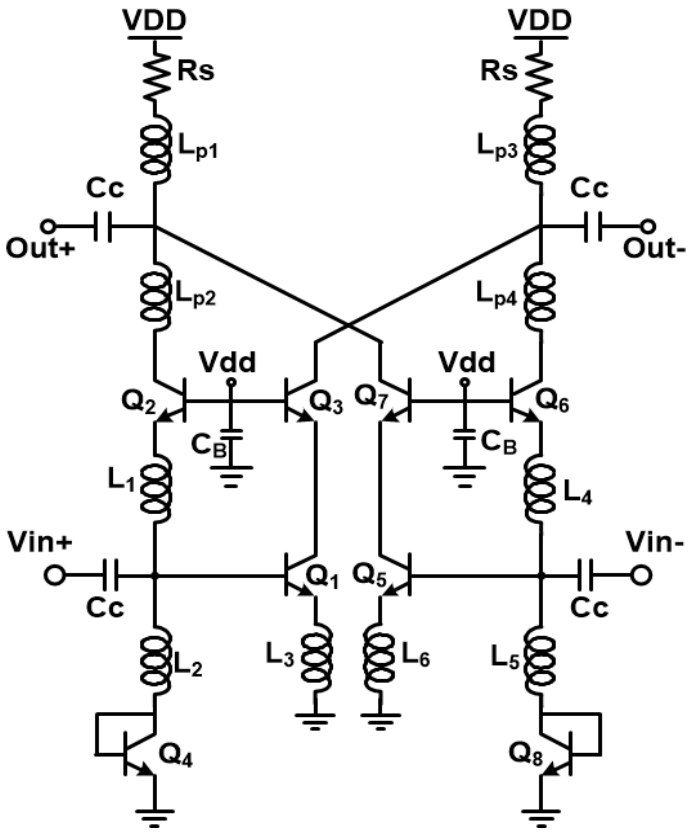

Fig. 5.48 Class AB Amplifier.

Further, the class AB amplifier architecture has a built-in cancelation mechanism through the recycles averaging correction technique described in chapter IV for all phases and amplitudes mismatches generated from the asymmetry balun-LNA structure. Although the differential outputs of the balun-LNA are evenly loaded, the input signal asymmetry path to the outputs causes unequal capacitive coupling parasitic to the substrate, thus the phase and amplitude mismatches.

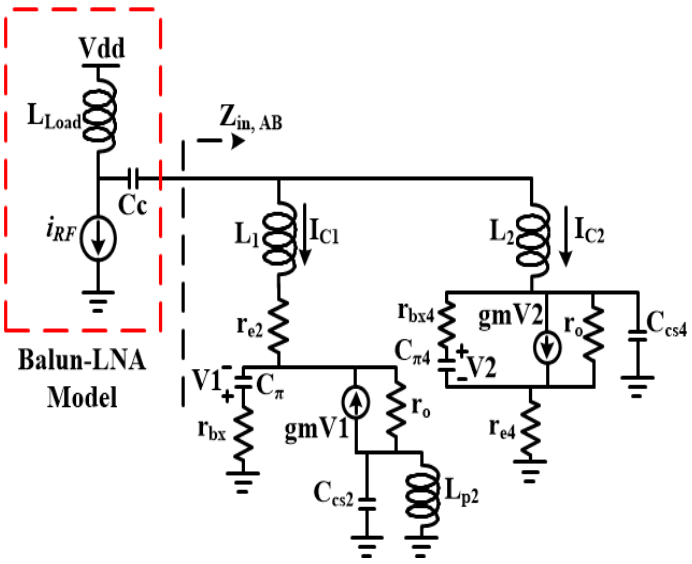

Fig. 5.49 Small signal model for the class AB amplifier input impedance with rbx is the base parasitic resistance, ro is the output resistance, re emitter resistance, base-emitter capacitance Cπ, transconductance gm, and collector-substrate capacitance Ccs.

To resolve this dilemma, a second gain stage, class AB amplifier, is added to the receiver chain. The class AB amplifier consists of two identical baluns with in-phase input current buffer combined with an out of phase current shifted (180º+α) where α is the aggregated multi-stages balun-LNAs' phase mismatches. At the output node of each balun the phase and amplitude mismatches are averaged through the current combinations. Once measuring the differential signal at the outputs of the class AB amplifier, a complete phase error cancellation is possible in theory due to equal averaged phase errors reflected at the outputs. However, the amplitude mismatch error is limited by the class AB amplifier output currents ratios. This partial amplitude error cancellation can limit the phase error cancellation mechanism. Note that the phase and amplitude cancellation mechanism has a built-in calibration technique independent of any passive compensation or neutralization techniques to nullify the capacitive parasitics and is only

limited by the active devices mismatches, thus the operation for the error cancellation mechanism is frequency independent and can reach well into the millimeter-wave frequencies. The amplitude and phase mismatches cancellation at the output of the class AB amplifier are demonstrated in Chapter IV. The simulations show phase and amplitude mismatches less than 2.8º and less than 0.7 dB, respectively from DC up to 50 GHz frequency band.

5.2.3 Passive Mixer and Phase Shifter

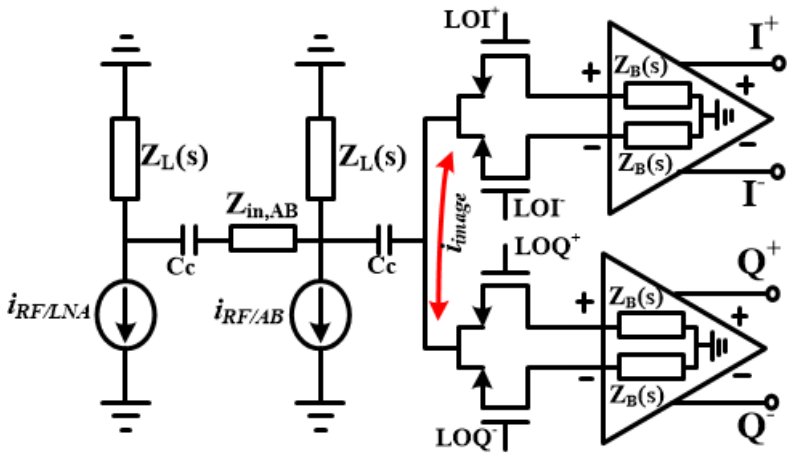

Fig. 5.50 Single sided I/Q receiver RF front end model with current driven passive mixer using 50% duty cycle. Class AB amplifier limits i_image drawbacks on the I/Q receiver.

Fig. 5.50 shows a simple model of the millimeter-wave direct conversion I/Q receiver front-end using ac coupled fully balanced current-driven quadrature passive mixers with 50% duty cycles. The balun-LNA described in chapter III is a transconductor that supplies the RF current modeled by a current source and having load

impedance $Z_L(s)$. The second transconductance gain stage modeled with a secondary RF current source is a class AB amplifier with low differential input impedance, thus *no RF voltage gain and low voltage swing at the output node,* hence the receiver linearity is maintained due to low distortion levels. In addition, the proponents of the ac coupled second gain stage class AB amplifier to the passive mixers are not only limited to the second order intermodulation product improvement, but also help eliminate the *I/Q* channels crosstalk or interaction due to the lack of reverse isolation between RF and baseband side of the passive mixer. This phenomenon is based on baseband offset voltage produced at the input impedance of the current buffer also known as the input impedance of the feed-forward trans-impedance amplifier; where an antiphase current image is generated from one set of switches to another cause *I/Q* interaction that affect high and low sides mismatches of gain conversion, linearity (IIP2, IIP3), and noise figure of the current buffer [25]. Then, the major problem with using 50% duty cycle approach has been resolved due to the second class AB gain stage without sacrificing linearity. Furthermore, no dc current is commutating in the ac coupled deeply trenched dual-well nMOS switches with a built-in high pass filter is established through the combination of the coupling capacitor and the switches attenuating the low noise frequency components, thus the *1/f* noise is greatly reduced at the input current buffer. In Fig. 5.8, two design parameters the designer has control over the device's size and the LO characteristics. In the passive mixer increasing the device's size width helps reduce the switch on resistance, thus its thermal noise contribution is lower. The dc biasing condition at the drain and source of the CMOS switch is set from the input current buffer

impedance. Consequently, the dc bias voltage level of the LO signal is a paramount factor in controlling the switches mode of operation. The characteristics of the LO driver affects the performance of the mixer. Therefore, a large LO signal can help improve the passive mixer conversion gain as well its noise figure. In a 50% duty cycle fully balanced passive mixer, the gain conversion is ideally equal to $2/\pi$ [32]. However, if the switches of the quadrature passive mixer experience less turn on time than off time then; the conversion gain as well as the noise figure are improved at the expense of less linearity. Fig.5.9 shows the circuit schematic for the differential In-phase/Quadrature signal generator based on Quadrature All Pass (QAP) filter reported in [66]. The in-phase/quadrature phase generator is placed in the LO signal path due to relatively high insertion loss. Alternatively, the QAP can be placed the RF signal path however, the tradeoffs between gain and noise figure are to be considered. The simulations results for QAP in the frequency range 22-44 GHz show an insertion loss of 13 dB with in-phase/quadrature amplitude and phase mismatches less than 1.8 dB and $\pm 3^{o}$, respectively. The tradeoff is clear between keeping low insertion loss versus maintaining flat phase response. The total LO power requirement for the passive mixer is 15 dBm using a switch on resistance of 40Ω. The switch size is limited by the maximum available LO power to maintain hard switching; in case of a higher LO power the passive mixer can tolerate a lower switch on resistance and can benefit from higher linearity. From the combination of the LO power signal and the switches sizes, the quadrature passive mixer reaches an acceptable 4 dB noise figure with no power consumption.

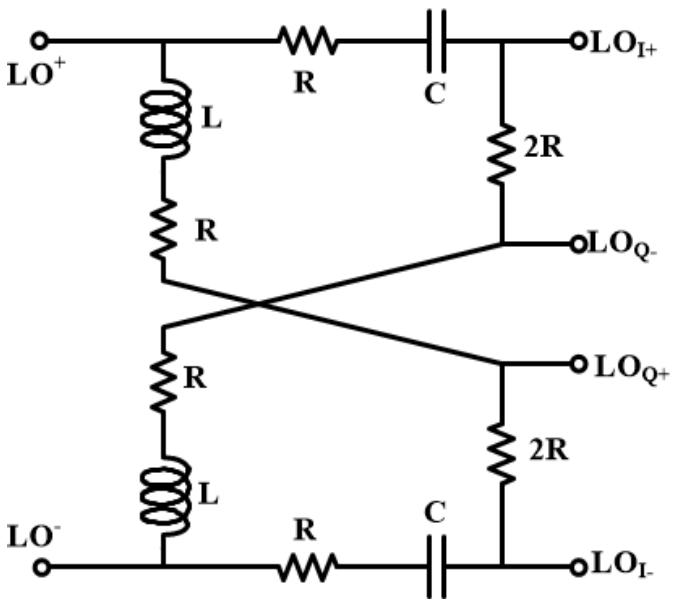

Fig. 5.51 Quadrature all pass signal phase generator

5.2.4 TIA and Anti-Aliasing Filter

Fig. 5.52(a) shows the TIA conceptual system level as well as the schematic circuits' implementation. A feed-forward trans-impedance amplifier (TIA) also known as open loop TIA is deployed to convert the down converted correlated output current from the in-phase/quadrature passive mixers into voltages at the differential outputs of the TIA.

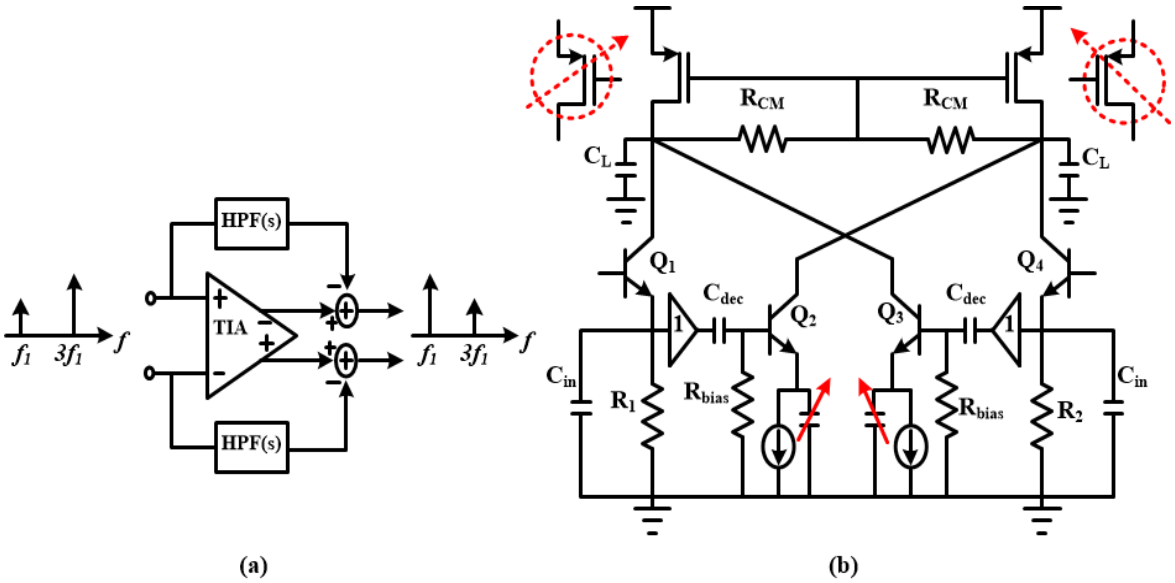

Fig. 5.52 (a) Proposed system level TIA with feed-forward HP filter (b) circuit level design with possible bandwidth control and feed-forward HP filter zeros' locations bits control.

Furthermore, an auxiliary path uses a feed-forward high pass polyphase filter (HPF) to reject blockers and LO harmonics leakage due to direct conversion receiver architecture. Note the importance of 3rd and 5th LO harmonics rejection that cause intermodulation with blockers and interferes to down convert to UWB baseband. Also, a buffer for dc interface is implemented to isolate between the TIA input impedance and the active HPF with no phase and amplitude changes. C_L, C_{in} are designated as the total load and total input capacitances, respectively. The derived trans-impedance transfer function is the following:

$$Z_T(s) = \frac{R_T}{(1+s/\omega_{p1})(1+s/\omega_{p2})} \cdot \left[\left(1 - \left(\frac{s/\omega_{p3}}{s/\omega_{p3}+1} \right) \left(\frac{sgm_2C_s}{sC_s+gm_2} \right) \right) \right] \qquad (5.5)$$

where R_T is defined as the output impedance of the TIA. Poles $\omega_{p1}=gm_1/C_{in}$ and $\omega_{p2}=1/Z_TC_L$ are designated as the dominant and non-dominant poles for the feed-forward TIA, respectively. To optimize the out of band interferers and harmonics cancellation mechanism, the open loop TIA and the feed-forward auxiliary cancellation path exhibit the same transconductances, gm_1 and gm_2 are set equals. The active HPF is preceded by a coarse first order non-evasive HPF with $\omega_{p3}=1/C_{dec}R_{bias}$ where the high frequency signal characteristics are unaltered. The active HPF is established using a capacitively degenerated common source stage as shown in Fig. 5.52(b). A fourth order HPF is seen at the differential output of the feed-forward TIA. Higher order of the feed-forward cancellation filter can be easily implemented through multi-cascaded HPF stages at the expense of greater in-band noise figure. Note that in the case of desirable reconfigurable bandwidth to support various IEEE standards, the degenerated capacitance at the HPF is bit controlled through an encoder to change its poles and zeros' location so as to maintain the same attenuation factor. Furthermore, the output impedance of the TIA has to incorporate a parallel conductance with variable bias control as to trade the trans-impedance gain for the bandwidth. From simulation results, the trans-impedance gain is 55 dBΩ[1] with 500 MHz bandwidth with no stability issues in accordance with minimum UWB receivers' bandwidth requirement. In addition, the open loop TIA achieves 20 dB attenuations of the third harmonic tone at 1.5 GHz. The total system power consumption is 18.6mA drawn from a 1.8V supply.

1. $20\log\left(\frac{V}{I}\right)=dB\Omega$

5.3 Simulations and Measurements

This section addresses the performance of the proposed millimeter-wave coexistent receiver architecture. The first building block programmable multi-stages balun-LNA results are reported in chapter IV. Fig. 5.53 shows the optimized LO power sweep compared to the 50 % duty cycle quadrature passive mixer insertion loss. To limit the excess LO power requirements due to high insertion signal path loss associated with quadrature phase generator and mixer switches sizes; the LO power was selected to be around 15 dBm, hence a 15 dB current mode mixer insertion loss is established. Fig. 5.54 shows the quadrature mixers I/Q channels current mode insertion loss over the bandwidth requirement for a UWB receiver. The I/Q channels exhibit a 0.7 dB amplitude mismatch between the two channels and less than 0.3 dB amplitude variation across the entire bandwidth requirement of 500 MHz. Fig. 5.55 shows the double side band noise figure for the quadrature passive mixer measured across LO power sweep. In general, noise figure measurements are in voltage mode and lower quadrature mixer insertion loss can be achieved in voltage mode compared to Fig. 5.53, an estimated 6 dB lower insertion loss differential compared to its counterpart in current mode. For a 15 dBm LO power, the double side band quadrature passive mixer noise figure, NF_{dsb}, is 4.45 dB. Fig. 5.56 shows the feed-through from LO to IF. The receiver architecture achieves higher than -130 dB isolation which makes the receiver robust for any LO power desensitization. Fig. 5.57 shows LO to RF isolation where one important measure is to limit imaging artifacts due to LO RF re-mixing. The simulated results are higher than 75 dB at 30 GHz. Fig. 5.58 shows the RF to IF isolation. This is a paramount design

parameter associated particularly with direct conversion receiver architecture that has direct impact on the receiver second order intermodulation product IM2 even though the circuit implementation is fully differential. The RF/IF isolation for both channels I/Q are higher than 90 dB isolation tested at 30 GHz with 500 MHz bandwidth. The second important isolation measure from the RF side is the RF/LO isolation shown in Fig. 5.59. The result shows higher than 140 dB isolation between the RF/LO ports at 30 GHz for 500 MHz bandwidth. The input return loss S_{11} of the quadrature phase generator is shown in Fig. 5.60. The input matching S_{11} > -10 dB for the frequency range 18-44 GHz. Fig. 5.61 shows the insertion loss $S_{21,\ 31,\ 41,\ 51}$ of the differential quadrature phase generator based on quadrature all pass approach where the maximum difference between the I/Q channels is 2.2 dB. The high insertion loss is in part associated with low quality factor LC tank to maintain a broadband quadrature operation with minimum phase variations as shown in Fig. 5.62. The trans-impedance amplifier shows a gain of 55 dBΩ for a 500 MHz bandwidth with higher than 18 dB rejection for out of band interferers at 1.5 GHz. The total receiver gain is better than 42 dB with RF front-end noise of 8 dB with P1dB input referred higher than -16 dBm. The die micrograph of the entire millimeter-wave receiver is shown in Fig. 5.63 and the total die area is 1.7mm x 2.8mm including DC pads. Table 5.9 shows the receiver performance in comparison to existing various mm-wave receivers' architectures. These results confirm that the mm-wave coexistent current mode direct conversion receiver exhibits excellent performance for UWB standards achieving high power gain, low noise figure, very high linearity, and very competitive power consumption in the *K/Ka- and V* bands of operation. The

receiver total power consumption including both channels is less than 105mW drawn from 1.8V power supply and using 0.18µm SiGe BiCMOS Jazz semiconductor technology.

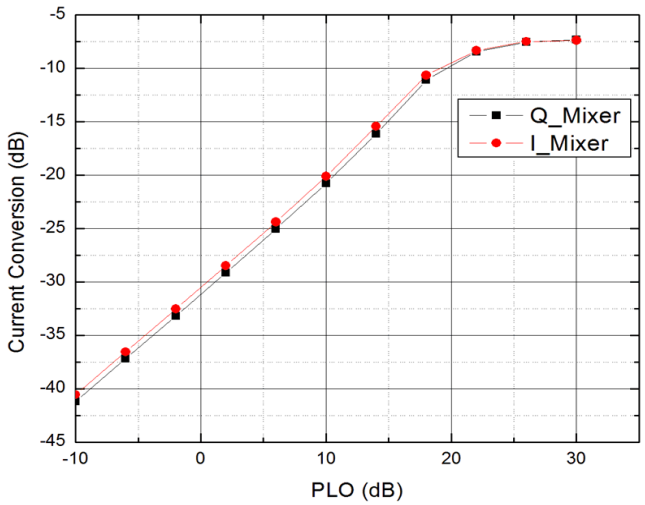

Fig. 5.53 Optimum LO power sweep for minimum current conversion loss.

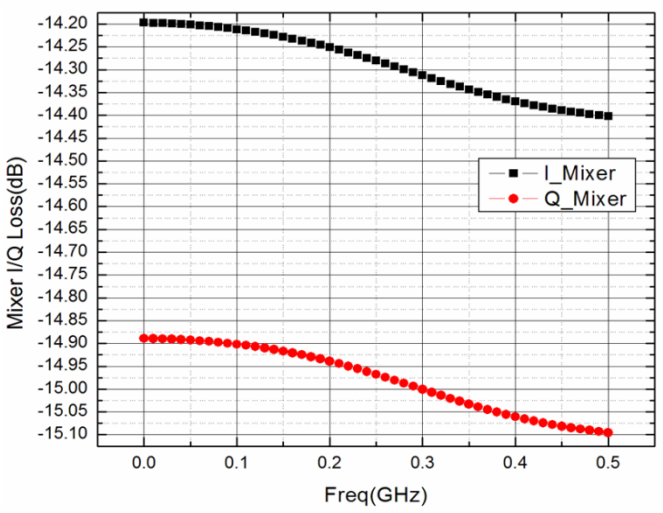

Fig. 5.54 Passive mixer current conversion loss for PLO = 15 dBm.

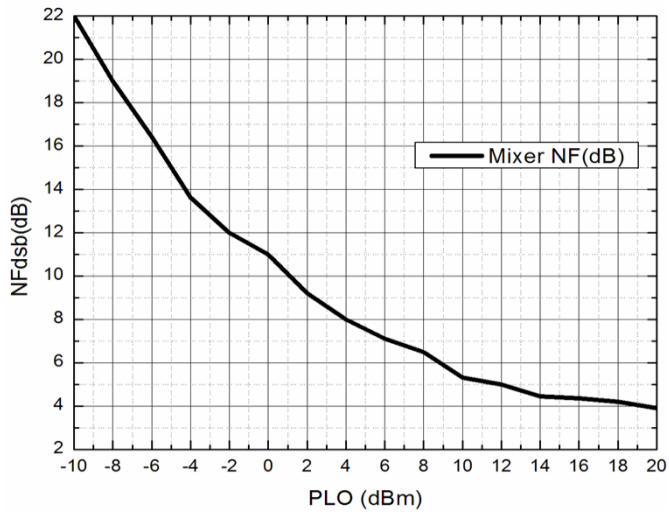

Fig. 5.55 Passive mixer doubled sided noise figure for PLO sweep.

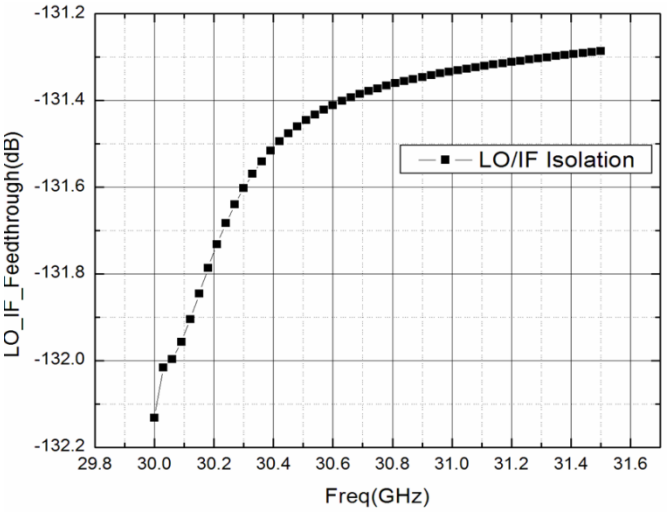

Fig. 5. 56 LO to IF feedthrough.

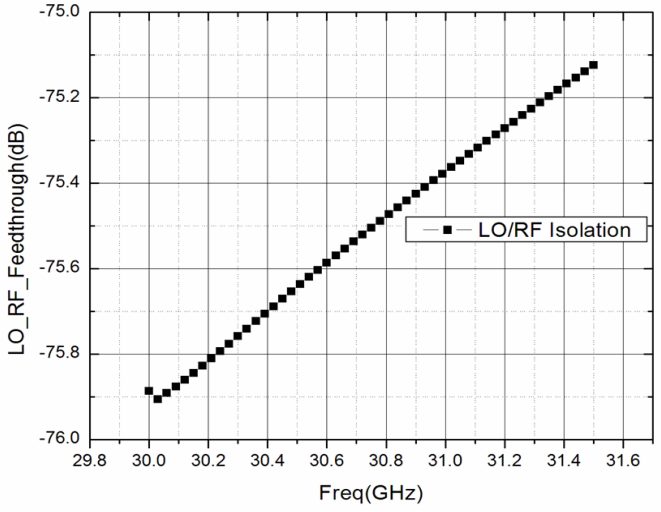

Fig. 5.57 LO to RF feedthrough.

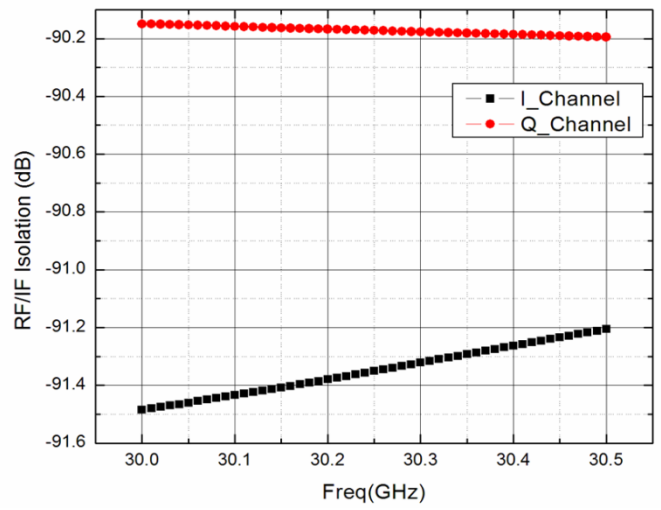

Fig. 5.58 RF to IF feedthrough.

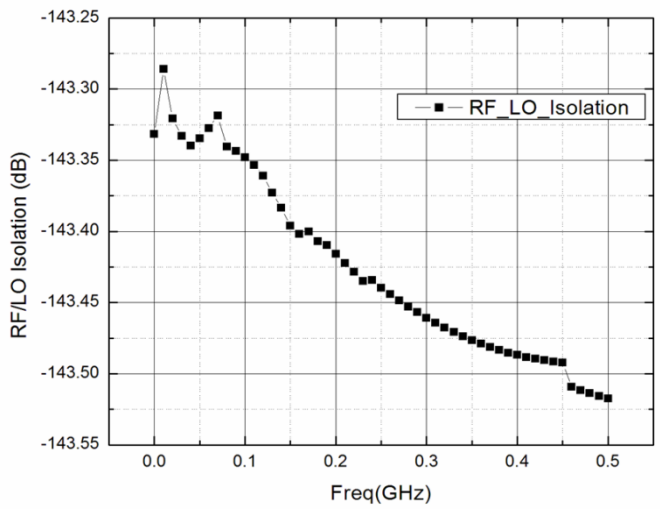

Fig. 5.59 RF to LO feedthrough

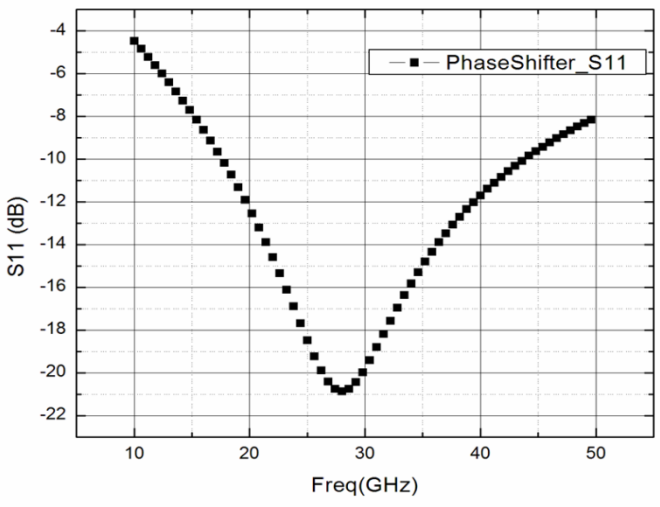

Fig. 5.60 Input return loss into the phase shifter.

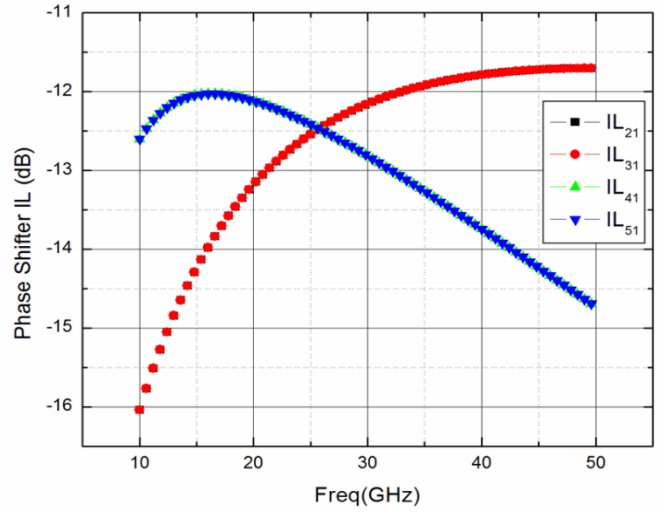

Fig. 5.61 Insertion loss of the quadrature phase shifter.

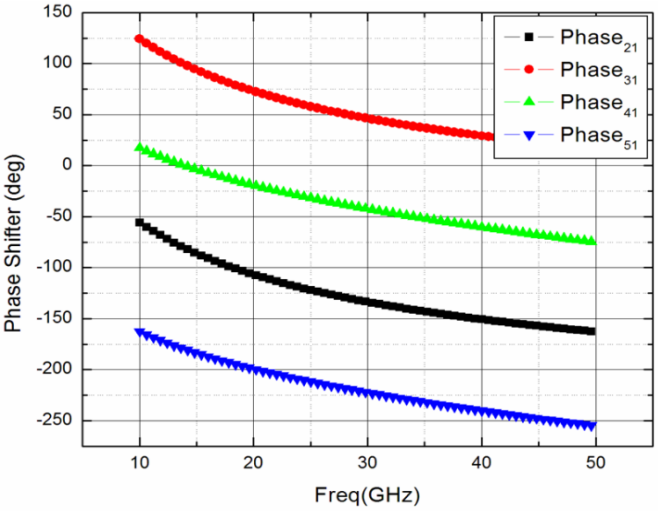

Fig. 5.62 Phase balance of the quadrature phase shifter

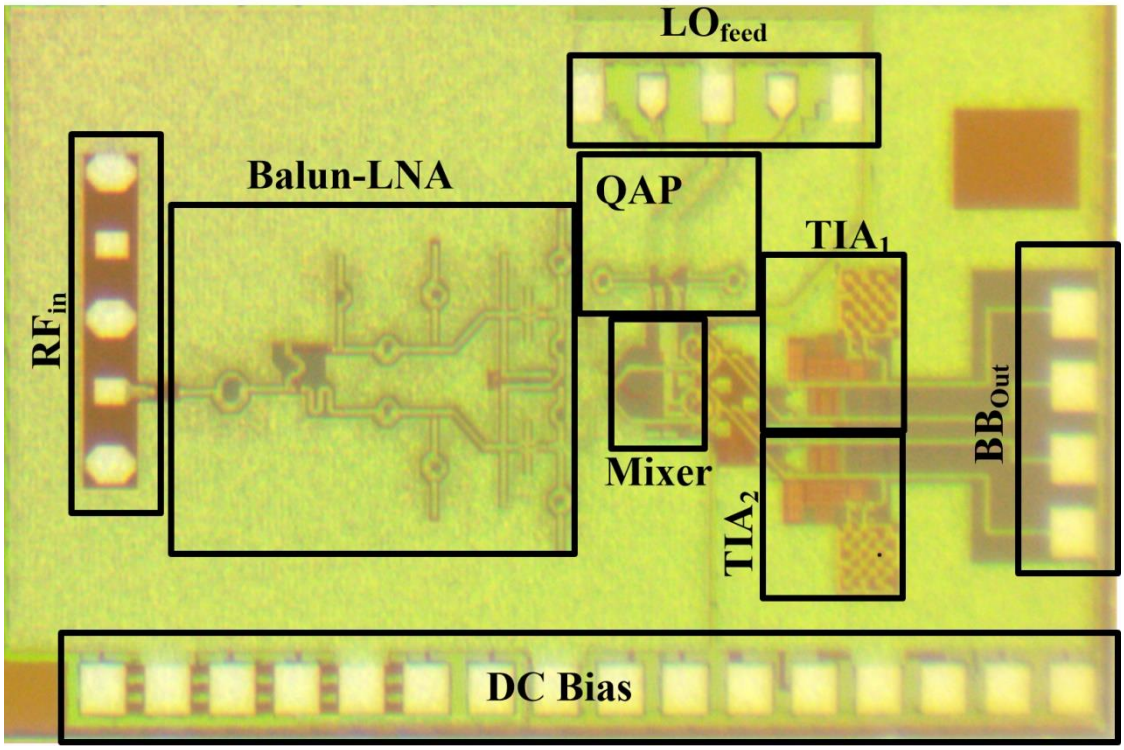

Fig. 5.63 Micrograph die of the receiver.

Table 5.9 MM-wave coexistent receiver performance compared to existing designs

RX	[22]	[70]	[71]	**This Work**
Gain(dB)	35-38.1	23.7	43	**42**
NF (dB) RF Front End	5.5-7.4	5.1	7.4	**8**
P1dB (dBm)	-20.8	-28	-27	**-17**
IIP3	-9	-17.9	-11.5	**>-8**
LO/RF/IF Iso (dB)	<-30,<-23	>-47, >-55	N/A	**>-75 />-132**
RF/IF/LO Iso (dB)	N/A	<-36	N/A	**>-90 / >-143**
BW(3dB) GHz	22-29	21-29	24	**22-44**
Technology	0.18um RFCMOS	0.18um CMOS	0.18um SiGe BiCMOS	**0.18um SiGe BiCMOS**
Power Consumption	131mW	39.2mW	227 mW	**105 mW**

CHAPTER VI

SUMMARY AND CONCLUSION

6.1 Dissertation Summary

Consumers' high demands for wireless data communications and high resolution high accuracy positioning radar sensors have pushed the envelope from low frequency applications spectrum into the mm-wave frequency ranges. RFIC circuits at mm-wave play a crucial role in mm-wave systems and entail numerous challenges on the systems and circuits design levels. In this dissertation, several innovative techniques and RFIC circuit architectures exhibiting unprecedented performance have been proposed and validated, demonstrating potentially significant improvement for mm-wave radar and communication systems. Consequently, the design of an advanced, small die and low-cost millimeter-wave coexistent direct conversion current mode receiver and its components for multi-standards multi-channels short-range, high-resolution radar and high-data rate communication systems have been presented.

A new wideband low power consumption balun-LNA with high linearity has been presented and analyzed. The balun-LNA architecture combines CE-CE stages AC coupled thru a transformer for power saving mode and noise reduction. The balun-LNA exhibits a new linearity technique based on constant gm cell transconductance with equal emitters' ratios, hence making the structure insensitive to large input and outputs variations. The balun-LNA operates in *K*- and *Ka*-bands and provides cancellation for the second order intermodulation IM_2. The new balun-LNA design in 0.18µm SiGe

BiCMOS technology demonstrates an exceptional performance with ultra-low power consumption. The balun-LNA is very suitable for mm-wave low power wireless standards as well as radar applications.

An innovative technique to mitigate amplitude and phase imbalances in active balun-LNA is proposed, analyzed, and demonstrated. The multi-stages new balun-LNA with distributed feed-forward averaging recycles correction technique for amplitude and phase errors is insensitive to unequal paths parasitic from input to outputs. The distributed averaging recycles correction technique resolves the amplitude and phase errors residuals in a multi-iterative process. The new multi-stages balun-LNA averaging correction technique is frequency independent and can perform amplitude and phase calibrations without relying on passive lumped elements for compensation. The multi-stages balun-LNA exhibits excellent performance from 10 to 50 GHz with amplitude and phase mismatches less than 0.7 dB and 2.86º, respectively. Furthermore, the new multi-stages balun-LNA operates in current mode and shows high linearity with low power consumption. The unique balun-LNA design can operates well into mm-wave regions and interfaces well with radar and communication systems.

A new millimeter-wave coexistent current mode direct conversion receiver for multi-standards multi-channels with system level design specifications optimized for high dynamic range is proposed, designed, and validated. The new coexistent receiver architecture consists of two paths one of which transfers the down converted output current gain stages into low input impedance of a trans-impedance amplifier (TIA) with a feed-forward high-pass anti-aliasing blockers filter; *no RF voltage gain*. In addition,

the auxiliary path utilizes an attenuator first block providing robustness to high power jamming UAV radar signals from 35-37 GHz. A class AB amplifier with low input impedance is added to enhance receiver's gain and minimizes amplitude and phase mismatches without limiting the system linearity. The direct conversion receiver is targeted to down convert all IEEE standards within 22-44 GHz spectrum with 500 MHz baseband frequency (IF) bandwidth supporting UWB device applications. The new wideband coexistent receiver architecture exhibits a differential I/Q gain of 42 dB with 11 dB in-band noise figure. The proposed coexistent receiver achieves better than 20 dB rejections for out of band interferes and harmonics and demonstrates a 1-dB gain compression better than -17 dBm. The exceptional receiver versatility and functionality makes it well suited to operate on mm-wave platform serving most IEEE standards for radar and communication systems.

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APPENDIX A

The noise analysis presented in this Appendix is based on the noise model shown in Fig.3.6. Before determining the input referred voltage noise due to the base and collector shot currents of transistors Q_1, Q_2, we had to solve various circuits' impedances affected by the transformer behavior. From the noise model, Z_x is the impedance looking from the base of transistor Q_2 into the transformer. Similarly, Z_c is the impedance at the collector of Q_1. Z_M is the impedance due to Miller effect at transistor Q_1. Further, Z_e, and Z_s are the impedances looking at the emitter and from the base into the source generator of Q_1, respectively. Applying KCL analysis yields Eqs. (A1)-(A5) as follows.

$$Z_x \approx Z_2 \| \left[R_{bx2} + sL_{b2} + \frac{(Kn)sL_{e1}(sL_{b2} + Z_1 + Z_2)(sC_{be} + g_{m1})}{g_{m1}Z_1 - (Kn)sL_{e1}(sC_{be} + g_{m1})} + Z_1 \right] \tag{A1}$$

where Z_1, Z_2 are defined in section II-A.

$$Z_c \approx Z_1 \| \left[sL_{b2} + \frac{(Kn)sL_{e1}(sL_{b2} + Z_1 + Z_2)(sC_{be} + g_{m1})}{g_{m1}Z_1 - (Kn)sL_{e1}(sC_{be} + g_{m1})} + Z_2 \right] \tag{A2}$$

$$\begin{aligned} Z_\mu &\approx [Z_c] + \left({}^{1}\!/_{sC_{bc}} \right) \\ Z_M &\approx \left(\frac{Z_\mu}{(1 - A_v)} \right) \end{aligned} \tag{A3}$$

where A_v is the voltage gain of the balun-LNA.

$$Z_e \approx sL_{e1}\left[1+\frac{(Kn)\left(g_{m1}Z_1-(Kn)sL_{e1}\left(sC_{be}+g_{m1}\right)\right)}{\left(sL_{b2}+Z_1+Z_2\right)\left(sC_{be}+g_{m1}\right)}\right] \tag{A4}$$

$$Z_s \approx \left(R_{bx}+R_{L_b}+sL_b+\left(\frac{R_s}{sC_{pad}R_s+1}\right)\right) \tag{A5}$$

The base and collector current shot noises for transistors Q_1, Q_2 are given by:

$$\overline{i^2_{n,b1,2}} = 2qI_{B1,2} \tag{A6}$$

$$\overline{i^2_{n,c1,2}} = 2qI_{C1,2} \tag{A7}$$

where q is the electron charge constant, and $I_{B1,2}$ and $I_{C1,2}$ are the collector and base currents for transistors Q_1, Q_2, respectively.

The input referred voltage noise due to the base and collector currents shot noises of transistors Q_1 and Q_2 including the parasitic base resistance R_{bx2} are shown in (A8)-(A12) where β is the current gain of Q_1 and Q_2.

$$\frac{\overline{v^2_{ni,Q1}}}{\overline{i^2_{n,c1}}} \approx \left|\left[1-\frac{Z_e}{Z_e+\left(\frac{r_e}{sC_{be}r_e+1}\right)\left(1/\beta\right)\left(\frac{Z_MZ_s}{Z_M+Z_s}\right)}\right]\frac{1}{g_{m1}}\right|^2 \tag{A8}$$

$$\frac{\overline{v^2_{ni,Q1}}}{\overline{i^2_{n,b1}}} \approx \left|\begin{array}{l}\left(\frac{Z_MZ_s}{Z_M+Z_s}\right)\left\|\left(\left(\frac{\beta r_e}{sC_{be}\beta r_e+1}\right)+\beta Z_e\right)\right.\right. \\ \left.\left.+\frac{Z_e}{Z_e+\left(\frac{r_e}{sC_{be}r_e+1}\right)+\left(1/\beta\right)\left(\left(\frac{Z_MZ_s}{Z_M+Z_s}\right)\right)}\frac{1}{g_{m1}}\right|\right.\end{array}^2 \tag{A9}$$

$$\frac{\overline{v^2_{ni,Q2}}}{\overline{R^2_{bx2}}} \approx \left| \left[\frac{Z_2}{Z_2 + Z_x} \right] \left[\frac{1}{\left(\frac{g_{m1}}{g_{m3}} + nK \right)} \right] \right|^2 \tag{A10}$$

$$\frac{\overline{v^2_{ni,Q2}}}{\overline{i^2_{n,b2}}} \approx \left| \left[\left(\frac{Z_2 Z_x}{Z_2 + Z_x} \right) + \frac{\left(R_{L_{e2}} + sL_{e2} \right)}{\left(R_{L_{e2}} + sL_{e2} \right) + \left(\frac{r_{e2}}{sC_{be2} r_{e2} + 1} \right) + \left(1/\beta \right) \left(\frac{Z_x}{sC_{p2} Z_x + 1} \right)} \right] \left[\frac{1}{\frac{g_{m1}}{g_{m3}} + nK} \right] \right|^2 \tag{A11}$$

$$\frac{\overline{v^2_{ni,Q2}}}{\overline{i^2_{n,c2}}} \approx \left| \left[1 - \left[\frac{R_{L_{e2}} + sL_{e2}}{\left(R_{L_{e2}} + sL_{e2} + \left(\frac{r_{e2}}{sC_{be2} r_{e2} + 1} \right) \right) + \left(1/\beta \right) \left(\frac{\left(R_{bx2} + Z_x \right)}{sC_{p2} \left(R_{bx2} + Z_x \right) + 1} \right)} \right] \right] \cdot \left[\frac{1}{\frac{g_{m1}}{g_{m3}} + nK} \right] \right|^2 \tag{A12}$$

Now, taking the outcomes from (A8)-(A12) and normalize it to the source generator impedance R_s results in (A13)-(A17). $\Psi_1(\omega) - \Psi_5(\omega)$ is the total equivalent input referred voltage noise power shown in (14).

$$\Psi_1(\omega) \approx \frac{1}{2R_s} \left| \left[1 - \frac{Z_e}{Z_e + \left(\frac{r_e}{sC_{be} r_e + 1} \right) \left(1/\beta \right) \left(\frac{Z_M Z_s}{Z_M + Z_s} \right)} \right] \right|^2 \tag{A13}$$

$$\Psi_2(\omega) \approx \frac{1}{2\beta R_s}\left|\frac{\left(\frac{Z_M Z_s}{Z_M + Z_s}\right) \| \left(\left(\frac{\beta r_e}{sC_{be}\beta r_e + 1}\right) + \beta Z_e\right)}{+\frac{Z_e}{Z_e + \left(\frac{r_e}{sC_{be} r_e + 1}\right) + \left(1/\beta\right)\left(\left(\frac{Z_M Z_s}{Z_M + Z_s}\right)\right)}}\right|^2 \tag{A14}$$

$$\Psi_3(\omega) \approx \frac{R_{bx2}\left|\left[\frac{Z_2}{Z_2 + Z_x}\right]\right|^2}{R_s} \tag{A15}$$

$$\Psi_4(\omega) \approx \frac{1}{2\beta^2 R_s}\left|\left[\left(\frac{Z_2 Z_x}{Z_2 + Z_x}\right) + \frac{\left(R_{L_{e2}} + sL_{e2}\right)}{\left(R_{L_{e2}} + sL_{e2}\right) + \left(\frac{r_{e2}}{sC_{be2} r_{e2} + 1}\right) + \left(1/\beta\right)\left(\frac{Z_x}{sC_{p2} Z_x + 1}\right)}\right]\right|^2 \tag{A16}$$

$$\Psi_5(\omega) \approx \frac{1}{2\beta^2 R_s}\left|\left[1 - \left[\frac{R_{L_{e2}} + sL_{e2}}{\left(R_{L_{e2}} + sL_{e2} + \left(\frac{r_{e2}}{sC_{be2} r_{e2} + 1}\right)\right) + \left(1/\beta\right)\left(\frac{\left(R_{bx2} + Z_x\right)}{sC_{p2}\left(R_{bx2} + Z_x\right) + 1}\right)}\right]\right]\right|^2 \tag{A17}$$