Full-bridge Current-fed PV Microinverter with DLFCR Reduction Ability

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***Abstract*- A simple current-fed full-bridge converter (CF-FBC) is proposed as prestage for PV microinverter after comparing with the existing topologies. A modulation strategy based on the CF-FBC with two control freedoms is presented in this paper. One freedom is the boost duty cycle, which controls the voltage of the PV panel. The power duty cycle is other freedom, which controls the voltage in low-voltage-side (LVS). The operational principle of the proposed CF-FBC is analyzed. A control strategy composing three colosed loops is proposed. The regulator parameters are designed based on the small-signals model of the converter. The experimental results verify the effectiveness of the proposed converter and its corresponding modulation and control strategy.**

***Index terms*-** PV microinverter, current-fed full-bridge converter, two control freedoms, DLFCR reduction, resonant regulator.

I. INTRODUCTION

In recent years, various types of inverters used in PV generation systems are extensively researched [1] – [4]. PV microinverter, whose typical power is 100~300W, has been paid more and more attention to due to the following advantages: maximum of energy harvest, low cost of mass production, plug and play operation, easier installation and expansion [5] – [7].

The most commonly used topologies for PV microinverters are based on flyback converter [8] and forward converter [9]. The interleaved flyback [10] and forward [11] converters are adopted for high rated power. With the increment of photoelectric transformation efficiency, the rated power of THE PV microinverter becomes larger and larger whose maximum value is upto 500W [12]. More interleaved units make The PV microinverter more complicated and more expensive, which reduce the competitiveness of the PV microinverter. Therefore, the PV microinverters based on half-bridge[13], current-fed and voltage-fed push-pull[14]- [15], current-fed isolated dual-boost[16], various kinds of resonant full-bridge[17]-[18] have been proposed to achieve higher efficiency and relatively lower cost compared with the interleaved topology.

The requirement of another important performance for PV microinverter is that its lifespan must match the lifespan of PV panel whose lifespan is normally about 25 years. [19]. However, there is power difference between the input-side and the grid-side of the PV microinverter. The input-side power generating from the PV panel is constant in steady state. The grid-side power is determined by the gird voltage and grid current and its instantaneous fluctuation range is very large. Therefore, an element for balancing energy difference between the grid-side and the the PV side must be equipped in the PV microinverter [20] – [21]. An electrolytic capacitor with large capacitance is usually employed to realize this function. It is the most economical method and easy to decouple the power difference. However, the PV microinverter usually operates in harsh environment, such as on the top of building or in barren desert, etc. The utilization of the electrolytic capacitor decreases the lifespan of the PV microinverter [22]. Compared with the same volume of the electrolytic capacitor, the film capacitor has much smaller capacitance while with longer lifespan. Larger double-line-frequency current ripple (DLFCR) component will be included in output current of the PV panel if the electrolytic capacitor is substituted by the film capacitor with smaller capacitance [23]. The DLFCR leads to the decrement of the energy harvest for the PV panel [24]. Hence, the DLFCR must be removed by proper control strategy [25] or additional active power decoupling circuit (APDC) [26] used to store the energy difference between the PV panel and the grid. Although the method of APDC can effectively reduce DLFCR, it also brings the cost and the efficiency to an unacceptable level. Therefore, the method of swing DC bus voltage is a more feasible solution after adopting the film capacitor with smaller capacitance, which requires high performance regulator to reduce DLFCR in output current of the PV panel.

According to the description mentioned above, the purpose of this paper is to find a simple topology with a proper control strategy for low cost, high efficiency and acceptable current ripple level. The existing methods are with some shortcomings

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for achiving this purpose. In [27], the employed converter is the conventional full-bridge converter. The controlled current is the inductor current in the output-side and the current in the input-side isn't directly controlled. The satisfactory effect of DLFCR reduction can be obtained only if electrolytic filter capacitor with large capacitance in the output-side. In [28], current-fed dual-half-bridge converter is used as the prestage of a two-stages inverter, where the input-side current is directly controlled. However, the control strategy is designed for fuel cell system. Meanwhile, the control strategy is coupling because the output voltage and the input current are also regulated by the phase shift angle. In [13], the simplest topology is employed in all existing methods. Its voltages in the low voltage side (LVS) and the high voltage side (HVS) aren't match well, which results in high current stress. In [29], all control objectives have been achieved, but the topology is too complicated for the PV micro-inverter.

In this paper, a simple topology based on current-fed full-bridge converter as the prestage of the PV microinverter has been proposed. There are two control freedoms [30]. One freedom is used to control the voltage and current of the PV panel. Thus, the maximum power point tracking (MPPT) of the PV and DLFCR reduction can be achieved. The other freedom is used to control the voltage in LVS, which can match the voltage between LVS and HVS. Thus, the current stress can be effectively reduced. The experimental results verify the correctness of the theoretical analysis.

II. Motive of Proposed the PV Microinverter

A. The performance requirement of the PV microinverter

The two-stage topology for grid-connected inverter is very prevalent among industrial applications. The output filter capacitor of the prestage DC/DC converter is selected to buffer the power difference between the DC input-side and the AC grid side by swinging its voltage. The commonly used structure for the PV microinverter is shown in Fig. 1.

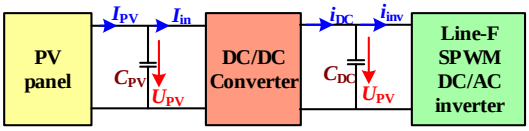


Fig. 1. The commonly used structure for the PV microinverter.

In order to achieve high performance and requirements of different commissions, PV microinverter should satisfy the following index.

1) Maximum power point tracking (MPPT) should be realized and it is usually achieved by controlling the output voltage (U_{PV}) of the PV panel.

2) It is preferred to use film capacitor with smaller capacitance instead of electrolytic capacitor in the microinverter due to the short life of the electrolytic capacitor and bad working environment.

3) Smaller capacitance results in large ripple in the HVS of the DC/DC converter (U_{DC}) due to the instantaneous power difference between the PV-side and grid-side. Proper control strategy should guarantee that there is no DLFCR in the output current of the PV panel (I_{PV}).

4) A proper control strategy should be adopted to guarantee low current stress of elements and high efficiency.

5) It is necessary to adopt a structure with relative simple topology and low cost.

B. The conventional voltage-fed full-bridge converter

In [26] - [27], the used prestage DC/DC converter is based on the conventional voltage-fed phase-shift full-bridge, as shown in Fig. 2(a). The output current I_{DC} is selected as the feedback variable. Meanwhile, there is almost no DLFCR component in I_{DC} through proper control strategy. Hence, there is no DLFCR in I_{DC} and it can be expressed as (1) if high-frequency components over switching frequency are neglected.

$$i_{DC}(\omega t) = I_{DC} \qquad (1)$$

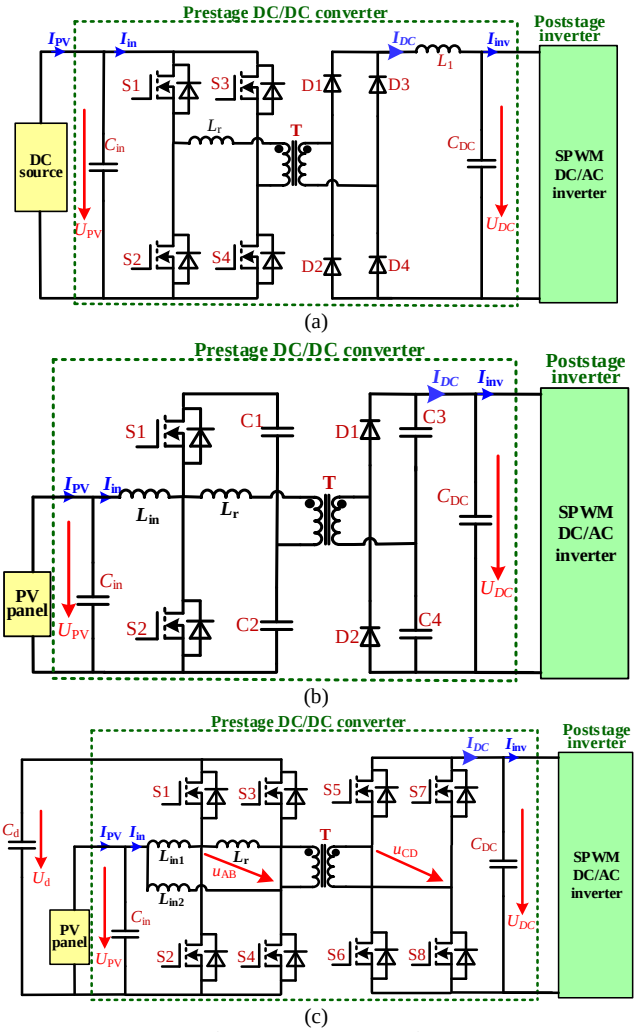


Fig. 2. Three types of prestage converter for PV microinverter: (a) conventional voltage-fed full-bridge in [26] and [27], (b) current-fed boost-half-bridge in [13], (c) current-fed full-bridge in [29].

The input current I_{inv} of poststage inverter can be expressed as (2) if unity power factor is obtained in grid-side.

$$i_{inv}(\omega t) = \sqrt{2}\frac{P}{U_G}\left|\sin \omega t\right| \qquad (2)$$

Where, P is the output power of the microinverter, U_G and ω are the voltage RMS value and the angle frequency of the grid, respectively. The HVS capacitor C_{DC} is required to buffer the energy. The HVS voltage can be calculated by (3) derived in [29].

$$U_{DC}(\omega t) = U_{DC1} + \frac{P}{2\omega C_{DC} U_{DC1}} \sin 2\omega t \quad (3)$$

Where, U_{DC1} is mean value of U_{DC}. There is a double line-frequency component in HVS voltage. Thus, the power from the input-side is expressed as (4).

$$P_{in}(\omega t) = I_{DC} U_{DC}(\omega t) = I_{DC} U_{DC1} + \frac{I_{DC} P}{2\omega C_{DC} U_{DC1}} \sin 2\omega t \quad (4)$$

The fluctuation of input-side power results in the DLFCR in the input current I_{PV}. From (3), the electrolytic capacitor must be equipped to reduce double line-frequency component in the HVS voltage and ripple power in input-side. Therefore, it is hard to satisfy the 2nd requirement mentioned in A-part of Section II.

C. The current-fed Boost-Half-Bridge

A type of current-fed boost-half-bridge is presented in [13], as shown in Fig. 2(b). There is no DLFCR in I_{PV} if boost inductor current I_{in} is selected as feedback variable and resonant regulator is adopted. However, there is only one control freedom, duty cycle of switch S1 or S2, of the converter. The sum voltage across the capacitors C1 and C2 cannot be controlled, which is varying with different output power of the the PV panel. It results in difficulty of current stress optimization. So, it is hard to satisfy the 4th requirement mentioned in A-part of Section II.

D. The current-fed full-Bridge converter

A two-control-freedoms strategy is proposed in [29] and its corresponding topology is shown in Fig. 2(c). One control freedom is the duty cycle of the AC-side voltage (u_{AB} and u_{CD} in Fig. 2(c)) of dual active bridge. The other one is phase shift angle between u_{AB} and u_{CD}. The two-control-freedoms make it possible to realize MPPT, no DLFCR in the current I_{PV} and low current stress. However, the topology is too complicated and too expensive for the PV microinverter with low power.

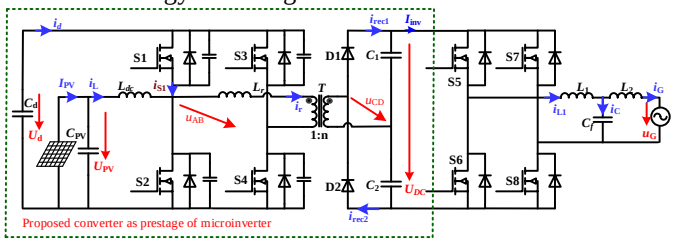
E. The proposed converter and its modulation strategy

In this paper, a current-fed full-bridge converter, as shown in Fig. 3 (a), is proposed as the prestage of the PV microinverter. A boost converter is integrated in the proposed converter, which contains a boost inductor L_{dc}, a bridge arm composed of the switches S1-S2, and a filter capacitor C_d in LVS. The voltage u_{AB} and u_{CD} are AC-side of full-bridge and the rectifier, respectively. The modulation method and the main waveform for the proposed converter is shown in Fig. 3 (b). There are two control freedoms in the modulation strategy. One is called boost duty cycle D_b, which is defined in (5). The other control freedom is called power duty cycle D_p and it is defined in (6). In fact, D_b and D_p are also the duty cycle of S1 and S3/S4 respectively.

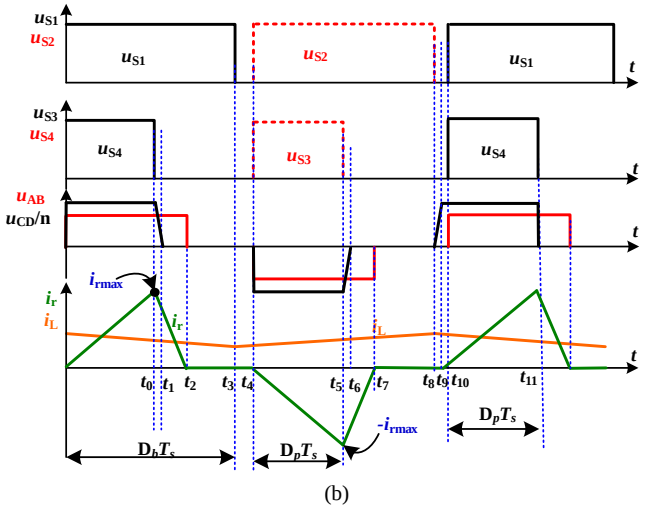
$$D_b = 1 - \frac{t_{10} - t_3}{t_{11} - t_0} = 1 - \frac{t_{10} - t_3}{T_s} \quad (5)$$

$$D_p = \frac{t_{11} - t_{10}}{t_{11} - t_0} = \frac{t_5 - t_4}{t_{11} - t_0} = \frac{t_{11} - t_{10}}{T_s} = \frac{t_5 - t_4}{T_s} \quad (6)$$

Where T_s is the switching cycle. The output voltage U_{DC} is called voltage in HVS in the subsequent paper. The inductor L_r acts as the energy buffering element between LVS and HVS.



(a)



(b)

Fig. 3. The proposed current-fed converter as the prestage of the PV microinverter and its corresponding modulation method, (a) the proposed full-bridge converter, (b) the modulation method for the proposed converter.

The function of the proposed converter with the modulation strategy is equivalent to the combination of a boost converter and a full-bridge converter connected in series. The two control freedoms mentioned above make it possible to realize the same function with the converter in [29]. Most of all, the proposed converter is much simpler and cheaper than that in [29]. As a result, the proposed topology is fitted for the application of the PV microinverter.

One complete switching cycle can be divided into eleven steps. The former three steps are explained in detail as follows. The operation condition of the later three steps is symmetrical with the former three steps. Fig. 4 gives the commutation step diagrams during a switching cycle.

Step 1 [t_0 - t_1 Fig. 4(a)]: Before t_0, S1 and S4 are ON. The current i_L is decreasing linearly and the current i_r is increasing linearly. The rectifier diode D1 is in conduction state.The energy stored in C_d is transmitted to the secondary-side of the transformer. At t_0, S4 is turned off. A resonance between buffering inductor L_r and the parasitic capacitors (or external paralled capacitors) of S3 & S4 begin from t_0. Therefore, the

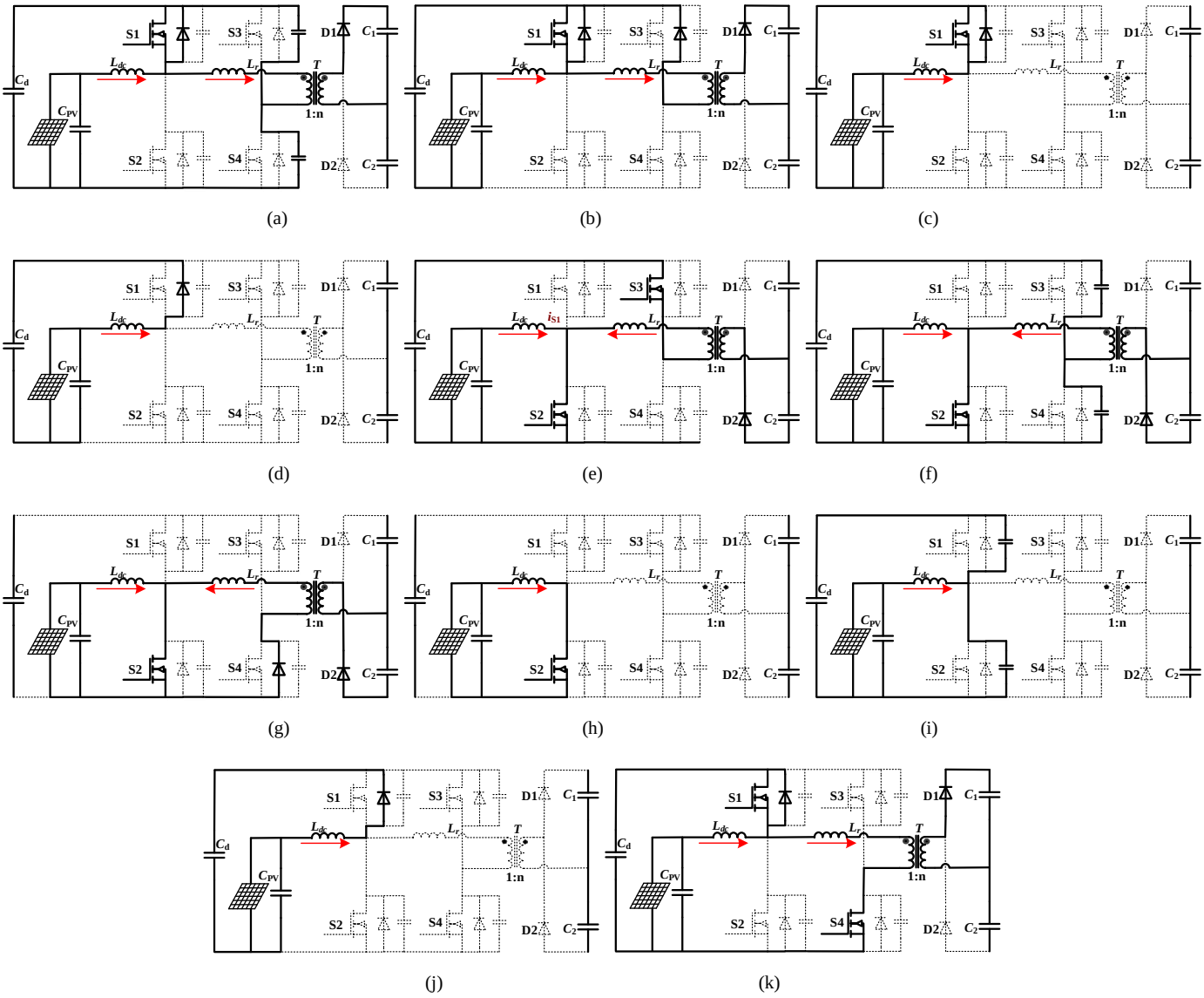


Fig. 4. The equivalent circuit of the proposed converter in different steps, (a) Step 1: t_0-t_1, (b) Step 2: t_1-t_2, (c) Step 3: t_2-t_3, (d) Step 4: t_3-t_4, (e) Step 5: t_4-t_5, (f) Step 6: t_5-t_6, (g) Step 7: t_6-t_7, (h) Step 8: t_7-t_8, (i) Step 9: t_8-t_9, (j) Step 10: t_9-t_{10}, (k) Step 11: t_{10}-t_{11}.

TABLE I SOFT/HARD SWITCHING CONDITION OF ELEMENTS

	S1	S2	S3	S4	D1	D2
ON	t_{10} ZVS	t_4 HS	t_4 ZCS	t_{10} ZCS	t_{10} ZCS	t_4 ZCS
OFF	t_4 HS	t_8 ZVS	t_5 ZVS	t_0 ZVS	t_2 ZCS	t_7 ZCS

terminal voltage of S4 (S3) gradually increases (decreases) from zero (Ud). At t1, the terminal voltage of S4 (uS4) is equal to U_d and the resonant process is over. Thus, the switch S4 achieves ZVS off.

Step 2 [t_1 – t_2 Fig. 4(b)]: After t_1, the body diode of S3 is ON. The voltage u_{AB}=0 and u_{CD}=0.5U_{DC}. The current i_r begins to decrease. At t_2, the current i_r=0. So, there is almost no reverse recovery loss in body diode of S3 and the rectifier diode D1 and we can say that the diode D1 achieves ZCS off.

Step 3 [t_2 – t_3 Fig. 4(c)]: After t_2, the current i_r holds zero. Only the current through switch S1 isn't equal to zero. This step is over until t_3 when the switch S1 is turned off.

Step 4 [t_3 – t_4 Fig. 4(d)]: At t_3, S1 is turned off. The body diode of S1 undertakes the current flowing through the boost inductor i_L.

Step 5 [t_4 – t_5 Fig. 4(e)]: At t_4, switches S2 and S3 are turned on simultaneously. The commutation happens immediately from the body diode of S1 to S2. So, hard switching is received during its ON process. Moreover, there

is reverse recovery loss in the body diode of S1. We can say that S1 is turned off with hard switching and S2 is turned on also with hard switching. After t_4, the current i_L begins to increase linearly and the current i_r begins to increase from zero with negative direction. Both of the switch S3 and diode D2 achieve ZCS on.

Step 6 [t_5 – t_6 Fig. 4(f)]: At t_5, switches S3 is turned off and this process is symmetrical with step 1. It isn't discussed here. From the analysis result, the switch S3 achieves ZVS off.

Step 7 [t_6 – t_7 Fig. 4(g)]: After t_6, the body diode of S4 is ON. This process is symmetrical with step 2 and the diode D2 achieves ZCS off.

Step 8 [t_7 – t_8 Fig. 4(h)]: After t_7, the current i_r holds zero. This process is symmetrical with step 3.

Step 9 [t_8 – t_9 Fig. 4(i)]: At t_8, S2 is turned off. A resonance between boost inductor L_{dc} and parasitic capacitors (or external paralled capacitors) of S1 & S2 begin from t_8. At t_9, the voltage u_{AB}= U_d and the resonance is over. In this resonant process, the terminal voltage of S2 is increasing linearly. At the same time, the terminal voltage of S1 is decreasing linearly. So, S2 achieve ZVS off.

Step 10 & *Step 11* [t_9 – t_{10} Fig. 4(j)] & [t_{10} – t_{11} Fig. 4(k)]: At t_9, the body diode of S1 is on. The switches S1 and S4 are turned on at t_{10} simultaneously. The current i_r begins to increase linearly from zero. Thus, S1 achieves ZVS on. In the secondary-side of the transformer, the rectifier D1 starts to conduct. Therefore, both of the switch S4 and rectifier diode D1 achieve ZCS on. This process lasts until the switch S4 is turned off at t_{11}. The next switching cycle starts after t_{11}.

From the analysis above, the soft/hard switching condition can be concluded in Tab. I.

It should be noted that, the boost duty cycle D_b fluctuates within a small range around 0.5 due to the fluctuation of the PV panel voltage with the weather condition. The fluctuation of the low-voltage side voltage U_d in every line-cycle will be discussed in Section III. Therefore, the waveform of the current i_r is not strictly symmetric within a half switching period. However, as long as the on-time of S3 and S4 is equal, the core of the transformer can operate normally without saturation.

III. Low Current Stress, Low-Frequency Ripple Reduction Strategy

As mentioned in Section II, a boost converter is integrated into the proposed converter. The input voltage of the boost converter is the voltage of the PV panel U_{PV}. The output voltage of the boost converter is U_d in LVS. The current i_L is designed to operate in continuous conduction mode (CCM). So,

$$U_d = \frac{1}{D_b} U_{PV} \tag{7}$$

The filter capacitor C_d in LVS also acts the role of energy buffering. Its absorbed energy is equal to its released energy in every half line cycle. In every switching cycle, there are two components in the current i_d in LVS. One part results from the current i_L between t_0- t_3 and it is defined i_{Ld}. The other part results from the current i_r between t_0- t_1 and t_3- t_4 and it is defined i_{rd}. So,

$$i_d = i_{rd} - i_{Ld} \tag{8}$$

Therefore, the input power and output power in LVS can be obtained according to the product of the i_d and U_d.

$$P_{Ld} = D_b I_L U_d \tag{9}$$

$$P_{rd} = \frac{U_d}{T_s}\left[\int_{t0}^{t1} i_r dt + \int_{t3}^{t4} |i_r| dt\right] = \frac{U_d(2nU_d - U_{DC})D_p^2 T_S}{2nL_r} \tag{10}$$

According to the expression of the power flowing, every control freedom is only related to the corresponding power. It indicates that there is no control decoupling between D_b and D_p. The equivalent circuit of the proposed converter is shown in Fig. 5, where the PV panel is viewed as a current source paralleled with a resistance. C_{12} is the equivalent capacitance of the series of C_1 and C_2. The proposed converter can be controlled as the conventional structure where an isolated full-bridge converter follows a boost converter. So, the control strategy for the proposed converter is given in Fig. 6.

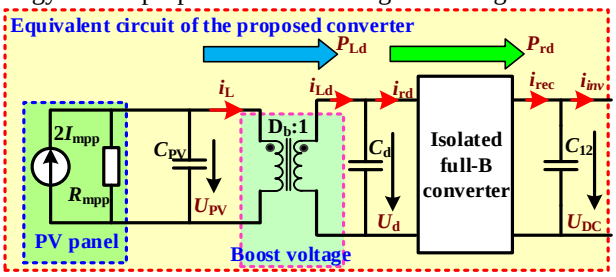


Fig. 5. The equivalent sketch circuit of the proposed full-bridge converter.

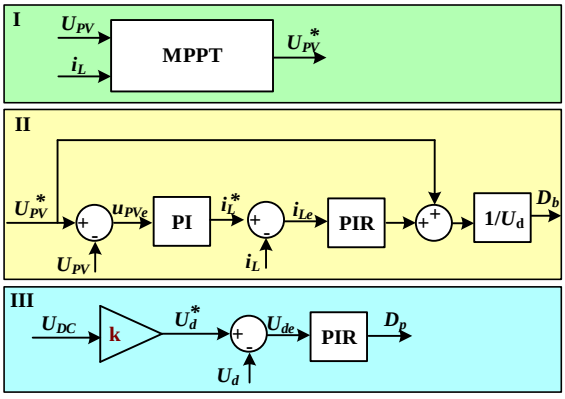


Fig. 6. The control strategy for the proposed full-bridge converter.

There are three parts in the control strategy. The first part is to fulfill the function of MPPT. The reference voltage for the PV panel (U^*_{PV}) is achieved by MPPT controller. The second part is to stabilize the PV voltage and reduce DLFCR by boost duty cycle D_b where a resonant regulator is adopted. There is a voltage feed forward link in the voltage control of the PV panel. Its purpose is to shorten the starting time of the converter. The voltage control cannot affect the stability of the converter. The third part is to control the voltage in LVS to match the voltage in HVS by power duty cycle D_p, which can effectively reduce the current stress of elements in the converter.

IV. Parameter Design Of Regulators

According to the equivalent schematic diagram of the converter shown in Fig. 5, the corresponding voltage-current relationships for the PV cell side filter capacitor C_{PV}, the boost inductor L_{dc}, and the capacitor C_d in LVS are established, respectively.

$$C_{PV}\frac{dU_{PV}}{dt}=2I_{mpp}-\frac{U_{PV}}{R_{mpp}}-i_L \tag{11}$$

$$L_{dc}\frac{di_L}{dt}=U_{PV}-D_bU_d \tag{12}$$

$$C_d\frac{dU_d}{dt}=i_{Ld}-i_{rd} \tag{13}$$

The small-signal state-space equations of the proposed converter can be obtained if the disturbances are introduced into the expression in (11)-(13) (shown in appendix A). Accordingly, the control-to-output transfer functions G_{UPV_Db} (s), G_{Ud_Dp} (s) are summarized in (14) and (15).

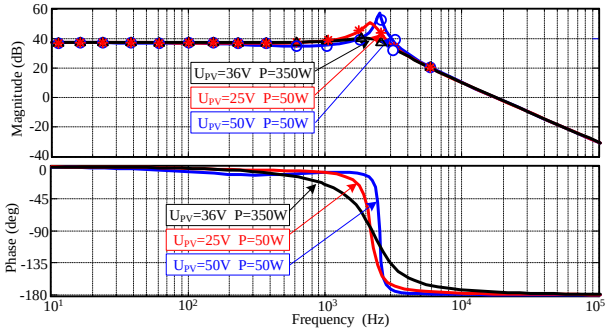
$$G_{UPV\_Db}(s)=\frac{\frac{U_d}{L_{dc}C_{PV}}s+\frac{U_dD_p^2T_S+L_rD_bi_L}{L_{dc}L_rC_{PV}C_d}}{A(s)} \tag{14}$$

$$G_{Ud\_Dp}(s)=\frac{-\frac{(2nU_d-U_{DC})D_pT_S}{nL_rC_d}\left(s^2+\frac{1}{C_{PV}R_{mpp}}s+\frac{1}{L_{dc}C_{PV}}\right)}{A(s)} \tag{15}$$

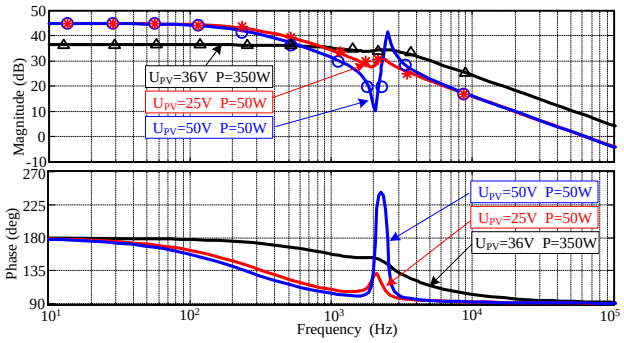
Where,

$$A(s)=s^3+\frac{L_rC_d+C_{PV}R_{mpp}D_p^2T_S}{L_rC_{PV}C_dR_{mpp}}s^2+\frac{L_{dc}D_p^2T_S+L_rC_{PV}R_{mpp}D_b^2+L_rC_dR_{mpp}}{L_{dc}L_rC_{PV}C_dR_{mpp}}s+\frac{L_rD_b^2+R_{mpp}D_p^2T_S}{L_{dc}L_rC_{PV}C_dR_{mpp}}$$

Fig. 7 shows the bode plots of G_{UPV_Db}(s) and G_{Ud_Dp}(s) with different operational parameters, which are shown in Table I in Section IV. In Fig. 7, the curves with the symbols '△, ○, *' represent the bode-plots achieved by scanning AC-signal with PSIM software. We can see that the bode-plots achieved by different methods basically coincide with each other, which verifies the correctness of the small-signal state-space equations.



(a)



(b)

Fig. 7. The bode plot of G_{UPV_Db} and G_{Ud_Dp} in different operational condition. (a) Bode-plot of G_{UPV_Db}. (b) bode-plot of G_{Ud_Dp}.

A. Parameter design of voltage and current regulator for the PV panel

The second part of the proposed control strategy in Fig. 6 is composed of two closed-loops. The feedback variable of the inner loop is the boost inductor current i_L. The DLFCR is reduced by employing a proportional-integral-resonant (PIR) regulator. The feedback variable of the outer loop is the PV panel voltage U_{PV} and only a proportional-integral (PI) regulator is used to stabilize the PV panel voltage. The bandwidth of voltage loop can be low to ensure the robustness of the converter because the variation of operation voltage for the PV panel is slow when weather changes.

The control diagram of the dual-loop is shown in Fig. 8, where the voltage feed forward link is not shown. It is because that the voltage feed forward link is not included in the feedback loop path. In Fig. 8, G_v(s) and G_{cb}(s) are the transfer function of voltage outer loop regulator, and the current inner loop regulator, respectively. H_r(s) is the equivalent delay link of the sample time and feedback filter, which is a first-order low-pass filter with corner frequency of 1/4 switching frequency in the experiment. So,

$$H_r(s)=\frac{1}{1.6\times10^{-5}s+1} \tag{16}$$

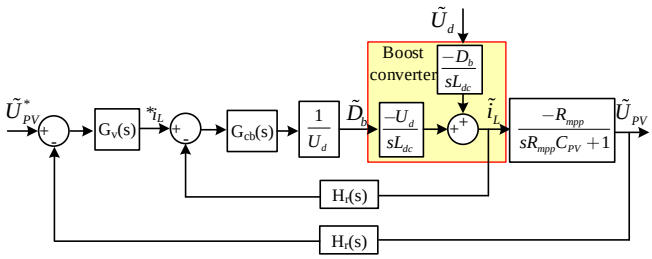


Fig. 8. The control block diagram for the PV output voltage.

According to the characteristic of the open loop transfer function, the inner current regulator can be determined as (17).

$$G_{cb}(s)=-1.5-\frac{250}{s}-\frac{200\pi s}{s^2+4\pi s+4\omega^2} \tag{17}$$

The total open loop gain of the current-loop is shown in (18).

$$T_{cb}(s)=-\frac{1}{sL_{dc}}H_r(s)G_{cb}(s) \tag{18}$$

Figs. 9 (a) and (b) show the uncompensated and compensated bode-plots of the inner boost inductor current loop and outer voltage loop, repectively, when U_{PV}=36V and P=350W.

From Fig. 9 (a), the phase margin of current loop is 66° after adopting the current regulator in (24). The bandwidth, one-decade frequency away at dual-line-frequency (100Hz), is 1020Hz, which guarantees good dynamic performance of current tracking. The gain is high (50.8dB) at dual-line-frequency (100Hz) because of the introduction of resonant regulator, which makes it possible to reduce the DLFCR to a proper level in the PV current.

The closed-loop transfer function of the inner current loop is

$$G_{i\_loop}(s)=\frac{i_L(s)}{i_L^*(s)}=\frac{G_{cb}(s)}{H_r(s)G_{cb}(s)-sL_{dc}} \tag{19}$$

So, the total open loop gain of the outer voltage loop with the voltage regulator is

$$T_v(s)=-\frac{R_{mpp}G_{i\_loop}(s)G_v(s)}{sR_{mpp}C_{PV}+1} \tag{20}$$

The voltage regulator is designed as (28).

$$G_v(s)=-0.1-\frac{50}{s} \tag{21}$$

From Fig. 9 (b), the phase margin of the voltage loop is 100° and the bandwidth is 30Hz. Although the bandwidth is low, it is fast enough to control the PV voltage compared to the slow changing weather and disturbance time intervals of MPPT.

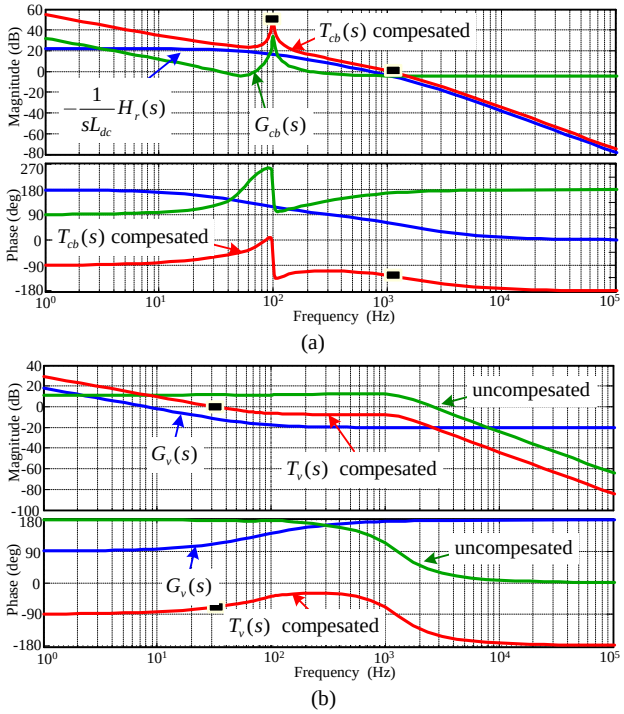


Fig. 9. The bode plot of inner current loop and the outer voltage loop, (a) the bode plot of inner current loop, (b) The bode plot of outer voltage loop.

Fig. 9 only shows the bode-plots when U_{PV}=36V, P=350W. It is necessary to verify the stability under different operating conditions of the PV panel. In Fig. 8, setting

$$H_1(s)=\frac{-1}{sL_{dc}} \tag{22}$$

$$H_2(s)=\frac{-R_{mpp}}{sR_{mpp}C_{PV}+1} \tag{23}$$

Thus, the closed-loop transfer function of the current loop and the voltage loop can be achieved as (24) and (25), respectively.

$$G_{i\_loop}(s)=\frac{H_1(s)G_{cb}(s)}{1+H_1(s)H_r(s)G_{cb}(s)} \tag{24}$$

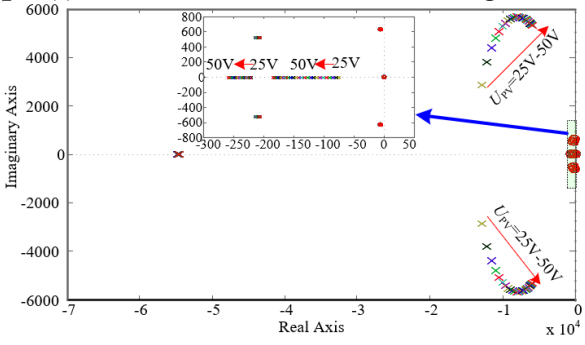
$$G_{v\_loop}(s)=\frac{H_2(s)G_v(s)G_{i\_loop}(s)}{1+H_r(s)H_2(s)G_v(s)G_{i\_loop}(s)} \tag{25}$$

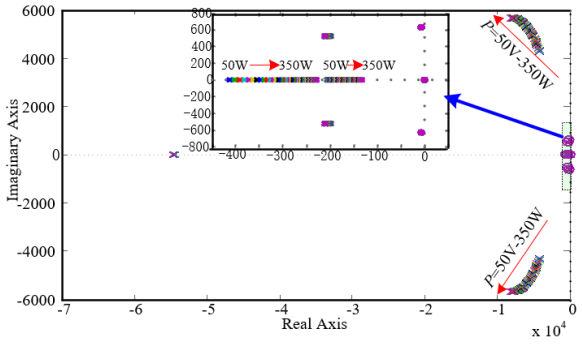
The pole-zero locus of the closed the PV voltage loop in Fig. 10 evaluates the control system stability and performance of the proposed converter. The system is always stable in the whole operating range since all the poles of the closed-loop system are in the left half of s-plane. The pole-zero locus shows that the stability is stronger in time of higher PV voltage and lower power.

B. Parameter design of Voltage regulator in LVS

The voltage in LVS (U_d) can be regulated by the power duty cycle (D_p), which can control the power flow from LVS to DC bus. The converter can also be normally operated even if the voltage in LVS (U_d) cannot be controlled. However, the voltage in LVS (U_d) fluctuates with the variation of power. There is a large voltage variation of the DC bus (U_{DC}) due to the power difference between the PV panel and the grid. The unmatched voltage between U_d and U_{DC} leads to the large current stress of the elements and the low efficiency of the microinverter. Thus, it is necessary to force the voltage U_d to follow the varying voltage U_{DC}. This function can be fulfilled if the reference voltage U_d is set to be k times of the voltage U_{DC}.

The diagram for controlling the voltage in LVS is shown in Fig. 11. In the control diagram, it contains the transfer function of voltage loop regulator $G_{vp}(s)$, transfer function $G_{Ud\_Dp}(s)$ derived in (21), transfer functions $G_{Ud\_Db}(s)$ and $G_{Ud\_UDC}(s)$ from disturbance sources to the voltage U_d.





(b)

Fig. 10. Pole-zero locus of closed transfer function of the PV voltage loop, (a) P=350W，U_{PV} varies from 25V to 50V, (b) U_{PV} =36V，P varies from 50W to 350W.

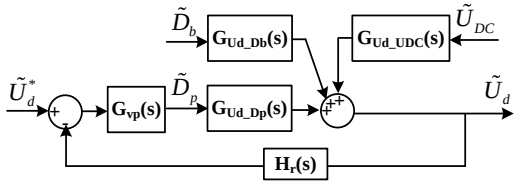


Fig. 11. The control block diagram for the voltage U_d.

The impact of transfer function $G_{Ud\_Db}(s)$ and $G_{Ud\_UDC}(s)$ cannot affect the stability of the closed loop of voltage in LVS. Thus, only the effect of the disturbance D_p in the forward channel is considered. A modified PI with plugged resonant regulator in (26) is given to control the voltage in LVS.

$$G_{vp}(s) = -\frac{350(s+160\pi)}{s(s+2400\pi)} - \frac{4\pi s}{s^2+4\pi s+4\omega^2} \tag{26}$$

A zero at 80Hz is designed to ensure that the gain at dual-line-frequency isn't too small. A pole at 1200Hz, about half of the frequency with natural resonant peak, as shown in Fig. 7, is placed to attenuate this peak at low-power condition. Moreover, the purpose of the resonant regulator is to realize high gain at 2ω frequency so that the LVS voltage is well synchronized with the HVS voltage. Fig. 12 shows the uncompensated and compensated bode-plots of the voltage loop in LVS when U_{PV}=36V and P=350W. The gain at 2ω frequency is 36.7dB and the bandwidth of the loop is 1.25kHz, which can effectively guarantee that the voltage at LVS can quickly track the fluctuation of the DC bus voltage. Therefore, the current stress can be reduced effectively.

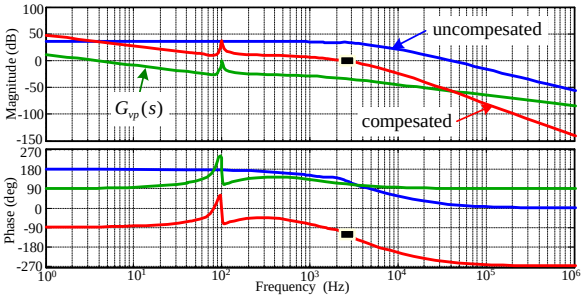
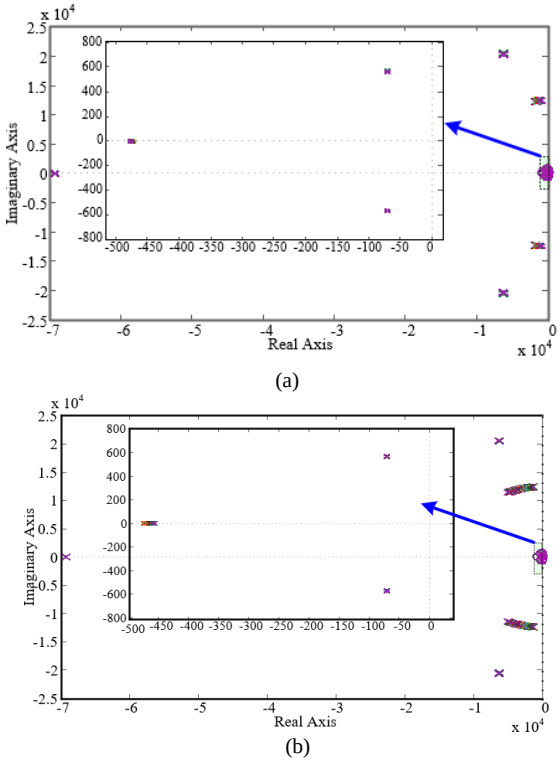


Fig. 12. The bode plot for deigning voltage loop in LVS.

The pole-zero locus of the closed LVS voltage loop is shown in Fig. 13 to evaluate the control system stability and performance of the proposed converter with the changes g of the PV voltage and the power. We can see that the position of the main characteristic roots is almost unchanged unchanged. Thus, the stability of the system cannot be affected by the variations of external parameters.



(a)

(b)

Fig. 13. Pole-zero locus of closed loop transfer function of LVS voltage loop, (a) P=350W, U_{PV} varies from 25V to 50V, (b) U_{PV} =36V, P varies from 50W to 350W.

V. Experimental and Simulation Verification

In order to verify the feasibility of the proposed converter for the PV microinverter, a 350-W PV microinverter prototype is built. The parameters and elements model are presented in Table II and the PV microinverter prototype is shown in Fig.14.

TABLE II PARAMETERS FOR MICROINVERTER PROTOTYPE

Switching frequency	Proposed DC/DC:40kHz SPWM DC/AC: 10kHz
Grid voltage	$110\sqrt{2}\sin(100\pi t)$
PV panel	Maximum power：350W Voltage in MPP：36V
switches	S1-S4: IRFB4110 D1-D2:C3D05060A S5-S8: IXFX 55N50
Filter capacitors	C_{PV}:10μF/50V C_d:22μF/100V C_1, C_2:150μF/100V C_f: 5μF/250V
inductors	L_{dc}:200μH L_r:13μH L_1:1mH L_2:0.5mH
transformer	n=1.7

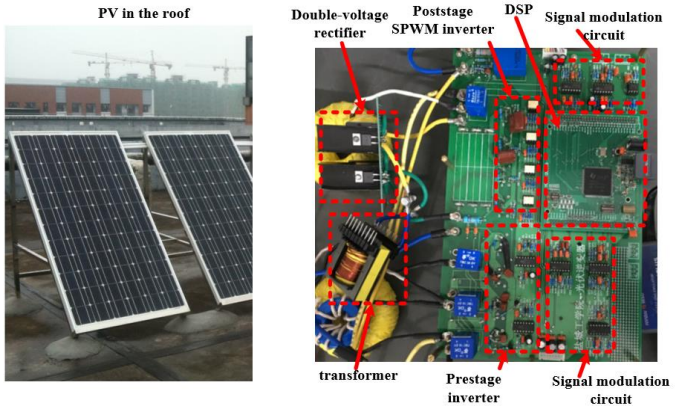


Fig. 14. The photo of PV microinverter prototype .

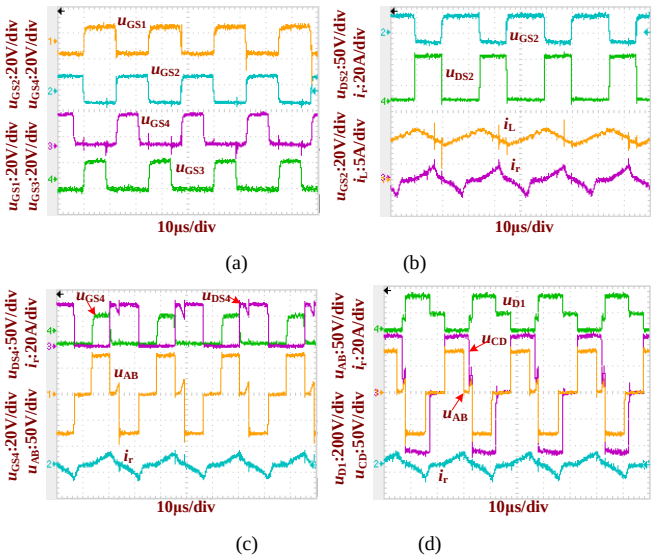
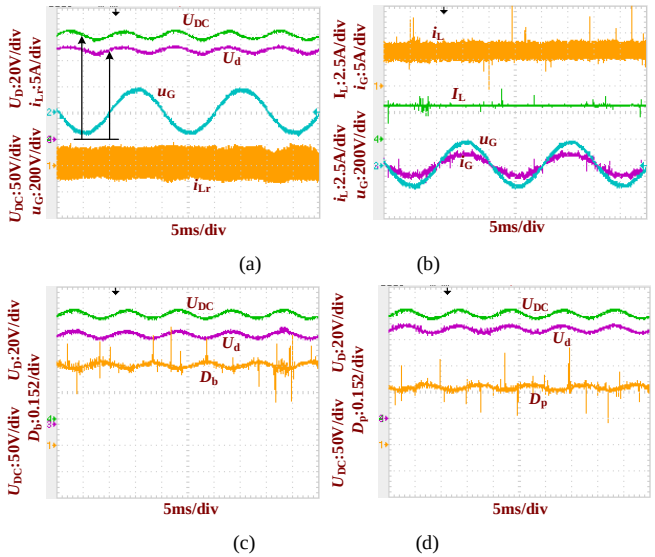


Fig. 15. Waveforms of the proposed converter within switching cycle when power is 350W. (a) Drive signals for S1-S4. (b) Waveforms of u_{GS2}, u_{DS2}, i_r, i_L. (c) Waveforms of u_{GS4}, u_{DS4}, u_{AB} i_r. (d) Waveforms of u_{D1}, u_{AB}, u_{CD}, i_r.



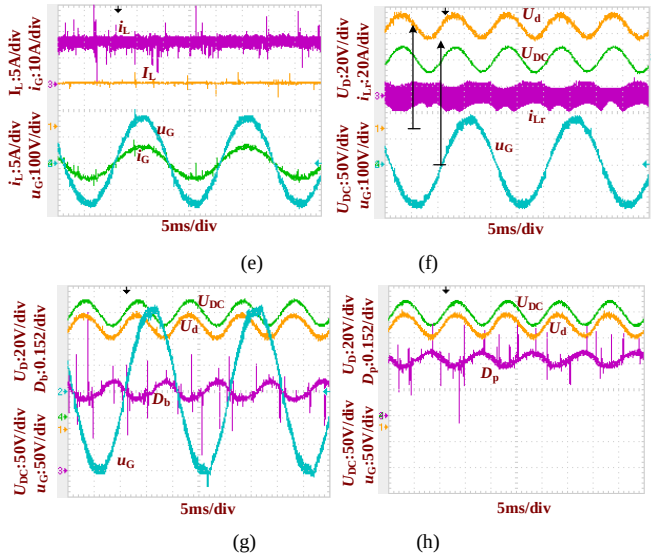


Fig. 16. Waveforms of the proposed converter within line cycle with different power. (a) Operational waveforms 1 with 100-W power. (b) Operational waveforms 2 with 100-W power. (c) Operational waveforms 3 with 100-W power. (d) Operational waveforms 4 with 100-W power. (e) Operational waveforms 1 with 300-W power. (f) Operational waveforms 2 with 300-W power. (g) Operational waveforms 3 with 300-W power. (h) Operational waveforms 4 with 300-W power.

Fig. 15 shows the operational waveforms of the proposed converter in steady state when the output power is 350W. The drive signals of switches S1-S4 (u_{GS1}- u_{GS4}) are shown in Fig. 15(a). The realtionships of the phases are same with the theoretical waveforms in Fig. 3(a). The waveforms of drive signal and terminal voltage of switch S2 (u_{GS2}, u_{DS2}), and the current i_r and i_L are shown in Fig. 15(b). The rising process of i_L corresponds to the time during which the switch S2 is turned on. The current i_r always returns to zero at every half switching cycle. The waveforms of drive signal and terminal voltage of switch S4 (u_{GS4}, u_{DS4}), voltage u_{AB} and current i_r are shown in Fig. 15(c). The positive and the negative parts of the voltage u_{AB} synchronize with the positive direction increase and negative direction increase of i_r, respectively. It is noted that there is a resonant process between the buffering inductor and parasitic capacitors of the switches S1-S4 after the current i_r falls to zero, which results in a gap in the terminal voltage of S4 (u_{DS4}). There is almost no power loss during this resonant process due to the small resonant current. Fig. 15(d) shows the waveforms of the reverse voltage of diode D1 (u_{D1}), the voltage u_{AB}, u_{CD} and the current i_r. We can see that the positive and negative parts of the voltage u_{CD} synchronize with the positive part and negative part of i_r. The voltage amplitude of u_{D1} is equal to half of the voltage U_{DC} in HVS.

The waveforms shown in Figs. 16 (a) – (d) are obtained when the output power is 100W with the proposed control strategy. Fig. 16 (a) shows the waveforms of the voltage in LVS (U_d), DC bus voltage (U_{DC}), grid voltage (u_G) and current i_r. There is 2ω frequency voltage ripple component both in U_{DC} and U_d, which they are synchronous with each other. It is because that the reference value of U_d is k times of U_{DC}, as shown in Fig. 6. Although there is a 2ω voltage ripple with

20V amplitude in U_{DC}, the DLFCR is well reduced in Fig. 16 (b), where I_L represents the mean value of the current i_L. It should be mentioned that the waveform of I_L is achieved by using a second-order low pass filter with a 10kHz cut-off frequency. The signal with frequency lower than 1kHz can pass through this second-order low pass filter without attenuation. Figs. 16 (c) and (d) show the relationship among boost duty cycle D_b, power duty cycle D_p and the voltage U_{DC}, U_d. The boost duty cycle Db reduces with the increment of the voltage U_d, which is conformed to the relation in (13).

The waveforms shown in Figs. 16 (e) – (f) are obtained when the output power is 300W with the proposed control strategy in this paper. The amplitude of ripple voltage with 2ω frequency, about 50V, is larger than that of micro-inverter with 100W power in Figs. 16 (a) – (d). The control strategy regulates two control freedoms (D_b and D_p) with larger ripple for obtaining no DLFCR in the current i_{PV}. From the waveforms shown in 16 (a) – (f) with different output power, it is verified that the proposed control strategy can reduce DLFCR effectively.

The component of DLFCR in I_L is less than 4% of the mean value of I_L from Figs. 16 (b) and (e), which can guarantee that the the output power can exceed 99% of the maximum power of the PV panel [4].

and strategy in this paper is effective to reduce DLFCR.

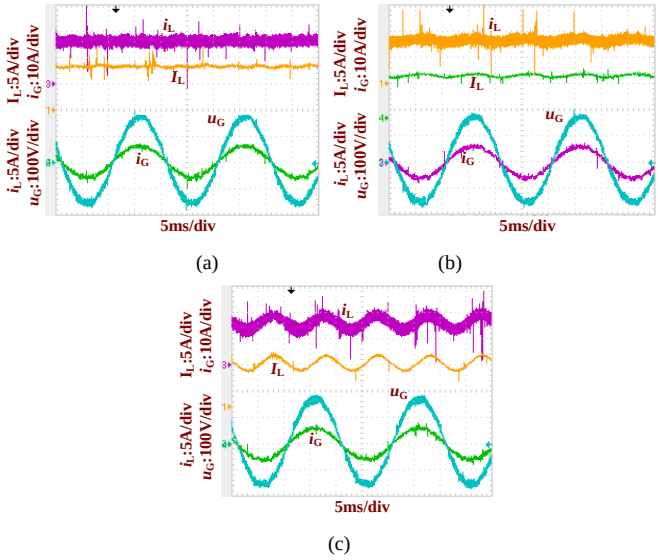


Fig. 17. Performance comparison among different inner-loop strategies. (a) only PIR regulator. (b) PI regulator with LVS voltage link ($1/U_D$). (c) only PI regulator.

In Fig. 8, there are two control links in the inner current loop. One is PIR regulator. The other is LVS voltage link ($1/U_D$ in Fig. 8). In order to verify the function of each control link, the following three controller are adopted, respectively. ① only PIR regulator, ② PI regulator with LVS voltage link ($1/U_D$), and ③ only PI regulator. The waveforms in three conditions are shown in Figs. 17 (a) – (c), respectively. We can see that the waveforms of I_L in three conditions all have DLFCR component. Both of the resonant regulator and LVS voltage link play an important role in DLFCR reduction. Compared with the waveforms of I_L in Figs. 16 (b) and (e) controlled by the proposed strategy, the proposed converter

The output power of the PV panel is determined by the solar irradiance, temperature, etc. So, it is random and difficult to achieve an obvious power change in a short time. In order to observe the MPPT process obviously, a simulation model of the proposed PV microinverter has been established by Matlab/simulink. Fig. 18(a) shows the simulation results of MPPT process when the solar irradiance changes from 1000W/m^2 to 500W/m^2 at 0.2s. The algorithm for MPPT is perturbation and observation (P&O) method, which is a simple and effective method. The perturbation step is 0.5V for the reference of the PV voltage and the perturbation interval is 0.01s. The tansient time is approximate 0.1s after sudden change of the solar irradiance. Fig. 18(b) shows the waveforms of the DC bus voltage, grid voltage and grid current. Although there is a large dual line frequency component in HVS voltage, there is almost no DLFCR in the PV output current and with a satisfactory quality of the grid current.

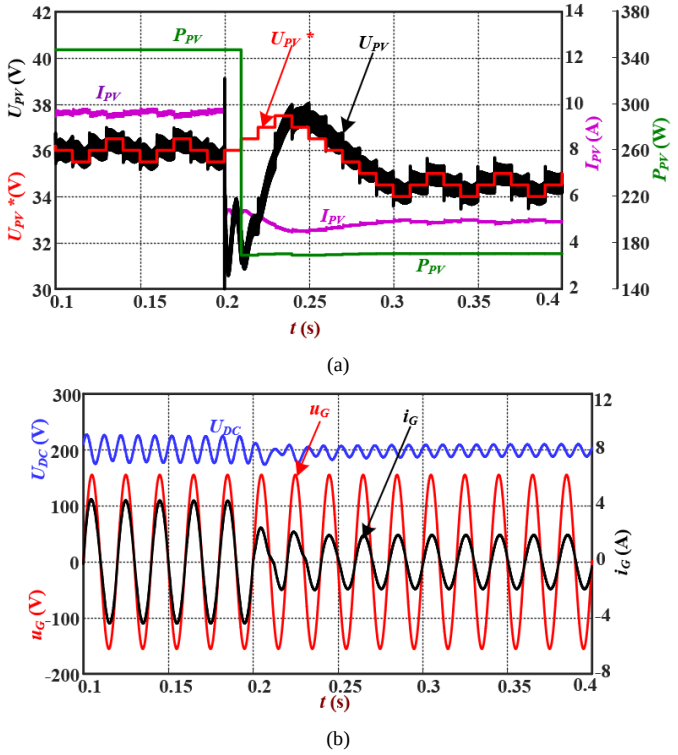


Fig. 18. Simulation results when there is a sudden change of solar irradiance. (a) MPPT process. (b) waveforms of DC bus voltage, grid voltage and grid current.

The efficiency curve is difficult to record accurately because the output power of the PV panel is affected by different factors, such as light irradiance, temperature, etc. Thus, the constant voltage source is adopted as power supply. The curve of input voltage versus power simulates the output characterisitic of the PV panel. The achieved efficiency curve is shown in Fig. 19. The maximum efficiency is 92.6%.

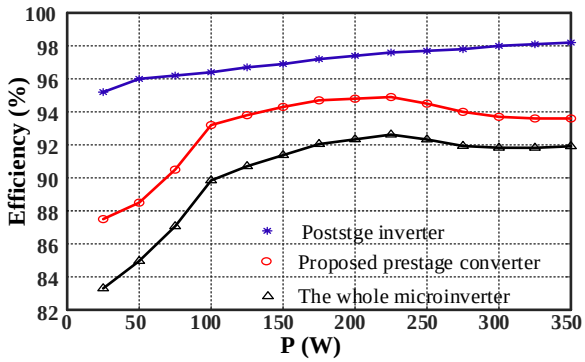


Fig. 19. Efficiency curves of the proposed microinverter.

VI. Conclusion

This paper proposed a current-fed full-bridge converter as the prestage of the PV micro-inverter. A boost converter is integrated into the proposed converter without additional switches. A two-control-freedoms modulation method is presented based on the proposed converter. One freedom is used to control the PV voltage and current, where resonant regulator is employed to reduce DLFCR due to high gain at 2ω frequency. The other freedom is employed to control the LVS voltage vary with the DC bus voltage, which can be realized by a resonant regulator. The current stress of elements can be effectively reduced. The parameters of the regulators in the proposed strategy are designed according to the small-signal model of the proposed converter. The experimental results verify the effectiveness of the proposed converter and corresponding control strategy.

Appendix

State-space equations for the small-signal model of the proposed CF-FBH converter

$$\dot{\tilde{x}} = A\tilde{x} + B\tilde{u} \qquad \text{(A-1)}$$

Where,

$$\tilde{x} = \begin{bmatrix} \tilde{i}_L & \tilde{U}_{PV} & \tilde{U}_d \end{bmatrix}^T \qquad \text{(A-2)}$$

$$\tilde{u} = \begin{bmatrix} \tilde{D}_b & \tilde{D}_p & \tilde{U}_{DC} \end{bmatrix}^T \qquad \text{(A-3)}$$

$$A = \begin{bmatrix} 0 & \frac{1}{L_{dc}} & -\frac{D_b}{L_{dc}} \\ -\frac{1}{C_{PV}} & -\frac{1}{C_{PV}R_{mpp}} & 0 \\ \frac{D_b}{C_d} & 0 & -\frac{T_S D_p^2}{L_r C_d} \end{bmatrix} \qquad \text{(A-4)}$$

$$B = \begin{bmatrix} -\frac{U_d}{L_{dc}} & 0 & 0 \\ 0 & 0 & 0 \\ \frac{i_L}{C_d} & -\frac{(2nU_d - U_{DC})D_p T_S}{nL_r C_d} & \frac{D_p^2 T_S}{2nL_r C_d} \end{bmatrix} \qquad \text{(A-5)}$$

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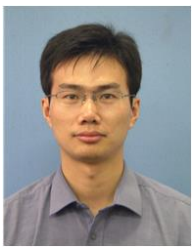

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