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The Influence of ZnO Layer Thickness on the Performance and Electrical Bias Stress Instability in ZnO Thin Film Transistors

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Abstract

Thin Film Transistors (TFTs) are the active elements for future large area electronic applications, in which low cost, low temperature processes and optical transparency are required. Zinc oxide (ZnO) thin film transistors (TFTs) on SiO_2/n+-Si substrate are fabricated with the channel thicknesses ranging from 20 nm to 60 nm. It is found that both the performance and gate bias stress related instabilities of the ZnO TFTs fabricated were influenced by the thickness of ZnO active channel layer. The effective mobility was found to improve with increasing ZnO thickness by up to an order in magnitude within the thickness range investigated (20 – 60 nm). However, thinner films were found to exhibit greater stability in threshold voltage and turn-on voltage shifts with respect to both positive and negative gate bias stress. It was also observed that both the turn on voltage (V_{on}) and the threshold voltage (V_T) decrease with increasing channel thickness. Moreover, the variations in subthreshold slope (S) with ZnO thickness as well as variations in V_T and V_{on} suggest a possible dependence of trap states in the ZnO on the ZnO thickness. This is further correlated by the dependence of V_T and V_{on} instabilities with gate bias stress.

Keywords: zinc oxide, Gate bias stress, RF Sputtering, Performance, Stability, ZnO Thickness

1. INTRODUCTION

Poly-silicon thin film transistors (TFTs) have so far been the main attractive alternative to amorphous silicon TFTs used in large area electronic applications such as in flat panel displays [1, 2]. This has been due to the mobility limitation imposed on amorphous silicon based TFTs. However, both the poly silicon and amorphous silicon TFTs are non-transparent to visible light, thus would limit the aperture ratio of the active matrix arrays in flat panel displays. Semiconducting oxides with large bandgap (transparent to the visible regime, such as ZnO with a bandgap of ~3.37 eV), can be used to fabricate high mobility TFTs (at temperatures lower than that used in poly silicon processes) and offer a way to overcome both the mobility and the transparency issues with improved device stability to light [3-10]. Transparent TFTs, based on ZnO have been demonstrated [4, 5, 7, 1]. These transistors exhibit high channel electron mobility that would lead to higher drive currents and faster device operating speeds (required for high frequency applications).

The source/drain (S/D) series resistance in field effect transistor (FET) devices is often determined as a sum of the source contact resistance (R_S), the drain contact resistance (R_D) and the channel resistance (R_{ch}). As a consequence of the S/D contact resistance, current crowding in the source in the vicinity of the channel gives rise to the spreading

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resistance (R_{sp}). A first order approximation of R_{sp} is often given by the analytical expression (1);

$$R_{sp} = \frac{0.64\rho}{W}\ln\left(\frac{\xi x_j}{x_{ch}}\right) \quad \text{………………..………………… (1)}$$

where W is the channel width, ρ the source-drain resistivity, x_j the junction depth, x_{ch} the channel thickness and ξ is a scaling factor [11, 12]. In physical terms this means that both the doping concentration and the channel thickness can be used to modulate R_{sp} and hence the device performance. ZnO channel thickness has already been reported to be a useful parameter for modulating performance and off-state leakage currents in TFTs [13]. For TFT applications, the channel thickness (d) is related to off-state leakage current ($I_{ds\text{-}off}$) when the gate to source voltage V_{gs} = 0 V, according to equation (2).

$$I_{ds-off} = \frac{\sigma W d}{L} V_{ds} \quad \text{…………………..……..…….. (2)}$$

where σ is the electrical conductivity of the film, V_{ds} is the source to drain voltage, W is the active channel width and L is the channel length.

Despite the advantages offered by ZnO TFTs, threshold voltage (V_T) instability resulting from prolonged application of gate bias is one of the major challenges hindering its eventual integration into large area electronic technology [14, 10, 15]. The purpose of this work is to demonstrate that both performance and gate bias stress related electrical instability in ZnO TFTs can be modulated via thickness optimisation of the ZnO active layer.

2. EXPERIMENTAL

The effect of ZnO thickness on the performance of ZnO TFTs; and gate bias instability is demonstrated by sputtering ZnO layers of varying thicknesses (20 – 60 nm) on thermally grown silicon dioxide (SiO_2) dielectric with identical deposition parameters. The relative dielectric constant of the SiO_2 layer was obtained from capacitance-voltage (CV) data in the saturation region using the semiconductor parameter analyzers HP4192B by Agilent. The source/drain (S/D) electrodes are formed by depositing 100 nm aluminium patterned by shadow masks on the ZnO active channel length of 100 µm, and width/length ratio W/L=10:1. The finished TFT is a bottom-gate (n^+-silicon) inverted staggered configuration as in figure 1.

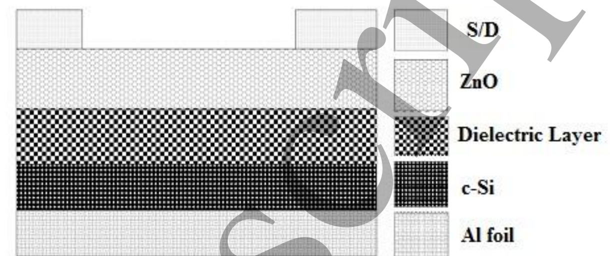

Figure 1 Inverted staggered bottom-gate TFT structure.

Prior to sputtering the ZnO layer, a 100 nm layer of SiO_2 was thermally grown in a Carbolite furnace at a temperature of 950 ^{0}C by the dry oxygen (O_2) process. All the SiO_2 layers used were grown at the same time in order to minimize any variations in the insulator thicknesses and properties. Different ZnO layers were then sputtered onto the SiO_2 layer using a reactive RF magnetron sputtering process (O_2/Ar ratio of 0.025) from a ceramic ZnO target of 99.99 % purity. The ZnO layers were post-treated with O_2 in vacuum (0.2 mTorr) for 30 minutes prior to breaking the vacuum to improve the film crystallites and its electrical stability in air [6]. The sputtering process was performed under room temperature conditions with no intentional heating. Film thicknesses were measured using a Rudolph AutoEL-III ellipsometer equipped with a 633.2 nm helium-neon (HeNe) laser at an incident angle of 70^0. The thickness orders were confirmed by measurements obtained from surface profilometry using a Tencor Alpha Step 200 profilometer. The current-voltage (IV) characteristics were measured using an Agilent HP4140B pico ammeter. The stability of the devices were investigated under gate bias stress of ±10 V (corresponding to a field of 1 MV/cm for a 100 µm thick dielectric layer) for a maximum stress time of 10^4 s. All measurements were performed at room temperature in the dark.

3. RESULTS AND DISCUSSION

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ZnO TFTs fabricated using the sputtered ZnO layers produced in this work exhibited the following characteristics (see table 1).

TABLE 1

PERFORMANCE DATA OF ZNO TFTS ACROSS DIFFERENT ZNO THICKNESSES

ZnO thickness (nm)	**μ_{eff} (cm^2/V.s)**	**V_T (V)**	**V_{on} (V)**	**I_{on-off}**	**S (V/dec)**
20	0.4	23.3	8.3	1.4×10^7	1.4
25	2.0	22.7	2.0	1.2×10^6	1.7
35	4.0	21.4	1.0	1.2×10^7	0.9
40	7.0	18.7	-4.5	1.6×10^6	0.9
50	9.0	20.0	-5.3	2.0×10^5	2.5
60	10.9	18.5	-9.1	5.1×10^5	3.8

The threshold voltage (V_T) and the effective mobility (μ_{eff}) were derived from a linear fit to a plot of drain current (I_{ds}) versus gate to source voltage (V_{gs}) in the linear region with V_{ds} = 2 V($where\ V_{ds} << (V_{gs} - V_T)$), according to the expression:

$$I_{ds} = \mu_{eff}\frac{W}{L}C_{ins}(V_{gs} - V_T)V_{ds} \quad \text{.....................} (3)$$

where $C_{ins} = \frac{\varepsilon_0 \varepsilon_{SiO_2}}{t_{SiO_2}}$ is the capacitance per unit area of the gate insulator, and W and L are the channel width and length respectively. The remaining parameters ε_0, ε_{SiO_2} and t_{SiO_2} represent the permittivity in free space, the relative permittivity of SiO_2 and the thickness of SiO_2 respectively. In this work, ε_{SiO_2} was obtained from the CV measurement to be 3.9.

The turn-on voltage (V_{on}) is extracted as the gate voltage at which the drain current just begins to increase monotonically with increasing gate voltage, and corresponds to the minimum current on the semi log plot of I_{ds} versus V_{gs}. Using these parameters, the shifts $\Delta\mu_{eff}$, ΔV_T and ΔV_{on} are calculated using the following relations (4a – 4c).

$$\Delta\mu_{eff} = \mu_{eff}(t) - \mu_{eff}(t = 0) \quad \text{.................} (4a)$$

$$V_T = V_T(t) - V_T(t = 0) \quad \text{.........................} (4b)$$

$$V_{on} = V_{on}(t) - V_{on}(t = 0) \quad \text{.......................} (4c)$$

where, $\mu_{eff}(t)$, $V_T(t)$ and $V_{on}(t)$ are the effective mobility, threshold voltage and turn-on voltages of the TFT after a stress bias time of t seconds respectively. The initial values of the parameters prior to the application of the gate bias stress correspond to $t = 0\ seconds$.

Typical output and transfer characteristics of the finished ZnO TFTs are shown in figure 2 and 3 respectively. In figure 3, a voltage sweep from -30 V to +30 V and back presents a hysteresis of about 1 V. This suggests the dielectric layer used is of good quality. From table 1, the subthreshold slope (S) for these devices ranges between 0.9 V/dec and 3.8 V/dec. The thickest film (60 nm) exhibited the largest value of S, which was more than double the value observed for the thinnest ZnO film (20 nm). The value of S is indicative of the trap density (N_t) at or near the interface between the ZnO semiconductor and gate dielectric material. Moreover, the variations in S with ZnO thickness as well as variations in V_T and V_{on} (see figures 6(b) and 6(c)) is an indication that interface traps may depend on the ZnO thickness. The total density of states present at all interfaces in the semiconductor N_t is estimated using equation (5) [16].

$$N_t = \left[\frac{S\log_{10}(e)}{kT/q} - 1\right](C_{ins}/q) \quad \text{.....................} (5)$$

where k is the Boltzmann's constant, T is the measurement temperature, q the elemental electron charge, S the subthreshold slope, and C_{ins} the capacitance of the dielectric layer.

It is also observed from table 1 that the thicker films presented superior performance with respect to the effective mobility even though a poorer subthreshold slope value is observed for the 50 nm film (the thickest). One may therefore speculate that traps states at the ZnO/insulator interface may not be responsible for the large values of S observed in thicker films. It is worth noting that all ZnO

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active layers used in this work were exposed to oxygen (O_2) post-deposition treatment for 30 minutes prior to breaking the vacuum. Therefore the conductivities of the films at the top surface are modified by chemisorbed O_2 [17, 18]. O_2 chemisorption have been reported to degrade effective mobility in ZnO TFTs as well as shifting V_T to more positive values [19]. On the average in this work, thinner films were observed to have larger values of V_T. Although the effective mobility is observed to improve with film thickness. The effect of O_2 chemisorption can be considered to be contant on all films as the post-deposition procedure was exactly the same for all films. One may therefore attribute the variations observed in V_T and μ_{eff} to the dominance effect of the top surface due to O_2 chemisorption on thinner films. As seen from table 1, V_{on} values are more positive with decreasing ZnO layer thickness. This may be attributed to the fact that the negatively charged chemisorbed O_2 species on the top surface deplete the ZnO layer of carriers during the adsorption process [18, 20]. The magnitude of the electric field created by these charged species at the ZnO/insulator interface is inversely proportional to the ZnO thickness. This is in agreement with thickness dependencies exhibited by the effective mobility as a result of reduced scattering from the electric field resulting from the chemisorption in thicker films.

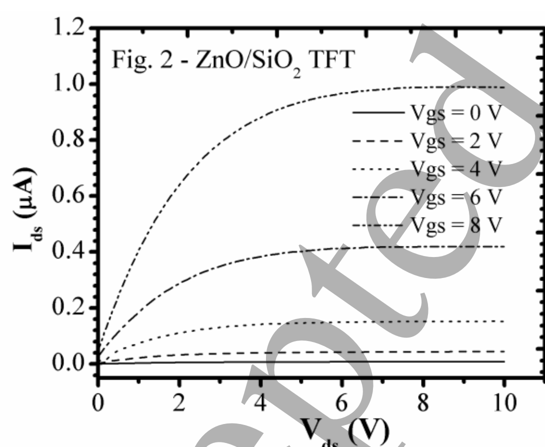

Figure 2 Typical output characteristic of a TFT incorporating a 40 nm thick active layer, clearly illustrating transistor action.

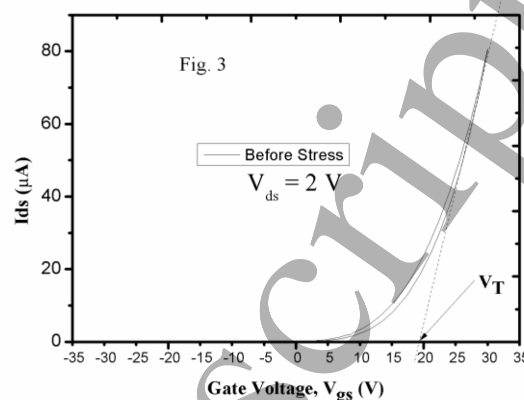

Figure 3 Typical voltage sweep transfer characteristic of a TFT incorporating a 40 nm thick active layer, indicating the threshold voltage.

One clearly sees from table 1 that within the thickness range studied, the effective channel mobility (μ_{eff}) exhibits a general increase with thickness (figure 4). This is similar to observations reported for undoped ZnO and other ZnO derivatives, hydrogenated amorphous silicon (a-Si:H) TFTs [21, 22]. In addition, turn-on voltage (V_{On}) and V_T are observed to decrease monotonically with increasing thickness (figure 5). These relationships could be ascribed to a stronger effect of chemisorbed O_2 [19] on the ZnO top surface with decreasing film thickness. All these will likely affect the performance of the TFT device.

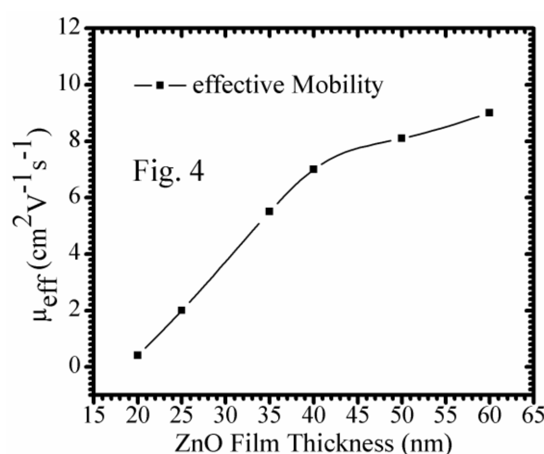

Figure 4 The variation of μ_{eff} with ZnO layer thickness.

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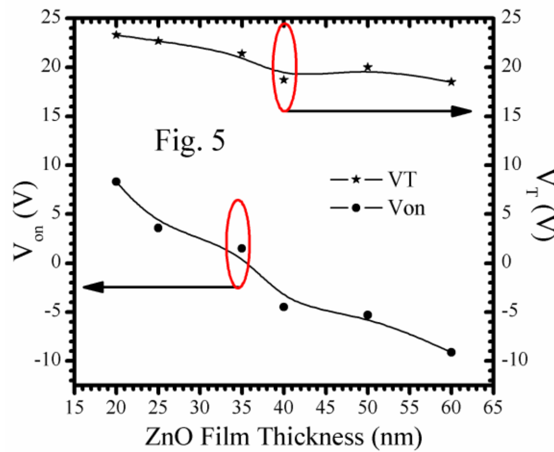

Figure 5 The variation of V_T and V_{on} with ZnO layer thickness.

On application of a +10 V or -10 V gate bias stress to the devices, it can be observed that the active layer thickness also affects the electrical stability of the ZnO TFT (figure 6). In general, it is observed that an application of a gate bias stress on the ZnO/SiO_2 TFTs results in variations in μ_{eff}, V_T and V_{on}. An application of a positive gate bias stress moves the transfer characteristic curve to the right whereas a negative bias shifts the curve to the left (figure 7). Other authors have attributed such behaviours to charge trapping and detrapping at or near the semiconductor/dielectric interface as well as defects creation at longer stress times [19, 23, 24]. However, the fact that $I_{ds\text{-}off}$ is not enhanced by this instability suggest charge creation is not likely to be a significant effect. The shifts in $\Delta\mu_{eff}$, ΔV_T and ΔV_{on} following a positive gate bias stress are shown in figure 7 for stresses up to a maximum of 10^4s. The gate bias stress was performed using stress time intervals of: 0, 10^1,10^2, 10^3 and 10^4 seconds. Similar behaviour has been reported in yttrium and tungsten doped ZnO TFTs and was dependent on doping concentration [25, 26]. We observed that the shifted characteristics curves returned freely to their original positions after relaxation time of 4 hours in air at room temperature following a 10^4 seconds stress time. This suggests that charge trapping at or near the interface in the semiconductor is the dominant mechanism responsible for the instability [27].

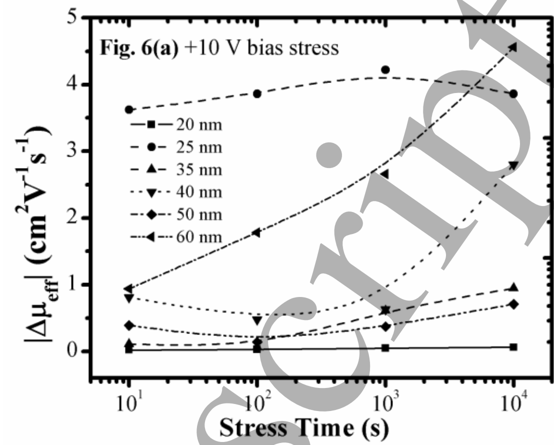

Figure 6(a) Variation of effective mobility as a function of gate stress time parameterised for different ZnO thicknesses (20 – 60 nm).

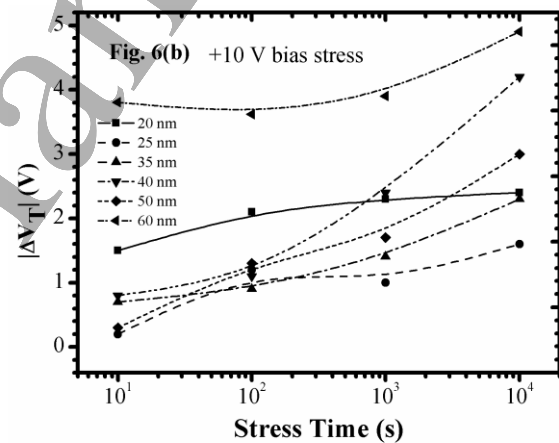

Figure 6(b) Variations of threshold voltage as a function of gate stress bias time parameterised for different ZnO thicknesses (20 – 60 nm).

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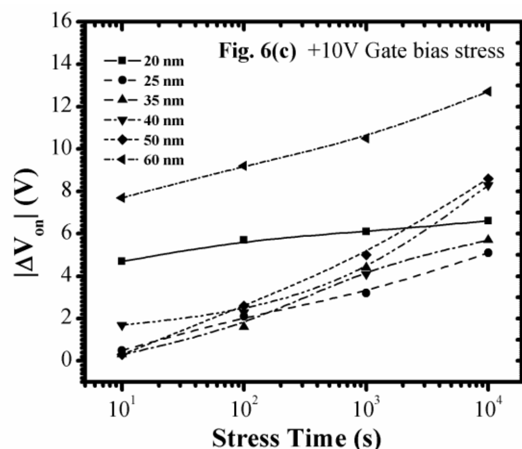

Figure 6(c) Variations of turn-on voltage as a function of gate bias stress time parameterised for different ZnO thicknesses (20 – 60 nm).

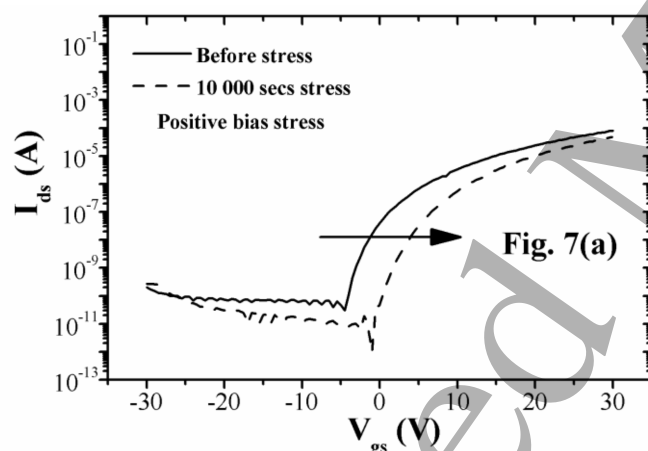

Figure 7(a) Typical instability in SiO2 based ZnO TFT as a result of positive and negative bias stress showing the shift in the transfer characteristics following positive gate bias stress.

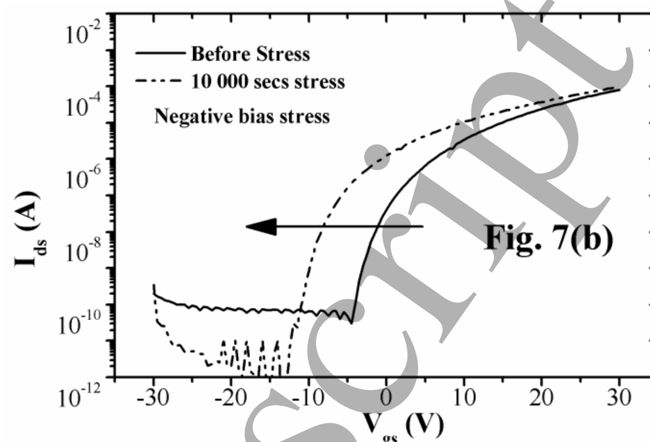

Figure 7(b) Typical instability in SiO2 based ZnO TFT as a result of positive and negative bias stress showing the shift in the transfer characteristics following negative gate bias stress.

4. CONCLUSION

It has been shown that ZnO TFT performance parameters (μ_{eff}, V_T and V_{On}) are affected by ZnO active layer thickness. It is suggested in this work that O_2 adsorption at the ZnO top surface results in a carrier depletion that has a strong effect on the device performance. Also, the dependence of V_T on channel thickness would lead one to speculate that TFTs optimised to operate at low V_T are likely to be more stable during prolong operation. This can be attributed to reduced gate bias stressing effect at low operational voltages. It is also observed that for all three parameters (μ_{eff}, V_T and V_{On}) studied in this work, greater instability as a result of gate bias stress is exhibit by thicker ZnO films.

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References

[1] Song I and Han M 2003 Current Applied Physics **3** 363

[2] Kim J, Sim Y, Cho Y, Seo J, Kwon S, Park J, Choi H, Kim H and Lee S 2009 Microelectronic Engineering **86** 2427

[3] Bang S, Lee S, Park J, Park S and Jeon H 2011 Thin Solid Films **519** 8109

[4] Jiang L, Huang K, Li J, L. S, Gao Y, T. W, Guo X, Wang J, Mei T and Wang X 2018 Ceramics International **44** 11751

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[5] Kumar M, Jeong H and Lee D 2018 Superlattices and Microstructures **120** 395

[6] Ngwashi D, Cross R and Paul S 2010 Materials Research Society Symposium Proceedings **1201** H05

[7] Ngwashi D, Cross R., Paul S, Andrian P and Anjana D 2011 Mater.ials Research Society Symposium Proceedings **1315** 71

[8] Vyas S, Dwivedi A and Dwivedi R 2018 Superlattices and Microstructures **120** 223

[9] Walker B, Pradhan A and Xiao B 2015 Solid-State Electronics **111** 58

[10] R. Wang, S. Wu, Li X and Zhang J 2017 Solid-State Electronics **133** 6

[11] D. K. Schroeder, Semiconductor Material and Device Characterization, Second ed., John Willeys & Sons, Inc, 1998.

[12] T. Yaun and T. H. Ning, Fundamentals of Modern VLSI Devices, Cambridge University Press, 2002.

[13] Chung J, Lee J, Kim H, Jang N and Kim J 2008 Thin Solid Films **516** 5597

[14] Park S, Cho E and Yun I 2012 Microelectronics Reliability **52** 2215

[15] Xu P and Yao R 2018 Displays **53** 14

[16] Ralland A, Richard J, Kleider J and Mencaraglia D 1993 Journal of Electrochemical Society **140** 3679

[17] D. H. Zhang 1996 Materials Chemistry and Physics **45** 248-252

[18] Mirkhani V, Yapabandara K, Wang S., Khanal M P, Uprety S, Sultan M S, Ozden B, Ahyi A. C., Hamilton M C, Sk M H and Park M 2019 Thin Solid Films **672** 152-156

[19] Yapabandara K, Mirkhani V, Sultan M S, Ozden B, Khanal M P and Minseo P 2017 Journal of Vacuum Science B **35** 03D104

[20] Lagowski J. , Sproles E. S. and G. H. C. 1977 Journal of Applied Physics **48**

[21] Kishimoto S, Yamamoto T, Nakagawa Y, Ikeda K, Makino H and Yamada T 2006 Superlattices and Microstructures **39** 306

[22] Bouderbala M, Hamzaoui S, Amrani B, Reshak A, Adnane M, Sahraoui T and Zerdali M 2008 Physica B: Condensed Matter **403** 3326

[23] Cross R. B. M. and De Souza M. M. 2006 Applied Physics Letters **89** 263513

[24] Furuta M, Kamada1 Y, Hiramatsu T, Li C, Kimura M, Fujita1 S and Hirao T 2011 Japanese Journal of Applied Physics **50** 03CB09

[25] Abliz A, Xu L, Wan D, Duan H, Wang J, Wang C, Luo S and Liu C 2019 Applied Surface Science **475** 565

[26] Abliz A, Wan D, Yang L, Mamat M, Chen H, Xu L, Wang C and Duan H 2019 Materials Science in Semiconductor Processing **95** 54

[27] Yurong L, Shufeng M and Ruohe Y 2014 Journal of Vacuum Science B **32** 061208

Accepted Manuscript