Structure and realization of pole-shared switched-current complex wavelet filter

Wenshan Zhao • Yigang He • Yichuang Sun

Abstract A pole-shared switched-current complex wavelet filter structure with follow-the-leader feedback configuration is proposed for synthesizing the real and imaginary approximation functions with the same poles. The double-sampling fully-balanced SI bilinear integrator and current mirror are employed as the building cells. By sharing the implementation circuit for approximation poles of the real and the imaginary part, the proposed structure only has the same circuit complexity as that of real-valued wavelet filter, which is very suitable for small-size and low-power application. The complex Morlet wavelet is selected as an example to elaborate the design procedure. Simulation results confirm that the presented complex wavelet filter structure can generate the real and imaginary coefficients of complex wavelet transform accurately with simple synthesis method and explicit design formulas.

Keywords Switched-current filter • Complex wavelet transform • Bilinear integrator • Double-sampling fully-balanced • Follow-the-leader feedback configuration

1 Introduction

Complex wavelet transform (CWT) has been proven to be a powerful tool in transient signal detection, due to its ability to provide modulus and phase information [1,2]. To achieve real-time performance and low power consumption, analog implementation of CWT has been proposed, mainly involving the design of analog complex wavelet filter (ACWF) and modulus/phase computing circuit [3]. As the first stage of CWT circuit, ACWF generates the real and imaginary coefficients, which plays an important role in modulus and phase computation. Theoretically, CWT is equivalent to two real-valued wavelet transforms, which are operated in the real and the imaginary part respectively [2]. Thus, ACWF can be realized by using two analog real-valued wavelet filters (ARVWFs), but this leads to large chip size and high power dissipation. To overcome this problem, [3] proposed a pole-shared approximation method to make the rational approximations for the real and imaginary parts of complex wavelet base have the same poles, based on which the ARVWFs designed for the real and imaginary parts can share the implementation circuits for the poles.

This Letter aims to propose a complex wavelet filter structure to synthesize the pole-shared rational approximation functions obtained by [3]. The switched-current (SI) circuit is employed to construct the pole-shared structure and design formulas are derived.

2 Design strategies for complex wavelet filter structure

Assuming $\psi(t)$ is the complex wavelet base, the CWT of the signal $f(t)$ at scale a and time-shift τ is given by

$$\begin{aligned} WT_f(a,\tau) &= \frac{1}{\sqrt{a}}\int f(t)\psi^*\left(\frac{t-\tau}{a}\right)dt \\ &= \frac{1}{\sqrt{a}}\int f(t)\psi_r\left(\frac{t-\tau}{a}\right)dt - i\frac{1}{\sqrt{a}}\int f(t)\psi_i\left(\frac{t-\tau}{a}\right)dt \end{aligned} \quad (1)$$

where $\psi_r(t)$ and $\psi_i(t)$ are the real and imaginary parts of $\psi(t)$ respectively.

According to the definition of convolution, (1) can also be expressed as

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$$WT_f(a,\tau) = f(\tau) \otimes \frac{1}{\sqrt{a}} \psi^*(\frac{-\tau}{a}) = [f(\tau) \otimes \frac{1}{\sqrt{a}} \psi_r(\frac{-\tau}{a})] - i[f(\tau) \otimes \frac{1}{\sqrt{a}} \psi_i(\frac{-\tau}{a})] \quad (2)$$

Observed from (2), CWT uses complex-valued filter (essentially composed of two real-valued filters) to decompose the signal into real and imaginary parts. Consequently, the implementation method for ACWF can be derived from ARVWF design, i.e. mathematically approximate the complex wavelet base in the real and the imaginary part with realizable rational expression respectively, and then implement these two rational approximation functions using suitable circuit topologies. So far, several approximation algorithms for ARVWF design have been proposed [4-11], which can be used directly to obtain the rational approximations to the real and the imaginary part of complex wavelet base respectively. However, this conventional approximation method will yield two rational functions with different poles and zeros, and thus two totally different implementation circuits. This characteristic is indeed unsuited for small-sized and low-power application, since ARVWF is normally the high-order system and thus its double size will greatly enhance the overall circuit complexity. To resolve above problem, [3] presented a novel approximation method to make these two rational functions have the same poles, the so-called "pole-shared" approximation. Then, the ARVWFs designed for the real and imaginary parts can share the implementation circuits for poles, which will greatly lower the circuit complexity.

Herein, this Letter mainly focuses on the design of pole-shared filter structure to synthesize the pole-shared rational approximation functions derived from [3]. To minimize circuit complexity while keeping a guaranteed performance, the following design strategies should be taken into account.

First, ACWF's performance relies on the analogue circuit techniques. To date, log-domain circuit has been employed in ACWF design [3]. Although successful in many aspects, log-domain filter needs on-chip tuning since it is difficult to fabricate the time constant accurately in the IC processes. SI filter does not have this problem because its time constant depends on the MOSFET aspect ratio [12]. Also, SI circuit can overcome the bottleneck encountered by its predecessor switched-capacitor circuit, e.g. incompatibility with digital VLSI technology. Therefore, SI technique becomes obvious choice for our purpose.

Second, ACWF's performance also depends strongly on the filter structure. Generally, any SI filter structure can be used in ACWF construction. However, for the purpose of sharing poles implementation circuits, the SI filter structure employed for synthesizing the rational approximations to the real and imaginary parts should have a special characteristic, that is, the implementation circuits for the denominator and numerator of the rational function should be independently controllable. Among all the existing SI filter architectures [5-7,10,11,13], the follow-the-leader feedback (FLF) multiple loop feedback (MLF) SI filter structure [10,13] is well suitable for pole-shared ACWF design, since the denominator coefficients (or poles) are controlled by the feedback weights, and separately the numerator coefficients (or zeros) are adjusted by the output weights. Hence, for synthesizing the pole-shared rational functions with FLF SI filter structure, the implementation circuits can share the SI integrator cores and feedback network. Furthermore, FLF filter structure has low magnitude sensitivity, which would provide a strong potential for high-quality ACWF design.

With regard to all the considerations discussed above, the FLF SI filter structure is utilized to construct a pole-shared ACWF.

3 Proposed pole-shared SI complex wavelet filter

3.1 Filter structure

In this Letter, SI integrator is selected as the building cell in ACWF design. Fig. 1 shows the employed double-sampling fully-balanced SI bilinear integrator (BI) operated with two non-overlapping phase ϕ_1 and ϕ_2 [13], whose four pairs of balanced outputs are realized by adding more output transistors with certain integrator coefficients. Black box M_i generally can be implemented by any elementary current memory, which samples input current on phase ϕ_i and sustains on the next phase. The operation of double-sampling makes BI cell sample and output signals on both phase ϕ_1 and ϕ_2, which will halve the clock frequency and introduce several superiorities [13].

Denoting $i_x=i_x^+=-i_x^-$ (x= c, f, r or m), the outputs in Fig. 1 have the relation [13]

$$i_c(z)/c = i_f(z)/f = i_r(z)/r = i_m(z)/m = \frac{1+z^{-1}}{1-z^{-1}} i(z) \quad (3)$$

where coefficients c, f, r and m are defined by the current mirror ratios between the transistors in the integrator core and those at the outputs.

Fig. 2 gives the proposed double-sampling fully-balanced pole-shared SI ACWF structure based on FLF configuration. The balanced signals $i_c^{\pm}$, $i_f^{\pm}$, $i_r^{\pm}$ and $i_m^{\pm}$ represent the forward, feedback, real output and imaginary output branch, respectively. The balanced output signals $i_{or}^{\pm}$ and $i_{om}^{\pm}$ represent the real and imaginary coefficients generated by ACWF, respectively.

In Fig. 2, a current mirror (CM) with coefficient c_0 is introduced at the input terminal of BI_1 to make circuit design more flexible and realizable [13]. Fig.3 illustrates the structure of CM cell, whose transfer function can be expressed as $i_c(z)=ci(z)$.

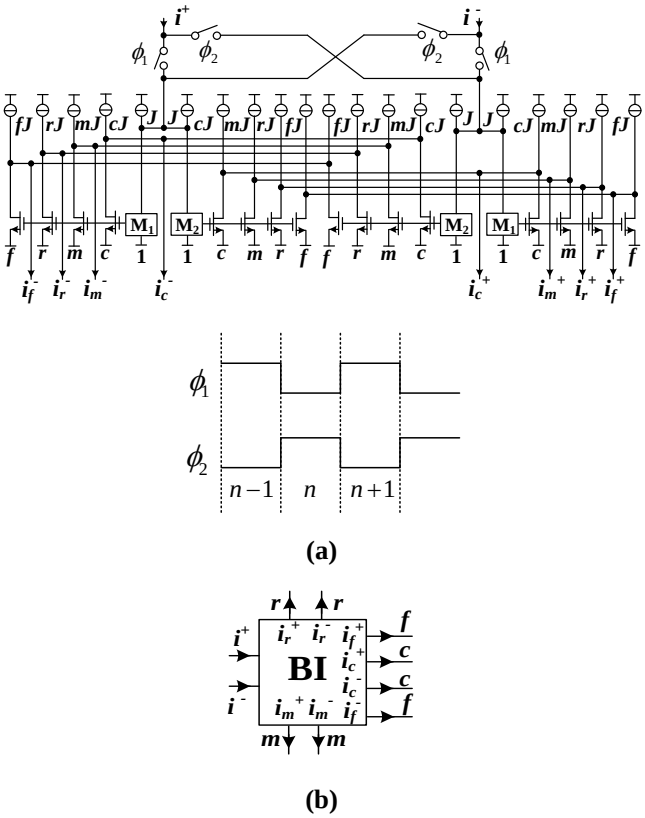


Fig. 1 Double-sampling fully-balanced SI bilinear integrator ***a*** circuit diagram and clock waveforms, ***b*** symbol

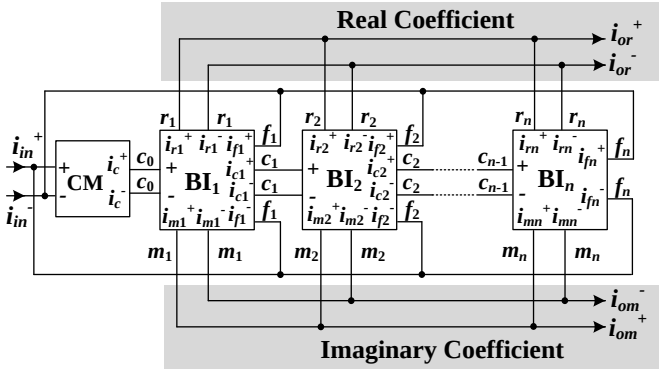


Fig. 2 Pole-shared SI complex wavelet filter structure

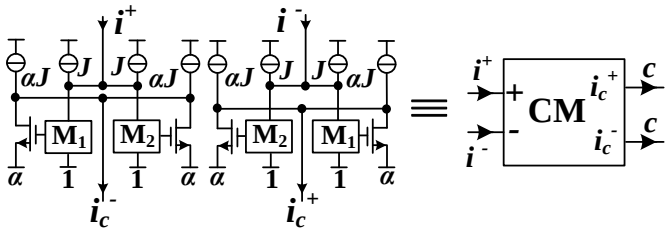


Fig. 3 Double-sampling fully-balanced SI current mirror

3.2 Filter synthesis and design formulas

Observed from Fig.2, the imaginary output $i_{om}^{\pm}$ is realized by adding two pairs of output transistors with integrator coefficient m in each BI cell of the real-valued FLF SI structure presented in [13]. Therefore, conducting similar deduction as [13], the transfer functions for real and imaginary output in Fig. 2 can be written as

$$H_r(z)=\frac{i_{or}(z)}{i_{in}(z)}=\frac{r_1c_0D(z)+r_2c_0c_1D^2(z)+\cdots+r_n\prod_{j=0}^{n-1}c_jD^n(z)}{1+f_1c_0D(z)+f_2c_0c_1D^2(z)+\cdots+f_n\prod_{j=0}^{n-1}c_jD^n(z)} \quad (4)$$

$$H_m(z)=\frac{i_{om}(z)}{i_{in}(z)}=\frac{m_1c_0D(z)+m_2c_0c_1D^2(z)+\cdots+m_n\prod_{j=0}^{n-1}c_jD^n(z)}{1+f_1c_0D(z)+f_2c_0c_1D^2(z)+\cdots+f_n\prod_{j=0}^{n-1}c_jD^n(z)} \quad (5)$$

where $D(z)=(1+z^{-1})/(1-z^{-1})$.

Meanwhile, the pole-shared approximation functions to the real and imaginary parts of complex wavelet base generally have the form of

$$H_{real}(s)=\frac{A_{r(n-1)}s^{n-1}+A_{r(n-2)}s^{n-2}+\cdots+A_{r1}s^1+A_{r0}}{s^n+B_{n-1}s^{n-1}+\cdots+B_1s+B_0} \quad (6)$$

$$H_{imag}(s)=\frac{A_{m(n-1)}s^{n-1}+A_{m(n-2)}s^{n-2}+\cdots+A_{m1}s^1+A_{m0}}{s^n+B_{n-1}s^{n-1}+\cdots+B_1s+B_0} \quad (7)$$

Applying bilinear transform $s=(2/T_s)(1/D(z))$ to (6) and (7), we have

$$H_{dr}(z)=\frac{A_{r(n-1)}\frac{T_s}{2}D(z)+A_{r(n-2)}(\frac{T_s}{2})^2D^2(z)+\cdots+A_{r0}(\frac{T_s}{2})^nD^n(z)}{1+B_{n-1}\frac{T_s}{2}D(z)+B_{n-2}(\frac{T_s}{2})^2D^2(z)+\cdots+B_0(\frac{T_s}{2})^nD^n(z)} \quad (8)$$

$$H_{dm}(z)=\frac{A_{m(n-1)}\frac{T_s}{2}D(z)+A_{m(n-2)}(\frac{T_s}{2})^2D^2(z)+\cdots+A_{m0}(\frac{T_s}{2})^nD^n(z)}{1+B_{n-1}\frac{T_s}{2}D(z)+B_{n-2}(\frac{T_s}{2})^2D^2(z)+\cdots+B_0(\frac{T_s}{2})^nD^n(z)} \quad (9)$$

where T_s is the sampling interval.

Using coefficient matching between (4) and (8), and (5) and

(9), the design formulas for the parameters in Fig. 2 can be determined as

$$r_i = \frac{A_{r(n-i)}}{\prod_{j=0}^{i-1} c_j}\left(\frac{T_s}{2}\right)^i,\ \ m_i = \frac{A_{m(n-i)}}{\prod_{j=0}^{i-1} c_j}\left(\frac{T_s}{2}\right)^i,\ \ f_i = \frac{B_{n-i}}{\prod_{j=0}^{i-1} c_j}\left(\frac{T_s}{2}\right)^i,\ \ (i=1,2,\cdots,n) \tag{10}$$

Obviously, by presetting c_i to be a reasonable value, parameters r_i, m_i and f_i can be easily obtained. Hereby, c_i is normally selected to be the decimal fraction to enhance common-mode rejection [13]. Some advantages of the proposed structure are listed as below:

First, the proposed structure for ACWF almost has the same circuit complexity as that of ARVWF. For certain c_i, the shared denominator coefficients B_i are only controlled by f_i. Therefore, the implementation circuits for the poles in (6) and (7) can share the integrator cores, forward and feedback branches as shown in Fig 2. Meanwhile, the numerator coefficients A_{ri} and A_{mi} are independently controlled by r_i and m_i, which means the zeros in (6) and (7) can be realized by the real and the imaginary output branch, respectively. Thus, for the nth-order pole-shared approximation functions as (6) and (7), the imaginary output can be realized by adding only $2n$ pairs of output transistors in ARVWF, which only takes up a small part of the filter structure.

Second, the proposed structure can synthesize arbitrary pole-shared approximation function, with simple and explicit design formulas. For certain c_i, parameters r_i, m_i and f_i can be used to realize coefficients A_{ri}, A_{mi} and B_i based on (10), in which negative r_i (or m_i) can be simply realized by interchanging the related two output terminals with coefficient r_i (or m_i) of BI_i. When $A_{r(n-i)}$ or $A_{m(n-i)}$ is lacunary, r_i or m_i will be calculated as zero, then the related output terminals of BI_i should be removed.

Third, compared with single-ended FLF configuration [10], fully-balanced structure can realize signal inversion simply by interchanging the two output terminals of SI integrator without introducing excess phase errors, a feature that is particularly attractive in bilinear transform [13].

4 Design example

The proposed structure is suitable for any complex wavelets due to the generality of the MLF architecture. Herein, for brevity, the complex Morlet wavelet is selected as an example to illustrate the design procedure, which can be defined as the complex sinusoidal wave modulated by Gaussian function [14], i.e.

$$\psi_{cmor}(t) = e^{j\omega_0 t} e^{-t^2/f_b} \tag{11}$$

The parameters f_b and ω_0 in (11) denotes the bandwidth and wavelet center frequency, respectively. To obtain a true wavelet characterized as zero integral, ω_0 is usually made large enough in practice. For this example, f_b=2 and ω_0=6. Meanwhile, to facilitate physical hardware implementation, a time delay t_0 should be introduced to make complex Morlet wavelet casual. Hereby, t_0=3 is selected.

Based on the pole-shared method proposed in [3], the eighth-order rational approximation functions to complex Morlet wavelet can be determined, whose numerator and denominator coefficients in (6) and (7) are shown as Table 1.

Normally, the center frequency f_o of wavelet filter should be denormalized to specified value in order to perform wavelet analysis at certain scale. In this Letter, the center frequency of 10 kHz and sampling frequency of 100 kHz are selected as an example. Also, to avoid the nonlinear frequency distortion brought by bilinear transform, f_o should be pre-warped to 10.343 kHz calculated by $f_p=(f_s/\pi)\tan(\pi f_o/f_s)$, where f_p and f_s are the pre-warped center and sampling frequency respectively [12].

Setting $c_0=c_1=c_5=c_6$=0.1, $c_2=c_3$=0.6, $c_4=c_7$=0.3, the circuit parameters in Fig.2 can be determined by (10), which are listed in Table 2. Fig. 4 illustrates the structure of designed SI complex Morlet wavelet filter derived from Fig.2, in which the second generation SI memory cell is employed on the purpose of testifying the feasibility of proposed structure.

Table 1 Coefficients of pole-shared rational approximations to complex Morlet wavelet

i	0	1	2	3	4	5	6	7
A_{ri}	-1.6174e4	-1.3399e3	-169.5821	-430.3728	48.1897	-9.5038	0.5512	-0.0376
A_{mi}	-1.3581e4	5.7199e3	-2.1537e3	316.5315	-28.9016	-0.5890	0.1092	-0.0428
B_i	1.5006e6	1.8697e5	1.9288e5	1.6639e4	8.5534e3	464.3558	156.3425	4.0841

Table 2 Parameters of pole-shared SI complex Morlet wavelet filter

i	1	2	3	4	5	6	7	8
γ_i	-0.0203	0.1600	-0.2476	0.1127	-0.1807	-0.0384	-0.1633	-0.3539
m_i	-0.0230	0.0317	-0.0153	-0.0676	0.1329	-0.4872	0.6970	-0.2972
f_i	2.2000	45.3656	12.0969	20.0050	6.9878	43.6324	22.7834	32.8346

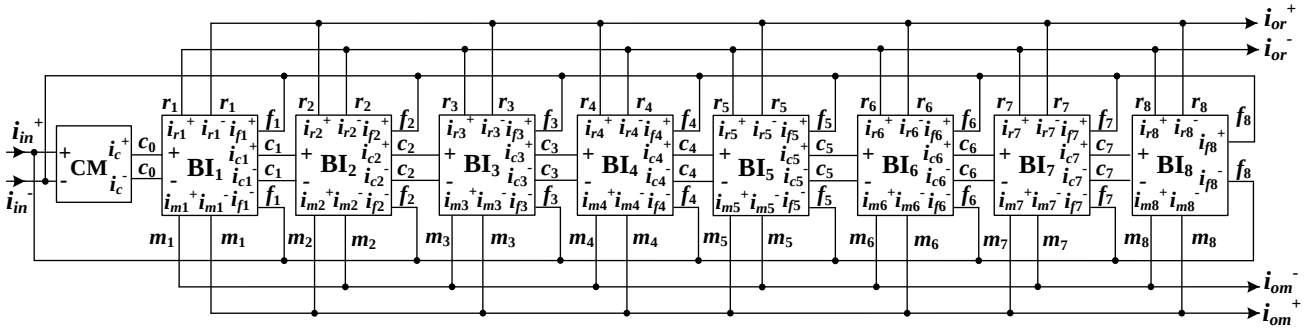
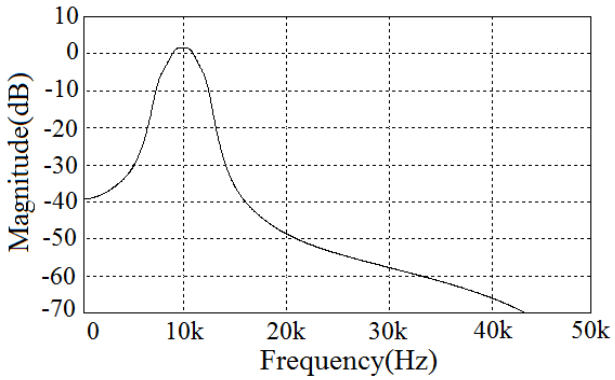


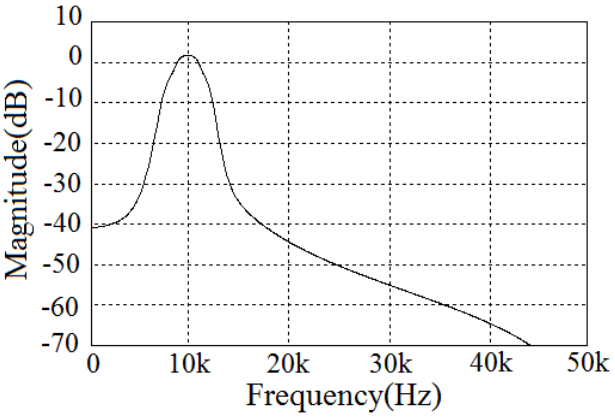
Fig. 4 Structure of SI complex Morlet wavelet filter

Fig. 5 shows the frequency response of complex Morlet wavelet filter simulated by ASIZ [15]. Observed from Fig. 5a, the real output of ACWF achieves peak value at center frequency 9.8 kHz. The lower and upper cutoff frequencies are 8.6 kHz and 11.2 kHz respectively, slightly different from ideal values, i.e. 8.4 kHz and 11.1 kHz. Meanwhile, Fig. 5b plots the imaginary output of ACWF, achieving peak value at center frequency 10.1 kHz. The measured lower and upper cutoff frequencies are 8.6 kHz and 11.2 kHz respectively, almost the same as should be close to, i.e. 8.4 kHz and 11.1 kHz. Fig. 6 gives the impulse response of designed complex Morlet wavelet filter at f_s=100 kHz.

To testify the feasible application of the generated real and imaginary coefficients in the next stage of modulus and phase computation, Fig.7 plots the modulus and phase responses of complex Morlet wavelet filter calculated from the data in Fig.6 by using Matlab. Apparently, the approximated modulus and phase are close to the ideal cases. The time-delay of modulus response in Fig. 7a is due to the sample-and-hold operation of SI technique. The approximation error of phase response in Fig. 7b in the range of 0-0.05ms and 0.55-0.65ms is mainly caused by the non-ideality of rational approximation functions as shown in Table 1, whose phase response illustrated in Fig. 8 gives a clue. A high-performance pole-shared approximation method needs to be proposed to resolve above problem, but it is beyond the scope of this Letter and left to the future work.

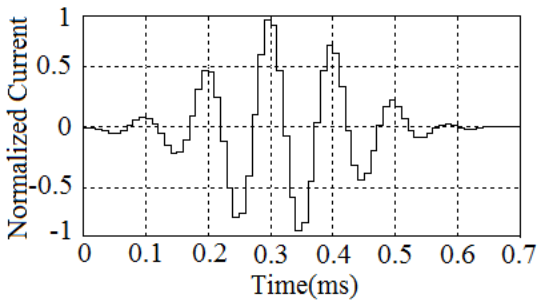


(a)

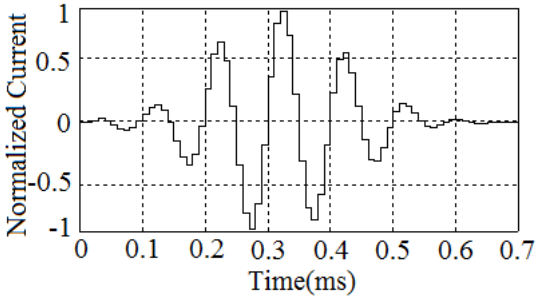


(b)

Fig.5 Frequency response of complex Morlet wavelet filter **a** real output, **b** imaginary output

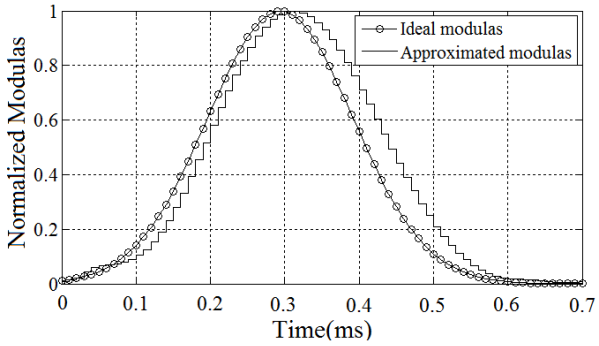


(a)

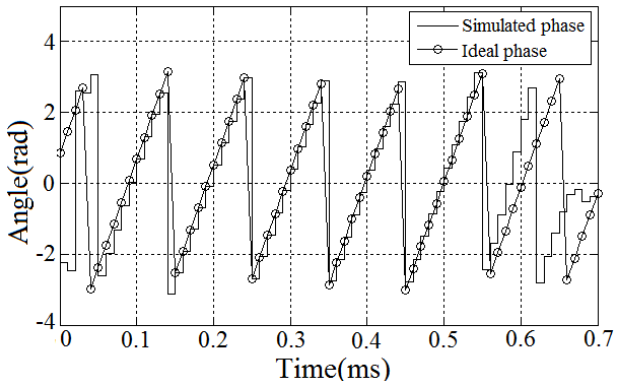


(b)

Fig. 6 Impulse response of complex Morlet wavelet filter **a** real coefficient, **b** imaginary coefficient



(a)



(b)

Fig. 7 Transient response of complex Morlet wavelet filter **a** modulus, **b** phase

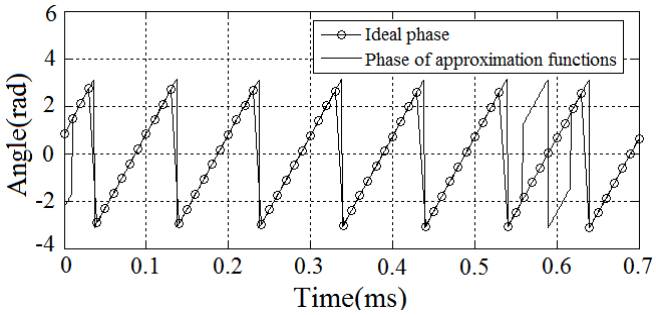


Fig. 8 Phase response of the rational approximation functions

5 Conclusions

A double-sampling fully-balanced SI complex wavelet filter structure with low circuit complexity has been presented. Also, the explicit design formulas are demonstrated. Built on FLF configuration, the proposed structure can share a great part of the implementation circuits for the pole-shared real and imaginary approximation functions, which can minimize chip size and power consumption. To verify our proposal, the complex Morlet wavelet is used as an example. Simulation results show that the proposed filter structure can be used to extract the CWT's modulus and phase information with high precision, and is well suited for the implementation of analog CWT circuits. It should be stressed that the proposed structure is suitable for arbitrary pole-shared rational complex wavelet bases due to the generality of the MLF architecture.

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