A Wideband Linear Tunable CDTA and its Application in Field Programmable Analogue Array

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Abstract In this paper, a NMOS-based wideband low power and linear tunable transconductance current differencing transconductance amplifier (CDTA) is presented. Based on the NMOS CDTA, a novel simple and easily reconfigurable configurable analogue block (CAB) is designed. Moreover, using the novel CAB, a simple and versatile butterfly-shaped FPAA structure is introduced. The FPAA consists of six identical CABs, and it could realize six order current-mode low pass filter, second order current-mode universal filter, current-mode quadrature oscillator, current-mode multi-phase oscillator and current-mode multiplier for analog signal processing. The Cadence IC Design Tools 5.1.41 post-layout simulation and measurement results are included to confirm the theory.

KeyWords CMOS analogue circuits analog; signal-processing; current-mode circuits; current differencing transconductance amplifier, configurable analogue blocks; field programmable analogue arrays.

1 INTRODUCTION

Reconfigurable hardware platform is gaining increasing importance in all application areas of the semiconductor industry due to providing flexible customize application-specific integrated circuit(ASIC), and it is an attractive design for decreasing the monetary cost and circumventing the long development cycle [1]. Rapid-prototyping techniques for prototyping digital integrated circuits have become a widely endorsed approach in digital design for fast time-to-market products, such as the use of field programmable gate arrays (FPGAs) to cater particularly well reconfigurability. Analogical to the FPGAs in digital circuits, the field programmable analog arrays (FPAAs) are type of reconfigurable analog circuits capable of implementing a variety of analog signal-processing functions, and they are widely used in fuzzy inference systems [2], micro-sensor interfaces [3] and measurement systems [4-5].

The FPAA is a programmable and rapid-prototyping device for implementing various analog circuits, like analog filters, oscillators, multipliers etc. [6-7]. A FPAA consists of configurable analog blocks (CABs) and signal interconnection between them. The reported FPAAs can be divided into two categories: discrete time FPAA [8-12] and continuous time FPAA [13]. The discrete time FPAAs are based on switched-capacitor techniques, which providing benefits in adjustability and matching but brings drawbacks in terms of power-consumption and switching noise and narrow bandwidth [14]. The continuous-time FPAAs usually have larger bandwidth than discrete-time ones.

During the past decade, a great number of studies on continuous-time FPAAs have been reported. Lee and Gulak describe the basic idea of FPAAs [15] where CABs, capacitors, and resistors can be connected by a routing network in 1991. In 2002, a FPAA designed using chessboard layout [16] was presented by Pankiewicz, et. al. This FPAA comprises of 40 CABs built of one operational transconductance amplifier and one capacitor (OTA-C) each. The local interconnections, switches and the OTA tuning circuit are achieved by programmable current mirror. Becker and Henrici proposed a hexagonal FPAA structure in 2008 [14], this structure does not require a routing network and switches in the signal path which improves the frequency response. Loobi and Lyden reported a FPAA which contains two types of CAB based on operational amplifiers (OP) [17]. The interconnection between CABs occupies nearly 60% of the area. FPAAs based on operational transconductance amplifiers and capacitor (OTA-C) technique are promising for high frequency operation [16, 18-20], because of programmable transconductance of OTAs. The FPAAs presented in [7, 21-22] consist of CABs based on current conveyors (CCII). The gain of each CAB can be digitally controlled by digital control word in [7] with fixed interconnection. In [21], each CAB contains a CCII, two transconductors working as tunable grounded resistors, two programmable capacitors and a buffer. Madian, Mahmoud et al. constructed their FPAA by 16 CABs based on current feedback operational amplifiers (CFOA) [23]. The CABs interconnect with each other based on crossbar structure. In 2012, Fernadez et al. proposed a FPAA using translinear element [24], the CABs are based on the log-domain circuit. Reference [25] reported a FPAA which consists of 18 CABs based on translinear element also. Within each CAB, there are 20 nearest neighbor lines in vertical routing. These lines can reduce parasitic capacitance.

However, the reported analog FPAAs, whether they are based voltage mode (OP etc.) blocks or current mode (OTA, CCII and CFOA etc.) blocks, have relatively narrow bandwidth and high supply voltage (for example, OTA (CA3080) has BW = 2 MHz and V_{pp} = ±15 V, CCII (AD844) has BW = 20 MHz and V_{pp} =±20 V, OP (F741A) has BW = 1.5 MHz and V_{pp} = ±15 V). In addition, these blocks are lack of linear tunablility. Therefore, the reported continuous-time FPAAs based on

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above blocks suffer from relatively narrow bandwidth and lack of linear tunablility.

CDTA is a recently reported current mode active block with a current differencing circuit and a transconductance circuit, and CDTA is widely used in current-mode filters [26-28],sinusoidal oscillators [29-31] and inductance simulator circuit [32].Unlike previously reported current mode blocks, the most important characteristic of CDTA is that the two input ports (*p* and *n*) of the CDTA are virtually grounded, and the parasitics of the input ports are relatively smaller than the other current mode blocks, and the bandwidth of CDTA is relatively wider than the other current mode blocks.

In 2003, D. Biolek proposed the CDTA for the first time [33], the circuit uses two current conveyors and one operational transconductance amplifier to achieve the CDTA, and the bandwidth is about 15MHz. Keskin et al proposed a CDTA CMOS circuit in 2006 [34], which consists of a CMOS current differential amplifier and a CMOS OTA .Uygur et al proposed a simple CMOS CDTA in 2007 [35]. This circuit consists of a current control current source and a simple structure of the transconductance and its operating bandwidth can reach 100MHz. In 2011, Firat proposed a modified CMOS CDTA [36]. In the difference current stage (pre-stage) of this circuit, basic current mirror is replaced by a cascade current mirror. At the input end of the OTA (the last stage), the cross coupling technology is used. And at the OTA output terminal, high impedance technology is used. These modifications make this circuit possess such features as the linearity of the circuit is increased, the output impedance of the circuit is improved, and its supply voltage can low to ± 1.5V, -3dB bandwidth can achieve about 100MHz. In 2013, J. Xu, C. Wang and J. Jin proposed a CDCTA in [37], and its supply voltage is ±1.5V, -3dB bandwidth is about 200MHz. However, there are some drawbacks for above these circuits: (a) the bandwidth of those circuits is limited, which is almost less than 200MHz. (b)Those circuits have no linear tunablility of transconductances, so do not convenient to form multiplier or amplitude modulation circuits, and the tuning range is narrow. The application circuits based on CDTA are also reported [43-45], such as filters and oscillators which are better high frequency characteristic than similar OTA-based and CCII-based the filters [38-39] and oscillators [40-42] because of CDTA higher frequency characteristic compared with OTA and CCII.

Based on the above analysis of CDTA， a novel wide bandwidth low power and linear tunable transconductance CDTA is presented in this paper. The proposed CDTA has NMOS AC equivalent signal path, which could avoid the limitations of the high frequency application by the PMOS transistors (in the standard n-well CMOS process, the unity gain frequency of NMOS is about twice of PMOS [38]). Moreover, the transconductance of the proposed circuit is linear tunable.

To overcome the drawbacks (narrow bandwidth, lack of transconductance linear tunablility and higher power consumption) of previous reported FPAAs, a current-mode field-programmable analog array (FPAA) using CDTA-based CABs as basic building blocks and a novel butterfly-shaped continuous-time analog circuits is presented in this article. In order to reduce the number of CABs used in the FPAA, the butterfly-shape is adopted in this work. There are only six CABs used in the proposed FPAA, and the CABs in the FPAA are connected by meshed vertical input lines and horizontal output lines, and each node of the mesh is connected by a switch. The proposed FPAA could successively provide the following five basic analog circuit functions: six order current-mode low pass filter, second order current-mode universal filter, current-mode quadrature oscillator, current-mode multi-phase oscillator and current-mode multiplier. However, six CABs are not always working simultaneously. In this circumstance, unnecessary CABs could be shut down by the programmable CAB selection switches (S_1), which could effectively reduce the power consumption of the FPAA chip. The other advantage of the butterfly-shaped FPAA is the excellent scalability, and it is easy to expand the size of the FPAA by adding CABs in the horizontal and vertical directions of the FPAA.

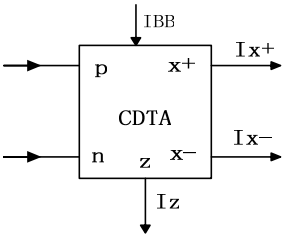
2 The CDTA based current-mode CAB

2.1 The current differencing transconductance amplifiers

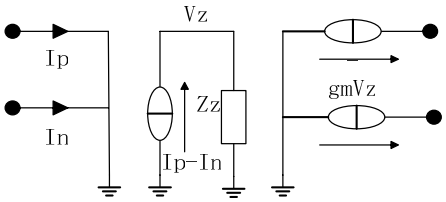
Fig.1 (a) is the symbol of CDTA, and Fig.1 (b) is the equivalent circuit of CDTA. The terminal relations of CDTA could be characterized by the following set of equations [36-37]:

$$\begin{cases} v_p = v_n = 0 \\ i_z = i_p - i_n \\ i_x = g_m v_z = g_m Z_z i_z \end{cases} \quad (1)$$

In Fig.1, *p* and *n* are the input terminals, *z* and *x* are the output terminals, g_m is the transconductance gain, and Z_z is the external impedance connected to the terminal z. From equation (1), the voltage of input terminal p and n are all zero, and they are virtually grounded, and the parasitics of the input ports are very small. The current i_z is the difference of the currents at *p* and *n* (i_p-i_n), and it flows from the terminal z into the impedance Z_z. The voltage at the terminal z is transferred to a current at the terminal x (i_x) by a transconductance gain (g_m), which can be electronically controlled by an external bias current IBB.



(a) Symbol for the CDTA



(b) Ideal model of the CDTA

Fig.1 symbol and ideal model of CDTA

A classical CMOS realization of CDTA circuit is shown in Fig.2 [39]. On the basis of this circuit, much improved CDTA circuits have been reported in literatures [40-41], and they obtain good performances. However, those circuits have following shortages: 1) The AC equivalent circuit in Fig. 2 includes PMOS transistor, because of the hole carrier mobility in PMOS is slower than the electronic carrier mobility in NMOS, the bandwidth of this equivalent circuit is relatively small. 2) as the transconductance g_m is proportional to the $\sqrt{I_{B3}}$ rather than has a lienear relation with I_{B3}, it is inappropriate to construct a multiplier or modulator by CDTA.

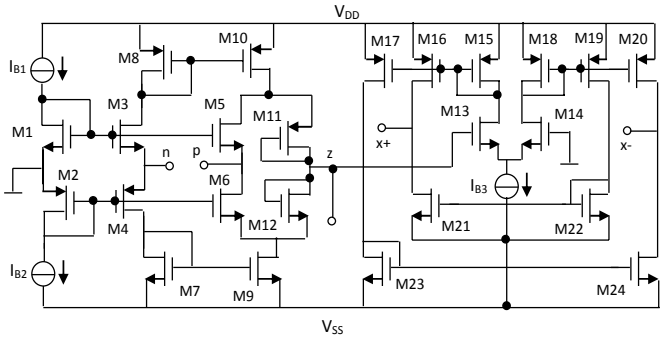


Fig.2 a classical CMOS CDTA circuit

To overcome these drawbacks, we present a novel NMOS CDTA whose AC equivalent signal is composed of full NMOS transistors. The proposed NMOS CDTA is capable of providing a wide frequency bandwidth, and its transconductance G_m can be linearly tuned by a single continuous bias current I_{BB}. Meanwhile, it also has features of lower DC supply voltage, lower input resistance and higher output resistance. The functional block diagram of the proposed NMOS CDTA circuit is shown in Fig.3, and the implementation of the circuit is realized by NMOS based current differencing circuit and NMOS based linear tunable transconductance, which is presented in Fig.4.

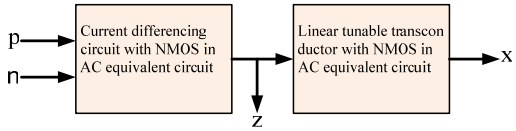


Fig.3 architecture of wideband linear tunable NMOS CDTA

The complete CDTA circuit is shown in Fig.4. The CDTA is designed such that all PMOS transistors only serve as current sources so that the signal has an all NMOS signal path. The input and output branches are biased by a DC current I_B, which is provided by the current sources MP_0-MP_9.

The current differencing circuit is formed by NMOS transistors MN_1-MN_{15} [46]. Since the drain electrodes of NMOS transistors MN_1, MN_2 and MN_6 are biased by the same current source I_B, the voltage of two current input node *p* and *n* are forced to track the grounded source electrode of MN_1, and then the input terminal can be considered as the virtual ground. When the input currents i_p and i_n are forced into the input terminals *p* and *n*, they will be mirrored to the output *z* terminal through the groups of transistors MN_6-MN_{14} and MN_4, MN_5, MN_{15}, respectively. After that, the drain current of MN_{12} is I_B-i_p and MN_{15} is I_B+i_n, therefore, the output current at port z is equal to the difference of the input currents at ports p and n, i.e., i_z = i_p-i_n.

In this configuration, the input shows a reduced small-signal input resistance by using a negative feedback at its input terminals, which can be calculated as:

$$R_{p,n} \approx \frac{(g_m+g_{mb})_{MN3}+g_{mMN5}}{r_{dsMN2}(g_m+g_{mb})_{MN2}g_{mMN3}g_{mMN4}} = \frac{(g_m+g_{mb})_{MN3}+g_{mMN5}}{Ag_{mMN3}g_{mMN4}} \quad (2)$$

where A = r_{dsMN2} $(g_m + g_{mb})_{MN2}$, g_{mMNi} represents the transconductance of the transistor MN_i (i=1,2,3...32), g_{mbMNi} is the bulk transconductance and r_{dsMNi} denotes the drain-source resistance of the transistor. Hence the negative feedback reduces the small-signal input impedances R_p and R_n by a factor equal to the gain *A*. In addition, the high output impedance at ports *z* can be evaluated as:

$$R_z \approx r_{dsMP5} \,||\, \{r_{dsMN12}[2+(g_m+g_{mb})_{MN12}r_{dsMN13}]\,||\, r_{dsMN15}\} \quad (3)$$

The transconductor stage is an essential part of CDTA circuit, providing a transconductance gain (G_m) which can directly transfer voltage signal of *z* terminal (V_z) into current output signal i_x, and the G_m of the CDTA can be electronically tuned by the bias current I_{BB}. However, in traditional CDTA circuit, the G_m is in the form of square root function, i.e.:

$$G_m = \frac{di_0}{dV_z}\Big|_{V_z=0} = \sqrt{2I_{BB}K} \quad (4)$$

where *K* is the transconductance parameter of differential pair transistors. From equation (4), it is clear that the output-input characteristic of traditional CDTA is nonlinear.

To overcome this drawback, a NMOS based linear tunable transcondutor is presented by using the linear tunable technique [47]. In Fig.4, transistors MN_{16} to MN_{31} consist of the wide linear tunable transconductor stage. The scheme adopts two OTAs, where an active resistor [48] formed by MN_{23} and MN_{24} are connected in series between OTA_1 and OTA_2. Fig.5 shows the block diagram of linear tunable transconductor stage and the simulation result of the active resistor. From Fig.5(b) we knew the linearity error of the active resistor is about 0.35% when VDD=-VSS=1.5V, which completely conforms to the circuit design requests in our work and has better actual application value.

Using the square law characteristics and neglecting the second-order effort of MOS transistors operating in the saturation region, the differential output current of the circuit of Fig. 4 can be expressed as:

$$i_X = \frac{I_{BB}\sqrt{K_1K_2}}{4K_{(MN23)}(V_D - V_{th(MN23)})}v_Z = G_m^{'}v_Z \quad (5)$$

where $G_m^{'} = I_{BB}K$, $K = \dfrac{\sqrt{K_1K_2}}{4K_{(MN23)}(V_{DD} - V_{th(MN23)})}$, K_1 and K_2 are the transconductance parameters of two differential pair transistors of OTA_1 and OTA_2, respectively, and V_{th} is the threshold voltage of transistor MN_{23}. From equation (5), we could conclude that the transconductor has a constant gain

value $G_m^{'}$, which can be electronically and linearly tuned by the bias current I_{BB}.

Additionally, the output resistance looking into the x terminal could be expressed as:

$$R_x \approx r_{dsMP8} \| [r_{dsMN28}(2 + g_{mMN28} r_{dsMN30}) \| r_{dsMN26}] \quad (6)$$

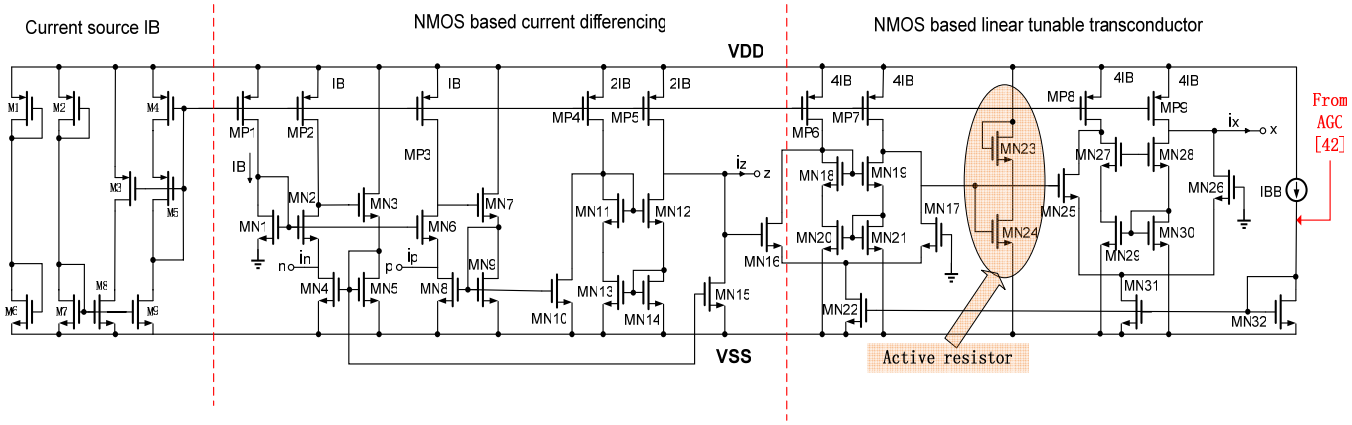
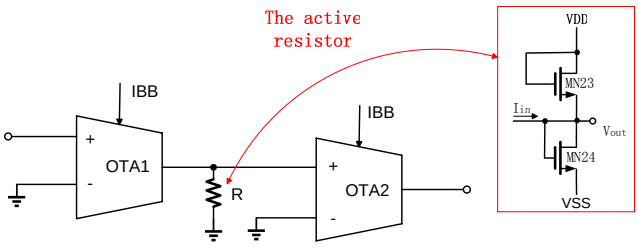
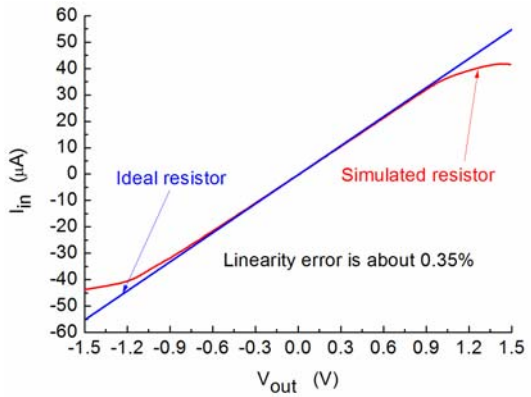


Fig.4 proposed wideband linear tunable CDTA circuit

Fig.6 is the simulated and measured frequency responses of the proposed CDTA. Fig.6(a) shows the current transfer characteristics from the terminal p and n to terminal z. From Fig.6(a), it is clear that the current transfer bandwidths from terminal p and n to terminal z are 1.338GHz, 2.092GHz in experimental situation, and 1.359GHz, 2.001GHz in simulation situation respectively. Fig.6(b) shows the current transfer characteristics from the terminal x to terminal z. From Fig.6(b), it is clear that the current transfer bandwidth from terminal x to terminal z is greater than 1GHz. The difference between all the measured and simulated results is less than 5%, which is within range of the manufacturing process variations.

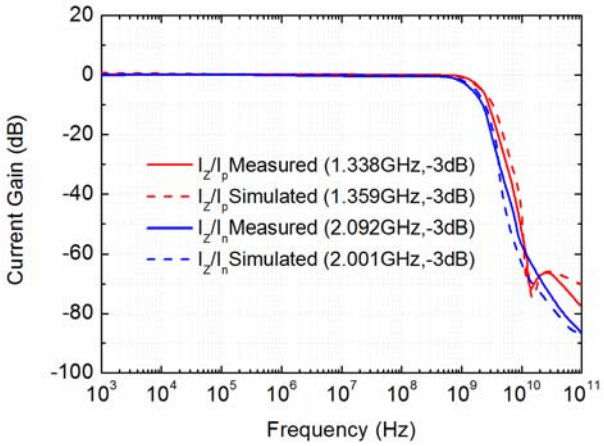


(a) The block diagram of linear tunable transconductor stage of the proposed CDTA

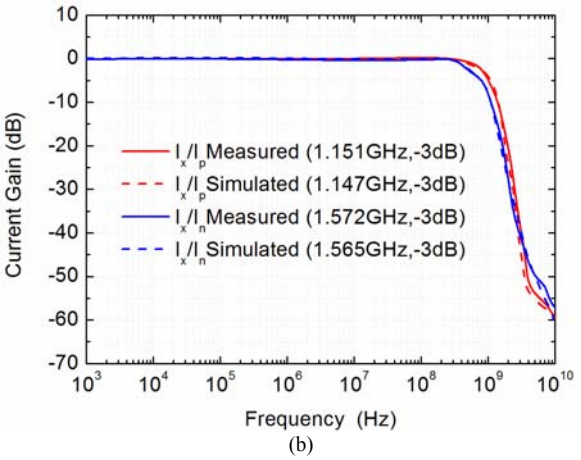


(b) The characteristic V_{out}/I_{in} of the active resistor

Fig.5. the active resistor and its characteristic



(a)



(b)

Fig.6 frequency responses of the proposed CDTA:
(a) Z terminal (R_Z=1kΩ) (b) X terminal (R_Z=1kΩ, I_{BB}=200uA)

Fig.7 is the linear tunable range of the transconductance G_m. From Fig.7, it is clear that the transconductance of the CDTA is nearly linear, when the bias current I_{BB} tunes from 20μA-200μA. DC response of port current I_x of the CDTA by changing IBB from 20μA to 200μA is shown in Fig.8. The linearity errors in

Fig.7 and Fig.8 are kept between 1.73% to 2.37%, and the linearity is sufficient for the following applications.

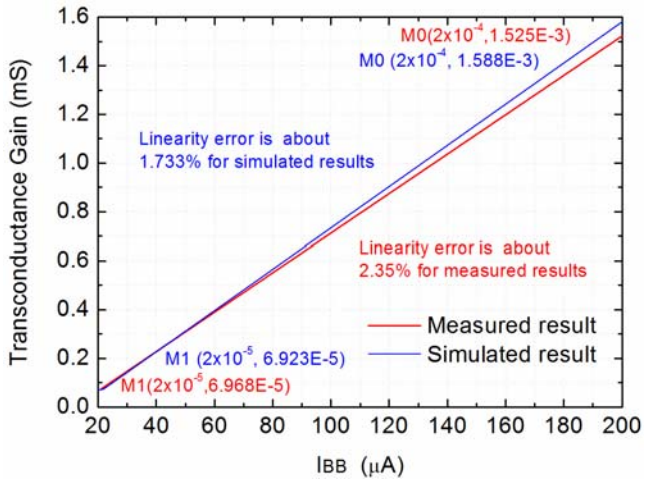


Fig.7 linear tunable range of the transconductance G_m (I_{BB} tunes from 20μA-200μA)

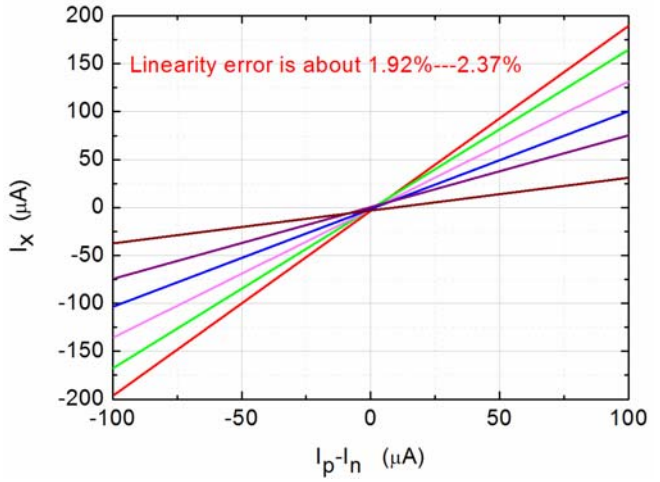
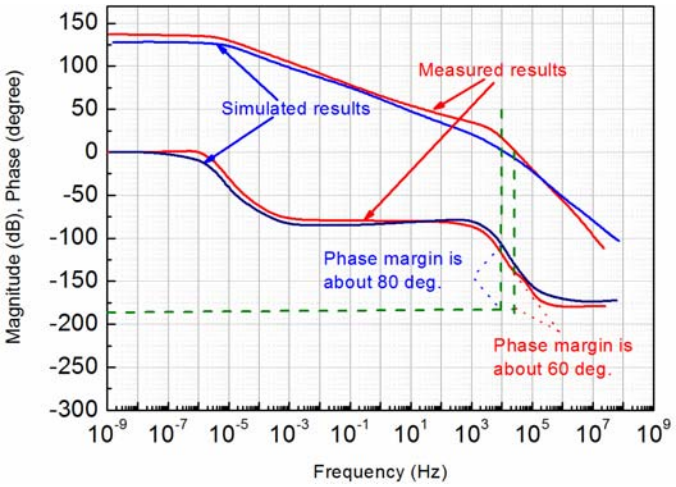


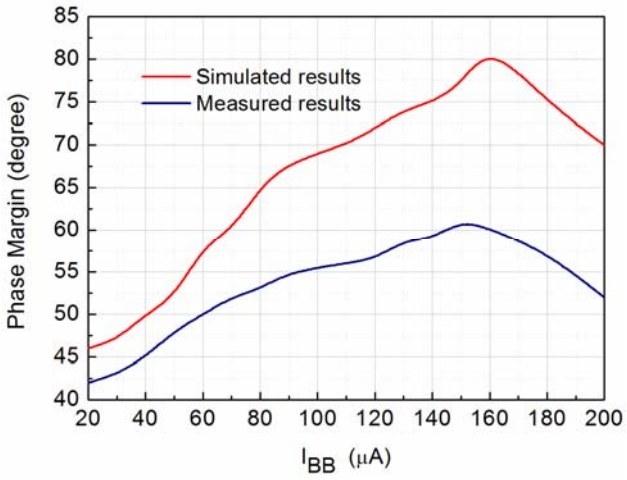
Fig.8 DC response of port current of the CDTA by changing I_{BB} from 20μA to 200μA

The Bode plot of the proposed CDTA is shown in Fig. 9. Fig.9(a) shows that the phase margin is about 80 and 60 degree in simulation situation and experiment situation when I_{BB} is 160μA, respectively. From Fig.9(b), we can see the varying scope of margin phase is about 46.15~80.01 (degree) in simulation situation, 42.30~59.87 (degree) in experiment situation where I_{BB} changes from 20μA to 200μA. The difference between measurements and simulations are due to the manufacturing process variations and measurement limitations. The gain margin of the proposed CDTA is about $30 \pm 0.5dB$ where I_{BB} changes from 20μA to 200μA in simulation situation and experiment situation. The simulated and measured results show that phase margin can make CDTA has good stability [49].

Fig.10 is the Microphotograph of the chip of the CDTA.



(a) Bode plot of CDTA where I_{BB}=160μA



(b) Dependence of phase margin on IBB

Fig. 9 Bode diagram of the proposed CDTA

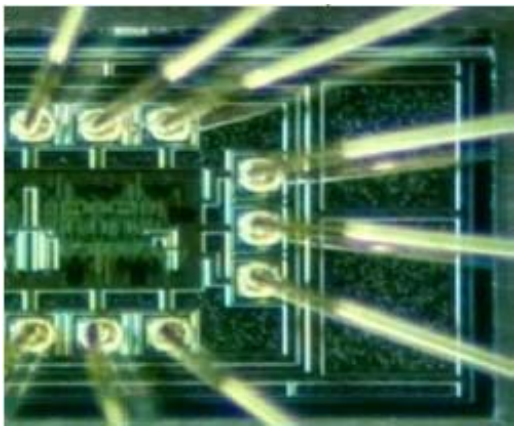


Fig.10 microphotograph of the chip of the CDTA

Table I gives the W/L ratio of the MOS transistors in Fig.4. Table II summarize the measured results of the proposed CDTA, and Table III compares the performances of the proposed CDTA with other reported works. From Table 1 and Table 2, we could know that the proposed NMOS-based CDTA has the advantages of higher current transfer bandwidths, lower power consumption and linear tunable than the other reported works.

TABLE I
W/L RATIO OF THE MOS IN FIGURE 4

MOS transistors	W(μm)/L(μm)
MP0-MP3	10/0.36
MP4-MP5	20/0.36
MP6-MP9	40/0.36
MN1, MN2, MN4-MN6, MN8-MN15	5/0.36
MN3, MN7	0.8/0.36
MN16-MN32	10/0.36
M1	3.8/0.36
M2	40/0.36
M4	2.3/0.36
M3, M5	18.8/0.36
M6-M8	4.6/0.36
M9	21.6/0.36

TABLE II
SUMMARY OF THE PROPOSED CDTA'S MEASURED SPECIFICATIONS

Parameters		Measured results
DC Supply voltages		±1.1V
Linearity range	I_p	±50μA
	I_n	±50μA
	I_X	±200μA
Linear tuning range of Gm (I_{BB} tunes from 20μA-200μA)		69.6μS -1.525mS
Current transfer ratio -3dB Bandwidth:	I_Z/I_P	1.105GHz
	I_Z/I_N	0.982GHz
	I_X/I_P	1GHz
	I_X/I_N	0.982GHz.
Impedance at ports	P	23.5Ω
	N	23.5Ω
	Z	175kΩ
	X	216kΩ
Offset currents I_Z, I_X		135nA, 1.02μA
Max power consumption		2.38mW

2.2 The CDTA-based CAB

The proposed CDTA-based CAB is presented in Fig.11. The CAB consists of a CDTA, a programmable capacitor C_{eq} and two programmable switches. The *p* and *n* are the input terminals of the CAB, the *z* and *x* are the output terminals of the CAB. The connections and disconnections of the supply voltage and capacitor array are controlled by the switches S_1 and S_2, respectively. The terminal V_b is the bias of the transconductance amplifier of the CAB, moreover, the terminal V_b has another important function, and it could be used as an input terminal in the current-mode multiplier.

Here, the programmable capacitor C_{eq} is presented in Fig.11. The programmable capacitor array consists of five groups of capacitors from C_0 to C_4, and the capacitance value of the programmable capacitor is adjusted by the selection switches S_{C0} to S_{C4}.

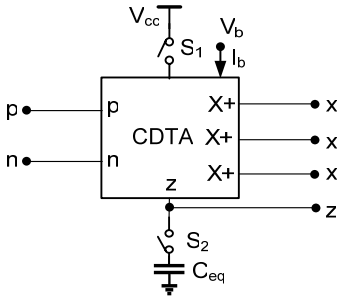


Fig.11 the CDTA-based CAB

The equivalent capacitance of the programmable capacitor array in Fig.12 could be expressed as:

$$C_{eq} = \sum_{n=0}^{4} a_n 2^n C_n + C_p \tag{7}$$

where $a_n = 0$ or 1, when switch S_{Cn} is turned on, a_n equals to 1, and when switch S_{Cn} is turned off, a_n equals to 0. C_p is the parasitic capacitance when all the switches are turned off.

TABLE III
PERFORMANCE COMPARISON

Parameters		Ref [30]	Ref [32]	Ref [38]	Ref [39]	This work
supply voltages		±1.5 V	±1.25 V	±1.8V	±0.6 V	±1.1V
Current transfer ratio -3dB bandwidth	I_Z/I_P	609 MHz	953MHz	NA	0.985MHz	1.105GHz
	I_Z/I_N	462 MHz	959 MHz	NA	1/36MHz	0.982GHz
	I_X/I_P	NA	927 MHz	0.996MHz	NA	1GHz
	I_X/I_N	NA	930MHz	0.978MHz	NA	0.982GHz
Impedance at ports	P	812Ω	7.03Ω	1.92Ω	227Ω	23.5Ω
	N	348Ω	15.8Ω	1.92Ω	227Ω	23.5Ω
	Z	1.08MΩ	3.7Ω	388kΩ	262KΩ	175kΩ
	X	167GΩ	9.4 MΩ	16.21MΩ	1.2MΩ	216kΩ
Linear tunable feature		NO	NO	NO	NO	YES
Power consumption (mW)		3.61	2.48	6.31	143	2.38

3 Proposed Field Programmable Analogue Array

The goal of the presented work is a design study of programmable and reconfigurable FPAA, and the FPAA could generate five basic analog circuit functions, such as: six order current-mode low pass filter, second order current-mode universal filter, current-mode quadrature oscillator, current-mode multi-phase oscillator and current-mode multiplier.

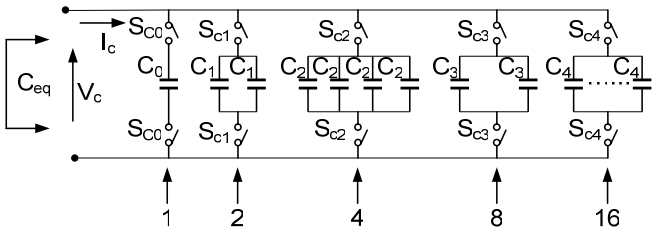


Fig.12 the programmable capacitor array

The proposed butterfly-shaped FPAA is presented in Fig.13. The FPAA consists of six identical CDTA-based CABs. The vertical lines are the inputs of the FPAA, and the horizontal lines are the outputs of the FPAA. The input lines and output lines interweave into a mesh, and each node of the mesh is connected by a MOS switch. Actually, it is easy to expand the size of the FPAA by adding CABs in the horizontal and vertical directions of the FPAA, and the excellent scalability is a big advantage of the butterfly-shaped FPAA. Here, the vertical auxiliary lines in the middle of the FPAA further facilitate the connection of each node of the butterfly-shaped FPAA.

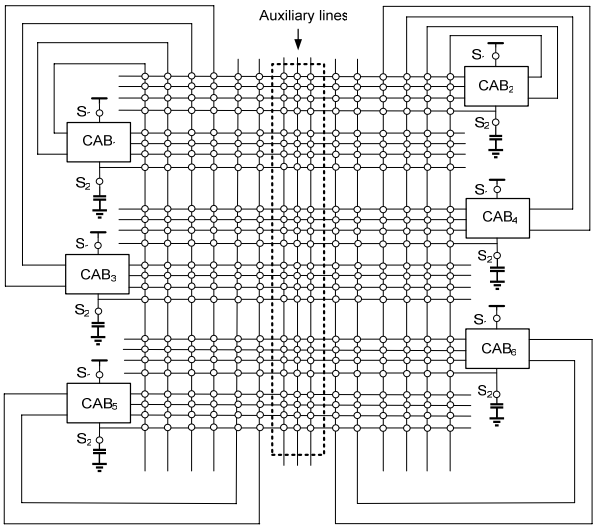


Fig.13 structure of the FPAA

The structure of interwoven vertical input lines and horizontal output lines is suitable for analog FPAA, because by turning on and off some specific node switches, the six order current-mode low pass filter, second order current-mode universal filter, current-mode quadrature oscillator, current-mode multi-phase oscillator and current-mode multiplier could be generated successively. However, the six CABs are not always working simultaneously. In this circumstance, the unnecessary CABs could be shut down by the programmable CAB selection switches (S_1), which could effectively reduce the power consumption of the FPAA chip. Similarly, the programmable capacitor selection switches (S_2) are used for capacitor selection. All the below simulated and measured results are based on the Cadence IC Design Tools 5.1.41.

3.1 The six-order current-mode low pass filter

The CDTA-based low pass filter is based on a sixth-order all-pole passive LC low-pass filter, and the passive LC low pass filter is presented in Fig.14.

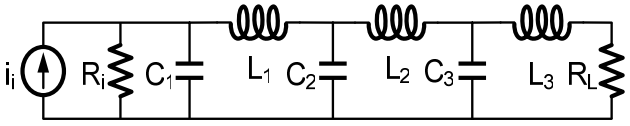


Fig.14 six-order passive LC low pass filter

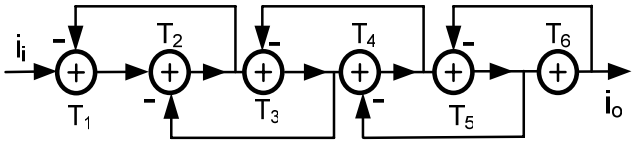


Fig.15 signal flow diagram of the passive LC low pass filter

Fig.15 is the leapfrog signal flow diagram of the sixth-order all-pole passive LC low-pass filter. T_1 and T_6 are lossy integrators, and T_2 – T_5 are lossless integrators. Using the CDTA-based lossy integrators and lossless integrators instead of T_1 – T_6 in Fig.15, the CDTA-based six order low pass filter is presented in Fig.16. Fig.17 is the FPAA realization of the six order low pass filter. The thick lines in Fig.17 stand for the connected signal paths, and the solid dots stand for the switches between the signals paths are turned on.

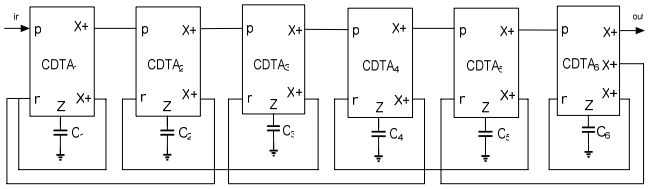


Fig.16 CDTA-based six order low pass filter

The circuit was simulated and measured with the values of external capacitors C_1-C_6 are all equal to 10pF, and all I_{BB} of CDTAs are 87.5μA. The results are presented in Fig.18. From Fig.18, it is clear that the bandwidth of the low pass filter is about 500MHz. The falling edge of the curve at about 200MHz is very steep, and the low pass filter has excellent band noise suppression ability. The slight deviations of the measurements from the simulations are due to the manufacturing process variations and measurement limitations.

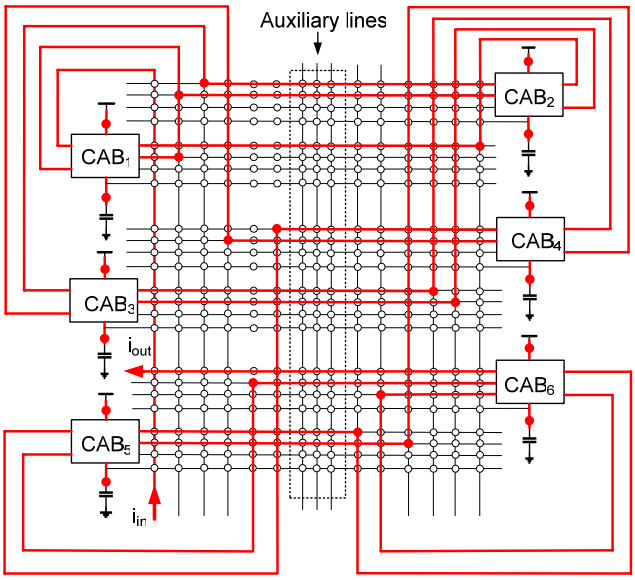


Fig.17 FPAA-based six order low pass filter

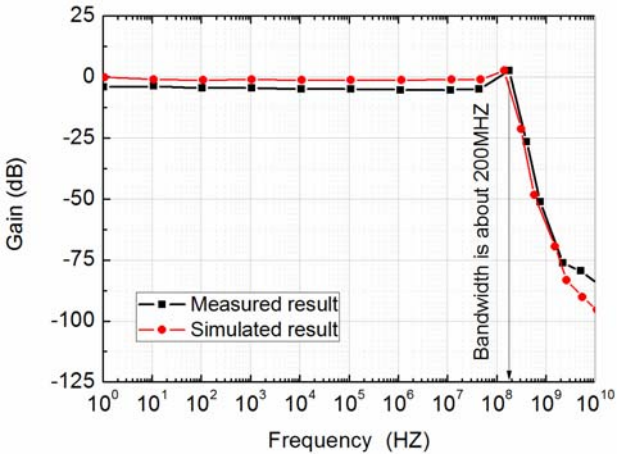


Fig.18 simulated and measured frequency response of six-order LP filter

3.2 The second order current-mode universal filter

The CDTA-based second order current-mode universal filter is shown in Fig.19. The filter could realize low-pass (LP), high-pass (HP), band-pass (BP) band-stop (BS) and all-pass (AP) filter functions simultaneously.

Analyzing Fig.19 by using equation (1) yields the following current transfer equations as (8) - (12).

$$T_{LP}(s)=\frac{i_{o1}}{i_{in}}=\frac{\frac{g_{m1}g_{m2}}{C_1C_2}}{s^2+s\frac{g_{m2}}{C_2}+\frac{g_{m1}g_{m2}}{C_1C_2}} \tag{8}$$

$$T_{BP}(s)=\frac{i_{o2}}{i_{in}}=\frac{s\frac{g_{m2}}{C_2}}{s^2+s\frac{g_{m2}}{C_2}+\frac{g_{m1}g_{m2}}{C_1C_2}} \tag{9}$$

$$T_{HP}(s)=\frac{i_{o3}}{i_{in}}=\frac{s^2}{s^2+s\frac{g_{m2}}{C_2}+\frac{g_{m1}g_{m2}}{C_1C_2}} \tag{10}$$

$$T_{BS}(s)=\frac{i_{o4}}{i_{in}}=\frac{s^2+\frac{g_{m1}g_{m2}}{C_1C_2}}{s^2+s\frac{g_{m2}}{C_2}+\frac{g_{m1}g_{m2}}{C_1C_2}} \tag{11}$$

$$T_{AP}(s)=\frac{i_{o4}-i_{o2}}{i_{in}}=\frac{s^2-s\frac{g_{m2}}{C_2}+\frac{g_{m1}g_{m2}}{C_1C_2}}{s^2+s\frac{g_{m2}}{C_2}+\frac{g_{m1}g_{m2}}{C_1C_2}} \tag{12}$$

From equations (8) - (12), it is clear that i_{o1} is the low-pass output, i_{o2} is the band-pass output, i_{o3} is the high-pass output, i_{o4} is the notch output and (i_{o4} - i_{o2}) is the all-pass output.

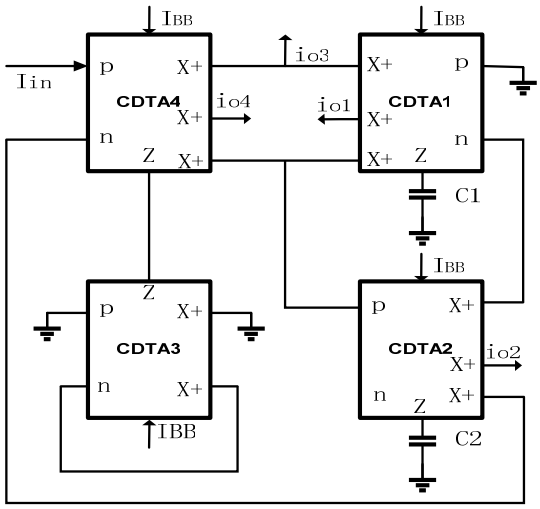


Fig.19 CDTA-based second order universal filter

Fig.20 is the FPAA realization of the second order universal filter. CAB_1 – CAB_4 are turned on and CAB_5 – CAB_6 are turned off by the switches S_1. Here, the programmable CAB selection switches (S_1) are very useful, the unnecessary CABs in the second order universal filter (CAB_5 and CAB_6) are turned off, and it is a good approach to save energy, especially in large scale FPAA design.

Fig.21 is the post-layout simulation results and measured results of the second order current-mode universal filter, where I_{BB} of $CDTA_1$, $CDTA_2$ and $CDTA_3$ are set as 100μA , the values of the capacitors are C_1=55pF and C_2=22pF, C_1 and C_2 are external capacitance. The low pass (LP), high pass (HP), band pass (BP), all pass (AP) and band stop (BS) frequency responses of the universal filter, and the center frequency of the filter is about 70MHz; The all pass (AP) frequency response and phase response of the universal filter, the AP response is relatively flat, and the phase variation is 360°, from -180° to +180°. The difference between simulated and measured results is due to fabrication tolerances and measurement limitations.

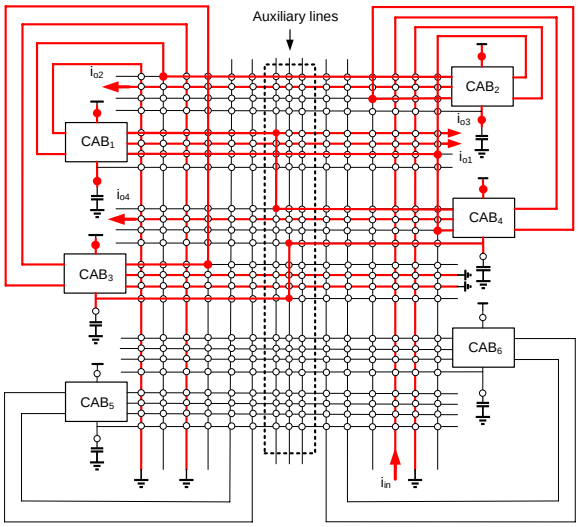


Fig.20 FPAA-based second order current-mode universal filter

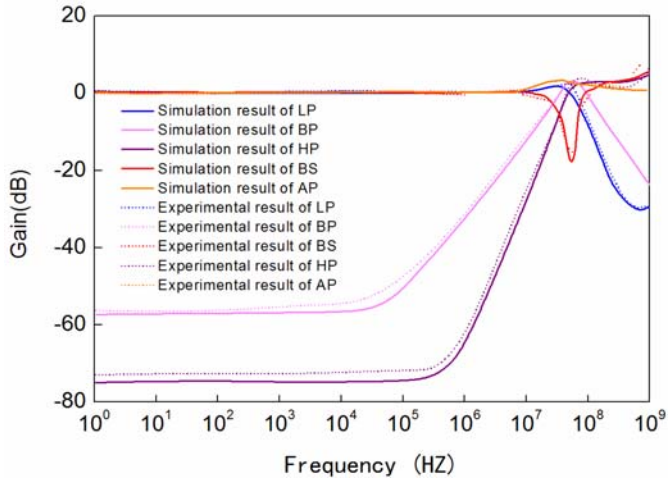


Fig.21 the simulation and measured frequency response of universal filter

3.3 The current-mode quadrature oscillator

The CDTA-based quadrature oscillator is presented in Fig.22. There are three CDTAs and two capacitors used in this circuit. A routine circuit analysis using equation (1), we can get the characteristic equation of the quadrature oscillator is:

$$s^2C_1C_2 + s\left(g_{m2} - g_{m1}\right)C_2 + g_{m2}g_{m3} = 0 \qquad (13)$$

where g_{m1}, g_{m2} and g_{m3} are the transconductance of the $CDTA_1$, $CDTA_2$ and $CDTA_3$, respectively.

From equation (13), the condition of oscillation (CO) and frequency of oscillation (f_0, ω_0, FO) of the quadrature oscillator can be expressed as:

$$CO: \quad g_{m1} = g_{m2} \qquad (14)$$

$$FO: \quad \omega_0 = \sqrt{\frac{g_{m2}g_{m3}}{C_1C_2}} \qquad (15)$$

where $\omega_0 = 2\pi f_0$.

From Fig.22, the current transfer function between i_{o1} and i_{o2} is:

$$\frac{i_{o1}(s)}{i_{o2}(s)} = \frac{g_{m2}}{sC_2} = \frac{i_{o1}(j\omega)}{i_{o2}(j\omega)} = \frac{g_{m2}}{sC_2}e^{-j90^\circ} \qquad (16)$$

So, the phase difference between i_{o1} and i_{o2} is 90°, and the two output currents are quadrature.

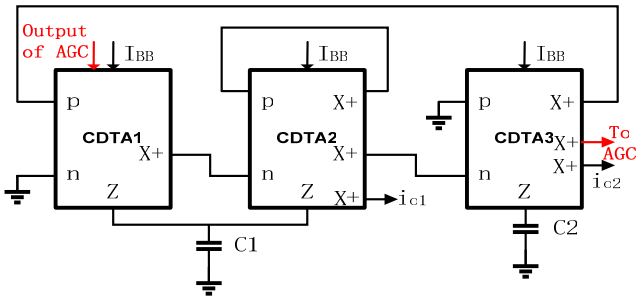


Fig.22 CDTA-based quadrature oscillator

From equation(14), the CO require that g_{m1} and g_{m2} must be exactly matched but it can't be carried out well since there are inevitably non-ideal characteristics. So, amplitude automatic gain control circuit (AGC) [42] is necessary in the design of oscillator, shown in Fig.23. The input voltage AGC_{INP} comes from port X+ of $CDTA_3$ in the Fig.22 through a load resistor. In the Fig.23, Diodes D1 and D2 form a diode rectifier which rectifies the input AGC voltage. Capacitor C_f and resistor R_f constitute a filter. Voltage to current converter can transfer DC voltage to DC current which is directly connected to IBB of CDTA1 (see AGC current in the Fig.4). A gain compensation mechanism is established via AGC, which can keep the amplitude of oscillator more stable and achieve lower total harmonic distortion (THD) [42]. In the Fig23, the circuit is realized by commercially available discrete devices. VCA810_12, IN4148 and CA3080E are chosen as the types of the amplifier, diode and voltage to current converter respectively. The values of resistors, capacitors are shown in Fig.23.

Fig.24 is the FPAA realization of the quadrature oscillator. CAB_1 – CAB_3 are turned on and CAB_4 – CAB_6 are turned off by the switches S_1.

The quadrature oscillator circuit is tested with all the bias current I_{BB}=87.5μA, the capacitors C_1=10pF and C_2= 50pF, C_1 and C_2 are external capacitance. Fig.25 shows simulation results of the quadrature oscillator.

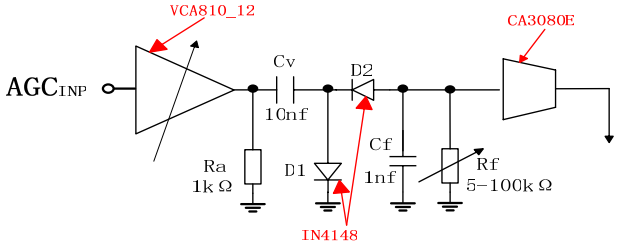


Fig23. Amplitude automatic gain control(AGC) circuit

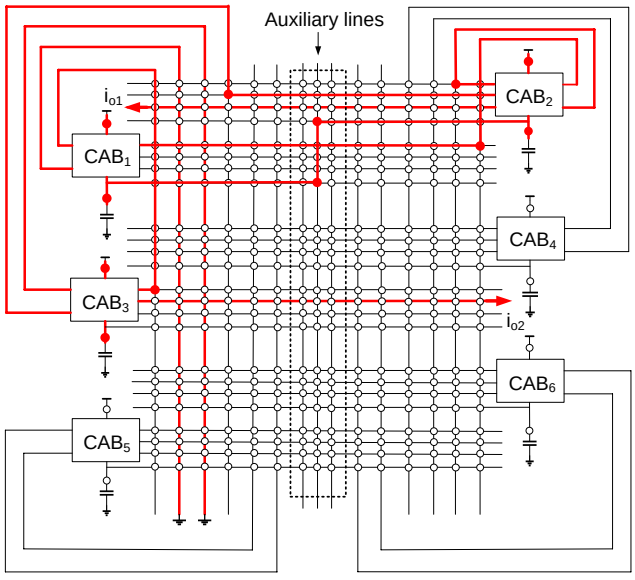


Fig.24 FPAA-based quadrature oscillator

Fig.26 shows dependence of frequency f_0 of quadrature oscillators on bias current I_{BB}, where ideal, expected, measured and simulated results are compared. The ideal range of f_0 is

calculated as 21.2 to 78 MHz. About 5% error tolerance is allowable in the expected estimation. The expected, simulated and measured results are fairly consistent. The time of starting oscillation is about 2.8us and the oscillation frequency is about 74MHz.

Fig.27 shows dependence of THD, output amplitude, phase shift and phase error quadrature oscillator on frequency f_0. The measured THD is lower than 1 % when f_0 is larger than 20 MHz for both observed outputs V_{01} and V_{02} (Fig.27a). The observed output voltage is about 500mV, and voltage level changes slightly during the tuning processing (Fig.27b). Phase shift between V_{01} and V_{02} and phase shift error with -90^0 are shown in Fig.27(c, d), the ideal phase shift between V_{01} and V_{02} is -90^o. From Fig.27(c, d), the maximal phase error with -90^0 is about $\pm 3^o$.

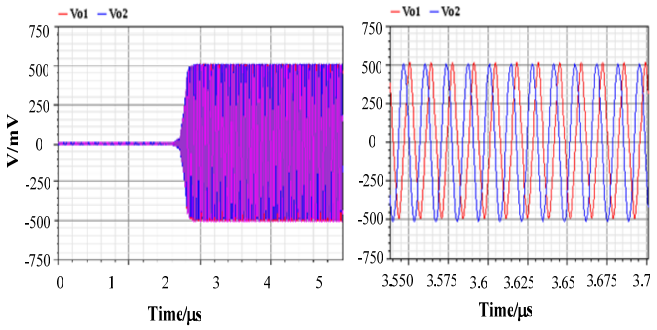


Fig.25 simulation results of the quadrature oscillator

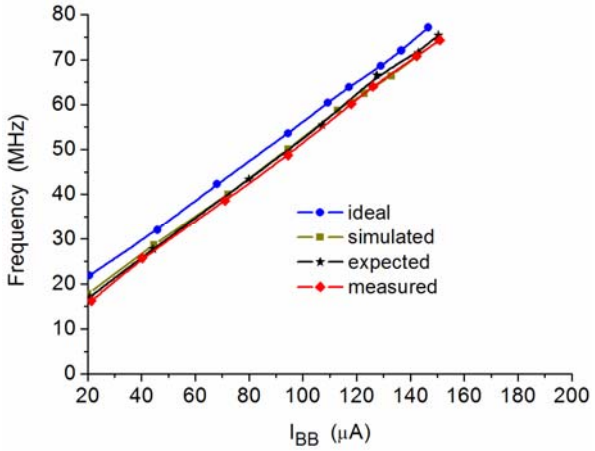
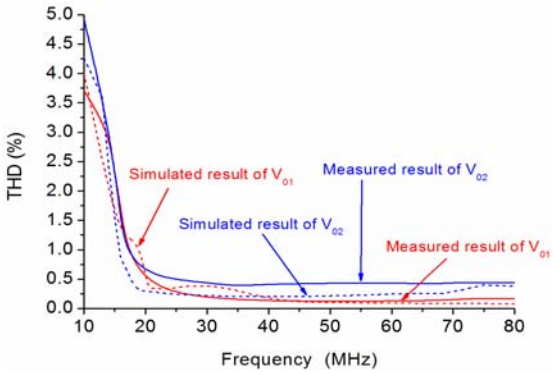
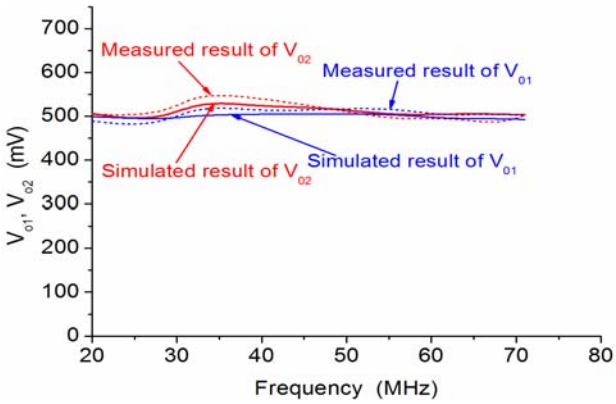


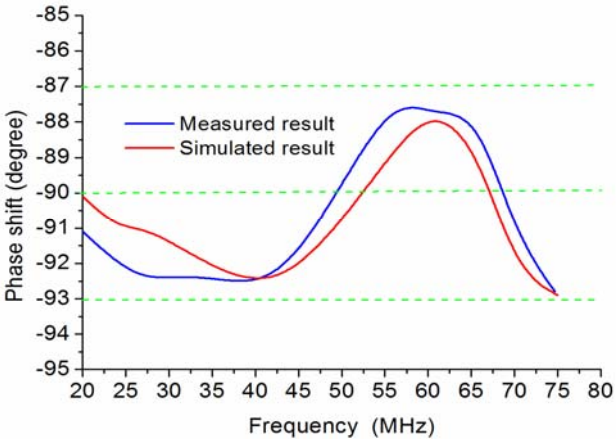
Fig.26 dependence of frequency f_0 on I_{BB} of quadrature oscillator



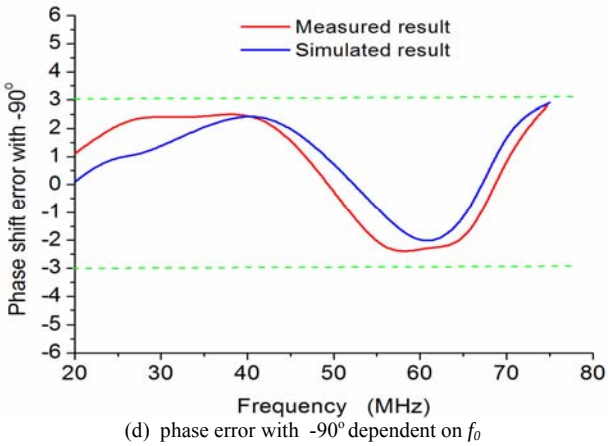
(a) THD dependent on f_0



(b) output amplitude dependent on f_0



(c) phase shift dependent on f_0.



(d) phase error with -90^o dependent on f_0

Fig.27 characteristics of the proposed quadrature oscillator

3.4 The current-mode multi-phase oscillator

The CDTA-based multi-phase oscillator is presented in Fig.28. $CDTA_1$ – $CDTA_3$ and C_1 – C_3 are used for lossy integrators, and the characteristics equations should be:

$$\frac{i_o}{i_{in}} = \frac{1}{1+s\left(\frac{C}{g_m}\right)} \tag{17}$$

where g_m is the transconductance of the CDTA and C stands for the capacitor connected with the CDTA.
$CDTA_4$ and $CDTA_5$ constitute the variable gain amplifier, and its characteristics equation should be:

$$\frac{i_o}{i_{in}} = -k = \frac{g_{m4}}{g_{m5}} \tag{18}$$

Assuming that $g_{m1} = g_{m2} = g_{m3}$, and $C_1 = C_2 = C_3$, and the loop gain of the multi-phase oscillator should be:

$$L(s) = -k\left[\frac{1}{1+s\left(\frac{C}{g_m}\right)}\right]^3 = -\left(\frac{g_{m4}}{g_{m5}}\right)\left[\frac{1}{1+s\left(\frac{C}{g_m}\right)}\right]^3 \tag{19}$$

According to the Barkhausen stability criterion (i) oscillators will sustain steady-state oscillations only when the loop gain is equal to the unity; (ii) the phase shift around the loop is zero or an integer multiple of 2π. The condition of oscillation and the frequency of oscillation (f_0, ω_0, FO) of the multi-phase oscillator could be given as:

$$\frac{g_{m4}}{g_{m5}} = \left|1+\left(\frac{\omega_o C}{g_m}\right)^3\right| \tag{20}$$

$$\omega_o = \left(\frac{g_m}{C}\right)\tan\left(\frac{\pi}{n}\right) \tag{21}$$

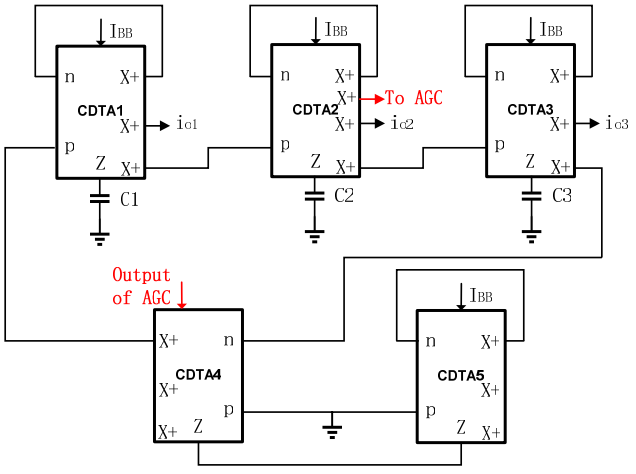


Fig. 28 CDTA-based multi-phase oscillator

Fig.29 is the FPAA realization of the multi-phase oscillator. There are five CABs used in the FPAA, and CAB_4 is turned off.

Simulations and experiments for the proposed multi-phase oscillator are performed with the capacitors C_1 =C_2=C_3=500pF, C_1, C_2 and C_3 are external capacitance.IBB of $CDTA_4$ is set as 100μA and IBB of $CDTA_5$ is set as 180μA.

Fig.30 is the transient response of quadrature outputs Vo1, V_{o2} and V_{o3} (where I_{BB} of $CDTA_1$-$CDTA_3$ is set as 87.5μA). From Fig.30, it is clear that the starting time is about 5.5 ns and the oscillation frequency is about 11.7MHz. Fig.30 shows the ideal range of f_0 is 3.5 to 12 MHz. Fig.31 shows characteristics of multi-phase oscillator Fig.31(a) is dependence of f_0 on IBB by changing I_{BB} of $CDTA_1$-$CDTA_3$ from 20μA to 200μA at the same time. Fig.31(b) shows the dependence of THD, output amplitude on f_0, the measured THD is lower than 1.5% when f_0 is larger than 3 MHz for all observed outputs. Dependence of output amplitude on f_0 in shown in Fig.31(c), it is clear that the output voltage level changes slightly during the tuning processing. Phase shift between V_{02} and V_{03} and phase shift error with -90° are shown in Fig.27(d,e), the ideal phase shift between V_{02} and V_{03} is -90°. From Fig.31(d,e), the maximal phase shift error with -90° is up to ±2.48°.

The amplitude automatic gain control (AGC) circuit in Fig.23 is also necessary for multi-phase oscillator. The input voltage AGC_{INP} is come from port X+ of CDTA2 in the Fig.28 through a load resistor, and the output of AGC is connected to IBB of $CDTA_4$.

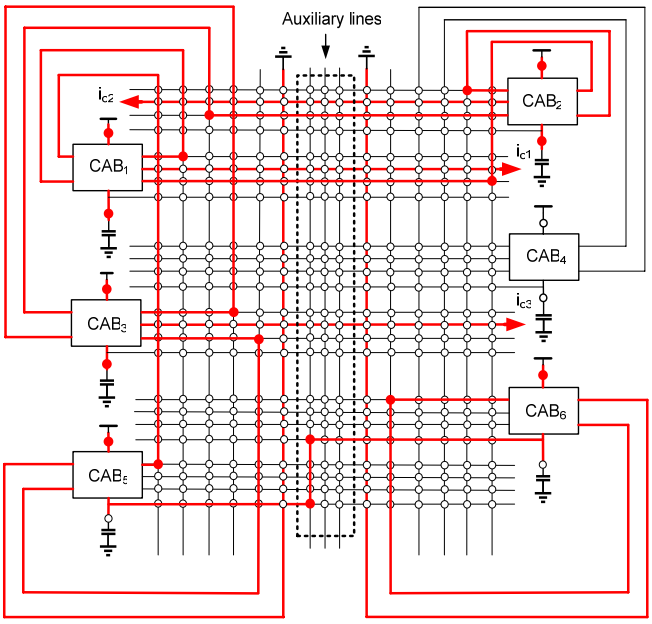


Fig. 29 FPAA-based multi-phase oscillator

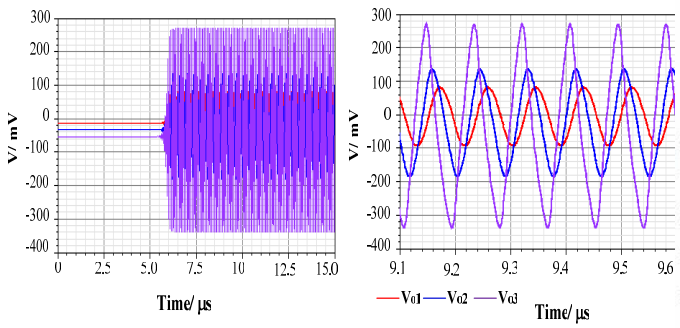
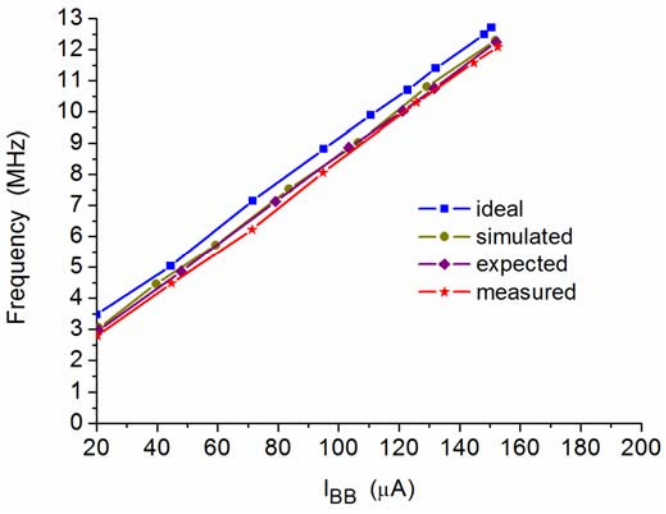
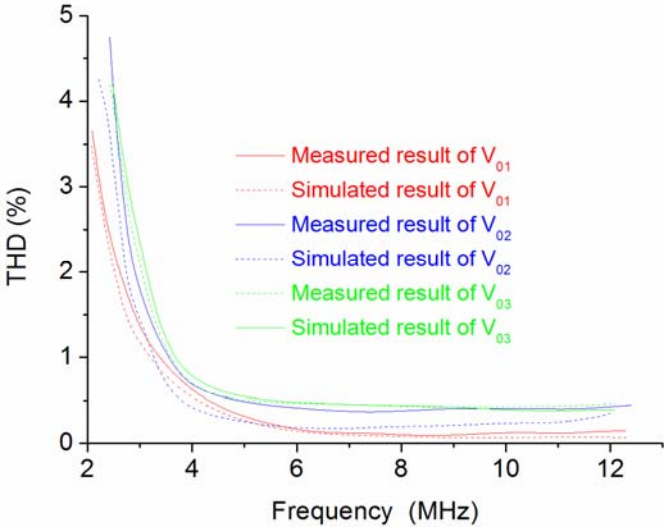


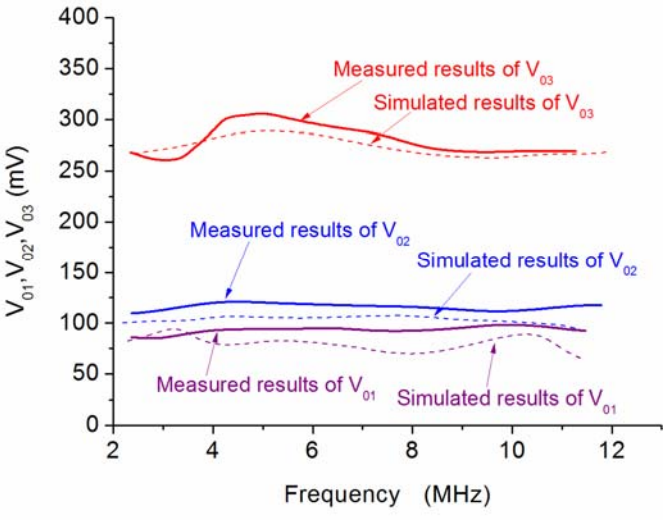
Fig.30 Transient response of the multi-phase oscillator



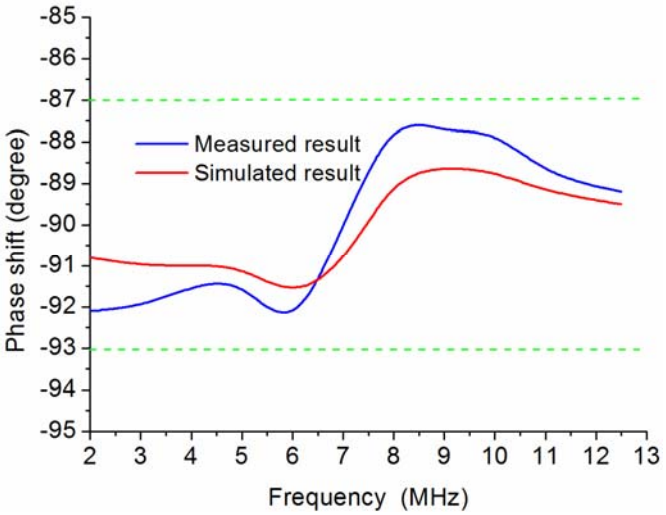
(a) f_0 dependent on IBB



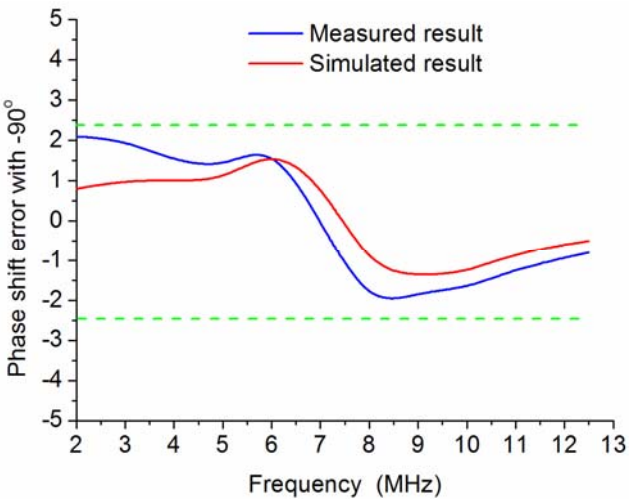
(b) THD dependent on f_0



(c) output amplitude dependent on f_0



(d) phase shift dependent on f_0



(e) phase error with – 90° dependent on f_0

Fig.31 characteristics of the proposed multi-phase oscillator

3.5 The current-mode multiplier and amplitude modulator

Fig.32 is the CDTA-based current-mode multiplier and amplitude modulator. There are four CDTAs used in this

circuit, and this circuit could realize the analog multiplier and amplitude modulator simultaneously. Here, the bias voltage terminal V_b of $CDTA_3$ is not only used as the bias terminal, but also used as the input terminal of the carrier signal.

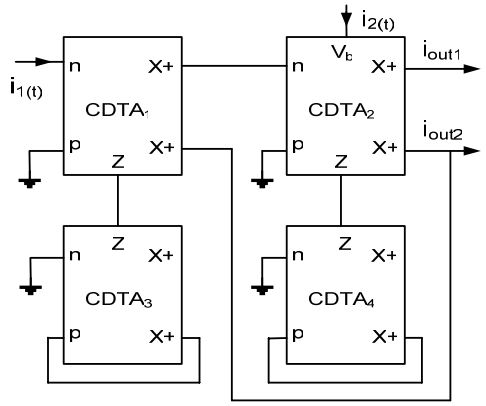


Fig. 32 CDTA-based multiplier and amplitude modulator

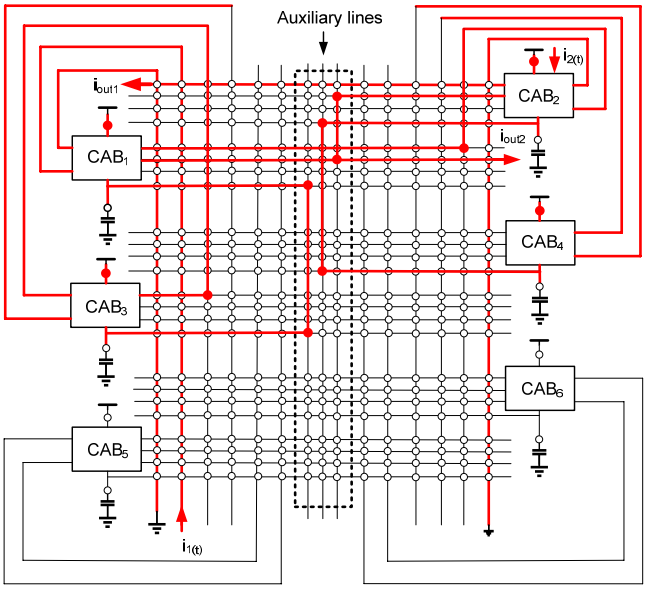


Fig.33 FPAA-based multiplier and amplitude modulator

By a routine circuit analysis using the terminal equation of the CDTA in equation (1), the two output signals of the multiplier and amplitude modulator could be expressed as:

$$i_{out1}(t) = \frac{I_{b2}}{I_{b3}}(1 + \frac{i_2(t)}{I_{b2}}) \tag{22}$$

$$i_{out\,2}(t) = \frac{1}{I_{b3}} i_1(t) i_2(t) \tag{23}$$

From equations (22) and (23), it is clear that i_{o1} is the amplitude modulator output, and i_{o2} is the multiplier output.

Fig.33 is the FPAA realization of the multiplier and amplitude modulator. CAB_1 – CAB_4 are used in the FPAA to realize the multiplier and amplitude modulator, and CAB_5 and CAB_6 are turned off to reduce the power consumption. Fig.34 is the simulation results of the multiplier and amplitude modulator, where I_{BB}=100μA in the circuit. From Fig.34, it is clear that the multiplier and amplitude modulator could realize multiplication and amplitude modulation simultaneously. All the above simulated and measured results are based on the Cadence IC Design Tools 5.1.41.

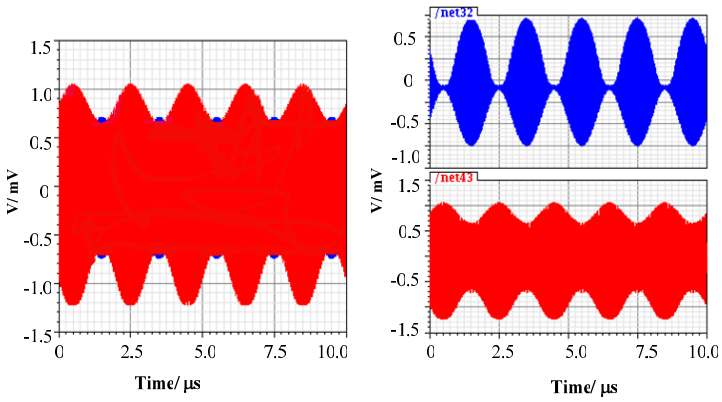


Fig. 34 simulation results of the multiplier and amplitude modulator

4 The chip and its measurement results

The proposed FPAA is realized using standard Charted 0.18μm CMOS technology. Fig.35 is Microphotograph of the chip of the FPAA, which takes a compact chip area of 0.429mm^2 including the testing pads. The measured results of the six order low pass filter, second order universal filter, quadrature oscillator, and multi-phase oscillator based on proposed FPAA are presented in Fig.18, Fig.21, Fig.26 and Fig.30, respectively. Fig.36 and Fig.37 show the laboratory waveforms of the quadrature oscillator and multi-phase oscillator based on the FPAA, respectively. The THD of the simulated results of the quadrature oscillator in Fig.24 is about 1%, and the THD of the simulated results of the multi-phase oscillator in Fig.28 is about 1.3%. The THDs of measured results in Fig.36 and Fig.37 are worse than simulation results. The difference between measured and simulation results is about 7%. Distortion of the sinusoidal output signals as shown in Fig.37 is main due to the 2nd and 3nd harmonic frequency components of multi-phase oscillators [50-52].

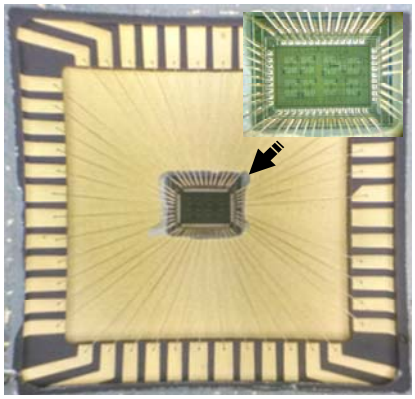


Fig. 35 microphotograph of the chip of the FPAA

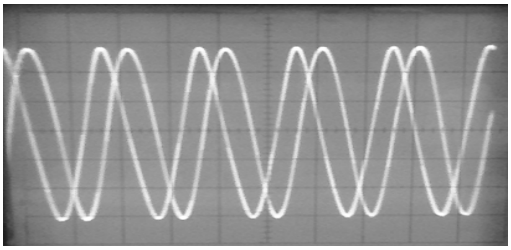


Fig.36 measured results of quadrature oscillator (main characters of the output signals: frequency is about 70MHz, THD is about 1.07%, phase distance is about 91.2 degree, and amplitude is 150 mV/div with IBB=87.5μA.)

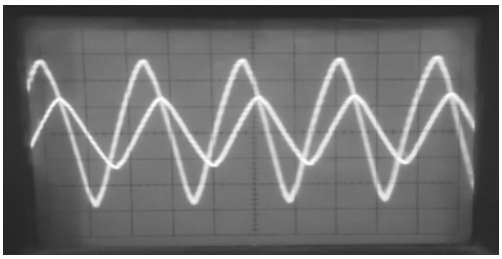


Fig.37 measured results of multi-phase oscillator (main characters of the output signals: frequency is about 11MHz, THD is about 2.13%, phase distance is about 88.8 degree, and amplitude is 100 mV/div with IBB of $CDTA_1$-$CDTA_3$ is set as 87.5μA.)

5 Non-ideal characteristics of CDTA and its second order filter

Considering the input and output impedance, the non-ideal model of CDTA is shown in Fig.38. In Fig.38, Z_{in} and Z_X are input and output impedance of CDTA, respectively. Fig.39 shows the simulated results of Z_{in} and Z_X. According to the results of simulation in Fig.38, we can employ add of R_{in0} and high pass impedance to approximate the input impedance, employ low pass impedance to approximate the impedance of terminal X. Thus, input impedance and the impedance of terminal X can denote the following estimated formulas:

$$Z_{in} = \frac{s^2 R_0}{s^2 - k_1 s - k_2} + R_{in0} \tag{24}$$

$$Z_X = \frac{R_{X0}}{1 + sp_X} \tag{25}$$

where R_{in0} and R_{X0} are resistance of CDTA in low frequency. To simulate the input and output impedance well, appropriate parameters k_1, k_2 and p_x in (24) and (25) should be selected. From Fig.39, we could get R_{X0} = 216 kΩ, R_{in0} = 23.5 Ω, then Z_{in} = 446.8 Ω, so we could calculated the parameters as: p_x = 2.2×10^8, Z_0=1000, k_1=3.77×10^9, k_2 = 3.948×10^{17}.

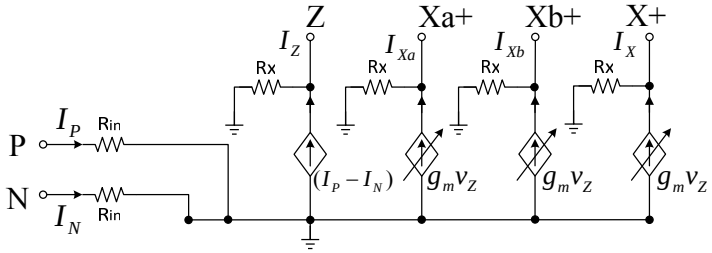
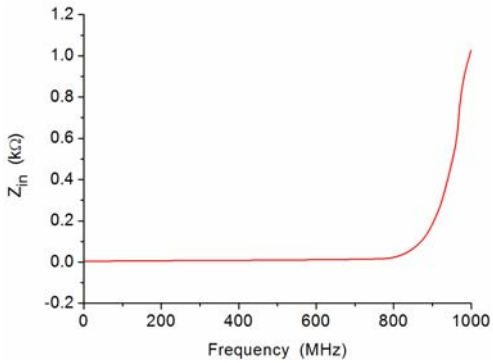
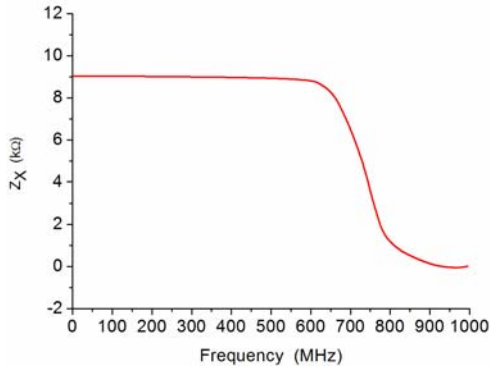


Fig.38 non-ideal model of CDTA



(a)



(b)

Fig.39 (a)input and (b)output impedance of CDTA

To the CDTA-based second order universal filter shown in the Fig.18, using non-ideal CDTA model shown in the Fig3, we can deduce the transfer function of the low pass universal second order filter as follow:

$$\begin{aligned}
H_{lp} =& [C_1C_2R_{X0}^2 g_{m1}g_{m2}(s^2 + k_1 s + k_2)^2]/ \\
&[2R_{in0}^2 p_X^2 s^8 + (4R_{in0}^2 p_X + 3R_{in0}R_{X0}p_X)s^7 \\
&+(2R_{in0}^2 + 3R_{in0}R_{X0}p_X k_1 + 3R_{in0}R_{X0} + R_{X0}^2)s^6 \\
&+(2R_{X0}^2 k_1 + C_2 g_{m2}R_{X0}^2 + 3R_{in0}R_{X0}k_1 + 3R_{in0}R_{X0}p_X k_2)s^5 \\
&+(R_{X0}^2 k_1^2 + 2C_2 g_{m2}R_{X0}^2 k_1 + 2R_{X0}^2 k_2 + C_1C_2 g_{m1}g_{m2}R_{X0}^2 + 3R_{in0}R_{X0}k_2)s^4 \\
&+(2R_{X0}^2 k_1 k_2 + 2C_2 R_{X0}^2 g_{m2}k_2 + C_2 g_{m2}R_{X0}^2 k_1^2 + 2C_1C_2R_{X0}^2 k_1 g_{m1}g_{m2})s^3 \\
&+(R_{X0}^2 k_2^2 + 2C_2R_{X0}^2 g_{m2}k_1k_2 + C_1C_2R_{X0}^2 g_{m1}g_{m2}k_1^2 + 2C_1C_2R_{X0}^2 g_{m1}g_{m2}k_2)s^2 \\
&+(C_2 g_{m2}R_{X0}^2 k_2^2 + 2C_1C_2R_{X0}^2 g_{m1}g_{m2}k_1k_2)s + C_1C_2R_{X0}^2 g_{m1}g_{m2}k_2^2]
\end{aligned} \tag{26}$$

The transfer function (26) contains a two-order zero in right half plane, which is given by:

$$\omega_{z1} = \frac{\sqrt{(k_1^2 + 4k_2)} - k1}{2} = 1.0196\times10^8 \tag{27}$$

Zeros could get +40 dB/dec in amplitude-frequency response, which caused the attenuation decreased in high frequency.

The non-ideal transfer function of band-stop filter is given by:

$$H_{BS}(s) = \frac{s^2 + \frac{g_{m1}g_{m2}}{C_1C_2}K}{s^2 + s\frac{g_{m2}}{C_2}K + \frac{g_{m1}g_{m2}}{C_1C_2}K} \tag{28}$$

where

$$K = \left[R_{in1}(sp_x + 1) + R_{X0} + \frac{R_0(sp_x + 1)s^2}{s^2 + k_1 s + k_2} \right] \quad (29)$$

$$\omega_0 = \sqrt{\frac{g_{m1}g_{m2}}{C_1 C_2}} \quad (30)$$

At the ω_0, the amplitude of transfer function of band-stop filter H_{BS} is minimum, namely, signal amplitude at the ω_0 is decayed at most.

Making $s = j\omega$, $H(j\omega)$ could be get, which is:

$$H(\mathrm{j}\omega) = \frac{1+K}{1+K+K\sqrt{\frac{g_{m2}C_1}{g_{m1}C_2}}} \quad (31)$$

Using MATLAB, the calculated value of (31) could be gotten, and the value is variable with the frequencies, and the variation of attenuation with the change of f is shown in Fig.40, where $\omega = 2\pi f$.

From Fig.40, the attenuation change as f with the change of gm and C (set gm1=gm2=gm, C1=C2=C). When gm changes from 100uS to 1mS, C is changed from 0.1pF to 30pF, f is changed from 3.3 MHz to 1GHz and the attenuation is changed from -35.2 dB to -13.3 dB. It is clear that the attenuation of the band-stop filter become small with frequency increase. From Fig40, it can be seen that the attenuation at about 70 MHz is larger than -20 dB which is agreed with attenuation of band-stop filter in the Fig.21. This explains the CDTA-based second order universal filter in the Fig.18 have no good characteristic of filter in the high frequency range larger than 100MHz.

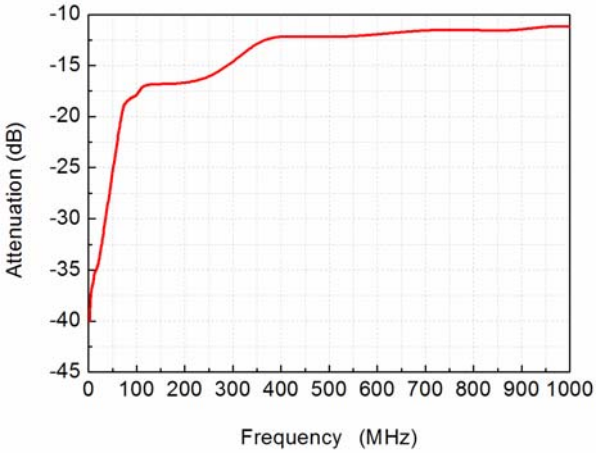


Fig.40 attenuation dependent on f with the change of gm and C

6 Conclusions

A novel CDTA-based versatile butterfly-shaped FPAA is designed in this paper. The proposed FPAA could successively realize six order low pass filter, second order universal filter, current-mode quadrature oscillator, current-mode multi-phase oscillator and current-mode multiplier for analog signal processing. By using the butterfly-shaped topology with meshed vertical input lines and horizontal output lines, there are only six CABs used in the proposed FPAA, which simplifies the complexity of designing of FPAA. Moreover, unnecessary CABs could be shut down by the programmable CAB selection switches, which further reduce the power consumption of the FPAA. It is easy to expand the size of the FPAA by adding CABs in the horizontal and vertical directions of the FPAA, and the excellent scalability of the CDTA-based FPAA is another advantage of the butterfly-shaped FPAA.

7 Acknowledgements

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