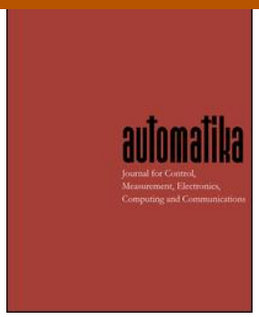

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Time-efficient fault detection and diagnosis system for analog circuits

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ABSTRACT

Time-efficient fault analysis and diagnosis of analog circuits are the most important prerequisites to achieve online health monitoring of electronic equipments, which are involving continuing challenges of ultra-large-scale integration, component tolerance, limited test points but multiple faults. This work reports an FPGA (field programmable gate array)-based analog fault diagnostic system by applying two-dimensional information fusion, two-port network analysis and interval math theory. The proposed system has three advantages over traditional ones. First, it possesses high processing speed and smart circuit size as the embedded algorithms execute parallel on FPGA. Second, the hardware structure has a good compatibility with other diagnostic algorithms. Third, the equipped Ethernet interface enhances its flexibility for remote monitoring and controlling. The experimental results obtained from two realistic example circuits indicate that the proposed methodology had yielded competitive performance in both diagnosis accuracy and time-effectiveness, with about 96% accuracy while within 60 ms computational time.

Vremenski učinkoviti sustav za detekciju kvara i dijagnostiku analognih sklopova. Vremenski učinkovita analiza i dijagnostika analognih sklopova najvažniji su preduvjeti za online monitoring elektroničke opreme koji uključuje kontinuirane izazove sveobuhvatne integracije, tolerancije komponenata, ograničene točke provjere uz višestruke kvarove. U radu je predstavljen analogni sustav za dijagnostiku kvarova zasnovan na FPGA i primjeni dvodimenzionalne fuzije informacija, analizi mreže s dvostrukim priključkom i teoriji intervala. Predloženi sustav ima tri prednosti u odnosu na tradicionalne. Prvo, posjeduje visoku brzinu proračuna i povoljnu arhitekturu sklopa gdje se ugradbeni algoritmi izvršavaju paralelno na FPGA. Drugo, struktura sklopovlja kompatibilna je s drugim dijagnostičkim algoritmima. Treće, postojeće Ethernet sučelje dodatno ističe fleksibilnost sustava za daljinski nadzor i upravljanje. Eksperimentalni rezultati prikupljeni u dva realistična primjera sklopovlja pokazuju da je predložena metodologija rezultirala u kompetitivnim svojstvima dijagnostičke točnosti i vremenske učinkovitosti, uz oko 96% točnosti unutar 60 ms potrebnih za proračune.

KEYWORDS
Fault diagnosis; field programmable gate array (FPGA); orthogonal technique; information fusion; analog circuits

KLJUČNE RIJEČI
Dijagnostika kvara; FPGA; ortogonalna tehnika; fuzija informacija; analogni sklopovi

1. Introduction

From fault dictionary [1–3], parameter identification [4,5] and fault verification [6] before 1990s to following neural network [7,8], fuzzy theory [9] and wavelet analysis [10], the past five decades have witnessed an unprecedented development in the field of analogue detection and diagnosis [11], especially in the study of basis theories, which provide theoretical foundations and probabilistic methods for overcoming the conundrums of component tolerance and nonlinearity. However, with the rapid growth of production technology in electronic circuit domain, the traditional fault diagnosis and detection approaches are costly and time-consuming to some extent, thus cannot wholly satisfy the real-time requirements [12,13]. Moreover, the corresponding platform for these applications is often limited [14]. In order to improve the manufacture efficiency, reduce the maintenance cost and enhance the product quality, the research on real-time and cost-effective fault detection and location system for analog circuits becomes increasingly crucial.

There are certain major difficulties in automatic fault detection and online diagnosis which are presented as follows.

(1) In the analog world, an increasing number of engineers benefit from various Electronic Design Automation (EDA) tools. To be sure, this tool-based simulation methodology helps us to understand the working principles and theoretical characteristics of certain circuits but confined to the small-scale. Hence the large-scale circuit should be divided into many parts, and each analogue sub-circuit is simulated independently, ignoring the correlations between faulty and fault-free ones. Moreover, due to influences of component tolerance, signal crosstalk and ubiquitous electromagnetic interference (EMI) in actual circuit board, the comprehensive fault simulation of complex mixed signal circuits is almost infeasible only relying on current EDA tools.

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(2) The traditional PC-based fault diagnosis system often cannot achieve online detecting and monitoring, because the circuit parameters are continuously sampled at the MHz-level or even GHz-level rate for the large-scale and wide bandwidth diagnostic objects. In such an extremely short period of time, massive data is gathered then transmitted, the real-time computation for uninterrupted health monitoring and fault locating is usually impracticable to PC.
(3) There are lots of fault features in analog circuits, the scientific feature selection strategy is a crucial issue which is hard to build.
(4) Most electronic products are continuously working on the project site which can not be uninstalled for testing. The good sign is that some remote approaches like [15] are arising, but there still exists a long way for us to search.

This research presents a prototype of fault diagnosis system and tries to do some works to overcome the problems described above. The field programmable gate array (FPGA) is by far parallel and highly reconfigurable, permitting rapid prototyping of control mechanisms and new algorithms for pre-research and real-world applications. It has been extensively used in real-time health monitoring of power converter [16], vibration detection and diagnosis [17] and ionizing radiation testing [18] among others due to its parallel data analysis capabilities. Therefore, application of FPGA in analog circuit fault diagnosis and health management field possesses strong vitality, which can not only provide public test-bench for the present fault diagnosis algorithms, also provide the new idea and implementation scheme for fault monitoring and prediction. Unfortunately FPGA, specialized in parallel data processing, is not widely used for analog circuit fault diagnosis and identification in recent literature.

Jurišić et al. proposed a frequency domain approach for single hard fault location, the experimental results carried out from an active fourth-order LP filter proved its effectiveness [19]. Two years later, this diagnosis method was optimized by applying a binary logical manipulation algorithm, this kind of fault dictionary optimization technique was effective to save time in the minimal test frequencies exploring stage [20]. Generalized from these dictionary-based fault analysis approaches in the frequency domain, M. Peng et al. proposed a fault diagnosis method based on circuit gain under different frequencies [21]. Further more in this article, we considered the circuit node voltage, characteristics of amplitude frequency (A–F) and phase frequency (P–F) as the raw circuit features. Then a hardware main-board is built to capture the fault features and compute the fault location. Two application cases aiming at band pass filter and notch filter are also presented, the testing results prove that the FPGA-based scheme and diagnosis approach can provide a compatible test-bench and feasible blueprint for the implementation of recent fault diagnosis theories.

The remaining part of this paper is organized in the following way. Section 2 focuses on extraction strategy of fault features. The system design overview is provided in Section 3. In Section 4, the wideband and synchronous data acquisition approach and orthogonal theory are stated. Section 5 describes the fault diagnosis algorithm then proposes the location regulation, followed by our experimental measurement and related results based on a notch filter. Section 6, finally, presents the conclusion of this research.

2. Requirement analysis about the fault feature extraction

It is the rapid development of automatic control technology and demand of product miniaturization that lead to the promotion of electronics integration and expansion of manufacturing scale. However, this process has inescapable problems such as weld, adhering tin, printed circuit board (PCB) deformation and device parameter fluctuation and so on, all of which become obstacles to the high stability and strong consistency of manufacture. In order to further enhance product integration, simplify PCB design process and shorten the cycle of product development, IC producers like ADI, Silicon LAB and TI supply a great number of monolithic mixed signal processors based on MCU or DSP for specialized analog circuit, then this kind of core can be constructed as a complete system only with a small quantity of passive devices, Undoubtedly, this great development brings out the prosperity of communication and electronic industries, however, the large scale of mixed signal analog circuits make the online fault detection and diagnosis increasingly complex and unwieldy, and how to safeguard the normal operation of electronic devices in real time has become the bottleneck.

In view of the above situation, combined with present circuit diagnosis theories, we aim to build a high performance system for analog fault detection and diagnosis. On the one hand, this system should be equipped with multi-channel high precision signal acquisition and analysis function, which can extract fault features by measuring the accessible node voltage. On the other hand, it should provide arbitrary waveform generator and wide bandwidth acquisition channels, relying on them, we can analyse the input/output characteristics of analog network.

3. Architectural structure design

This section puts forward the hardware scheme of the fault detection and diagnosis platform, its structure diagram is shown in Figure 1, the model of the main processor is XC3SD3400A (belongs to Spartan-3A DSP series, Xilinx). The signal generation part is

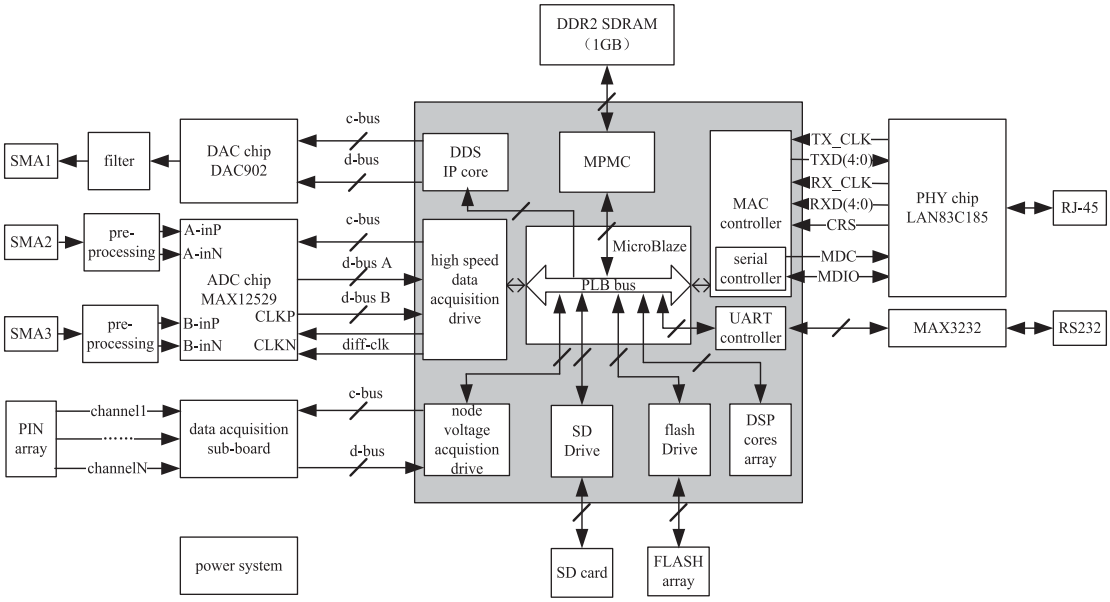

Figure 1. Topology structure of the proposed analogue fault detection and diagnosis system. It is organized according to the direction of signal flow (which is from left to right), and all the modules in the dotted grey box are implemented in FPGA chip.

consist of the digital to analog converter (DAC902, 165Msps/12-Bit) and the direct digital synthesizer (DDS) module. Then, the frequency sweep signal can be generated from SAM1 port, playing a role of the arbitrary signal source for analog circuit under test (CUT). When it comes to the data acquisition part, there are two different signal objects: for AC signals, we choose MAX12529, which is a dual channel signal acquisition chip owning high-performance up to 96Msps/12-Bit, hence the input/output signals of a certain circuit can be captured by this system through SMA2 and SAM3 respectively. For DC signals, in order to simplify design and enhance the flexibility, we developed it as sub-board form, so node voltage can be gathered through the interface of PIN array. As for the DSP cores being constituted with DSP48E slices, LUTs, dual-port block RAMs, and FIFOs, experimenters could rebuild them flexibly for their special design goal. In addition, the system is equipped with sufficient DDR2 SDRAM and Flash memories for computational variables and algorithm operation. Further, the raw gathered information and calculational data can be transmitted to remote host via the flexible Ethernet interface. A 32-bit embedded software processor, MicroBlaze, is used for global management.

4. Detection of fault features

It is widely accepted that the technology of fault diagnosis based on node voltage is becoming more and more mature, which has been studied in a large number of literatures [21,22]. So in this section, we do not repeat it again to avoid cumbersome, but demonstrate the real-time data acquisition and online fault location technologies based on the A–F and P–F characteristics.

4.1. Approaches of amplitude and phase detection

Digital amplitude and phase discrimination is widely used in intermediate frequency (IF) area. Because of the improvement of measurement speed and anti-interference ability, FPGA-based digital intermediate frequency (DIF) system is applied extensively in radar and communication systems [23]. Hence, it is practicable to apply digital methods for analogue fault diagnosis. Generally, large-scale analog circuits, such as multistage operational amplifier and active/passive filter circuits, could be divided as several subnetworks, each two-port subnetwork is connected in head to tail manner. As shown in Figure 2, our detection and diagnosis system generates a controllable signal from interface of SMA 1, acting as a driving source for the whole CUT, then acquires the intermediate signals (y_i) and final signal (y_n) via SMAi and SMAn, these information play the role of diagnostic algorithms. Furthermore, a simple MUX test middleware was developed to support the rotational scanning on the various signals of y_i and y_n, which benefits to the acquisition channel saving for our diagnosis system.

With Microblaze as the controller of the DDS IP core, the frequency, phase and amplitude of the driving signal are programmable and adjustable. The sampling frequency of ADC (MAX12529) was set to 80 MHz for the necessary safety margin, and two ADC channels were equipped in our diagnosis system. If we suppose the expression of the driving signal is $y = sin(\omega t)$, the input and output signal pairs of the subnetwork in Figure 2 can be respectively expressed as $y_1(t) = A_1\ sin(\omega t+\phi)$ and $y_2(t) = A_1A_2\ sin(\omega t+\theta)$, then are imported to the fault detecting system through SMA2 and SMA3. The embedded DSP algorithms in FPGA can calculate the amplitude and phase according

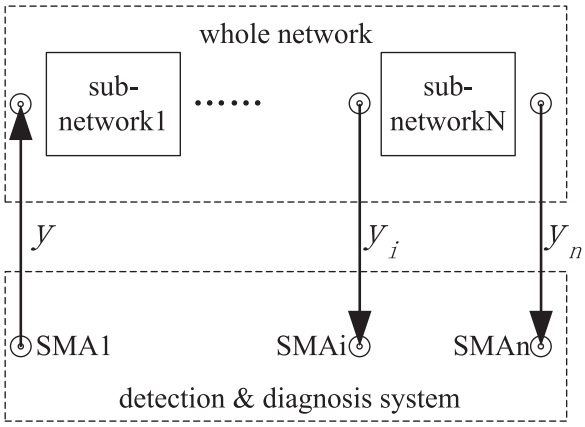

Figure 2. Testing diagram for analog network.

to (1)–(4) using the orthogonal technique.

$$\begin{aligned} k_{11} &= \sum_{n=0}^{N-1} y_1\left(\frac{nT}{N}\right) \times \cos\left(\frac{\omega nT}{N}\right) \\ &= \sum_{n=0}^{N-1}\left(\frac{1}{2}A_1 \sin\left(\frac{2\omega nT}{N}+\phi\right)+\frac{1}{2}A_2\sin\phi\right) \\ &= \frac{N}{2}A_1\sin\phi, \end{aligned} \tag{1}$$

$$\begin{aligned} k_{12} &= \sum_{n=0}^{N-1} y_1\left(\frac{nT}{N}\right) \times \sin\left(\frac{\omega nT}{N}\right) \\ &= \sum_{n=0}^{N-1}\left(\frac{1}{2}A_1 \cos\phi-\frac{1}{2}A_1\cos\left(\frac{2\omega nT}{N}+\phi\right)\right) \\ &= \frac{N}{2}A_1\cos\phi, \end{aligned} \tag{2}$$

$$\begin{aligned} k_{21} &= \sum_{n=0}^{N-1} y_2\left(\frac{nT}{N}\right) \times \cos\left(\frac{\omega nT}{N}\right) \\ &= \sum_{n=0}^{N-1}\left(\frac{1}{2}A_1A_2 \sin\left(\frac{\omega nT}{N}+\theta\right)+\frac{1}{2}A_1A_2\sin\theta\right) \\ &= \frac{N}{2}A_1A_2\sin\theta, \end{aligned} \tag{3}$$

$$\begin{aligned} k_{22} &= \sum_{n=0}^{N-1} y_2\left(\frac{nT}{N}\right) \times \sin\left(\frac{\omega nT}{N}\right) \\ &= \sum_{n=0}^{N-1}\left(\frac{1}{2}A_1A_2 \cos\theta-\frac{1}{2}A_1A_2\cos\left(\frac{2\omega nT}{N}+\theta\right)\right) \\ &= \frac{N}{2}A_1A_2\cos\theta, \end{aligned} \tag{4}$$

where T is the excitation signal period, N is the discretized number of one signal period. As for the theoretical derivation above, choosing certain integral number of periods (suppose K periods for an example) for calculating the average value of each intermediate variable is highly recommended for reducing the system error. Finally, the circuit parameters amplitude (5), phase (6) and network gain (7) can be deduced from (1) to (4).

$$\begin{cases} (1)/(2) \Rightarrow \phi = ac\tan(k_{11}/k_{12}) \\ (1)^2+(2)^2 \Rightarrow A_1 = (2/N)\sqrt{k_{11}^2+k_{12}^2} \end{cases}, \tag{5}$$

$$\begin{cases} (3)/(4) \Rightarrow \theta = ac\tan(k_{21}/k_{22}) \\ (3)^2+(4)^2 \Rightarrow A_2 = \left((2/N)\sqrt{{k_{21}}^2+{k_{22}}^2}\right)/A_1 \end{cases}, \tag{6}$$

$$\text{Network}_{\text{gain}} = A_2/A_1. \tag{7}$$

These parameters can be migrated to host server and observed clearly on the software interface. Consequently, it is possible for us to monitor the components' status and predict the parameter change trend, which mainly results from random environment variation and limited device lifetime. The proposed online detection approach constitutes a favourable foundation and condition for circuit health monitoring, fault location and prediction.

4.2. Two-port network example

A Chebyshev band pass filter is presented as a typical example, although its amplitude–frequency characteristic is not as flat as that of Butterworth type, it is still widely applied in communication projects because of its fast transition band attenuation speed and minimum error compared with frequency response curve of ideal filter. The third-order Chebyshev type II band pass filter is designed as Figure 3, its design objectives are: Centre Frequency is 562 kHz, Pass Band Width is 500 kHz, Stop Band Width is 650 kHz, Stop Band Ratio is 1.3, Stop Band Attenuation is 13.96 dB. Obviously, as a result of the limitation of the capacitance and inductance parameters in engineering application, we have no choice but to choose the nearby ones, besides, the PCB distribution parameters more or less affect the ultra-small parameters of these passive components. What is more, the higher the frequency of these analog circuits is, the more probably the soft faults occur, which are very confused with component legal parameters. As what is concluded from the above that the real-time fault monitoring becomes seriously complex, the proposed orthogonal approach can avoid the obstacles through analysing the transfer characteristics of sub network. With this raw data, we can identify which subnetworks performance has decreased and then locate its related fault component(/s) fusing with node voltage.

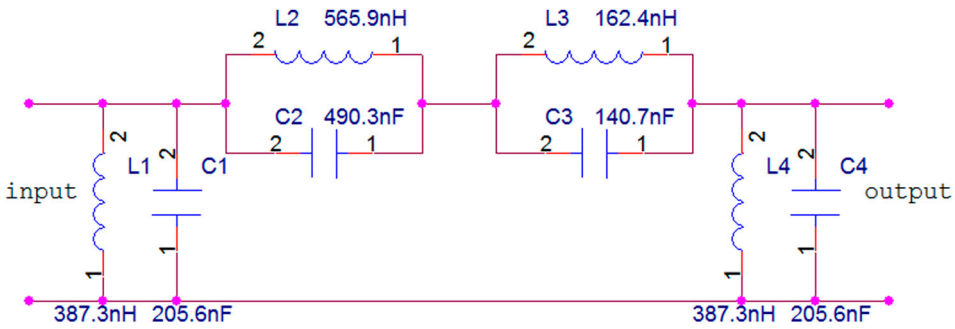

Figure 3. Band-pass filter circuit.

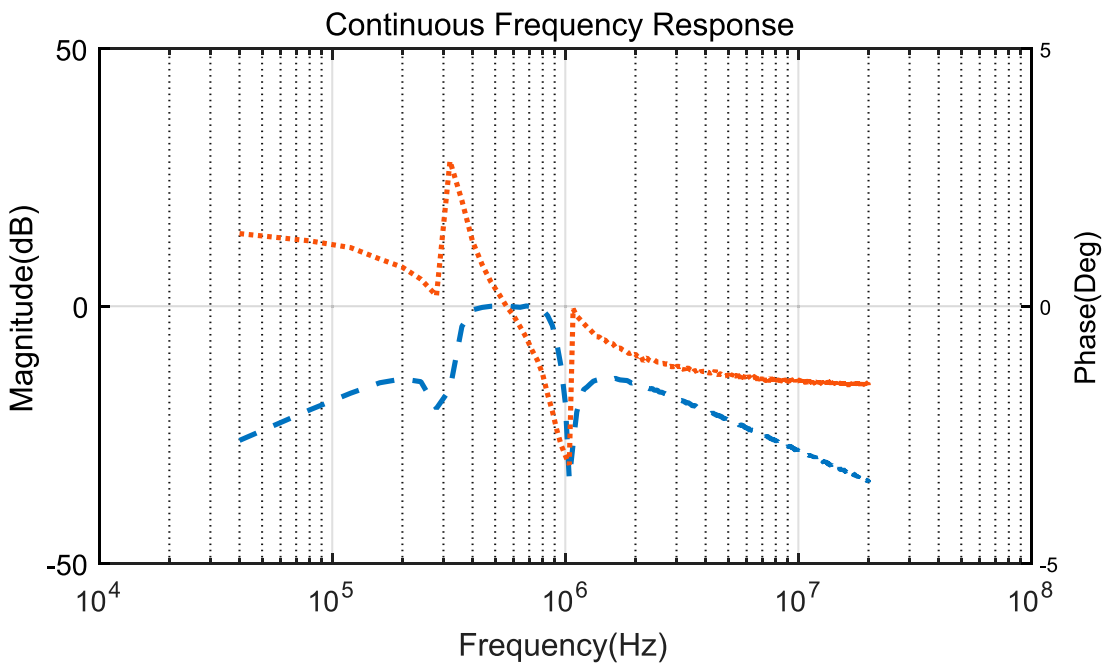

Figure 4. Amplitude–frequency curve and phase–frequency curve.

4.3. Detection results analysis

The frequency of the scan signal varies from 0 Hz to 20 MHz, where the frequency scale is logarithmic and its step equals 0.05. The high-speed data acquisition module captures the network signals through SMA2 and SMA3 after the initialization of DDS module, then the customized DSP cores embedded in FPGA complete the orthogonal calculation according to (1)–(7), finally the computing results are submitted to the host software via Ethernet. The accumulation and multiplication executed in FPGA are real-time, while the calculation for square root and arctangent can be performed by CORDIC (Coordinate Rotation Digital Computer) algorithm which needs only 26 operating clock cycles. Suppose FPGA's main operation frequency is 160 MHz configured by digital clock manage (DCM) module, the delay between feature values output and raw signals input is less than 200 ns, which meets the real-time requirements of detection and tracking for amplitude and phase characteristics. Figure 5 shows the continuous frequency response diagram for the band pass filter from the host software, it can be clearly seen that the band pass filter frequency response achieves the design objectives. Theoretically, most of the hard or soft faults are surely reflected in the frequency response curve [24], if we combined that with the look-up table of node voltage, circuit faults can be quickly analysed and accurately located.

5. Fault diagnosis

5.1. Theories of fault diagnosis

A. Parameter selection of the feature interval vector

Hard fault is considered as a special case of soft fault, the original feature vector (FV) of the circuit is set up by various circuit parameters: node voltage, A–F and P–F characteristics.

$$FV = (fn_1, \ldots, fn_{N1}, fa_1, \ldots, fa_{N2}, fp_1, \ldots, fp_{N3}), \tag{8}$$

where f_n, f_a, f_p respectively stand for the node voltages, characteristics of A–F and P–F, and $N1$, $N2$, $N3$ are the corresponding total number of them. To simplify the derivation, here we define $N1+N2+N3=N$, hence we can rewrite (8) as

$$FV = (f_1, f_2, \ldots, f_N), \tag{9}$$

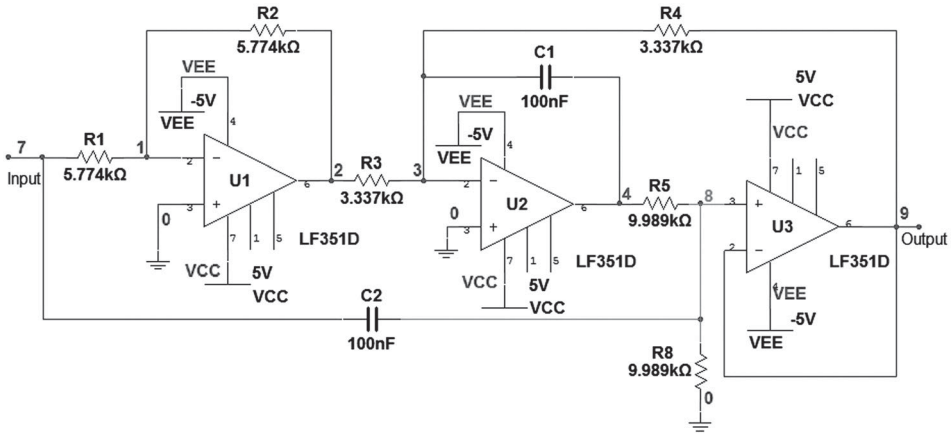

Figure 5. Notch filter circuit as an example.

where $f_j(j=1, \ldots, N)$ is the jth circuit parameter of the feature vector. Then we suppose there are M circuit modes including fault and normal ones, then the feature interval vectors can be defined as

$$FI_i = ((L_{i1}, R_{i1}), (L_{i2}, R_{i2}), \ldots, (L_{iN}, R_{iN})), \quad i = 1, \ldots, M, \tag{10}$$

where L_{ij}, R_{ij} $(j=1, \ldots, N)$ are the lower bound and upper bound of the jth circuit parameter of the ith circuit mode, for a certain circuit, they can be calculated from PSpice with Monte-Carlo method and verified by the data acquisition module designed in Section 4.

B. Circuit similarity of the sample to the feature interval vector

The distinct circuit mode can be reflected by the feature interval vector. Thus the fault diagnosis problem is translated to evaluating the correlation degree between the test sample and the feature interval vectors, which could be represented by the membership degree.

A test sample (TS) is given

$$TS = (ts_1, ts_2, \ldots, ts_N), \tag{11}$$

then, ϵ_{ij} can be defined as "interval similarity" of the TS to the feature interval ($L_{i,j}$,$R_{i,j}$) as

$$\varepsilon_{ij} = \begin{cases} 1, (i,j) \in I \\ 1 - \frac{\eta_{ij}}{\sum_{i=1}^{M} \eta_{ij}}, (i,j) \notin I \end{cases}, \tag{12}$$

where $I = \{(i, j) \mid L_{ij} \le TS_j \le R_{ij}, i = 1, \ldots, M, j = 1, \ldots, N\}$, and η_{ij}, namely the "interval relative distance" of TS to the feature interval ($L_{i,j}$, $R_{i,j}$) is denoted as

$$\eta_{ij} = \frac{\min\{|TS_j - L_{ij}|, |TS_j - R_{ij}|\}}{|L_{ij} - R_{ij}|}, j = 1, \ldots, N. \tag{13}$$

The narrower gaps between TS_j and two boundaries and the larger feature interval, the lower η_{ij} and the larger ϵ_{ij} but within 1. Only when $L_{ij} \le TS_j \le R_{ij}$, the ϵ_{ij} equals to 1. Further, the circuit similarity can be derived as

$$\varepsilon_i = \frac{1}{N} \sum_{j=1}^{N} \varepsilon_{ij}, i = 1, \ldots, M, \tag{14}$$

which stands for the circuit similarity of the TS to the ith feature interval vector under information fusion of N circuit parameters.

C. Information fusion-based diagnosis principle

Theoretically, only considering single kind of circuit parameters would trigger fuzzy diagnostic results as a result of the component tolerance [24], so an information fusion techniques involving multiple features are used in our work.

According to the frequency sweeping method, we choose the whole testing bandwidth as 20 MHz (Mega Hertz), the total number P of the selected frequency points equals 146 which calculated from (15), and the frequency logarithm step is 0.05.

$$P = (1/0.05)\log(20\,\text{MHz}) = 146. \tag{15}$$

Then a circuit similarity matrix is denoted as

$$\Gamma = \begin{bmatrix} \varepsilon_{11} & \varepsilon_{12} & \cdots & \varepsilon_{1P} \\ \varepsilon_{21} & \varepsilon_{22} & \cdots & \varepsilon_{2P} \\ \vdots & \vdots & \ddots & \vdots \\ \varepsilon_{M1} & \varepsilon_{M2} & \cdots & \varepsilon_{MP} \end{bmatrix}, \tag{16}$$

where ϵ_{ik} $(i=1, \ldots, M$ and $k=1, \ldots, P)$ is circuit similarity, M and P are the totality of circuit modes and the discrete frequencies. If suppose that the reliability of different input with selected frequency is

$$W = (\omega_1, \ldots, \omega_P)^{\mathrm{T}}, \tag{17}$$

then the final similarity of the TS to circuit modes can be rewritten as

$$\varepsilon = \Gamma \times W = [\varepsilon_1, \varepsilon_2, \ldots, \varepsilon_M]^{\mathrm{T}}, \tag{18}$$

Algorithm 1 Identifying the faults of analog circuits.

Input: The current similarity vector ε_{cur} to be handled.
Output: Fault status (*FS*), equals "1" if be suffered with fault(s).
Main procedure:
1. Initialize the $FS = 0$, calculating the maximum final similarity $\varepsilon_{\max 1}$, the second maximum final similarity $\varepsilon_{\max 2}$, the average value of all final similarities ε_{avg} from ε_{cur}
2. ***IF*** $\varepsilon_{\max 1} > \delta$ and $\varepsilon_{\max 2} - \varepsilon_{\max 1} > \theta$
3. $FS = 1$
4. ***ELSEIF*** $\varepsilon_{\max 1}/\varepsilon_{avg} > \lambda$
5. $FS = 1$
6. ***ELSE***
7. $FS = 0$
8. ***ENDIF***
9. Return *FS*

where

$$\varepsilon_i = \sum_{k=1}^{P} \varepsilon_{ik}\omega_k, i = 1, \ldots, M. \tag{19}$$

Applying the predefined ϵ_i in (14), ϵ_i defined in (19) stands for the final similarity of the *TS* to the *i*th circuit mode using information fusion of *N* parameters of circuits obtained from *P* frequency points.

Refer to [24], ω_k $(k=1, \ldots, P)$ in (17) could be defined as

$$\omega_k = \alpha_k\beta_k / \sum_{k=1}^{P} \alpha_k\beta_k, \alpha_k = \max_{i=1,\ldots,M}\{\varepsilon_{ik}\}, \beta_k$$
$$= \alpha_k / \sum_{i=1}^{M} \varepsilon_{ik}.$$

The larger the final similarity, the higher is the probability that the corresponding component is the fault one. And it is widely accepted that the maximum and the second maximum final similarities of ϵ_i $(i=1, \ldots, M)$ possess higher fault probability. The pseudo codes of fault diagnostic rules is presented in Algorithm 1. The reason of fuzziness would be that some distinct fault modes take the same or similar maximum values of final similarity, while our adopted information fusion-based techniques suppressed these fuzzy decisions to large extent, through considering three basically independent kinds of significant circuit features.

5.2. Diagnosis example circuit

The notch filter is popularly used in the fields of radar and sonar, communication, measuring instruments, etc. owing to the selective characteristic for specific frequency band [25–27]. In order to evaluate the real-time efficiency and computing capacity of the realized system, we have diagnosed the notch filter circuit in Figure 6 [27], the component parameters are given in Figure 6 and the parameter precision is 1%, the trap centre frequency is 275.6 Hz. The input node 7 and output node 9, together with intermediate nodes 1, 2, 3, 4 and 8 are selected as accessible nodes, thus, the voltage

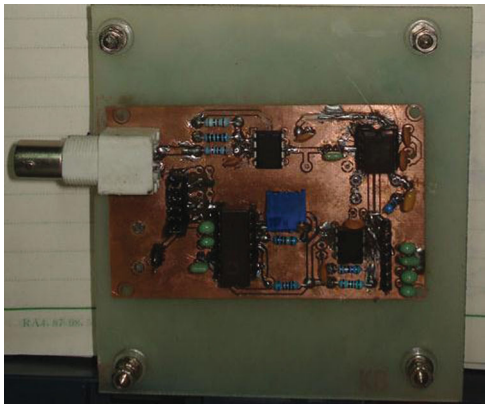

Figure 6. The actual circuit of notch filter.

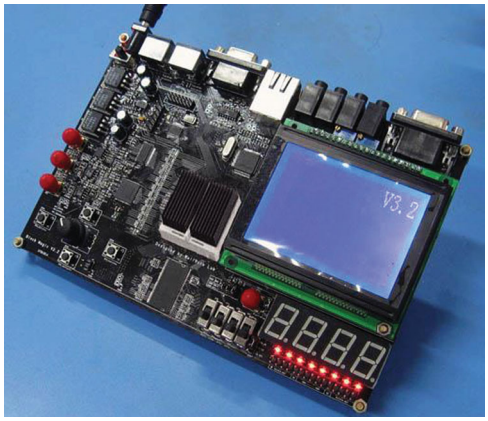

Figure 7. The FPGA-based dignosis platform.

of accessible nodes V7, V9, V1, V2, V3, V4, V8 constitute a kind of test signal. And the A–F and P–F characteristics are captured by the MAX12529 as another two kinds of test signals. Consequently, the value of the circuit parameters *N* defined in (9) equals 9. The photograph of its actual circuit has given in Figure 7.

5.3. Diagnosis results and further analysis

In the literature [28], Peng et al. selected A–F characteristic as a set of feature information for fusion technology by selecting six frequency points from the limited frequency range (0–45 kHz), and combined with the traditional node voltage detection technology, the correct diagnosis rate after fusion was increased by approximately 10% than that using one single information. Furthermore in this paper, we choose the node voltage, A–F and P–F characteristics distributed in the whole bandwidth from 0 to 20 MHz as three kinds of fusion information. Figure 7 gives the designed test platform.

We suppose that there is an independent relationship between each hard fault of the notch filter shown in Figure 5, then all the faults can be divided into two types:

(i) 16 kinds of hard faults caused by single component open-circuit or short-circuit;

Table 1. Segment of test results based on single frequency F_1 and information fusion method F_2.

		Location result									
Fault category	Diagnosis method	*N*	R1	R2	R3	R4	R5	R8	C1	C2	Fuzziness
N	F_1	45	7	4						2	6 (R1,R2)
	F_2	64									
R1↑	F_1	6	47	9							2 (R1,R2)
	F_2		62	2							
R2↑	F_1		8	51	1						4 (R1,R2)
	F_2		2	61							1 (R1,R2)
R3↓	F_1			3	42	7			2		10 (R3,R4)
	F_2				59	2					3 (R3,R4)
R4↑	F_1				9	44			3		8 (R3,R5)
	F_2				1	61					2 (R3,R4)
R5↓	F_1						48	9	2	1	4 (R5,R8)
	F_2						62	2			
R8↓	F_1						11	46		4	3 (R8,C2)
	F_2						3	61			
C1↓	F_1				3	7	4		41		9 (C1,R4)
	F_2					3			58		3 (C1,R4)
C2↑	F_1						3	6		49	6 (C2,R8)
	F_2						1	3		60	

(ii) 64 kinds of soft faults resulted from parameter variation considering $|\Delta X_j|/X_j$ $(j = 1, 2, \ldots, 8)$ as 0.02, 0.1, 10 and 50.

Then the total value of the circuit modes M defined in (10) equals 81 including the normal one. It is convenient to change waveform kinds or increase the number of testing samples by using the frequency sweep method with DDS technology. So we generated 210 excitation signals to calculate the feather interval vectors, then 64 of which are chosen as the test samples to identify the efficiency and accuracy of diagnosis algorithm, According to the training method based on neural network proposed in [28], the decision thresholds chosen in this algorithm are $\delta = 0.82$, $\sigma = 0.18$, $\lambda = 1.75$.

Results presented in Table 1 illustrate the comparison details between the single frequency method at 1258.93 Hz (derived from $10^{0.05*62}$) and the fusion method based on 146 frequency responses defined in (15), and we define the two methods as F_1 and F_2 in Table 1. It can be clearly seen that method F_1 has a lower rate of accuracy and more fuzziness, while applying method F_2 these figures are improved dramatically. The reason is that the feature interval vectors of different frequency responses have complementary information especially to this kind of non-linear or approximately linear network, which can be fused to a more reliable location conclusion.

Table 2 indicates that the proposed information fusion approach can increase the diagnosis accuracy reliably, the final average accuracy rate is high up to approximately 96%. At the same time, because of the parallel data processing ability provided by FPGA, the total time consumption is no more than some 60 ms. In addition, as a result of the wide bandwidth (0–20 MHz) and real-time fault decision mechanism, the proposed scheme and implemented system possess strong vitality and adaptability for fault diagnosis and location of analog circuit.

Table 2. Fault diagnosis performance evaluation.

Category (based on)	Rate of correctness (%)	Rate of mistake (%)	Rate of refusal (%)	Time consumption (ms)
Node voltage	75.46	23.19	1.35	18.7
A–F	71.28	19.08	9.64	34.5
P–F	69.52	20.29	10.19	36.3
Fusion	97.54	2.15	0.31	57.6

6. Conclusion

A real-time and cost-effective fault detection and diagnostic methodology for analog circuits has been realized on the customized FPGA platform, and its abundant acquisition channels gather the accessible node voltages, information of amplitude–frequency and phase frequency of analog circuits. It can identify the hard and soft faults reliably with around 96% detection rate, benefiting from the information fusion, orthogonal techniques and interval math theory based on multiple circuit features. When compared with the traditional PC-based approach, our diagnosis method is more efficient as a result of the speedy and parallel data processing ability provided by FPGA. The offered Ethernet interface facilitates the remote monitoring and controlling in production which is superior to the RS232 interface in [29] to some extent. However, because the neural network-based training method is computationally complex, we have to spend a certain time expense on the calculation of the decision thresholds δ, σ and λ. Our another PCI express blade system equipped with larger resource FPGA is currently being developed, which is expected to be able to reduce the training time consumption. And improving the algorithm on hardware programming plays the significant part in real-time diagnosis, which also needs further research.

Disclosure statement

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