RF energy harvesting from multi-tone and digitally modulated signals

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***Abstract*—This paper presents the design of an RF energy harvesting circuit when excited by signals with a time-varying envelope such as multi-tone signals or digitally modulated signals with random modulation. The input matching network and the output load of a rectifier circuit are simultaneously optimized using harmonic balance in order to maximize its RF-dc conversion efficiency. The paper focuses on identifying the optimum load value which corresponds to maximum efficiency for different types of input signals. The efficiency curves versus the load value show a single optimum efficiency point, which is a different for signals with a time-varying envelope and continuous wave (CW) signals. Specifically, for the series diode rectifier which was considered, the optimal load shifts to larger values as the signal peak-to-average-power-ratio (PAPR) increases compared to a CW signal with the same average power. As a result, for certain load values a signal with a time-varying envelope can result in a larger efficiency value than a CW signal. The peak efficiency value does not necessarily improve by using a signal with a time-varying envelope. A UHF rectifier prototype is built and its performance is evaluated experimentally showing good agreement with simulation.**

***Index Terms*— wireless power transfer, rectifier, harmonic balance, multi-tone, RF-dc conversion efficiency, optimization.**

I. Introduction

THE RF-dc conversion efficiency of rectifier circuits has been the object of numerous research works due to the recent interest in wirelessly powered circuits for radio frequency identification (RFID) and other low power sensor applications as part of the Internet-of-Things (IoT) [1], and the application potential of energy harvesting [2] and wireless power transfer technologies [3]. A typical but non-exhaustive list of examples covers different frequency bands from high frequency (HF) applications to optical waves [4], wideband [5] or multi-band [6] performance, harmonic terminations [7], [8], as well as different types of devices operating as rectifiers including Schottky diodes [9], transistors [7] and tunnel diodes [4] to name a few.

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In addition to the matching network and device selection, recent works have focused on the performance of rectifiers by considering different types of signals. In earlier works the rectifier efficiency was studied in the case of two-tone signals with different tone frequency separation [5]. The use of power optimized waveforms [10], [11] or multi-tone signals [12], [13] was investigated and it was shown that signals with high peak to average power ratio (PAPR) may lead to a higher RF-dc conversion efficiency compared to a continuous wave (CW) signal with the same average power. Furthermore, the performance of rectifier circuits under randomly modulated signals has been evaluated experimentally in [14], [15], [16], [17][18]. The time-varying envelope of such signals leads to a non-zero frequency bandwidth, which requires a proper design of both the input impedance matching network and the output low pass filter of the rectifier [19][20].

In this work we optimize using harmonic balance the RF-dc efficiency performance of a series diode rectifier under signals with time-varying envelope. While previous works focused on the performance versus the average power and bandwidth of the input signals, this work focuses on identifying the optimal load resistance. Furthermore, a theoretical model is provided and a closed form for the optimal load is obtained for CW signals. It is seen that the optimal load leading to a maximum RF-dc conversion efficiency shifts to a different value depending on the PAPR of the input signal. Specifically for the circuit under consideration it shifts to larger values as the signal PAPR increases compared to a CW signal with the same average power. As a result, depending on the selected load value a signal with a time-varying envelope can lead to a larger efficiency than a CW signal. Furthermore, the maximum possible efficiency value is not necessarily larger than the one which can be obtained using a CW signal, obtained however at a different load value. A prototype UHF rectifier was designed and fabricated and its performance under different multi-tone and randomly modulated signals and load values was investigated, showing good agreement with simulation.

The paper is structured as follows: in section II, the theoretical background is presented and the simulation and optimization goals are defined. In section III, the various input signals with time-varying envelope used in this work are defined. In section IV simulation and measurement results are presented, and in section V the conclusions from this work.

II. Theoretical Analysis

There is a significant amount of literature regarding the theoretical performance analysis of rectifier circuits. Earlier works focus on diode based power detectors [13], while more recent publications focus on the performance as RF-dc power conversion circuits in wireless power transfer [9], [22], [23] or RFID applications [21], [25]. A harmonic expansion using modified Bessel functions is often used for the diode current [21], [23], [24], while the dc power is evaluated by averaging over the input signal period [21], [23], [24], [25]. In [9], [22] a diode model including a series resistance and a parallel combination of a nonlinear resistance and capacitance was used to model a single shunt diode rectifier connected to a load. The voltage across the diode nonlinear resistance was modeled as a constant voltage drop when the diode is on and a harmonic signal containing a dc term and a fundamental frequency term when the diode is off. A harmonic expansion using dc and fundamental frequency terms was used for the nonlinear capacitor, the linear diode resistance, and the total voltage across the shunt diode and rectifier load. The rectifier efficiency was evaluated by averaging over a single fundamental period of the input signal excitation. In [7] analysis was presented for harmonically terminated diode and transistor rectifiers and in [26] fundamental limits of diode rectifier RF-dc conversion efficiency were demonstrated. Proper harmonic termination can lead to a maximum theoretical efficiency of 100 % [7][26]. Recently theoretical limits of rectifier efficiency under power optimized waveform input signals were studied [11].

In this work, harmonic balance simulation is used to analyze and optimize a series diode rectifier circuit. A source with a resistance R_s is connected to an impedance matching network with a desired harmonic impedance profile, and then in series with a Schottky diode D, followed by a shunt capacitor C_L and resistive load R_L, shown in Fig. 1. The source resistance and impedance matching network provide a desired impedance Z_s to the rectifier circuit in order to maximize its RF-dc efficiency. The rectifier efficiency η_A is defined as the ratio of the dc power $P_{L,dc}$ delivered to the output load R_L over the average available RF power from the source P_A.

$$\eta_A = \frac{P_{L,dc}}{P_A} \tag{1}$$

Alternatively an efficiency expression η using the input RF power can be used [15]. η_A represents a lower bound of η ($\eta_A \leq \eta$).

A harmonic balance simulation with 7 harmonics has been setup in a commercial simulator. A nonlinear Schottky diode model has been considered corresponding to the Skyworks SMS7630 diode. The main parameters of the model are a nonlinear resistance R_j, a nonlinear capacitance C_j and a series resistance R_{ds} = 30 Ω shown in Fig. 1c. The diode saturation current is I_s = 5 μA and a breakdown voltage V_B = 2 V. The diode ideality factor is n = 1.05. The diode package parasitics are L_p = 0.6 nH and C_p = 0.25 pF.

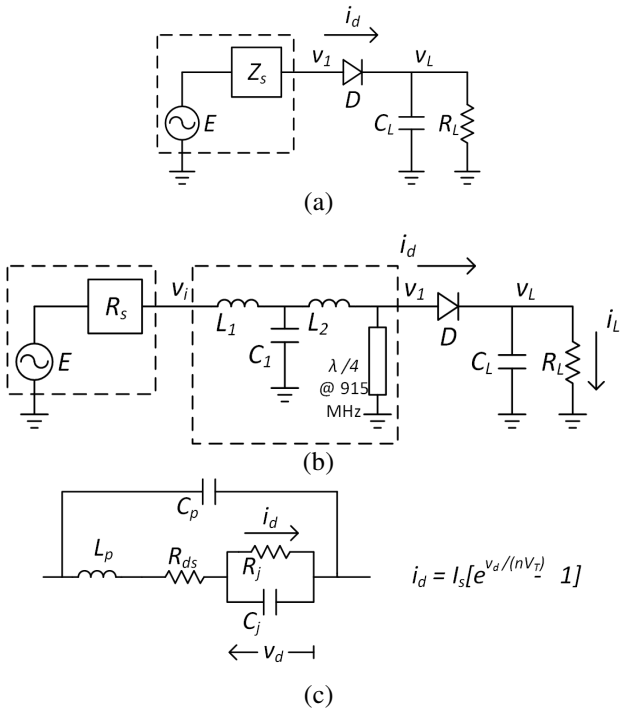


Fig. 1. Block diagram of the rectifier setup in harmonic balance, a) general model of the source, rectifier and output filter, b) model including source, matching network with harmonic termination, rectifier and output filter, c) Schottky diode model.

A. Model Definition

In this section an ideal diode is considered with $R_{ds} = C_j = 0$, V_B = 100 V, and $L_p = C_p = 0$. The load capacitance is sufficiently large (10 nF) so that v_L consists only of dc voltage. In order to derive an approximate model for the rectifier, the following is considered:

$$v_1(t) = V_{10}(t) + \sum_{n=1}^{N} V_{1n}(t)\cos(n\omega_o t) \approx V_{11}(t)\cos(\omega_o t) \tag{2}$$

$$v_L(t) = V_{L0}(t) + \sum_{n=1}^{N} V_{Ln}(t)\cos(n\omega_o t) \approx V_{L0}(t) \tag{3}$$

$$i_d(t) = I_{d0}(t) + \sum_{n=1}^{N} I_{dn}(t)\cos(n\omega_o t) \approx I_{d0}(t) + I_{d1}(t)\cos(\omega_o t) \tag{4}$$

$$i_L(t) = I_{L0}(t) + \sum_{n=1}^{N} I_{Ln}(t)\cos(n\omega_o t) \approx I_{L0}(t) \tag{5}$$

Due to the assumption of an ideal diode model (without considering its capacitance), and that C_L is large, only resistive terms are considered leading to the fact that the harmonic voltages and currents are in-phase and no sinusoidal terms are included in the expansions (2), (3), (4) and (5). The first equation (2) relies on the fact that the stub of the matching network (Fig. 1b) leads to zero dc and even harmonic voltage components at the input of the diode and it is assumed that odd harmonic voltage components are very small compared to the fundamental voltage. Similarly, it is assumed that the

output capacitor C_L, minimizes the fundamental and harmonic components of the output voltage. The phasors of the harmonic expansions (2) and (3) are allowed to be time-varying in order to accommodate signals with a time-varying envelope.

The application of Kirchoff's voltage law at the input of the diode gives

$$e(t) = i_d(t)R_s + v_1(t) \Rightarrow E(t) = I_d(t)R_s + V_{11}(t) \quad (6)$$

where $e(t) = E(t)\cos(\omega_o t)$. Given a source with amplitude *E(t)*, source resistance R_s and available average power P_A, one has

$$\langle E \rangle = \sqrt{8P_A R_s} \quad (7)$$

where $\langle \quad \rangle$ denotes time average.

The diode current is

$$i_d(t) = I_s\left[\mathrm{e}^{\alpha(v_1 - v_L)} - 1\right] \quad (8)$$

where $\alpha = 1/(nV_T)$ ($V_T = kT/q$ is the thermal voltage, n the diode ideality factor, k the Boltzman constant, T the junctions temperature and q the electron charge). Similarly to [24], and using (2), (3) and the modified Bessel function of the first kind $\mathrm{B_n}$ series expansion [27]

$$\mathrm{e}^{z\cos x} = B_0(z) + 2\sum_{n=1}^{+\infty} B_n(z)\cos(nx) \quad (9)$$

one obtains a set of two coupled nonlinear equations for the rectifier diode current

$$I_{d0}(t) = I_s\left[\mathrm{e}^{-\alpha V_{L0}(t)} B_0\left(\alpha V_{11}(t)\right) - 1\right] \quad (10a)$$

$$I_{d1}(t) = 2I_s \mathrm{e}^{-\alpha V_{L0}(t)} B_1\left(\alpha V_{11}(t)\right) \quad (10b)$$

The diode current includes the current flowing into the load resistance R_L and load capacitance C_L and therefore

$$I_{d0}(t) = I_{L0}(t) + C_L \dot{V}_{L0}(t) \quad (11)$$

where the dot $\dot{}$ indicates time derivative. Using $V_{L0}(t) = I_{L0}(t)R_L$ applying (11) in (10a), (6) in (10a) and letting $y = \alpha V_{L0}$, $x_L = \alpha I_s R_L$, $x_s = \alpha I_s R_s$, $z_1 = \alpha V_{11}(t)$, $z_e = \alpha E(t)$, $\tau = \alpha R_L C_L$ and $B_0 = B_0(z_1)$, one obtains the coupled system of nonlinear differential algebraic equations

$$z_e(t) - z_1(t) = 2x_s B_1(z_1) e^{-y(t)} \quad (12a)$$

$$y(t) + \tau\dot{y}(t) = x_L B_o(z_1) e^{-y(t)} - x_L \quad (12b)$$

where $z_e(t)$ represents the external forcing term (source). Using (10b) one may also calculate the input RF impedance of the rectifier R_1

$$R_1(t) = \frac{V_{11}(t)}{2I_s \mathrm{e}^{-\alpha V_{L0}(t)} B_1\left(\alpha V_{11}(t)\right)} \Rightarrow$$

$$x_1(t) = \frac{z_1(t)}{2\mathrm{e}^{-y_L(t)} B_1\left(z_1(t)\right)} \quad (13)$$

where $x_1 = \alpha I_s R_1$, $B_0 = B_0(z_1(t))$.

One may further assume without loss of generality that the capacitor C_L is sufficiently large that the output voltage essentially consists of a dc term and a small varying term, $y = y_L + y_t(t)$ with $y_t(t) \ll y_L$ and let $e^{-y(t)} \approx e^{-y_L} - e^{-y_L} y_t(t)$. Applying the above approximation in (12), and additionally setting $B_0(z_1(t)) = \langle B_o \rangle + b_o(t)$ results in

$$z_e(t) - z_1(t) = 2x_s B_1(z_1) e^{-y_L} - 2y_t(t) x_s B_1(z_1) e^{-y_L} \quad (14a)$$

$$y_L = x_L \langle B_o \rangle e^{-y_L} - x_L \quad (14b)$$

$$y_t(t)[1 + x_L\langle B_o\rangle e^{-y_L}] + \tau\dot{y}_t(t) = x_L\langle B_o\rangle e^{-y_L}\left(1 - y_t(t)\right)b_o(t) \quad (14c)$$

It is possible to solve (14b) for y_L by making the transformation $y_L = t - x_L$ and using the Lambert *W* function [24] $q = te^t \Leftrightarrow t = W(q)$, obtaining

$$y_L = W_0(x_L \mathrm{e}^{x_L}\langle B_0\rangle) - x_L \quad (15)$$

Due to the even symmetry of the modified Bessel function of the first kind of order 0, $B_0 = B_0(z_1(t)) = B_0(|z_1(t)|) > 0$, the argument of the Lambert function in (15) is always positive and the principal branch $\mathrm{W_0}$ of the Lambert function is used. The non-linear algebraic differential equation system (12) or (14) may be solved by numerical integration. Equation (15) presents an interesting result showing that the average value of $\langle B_0(z_1(t))\rangle$ together with the output load R_L determine the output dc voltage y_L, however it also requires to numerically solve (14) in order to obtain $z_1(t)$. Despite the benefit of (12) and (14) to provide insight into the factors that determine the optimum rectifier performance, due to its complexity a commercial harmonic balance simulator is used in this paper to optimize the performance of the rectifier under signals with a time-varying envelope.

Using the ideal diode model, the optimal load resistance $x_m = \alpha I_s R_{Lm}$ obtained with harmonic balance optimization versus the input average available power P_A for $R_s = 50\ \Omega$ and $R_s = 3\ \mathrm{k\Omega}$ is shown in Fig. 2 for various multi-tone signals. One can see that for low source resistance values the optimal load is reduced as the input average available power increases, and furthermore for a fixed average available power it can reduce further as the number of tones increases. However, for a high source resistance value the behavior is different and for a fixed input average available power the optimal load increases with the number of tones. One should consider that R_s is the equivalent source resistance at the input of the rectifier and consequently, a matching network which acts as an impedance transformer from e.g. a source resistance of 50 Ω to a larger value of the input rectifier resistance in order to achieve maximum power transfer, determines the

variation of the optimal load resistance with respect to the input power.

B. Optimal Load for Continuous Wave (CW) Signals

In the event a CW source signal is used, one may assume all harmonic amplitudes in (2),(3),(4) and (5) to be non-time varying, which results in a steady state with $b_0 = y_t = 0$ and the system of equations (14) becomes a nonlinear algebraic system

$$z_e - z_1 = 2x_s B_1(z_1) e^{-y_L} \tag{16a}$$

$$y_L = x_L B_o e^{-y_L} - x_L \tag{16b}$$

and

$$y_L = W_0(x_L \mathrm{e}^{x_L} B_0) - x_L \tag{17}$$

One may combine (17) and (16a) to get

$$z_e - z_1 = \frac{2x_s}{x_L}\frac{B_1(z_1)}{B_0(z_1)} W_0(x_L \mathrm{e}^{x_L} B_0(z_1)) \tag{18}$$

Given z_e, it is possible to solve numerically (18) for z_1 and then determine y_L.

The output dc power is $P_{L,dc} = V_{L0}^2/R_L$, and using (16b) it is evaluated as

$$P_{L,dc} = \frac{I_s}{\alpha} y_L (B_0(z_1)\mathrm{e}^{-y_L} - 1) \tag{19}$$

The value of $y_L = y_m$ which leads to a maximum dc output power is calculated by taking the derivative of (19) with respect to y_L and setting it equal to zero. It is straightforward to find that y_m fulfils

$$B_0 - y_m C = \mathrm{e}^{y_m} \tag{20}$$

with

$$C = B_0 - \frac{dz_1}{dy_L} B_1 \tag{21}$$

where $dB_0(z)/dz = B_1(z)$ [27] was used. The derivative of z_1 with respect to y_L is found by differentiating (16a) as

$$\frac{dz_1}{dy_L} = \frac{z_e - z_1}{1 + \frac{B_0 + B_2}{2B_1}(z_e - z_1)} \tag{22}$$

with $B_2 = B_2(z_1)$ and $2dB_1(z)/dz = B_0(z) + B_2(z)$ [27].

Solving (16b) for e^{y_L} and substituting its value in the right hand side of (20) one finds a relation between the optimal (normalized) voltage y_m and the optimal load $x_L = x_m$ as

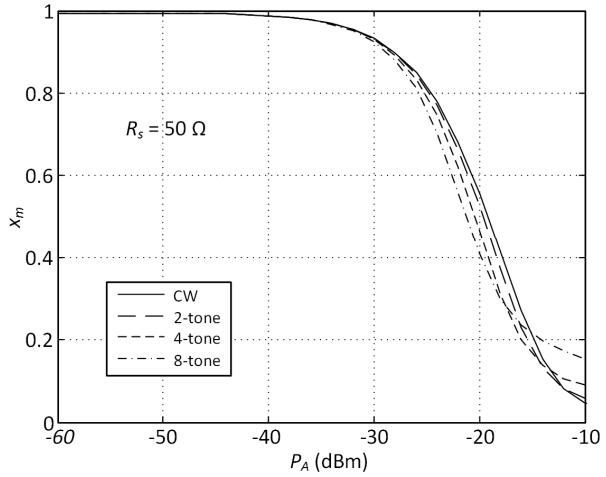
$$x_m + y_m = \frac{B_0}{C} \tag{23}$$

Equation (20) is solved by making the transformation $y_m = B_0/C - t$ and using the Lambert W_0 function [21] $q = t\mathrm{e}^t \Leftrightarrow t = W(q)$, to obtain

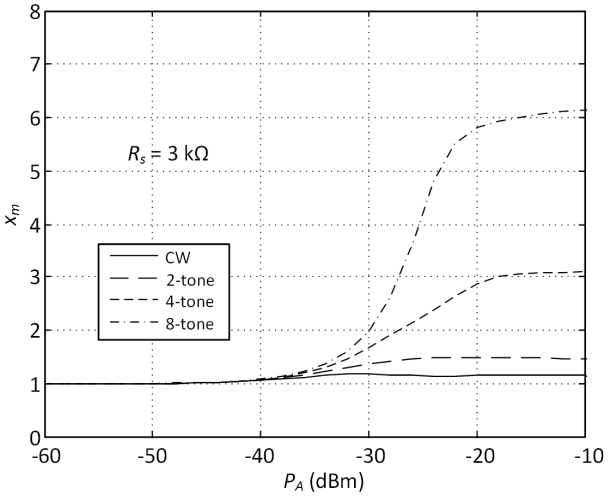
$$y_m = \frac{B_0}{C} - W_0\left(\frac{e^{B_0/C}}{C}\right) \tag{24}$$

which using (23) gives

$$x_m = W_0\left(\frac{e^{B_0/C}}{C}\right) \tag{25}$$



(a)



(b)

Fig. 2. Optimal load resistance versus input available average power for different multitone signals and source resistance values.

The maximum dc output power is then

$$P_{Lm} = \frac{I_s}{\alpha}\frac{\left(\frac{B_0}{C} - W_0\left(\frac{e^{B_0/C}}{C}\right)\right)^2}{W_0\left(\frac{e^{B_0/C}}{C}\right)} \tag{26}$$

Using (23) in (17) one has

$$CW_0(x_m e^{x_m} B_0) = B_0 \tag{27}$$

which is applied in (18) to obtain

$$(z_e - z_1)CW_0\left(\frac{e^{B_0/C}}{C}\right) = 2x_s B_1(z_1) \tag{28}$$

A given input available average power P_A and a given source resistance x_s define z_e and (28) can be solved numerically to find z_1 corresponding to optimal load x_m, optimal output dc voltage y_m, and optimal dc output power P_{Lm}, which can be then evaluated using (25), (24) and (26) respectively.

In Fig. 3, the optimal dc load x_m resistance and optimal input RF resistance x_{1m} are plot versus the available average power P_A and different source resistance values R_s. One can see that as the input average available power goes to zero both the optimum input resistance and the optimum load become

$$\lim_{P_A \to 0} x_m = x_{m0} = 1 \Rightarrow R_{Lm0} = \frac{1}{\alpha I_s} \tag{29a}$$

$$\lim_{P_A \to 0} x_{1m} = x_{1m0} = 1 \Rightarrow R_{1m0} = \frac{1}{\alpha I_s} \tag{29b}$$

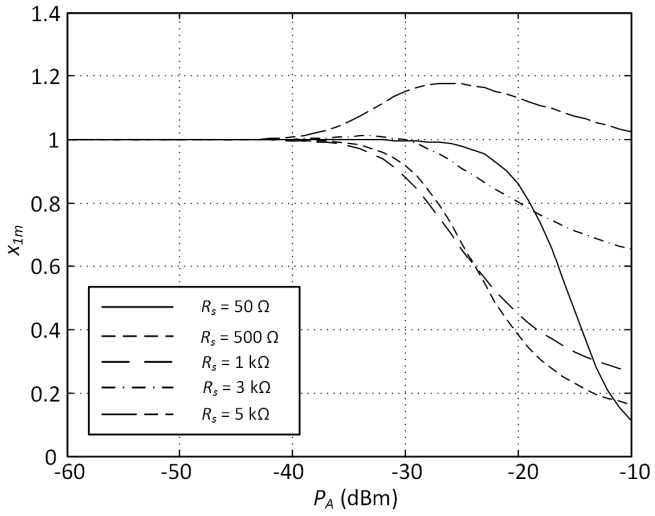
The diode model under consideration with I_s = 5 μA, n = 1.05, V_T = 25.85 mV at 300 K, gives $R_{Lm0} = R_{1m0} = 5.43$ kΩ. One can see from Fig. 3 that as P_A increases, depending on the source resistance R_s, the optimal load can vary significantly relative to R_{Lm0} (or x_{m0}). In fact, for low R_s values the optimal load decreases with increasing P_A, but for large R_s values comparable to R_{Lm0} the optimal load value can increase with the input power P_A above R_{Lm0}. This is consistent with the results of the previous paragraph obtained using harmonic balance simulation for multi-tone signals.

In order to verify (25) the optimal load resistance was also evaluated in harmonic balance simulation using commercial software by performing a sweep of the load resistance for four P_A values and $R_s = 50$ Ω and $R_s = 3$ kΩ, showing excellent agreement (Fig. 3b).

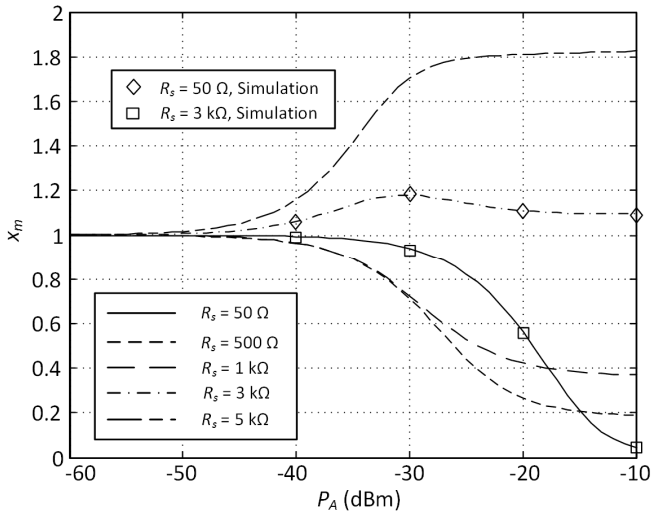
III. Signals with Time-Varying Envelope

Signals with time-varying envelope are characterized by their peak-to-average-power ratio (PAPR). The complementary cumulative distribution function (CCDF) represents the probability or the fraction of time that the instantaneous power of a signal has a value larger or equal than the CCDF argument. The argument of CCDF is typically presented as the ratio (in dB) of a considered power level over the average power [29]. The PAPR of a signal was evaluated as the argument of its CCDF function with value 0.001 %.

The measured CCDF of various multi-tone signals with 2, 3, 4, and 8 tones and their corresponding PAPR values is shown in Fig. 4. The measurements were performed using a Keysight ESG 4438C Digital Vector Signal Generator with multitone signal generation capability and a Vector Signal Analyzer (VSA) running on a PSA E4448A Spectrum Analyzer as a receiver. A tone frequency spacing of 0.5 MHz was used. The CCDF and PAPR depend on the relative phases between the tones and it is maximum for a relative phase distribution with a constant progressive phase shift among neighboring tones. The simplest form of this condition is when all tones are in-phase (0 relative phase shift). It is straightforward to show that the maximum theoretical PAPR is equal to 10*log10(*N*) where *N* is the number of tones [30]. One can set the PAPR (dB) of a multi-tone signal within an interval [0, 10*log10(*N*)] by modifying the relative phase shift among the different tones [25], [26]. In Fig. 5, the measured CCDF of a 2 tone signal with zero phase shift is compared to the CCDF of a 4 tone signal with relative tone phases θ_1 = 0 °, $\theta_2 = \theta_3 = \theta_4$ = 180 °, and one can see that they have similar PAPR.



(a)



(b)

Fig. 3. Optimal a) input RF resistance, and b) load resistance for different input available average power and source resistance values.

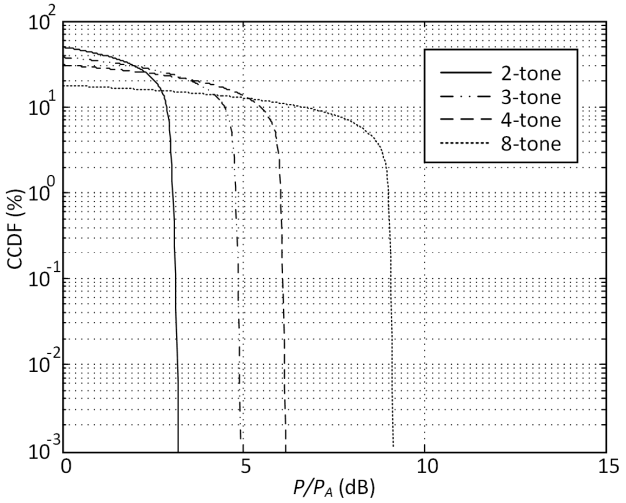


Fig. 4. Measured CCDF and PAPR of multi-tone signals.

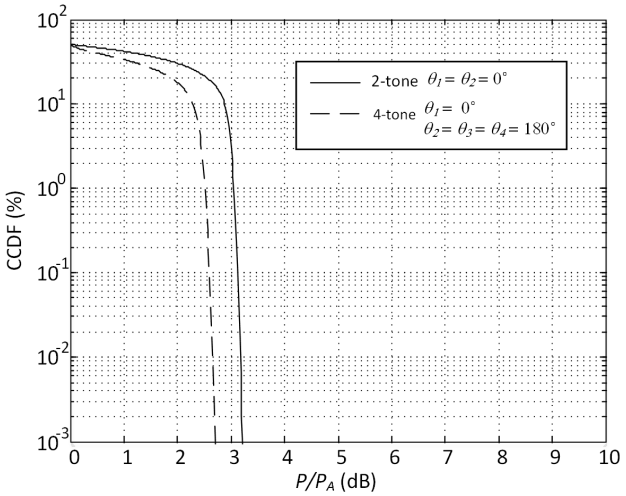


Fig. 5. Measured CCDF and PAPR of a 2-tone signal with in-phase tones and a 4-tone signal with phases $\theta_1 = 0$ °, $\theta_2 = \theta_3 = \theta_4 = 180$ °.

The measured CCDF of various randomly modulated signals is shown in Fig. 6. The signals were generated using the same setup as the multi-tone signals. A symbol rate of 0.5 MSPS was used and the transmitted pulses were filtered using a raised cosine filter of roll-off factor β. The roll-off factor has a strong effect on PAPR as shown in Fig. 7.

Finally, in Fig. 8, we present measurements of the CCDF of a 4-tone signal with in-phase tones and a 64QAM signal with $\beta = 0.5$. Both signals have the same PAPR value but their CCDFs are different. The CCDF of the 4-tone signal shows that it has more peaks of at least 2 dB above its average power than the QPSK signal. In the next section we investigate how the PAPR and CCDF of a signal input to a rectifier affects the RF-dc conversion efficiency with respect to the rectifier load and for different average input power levels.

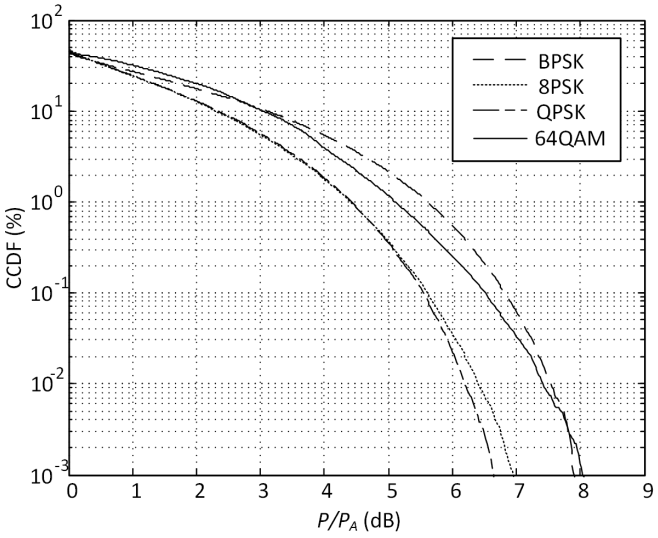


Fig.6. Measured CCDF of modulated signals with $\beta = 0$.

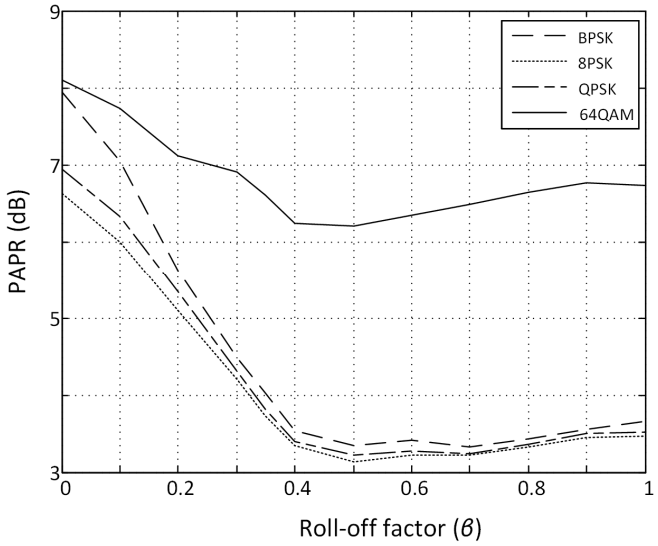


Fig. 7. Measured PAPR for different roll-off factors β.

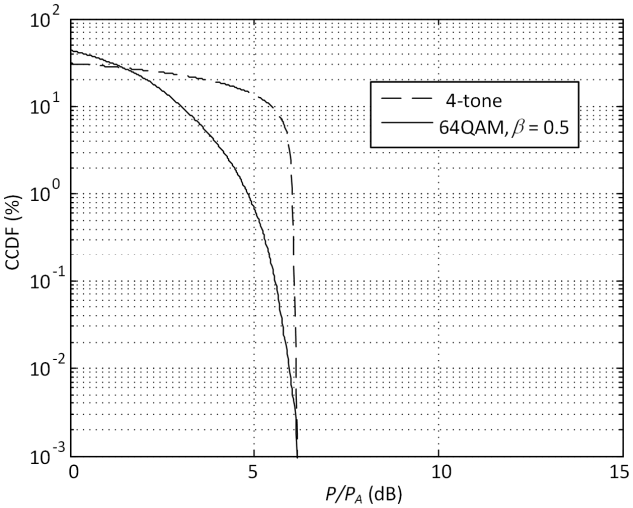


Fig.8. Measured CCDF comparing a 4-tone signal with in-phase tones and a 64QAM signal with $\beta = 0.5$.

IV. RF-DC Efficiency Optimization and Measurements

A 915 MHz series diode rectifier was designed using Keysight ADS. The Skyworks SMS7630 diode was used as the rectifying device. The circuit diagram is shown in Fig. 1b. The input matching network includes a shorted stub placed at the input of the diode, followed by a T-type matching network made from off-the-shelf inductors and a capacitor. The shorted stub is a quarter wavelength long at the fundamental frequency of 915 MHz. It presents an open circuit at 915 MHz. The stub additionally provides a short at dc, a short at the second harmonic and an open at the third harmonic frequency. The rectifier is matched using lumped inductors (Coilcraft) L_1 = 3.3 nH, L_2 = 43 nH and capacitor (Murata) C_1 = 3 pF. At the output of the rectifier a shunt capacitor of 10 nF (Murata) is used, while a trimmer resistor 0 Ω – 20 kΩ is used as the rectifier load. The prototype was built on 20 mil thick Arlon A25N substrate with dielectric permittivity 3.38 and loss tangent 0.0025 (Fig. 9). The effect of the substrate and layout was simulated using Keysight Momentum, while s-parameter files were used for the inductors and capacitor provided by the manufacturers.

TABLE I
Optimum Matching Network and Load for Different Input Signals (P_A = -20 dBm)

Symbol	Value (CW)	Value (2-tone)	Value (4-tone)	Value (8-tone)
L_1 (nH)	8.62	4.01	7.26	5.87
L_2 (nH)	51.05	48.3	50.01	47.4
C_1 (pF)	4	3.45	3.38	2.68
R_L (kΩ)	3.67	4.631	7.415	12.38
Eff (%)	29.123	28.83	28.56	29.036

TABLE II
Optimum Matching Network and Load for Different Input Signals (P_A = 0 dBm)

Symbol	Value (CW)	Value (2-tone)	Value (4-tone)	Value (8-tone)
L_1 (nH)	14.43	12.35	10.88	9.017
L_2 (nH)	58.41	56.08	53.498	49.89
C_1 (pF)	2.389	2.478	2.457	2.168
R_L (kΩ)	1.682	2.369	5.118	8.997
Eff (%)	67.849	62.434	59.174	59.48

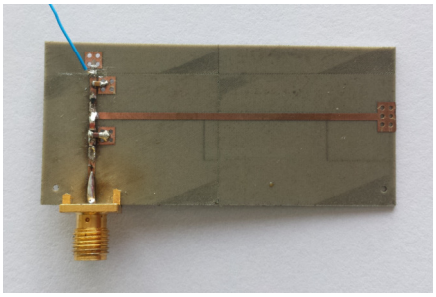


Fig. 9. Photo of the fabricated rectifier prototype.

The matching network together with the output load was simultaneously optimized to maximize the efficiency at a fixed P_A = -20 dBm and for a given input signal. A tone spacing of 0.5 MHz was considered in order to ensure that the rectifier operates within the bandwidth of the matching network and that the output capacitor C_L combined with the output load provides sufficient filtering.

Table I and Table II show ideal values of the matching network components optimized for maximum efficiency and using a different number of tones for P_A = -20 dBm and P_A = 0 dBm respectively. The values highlight the main result of this work which is the fact that the optimum load value depends (specifically for this circuit it increases) with the number of tones and consequently with increasing PAPR. Furthermore, the optimum load value decreases with increasing input average power. The peak efficiency values depend strongly on power P_A. The peak efficiency is reduced at high power levels P_A for signals with high PAPR due to the diode breakdown voltage.

In order to verify the obtained results, a rectifier was simulated by selecting the optimum matching network values for the 4-tone case and re-optimizing the circuit using non-ideal s-parameter models for the inductors and the capacitor. In order to better observe the effect of input power and load resistance, constant efficiency contours of 20 % and 40 % were simulated for various multi-tone signals in Fig. 10. It is seen that the 20 % efficiency contour is shifted towards larger load values with increasing number of tones or PAPR. The 40 % efficiency contour is also shifted towards higher load values with increasing number of tones. However, the 40 % contour area is also reduced with higher PAPR due to the fact that higher efficiency requires a larger input power but losses due to the diode breakdown voltage limit the load and power range. The efficiency limitation due to effect of the breakdown voltage is clearly seen in the upper right side of the contours towards higher power and load values which lead to larger voltages across the diode.

The rectifier efficiency was measured for varying loads and selected input power levels in Fig. 11. There is good agreement between measurement and simulation. The optimum load value is slightly reduced with increasing average power and it increases with increasing PAPR. Due to the different optimum load values, there is a range of loads where signals with higher PAPR than a CW signal can produce a better RF-dc efficiency. As an example, at P_A = -20 dBm input average power, the RF-dc conversion efficiency of the rectifier using a 4-tone signal is higher than that of a CW signal for load values above 3 kΩ.

The peak efficiency value depends on the various sources of loss present in the circuit. Specifically, as the input power increases the breakdown voltage of the diode becomes critical because the presence of peak values of instantaneous power can drive the diode into the breakdown region. This is evident in Fig. 11, where for very low input average power levels (-20 dBm) the presence of the power peaks can lead to a higher peak efficiency but for high input average power levels (0 dBm) the presence of the power peaks reduces the achievable maximum efficiency.

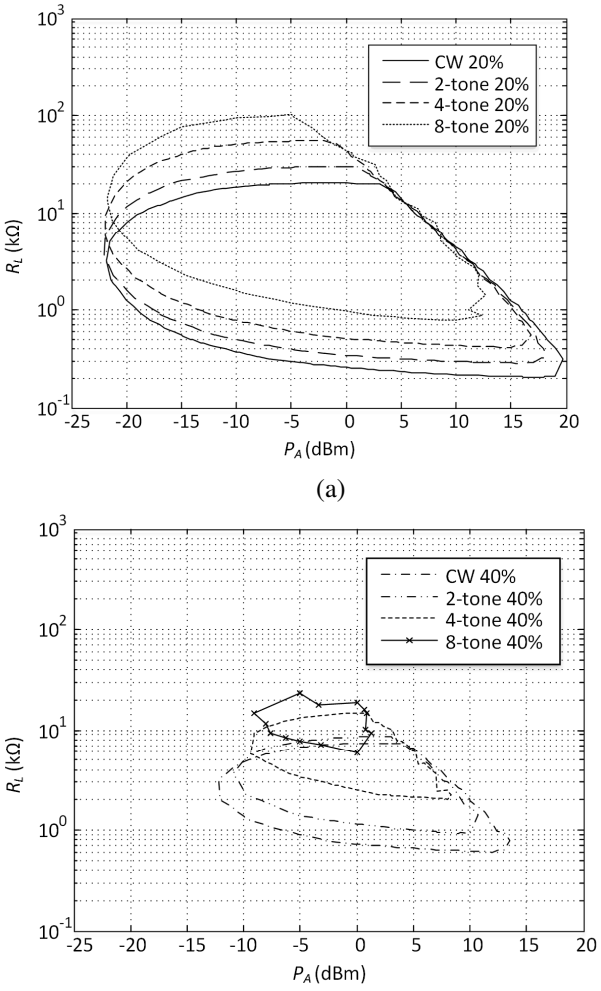


Fig. 10. Simulated contours of RF-dc efficiency a) 20% and b) 40 %.

The value of the load resistance affects the input power matching and therefore the input s-parameters of the rectifier were measured for different load values in order to verify that a satisfactory matching condition is maintained and the variation in efficiency is primarily due to the input signal properties and the load and not due to mismatch. The results are shown in Fig. 12, where one can see that a return loss better than 10 dB is maintained at 935 MHz for load values between 1 kΩ and 10 kΩ. It is also seen from Fig. 12 that the manufactured prototype presented an offset of 20 MHz in frequency performance which is in the order of 2% and it is attributed to fabrication errors and component yields. It should be noted that the s-parameter measurement is done using a CW signal and an instantaneous s-parameter measurement should ideally be considered for the case of multi-tone signals in order to draw a more accurate conclusion.

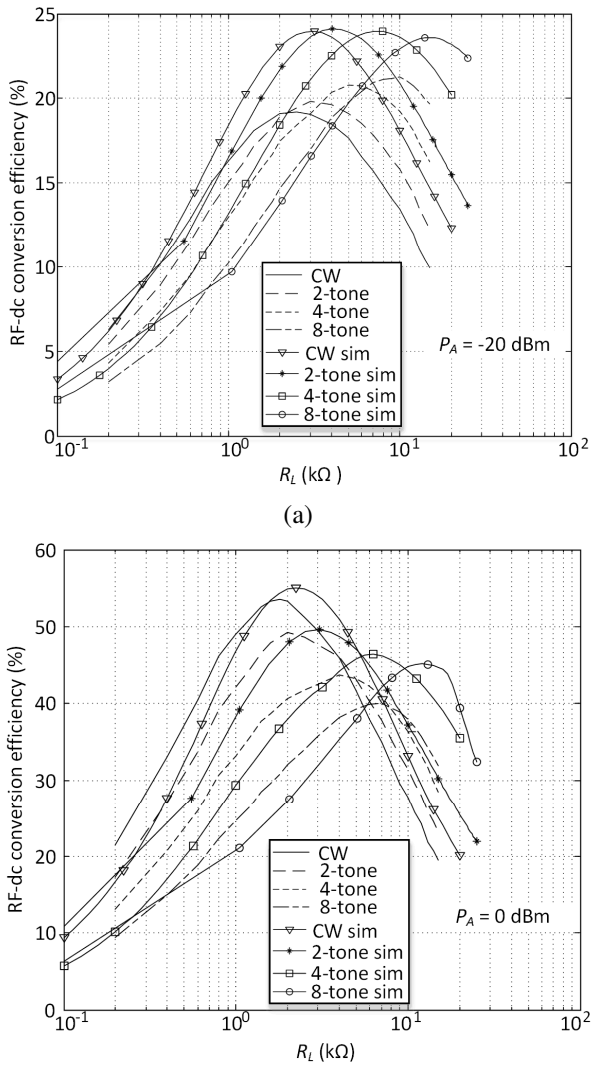


Fig. 11. RF-dc efficiency of multi-tone signals versus R_L, a) P_A = -20 dBm, b) P_A = 0 dBm.

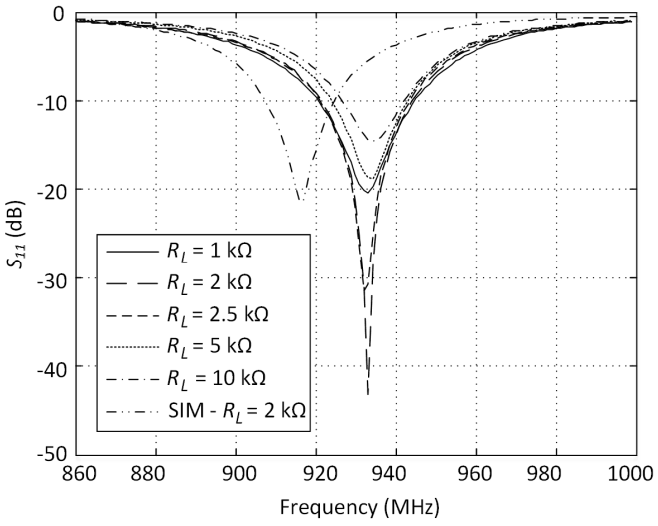
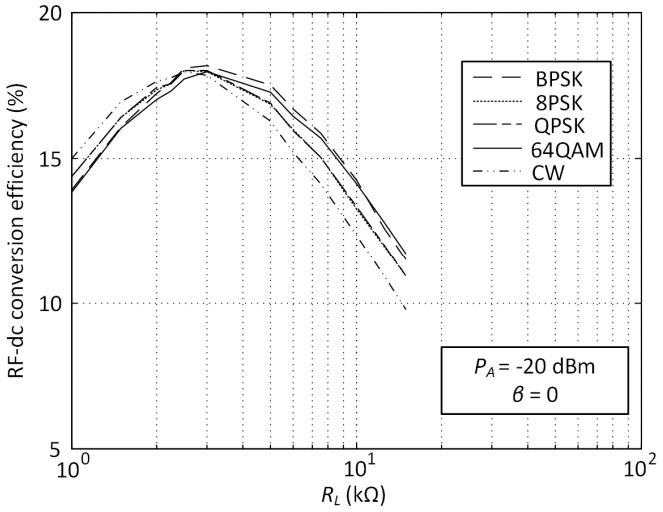
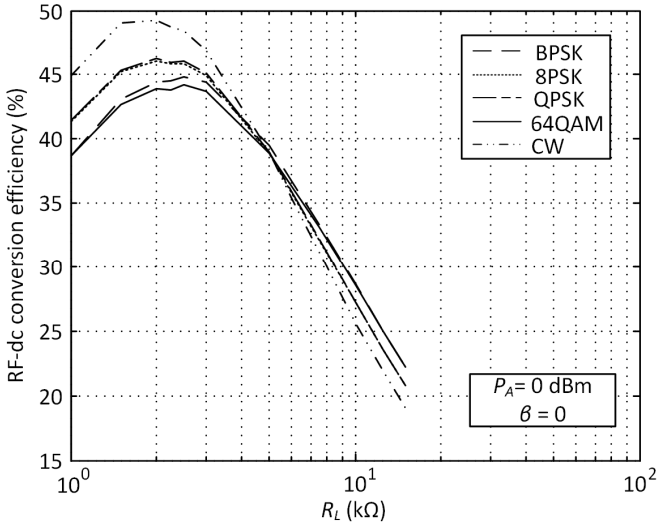


Fig. 12. Input s-parameters of the rectifier for different loads.

The variation of the RF-dc conversion efficiency was also investigated for the case of randomly modulated signals. The results are plotted in Fig. 13 showing a similar trend for increasing PAPR. The optimal load shift is smaller relative to the multi-tone case due to the smaller variation of the PAPR (Fig. 6).



(a)



(b)

Fig. 13. Measured RF-dc efficiency of randomly modulated signals with symbol rate 0.5 MBPS versus R_L, a) P_A = -20 dBm, b) P_A = 0 dBm.

Finally, we compare the RF-dc conversion efficiency of different signals with a similar PAPR. The first example consists of a 2-tone signal with in-phase tones and a 4-tone signal with tone phases θ_1 = 0 °, θ_2 = θ_3 = θ_4 = 180 °, whose CCDF plot was shown in Fig. 5. The obtained RF-dc efficiency, shown in Fig. 14, is similar for the two signals and slightly higher for the 2-tone signal which has a larger PAPR. The second example consists of a 4-tone signal with in-phase tones and a 64QAM signal with β = 0.5, which have the same PAPR but different CCDF curves as shown in Fig. 8. One can see in Fig. 15 that due to the difference in the CCDF curves of the two signals a different load value which leads to maximum efficiency is obtained. Furthermore, due to the fact that the 4-tone signal has a larger instantaneous power variance, in other words it passes a larger amount of time further away from its mean power value, it results in a larger maximum efficiency at P_A = -20 dBm. The advantage in efficiency is lost at higher power levels due to losses in the rectifier circuit, such as the breakdown voltage of the diode.

V. CONCLUSION

The optimization of rectifier circuits under signals with a time-varying envelope is presented. Deterministic multi-tone signals and stochastic randomly modulated signals are considered, and the dependence of the RF-dc conversion efficiency on the rectifier load is investigated. It is shown that for a series diode rectifier the optimum load is slightly reduced as the average input power increases and it is increased as the signal PAPR is increased. A UHF prototype was designed, fabricated and tested showing good agreement with simulation.

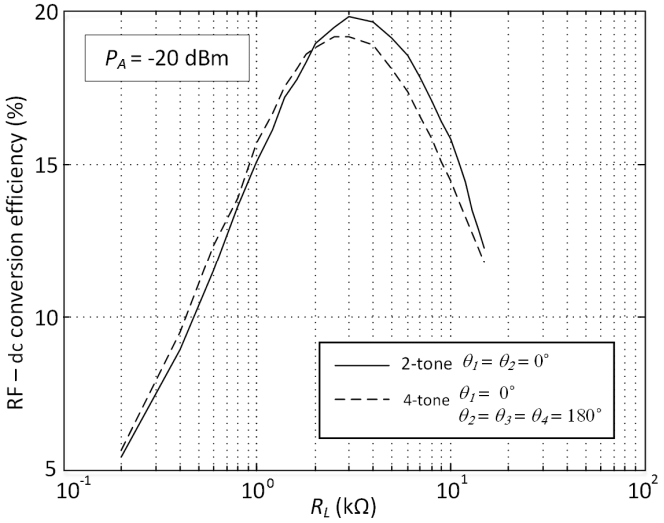


Fig. 14. RF-dc conversion efficiency of a 2-tone signal with in-phase tones and a 4-tone signal with phases θ_1 = 0 °, θ_2 = θ_3 = θ_4 = 180 °.

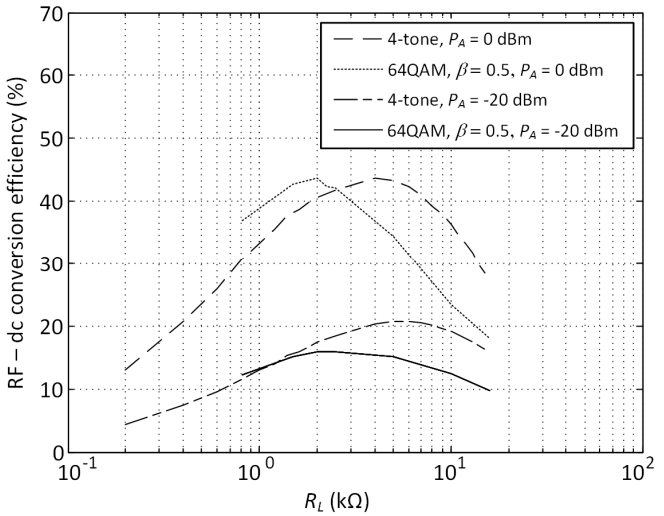


Fig. 15. RF-dc conversion efficiency of a 4-tone signal with in-phase tones and a 64QAM 500KBPS signal with β = 0.5.

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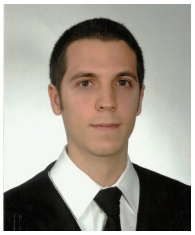

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