

1 Dislocation Loops as a Mechanism for 2 Thermoelectric Power Factor Enhancement in 3 Silicon Nano-Layers

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14 A more than 70% enhancement in the thermoelectric power factor of single-crystal
15 silicon is demonstrated in silicon nano-films, a consequence of the introduction of
16 networks of dislocation loops and extended crystallographic defects. Despite these
17 defects causing reductions in electrical conductivity, carrier concentration and carrier
18 mobility, large corresponding increases in the Seebeck coefficient and reductions in
19 thermal conductivity lead to a significant net enhancement in thermoelectric
20 performance. Crystal damage is deliberately introduced in a sub-surface nano-layer

21 within a silicon substrate, demonstrating the possibility to tune the thermoelectric
22 properties at the nano-scale within such wafers in a repeatable, large-scale and cost-
23 effective way.

24 The recent global drive to be more efficient in the way we use energy, particularly to reduce the
25 amount of energy that goes to waste, has led to renewed interest in thermoelectrics (TE) for
26 waste heat harvesting. In particular demand are materials that use elements that are less costly,
27 less toxic and more Earth-abundant than the popular TE material bismuth telluride (Bi_2Te_3).

28 Despite requiring the scarce element tellurium, Bi_2Te_3 has significantly better thermoelectric
29 performance than more abundant elemental semiconductors, such as silicon (Si). Three material
30 properties determine this performance – thermal conductivity (κ), Seebeck coefficient (S) and
31 electrical conductivity (σ). These interlinked properties are commonly combined to describe
32 performance in terms of the thermoelectric figure-of-merit (Z), where $Z = S^2 \sigma / \kappa$. Bi_2Te_3 has
33 approximately 100-fold better Z than bulk Si [1], but is approximately 30-times more expensive
34 [2]. Therefore developing methods that provide significant gains in the Z of Si offers a potential
35 route to more cost-effective and environmentally friendly thermoelectric devices.

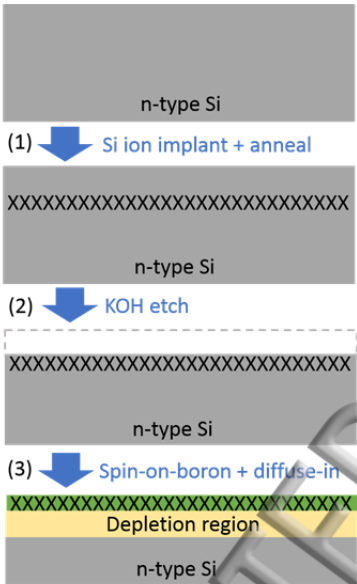
36 Since highly-doped Si (doping $\sim 10^{19} \text{ cm}^{-3}$) possesses S and σ competitive with other TE
37 materials, much recent focus has been on reducing its thermal conductivity, which is too high for
38 most practical applications. It been demonstrated possible via nano-structuring, to vastly reduce
39 κ with little or no degradation of other parameters in structures such as Si nanowires, nanofilms
40 or films containing porosity, periodic voids or vacancies [3-13]. This allows for higher Z and
41 makes nano-structured Si an attractive TE material. Such findings, with variations, have been
42 corroborated by numerous groups worldwide, through both theoretical and experimental studies
43 [3-13].

44 due to this drastic reduction in κ , which is quickly reaching the amorphous limit, further
45 improvements might come from Si's thermoelectric power factor ($PF = S^2 \sigma$), for which to date
46 limited progress has been made. However, a small set of recent studies have demonstrated that a
47 significant improvement in Si's PF is sometimes possible for polycrystalline Si [14-16] where
48 built-in potential barriers are created by nano-scale grain boundaries or voids [17], combined
49 with high levels of doping. These potential barriers increase energy filtering and as a
50 consequence, the Si Seebeck coefficient. Our previous work demonstrated that a Seebeck
51 coefficient improvement is also realizable in single-crystal Si nanowires by the introduction of
52 dislocation loops, which also create potential barriers and produce a similar effect [18]. This was
53 so far only demonstrated in n-type material and for relatively lowly-doped Si, where the PF is far
54 too low for practical applications.

55 In this current article we report that a significant enhancement in the power factor is also possible
56 for p-type bulk material, and more importantly, with high doping concentrations. Improvements
57 in the PF by $\sim 70\%$ compared to control samples (bulk Si) are realized, giving $PF = 6.6 \text{ mW m}^{-1}$
58 K^{-2} at 300 K – significantly higher than that of traditional Bi_2Te_3 materials used in current
59 commercial devices.

60 Four different sample types were fashioned from prime $\langle 100 \rangle$ single-crystal Si wafers (n-type, 5-
61 $10 \text{ } \Omega \text{ cm}$). Ion-implantation of ^{28}Si ions was carried out on a Varian VISta ion implanter at beam
62 energy 2 MeV. Two wafers received a fluence of $2 \times 10^{15} \text{ ions cm}^{-2}$ and two others received
63 $6 \times 10^{15} \text{ ions cm}^{-2}$. Wafers received thermal annealing in nitrogen in a furnace at 900°C for a time
64 of either 20 or 60 mins, before being diced into squares. Along with a non-implanted control
65 wafer, samples were then thinned by etching in 25% KOH solution at 60°C , to precisely remove
66 the top $1.5 \text{ } \mu\text{m}$ of the wafer. Spin-on dopant (boron) was deposited on each sample before heating

67 for 10 mins at 900°C in nitrogen to drive-in the dopant, creating a p-type region with a p/n
 68 junction immediately beneath it, isolating the p-type defect-rich nano-layer from the n-type
 69 substrate. A dip in HF was applied to remove surface boron-silicate glass. The B doping profile
 70 was confirmed as being the same in all samples by differential Hall profiling [19], with a
 71 relatively flat doping peak. This confirmed the junction depth as being ~800 nm, to coincide with
 72 the bottom of the defective layer and that the thickness of pristine Si remaining at the top of the
 73 film was only ~30-45 nm. Fig. 1 provides a schematic illustration of the steps used for sample
 74 fabrication.

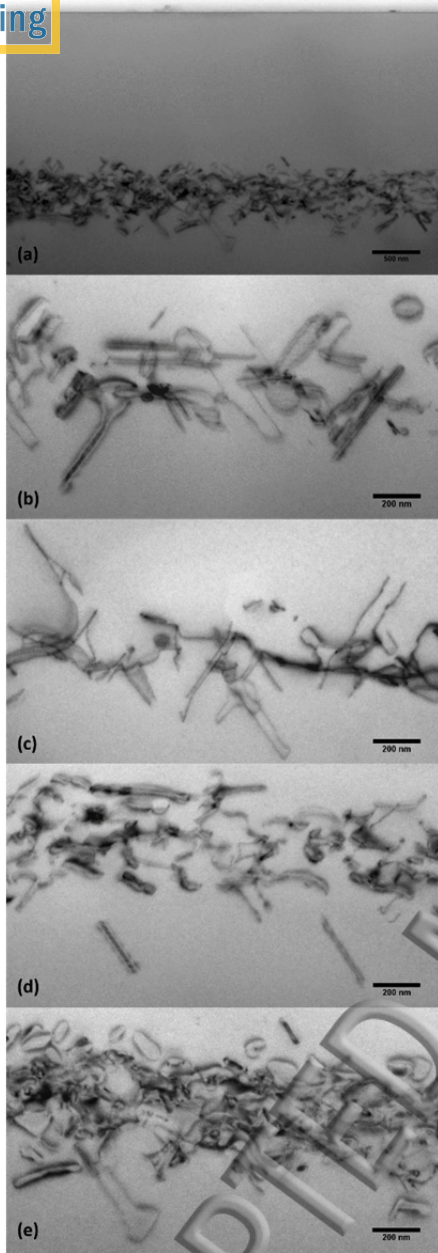


75
 76 **Figure 1.** Schematic diagram showing the sample fabrication steps. The Si wafers underwent Si ion-implantation
 77 and annealing to create a sub-surface nano-layer rich in defects (represented by Xs). Following removal of the wafer
 78 surface by KOH etching, the nano-layer was doped p-type, creating a p/n junction and isolating it from the n-type
 79 substrate.

80 Each sample underwent characterization. The presence and nature of defects in the nano-layers
 81 were characterized by cross-sectional transmission electron microscopy (XTEM). Micrographs of
 82 each of the samples created are presented in Fig. 2. Fig. 2(a) shows the location of the buried

83 er relative to the original wafer surface. The remaining micrographs show shows defects
84 created with each of the four implant/annealing conditions. All micrographs show clear evidence
85 of dislocation loops and implantation extended defects, with the higher implant dose creating a
86 higher density of defects. Samples were sent to a commercial vendor for through-plane thermal
87 conductivity measurements. These were extracted by a thermo-reflectance method. Electrical
88 conductivity, Hall-effect and differential Hall measurements were made in air in van der Pauw
89 geometry, using a Biorad HL5900 tool. Temperature-dependent electrical conductivity and
90 Seebeck measurements were made in-plane on a Linseis LSR-3 instrument in He ambient at 10^4
91 Pa.

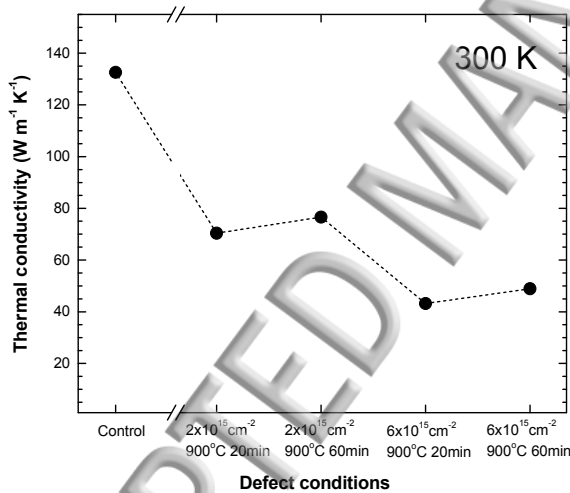
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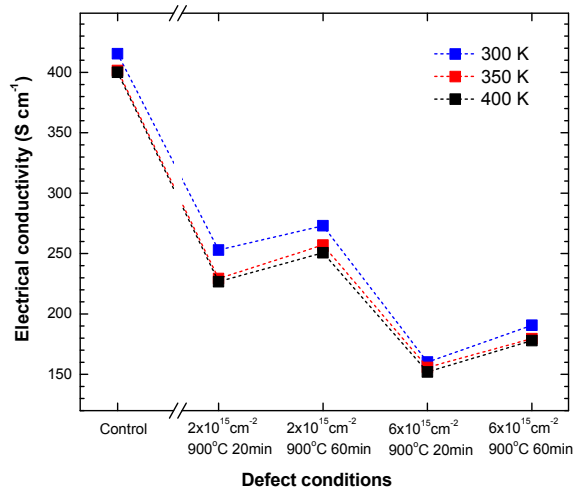
93 **Figure 2.** Micrographs showing sub-surface defect-rich regions created in the Si wafers. (a) Shows the layer
94 location relative to the wafer surface (scale bar is 500 nm). (b) Shows defects created with $2 \times 10^{15} \text{ cm}^{-2}$ implant,
95 900°C , 20 mins annealing. (c) Shows defects created with $2 \times 10^{15} \text{ cm}^{-2}$ implant, 900°C , 60 mins annealing. (d)
96 Shows defects created with $6 \times 10^{15} \text{ cm}^{-2}$ implant, 900°C , 20 mins annealing. (e) Shows defects created with 6×10^{15}
97 cm^{-2} implant, 900°C , 60 mins annealing. (Scale bars in (b)-(e) are 200nm).

Fig 3 shows the variation with implant/annealing conditions for through-plane thermal conductivity at 300 K. κ was $132.6 \text{ W m}^{-1} \text{ K}^{-1}$ for the defect-free control sample and was found to decrease significantly as a result of implantation-induced damage. κ fell to a value of $70.4 \text{ W m}^{-1} \text{ K}^{-1}$ for the lower implantation fluence with 20 min annealing, but recovered slightly to $76.6 \text{ W m}^{-1} \text{ K}^{-1}$ following annealing for 60 min. This was an expected result since it is both intuitive and well-established that the introduction of defects within a ‘perfect’ crystal lattice reduces its thermal transport, and that with longer annealing, more damage will be removed and recovery of thermal transport will occur. For the larger fluence, κ was reduced more, to $43.2 \text{ W m}^{-1} \text{ K}^{-1}$ for 20 min annealing and to $48.9 \text{ W m}^{-1} \text{ K}^{-1}$ with 60 min annealing.



107
108 **Figure 3.** Thermal conductivity (through-plane) as a function of implant/annealing conditions for a control sample
109 relative to samples with 2 MeV Si implant with (i) $2 \times 10^{15} \text{ cm}^{-2}$ fluence, 900°C, 20 mins annealing, (ii) $2 \times 10^{15} \text{ cm}^{-2}$
110 fluence, 900°C, 60 mins annealing, (iii) $6 \times 10^{15} \text{ cm}^{-2}$ fluence, 900°C, 20 mins annealing, and (iv) $6 \times 10^{15} \text{ cm}^{-2}$
111 fluence, 900°C, 60 mins annealing. Measurements were made at 300 K.
112 Fig. 4 shows the change in σ in each sample as a function of the conditions used to create
113 defects. Results are displayed for measurements made at 300, 350 and 400 K, although

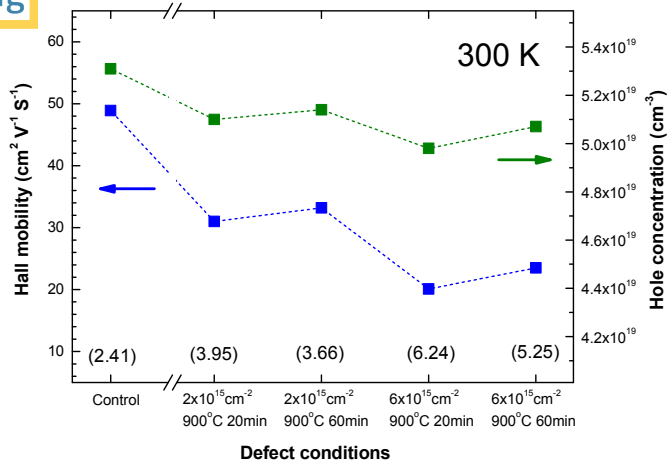
115 differences as a result of temperature were modest in these samples, with only a small
116 conductivity decrease seen in each sample as the measurement temperature is raised. More
117 obvious was the change in conductivity as the implant/annealing conditions were changed.
118 Clearly the control sample had the highest σ of 415 S cm^{-1} . For the lower of the implant fluences,
119 conductivity was reduced relative to the control, and for the higher fluence, conductivity was
120 reduced to less than half. For each fluence, it was the sample that received the shortest anneal
121 that had the lowest conductivity. These trends are intuitive and it is unsurprising that trends in
122 electrical conductivity match those in thermal conductivity (Fig. 3). These trends are similar in
123 magnitude, i.e. as thermal conductivity is reduced for a given condition, so is electrical
124 conductivity by a similar extent, suggesting little net gain in electrical/thermal transport behavior
125 results from the introduction of dislocations, each quantity being reduced by a factor of ~ 3 . It is
126 worth mentioning that XTEM images – particularly Fig. 2(d) and 2(e) – are perhaps deceiving,
127 as one might expect the electrical/thermal conductivity to be lower for the sample in Fig. 2(e)
128 where defects are more apparent. This is opposite to what is measured. In reality, samples having
129 received shorter anneals contain the most defects and lower electrical/thermal conductivity, yet
130 these defects are in the form of smaller Si-interstitial clusters, not visible in the XTEM at its
131 current resolution.



131

132 **Figure 4.** Electrical conductivity (in-plane) as a function of ion-implantation condition and annealing time, for three
 133 measurement temperatures (300 K - 400 K).

134 Fig. 5 gives further detail of the room-temperature σ by way of Hall measurement data. Carrier
 135 concentration and Hall mobility at 300 K are presented. They show that defect-mediated
 136 decreases in σ are a result of a fall in both Hall mobility and carrier concentration, though the
 137 former drop is more significant. Crystallographic defects are well known to degrade carrier
 138 mobility in Si and this clearly occurs in current samples. B dopant activation is highest in the
 139 control sample following drive-in, whereas defects reduce the carrier concentration by up to
 140 10%. Since B is well-known to cluster with self-interstitials it is likely that their presence during
 141 the drive-in phase means a proportion of the dopants are trapped in inactive clusters rather than
 142 finding substitutional sites. B activation improves slightly after longer-duration annealing.

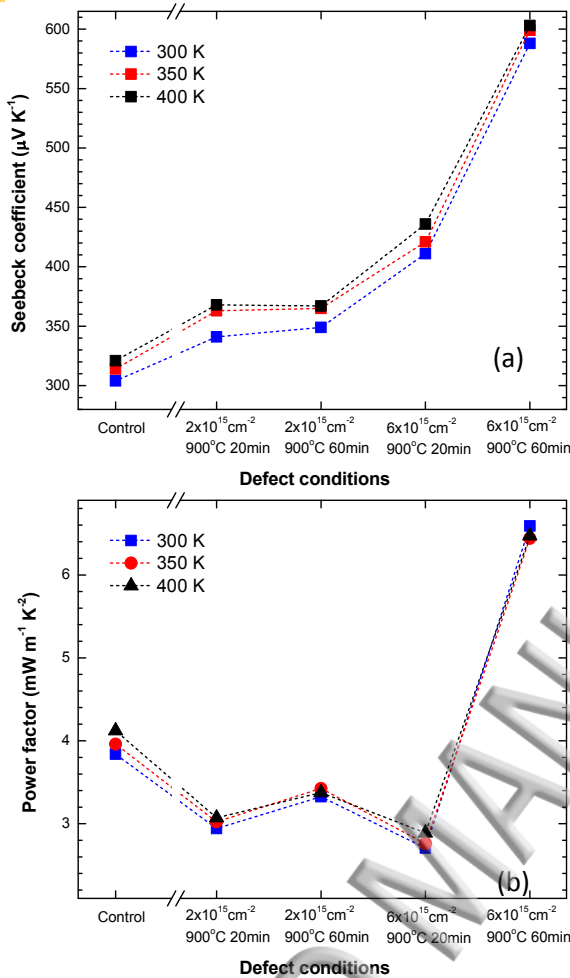


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144 **Figure 5.** Hall mobility (left axis) and hole concentration (right) as a function of defect conditions. Measurements
 145 were made at 300 K. Values in parentheses are corresponding resistivity values in mΩ cm.

146 In-plane Seebeck coefficient measurements were carried out for each of the samples. Results are
 147 displayed for measurements made at 300, 350 and 400 K, although as for σ , temperature-
 148 dependent differences are modest, with only a small S increase seen in each sample as the
 149 measurement temperature is raised. In this case S was lowest in the control sample (Fig. 6(a)),
 150 though this was expected since that sample had the highest electrical conductivity and the two
 151 parameters are interrelated, with one usually increasing at the expense of the other. Combining
 152 the two in the form of the power factor gives an indication of the net thermoelectric performance,
 153 with $PF = 3.8 \text{ mW m}^{-1} \text{ K}^{-2}$ at 300 K for the control sample (Fig. 6(b)). This PF value is in line
 154 with the highest value pristine Si can provide under optimal doping conditions. All other
 155 samples, with lower electrical conductivity, have a higher Seebeck coefficient. The two samples
 156 receiving the lower implant dose ($2 \times 10^{15} \text{ cm}^{-2}$) have modestly higher S that, when combined with
 157 σ , result in a significantly lower thermoelectric PF than the control sample. For the higher
 158 implant fluence ($6 \times 10^{15} \text{ cm}^{-2}$) with 20 min annealing the PF is worse still, since the relatively

159 a small rise in S is more than negated by the much larger drop in σ . An interesting result occurs
160 however, when the higher fluence sample is annealed for longer, resulting in the formation of a
161 dense network of mostly dislocation-loops with diameters roughly between 100 nm and 200 nm
162 (Fig. 2(e)). In this case the increase in S is much greater than for all other samples and bucks the
163 trend, since given its higher electrical conductivity than the previously mentioned sample, one
164 would expect its Seebeck coefficient to decrease. In fact, as the reader can see, not only is the
165 opposite true, but the increase in S is significant. This has a striking effect on the power factor,
166 which is now on average 70% higher than that of the control sample, with $PF = 6.6 \text{ mW m}^{-1} \text{ K}^{-2}$
167 at 300 K.



168

169

170 **Figure 6.** (a) Seebeck coefficient (in-plane) and (b) power factor as a function of defect conditions for three
 171 measurement temperatures (300 K - 400 K).

172 The simultaneous increase in σ and S is rare, but significant, and results in improved power
 173 factors. It is similar to that observed in reference [14] for heavily B-doped nano-crystalline Si,
 174 again under high-temperature annealing. While the underlying reasons behind this are still under
 175 investigation, it is possible that a number of contributing factors coexist and act synergistically in
 176 order to achieve a simultaneous S and σ improvement. For the former, it is probable that
 177 potential barriers for holes are created at the dislocation sites, which improve energy filtering and
 178 consequently S . Indeed, when present within the crystal lattice, dislocation loops are known to

180 gap local to the dislocation site [20]. For the first annealing condition, this local band-gap
181 increase could be responsible for the reduction in conductivity and mobility. As well as allowing
182 loops to form, longer annealing would heal the majority of the Si volume, and thus a slight
183 increase in the electrical conductivity is observed, compensating for any further reduction from
184 the increasing potential barriers. The increased pressure may also improve carrier mobility, a
185 well-known consequence of applying stress in Si [21]. In addition, any local thermal
186 conductivity differences between pristine Si regions and the dislocations might improve S as
187 well. This is because the overall Seebeck coefficient is determined by the weighted average of S
188 in the two regions, with the weighting factor being the temperature drop in each region,
189 determined by their thermal conductivities [14, 22]. Thus, as the crystal lattice is healed,
190 especially in the last annealing step, and local thermal conductivity increases, the local Seebeck
191 coefficient in the dislocation regions (which is expected to be high compared to bulk Si)
192 becomes more important and could warrant the large increase in the overall S observed in Fig.
193 6(a). Our earlier calculations on the effect of filtering by barriers in p-type Si, indicate that
194 filtering alone could provide ~30-40% PF improvements [22, 23], whereas the rest of the
195 measured improvements could originate from the various other factors identified, such as local
196 variations in thermal conductivity and carrier mobility.

197 We have reported a significant enhancement in the power factor of single-crystal Si is
198 possible for highly-doped p-type material, specifically an improvement of ~70 % compared
199 to control samples (bulk Si), giving $PF = 6.6 \text{ mW m}^{-1} \text{ K}^{-2}$ at 300 K. This is higher than that
200 of traditional Bi_2Te_3 materials used in commercial thermoelectric devices [24] and is a
201 consequence of the introduction of a dense network of dislocation loops with diameter

201 between 100 nm and 200 nm. Despite these defects causing reductions in electrical
203 conductivity, carrier concentration and carrier mobility, large corresponding increases in
204 Seebeck coefficient and reductions in thermal conductivity lead to a significant net
205 enhancement in thermoelectric performance. This finding provides a route to significant
206 gains in the thermoelectric power factor of Si, a material that potentially offers a path to
207 more cost-effective and environmentally-friendly thermoelectric devices.

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n-type Si

(1)  Si ion implant + anneal

XX

n-type Si

(2)  KOH etch

XX

n-type Si

(3)  Spin-on-boron + diffuse-in

XX

Depletion region

n-type Si

