A Compact 12-Way Slotted Waveguide Power Combiner for Ka-band Applications

José Antonio García-Pérez, *Student Member, IEEE* Savvas Kosmopoulos, *Life Member, IEEE* and George Goussetis, *Senior Member, IEEE*

***Abstract*—A power divider/combiner based on a double sided slotted waveguide geometry suitable for Ka-band applications is proposed. This structure allows up to 50% reduction of the total device length compared to previous designs of this type without compromising manufacturing complexity or combining efficiency. Efficient design guidelines based on an equivalent circuit technique are provided and the performance is demonstrated by means of a 12-way divider/combiner prototype operating in the range 29-31 GHz. Numerical simulations show that back to back insertion loss of 1.19 dB can be achieved, corresponding to a combining efficiency of 87%. The design is validated by means of manufacturing and testing an experimental prototype with measured back-to-back insertion loss of 1.83 dB with a 3 dB bandwidth of 20.8%, corresponding to a combining efficiency of 81%.**

***Index Terms*—Ka-band, double-side slotted waveguide, power combining, mm-wave power amplifier.**

I. Introduction

POWER combining techniques have been widely used in power amplifiers to overcome the power limitation associated with a single MMIC chip. They can be exploited to address limited availability and increased costs of higher power output MMICs, associated thermal management as well as to enhance graceful degradation [1], [2]. Recently, Ka-band is attracting interest for 5G as well as for satellite broadband applications [3], [4]. One limitation at Ka-band and higher mm-wave frequencies is that waveguides are reduced to sizes comparable (or smaller than) commercially available packaged chips. This poses challenges in terms of available space when scaling concepts used at lower frequencies e.g. [5].

Among the different possible techniques, the travelling wave power combining solution addresses these problems by cascading a series of reflectionless unit cells accommodating the chips [6]. By virtue of providing a bulk metal base in direct contact with the chips, this approach brings benefits in terms of thermal management. Moreover, phase imbalance is mitigated by connecting the divider and combiner in reverse order. Focusing to address applications that include Ka-band satellite or 5G communications, where volume, mass and cost are a priority, this paper proposes a new and compact travelling wave power divider/combiner based on a waveguide structure with slots on either side of the waveguide. The inclusion of slots on both the top and the bottom waveguide walls provides a total length reduction of up to 50% compared to previous research using similar methodology [7] without compromising manufacturing complexity or combining efficiency. In the following, design guidelines for the proposed technology are provided. Furthermore, simulated and measured results of a manufactured prototype are presented for validation.

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The authors are with the Microwave and Antenna Engineering Research Group, School of Engineering and Physical Sciences, Heriot-Watt University, Edinburgh, EH14 4AS, U.K. (email contact jag34@hw.ac.uk, g.goussetis@ieee.org).

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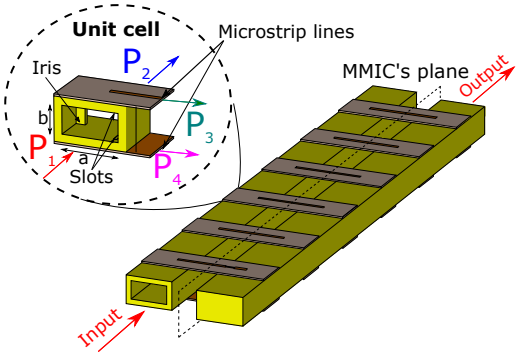

Fig. 1. Back-to-back power divider and combiner. The unit cell is depicted in detail.

II. Design

The design of the proposed power divider/combiner can be divided into the separate design of N reflectionless unit cells [8], each one with a specific coupling ratio, so that equal power division along all the output ports is achieved. The proposed structure is schematically depicted in Fig. 1, where a whole back-to-back structure as well as the detailed unit cell model are represented. The unit cell consists of a waveguide with two slots (at the top and bottom broad side walls) that couple power to two output microstrip lines. Inductive irises are used as matching elements. We note that other reactive discontinuities can also be employed for matching (e.g. capacitive iris), which can be advantageous depending on the manufacturing process.

The top view of a cell and its equivalent circuit are shown in Fig. 2. In the remaining, all admittances are normalized to the WR-28 waveguide ($a = 7.112$ mm and $b = 3.556$ mm) characteristic admittance ($y_0 = 0.001889$ S). The input admittance of the unit cell is y^i_{in}, which for a reflectionless design should be equal to 1. The coupling ratio for each cell is related to the conductance (g^i_{slot}) seen at the slot plane. Adopting the methodology described in [6] it is straightforward to show that the required conductance for each cell is given by

TABLE I
FINAL PARAMETERS VALUES FOR THE PROPOSED STRUCTURE (DIMENSIONS IN MM).

Cell	Slot_L	Slot_W	Slot_O	Short_L	Short_W	Trans_L	Trans_W	Extra_L	Extra_W	Iris_D	Iris_L	Iris_W
1	5.297	0.51	2.881	1.555	0.618	1.491	0.648	3	0.63	0.483	1.148	0.567
2	5.777	0.51	2.795	1.366	0.701	1.317	0.595	3	0.63	0.608	1.134	0.643
3	5.769	0.51	2.860	1.410	0.554	1.630	0.567	3	0.63	0.809	1.009	1.484
4	5.901	0.51	2.795	1.792	0.585	1.481	0.569	3	0.63	1.027	1.361	1.027
5	6.087	0.51	2.926	1.860	0.679	1.671	0.501	3	0.63	1.380	1.7	1.158
6	6.258	0.51	2.945	2.298	0.810	1.776	0.351	3	0.63	0.788	1.5	1.033

$$g^i_{slot} = \frac{1}{N - i + 1} \tag{1}$$

where i is the order of the cell (starting from the input) and N is the total number of cells. The slot is non-resonant and initially its length ($Slot\_L_i$) is set between $\lambda_0/2$ and $\lambda_g/2$ (where λ_0 and λ_g are the free space and waveguide guide wavelength respectively). The initial values for the open-ended ($Short\_L_i$) and the matching ($Trans\_L_i$) sections of the microstrip lines are set at $\lambda_{gm}/4$ (where λ_{gm} is the microstrip guide wavelength) in order to provide a virtual short circuit at the slot and an impedance matching to the microstrip ports (P_3 and P_4) respectively. The sections marked as $Extra\_L_i$ are 50 Ω microstrip lines of arbitrary length.

Based on these values, the design procedure is as follows. First, the iris is removed and the admittance at the slot plane $y^i_{slot} = g^i_{slot} + jb^i_{slot}$ is calculated using full-wave simulations. Any phase due to the length between P_1 and the slot plane is de-embedded. Effects due to the matched waveguide at P_2 can then be removed by simply substracting its unitary admittance ($y^i_{slot} = y^i_{sim_{deemb}} - 1$). A parametric sweep of the cells geometrical dimensions is carried out using this methodology to identify a geometry that satisfies (1). Once the dimensions of the slot and microstrip line have been determined, the iris is simulated and its dimensions and position are specified such that the unit cell becomes reflectionless ($y^i_{in} = 1$). This condition requires that

$$g^i_{slot} + g^i_k = 1 \quad \text{and} \quad b^i_{slot} = -b^i_k \tag{2}$$

where $y^i_k = g^i_k + jb^i_k$ is y^i_L translated over a length l^i_k and y^i_L is the combined admittance of the iris (y^i_{iris}) and the output port P_2 (which is equal to 1). The iris dimensions are thus designed to make the admittance seen towards the iris (y^i_L) intersect the constant VSWR circle in the Smith chart associated to y^i_k. Once the desired iris admittance is achieved, the length l^i_k is calculated using transmission line theory

$$l^i_k = \frac{\lambda_g}{2\pi} \arctan\left(j \frac{y^i_L - y^i_k}{y^i_L y^i_k - 1} \right) \tag{3}$$

Once dimensions for all the cells have been obtained, additional waveguide lengths between unit cells can be included to provide space for placing the amplifier chips. Since the unit cells are reflectionless, these lengths can be of arbitrary length with no effect in the total behaviour, provided that higher order waveguide modes of the slots and the iris can not interact between cells. In order to achieve the high coupling ratio required at the last stage, a short circuit is used at $0.75\lambda_g$ from the last slot plane. By virtue of the equivalent circuit, this procedure splits the global optimisation of each unit cell into two smaller and more efficient design steps. Ultimately the initial values obtained by this process yield good response and some limited optimization of the entire combiner may be required.

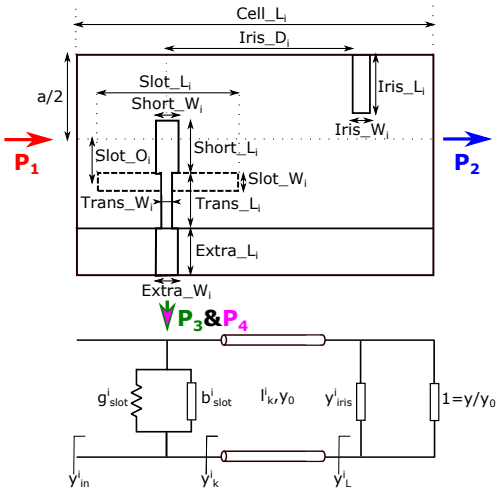

Fig. 2. Geometric parameters and equivalent circuit for each unit cell.

III. PROTOTYPE AND EXPERIMENTAL RESULTS

For validating the procedure, a 12-way power divider/combiner is designed for operation centred at 30 GHz. Following the procedure described above, the final optimized parameters for the prototype can be found in Table I. For this prototype, the unit cells are 7.02 mm length ($Cell\_L_i$). Waveguides of length 11.25 mm separate successive unit cells. The short-circuited waveguide following the last cell is 8.5 mm long. Fig. 3(a) shows the simulated S-parameters for the multi-port divider/combiner. As shown the return loss is (RL) better than 25 dB in the band 29-31 GHz and the power division ratio is close to the theoretical -10.79 dB over this range. The minimum simulated insertion loss (IL) within the design band is 1.19 dB (Fig. 5). Considering that the loss of the combining circuit is only half of that, this corresponds to power combining efficiency of $\eta_c = 87\%$. The simulated 3-dB IL bandwidth is 6.5 GHz, resulting in a relative 21.7% from 26.5 GHz (Ka-band cut-off frequency) up to 33 GHz. As discussed above, the unequal phase delay (Fig. 3(b)) at

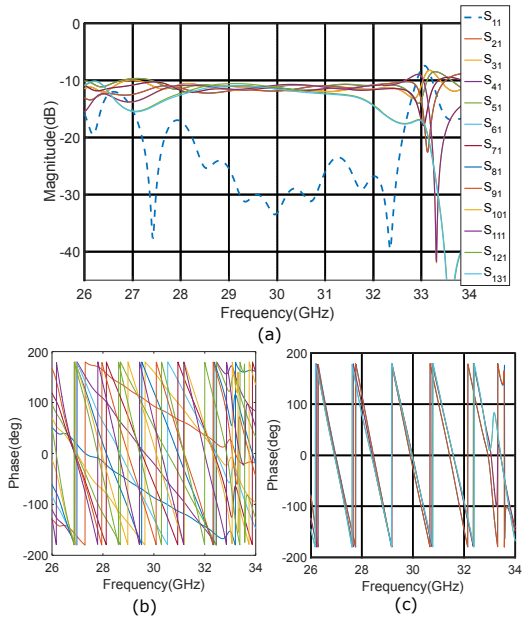

Fig. 3. (a) Simulated S-parameters for the designed power divider/combiner. (b) Phase delay at each microstrip output port. (c) Phase compensation when measuring phase through each microstrip path.

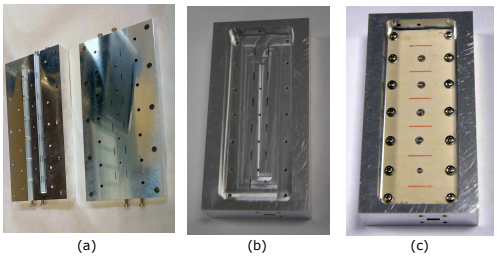

Fig. 4. Fabricated prototype with and witouth attached PCB's.

the microstrip output ports can be easily compensated by connecting the divider and combiner in a reverse order. This is shown in Fig. 3(c) where the phases for the back-to-back structure through each microstrip line are shown.

In order to experimentally validate this design, the complete back-to-back structure was fabricated using Computer Numeric Control (CNC) machining for grooving the whole waveguide cavity in an aluminium block. The top wall containing only slots was fixed with screws on the top of the structure (Fig. 4(a)). In this way the alignment requirement is reduced compared to cutting the waveguide at half height [9]. The microstrip circuit boards have been fabricated etching a 0.254 mm Rogers 6002 RT/Duroid substrate ($\epsilon_r = 2.94$). The alignment and attachment of the PCBs has been based on the use of screws. Fig. 4(b) and Fig. 4(c) shows a picture of the prototype with and without the PCBs attached.

The measured S-parameters are shown in Fig. 5. The measured RL is better than 21 dB within the design band and the minimum IL is 1.83 dB at 30.4 GHz. This corresponds to a peak measured combining efficiency of $\eta_{c_{max}} = 81\%$. The measured 3-dB IL bandwidth is 6.25 GHz (from 26.5 GHz up to 32.75 GHz), corresponding to a fractional value of

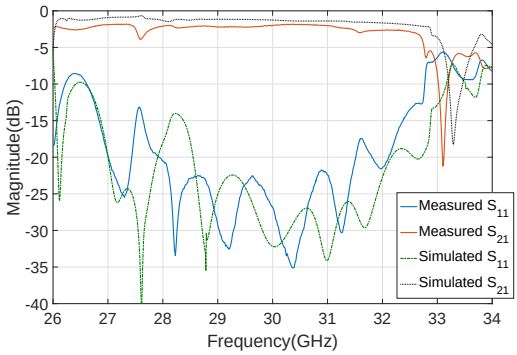

Fig. 5. Simulated and measured S-parameters for the fabricated back-to-back prototype.

20.8 %. It is noted that earlier work in [7] reports an 8-way combiner with measured insertion loss of 1.8 dB and fractional bandwidth of 15%. The small differences between simulated and measured results are attributed to tolerances in fabrication, mainly due to the handmade PCBs alignment and attachment.

IV. Conclusion

A new power divider/combiner structure has been demonstrated. This new architecture includes slots at the top and bottom broadside walls of the waveguide therefore allowing a reduction in the total length up to 50% compared to previous designs without compromising the electrical performance. The concept was validated by means of a fabricated 12-way prototype with measured combining efficiency of up to 81% and a 3-dB IL bandwidth of 20.8%. The relaxed tolerance fabrication allows to reduce manufacturing complexity and time, resulting in a more accurate response compared to the simulated results.

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