Tampere University

Samuli Piispanen

SIMPLIS EFFICIENCY MODEL FOR A SYNCHRONOUS MULTIPHASE BUCK CONVERTER

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ABSTRACT

Samuli Piispanen: SIMPLIS efficiency model for a synchronous multiphase buck converter
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In this master's thesis, an efficiency model was developed for the synchronous multiphase buck converters of the TPS6594x-Q1 integrated circuit using SIMPLIS simulator. The model includes internal losses occurring in power stage transistors, power stage drivers and bondwires. Modeled external losses include printed circuit board resistance and inductance, inductor direct and alternating current characteristics as well as capacitor nonidealities.

Internal loss modeling was mostly based on Cadence simulations. Power stage transistors especially were thoroughly modeled. The capacitances of the power stage transistors were extracted by integrating gate and drain currents during the transistor on and off transitions. Charging of the parasitic capacitances followed the theory in turn-off and turn-on transitions and therefore the capacitance extraction was fairly simple. Nonlinearities of the parasitic capacitors were modeled in SIMPLIS with multiple linear approximations. Transistor gate drivers were very rough approximations of the real drivers but good enough for the simulation model. Drivers were modeled to match the gate currents simulated in Cadence, which were then combined the accurate switching transistor models in order to accurately model the switching characteristics.

External loss models were based on measurements and simulations. Printed circuit board losses were based on Ansys simulations in which the printed circuit board inductances and resistances were solved from the geometry of the printed circuit board. Inductors were modeled to match the datasheet impedance and resistance graphs and the model was verified against the measurements done in the laboratory. An automated measurement testbench was done for the inductor measurements using LabVIEW and the results were parsed using Matlab. A ladder topology with resistances and inductances was used in the final inductor model to model the frequency characteristics of the inductor. The effect of direct current on inductance was also investigated but the inductance reduction did not have any significant impact on efficiency. Other external components such as capacitors also cause some external losses and they were modeled based on the capacitor datasheets.

The simulation model was compared against single- and two-phase efficiency measurements with multiple different input and output voltages which were chosen to match the most common use cases. Efficiency curves were drawn for each configuration using the implemented simulation model and over 300 different comparison points were compared in total. A post processing script that was launched after a simulation completes had to be written with the programming language SIMPLIS supports to draw the efficiency graph from the simulated data. Using the script allowed to run the efficiency simulation without any additional licenses other than the SIMPLIS license. The final model achieved an average error of under 1 % between all the measured and simulated efficiency curves. The most accurate results were obtained with lower switching frequency and larger inductance.

Apart from accuracy, the simulator had to be practical and therefore the simulation time had to be considered. Simulation time was attempted to be kept at minimum by simplifying the schematic in as many ways as possible without losing accuracy. For example, reducing the point of the linear approximations in the power stage transistors from 79 points to 17 points saved nearly 50 seconds in single-phase simulations without significant changes in simulation accuracy.

Keywords: Buck converter, DCDC, power losses, efficiency, modeling, SIMPLIS

TIIVISTELMÄ

Samuli Piispanen: SIMPLIS hyötysuhdemalli synkroniselle monivaiheiselle buck-hakkurille
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Tässä diplomityössä toteutettiin hyötysuhdemalli TPS6594x-Q1 integroidun piirin monivaiheisille buck-hakkureille käyttäen SIMPLIS-simulaattoria. Mallissa otetaan huomioon lähtöasteen transistoreissa, transistoreiden ajureissa ja liitoslangoissa tapahtuvat piirin sisäiset häviöt. Mallinnettuja ulkoisia häviöitä on piirilevystä aiheutuva resistanssi ja induktanssi, kelan tasa- ja vaihtovirtakäyttäytyminen sekä kondensaattoreiden epäideaalisuudet.

Piirin sisäisten häviöiden mallinnus perustui pääosin Cadence-simulointeihin ja eritoten lähtöasteen transistoreiden ja niiden ajureiden mallintamiseen käytettiin erityisen paljon aikaa. Lähtöasteen transistoreiden kapasitanssit määritettiin integroimalla transistoreiden hila- ja nieluvirtoja transistoreiden kytkeytyessä päälle ja pois. Kapasitanssien varautuminen vastasi teoriassa esitettyä kanavatransistorin kytkeytymistapahtumaa, jolloin kapasitanssien määrittäminen oli suhteellisen yksinkertaista. Kapasitanssien epälineaarisuudet mallinnettiin SIMPLIS-simulaattorissa käyttäen lineaarisia approksimaatioita. Transistoreiden hila-ajurien toteutukset olivat varsin pelkistettyjä, mutta riittävän tarkkoja hyvän tarkkuuden saavuttamiseen. Ajurit mitoitettiin vastaamaan Cadence-simulointien hilavirtoja, jotta lähtöasteen käyttäytyminen vastaisi Cadence-simulaattorissa havaittuja kytkeytymistapahtumia.

Ulkoisia häviölähteitä mallinnettiin mittausten sekä simulointien avulla. Työn piirilevyhäviöt perustuivat Ansys-simulointeihin, joissa piirilevyresistanssit ja -induktanssit ratkaistiin piirilevyn geometriasta. Kelat mallinnettiin datalehden impedanssi- ja resistanssikuvaajien perusteella ja tuloksia vertailtiin laboratoriossa tehtyihin mittauksiin. Kelamittauksia varten luotiin oma automatisoitu mittausohjelma käyttäen LabVIEW-ohjelmistoa ja mittaustuloksia käsiteltiin Matlab-ohjelmistolla. Lopullisessa kelamallissa käytettiin induktanssien ja resistanssien muodostamaa rakennetta, jonka avulla saadaan kelan taajuusriippuvat häviöt mallinnettua. Kelan tasavirrasta aiheutuvien muutoksien kuten induktanssin alenemisen vaikutusta hyötysuhteen tarkasteltiin, mutta tällä ei havaittu olevan suurta vaikutusta hyötysuhteeseen. Muita ulkoisia häviöitä aiheuttavia komponentteja olivat kondensaattorit, jotka mallinnettiin yksinkertaisesti kondensaattoreiden datalehtien perusteella.

Simulointimallia vertailtiin yksi- ja kaksivaiheisiin hyötysuhde mittaustuloksiin usealla eri lähtö- ja tulojännitteellä, jotka valittiin tyypillisimpien käyttökohteiden mukaan. Simulaattorilla piirrettiin jokaiselle testatulle konfiguraatiolle mittaustuloksia vastaavat hyötysuhdekuvaajat ja kaiken kaikkiaan vertailupisteitä kertyi yli 300 kappaletta. Kuvaajan piirtämistä varten tarvitsi ohjelmoida erillinen simulaattorin sisäinen aliohjelma, joka suoritetaan aina simuloinnin päätyttyä. Tämän jälkikäsittelyohjelman ansiosta hyötysuhdekuvaajan piirtäminen ei vaadi erillisiä lisälisenssejä SIMPLIS-lisenssin lisäksi. Lopullisella hyötysuhdemallilla saavutettiin alle 1 %:n keskimääräinen virhe kaikkien mitattujen ja simuloitujen hyötysuhdekuvaajien välillä. Tarkimmat tulokset simulointimalli antoi alhaisemmalla kytkentätaajuudella ja suuremmalla induktanssilla.

Tarkkuuden lisäksi toinen näkökulma mallille oli simulointiaika, jotta mallia olisi mielekästä ja järkevää käyttää. Simulointiaika pyrittiin pitämään mahdollisimman pienenä tekemällä yksinkertaistuksia monin eri tavoin edellyttäen, että yksinkertaistuksilla ei ollut vaikutusta simulointitarkkuuteen. Esimerkiksi pudottamalla lähtöasteen transistoreiden lineaaristen approksimaatiopisteiden määrä 79 pisteestä 17 pisteeseen simulointiaika pieneni yksivaiheisissa simuloinneissa lähes 50 sekuntia ilman merkittävää vaikutusta simulointitarkkuuteen.

Avainsanat: Buck-hakkuri, DCDC, tehohäviöt, hyötysuhde, mallinnus, SIMPLIS

PREFACE

This master's thesis was done for Texas Instruments in Oulu and the thesis examiners were Professor Karri Palovuori and University Lecturer Erja Sipilä. I want to thank them for giving feedback on the writing process and answering my questions about the practical arrangements of the degree. Supervisors for the thesis were applications engineering manager Tomi Koskela and design architect Ari Väänänen. I want to thank my supervisors Tomi Koskela and Ari Väänänen for guidance, answering my questions, reviewing my thesis multiple times and giving thorough feedback along the way.

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Samuli Piispanen

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LIST OF FIGURES AND TABLES

LIST OF SYMBOLS AND ABBREVIATIONS

AC	Alternating (current)
ADC	Analog to digital converter
BD	Body diode
BJT	Bipolar junction transistor
CMC	Current mode control
CPU	Central processing unit, processor
CSV	Comma-separated values
DC	Direct (current)
DCDC	Direct voltage to direct voltage (converter)
DCM	Discontinuous conduction mode
DCR	Direct current resistance
DVM	Design verification module
ESL	Equivalent series inductance
ESR	Equivalent series resistance
EVM	Evaluation module
FET	Field-effect transistor
GPIB	General purpose interface bus
HS	High side (transistor)
IC	Integrated circuit
IPWL	Current controlled piecewise linear (resistor)
IQ	Quiescent current
I-V	Current as a function of voltage
LC	Inductor-capacitor (filter)
LDO	Low-dropout regulator
LHPZ	Left-half plane zero
L-R	Inductance and resistance
LS	Low side (transistor)
MOSFET	Metal-oxide-semiconductor field-effect transistor
NMOS	N-type metal-oxide-semiconductor field-effect transistor
PCB	Printed circuit board
PCMC	Peak current mode control
PFM	Pulse-frequency modulation
PMIC	Power-management integrated circuit
PMOS	P-type metal-oxide-semiconductor field-effect transistor
POP	Periodic operating point
PWL	Piecewise linear
PWM	Pulse-width modulation
Q-V	Charge as a function of voltage
RLCG	Resistance, inductance, capacitance and conductance
RMS	Root mean square
SIMPLIS	Simulation of piecewise linear systems
SPICE	Simulation program with integrated circuit emphasis
USB	Universal serial bus
VCCS	Voltage-controlled current source
VMC	Voltage mode control
VPWL	Voltage controller piecewise linear (resistor)
ZVS	Zero voltage switching

ΔB	Peak AC flux density
ΔI_O	Output current ripple
ΔI_{oP}	Peak current in load current
ΔI_{oV}	Valley current value in load current

ΔL_R	Channel length reduction
ΔV	Voltage change in switching transition
ΔZ	Channel width reduction
μ_n	Electron mobility
a	Material specific parameter
a_1	Material specific parameter
a_2	Material specific parameter
A_c	Area of the core
a_s	Material specific parameter
B	Flux density
B_m	Amplitude of magnetic flux
C	Capacitance
C	Capacitance
C_{DG}	Drain-gate capacitance
C_{DS}	Drain-source capacitance
C_{GS}	Gate-source capacitance
C_i	Gate capacitance caused by the insulator
C_{OSS}	Output capacitance
D	Duty ratio
d	Gate insulator thickness
f	Frequency
f_0	Material specific parameter
f_1	Material specific parameter
f_2	Material specific parameter
f_{sw}	Switching frequency
H	Magnetic field
h	Height difference between trace and ground
$I_{AC,RMS}$	AC rms current
$I_{C,RMS}$	Capacitor current in rms
I_d	Drain current
I_{DC}	DC current
i_{EA}	Comparison current in current mode control
$i_{EA(comp)}$	Compensated comparison in current mode control
I_o	Output current
I_{OUT}	Output current
I_{peak}	Inductor peak current
I_Q	Quiescent current
I_{rr}	Reverse recovery current
I_{valley}	Inductor valley current
k	Transistor thermal coefficient, Material specific parameter
k_{12}	Coupling factor between inductors 1 and 2
K_{fe}	Material specific parameter
L	Inductance, physical gate length
L_1	Inductor 1 in mutual inductance calculation
L_2	Inductor 2 in mutual inductance calculation
l_m	Length of the core
L_s	Common source inductance
M_{12}	Mutual inductance between inductors 1 and 2
P_{BD}	Body diode power loss
P_{cap}	Capacitor power losses
P_{cond_hs}	High side transistor conduction loss
P_{cond_ls}	Low side transistor conduction loss
P_{diss}	Dissipated power
P_{driver}	Driver power losses
P_{fe}	Total core loss

P_{FET_cond}	FET conduction losses
P_g	Gate driver loss
P_H	Hysteresis loss
P_{in}	Input power
P_L	Inductor loss
P_{logic}	Logic and control power losses
P_{losses}	Power losses
P_{out}	Output power
P_{pcb}	Printed circuit board power losses
P_{rr}	Reverse recovery loss
P_{sw}	Switching power losses
P_v	Inductor core loss
P_{v0}	Material specific parameter
Q_{CDS}	Charge of drain-source capacitor
Q_{CDS0}	First charge point in drain-source capacitance model
Q_{CDS1}	Second charge point in drain-source capacitance model
Q_{gd}	Gate-drain charge
Q_{godr}	Gate overdrive charge
Q_{GS}	Gate-source charge
Q_{gs1}	Gate-source charge before threshold voltage
Q_{gs2}	Gate-source charge between threshold voltage and Miller plateau
Q_{rr}	Reverse recovery charge
R	Resistance
R_{AC}	Inductor AC resistance, trace AC resistance
R_{cap}	Capacitor resistance
R_{coil}	Inductor resistance
R_{DC}	Inductor DC resistance, trace DC resistance
R_{DCR}	Inductor DC resistance
R_{DS}	Drain-source on-resistance
R_{DS_25C}	MOSFET channel resistance at 25 °C
R_{DSHS}	High side transistor channel on-resistance
R_{DSLS}	Low side transistor channel on-resistance
R_{ESR}	Capacitor equivalent series resistance
R_G	Gate resistance
R_{GS}	Gate-source resistance
R_i	Gain of the current sense amplifier
R_{LD}	Load resistance
R_{PCB}	Printed circuit board resistance
R_{sw}	Switch resistance
S_f	Down slope of the inductor current
t	Trace thickness
$T(j\omega)$	Transfer function
t_{d1}	Rising edge deadtime
t_{d2}	Falling edge deadtime
t_{fall}	Transistor fall time
T_j	Junction temperature
T_m	Temperature at which minimum core losses occur
T_{off}	High side off-time
T_{on}	High side on-time
T_R	Core temperature
t_{rise}	Transistor rise time
T_{rr}	Reverse recovery time
U_R	Reverse voltage
W	Channel width
w	Trace width

V_{CDS}	Voltage over drain-source capacitance
V_{CDS0}	Second voltage point in drain-source capacitance model
V_{CDS1}	First voltage point in drain-source capacitance model
V_{DD}	Supply voltage
V_{DF}	Body diode forward voltage drop
v_{EA}	Error amplifier output voltage
V_G	Gate voltage
V_{GS}	Gate-source voltage
V_I	Input voltage
V_{IN}	Input voltage
V_o	Output voltage
V_p	Ramp generator peak voltage in voltage mode control
v_{RAMP}	Ramp generator voltage
V_{REF}	Internal reference voltage
v_s	Switch node voltage
V_T	Threshold voltage
Z	Channel width
Z_A	Impedance of the error amplifier
α	Material specific parameter
α_p	Ferromagnetic material's temperature coefficient for losses
α_T	Material constant
β	Material specific parameter
δ	Skin depth
δ_{copper}	Skin depth of copper
Δi_L	Inductor current ripple
Δv_o	Output voltage ripple
$\Delta v_{o,RMS}$	Root mean square value of the output voltage ripple
ε_i	Relative permittivity of the gate insulator
η	Efficiency
ρ	Conductor resistivity
ω	Angular frequency
ω_0	Unity gain frequency
ω_{ESR}	Zero caused by the capacitor ESR
ω_{LC}	Pole caused by the inductor-capacitor filter
ω_{p1}	Compensator pole
ω_{p2}	Compensator pole
ω_{z1}	Compensator zero
ω_{z2}	Compensator zero

1. INTRODUCTION

Efficiency is one crucial design parameter in switched mode converters and this master's thesis investigates how to model efficiency in a buck converter using simulation of piecewise linear systems (SIMPLIS). Previously efficiency simulations were done using the integrated circuit (IC) simulation tools in Cadence or doing rough approximations with Excel calculators. Cadence simulations are accurate, but Cadence simulations have multiple caveats that make running efficiency simulations not very user-friendly.

Firstly, using Cadence for efficiency simulations requires setting up libraries, loading setup states and so on before the simulation can even be run. Also, the user must have the intellectual property available to run the simulation and therefore sharing the Cadence simulation model with customers is not even a possibility. Secondly, Cadence simulations tend to be quite slow with larger design. The alternative option was to make an Excel calculator that does rough approximations on different losses. However, these calculators are rough approximations and modeling all the possible configurations with Excel becomes difficult. Therefore, SIMPLIS is more appropriate and more user-friendly simulator for the task.

SIMPLIS is a simulator with specific analysis tools, such as periodic operating point analysis, which is especially tailored for switched mode converters. SIMPLIS differs from the conventional simulators by making linear approximations to speed up simulations without having a great impact on simulation accuracy. SIMPLIS supports model encryption which opens the possibility of sharing the efficiency model with customers.

The simulation model is made for a new device called TPS6594x-Q1 which incorporates five integrated synchronous buck converters. Synchronous buck converters convert a higher direct (DC) voltage to a lower DC voltage with two switches, an inductor and filtering capacitors. Each of these components is responsible for power loss in the conversion process. Printed circuit board (PCB) on which the whole system is assembled causes power losses as well. There are some other loss components inside the IC as well such as gate driver losses and bondwire losses. Some of the losses can be classified as switching losses which are caused by the switching events and rest of the losses are categorized as conduction losses. The simulation model tries to model all the previously mentioned losses and keep the simulation time reasonable.

Chapter 2 covers the basics of buck converters such as Ampere-second and Voltage-second balance, the transfer function of ideal and non-ideal buck converters, voltage and peak current control as well as efficiency in general. Also, a brief overlook on TPS6594x-Q1 is taken. Chapter 3 focuses on the used simulator SIMPLIS, its features and peculiarities. Chapters 4 and 5 differentiate the different loss mechanisms present in buck converters. Chapter 4 focuses on the losses happening inside the IC whereas the chapter 5 emphasizes on the losses occurring in the external components. Chapter 6 covers the different measurements done for the simulation model to help the modeling process. In chapter 7, the actual modeling process is described. Chapter 7 is the results chapter where the simulation results are validated against real efficiency measurements and finally chapter 8 gives the conclusions about the work done in the master's thesis and gives ideas for future research.

2. BUCK CONVERTER

Buck converters, also known as step-down converters, are one the three basic switched-mode regulators. Buck topologies convert DC voltage to a lower level by charging an inductor, during on-time, connected in series with a switch and using the built-up magnetic field to supply the load during off-time. The resulting output voltage is ideally dependent on only duty ratio and input voltage

$$V_{OUT} = DV_{IN}, \quad (1)$$

where V_{OUT} is the output voltage, D is duty ratio and V_{IN} is input voltage. [1, p. 568–569] However, equation 1 will become more complex when the power losses will be taken into account. The basic buck converter circuit is shown in Figure 1.

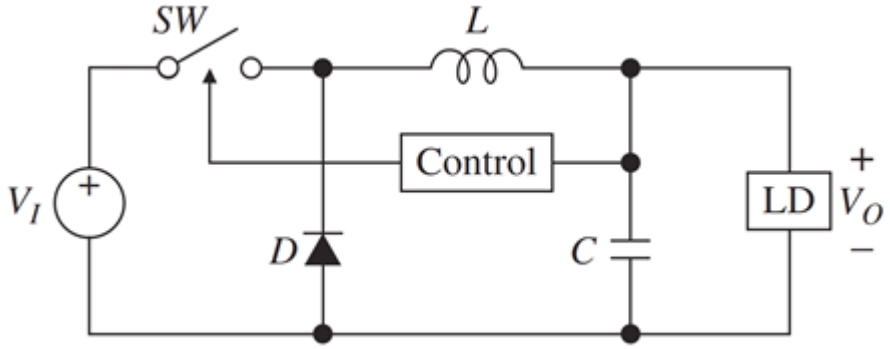

Figure 1. *Basic buck converter circuit [1, p. 568].*

Output voltage equation is derived using Ampere-second and Voltage-second balance equations which state that the average inductor voltages and the average capacitor currents are zero over one switching cycle in steady state. [2, p. 46–47]. In practice, the circuit is divided into two subcircuits for the on- and off-time from which the inductor voltage and the capacitor current equations are solved. After that, the Ampere-second and Voltage-second balance rules are applied, and the transfer function can be calculated.

The circuit shown in Figure 1 can be improved by replacing the diode with a second switch. When two switches, for example field-effect transistors (FET) are used as shown in Figure 2, the circuit is called a synchronous buck converter.

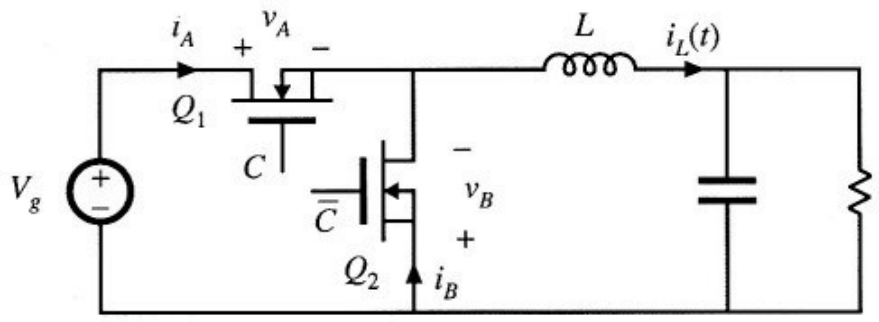

Figure 2. *Synchronous buck converter [2, p. 74]*

The advantage of using a transistor instead of a diode as a low side (LS) switch is that the forward voltage loss of the diode becomes a major source of power loss especially in low voltage devices. Metal-oxide-semiconductor field-effect transistor (MOSFET) typically has lower voltage loss than diodes. [1, p. 577], [2, p. 73–74] Adding some of the losses to the schematic in Figure 2 results in a schematic shown in Figure 3.

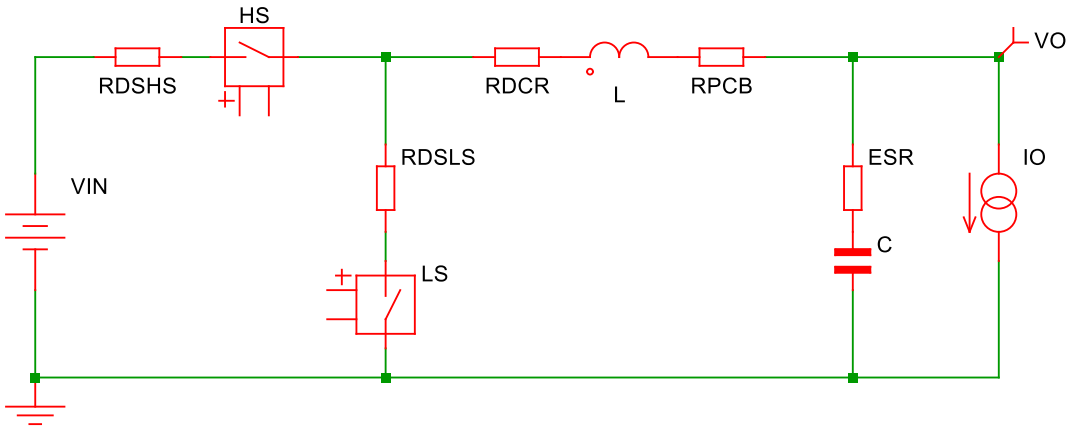

Figure 3. *Synchronous buck converter with some of the losses included.*

Calculating the output voltage equation with the losses included using Voltage-second and Ampere-second balance equations, the output voltage becomes

$$V_{OUT} = DV_{IN} - I_o[(R_{DSHS} - R_{DSLS})D + R_{DSLS} + R_{DCR} + R_{PCB}], \quad (2)$$

where I_o is the output current, R_{DSHS} and R_{DSLS} are high side (HS) and low side MOSFET channel on-resistances, R_{DCR} is the DC resistance (DCR) of the inductor and R_{PCB} is the resistance of the PCB. Due to the losses caused by the external components, the output voltage is now also dependent on the output current as well as input voltage and duty ratio.

Apart from the switching transistors, the other two important components are the inductor and the capacitor. The inductor has an impact on inductor current slope and current ripple where smaller inductance causes higher slope and larger current ripple than larger inductance. Current ripple can be calculated using equation

$$\Delta i_L = \frac{(V_{IN} - V_{OUT})D}{2Lf_{sw}} = \frac{V_{OUT}(1-D)}{2Lf_{sw}} \quad (3)$$

where L is the inductor's inductance and f_{sw} is switching frequency. However, this equation is valid only for fixed frequency devices and does not consider the parasitic losses in the circuit that were shown in Figure 3. [2, p. 17–19]

Output capacitor influences the output voltage ripple which can be calculated with equation

$$\Delta v_{OUT} = \frac{\Delta i_L}{8Cf_{sw}} \quad (4)$$

where C is the capacitance of the output capacitor [2, p. 33]. However, equation 4 is idealistic and does not consider the equivalent series resistance (ESR) of the capacitor which also causes voltage ripple. Based on application report done by Surinder P. Singh [3] the output voltage ripple also depends on the duty ratio. He showed that the peak-to-peak output voltage ripple can be calculated with

$$\Delta v_{OUT} = \frac{\Delta i_L R_{ESR}^2 C}{T_{off}} + \frac{\Delta i_L}{2CT_{off}}\left(\left(\frac{T_{off}}{2}\right)^2 - (R_{ESR}C)^2\right) + \frac{\Delta i_L R_{ESR}^2 C}{T_{on}} + \frac{\Delta i_L}{2CT_{on}}\left(\left(\frac{T_{on}}{2}\right)^2 - (R_{ESR}C)^2\right) \quad (5)$$

where Δi_L is the inductor current ripple, R_{ESR} the equivalent series resistance of the capacitor, C is the capacitance value and T_{on} and T_{off} are high side on- and off-times respectively. However, often simpler approximations are used for quick calculation of the output voltage ripple. One of these simpler models is

$$\Delta v_{OUT,RMS} = \sqrt{\left(\frac{\Delta i_L}{8Cf_{sw}}\right)^2 + (\Delta i_L R_{ESR})^2} \quad (6)$$

which assumes that the total voltage ripple is a sum of voltage ripples of capacitor and ESR alone. [3, p. 5–10]

2.1 Control

There are multiple different parameters that may vary between different buck converter implementations including output voltage, input voltage, load current and component values. Still, the buck converter should do its task to regulate and output a constant output voltage. With an open loop design and constant duty ratio, changing any of the parameters results in a different output voltage. For example, an increase in load current increases voltage drop over the filtering circuitry resulting in a lower output voltage. Therefore, constant duty ratio buck converters do not have many use cases. In

practice, it is required for the buck converter to have a control loop for the converter to acquire precise output voltage that is not dependent on load current. [2, p. 331–332]

The main idea of the control loop is to adjust the duty ratio to keep the output voltage constant despite the variations in component values, disturbances in input voltage and changes in output current using negative feedback. One concern when using a feedback loop is the overall stability of the system and adding the feedback to an otherwise stable device may cause unwanted behavior. [2, p. 332–334] Two of the most basic control design techniques will be introduced here called voltage mode control (VMC) and peak current mode control (PCMC).

2.1.1 Voltage mode control

Voltage mode control uses an error amplifier to compare the scaled output voltage and internal reference voltage V_{REF}. An error amplifier must be correctly designed to compensate against the delays introduced by the other components of the control loop, for example, output voltage filter. If the loop is not compensated for the other components in the control loop, the phase margin, and thus the overall stability of the circuit, will suffer. Therefore, the error amplifier is often called a compensator. The basic voltage mode control loop is shown in Figure 4.

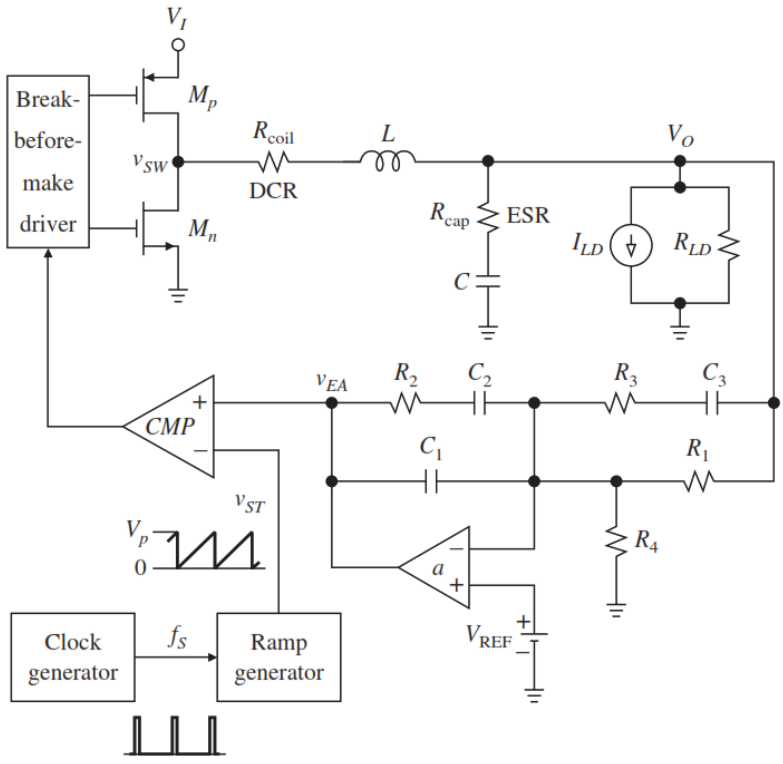

Figure 4. *Voltage mode control feedback in buck converter [1, p. 578].*

The compensator compares the output voltage to the internal reference voltage and generates voltage v_{EA}. The compensator output voltage v_{EA} is then compared against ramp generators output sawtooth waveform which is generated at switching frequency. If the compensator's output voltage is higher than the ramp, the comparator outputs a logical one driving output voltage higher and vice versa. [1, p. 575–579]

To derive the transfer function for the voltage control loop shown in Figure 4, a simplification to the alternating current (AC) analysis is done by using Thévenin's theorem on the power stage. The resulting Thévenin's equivalent for circuit is shown in Figure 5.

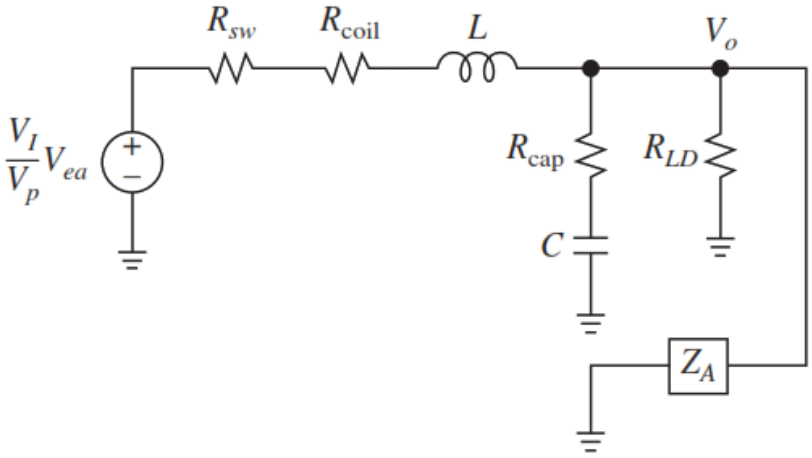

Figure 5. *AC equivalent circuit for the output filtering [1, p. 579].*

R_{sw} in the Figure 5 is the effective resistance of the power stage. The DC current sink that was used in the load is not present in the AC analysis because a DC current sink in an AC analysis is an open circuit. Also, the error amplifier's impedance Z_A is terminated to ground due to the virtual AC ground of the operational amplifier. If R_{LD} and Z_A can be neglected the transfer function for the control loop is

$$T(j\omega) = \frac{V_I}{V_p} \frac{1 + \frac{j\omega}{\omega_{ESR}}}{1 - \left(\frac{\omega}{\omega_{LC}}\right)^2 + (\frac{j\omega}{\omega_{LC}})/Q} \cdot \frac{(1 + \frac{j\omega}{\omega_{z1}})(1 + \frac{j\omega}{\omega_{z2}})}{(\frac{j\omega}{\omega_0})(1 + \frac{j\omega}{\omega_{p1}})(1 + \frac{j\omega}{\omega_{p2}})} \tag{7}$$

where

$$\omega_{LC} = \frac{1}{\sqrt{LC}}, \omega_{ESR} = \frac{1}{R_{cap}C}, Q = \frac{\sqrt{\frac{L}{C}}}{R_{sw} + R_{coil} + R_{cap}}. \tag{8}$$

Variables ω_{z1}, ω_{z2}, ω_{p1} and ω_{p2} are compensator zeros and poles respectively and ω_0 is the unity gain frequency. Input voltage is V_I and V_p is the peak voltage of the ramp generator. For the definitions of the different resistances and other component values,

refer to Figure 5. Zero introduced by ω_{ESR} is also called a left-half plane zero (LHPZ) and it is the frequency where the gain slope increases from -40 dB/decade to -20 dB/decade.

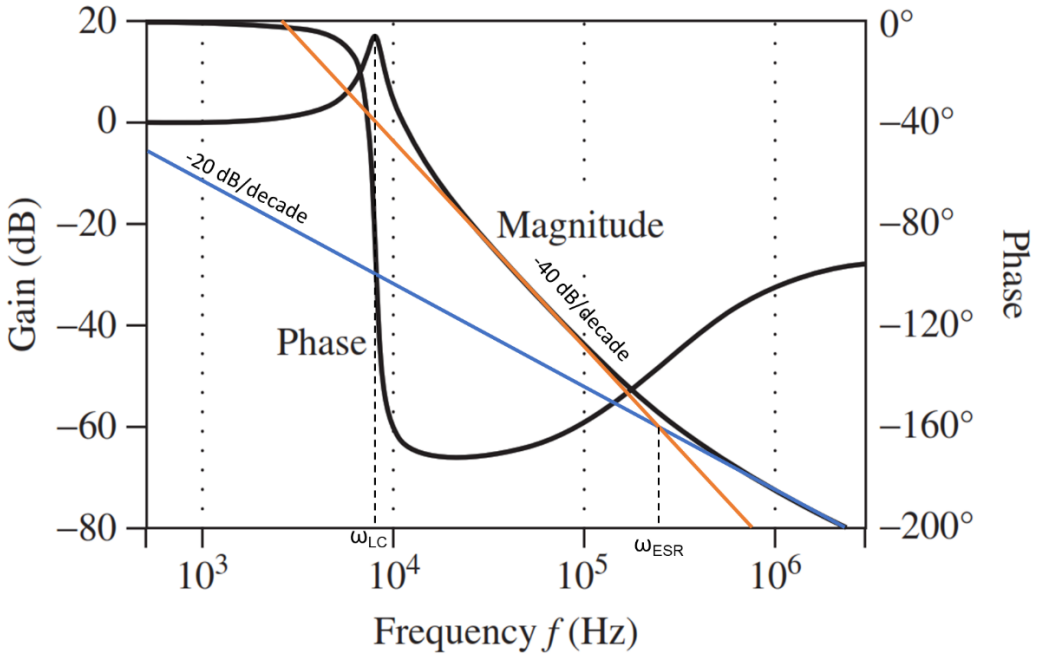

Figure 6. *Bode plot of a 10 µH and 40 µF inductor-capacitor (LC) filter. Edited from [1, p. 580].*

Figure 6 shows a bode plot of the inductor-capacitor filter where the ω_{LC} pole pair and zero ω_{ESR} created by the loop can be seen. Pole pair is at 8 kHz and zero caused by the ESR is at 265 kHz. [1, p. 574–582]

The error amplifier introduces two zeros and two poles in total. Rules for placing poles and zeros of the control loop are not explicit and may differ depending of the referred literature source. Generally, the crossover frequency should be placed at least a decade below the switching frequency. Zeros introduced by the feedback should be placed in similar frequencies as ω_{LC} to reduce the effect of the LC filter poles. Feedback poles should be placed near switching frequency. [1, p. 581–582]

2.1.2 Peak current mode control

Peak current mode control tries to force the inductor to act as a voltage controlled current source (VCCS). Advantages of using PCMC compared to VMC are that the inductor delay is removed from the loop making the design of the compensator simpler as well as this cycle-based control mechanism protects the inductor from excessive currents if the compensator's output is not limited. [1, p. 582–583] The basic circuitry for peak current mode control in a buck converter is shown in Figure 7.

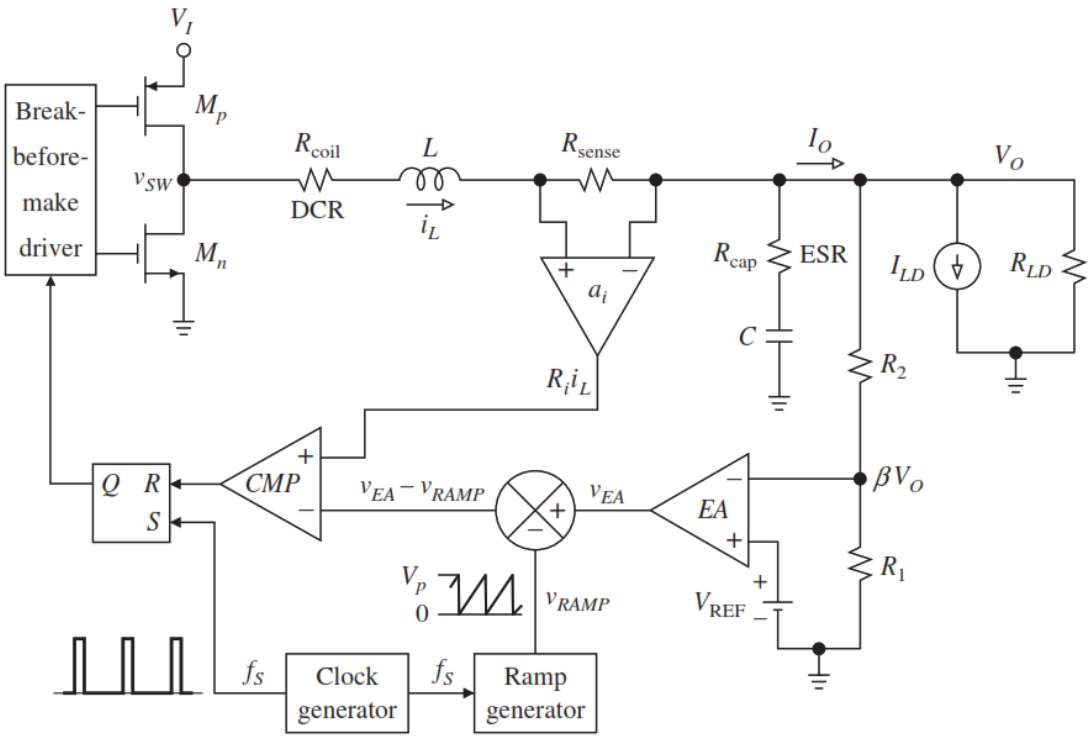

Figure 7. *Peak current mode control loop in a buck converter [1, p. 583].*

Controlling inductor current requires a way to sense the current and in Figure 7 this is done with a sense resistor and a sense amplifier. Other possible ways to sense the inductor current is to sense the current over the HS channel resistance or sense the current across the whole inductor. In practice, a similar current system is practically a requirement for any duty ratio-controlled system to protect the transistors from high currents during transients or fault conditions. All the same, this has a serious drawback because the sense resistance must be low in order to keep the efficiency as high as possible, consequently making the sensing more susceptible to noise. Therefore, some filtering on the sensed current waveform is usually necessary. [1, p. 583], [2, p. 441]

The most basic current mode-controlled (CMC) systems are not stable when duty ratio is over 0.5 or 50 %. Instability is a result of the inductor current not having enough time to fall back to the starting current of the switching cycle, resulting in an oscillating inductor current. Oscillation could begin, for example, from a current load transient. This phenomenon is called subharmonic oscillation and it is illustrated in Figure 8. [1, p. 585], [2, p. 441–443]

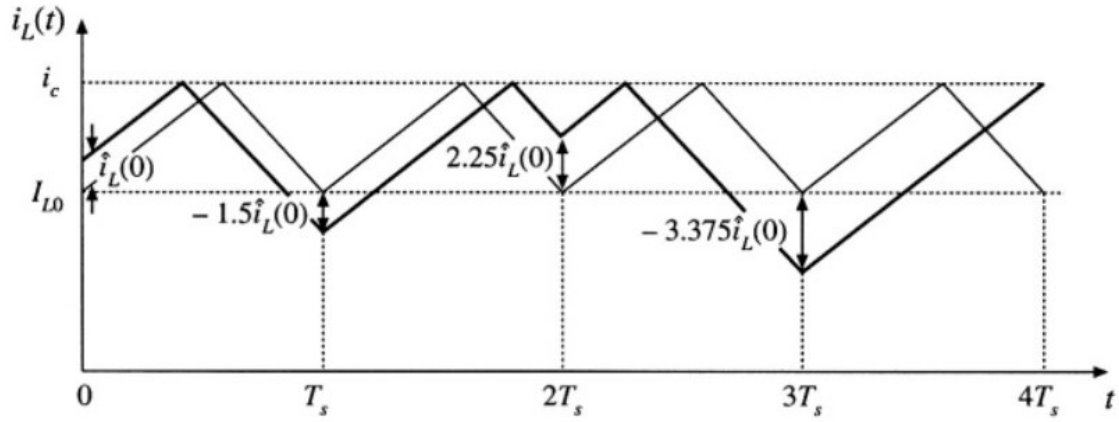

Figure 8. *Subharmonic oscillation with duty ratio of 0.6 [2, p. 445].*

To fix the instability problem with high duty ratios, the inductor current waveform must be pushed down. This is done by subtracting a ramp generator waveform from the output signal of the error amplifier. The sawtooth waveform changes the level where the comparator switches state as shown in Figure 9.

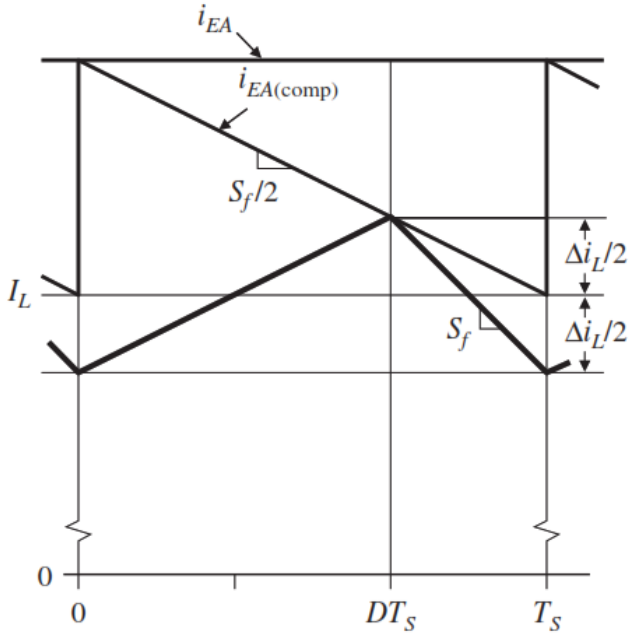

Figure 9. *Slope compensated inductor current waveform [1, p. 587].*

Symbol S_f is the down slope of the inductor current, Δi_L is the inductor current ripple, I_L is the average inductor current, D is the duty ratio and T_S is the length of a switching period in seconds. Comparison currents i_{EA} and $i_{EA(comp)}$ are the uncompensated and slope compensated comparison currents and these are the inductor currents when control loop turns the high side MOSFET off. Uncompensated comparison current can be calculated with

$$i_{EA} = \frac{v_{EA}}{R_i} \tag{9}$$

where v_{EA} is the output voltage of the error amplifier and R_i is the overall gain of the current sense amplifier. The compensated current limit is calculated by simply subtracting the ramp signal from the error amplifiers output as in Figure 7 and thus can be calculated with

$$i_{EA} = \frac{v_{EA} - v_{RAMP}}{R_i} \tag{10}$$

where v_{RAMP} is the ramp voltage from the ramp generator. This technique is called slope compensation which also solves the subharmonic oscillation problem. An alternative variant of this solution is to add a ramp signal to the output of the current sense amplifier instead of subtracting the ramp from error amplifier's output. Waveforms and the schematic will differ slightly, nonetheless the basic working principle is the same with either approach. [1, p. 585–587], [2, p. 446–447]

2.2 Efficiency

Switching regulators are efficient regulators compared to linear regulators which are the other commonly used direct voltage to direct voltage (DCDC) converters. Linear regulator's efficiency varies greatly depending on the input voltage and the efficiency may be even below 50 %. Special low-dropout regulators (LDO) may operate fairly efficiently when the input voltage is close to the output voltage but switched mode converters such as buck converters can operate efficiently regardless of the input voltage. The cost of higher efficiency is the increased component count as an inductor and a capacitor are required to filter the output voltage. Also, the overall complexity of the circuit increases due to the need of a control loop. [1, p. 567]

Regulator's efficiency can be calculated using the normal efficiency equation

$$\eta = \frac{P_{out}}{P_{in}} = \frac{P_{out}}{P_{out} + P_{diss}} \tag{11}$$

where P_{out} is the output power and P_{in} is the input power. Another semantically different way to calculate the efficiency is to use the sum of the output power and the dissipated power P_{diss} as the divider but either one will give the same result. [1, p. 574] Usually these losses are temperature, output current and phase count dependent which results in efficiency graphs drawn as a function of output current as shown in Figure 10.

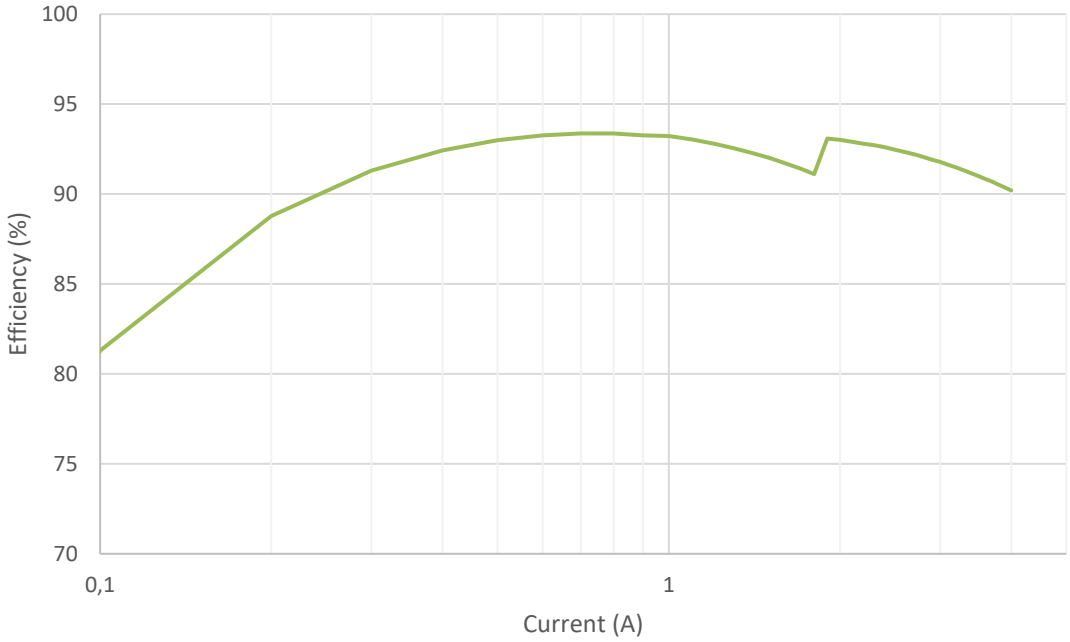

Figure 10. *Efficiency graph of two-phase TPS6594x-Q1 with 1.8 V output voltage and 3.3 V input voltage in room temperature.*

High load current efficiency can be improved for example using multiple switching phases in parallel and this can be seen from Figure 10 where the small efficiency increase at around 2 A is the moment when the second phase begins to switch [4, p. 1937]. Adding a second phase halves the conduction losses in power MOSFETs and inductors. Implementation of a basic two-phase multiphase configuration is shown in Figure 11.

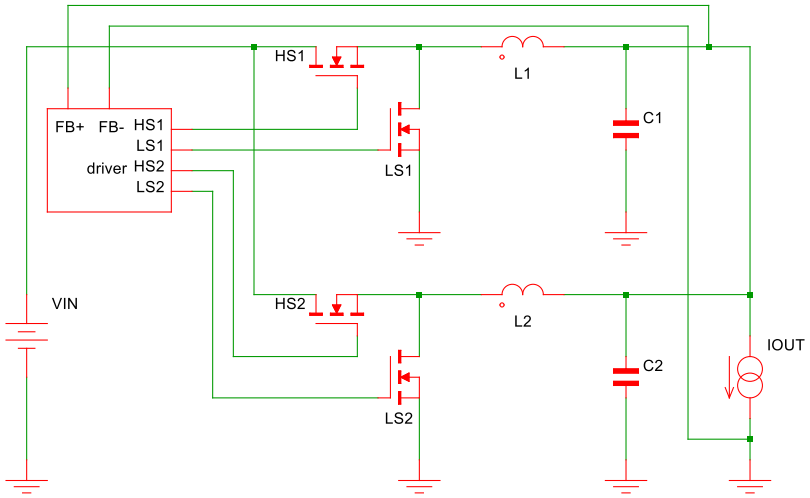

Figure 11. *Two-phase synchronous buck converter.*

The different phases are often interleaved with each other which effectively increases the switching frequency. Other advantages of using multiple switching phases are

current ripple reduction, faster transient response and reduction in passive component values. [5, p. 4769]

However, it is not always optimal to use all the available phases as more switching phases leads to higher switching losses. A converter that has high efficiency on high currents is not that efficient with smaller load currents and therefore it is desirable to control the number of phases used in buck converter. At higher load currents conduction losses dominate and on lower load currents the switching losses dominate and consequently with low load currents some of the phases should be shut down to improve efficiency. [6, p. 1025] Peak efficiency of a phase occurs when

$$RI_{OUT}^2 = CV_{DD}^2 f_{sw} \tag{12}$$

where R and C are the average parasitic resistance and the average parasitic capacitance of the phase respectively and I_{OUT} is the output current and V_{DD} is the supply voltage. [7, p. 2225] Another phase should start to switch when the power losses of multiple phases are the same as with less phases. The change happens at a current that is somewhat larger than the current where the peak efficiency occurs with less phases.

For low current applications pulse-skipping and pulse-frequency modulation (PFM) could be used to improve efficiency. With low load currents the switching losses dominate the total power losses in the circuit and the inductor current may fall negative. Negative inductor current introduces additional power losses since it causes the output capacitor to discharge. PFM eliminates the negative inductor current in low output current conditions by driving the circuit into discontinuous conduction mode (DCM) and reduces the switching frequency resulting in decreased switching losses. The obvious downside of using PFM control is the increased complexity of an already complex control loop. Control system must sense the current where it is beneficial to switch between pulse-width modulation (PWM) and PFM modes. PFM mode also introduces multiple different limits for output current and voltage which the control system should take into consideration. The control loop may monitor peak inductor current, inductor current zero-crossing detection, output voltage upper threshold and output voltage lower threshold but it is not necessary to monitor all the mentioned thresholds for the device to function correctly. [8, p. 6555], [9, p. 181], [10, p. 28–29]

In this thesis the losses have been further divided in to internal and external losses. Internal and external in this context mean in terms of the IC. The total dissipated power consists of multiple different parts and can be expressed with following equation

$$P_{losses} = P_{FET\_cond} + P_{sw} + P_{driver} + P_{logic} + P_L + P_{cap} + P_{pcb} \tag{13}$$

where P_{FET_COND} is the conduction loss caused by high side and low side MOSFETs, P_{sw} is the switching loss of high side and low side MOSFETs, P_{driver} is the power loss

caused by the driver, P_{logic} is the loss from the control and logic circuitry, P_L is the loss from the output inductor, P_{cap} is the loss caused by the input and output capacitors and P_{pcb} is the loss from PCB parasitics.

2.3 The studied topology

The power-management integrated circuit (PMIC) for which the efficiency model is made is Texas Instruments TPS6594x-Q1. TPS6594x-Q1 includes five synchronous buck converters and four of them can be configured to a multiphase configuration. Buck converters automatically switch between PFM and PWM modes depending on the device configuration and load current. The device operates in PWM mode at currents over 600 mA and in PFM mode with lower load currents. However, the device can be configured to work on forced PWM mode where the device operates in PWM mode at all times. [11, p. 78]

In multiphase operation, the different phases have been interleaved by 90 to 180-degree phase shift depending on the phase count. Interleaving the phases moves the voltage ripple frequency higher on the frequency spectrum which eases the requirements for the output filtering. TPS6594x-Q1 does automatic phase adding and shedding depending on the load current to maximize the efficiency, but it is also possible to force multiphase operation. However, fifth buck converter is always in single phase mode and therefore the model focuses on only the four main phases [11, p. 79]

3. SIMPLIS

SIMPLIS is a circuit simulation software designed with switching power systems in mind. Commonly used simulation program with integrated circuit emphasis (SPICE) works similarly on component level as SIMPLIS but SIMPLIS may be up to 50 times faster compared to SPICE simulators. The speedup is achieved by using piecewise linear (PWL) modeling and simulation techniques whereas SPICE solves nonlinear expressions. [12, p. 3–4] Based on comparison made by Grajdeanu et al. [13] SIMPLIS does suffer from lower simulation accuracy compared to the other simulators, Cadence Virtuoso, Matlab Simulink and CppSim, used in the comparison. Simulation time with SIMPLIS was indeed significantly lower compared to the other simulators. [13]

SIMPLIS is compatible with nonlinear SPICE models to ensure the compatibility with the wide range of different SPICE models available. SIMPLIS does a conversion from a SPICE model to a PWL model when the device is placed on the schematic. The conversion is done by running a sequence of simulations using SIMetrix SPICE simulator. Example of PWL approximation is shown in Figure 12 where blue PWL approximation of body diode (BD) current as a function voltage (I-V) is compared against similar red SPICE curve.

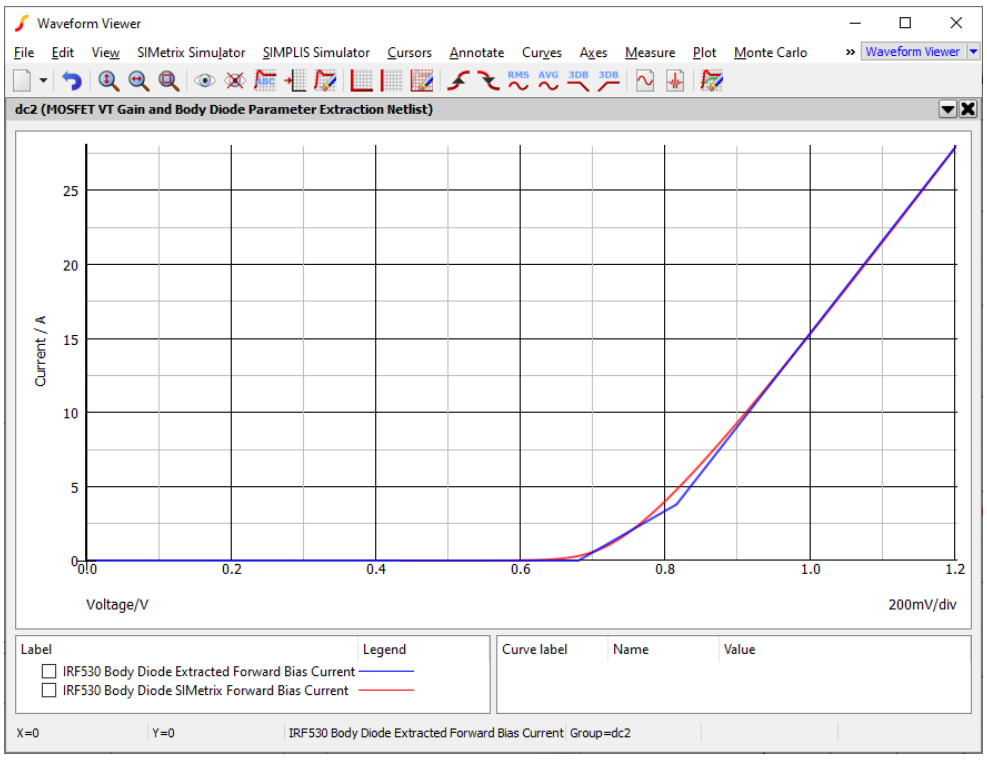

Figure 12. *PWL approximation (blue) of a body diode I-V curve from SPICE model (red).*

The PWL nature of the SIMPLIS is clearly noticeable from Figure 12 where the blue waveform generated by SIMPLIS consists of three linear segments. SIMPLIS supports this SPICE model conversions for MOSFETs, bipolar junction transistors (BJT) and diodes. [12, p. 4]

3.1 Periodic operating point analysis

SIMPLIS provides three different analysis methods for simulations: transient, periodic operating point (POP) and AC. Periodic operating point analysis is one of the unique features in SIMPLIS that automatically finds the steady state operating point of switched systems. POP analysis does not have to simulate the whole power up sequence of the switched system which results in drastic speed up on the design analysis. [12, p. 241]

The POP analysis begins with simulator running transient simulations until a new switching cycle is found or maximum period parameter is reached. Maximum period is defined with keyword MAX_PERIOD and it defines how long each transient simulation can be run until an error message is shown. However, if the transient analysis finds a new switching cycle, the next task is to find out if the system is in steady state. Steady state analysis utilizes the basic steady state rules introduced in the beginning of chapter 2 as Ampere-second and Voltage-second balance. SIMPLIS compares the capacitor voltages and inductor currents at the beginning and at the end of the switching cycle. If the differences in voltages and currents between the start and the end of switching cycle is negligible, the system is in steady state and POP analysis is completed. The difference that SIMPLIS considers as negligible is defined with keyword CONVERGENCE and the default value for it is 1E-12 percent. [14, p. 131]

If the system is not in steady state, the POP analysis does a prediction what the capacitor voltages and inductor currents should be at the beginning of steady state switching cycle. Then a new transient analysis is done again and the whole algorithm repeats until the steady state conditions are reached or maximum iteration limit is reached. Maximum iteration limit is defined with keyword POP_ITRMAX. If iteration count reaches iteration limit an error message is displayed and the POP analysis is aborted. [14, p. 131]

3.2 MOSFET modeling in SIMPLIS

For the efficiency model, it is crucial to model MOSFET parasitics as accurately as possible as will be seen in chapter 4. If the simulation model is being made from a circuit that is using discrete transistors for the power stage and SPICE models for those

transistors are available, then the modeling process will be trivial. SPICE model can be extracted automatically using the model extraction dialog shown in Figure 13.

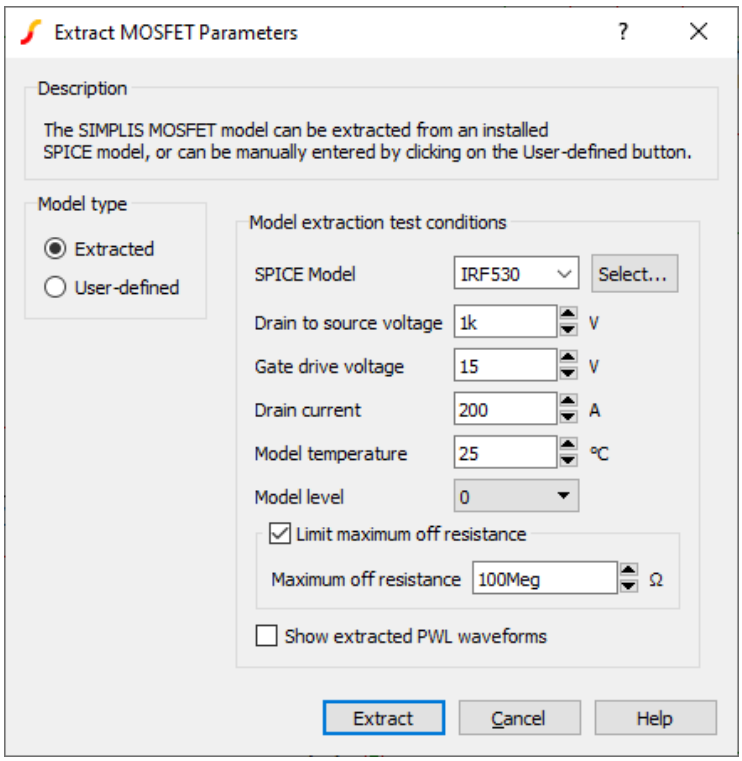

Figure 13. *MOSFET SPICE parameter extraction dialog.*

The SPICE model and the operating conditions are simply selected from the dialog and then SIMPLIS does a PWL approximation for the selected SPICE model. [15] However, TPS6594x-Q1 uses integrated power stage MOSFETs and there are no publicly available SPICE models available for them. Therefore, the MOSFET modeling must be done manually by modifying PARAM_VALUES property of a user defined MOSFET or making one of the equivalent circuits.

All MOSFET simulation parameters are stored in PARAM_VALUES property which is a space separated text string. For example, IRF530 has following parameters when making user defined MOSFET with default settings shown in Program 1.

```
USE_EXTRACTED=0 DEVICE='IRF530' LABEL='USER_LABEL' VD_PEAK=1k VGSON=15
ID_PEAK=200 TEMP=25 LEVEL=0 LIMIT_MAX_ROFF=1 MAX_ROFF=100Meg
USER_RDSON=10m USER_ROFF=100Meg USER_VT0=2.5 USER_HYSTWD=250m USER_CGS=0
USER_RG=0 USER_COSS=0 USER_DIODE_FWD_VOLTAGE=750m USER_DIODE_FWD_RES=10m
RG=0 CGS_NSEG=0 IBD0=-1 IBD1=0 IBD2=0 IBD3=1 BD_NSEG=3 VD0=-10.001k VD1=-
10k VD2=0.75 VD3=0.76 ROFF=100Meg RDSON=10m HYSTWD=250m VT0=2.5
CDS_NSEG=0 QCDS0=0 QCDS1=0 CDG_NSEG=0 VCDS0=0 VCDS1=1 VCGS0=0 VCGS1=1
QCGS0=0 QCGS1=0
```

Program 1. *Default PARAM_VALUES property for IRF530.*

Some of the parameters are quite self-explanatory, for example RDSON or TEMP, but parameters such as QCDS0, QCDS1 and CDG_NSEG are not clear at first glance.

Parameters such as IBDx, VDx, VCDSx, QCDSx, VCGSx and QCGSx are points that determine the PWL curve point by point. Capacitances are represented charge as a function of voltage (Q-V) curves with the voltage and charge parameters in the PARAM_VALUES property. The parameters with underscore NSEG determine the number of PWL segments for a given characteristic. [15]

However, this PARAM_VALUES list can be further extended by adding additional PWL points to the string and by increasing the model level parameter LEVEL. If taking a look at CDG_NSEG, in other words, number of PWL segments for drain-gate capacitance is set to zero which means that C_{DG} is not modelled. Even if the number of segments is increased and the PWL points are defined C_{DG} is still not modeled. This is because the default model level for user defined MOSFET models is zero and this can be changed by changing parameter LEVEL. Highest and thus the most complex and accurate model level is three. [15]

The simplest transistor model in SIMPLIS is the level 0 model and for efficiency modeling it is not usually accurate enough. Equivalent circuit for level 0 MOSFET model is shown Figure 14

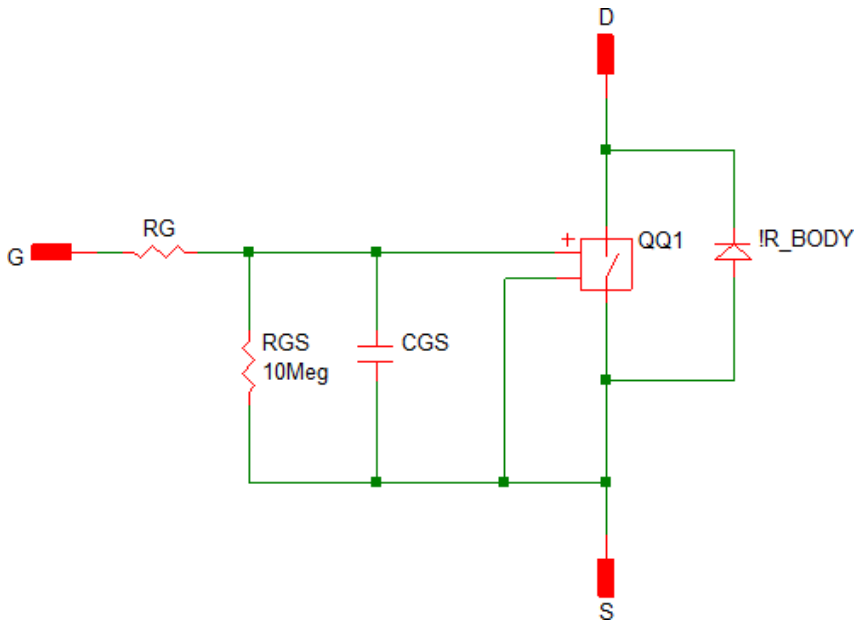

Figure 14. *Equivalent circuit for level 0 MOSFET model [15].*

Level 0 model includes transistor off and on-resistances, a linear gate-source capacitance C_{GS}, a gate-source resistance R_{GS}, a gate resistance R_G and a body diode modelled with PWL resistor. More accurate level 1 equivalent circuit is shown in Figure 15.

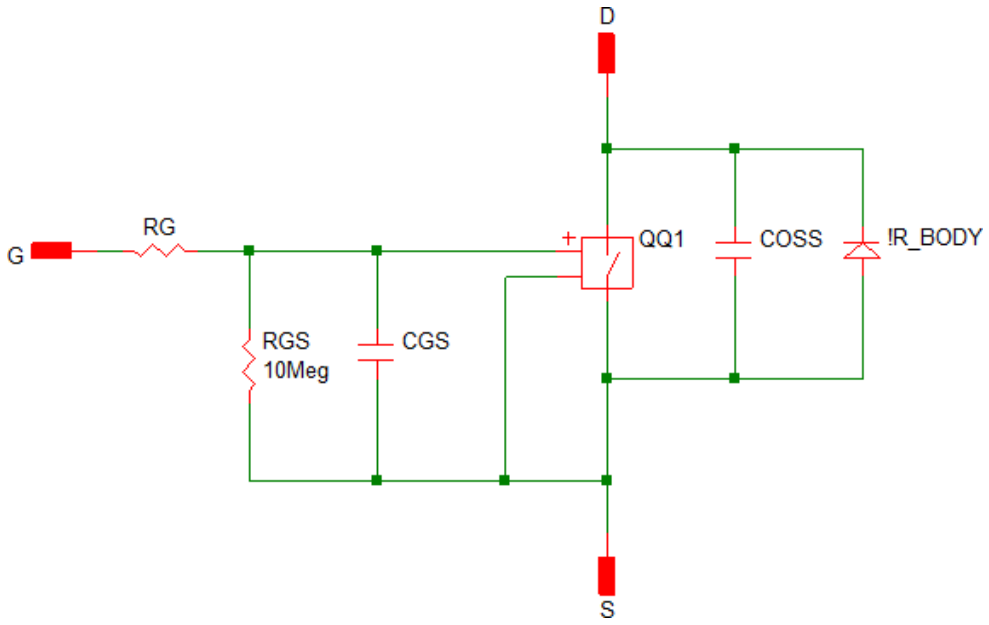

Figure 15. *Equivalent circuit for level 1 MOSFET model [15].*

Level 1 adds a bulk output capacitance C_{OSS} in parallel with the body diode. Value of the C_{OSS} capacitor is calculated with equation

$$C_{OSS} = \frac{Q_{CDS1} - Q_{CDS0}}{V_{CDS1} - V_{CDS0}}. \tag{14}$$

where Q_{CDS} and V_{CDS} parameters are the points in the PWL Q-V curve. Basically the slope of the Q-V curve determines the capacitance between the voltage segments. Equivalent circuit for level 2 model is shown Figure 16.

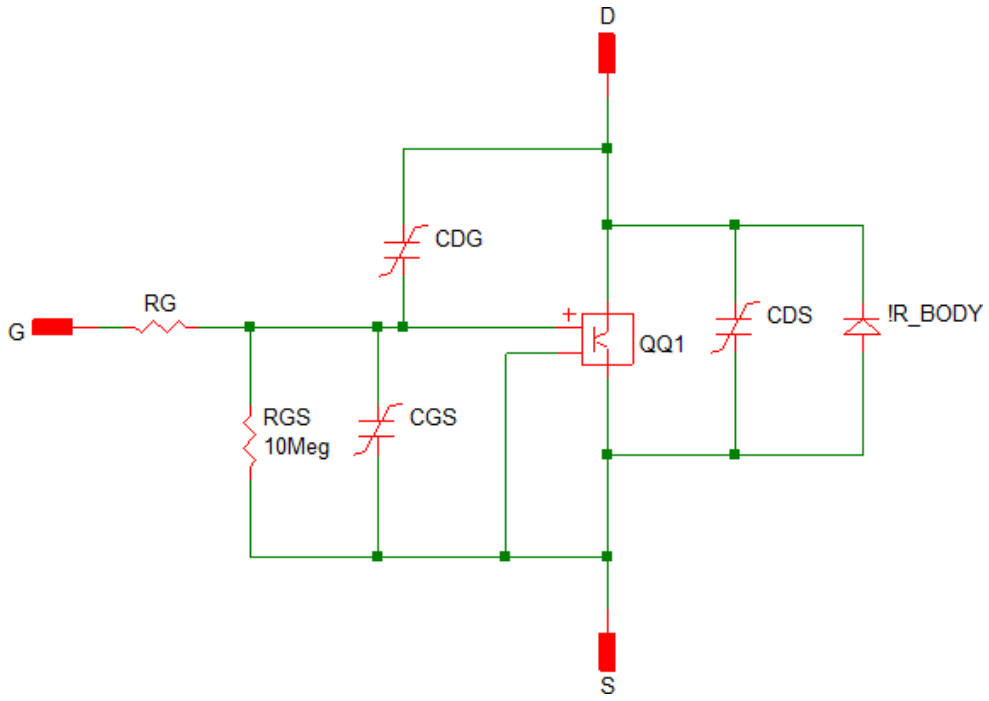

Figure 16. *Equivalent circuit for level 2 MOSFET model [15].*

Level 2 model splits the output capacitance C_{OSS} into a feedback capacitance, also known as Miller capacitance C_{DG}, and a drain-source capacitance C_{DS}. Nonlinearities of the capacitances are modeled with PWL segments and the number of segments can be defined with NSEG parameters. Level 2 model adds two-segment forward transconductance gain modeling as well. The most accurate level 3 model is shown in Figure 17

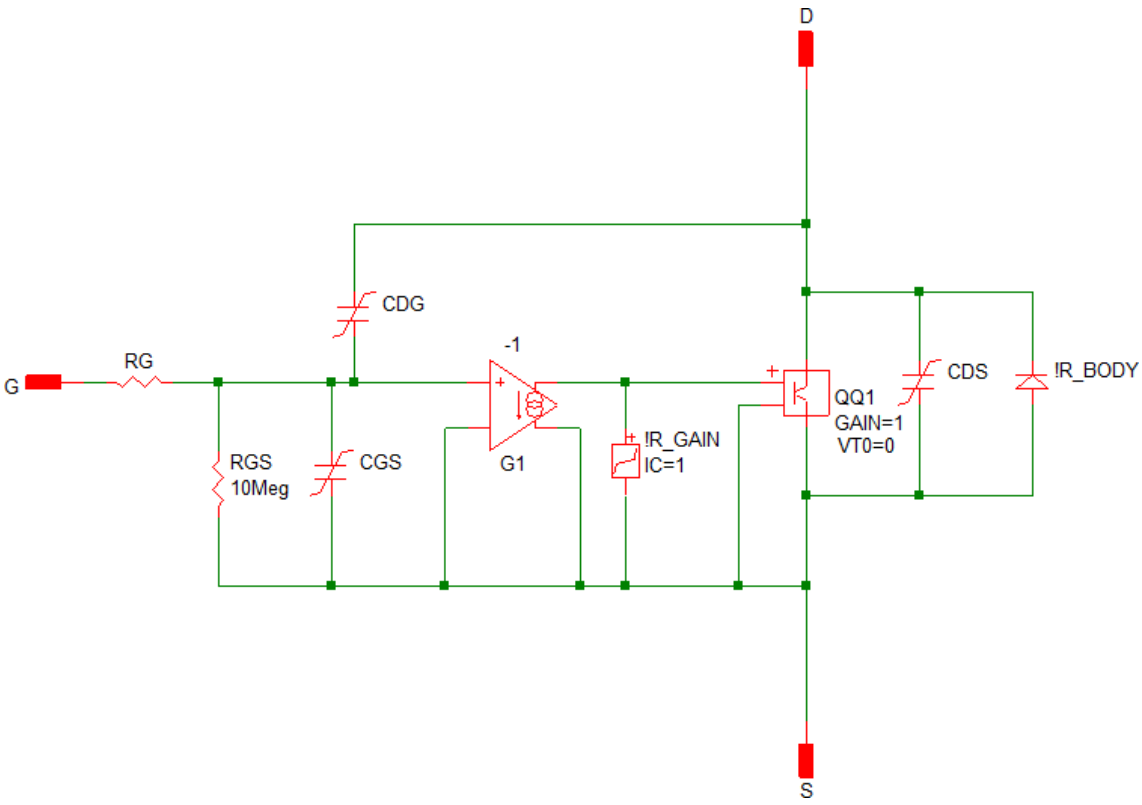

Figure 17. *Equivalent circuit for level 3 MOSFET model [15].*

The level 3 model extends the transconductance gain modeling by adding additional PWL segments for the transconductance model totaling up to five segments. Obviously, the most accurate level 3 model is also the slowest model to simulate and therefore the model level selection is a trade-off simulation accuracy and simulation time. [15]

3.3 Passive components

SIMPLIS provides multiple modeling levels for passive components, at least for capacitors and inductors and offers a possibility to model all passive components with PWL approximations. The different model levels add various parasitics to the circuit as in the basic equivalent circuits.

Table 1. *Parasitic modeling options in default SIMPLIS passive components.*

	RESISTORS	INDUCTORS	CAPACITORS
PARALLEL PARASITICS	-	-	Leakage resistance
SERIES PARASITICS	-	DCR	ESR and ESL
PWL	Voltage or Current dependent	Current-Flux linkage	Voltage-Charge

Table 1 summarizes the different features provided by the default passive components in SIMPLIS. Of course, the user has the possibility to make own subcircuits and add the desired parasitics that way. Even utilizing SPICE models that, for example manufacturer provides, is a possibility for the passive component models.

There are two different levels of inductor models in SIMPLIS. First one is an ideal inductor with or without a parallel shunt resistor and the second one is an inductor with parallel shunt resistor and DCR. These are called level 0 and level 1 models respectively. This multilevel modeling can be further extended by modeling the inductance with PWL approximations. The approximation is defined as flux linkage and current value pairs where the slope of the resulting curve is the inductance. This allows for example to model the effect of DC bias on the inductance value. [16] The models do not have a capacitor in parallel with the inductor which causes the parallel resonance at certain high frequency turning the inductor into a capacitor [17, p. 203]

Capacitors are modeled similarly as inductors in SIMPLIS but have one more possible model level to be utilized. Level 0 model is a capacitor with or without parallel leakage resistance and level 1 is the same as level 0 but with the ESR added. The most representative of reality is the level 2 model with equivalent series inductance (ESL) that causes the self-resonance frequency added on top of the leakage and series resistances. Same as with the inductor, capacitance can be modeled with PWL approximation with any of the previously mentioned model levels. Capacitance is defined with charge and voltage value pairs and the capacitance is the slope of the curve formed by the PWL points. [18] PWL approximation of capacitance is used in modeling the nonlinear MOSFET capacitances in this thesis.

Resistors are the most basic of the passive components and SIMPLIS does not have a multilevel part for resistors. All the SIMPLIS provided resistors are ideal in sense that they do not have a frequency dependence. User must create own subcircuit with the parasitic components if the frequency characteristics must be modeled. These parasitics

could be the parallel capacitance of the resistor and a series inductance. However, the I-V characteristics of a resistor can be modeled using PWL resistors. PWL segments are defined by voltage and current value pairs similarly as with capacitors and inductors. Reciprocal of the slope formed by the PWL point pairs is the resistance between the PWL points. There are two different kinds of PWL resistors, one for voltage controlled piecewise linear (VPWL) resistor and one for current controlled piecewise linear (IPWL) resistor. [17, p. 206], [19]

4. INTERNAL LOSSES

The power losses of an integrated power management circuit consist of losses caused by field-effect transistors and losses caused by controlling the transistors that includes the FET driver and the control logic. [20, p. 22] Also, the packaging and especially bondwires cause power losses. Ideally a field-effect transistor turns on immediately after gate-source voltage has risen over a certain threshold. An ideal FET would not have any voltage drop from drain to source either and the drain current would rise immediately.

In reality, this is not the case and there are multiple different parasitics that cause significant switching and conduction losses. MOSFET parasitics include gate-drain, gate-source, drain-source capacitances as well as gate and drain-source resistances [21, p. 1508]. Most of the parasitics of MOSFETs are illustrated in Figure 18.

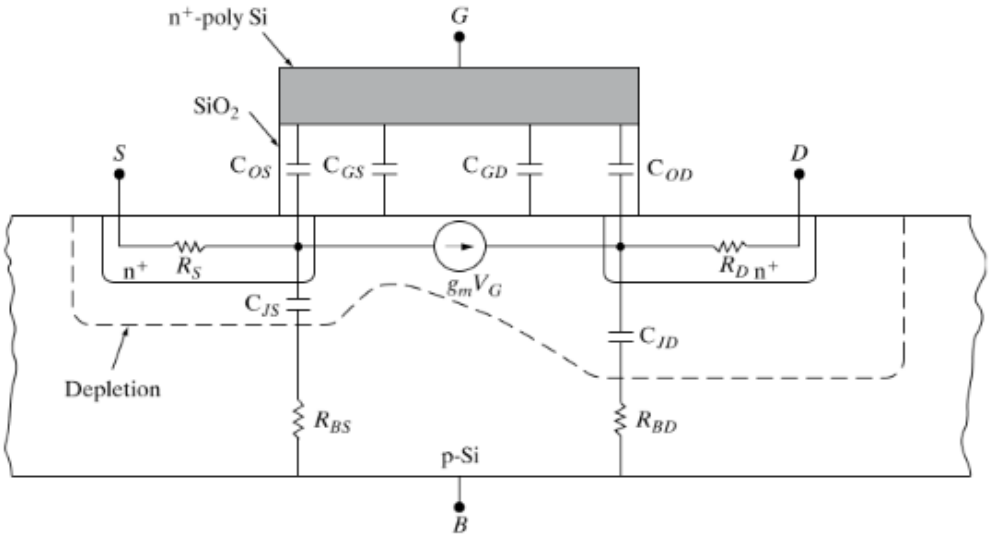

Figure 18. *Structure of a n-type MOSFET (NMOS) [22, p. 339].*

Body diode of the MOSFET might also cause losses depending of the use case of the transistor. Considering synchronous buck converters, the body diode in the low side MOSFET conducts during dead time causing conduction losses. [20, p. 25] The conducting body diode's reverse recovery effect, when high side MOSFET is turning on, causes a current spike in the transistor's turn-on current. [23, p. 705]

Some losses are caused by the actual packaging of the integrated circuit. For example, the structure of the integrated circuit exhibits bondwire and trace self-inductance, traces exhibit capacitance to ground and mutual trace-to-trace inductance and capacitance. Obviously, the traces and bondwires have some resistance as well and skin effect becomes a concern at higher frequency. Bondwire inductance and resistance

are the interesting parasitics in terms of this thesis due to the switching nature of the buck converter. Typical self-inductance of a bondwire varies from 2 nH to 20 nH depending on the length of the wire and packaging type. [24, p. 764–771]

4.1 DC losses

DC losses are the losses caused by the FET when the channel is fully conducting. Due to the nature of the loss source, it is relatively simple to model compared to the AC losses. Conduction losses are the high side FET conduction loss, low side FET conduction loss and low side FET body diode conduction loss. Conduction loss caused by body diode happens during deadtime when neither transistor is switched on. High side conduction loss is calculated with

$$P_{cond\_hs} = \left(I_o^2 + \frac{\Delta I_o^2}{12}\right) D R_{DSHS} \tag{15}$$

and low side FET conduction loss can be calculated similarly with equation

$$P_{cond\_ls} = \left(I_o^2 + \frac{\Delta I_o^2}{12}\right) (1 - D) R_{DSLS} \tag{16}$$

where I_o is output current, ΔI_o is output current ripple and R_{DSHS} and R_{DSLS} is the drain-source on-resistance of the high side and low side transistor respectively. [25, p. 315–317]

Drain-source resistance has a temperature dependency which can be expressed as

$$R_{DS} = R_{DS\_25C} + k(T_j - 25) \tag{17}$$

where R_{DS_25C} is the resistance at 25 °C, k is the transistor's thermal coefficient and T_j is the junction temperature. [25, p. 315–317] However, the model done in thesis does not take the temperature characteristics into account. Channel resistance can also be modeled on silicon level if the channel dimensions are known. Overall resistance seen between drain and source includes the channel resistance and resistances caused by source and drain regions. The channel resistance is

$$R_{DS} = \frac{L - \Delta L_R}{Z - \Delta Z} \frac{1}{\mu_n C_i (V_G - V_T)} \tag{18}$$

where L is the physical gate length, ΔL_R is the reduction in channel length caused by lateral diffusion of source and drain regions, Z and ΔZ are the same parameters as L and ΔL_R but for channel width. Electron mobility is μ_n, C_i is the gate capacitance caused by the gate insulator, V_G is the gate voltage and V_T is the threshold voltage. [22, p. 338–339] Often the lateral diffusion is neglected and thus the equation simplifies to

$$R_{DS} = \frac{1}{\mu_n C_i \frac{W}{L} (V_{GS} - V_T)} \tag{19}$$

where W is the channel width, L is the channel length, V_{GS} and V_{TH} are gate-source and threshold voltages respectively [24, p. 15].

Gate capacitance is calculated from

$$C_i = \frac{\varepsilon_i}{d} \tag{20}$$

where ε_i is the relative permittivity of the insulator and d is the thickness of the gate insulator. [22, p. 333] Drain-source resistance can be reduced by using larger channels in FETs. Nevertheless, higher channel conductance results in larger gate capacitance thus increasing gate-drive losses. Therefore, selection between the channel resistance and gate capacitance is a trade-off between the two parasitics. [20, p. 24]

Then there are the losses caused by the body diode during deadtime. It is the time when neither of the switching transistors is conducting and the inductor forward biases the low side body diode. The body diode conduction loss can be calculated using equation

$$P_{BD} = V_{DF} f_{sw} (\Delta I_{oV} t_{d1} + \Delta I_{oP} t_{d2}) \tag{21}$$

where V_{DF} is the forward voltage drop of the body diode, ΔI_{oV} is the valley current of load current, ΔI_{oP} is the peak value of the load current. Variables t_{d1} and t_{d2} are deadtimes for rising and falling edges and f_{sw} is the switching frequency. [25, p. 317] The effect of deadtime and body diode conduction on the switch node voltage can be seen in Figure 19.

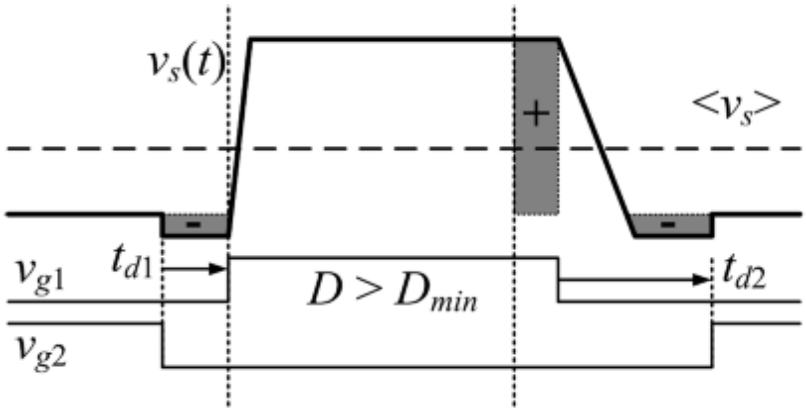

Figure 19. *Switch node voltage and the deadtime voltage drops. Edited from [26, p. 995].*

The voltage drops are the darkened areas marked with minuses in the switch voltage v_s waveform. The area marked with plus is the increase in duty ratio in order to compensate the losses caused by the deadtime. [26, p. 995]

4.2 AC losses

AC power losses are caused by transistor's capacitances. There are multiple different parasitic capacitances due to the overall structure of field-effect transistor as shown previously in Figure 18. Another major parasitic is the common source inductance which increases commutation time significantly.

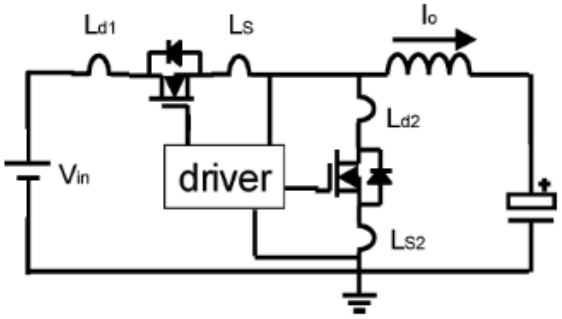

Figure 20. *Parasitic inductances in MOSFETs [25, p. 310].*

This common source inductance is noted as L_s in Figure 20. The inductances may be caused by the self-inductance of the bondwires or from other parasitics. [24, p. 766], [25, p. 310–311]

The most important capacitances for minimizing switching losses are the capacitances between the terminals of the transistor e.g. drain-source, gate-source and gate-drain capacitances. Using piecewise linear approximations, and including the parasitic capacitances mentioned, the switching event becomes more complex. Switching sequence can be divided into different parts as seen from Figure 21.

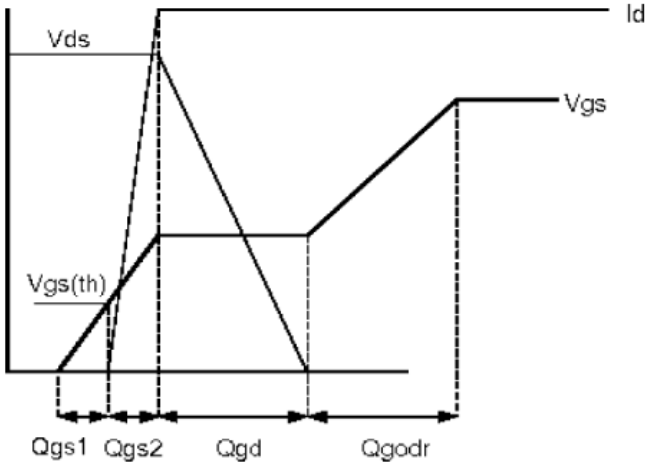

Figure 21. *V_{GS}, V_{DS} and I_D when n-type MOSFET turns on [25, p. 310]*

During the first segment the gate-source capacitance is charging and after the threshold voltage V_T the channel conductivity starts to rise rapidly. Meanwhile the gate side of the

gate-drain capacitance receives the same amount of charge and when the channel resistance starts to fall the drain voltage decreases. Therefore, the drain side of the drain-gate capacitance starts to discharge and the gate current flows through it. So, the gate side of the capacitor is charged, and the drain side is discharged which results in the V_{GS} staying constant. This constant voltage level is also called Miller plateau. [23, p. 703–705]

Basically, a switching loss is caused by the overlap between V_{DS} and I_D and the loss is sometimes referred as hard switching loss. The switching losses can be approximated with equation

$$P_{sw} = \frac{1}{2}\Delta V f_{sw}(I_{valley}t_{rise} + I_{peak}t_{fall}) \tag{22}$$

where ΔV is the voltage change during the switching transition, f_{sw} is the switching frequency, I_{valley} is the inductor valley current, I_{peak} is the peak inductor current and t_{rise} and t_{fall} are the times how long the drain current and drain-source voltage overlap in rise and fall transitions. For example, in Figure 21 the rise time would be the duration of Q_{gs2} and Q_{gd} segments. [27, p. 65]

4.2.1 Reverse recovery

Reverse recovery effect happens when diode is first forward biased and conducting and then reverse biased to block the current. This is caused by the stored charge in the p-n junction of the diode. When the bias changes from forward to reverse bias the junction remains forward biased because the stored charge cannot discharge instantaneously. Therefore, the current must flow to the reverse direction until the stored charge is depleted. The time how long it takes for the stored charge to deplete depends on the diode and can be a major factor when designing switching circuits. It is desirable to have the lowest possible reverse recovery time to minimize the losses caused by the reverse recovery. [22, p 232–234]

In a synchronous buck converter, reverse recovery happens when the conducting low side body diode is reverse biased by turning on the high side MOSFET. The reverse recovery current then flows through the high side MOSFET. Figure 22 shows approximated effect of reverse recovery current on the high side MOSFET current.

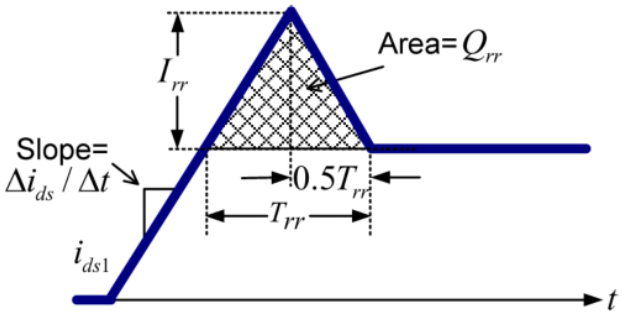

Figure 22. *HS current waveform during reverse recovery turn-on [23, p. 712].*

The losses caused by the reverse recovery can be approximated from the turn-on waveform. The area of the current waveform overshoot is the charge that must be removed from the low side body diode. The approximation states that the area can be approximated with a triangle and thus the reverse recovery charge is

$$Q_{rr} = \frac{1}{2} I_{rr} T_{rr} \tag{23}$$

where the I_{rr} is the maximum of the additional current added by the reverse recovery and T_{rr} is the time it takes to remove the excess charge from the body diode, see Figure 22 for clarification. Then the reverse recovery loss can be calculated with

$$P_{rr} = Q_{rr} U_R f_{sw} \tag{24}$$

where Q_{rr} is the reverse recovery charge and U_R is the reverse voltage. [28, p. 364]

The power losses caused by reverse recovery effect are minimized using various switching techniques. Hard switching is the normal switching condition when MOSFET suffers from power losses caused by the diode reverse recovery and the output capacitance of the transistor. Hard switching causes significant power losses during turn-on transition. One way to mitigate the turn-on switching losses of the high side MOSFET is to use switching technique called zero voltage switching (ZVS). In addition to power losses, reverse recovery currents caused by the body diode may cause voltage ringing which may cause electromagnetic interference and additional power losses. [2, p. 765–767], [21, p. 1510]

4.3 Logic and control losses

Losses caused by control and logic are characterized with quiescent current (I_Q) which is the current the device requires for the basic functionality. In other words, I_Q is the current the device draws from the input when the output current is zero and the power stage is not switching unless stated otherwise. I_Q includes currents consumed by, for example, internal precision reference voltage, oscillators, protection circuitry, state

machine and other logic gates but it does not include the current consumed by the power stage. [29, p. 18]

4.3.1 Gate drive

Driver losses are closely coupled with the MOSFET AC losses. Due to the apparent losses discussed in chapter 4.2 the MOSFET switching instance should be as fast as possible. MOSFETs are charge controlled devices so in other words, the parasitic capacitances should be charged and discharged as quickly as possible to minimize the voltage and current rise and fall times in the MOSFET. Theoretically it is possible to reach switching times of 50 to 200 ps whereas the real switching times are between 10 to 60 ns for discrete and insulated-gate bipolar transistors. [30, p. 6] However, integrated implementations tend to switch faster.

Gate driver efficiency depends on the driven MOSFET and driver circuitry. Driving a higher voltage to the MOSFET results in lower R_{DS} which results in lower conduction losses as discussed previously. On the other hand, the higher gate voltage means that more charge must be supplied to the gate resulting in slower switching and therefore higher switching losses. [31, p. 1] An example MOSFET driver circuit for a low side MOSFET is shown in Figure 23.

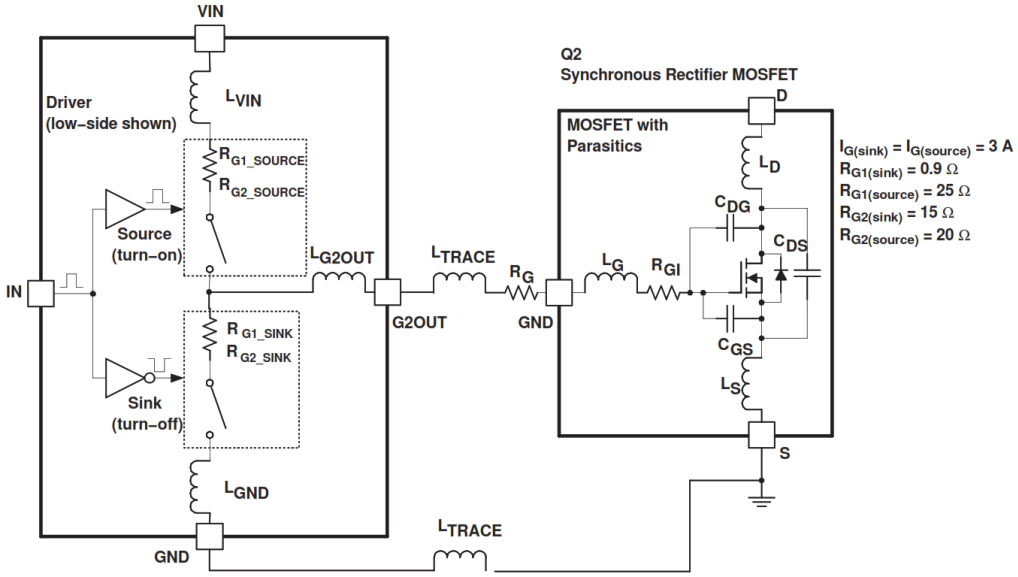

Figure 23. *Conventional low side MOSFET driver and the parasitics [31, p. 6].*

Basically, the lower switch in the push-pull driver is used to discharge the capacitances at the MOSFET gate and the higher turn-on switch is used to charge the capacitances. Gate driver losses mostly depend on the MOSFET gate design, for example, how much charge is needed and to which voltage the gate-source capacitance is charged. Gate driver losses can be calculated with

$$P_g = Q_{GS} V_{GS} f_{sw} \quad (25)$$

where Q_{GS} is the charge supplied to the gate-source capacitance, V_{GS} is the gate-source voltage to which the capacitance will be charged, and f_{sw} is the switching frequency. [32, p. 5140] This energy is completely dissipated into heat during turn-on and turn-off transitions of the MOSFET [33, p. 1005]. As the studied topology has integrated driver and power stage, the data for gate driver losses will be based on simulations in the efficiency model.

When the power stage is made of two n-type MOSFETs, similarly as in Figure 2, a higher voltage than the input voltage is needed to drive the gate. This is because the source of the high side MOSFET is connected to the switching node and when the high side starts to conduct the voltage at the switching node rises to input voltage minus the voltage drop across the high side transistor. The voltage drop across the transistor is as small as possible to minimize conduction losses. This means that if the gate voltage is same as the input voltage, the gate-source voltage V_{GS} is nearly zero which turns off the transistor. Therefore, the high side gate needs higher drive voltage than the input voltage and one way to do this is with a charge pump. Of course, another way to circumvent this is to use a p-type MOSFET (PMOS) as high side switch but for the same channel resistance, a PMOS would need 2.5 times the area of a NMOS transistor even when the charge pump driver area is taken into account [34, p. 1626].

5. EXTERNAL LOSSES

Additional power losses in a buck converter circuit are caused by external losses which include circuit components and printed circuit board parasitics. For inductors the main components for power losses are copper and core losses whereas for capacitors, most of the power loss is caused by the equivalent series resistance. PCB losses are caused by the DC and AC resistance of the PCB traces.

5.1 Inductor losses

Inductors and other magnetic devices have different loss mechanisms which may cause minor or major losses depending on the use case. Common loss mechanics are core loss, copper loss and eddy currents. [2, p. 506–508] According to Erickson and Maksimovic [2, p. 527] proximity losses are negligible and can be ignored as well as core losses depending of the physical size of the inductor. However, the device for which the losses are to be modelled uses physically small inductors and therefore core losses cannot be ignored. In turn, this will reduce skin effect even more due to the small wire diameter [2, p. 510].

5.1.1 Copper loss

DC loss, also known as low-frequency copper loss or DCR, is the simplest of the inductor loss mechanics. It is caused by the resistance of the inductor windings. Copper loss is modelled as an equivalent series resistance for the inductor. Copper loss can be calculated using equation

$$P_{DC} = I_{RMS}^2 R_{DCR}, \tag{26}$$

where I_{RMS} is the root mean square (RMS) value of the inductor current. Resistance can be calculated from the resistivity and the physical dimensions of the inductor windings by using equation

$$R = \rho \frac{l}{A}, \tag{27}$$

where l is the winding length, A is the cross-sectional area of the winding and ρ is the resistivity of used material. [2, p. 508] However, usually component manufacturers give the DC resistance directly in their datasheets and even if the data is not available the DC resistance is trivial to measure.

5.1.2 Core loss

Core loss is the energy lost from magnetization of the core as all the energy used to change the magnetization is not recoverable. These power losses can be divided into hysteresis, eddy current and residual losses. Hysteresis losses are common in frequency range between 10 kHz to 10 MHz with powdered materials whereas eddy current losses are dominant in low frequency, under 10 kHz, devices. The losses caused by hysteresis can be calculated using equation

$$P_H = f A_c l_m \int_0^T H \, dB, \tag{28}$$

where f is frequency, A_c is the area of the core, l_m is the length of the core, H is the magnetic field and B is the flux density. The integral is the area of the B-H loop. The area of the hysteresis loop does not depend on frequency resulting in hysteresis losses being directly proportional of switching frequency. [2, p. 506], [35, p. 398]

Core materials are often conductive materials and the magnetic field passing through the core causes eddy currents inside the core. The resulting eddy currents cause power losses in the core because of the resistance of the core material. Therefore, it is important to choose the core material which is suitable to the application. Usually the trade-off is between saturation flux density and core loss. High saturation flux densities result in smaller physical dimensions but higher core losses. [2, p. 506–507]

Total core loss can be calculated using empirical equation

$$P_{fe} = K_{fe}(\Delta B)^{\beta} A_c l_m \tag{29}$$

where K_{fe} and β are selected to fit the inductor manufacturer's measurement data. Typical value for β is between 2.6 and 2.8. ∆B is the peak AC flux density. [2, p. 506–507] Equation 29 can be further developed to take the switching frequency into account and thus the equation takes form of

$$P_{fe} = k f^{\alpha} B_m^{\beta} \tag{30}$$

where k, α and β are material specific parameters, f is frequency and B_m is the amplitude of magnetic flux. Equation 30 is also known as Steinmetz's equation. The equation is widely used in DCDC converter analysis, but it was originally developed for sinusoidal waveforms. Therefore, further developments of this equation have been taken place. [36, p. 129]

Based on analysis done by Górecki and Detka the differences between different models are even up to 80 % and the classical Steinmetz equation underestimates losses by approximately 10 %. According to their analysis the most accurate model for core losses is

$$P_v = P_{v0} f^{\alpha} B_m^{\beta} (2\pi)^{\alpha} (1 + \alpha_p (T_R - T_m)^2)(0.6336 - 0.1892 \ln(\alpha)) \quad (31)$$

where α_p is the ferromagnetic material's temperature coefficient for losses. T_R is the core temperature and T_m is the temperature where losses occur the least. One major problem in other core loss models is that the temperature dependence of material parameters P_{v0}, α and β is often overlooked. Proposed expression for P_{v0} is

$$P_{v0} = a e^{-\frac{f+f_0}{a_3}} + a_1 (T_R - T_m) + a_2 e^{-\frac{f+f_2}{f_1}} \quad (32)$$

where a and f variables are material parameters. Parameter β takes form of

$$\beta = \begin{cases} 2\left(1 - e^{-\frac{T_R}{\alpha_T}}\right) + 1.5 \textbf{ IF } 1 - e^{-\frac{T_R}{\alpha_T}} > 0 \\ 1.5 \textbf{ IF } 1 - e^{-\frac{T_R}{\alpha_T}} < 0 \end{cases} \quad (33)$$

where α_T is material constant. [35, p. 399], [36, p. 130–132]

As can be seen, the theory behind the inductor core losses is very complex and in practice these equations shown earlier are not that practical in the modeling perspective. It requires a lot of measurement data to be available or a large catalog of different measurement instruments. For this efficiency model and inductor power loss modeling, magnetic field measurement equipment was not available. In addition, the inductors used for the efficiency measurements are not yet released and therefore the datasheets are quite limited and do not provide data for Steinmetz equation. Hence, it is necessary to find an alternative and practical solution to model inductor losses. Losses can be measured by simply measuring the voltage across the inductor and the current flowing through the inductor. The power loss is the instantaneous product of the measured voltage and current. Measured AC losses can then be modeled with inductance and resistance (L-R) ladder which effectively introduces frequency dependent resistance to the circuit [37]. The losses can then be calculated with following equation

$$P_L = I_{DC}^2 R_{DC} + I_{AC,RMS}^2 R_{AC} \quad (34)$$

where I_{DC} is the DC current, R_{DC} the DC resistance of the inductor, $I_{AC,RMS}$ inductor AC current RMS value and R_{AC} the AC resistance [38, p. 2184].

5.2 Capacitor losses

Power loss of the capacitor is caused by the equivalent series resistance of the capacitor. The loss can be calculated from equation

$$P_{cap} = I_{C,RMS}^2 R_{ESR} \quad (35)$$

where $I_{C,RMS}$ is the RMS value of the capacitor current and R_{ESR} is capacitor equivalent series resistance. [1, p. 574] Capacitors also have a small amount of leakage current caused by the parasitic parallel resistor. However, this current is generally small enough

to be neglected completely and therefore it is neglected from the implemented efficiency model. Even the losses caused by the ESR are very small due to the small output current ripple.

5.3 Printed circuit board losses

The used PCB causes power losses in both the output and the input side of the switching regulator. Mostly the power losses are caused by the PCB resistance and it can be somewhat circumvented with phase shedding and adding depending of the current load condition. [6, p. 1025], [7, p. 2224] However, inductance becomes the more and more dominant factor for PCB impedance when the frequencies begin to rise.

Inductance of a microstrip PCB trace can be calculated using equation

$$L = 5.071 \ln\left(\frac{5.98h}{0.8w + t}\right) \tag{36}$$

where h is the height difference between the trace and ground plane, w is the width of the trace and t is the thickness of the trace. The unit of the result of equation 36 is nanohenries per inch. [17, p. 211] Inductance itself does not cause power losses but the voltage swings caused by the combination of inductance and current transients can slow down transistor turn-on and turn-off. This slowdown increases switching power losses as equation 22 defines the relation between the switching power loss and rise and fall times of the MOSFETs.

DC resistance of a rectangular conductor with width of w and thickness of t can be calculated with

$$R_{DC} = \frac{\rho}{wt} \tag{37}$$

where ρ is the resistivity of the conductor. Current will be uniformly distributed over the cross section of the conductor. High frequency current is concentrated on the outer edges of the conductor which results in AC current experiencing higher resistance compared to DC current. The effect is illustrated in Figure 24.

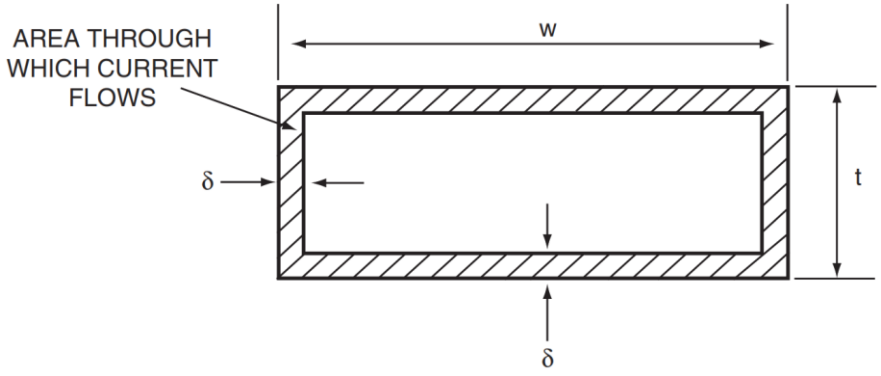

Figure 24. *AC current in a rectangular conductor [17, p. 213]*

This phenomenon is called skin effect. Because of the smaller conducting area in the trace the AC resistance is calculated with a different equation

$$R_{AC} = \frac{\rho}{2(w+t)\delta} \tag{38}$$

where δ is the skin depth of the material. For copper the skin depth can be calculated using equation

$$\delta_{copper} = \frac{66 \cdot 10^{-6}}{\sqrt{f}} \tag{39}$$

and when equation 39 is substituted to equation 38 results in

$$R_{AC} = \frac{131\sqrt{f}}{w+t} \tag{40}$$

where frequency is in megahertz. However, these AC resistance equations assume that the conductor is an isolated straight trace. Multiple conducting conductors results in the current concentrating on one side of another nearby conductor. This results in higher resistance due to the higher current density. [17, p. 213–214]

6. MEASUREMENTS

For the inductor power loss model, some measurements were done in the laboratory. DC resistance was measured with a basic four-terminal measurement setup with an additional verification measurement for the test current. Four-terminal measurement compensates the losses happening in the measurement device wires providing accurate measurement results even with low resistances. Inductor AC losses were measured with an automated LabVIEW measurement setup which was developed for this thesis.

6.1 Inductor AC losses

Inductor losses were measured with Tektronix DPO4054B oscilloscope using Tektronix P6247 differential voltage probe with 1:10 attenuation and TCP0030 current probe with 5 A range. All the used measurement probes were deskewed to minimize the effect of different propagation delays between the probes. Output current was varied with Keithley 2420 SourceMeter which was used as a current sink in a four-wire mode which allowed for the output voltage to be measured with the same device. Input voltage was measured using Agilent 34401A from point as close as possible to the TPS6594x-Q1 on the PCB and the input current reading was saved from the Aim-TTi QL355TP power supply. Current for the inductor was supplied with TPS6594x-Q1 evaluation module (EVM) which was powered with Aim-TTi QL355TP. The buck used for the measurements was BUCK1 on the EVM. TPS6594x-Q1 was controlled with Texas Instruments USB2ANY via I2C.

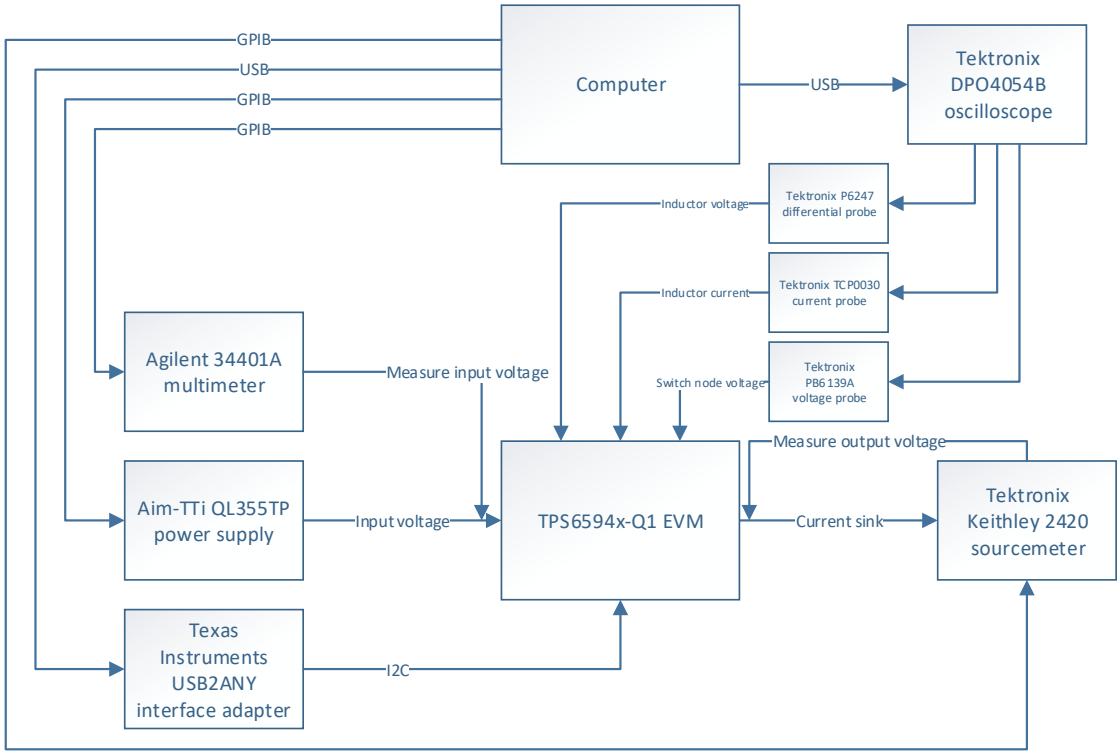

Figure 25. *Block diagram of the measurement setup.*

The sequence was made with LabVIEW 2016 and ready-made drivers were used for measurement instruments. Instruments were connected to a computer via universal serial bus (USB) and general purpose interface bus (GPIB). Figure 25 shows a block diagram which summarizes how the different measurement instruments were connected. The real measurement setup is shown in Figure 26.

Two different inductors were tested because TPS6594x-Q1 has multiple different configurations each with different inductor. The inductors tested were TFM322512ALMAR47MTAA and TFM322512ALMAR22MTAA which, at the time of writing, are yet to be released. For the measurements, the inductor was soldered to the PCB only from one contact and a wire was soldered to the second end of the component. Second end of the wire was soldered to the PCB and a current probe was applied around the soldered wire. A small pin header was soldered to the inductor contacts for the inductor voltage measurement. The measurement setup is shown in Figure 26.

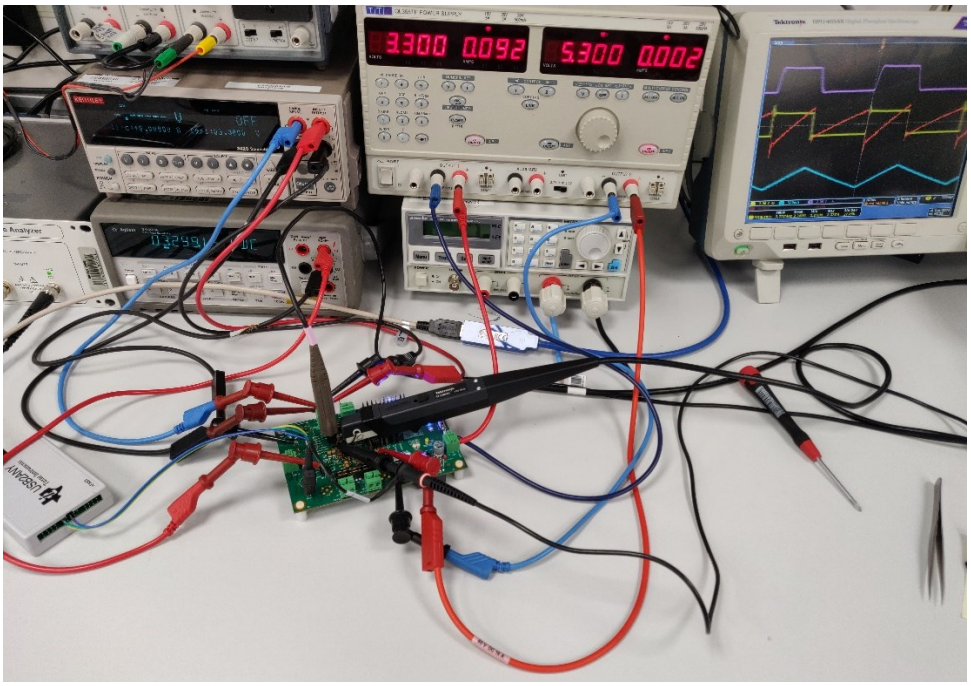

Figure 26. *Measurement setup.*

The measurement setup was extremely vulnerable to physical damage due to the way the inductor had to be soldered on the PCB. Attaching the current probe to the soldered wire between the inductor and PCB pad worked as a lever and easily cracked either the PCB pad or the contact from the inductor. Therefore, extra precautions had to be taken when working with the measurement setup.

Measurement sequence was automated with LabVIEW. To combat the inductor temperature changes caused by the load current, the load pulse duration was attempted to be kept at minimum. The buck was loaded for less than a second, just enough for the measurement instruments to do the required number of integration cycles. After every measurement, the load current and the buck were turned off to let the inductor cool for 14 seconds. During this time the oscilloscope's differential probe and current probe were autozeroed and degaussed in order to avoid measurement error and especially the magnetization of the current probe. The front panel of the LabVIEW sequence is shown in Figure 27.

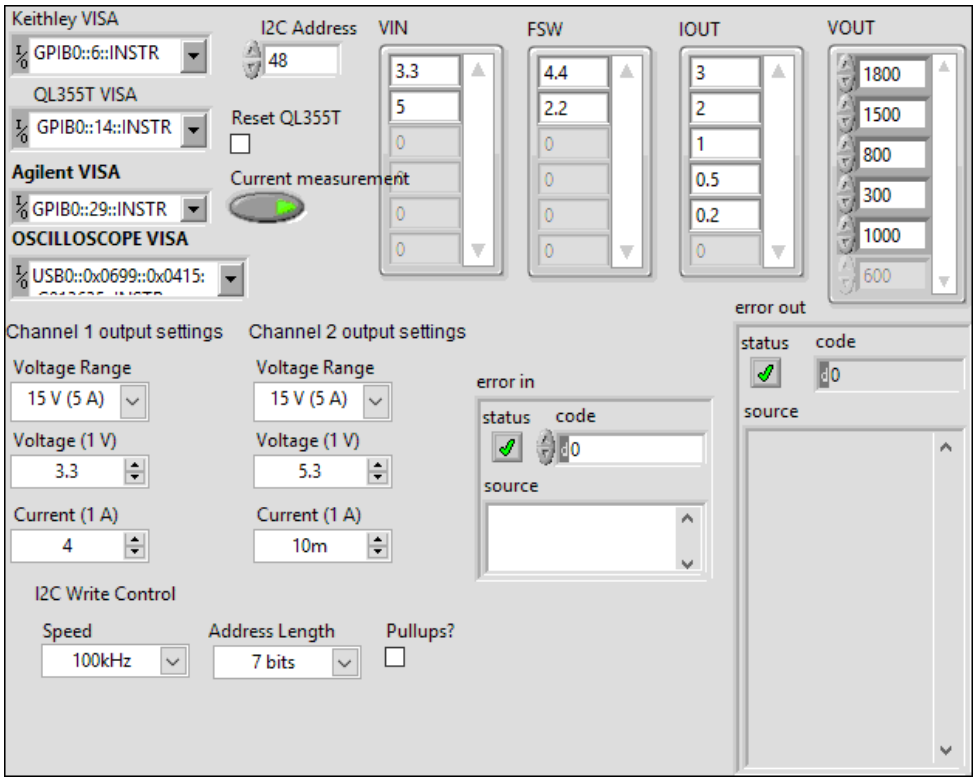

Figure 27. *Front panel of the LabVIEW sequence.*

The actual implementation is shown in Appendix A: LabVIEW sequence top view. Basically, the sequence consisted of four nested for-loops which each iterated through one of the measurement parameters which were input voltage, switching frequency, output current and output voltage.

The measurements done for the inductor were as comprehensive as possible and covered wide range of input and output voltages as well as different switching frequencies. The values were chosen to match the most common use cases. The measurement matrix is shown in Table 2.

Table 2. *Inductor loss measurement matrix.*

Inductance (nH)	V_{IN} (V)	V_{OUT} (V)	Switching frequency (MHz)	Load current (A)
220	3.3 & 5.0	0.30	2.2	0.2
		0.80		0.5
		1.00		1
		1.5		2
		1.8		3
470	3.3 & 5.0	0.30	4.4	0.2
		0.80		0.5
		1.00		1
		1.5		2
		1.8		3

All in all, 100 different configurations were measured totaling 50 measurements per inductor with two different input voltages, five different output voltages and five different load currents. The data that was saved from the measurement included the inductor voltage, inductor current, switch node voltage and the inductor power loss calculated with the math function of the oscilloscope. Other devices provided input voltage, output voltage and input current reading which were also saved into the same measurement file. Save format for the measurement data was a comma-separated value (CSV) file that included all 100 000 datapoints for each waveform.

A Matlab script was made to automatically parse all the measurement data files to a more useful form. The script calculated switching frequencies using fast Fourier transform for both the inductor current and the inductor voltage waveforms as well as average, RMS and peak-to-peak inductor current values. The peak-to-peak value was determined as an average difference between 1000 maximum and minimum points. The script also calculated other useful data such as duty ratio from the inductor voltage, mean as well as RMS power losses and calculated inductance based on the slope of the inductor current.

Firstly, the obvious outliers in the data had to be filtered out. First outliers were filtered based on the fundamental frequency calculated from the inductor voltage and current waveforms and fundamental frequencies with higher than 30 % difference were filtered from the results. Rest of the outliers were filtered based on duty ratio stability. If the difference between highest and lowest measured duty ratio was higher than 5 %, the result was deemed to be unstable.

Power loss was the mean value of the saved math waveform. Measured power losses of the 220 nH inductor at 4.4 MHz switching frequency are shown in Figure 28. Graphs are clearly split into two distinct groups by the input voltages at least with high inductor currents.

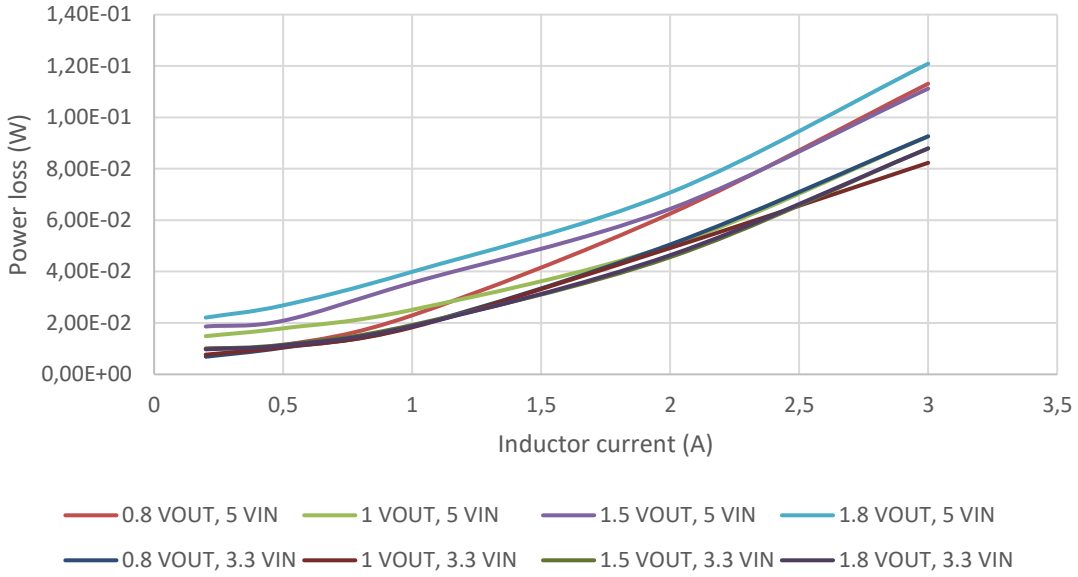

Figure 28. *220 nH inductor power losses at 4.4 MHz switching frequency.*

And similarly, the power losses of the 470 nH inductor at 2.2 MHz switching frequency are shown in Figure 29. The division into two separate groups is more noticeable in the results of the 470 nH inductor.

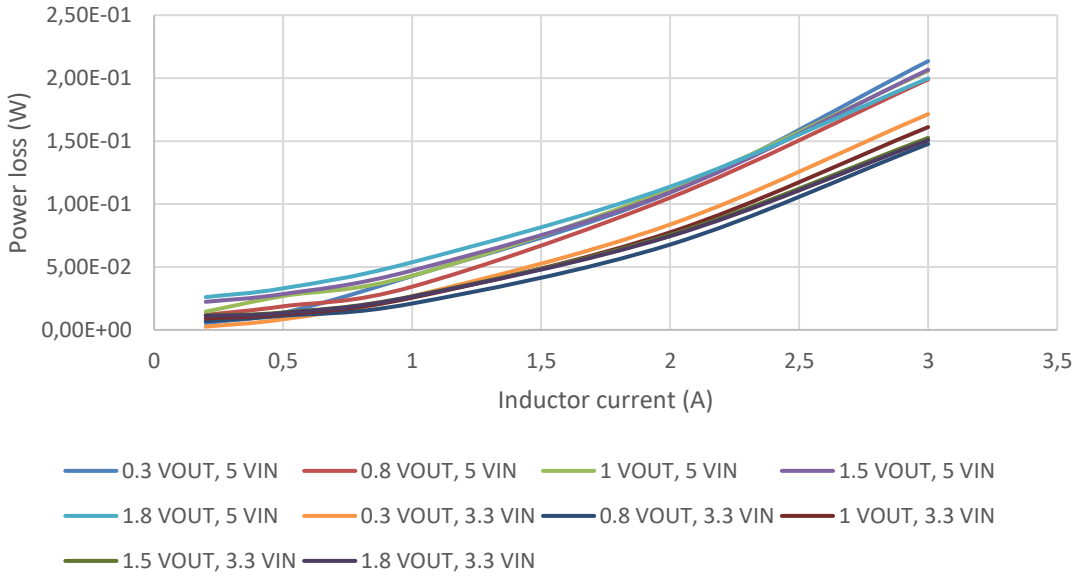

Figure 29. *470 nH inductor power losses at 2.2 MHz switching frequency.*

Overall the 470 nH inductor suffers from higher power losses and this is most likely caused by the higher DCR. However, power losses for both inductors seemed quite high

and a reference comparison would be beneficial. Therefore a few different inductor power loss calculators were chosen for a comparison.

Measured results were compared against similar other inductors from manufacturers who provide power loss calculators such as Murata, TDK as well as Wurth Electronics. All the comparisons were done using 1 V output voltage and 3.3 V as well 5 V input voltages. Compared inductors are shown in Table 3.

Table 3. *Compared inductors and power loss calculators [39-41].*

Calculator	Part number	DCR (mΩ)	Inductance (nH)
Murata [39]	FDSD0412-H-R47M	19	470
	FDSD0415-H-R22M	11	220
TDK [40]	TFM252012ALMAR47MTAA	19	470
	TFM252012ALMAR22MTAA	8	220
Wurth [41]	744373210047	18	470
	744373210022	6.6	220

Calculator parameters such as voltage loss over switching transistors were set to match the measurement setup. The comparisons of 220 nH inductors and 470 nH inductors were done separately. The comparison graph for the 220 nH inductors is in Figure 30.

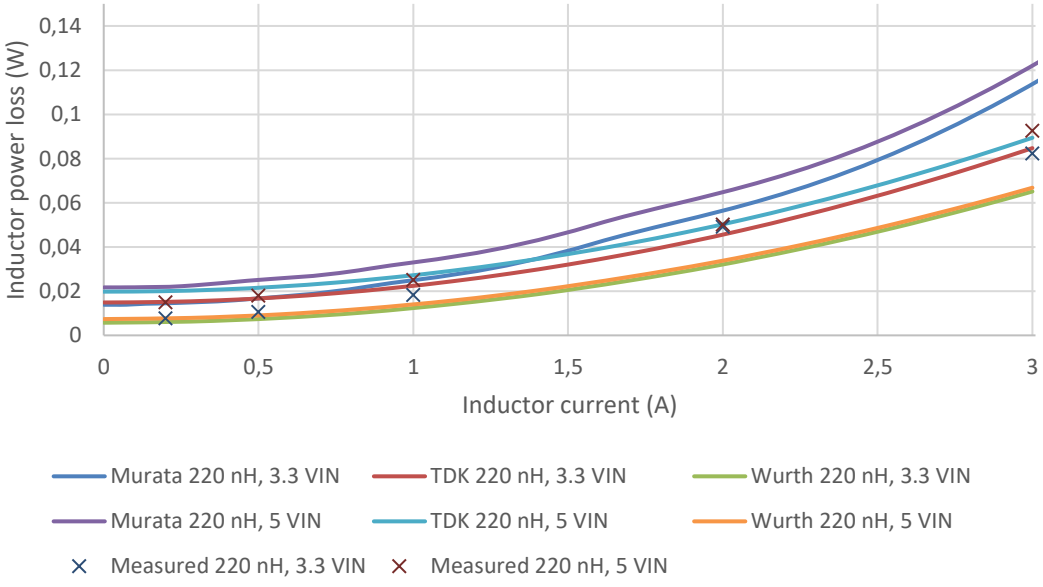

Figure 30. *Measured power losses of 220 nH inductor compared to different power loss calculators. Results for Murata, TDK and Wurth from sources [40-42].*

Measurements with 5 V input voltage gave slightly higher power losses. Overall the measured power losses align quite well with the different power loss calculators. Same comparison is done for the 470 nH inductor measurement results in Figure 31.

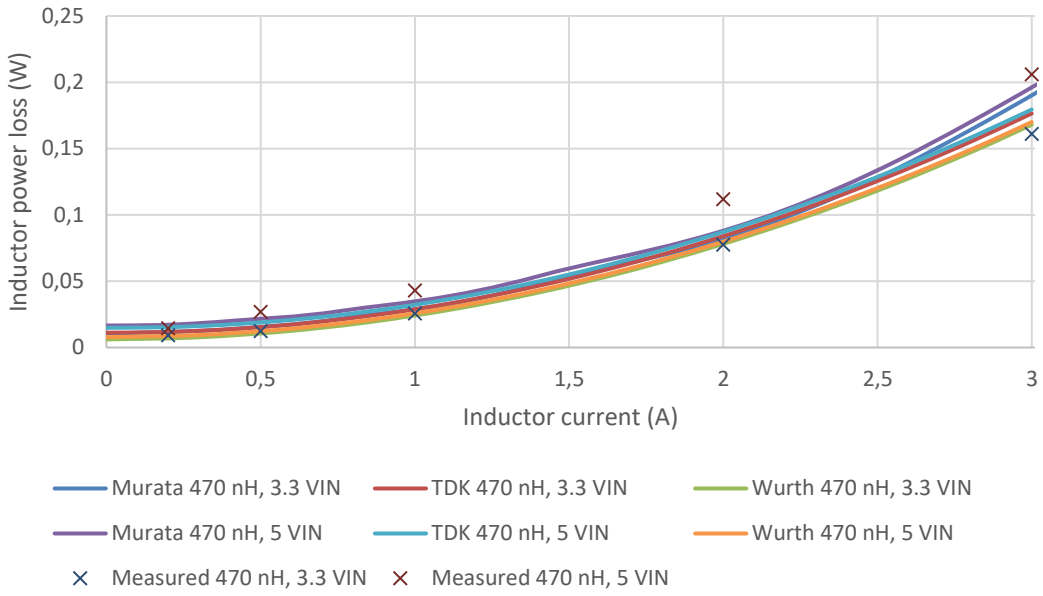

Figure 31. *Measured power losses of 470 nH inductor compared to different power loss calculators. Results for Murata, TDK and Wurth from sources [40-42].*

Measurements done with 5 V input voltage had higher power losses than expected with 470 nH inductor as well. This seems to be caused by the inaccuracy of the oscilloscope as the vertical range setting for inductor voltage measurement had a large impact on the average power loss. Also, 3.3 V and 5 V measurements had to be done with different vertical range for the inductor voltage measurement due to the differences in voltage swing across the inductor.

The used oscilloscope had a 8-bit analog to digital converter (ADC) [43]. However, the measurements used acquisition mode of 16 averages which improved vertical resolution to 10 bits [44, p. 10]. Vertical range used for 5 V input voltage measurements was 730 mV/div which results in full range of 7.3 V. Quantization error for this range with 10-bit vertical resolution is 7.13 mV. Comparing this to the 430 mV/div with full range of 4.3 V, which was used for 3.3 V input voltage measurements, had quantization error of 4.2 mV. If the measurements were done using the same 730 mV/div range for all measurements the power losses with 3.3 V input were nearly identical compared to results with 5 V input voltage.

In addition, ±1.5 % DC gain accuracy introduces additional error [43]. For example, with 5 V input voltage and 1 V output voltage the inductor voltage swing is from 4 V to -1 V which results in ±60 mV DC gain error during on-time and ±15 mV error during off-

time. Combination of quantization error and DC gain error result in ±201.3 mW and ±66.4 mW errors during on- and off-times with 3 A load current respectively. Duty ratio weighted mean error is then ±48.1 mW when duty ratio is the measured 22.15 %. This fits with the error observed in the measurements assuming the measured power loss with 3.3 V input voltage is correct.

6.2 Inductor DC losses

Inductor's DC resistance was measured using Keithley 2420 SourceMeter in a four-wire measurement mode. Voltage sense wires were soldered directly on the inductor while the test current connectors were connected using regular connector clamps as shown in Figure 32.

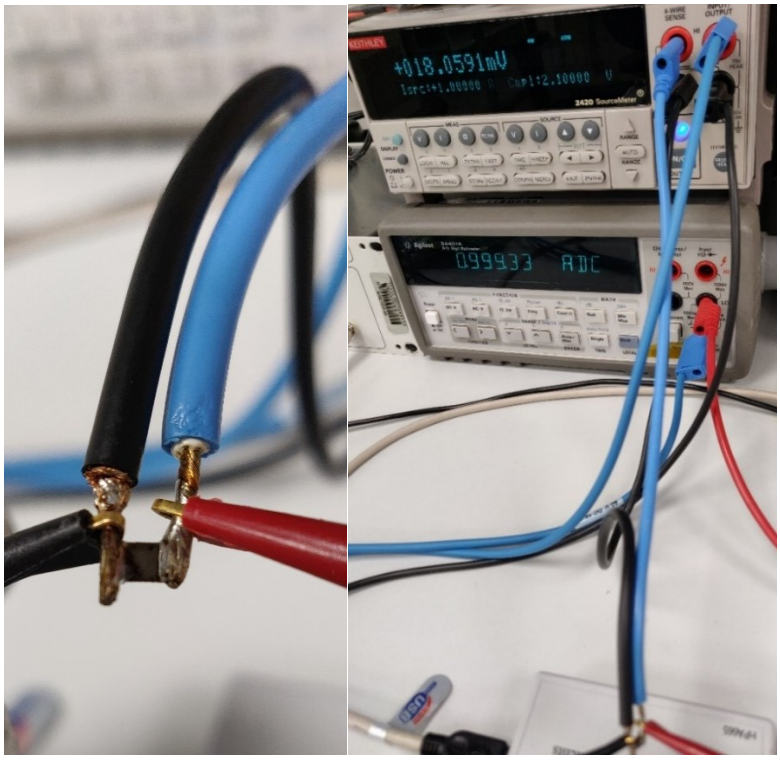

Figure 32. *Connections to the inductor for DCR measurement.*

Test current was measured and verified with Agilent 34401A multimeter and the current supplied by the Keithley 2420 SourceMeter was found to be accurate. Measurements were done with five different test currents and Keithley 2420 was configured to use the high accuracy mode for the measurements. The time duration how long the test current was applied to the inductor was minimized to keep the inductor as close as possible to the room temperature.

According to the datasheet the DC resistance for TFM322512ALMAR22MTAA is typically 6 mΩ and the typical DC resistance for TFM322512ALMAR47MTAA is 16 mΩ

[45]. DC resistance was measured from two different samples of the same inductor type. Results for the 470 nH inductor are shown in Figure 33.

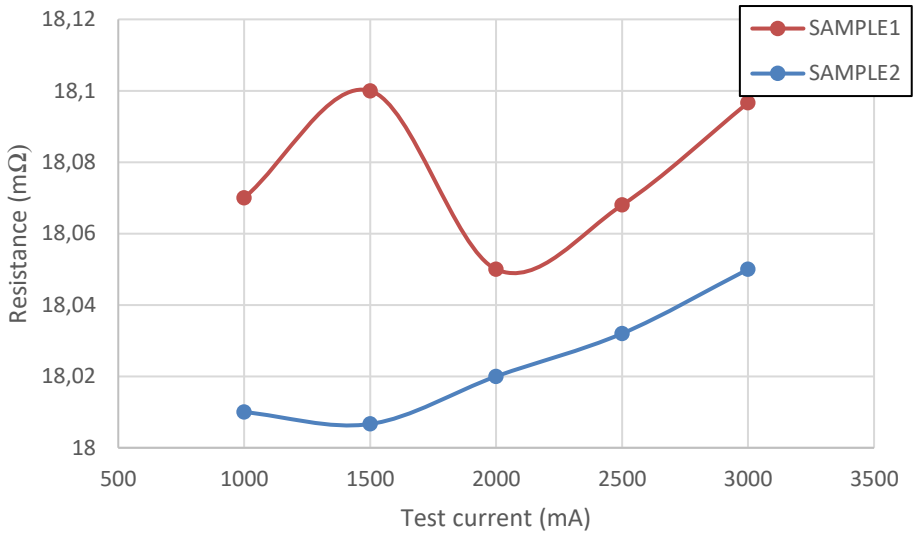

Figure 33. *DC resistance measurement results for two different samples of the same TFM322512ALMAR47MTAA inductor.*

Average DC resistance of the two samples in Figure 33 was 18.05 mΩ. Increase in the resistance as a function of test current is most likely caused by the inductor heating up. The measurements were done for two 220 nH inductors as well and the results for those inductors are shown in Figure 34.

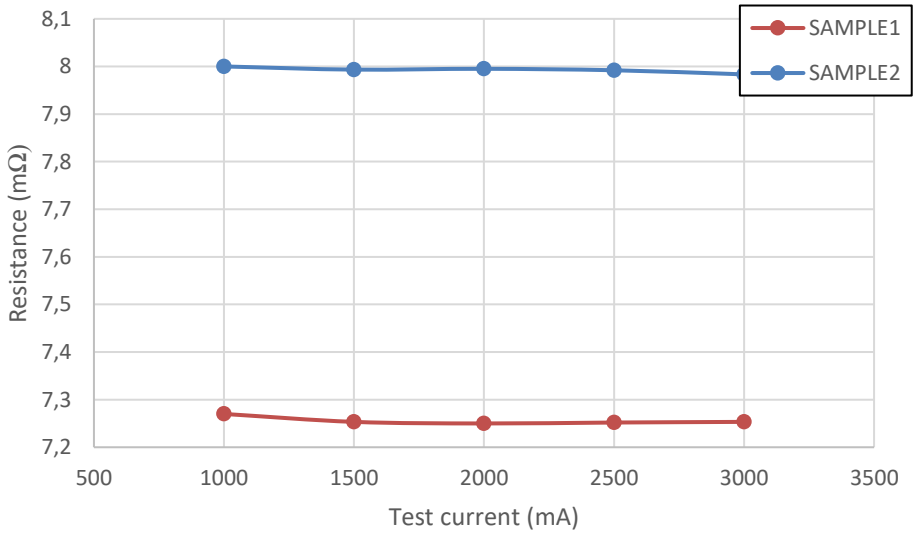

Figure 34. *DC resistance measurement results for two different samples of TFM322512ALMAR22MTAA inductor.*

The average DC resistance of the 220 nH inductor was 7.62 mΩ. All inductors had a slightly higher DC resistance than the typical value defined in the datasheet.

7. SIMULATION MODEL

When making the simulation model for efficiency, two different aspects of the model must be considered in every situation. The obvious one is the simulation accuracy. How accurately the simulation model depicts the different loss elements, is there any approximations and so on. The second aspect that must be considered is the simulation speed which is inversely proportional to the simulation accuracy as higher accuracy usually means longer simulation times. Therefore, the model is always a compromise between these two aspects.

The starting point for the model was the model used for transient simulations which had nearly ideal power MOSFETs with ideal gate drivers with deadtime control. The only MOSFET loss that was modeled was the channel resistance R_{DS}. Output loop PCB losses were approximated with a level 1 inductor and capacitor equivalent series resistances were implemented with level 2 capacitors. DCR of the inductor was also present in the basic model but AC losses were not implemented.

Power loss equations are summarized in Table 4 to recall what parameters affect the power losses in each loss component. The table also shows the reference to which each power loss was compared against in the SIMPLIS model.

Table 4. *Power loss equations*

Loss	Equation	Reference
HS conduction	$\left(I_o^2 + \frac{\Delta I_o^2}{12}\right) D R_{DSHS}$	Cadence Spectre simulations
LS conduction	$\left(I_o^2 + \frac{\Delta I_o^2}{12}\right) (1-D) R_{DSLS}$	Cadence Spectre simulations
Body diode	$V_{DF} f_{sw} (\Delta I_{oV} t_{d1} + \Delta I_{oP} t_{d2})$	Cadence Spectre simulations, Measurements
HS switching	$\frac{1}{2} \Delta V f_{sw} (I_{valley} t_{rise} + I_{peak} t_{fall})$	Cadence Spectre simulations
LS switching	$\frac{1}{2} \Delta V f_{sw} (I_{valley} t_{rise} + I_{peak} t_{fall})$	Cadence Spectre simulations
Logic	$I_Q V_{IN}$	Specification
Capacitor	$I_{C,RMS}^2 R_{ESR}$	Datasheet
Inductor	$I_{DC}^2 R_{DC} + I_{AC,RMS}^2 R_{AC}$	Datasheet, Measurements
PCB		Ansys Q3D SPICE extraction

Reverse recovery was not modeled as the losses caused by it were expected to be negligible due to the device being a synchronous buck converter and the switching period being short. First step in the modeling process was to improve the power stage MOSFETs.

7.1 MOSFETs

The idea was to use a MOSFET part provided by SIMPLIS. Then the PARAM_VALUES property would be parameterized and set to following.

```
USE_EXTRACTED=0 DEVICE='FET' LABEL='FET' VD_PEAK=10 VGSON=2.5 ID_PEAK=10
TEMP=25 LEVEL=3 LIMIT_MAX_ROFF=1 MAX_ROFF=1G HYSTWD=100m ROFF=10Meg
RG={RG} RDSON={RDSON} CDG_NSEG={cdgSeg} VCDG0={vdg0} VCDG1={vdg1}
VCDG2={vdg2} VCDG3={vdg3} QCDG0={qdg0} QCDG1={qdg1} QCDG2={qdg2}
QCDG3={qdg3} GAIN_NSEG={gainSeg} VT0={vt0} VGS2={gainvgs2}
VGS3={gainvgs3} VGS4={gainvgs3} ID2={id2} ID3={id3} ID3={id4}
CDS_NSEG={cdsSeg} VCDS0={vds0} VCDS1={vds1} VCDS2={vds2} VCDS3={vds3}
VCDS4={vds4} QCDS0={qds0} QCDS1={qds1} QCDS2={qds2} QCDS3={qds3}
QCDS4={qds4} BD_NSEG={bdSeg} VD0={vd0} VD1={vd1} VD2={vd2} VD3={vd3}
VD4={vd4} IBD0={ibd0} IBD1={ibd1} IBD2={ibd2} IBD3={ibd3} IBD4={ibd4}
CGS_NSEG={cgsSeg} VCGS0={vgs0} VCGS1={vgs1} VCGS2={vgs2} VCGS3={vgs3}
VCGS4={vgs4} QCGS0={qgs0} QCGS1={qgs1} QCGS2={qgs2} QCGS3={qgs3}
QCGS4={qgs4}
```

Program 2. *Parameterized PARAM_VALUES property.*

The value enclosed in curly brackets are parameterized variables. Then the MOSFET circuit would ideally be as simple as one FET symbol. The parameterized parameters could be set from the custom dialog which is defined in the symbol definition of the subcircuit. The custom dialog is shown in Figure 35.

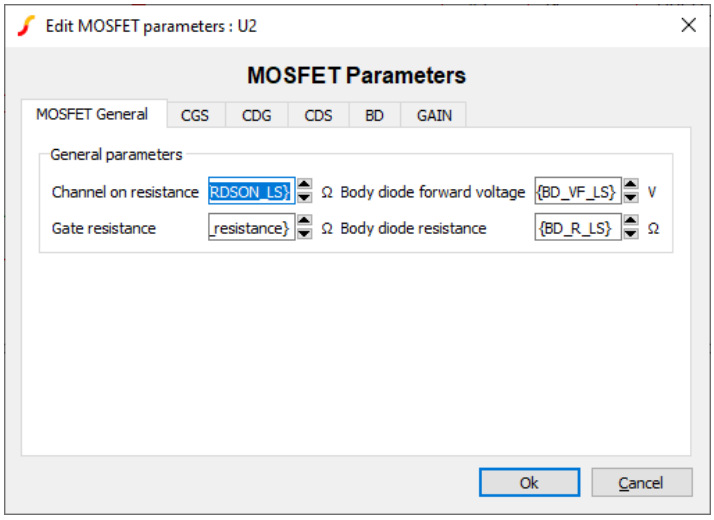

Figure 35. *The custom configuration dialog of the initial MOSFET model.*

Then the parameters in the custom dialog can be parameterized further. This mean that the dialog menu parameters could be set programmatically for example with design verification module (DVM).

However, the idea of using SIMPLIS provided MOSFET part with PARAM_VALUES property did not work. The issue was with the POP analysis since it would never converge when using the implemented MOSFET part. The convergence percentages

were never below 1E-4 percent so according to the analysis the circuit was nowhere near steady state. The convergence percentages are shown on the left in Figure 36.

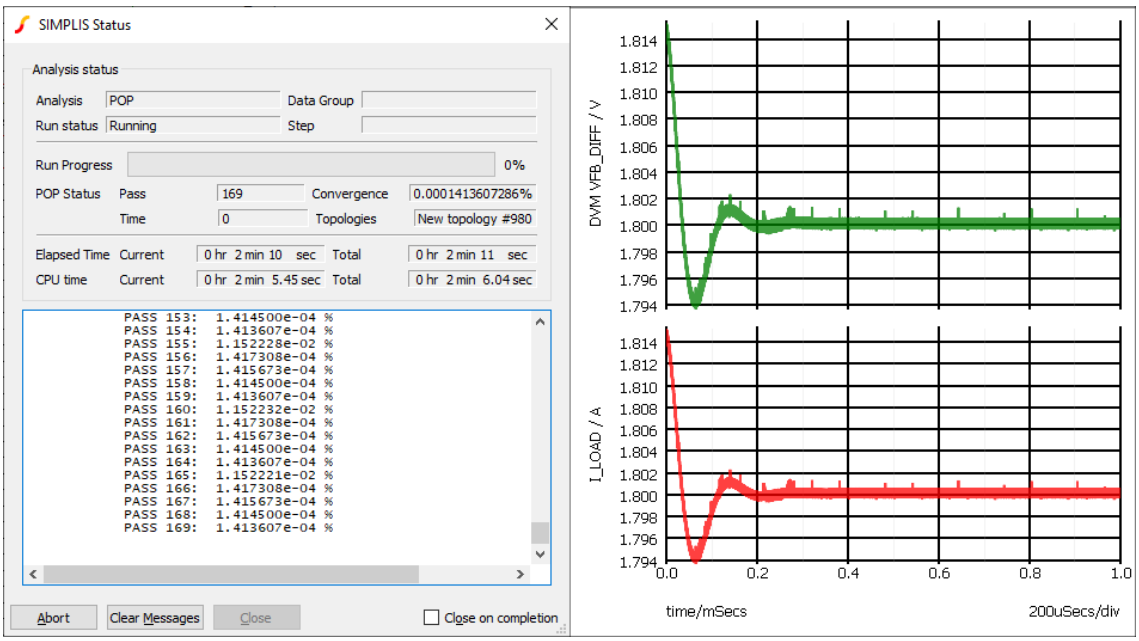

Figure 36. *Convergence issue (left) but steady state is reached in transient analysis (right).*

Normally the convergence percentage should be below 1E-8 but this can be reconfigured as was discussed in chapter 3.1. Nonetheless, if simulating the circuit with just the transient analysis it was seen that the circuit would reach a steady state after around 300-500 µs, so clearly something was wrong with the POP analysis. This issue was circumvented by using the level 2 equivalent circuit which was shown in Figure 17 and even some further simplifications were made.

7.1.1 Parasitic capacitances

MOSFET capacitances were simulated with Cadence using a testbench shown in Figure 37. The testbench simulates gate charge Q_g, gate-drain charge Q_{gd} and output charge Q_{oss} by integrating the gate and drain currents.

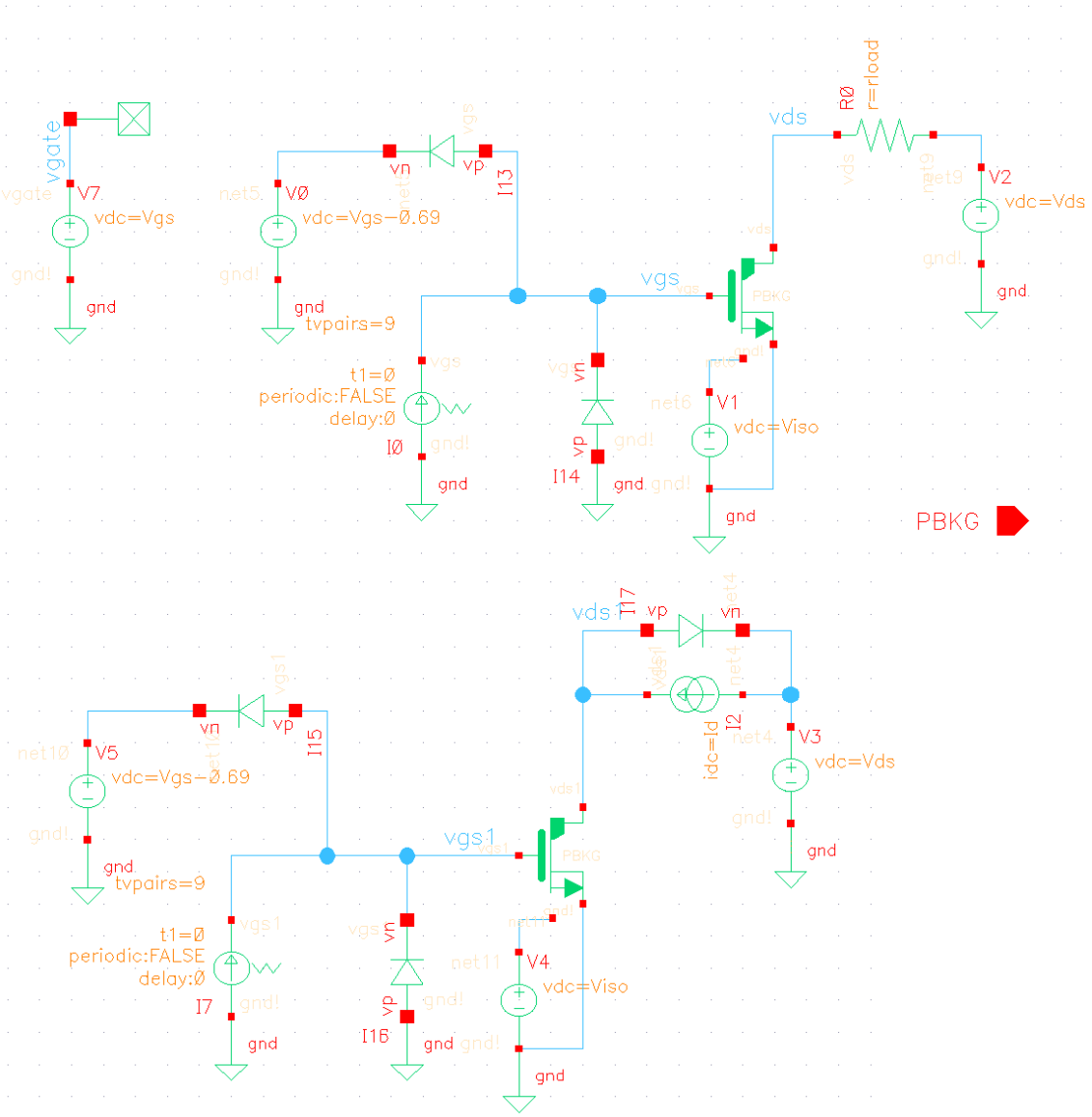

Figure 37. *MOSFET capacitance extraction testbench.*

Gate and output charge simulations where straightforward as the gate charge was an integration of the gate current during a turn-on transition and the output charge was simulated by integrating the drain current during the MOSFET turn-off transition. Gate-drain capacitance was an integration of the gate current and the integration limits were from time instance when V_{DS} falls to 90 % of the initial value to time instance when V_{DS} is 10 % percent of the initial value. Basically, this is the Miller plateau which was also shown in Figure 21.

Cadence testbench did not give the results as is because there were discontinuities in the charge curves acquired from the simulator. Particularly the gate-drain charge curve had a large gap near the threshold voltage and was completely flat after that which was not expected. The curves were parsed by assuming that the gate-source capacitance and consequently the charge-voltage curve would be quite linear at least compared to

other charge curves. Gate-source charge curve would then be a linear part of the first segment of gate charge curve before threshold voltage because as shown in Figure 21 the gate-source capacitance is the first to charge. This is clarified in Figure 38.

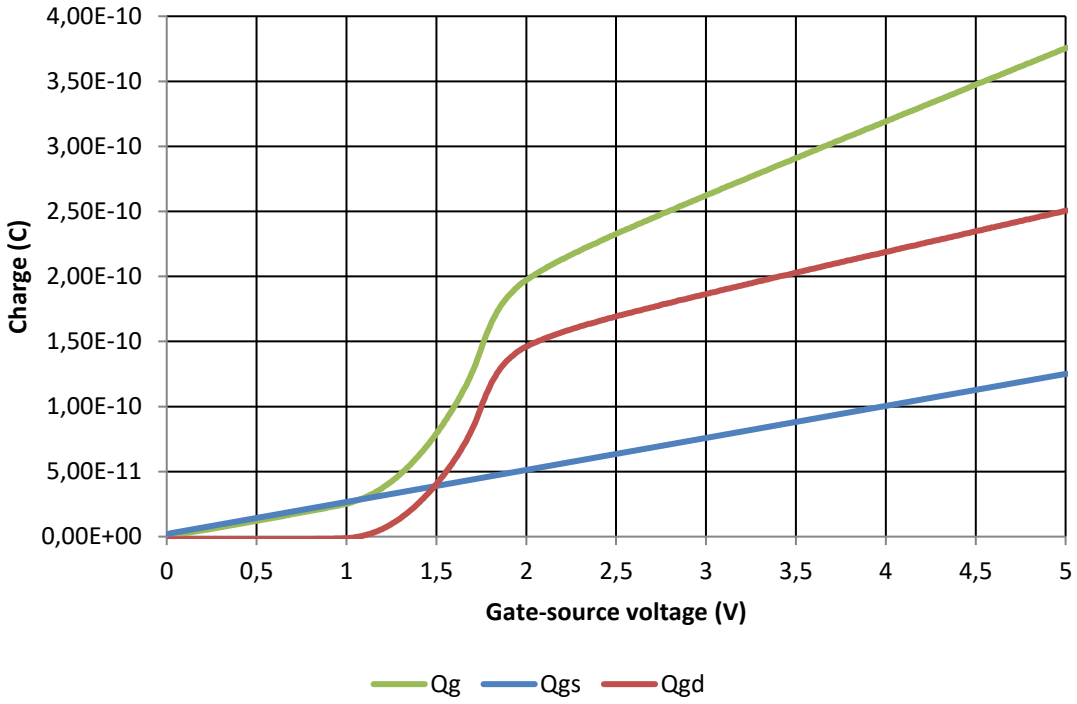

Figure 38. *Gate-source charge extraction from gate charge.*

From this first segment of the curve a linear approximation, the blue curve, was acquired. Then subtracting the Q_{gs} from the gate charge curve results in the gate-drain charge shown as red curve in Figure 38. This approach worked perfectly with the high side MOSFET but for the low side some MOSFET manual tuning was needed as the linear approximation for Q_{gs} did not hold. The tuning was done by changing the slope of the Q_{gd} curve until the switching characteristics matched with Cadence. The change in slope of Q_{gd} obviously affected Q_{gs} curve and therefore Q_{gs} was not possible to model linearly. Q_{ds} was simply subtraction between output charge and Q_{gd} curves. The simulated charge curves were then imported into SIMPLIS PWL capacitors.

Fitting the PWL capacitances is a balance between simulation accuracy and simulation speed and the MOSFET parasitics are the most significant in terms of possible PWL complexity. Careless PWL selection may lead into simulation slowdowns without any gain in simulation accuracy. For example, using the level 3 equivalent circuit, as shown in Figure 17, for the power MOSFETs did not significantly improve simulation accuracy but the simulation time multiplied by eight. One comparison of gate-source voltage differences between the implemented SIMPLIS model and Cadence simulation is shown in Figure 39.

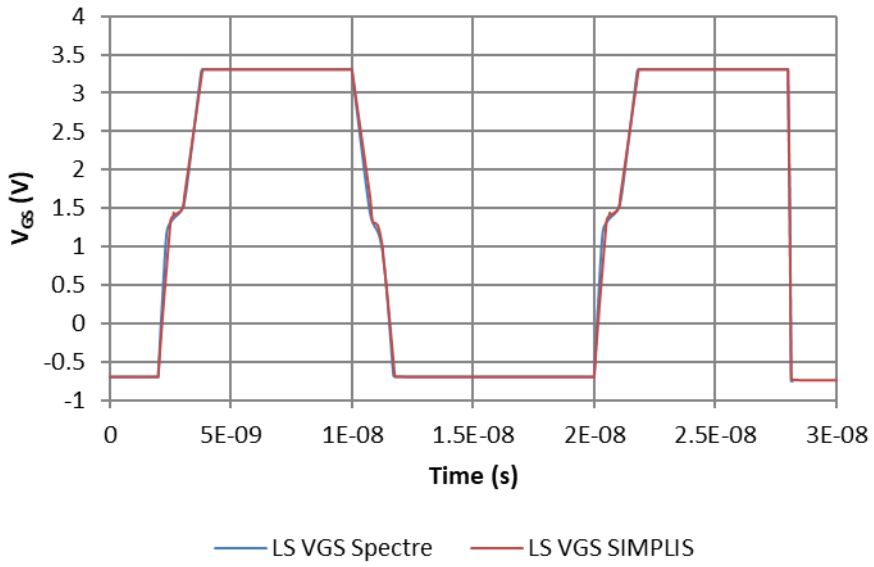

Figure 39. *Low side gate-source voltage comparison.*

The final MOSFET model was even a simpler model than the level 2 equivalent circuit as the high side MOSFET used linear C_{GS} and C_{DS} capacitors whereas low side MOSFET had only C_{DS} modeled linearly. Miller capacitance C_{DG} was the most nonlinear capacitor as expected and had to be modeled with PWL capacitors for both the high side and the low side transistor. But still the model matched Cadence simulations really well as can be seen from Figure 39. The simulation speed benefits acquired from these simplifications can be seen from Table 5.

Table 5. *Processor (CPU) time comparison between the MOSFET implementations.*

Simulation	**CPU time, simple (s)**	**CPU time, complex (s)**
LS MOSFET testbench	0.34	0.35
HS MOSFET testbench	0.32	0.39
Single-phase simulation	36.14	85.44
Two-phase simulation	538.93	1904.08

CPU time is used for comparison to reduce the effect of background load of the processor. Simulation conditions for single- and two-phase simulations are shown in Table 6 below.

Table 6. *Test conditions for simulation speed tests.*

Input voltage (V)	3.3
Output voltage (V)	1
Load current (A)	1
Switching frequency (MHz)	4.4
Inductor (nH)	220
Cycles before POP	300
Cycles plotted	3
Plot points	500 000

The total PWL point count in the power transistors reduced from 79 to 17 points without any significant loss in simulation accuracy. However, massive simulation time reduction was achieved with the simpler MOSFET models. The simpler MOSFET models were used in the final simulation model.

These transistors were then put into the power stage shown in Figure 40. Other power stage losses such as the control logic loss is modeled with the quiescent current I_Q. The value for the I_Q is 2 mA and it is documented on the device datasheet [11, p. 23].

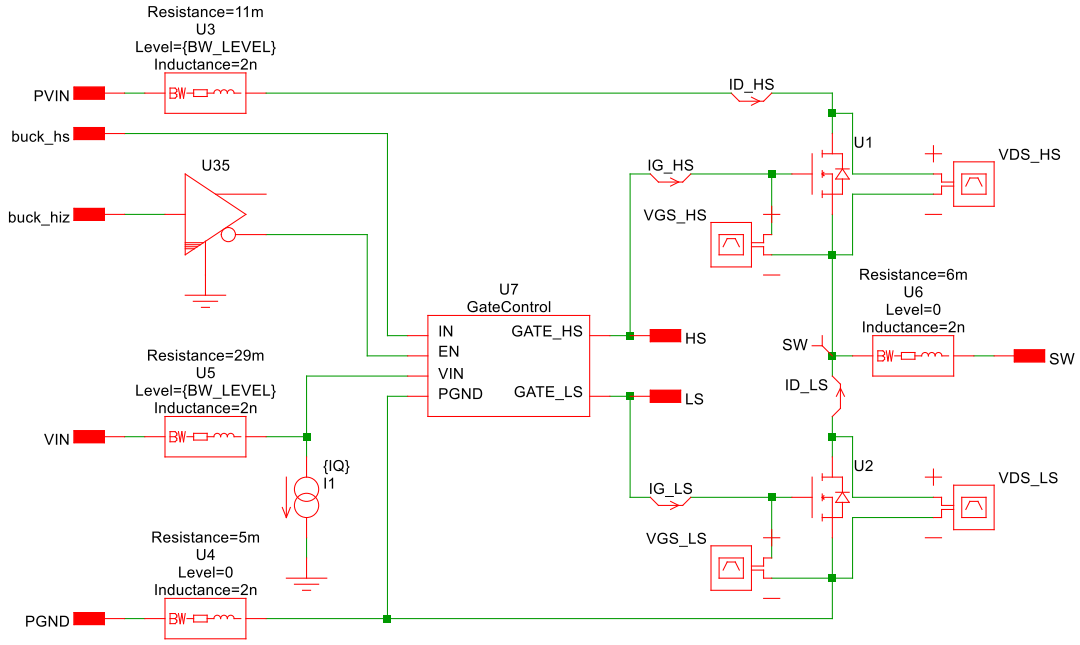

Figure 40. *Power stage.*

Power stage includes bondwires for input voltages of the driver and the power MOSFETs as well as the switch node and power ground plane. The bondwire components have a model level parameter which chooses if the bondwire model includes inductance. This parameter was added because the bondwire inductance introduced severe slowdowns

to the simulation and therefore an option to simulate faster with less accuracy was added. The functionality of multiple model levels for the bondwire was done by exploiting the netlist preprocessor in SIMPLIS. The SPICE subcircuit for the bondwire is shown in Figure 41.

```
.globalvar lev={Level}
.globalvar res={Resistance}
.globalvar ind={Inductance}

.simulator SIMPLIS
.subckt BONDWIRE 1 2
.if {lev == 1}
    R1 1 3 {res}
    L1 3 2 {ind} IC=0
.else
    R1 1 2 {res}
.endif
.ends BONDWIRE
```

Figure 41. *SPICE subcircuit of the bondwire.*

Basically, the implemented tab dialog propagates the inserted inductance, resistance and model level values to the SPICE subcircuit. The ".if" condition then selects which of the two subcircuits will be used. If the level parameter is set to 1, the model with inductance is used. If the level is set to 0 the model includes only the bondwire resistance.

7.1.2 Channel resistance

Based on Cadence simulations done by the designers, the channel on-resistance R_{DS} dependency with input voltage was already known. The resistance values also included the parasitics caused by the bondwires. This dependency was not linear and SIMPLIS does not have a way to model V_{IN}-R_{DS} directly. One way would be to utilize the gain modeling possibility in SIMPLIS which would change the drain current as a function of V_{GS}. This would then change the effective channel resistance of the MOSFET. However, this did not work as expected and did not give the desired result.

The simpler way to add this dependency to the model is to do a curve fitting for the V_{IN}-R_{DS} points and then parameterize the channel resistance in the MOSFETs. A second order polynomial function was found to be precise enough for both MOSFETs even though the high side MOSFET resistance started to ramp up rapidly with low input voltages. Low side MOSFET matched really well with the second order approximation. The approximations for both low side and high side channel resistances are shown in Figure 42.

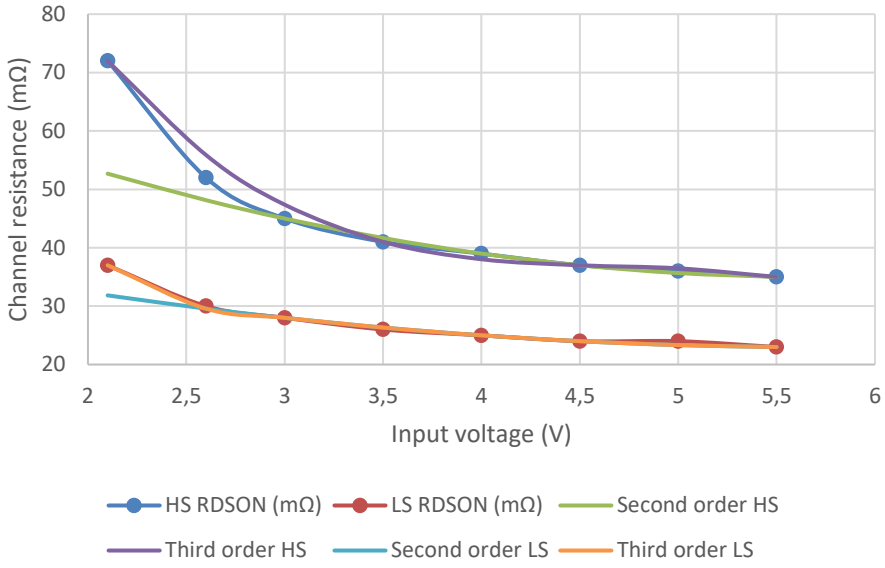

Figure 42. *Power stage channel resistances.*

The third order approximation is more accurate, but the second order curve fit gives good enough accuracy especially with higher than 3 V input voltages which present the most common use cases. The equation for high side channel resistances is

$$R_{DSHS} = 1.333 \cdot 10^{-3} \cdot V_{IN}^2 - 15.333 \cdot 10^{-3} \cdot V_{IN} + 79 \cdot 10^{-3} \quad (41)$$

and for the low side channel resistance

$$R_{DSLS} = 0.6677 \cdot 10^{-3} \cdot V_{IN}^2 - 7.66667 \cdot 10^{-3} \cdot V_{IN} + 45 \cdot 10^{-3} \quad (42)$$

where V_{IN} is the input voltage of the TPS6594x-Q1. These equations were used to calculate the R_{DS} for both MOSFETs in the power stage. Obvious downside of this implementation is that the R_{DS} is always constant during one simulation as the value is calculated during netlisting. This means that, for example, line transient simulations would not be accurate as the changes in channel resistance are not considered. Current dependency of the channel resistance was investigated and a slight increase in channel resistance as a function of drain current was observed in Cadence simulations. However, the increase in resistance was approximately only 1 mΩ and therefore it was negligible and not implemented in the model.

7.1.3 Deadtime and body diode

Deadtime of the power stage could be seen in the inductor voltage measurements as negative spikes at the rising and falling edges of the inductor voltage waveform. Simulations were done in Cadence for multiple different configuration to obtain the deadtimes and some data was already available in the design documents as well. Simulations were compared to the measured waveforms and measured deadtimes seemed to agree with the deadtime data gathered from Cadence simulations. Similarly,

as with the channel resistance, a second order curve fit was done using the simulation data.

Body diode was simulated with a test schematic that simply forward biases the body diode of the MOSFET and measures the drain current. Body diode of the low side MOSFET was simulated with a schematic shown in Figure 43.

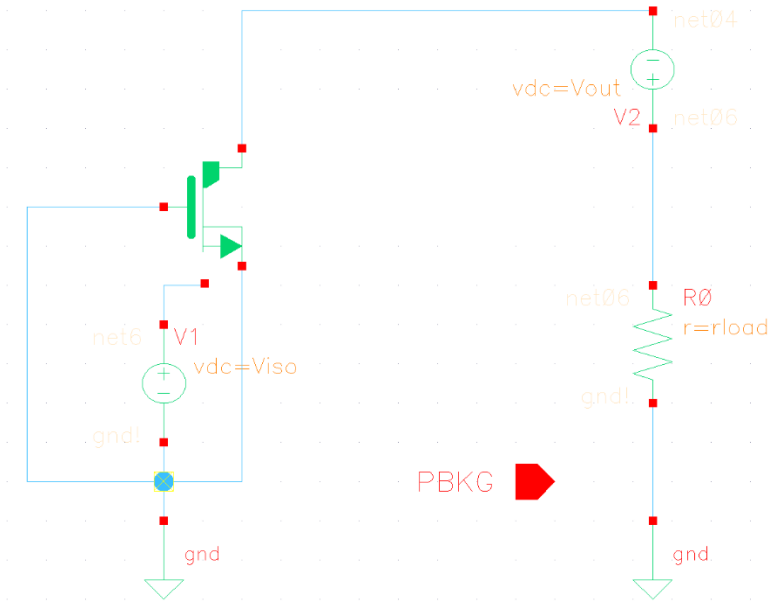

Figure 43. *Low side body diode test schematic.*

Simulations were done with ADE XL using Spectre and the bias voltage was swept from 0 to 2 V with 100 mV steps. The same test was repeated for high side MOSFET as well even though the HS body diode is not that important in terms of power consumption as the low side body diode.

The simulation results the drain current and forward bias voltage of the body diode were imported into the SIMPLIS MOSFET model using a VPWL resistor, a voltage dependent resistor. The PWL model was simplified to be nearly ideal diode because the simulation time was becoming an issue and optimizations had to be made. Threshold voltage of the body diode is the voltage where the Cadence results saw a significant increase in drain current. This resulted in three PWL points in the model of the body diode and the PWL points for the high side MOSFET are shown in Figure 44.

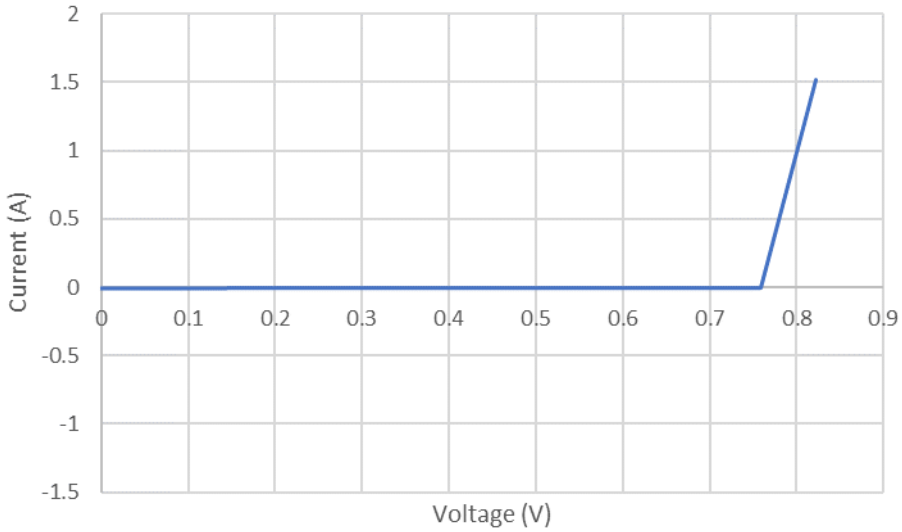

Figure 44. *High side body diode PWL approximation.*

First PWL point is at -100 kV with -1 A current which also determines the diode off-resistance. In this case the off-resistance is 100 kΩ. The point at -100 kV is not shown to improve the readability of the graph.

7.2 Driver

The basic SIMPLIS model, from which this efficiency model was started, turned on the power stage MOSFETs just by supplying them with voltage from a logical AND-port. Because the model used ideal switches as the power stage MOSFETs, higher gate voltage for the high side switch was not needed. However, when the power stage was switched to use the created MOSFET models a charge pump had to be made to raise the high side gate voltage above the input voltage. The implemented charge pump is shown in Figure 45.

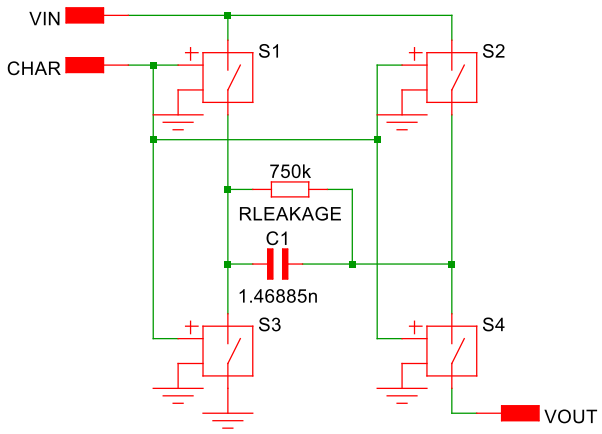

Figure 45. *Charge pump implementation.*

Switches S2 and S3 conduct when the charge signal CHAR is high, and the capacitor's right plate is charged to input voltage. When the CHAR signal is low, switches S1 and S4 conduct and the charged capacitor is then in a series with the input voltage which effectively doubles the voltage seen at the VOUT terminal. The voltage losses across the switches and the leakage loss were matched against Cadence simulations. The charge pump multiplied the input voltage by 1.89.

The gate driver itself also had to be further improved. The logical AND-port could be used to drive the gate but the digital logic ports in SIMPLIS are completely ideal. These logic ports do not have a pin for the input voltage other than the two logical inputs. Output of the logic port does not take the energy from either of the logical inputs because the port simply creates the voltage and current required for the output. Obviously, this is not allowed when the power losses are the main point of the simulation and therefore simple push-pull switch configurations were added between the MOSFET gates and the driving AND-ports. The whole MOSFET driving circuitry is shown in Figure 46.

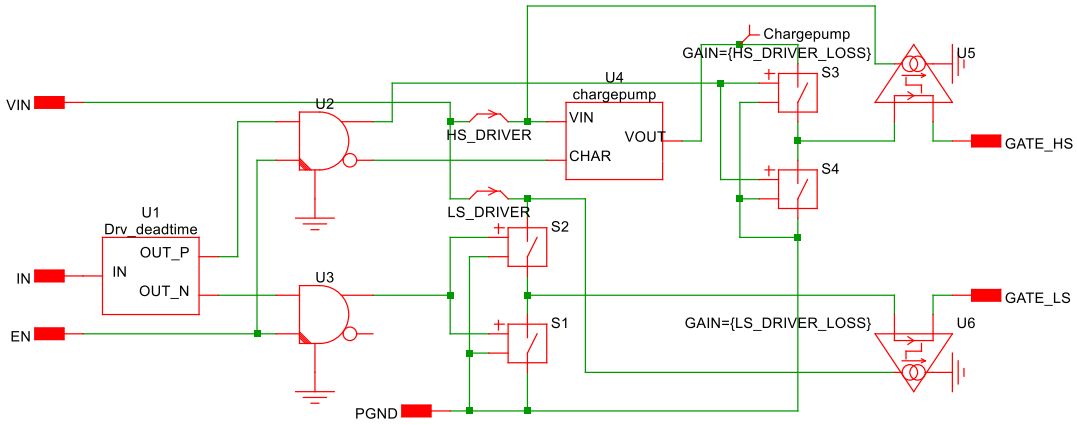

Figure 46. *Power stage driver schematic.*

The driver strengths for both the low side and the high side push-pull stages were acquired from Cadence simulations by simulating the gate currents and the driver input currents. The gate current waveforms using the simplified driver shown in Figure 46 was similar enough to the waveforms observed in Cadence and therefore just fitting the maximum and minimum of the gate currents in SIMPLIS is adequate to obtain a good enough approximation. This was done by simulating gate currents first in Cadence and then in SIMPLIS. The error in gate and driver currents was then compensated by changing the on-resistances in both push-pull drivers to match the Cadence gate current results. Also, because all the driver current does not flow to the gates of the power MOSFETs and is wasted in the driver itself, a current controlled current sources U5 and U6 were added to emulate the wasted current.

However, gate currents were also input voltage dependent and therefore the push-pull resistances and emulation currents should change accordingly. The same simulation as described above were done for different input voltages and the compensation was done in similar manner as well. All the compensations were tabulated for each input voltage and then a linear curve fit was done for the data which resulted in equations that gave the resistances for the push-pull stages.

7.3 Inductor

Inductor was modelled with parallel resistor and capacitor as well as with L-R ladder which allows to model the AC resistance of the inductor. The equivalent circuit for the 470 nH inductor is shown in Figure 47.

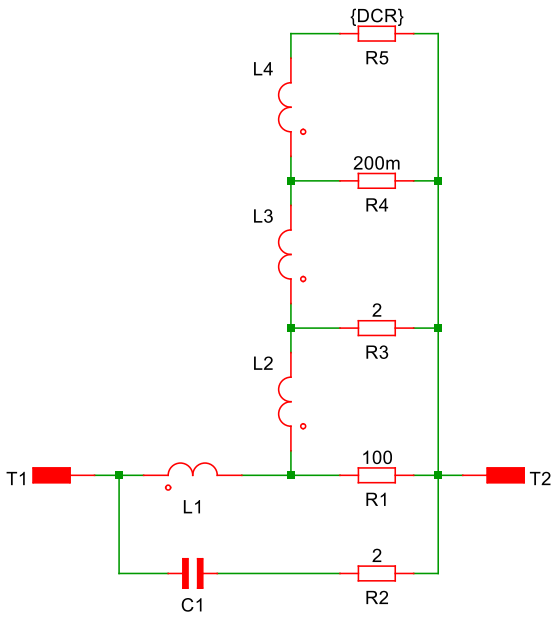

Figure 47. *Equivalent circuit for the modeled 470 nH inductor.*

The inductor L1 in Figure 47 could also be a PWL inductor which defines the inductance via flux linkage and inductor current, so it basically models the inductance and current relationship. Inductance of the PWL inductor is the slope of the flux-current curve. The effect was investigated to find out if it had a significant impact on efficiency.

To fit PWL data with the datasheet's inductance-current curve, a few inductance and current points could be selected from the datasheet. Then a fourth order polynomial curve fit was done using Matlab's curve fitting tool. The resulting function was the derivative of the flux linkage from which the actual function of flux linkage can be acquired by applying a numerical trapezoidal integration. However, this was not used in the final

simulation model as the effect on efficiency was minimal but the simulation time increased.

Other values for the equivalent circuit were iterated in Cadence PSpice to match the impedance and resistance data in the datasheet. The process to fit the AC resistance with the manufacturer's data was following.

1) Select three or more resistance values and the DC resistance value, for example 100 Ω, 10 Ω, 1 Ω and 18 mΩ from the R_{AC} graph and form L-R ladder with small inductances and selected resistances as resistor values. Largest resistance should be the lowest one in the ladder.
2) Place the self-resonance frequency to the correct frequency with corresponding magnitude using the parallel resistor and capacitor. The external inductor L1 should be set to the nominal inductance.
3) Start to iterate the lowest inductor in the ladder and see when the formed R_{AC} curve crosses the selected resistance. Once the fit for the resistance is found, proceed to the next step with smaller resistance and repeat the fitting procedure.
4) Once all the inductance steps have been fitted, shift the impedance graph back to the correct level by decreasing the inductance value of the external inductor set in step 2. A good initial guess is the nominal value minus the sum of all the fitted inductance values.

The idea of the L-R ladder was the same as proposed by Kim and Neikirk [37]. However, the way of acquiring the desired model was not the same. The iterative algorithm proposed above is a simple and quick way to achieve a good approximation by simulating the impedance curve. This method works as long as the resistances selected are much greater than the DC resistance since the DC resistance must dominate in the parallel resistance circuit.

The inductor SIMPLIS models were validated against the measured data using an automated testbench and SIMPLIS DVM. DVM enables automating the simulations by using a testplan which is an Excel spreadsheet that defines the simulation parameters. The tests were done on the actual efficiency simulation model in order to get the effect of deadtime and body diode on the waveforms. The testbench used for the simulations is shown in Figure 48.

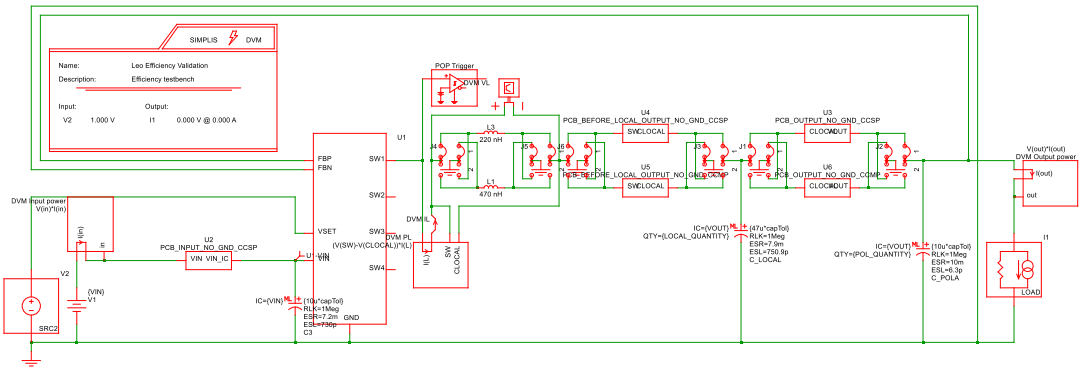

Figure 48. *Inductor power loss testbench.*

Input and output voltages and output current were the same as in the measurements during the simulations. The voltage loss was simulated with a fixed differential probe and the power loss was simulated with an arbitrary probe that multiplied the inductor current with the inductor voltage. An example comparison of the inductor voltage waveforms is shown in Figure 49.

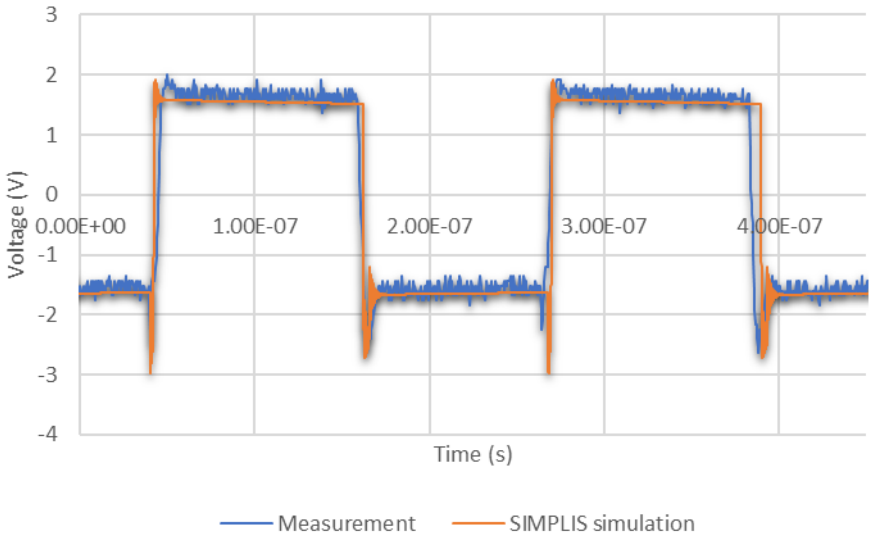

Figure 49. *Simulated and measured inductor voltage comparison, 220 nH inductor, V_{IN}=3.3 V, V_{OUT}=1.5 V, f_{sw}=4.4 MHz and I_{OUT}=3 A.*

Simulated inductor voltage waveforms match the real measured waveform well apart from the slight time shift caused by the slight variations in duty ratio and frequency of the real waveform. A slight difference between the on- and off-time voltage levels was also observed but this is probably due to the inaccuracy of the oscilloscope.

Comparison of the simulated and measured power losses is done by plotting all the measurement points into a graph. A reference loss is also calculated with equation 34 for the comparison. Loss comparison for the 470 nH is shown in Figure 50.

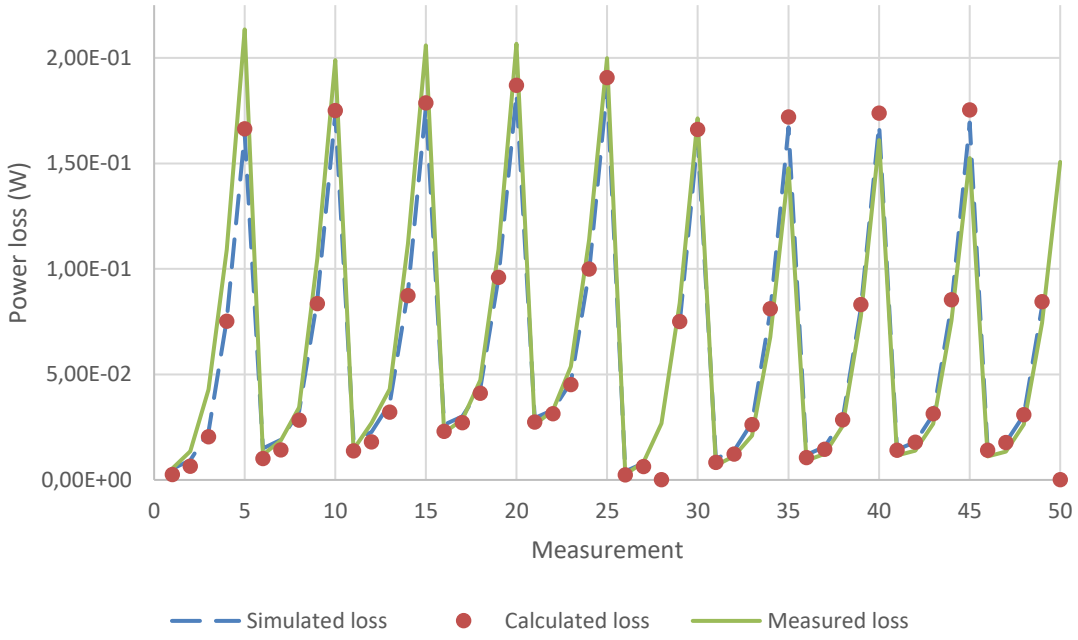

Figure 50. *Comparison of measured and simulated power losses for the 470 nH inductor.*

The error caused by the oscilloscope is also observable from Figure 50 where the first horizontal half of the measurements is done with 5 V input voltage where the error is larger. The latter half is the comparison with 3.3 V input voltage and the simulated losses are much closer to the measured losses. Similar graph is drawn for the 220 nH inductor in Figure 51.

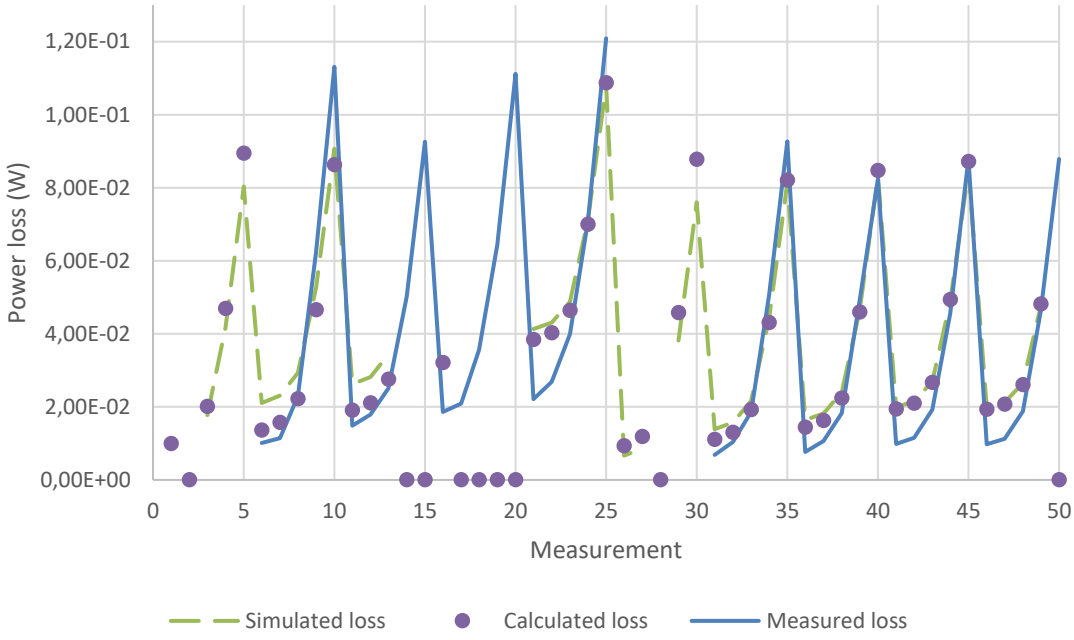

Figure 51. *Comparison of measured and simulated power losses for the 220 nH inductor.*

The error of the oscilloscope is much more severe with the 220 nH inductor as the loss components are smaller. Again, with the 3.3 V input voltage in the latter horizontal half of the measurements the simulation model matches the measurements really well apart from the slight difference with low inductor current situations. The simulated inductors were also compared against similar inductors from the other manufacturers who provide power loss calculators. Figure 52 shows a comparison between all the different power loss calculators, measured power losses and simulated power losses for 470 nH inductors.

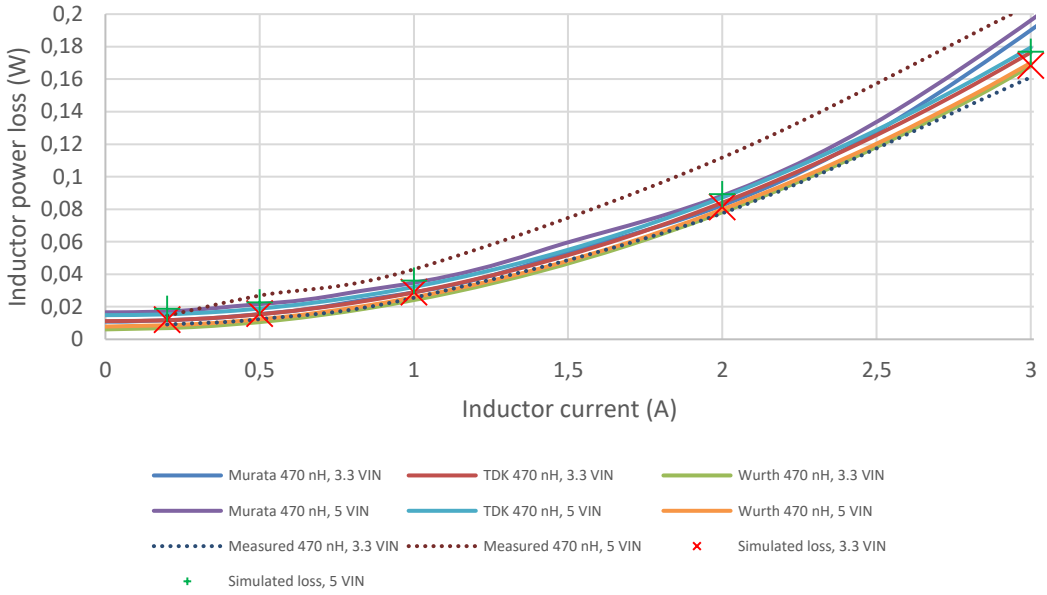

Figure 52. *Simulated power losses of 470 nH inductor compared to different power loss calculators. Results for Murata, TDK and Wurth from sources [40-42].*

Simulation model fits the calculators of various manufacturers quite well. The simulation data also suggests that the measurements with 3.3 V input voltages are closer to reality as was concluded in chapter 6.1. Similar comparison is done for the 220 nH inductor in Figure 53.

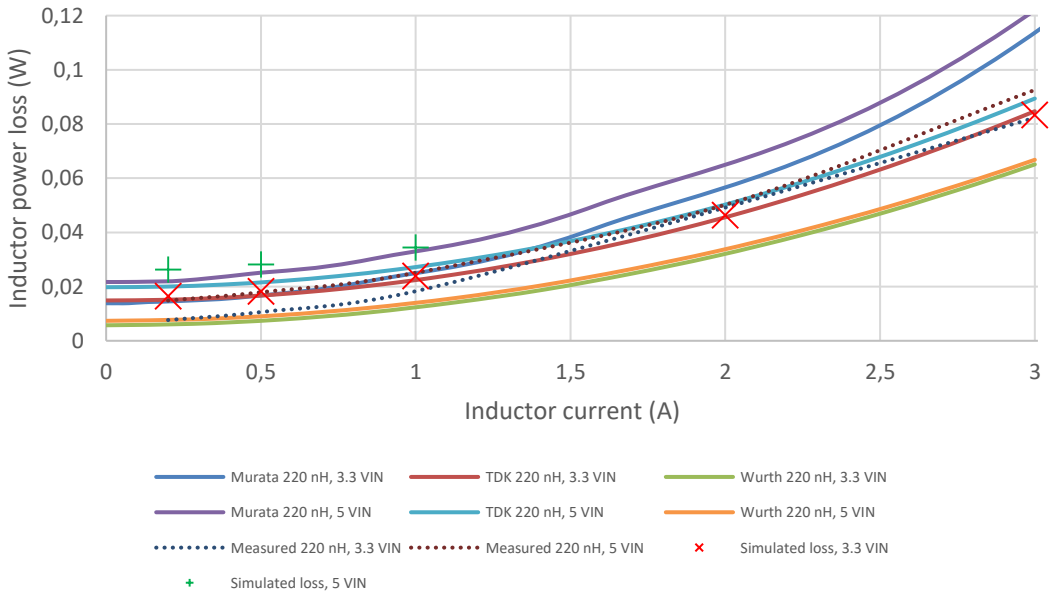

Figure 53. *Simulated power losses of 220 nH inductor compared to different power loss calculators. Results for Murata, TDK and Wurth from sources [40-42].*

Simulated results match the expected power losses quite well. At lower inductor currents the simulated losses are a bit higher than the measured losses, but the simulated losses

match the other inductor variants even at low currents. Both inductor models seem to be accurate enough for the efficiency model and certainly more accurate than the default inductor SIMPLIS provides.

7.4 Capacitors

Capacitors were simply modeled using the level 2 capacitor model that SIMPLIS provides. The ESR was read from the datasheet's ESR versus frequency characteristics curve. Value read for the ESR was the resistance value at 4.4 MHz frequency. The ESL was calculated from the impedance-frequency characteristic curve by reading the self-resonance frequency. The buck has the output capacitors listed in Table 7.

Table 7. *Output capacitors and their characteristics [46-48].*

Part number	Capacitance (µF)	ESR (mΩ)	ESL (pH)
NFM15HC105D0G	1	0.1	63.3*
NFM18HC106D0G	10	0.1	6.3*
GCM31CR71A226KE02	22	10.9	716.6
GCM32ER70J476ME19	47	7.9	750.9
GCM32ED70G107MEC4	100	9.7*	604.0*
T510X687K006ATA023	680	23	102.6*

Parameters with asterisks are approximations based on similar other components as real measurement data was not available. The first two capacitors in Table 7 are three terminal capacitors and therefore the ESL is very low. Parameters were set for the output capacitors of the simulation model according to Table 7. Also, the model includes one input capacitor CGA4J1X7S1C106K125AC which ESR is 7.2 mΩ and ESL is 730 pH [49]. GCM31CR71A226KE02 capacitor could be used as an input capacitor as well.

Other parasitics effects such as the effect of DC voltage bias is possible to model with PWL segments. However, the change in capacitance caused by the DC voltage is insignificant in terms of power losses caused by the capacitor and modeling this effect would only increase the simulation time. Capacitance values for the capacitors have been selected with a certain safety margin to combat the decrease in capacitance as well.

7.5 PCB

PCB parasitics were extracted using Ansys Q3D Extractor which extracts a SPICE model from the PCB geometry. The PCB layout was first exported from Altium in an ODB++ format which was then read with Ansys SIWave. The PCB region of interest was cut from the whole design to simplify the simulation. From SIWave, the layout was exported to Ansys Q3D Extractor in which the actual simulation is done. Q3D Extractor is quasi-static 3D solver that extracts lumped resistance, inductance, capacitance and conductance (RLCG) parameters as well as forms a SPICE model. Inductances and resistances can be calculated for both AC and DC problems.

For the PCB model, some of the RLCG parameters were extracted from the output and input power planes. TPS6594x-Q1 has five different buck outputs as mentioned in chapter 2.3 and obviously there is parasitic coupling between the different output phases. This parasitic coupling is acknowledged but it is not meaningful in terms of efficiency and more so for the electromagnetic interference analysis. Therefore, the other phases were not included in the parasitic analysis and the test stimulus is only injected into one of the outputs. Losses occurring in the ground plane were ignored as the power losses are negligible and the simulation time increased significantly. Simulation mesh was solved at frequency of 10 times the switching frequency. Frequency sweep was done using a discrete sweep with 10 harmonics. Resistance values were read from the solution at the switching frequency and inductance values from the frequency of the tenth harmonic component.

The current injection points are called sources and current destinations are called sinks in Ansys Q3D Extractor and one net can have one source but multiple sinks. The output plane simulations were done in two parts. The first part was the trace between switch pin and the local capacitor so basically the part where the triangular AC component caused by the inductor exists. The second part was from the local capacitor to the output voltage sense via. The division was done because the AC current suffers from higher PCB resistance caused by the skin effect as shown in Figure 24 but after the local capacitor the current is mostly DC and skin effect is negligible. Thus, AC resistance was extracted for the part between switch node and the local capacitor and DC resistance for the other part, but the inductances were ignored in both cases. Sources and sinks for the output power plane simulation are shown in Figure 54.

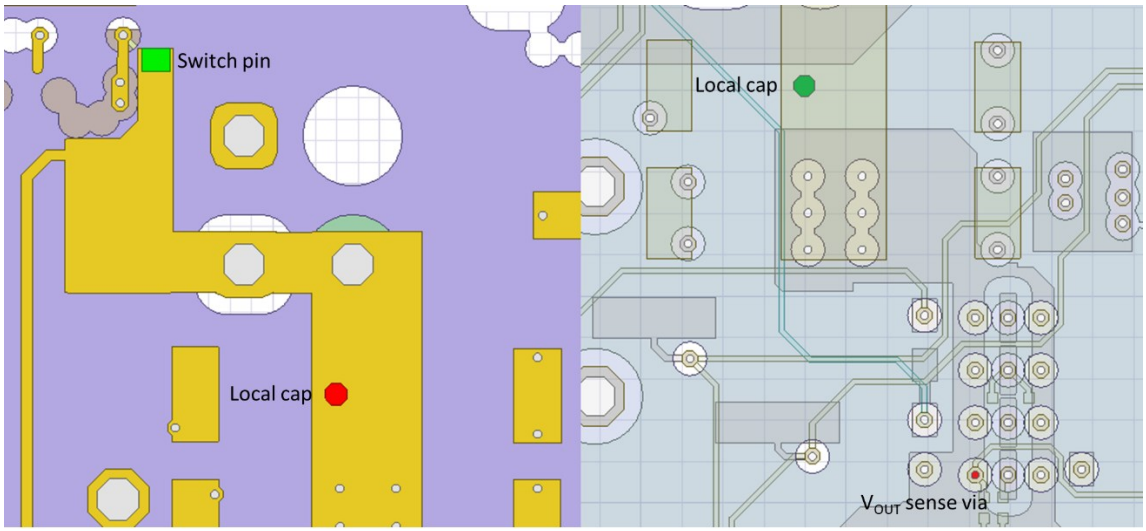

Figure 54. *Simulation ports for the output plane simulations. Sources are green and sinks are red.*

Left half of Figure 54 is the switch pin to the local capacitor part of the output and the right half is the local capacitor to the sense via part. Solution of the analysis was then extracted in a SPICE format and the SPICE model for the output planes can be found in Appendix B: Output SPICE Netlist. Since the efficiency measurements for 470 nH and 220 nH inductors were done on different printed circuit boards, a second output parasitic extraction was needed for the second PCB in a similar manner.

Comparable procedure was done for the input power plane of the device. A current path was formed between the closest input capacitor and the power input pin for buck 1. The input power plane simulation sources and sinks are shown in Figure 55.

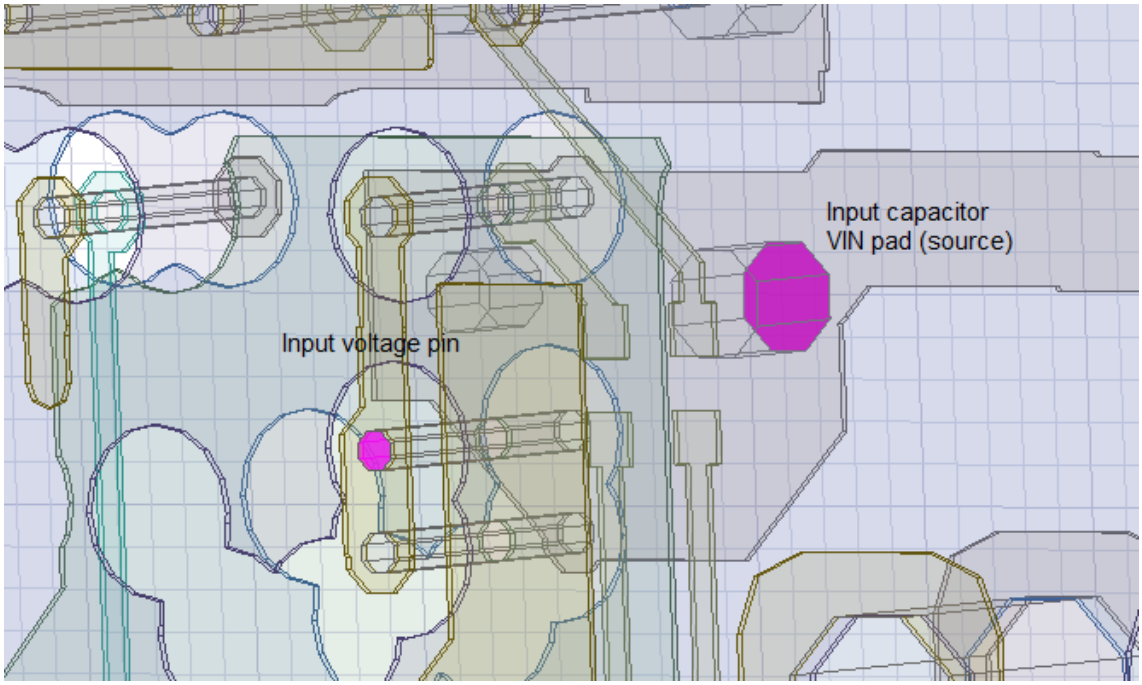

Figure 55. *Supply voltage plane simulation ports.*

The solution was extracted once again in SPICE format and the generated netlist is available in Appendix C: Input SPICE Netlist. DC resistance and AC inductance were extracted for the input power plane PCB model. AC inductance extraction was crucial to model due to the voltage swings the sudden input current changes that a switched mode converter inflicts.

A few modifications must be made to the SPICE netlists in order to the models to function in SIMPLIS. First, a simulator must be specified at the beginning of the netlist with command ".simulator SIMPLIS". If the netlist includes inductor coupling factors, for example K1_2 or so on, these must be changed to mutual inductance M-L1-L2. Mutual inductance can be calculated with equation

$$M_{12} = k_{12}\sqrt{L_1 L_2} \tag{43}$$

where M_{12} is the mutual inductance between inductors L_1 and L_2 and k_{12} is the coupling factor between the inductors. There was not any coupling in the extracted models as they were not complete current loops, in other words, the ground plane parasitics were not extracted.

After coupling factors have been changed to mutual inductances and the simulator has been specified, the model is ready to be installed. The installation can be done in two different ways. SIMPLIS documentation instructs to install the model simply by dragging the generated SPICE netlist file to the command prompt of the simulator which starts the installation procedure. During the procedure a symbol must be created or generated for the model and after that the model is ready to be placed and used.

Second method is to create subcircuit for the model and place just an empty symbol into the subcircuit. Empty symbol's name and pin order must be the same as in the SPICE netlist and the SPICE netlist must be inserted into the F11 window. Then the symbol for the SIMPLIS subcircuit can be made normally. The benefit of using this method is the ease of changing the model once the subcircuit has been made. If the SPICE netlist's pin order does not change, the same SIMPLIS subcircuit and empty symbol can be used, and the SPICE model can be simply changed by inserting the new SPICE netlist to the F11 window in SIMPLIS. Only a change in the empty symbol's name may be necessary. Also, multiple different SPICE netlists may be inserted into the F11 window and changing the name of the empty symbol switches between the SPICE models.

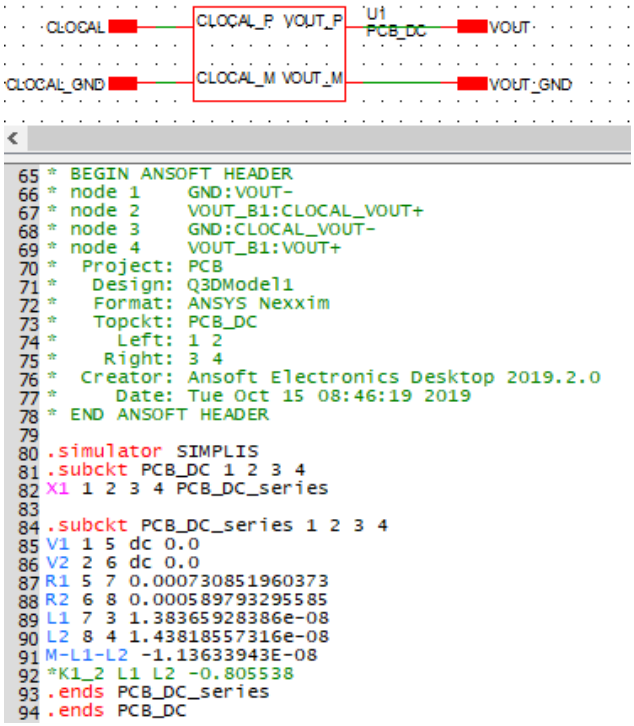

Figure 56. *Example of the second method of using SPICE models in SIMPLIS.*

Figure 56 shows an example use case of the second method described above. The SPICE subcircuit named PCB_DC is inserted into the F11 window and the name of the empty symbol U1 is changed to PCB_DC. The pin order of the empty symbol is changed to match the SPICE subcircuit.

7.6 Efficiency simulation

The simulated efficiency is calculated by launching a script after the simulation completes with a ".post_process" keyword in the F11 window. Post process launches the script in Appendix D: Efficiency calculation and the script can either be a separate file in same folder as the simulation schematic or the script can embedded into the F11 menu with ".file" keyword. The script reads the currents going through the input voltage source and the load resistor. The voltage source reference must be set to Vin and the output load resistor's reference must be RLOAD. The input and output voltages are read from nets named as Vout and Vin and the nets can be named in the schematic using small terminals. The input and output powers are then simply multiplied from the read waveforms and the efficiency is calculated with equation 11.

The intended use case of the efficiency model is to launch a current sweep using a multistep simulation. Therefore, the script must check how many steps have been simulated with a function "NumDivisions". By using the simulator's own multistep tool and the written efficiency calculation script, DVM license is not required to run the

efficiency simulation. Efficiency will be calculated in a for-loop for each simulation step. The steps will be reordered to an increasing load current order in order to draw the efficiency graph correctly. If only one simulation is done, for example by normally simulating just one current, the calculated efficiency will be printed into the console window.

8. RESULTS

The simulated efficiency results are compared against measurement data gathered by the validation team and the same configurations were simulated using the efficiency simulation model. The average error between the simulated efficiency and measured efficiency was then compared in various configurations. The final efficiency model had two model levels and both of them were simulated. Model level 1 adds the inductances to the bondwires where level 0 model only has bondwire resistances modeled. For single-phase configuration the compared results with the 220 nH inductor are in Table 8.

Table 8. *Errors between simulated and measured efficiency with 220 nH inductor.*

V_{IN} (V)	V_{OUT} (V)	Switching frequency (MHz)	Error (%) Model 0	Error (%) Model 1
3.3	0.3	4.4	0.69	1.73
	0.8		2.07	1.09
	1.0		1.91	1.04
	1.5		1.66	1.05
	1.9		1.54	1.13
5.5	0.3		1.50	2.38
	0.8		1.27	1.24
	1.0		1.32	1.20
	1.5		1.22	1.01
	1.9		1.19	0.87

Average error when using level 0 model is 1.44 % and when using level 1 model the average error is 1.27 %. Level 1 model slightly improves the simulation accuracy. Example of a comparison between measured and simulated model level 0 efficiency graphs is in Figure 57.

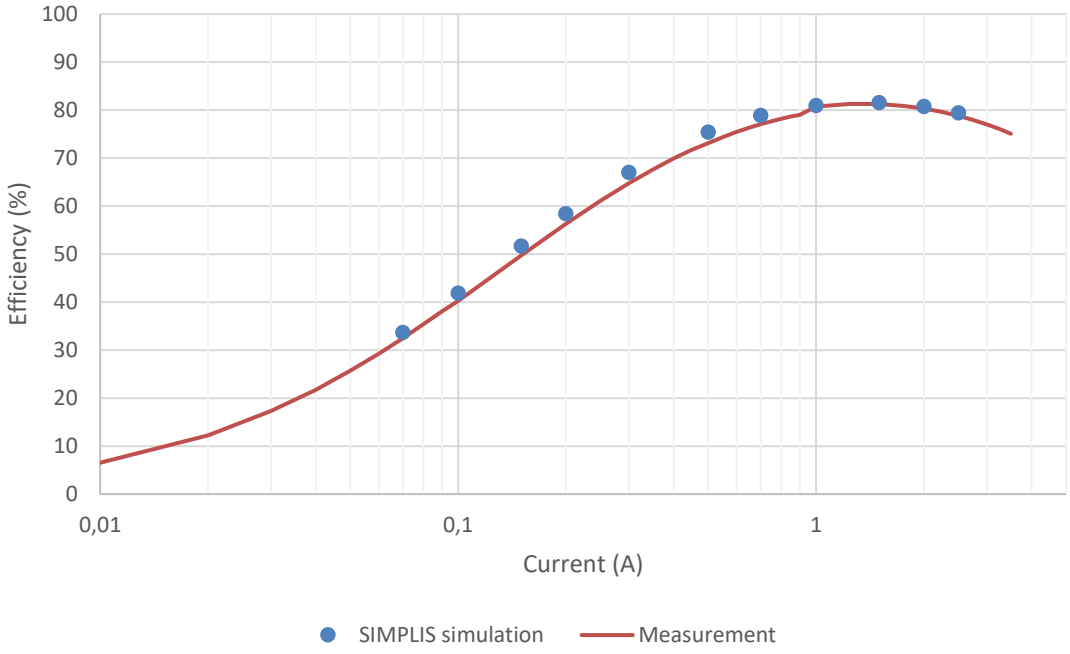

Figure 57. *Simulated (model 0) and measured efficiency graphs for 1 V_{OUT}, 5.5 V_{IN}, f_{sw}=4.4 MHz with 220 nH inductor.*

The simulation error is largest with low output currents and the accuracy improves when the output current increases. Similarly, the comparisons of the simulation and the measurement results for the single-phase configuration with the 470 nH inductor are in Table 9.

Table 9. *Errors between simulated and measured efficiency with 470 nH inductor.*

V_{IN} (V)	V_{OUT} (V)	Switching frequency (MHz)	Error (%) Model 0	Error (%) Model 1
3.3	0.6	2.2	0.66	1.14
	0.8		0.63	0.98
	1.0		0.62	0.87
	1.5		0.53	0.66
	1.8		0.46	0.57
5	0.6		1.15	1.93
	0.8		0.85	1.49
	1.0		0.85	1.45
	1.5		0.69	0.89
	1.8		0.72	0.81

Average error of all level 0 simulations in Table 9 is 0.72 % and 1.08 % for level 1 simulations. Adding the bondwire inductances with level 1 model did not improve the simulation accuracy. One of the comparisons between level 0 model and measured efficiency is plotted in Figure 58.

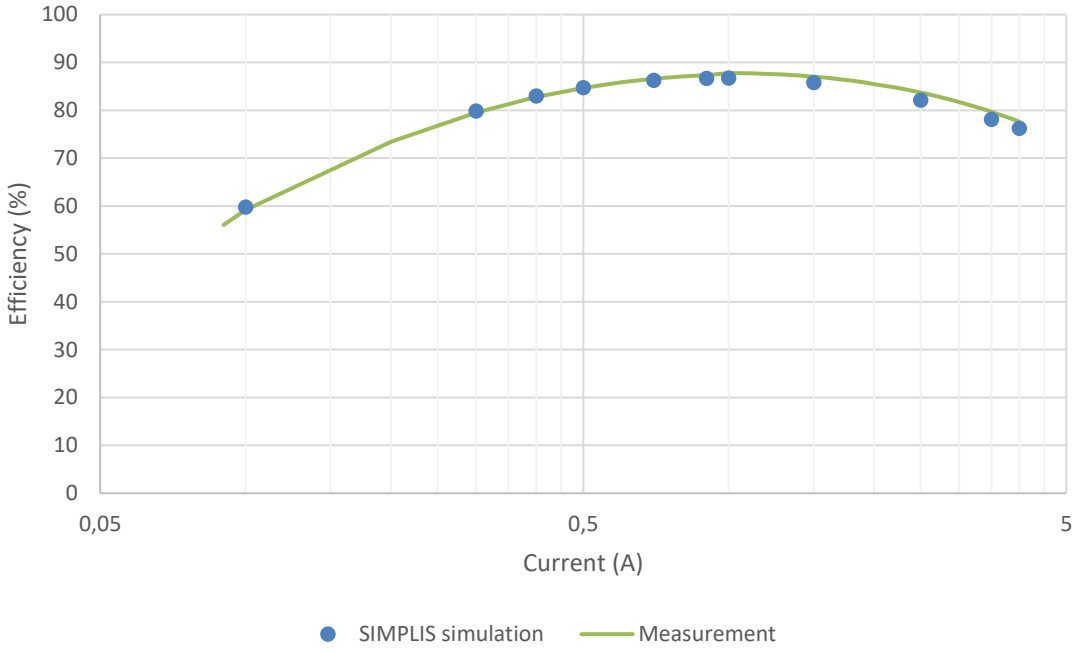

Figure 58. *Simulated (model 0) and measured efficiency graphs for 1 V_{OUT}, 5 V_{IN}, f_{sw}=2.2 MHz with 470 nH inductor.*

Unlike with the 220 nH inductor and 4.4 MHz switching frequency, this simulation gives really accurate results even at low output currents. Simulated currents differ slightly from the ones simulated for Figure 57 because of the different measurement currents.

Also, the multiphase functionality of the simulator was validated with a two-phase configuration with two 470 nH inductors. Phase adding functionality and simulation time were the main concerns with the multiphase simulations. The comparison with measured results is in Table 10.

Table 10. *Errors between simulated and measured efficiency with 470 nH inductors in two-phase configuration.*

V_{IN} (V)	V_{OUT} (V)	Switching frequency (MHz)	Error (%) Model 0	Error (%) Model 1
3.3	0.6	2.2	0.46	0.61
	0.8		0.61	0.58
	1.0		0.71	0.53
	1.5		0.72	0.53
	1.8		0.81	0.69
5	0.6		0.93	1.57
	0.8		0.47	0.99
	1.0		0.39	0.69
	1.5		0.59	0.56
	1.8		0.77	0.58

The average error for level 0 model is 0.65 % and for level 1 model the average error is 0.73 %. Again, the level 1 model did not improve accuracy. One of the two-phase configurations is compared and drawn in Figure 59.

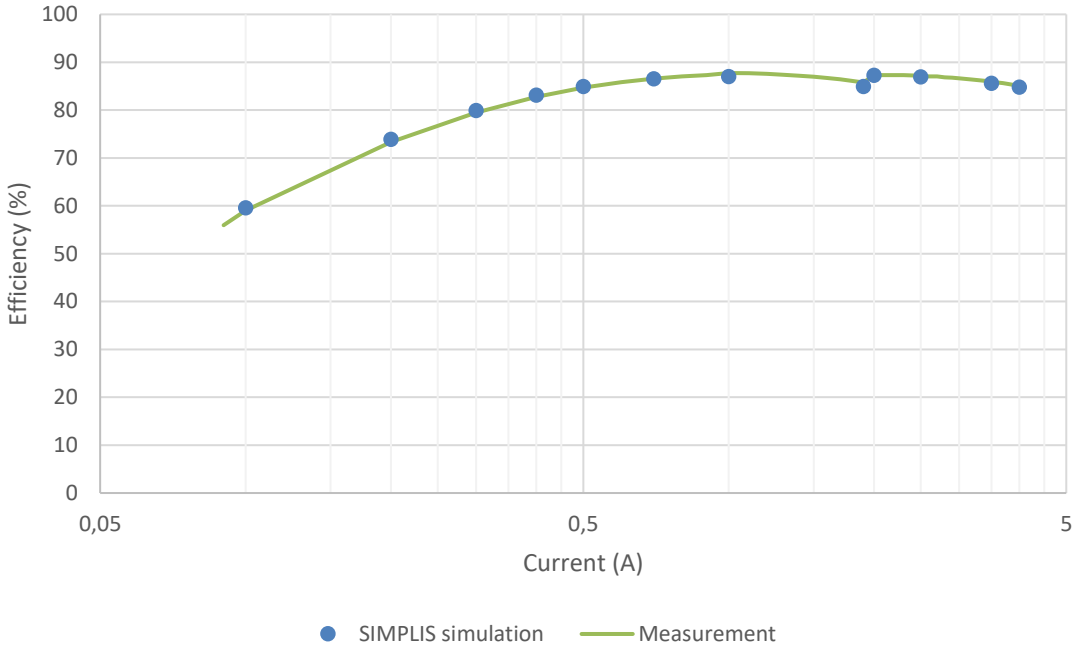

Figure 59. *Comparison of measured and simulated two-phase configuration with V_{OUT}=1 V, V_{IN}=5 V, f_{sw}=2.2 MHz and 470 nH inductor.*

Phase adding can be seen from the graph at 2 A load current when the second phase is added to increase the efficiency and the model does phase adding correctly. Interestingly level 1 model did not improve the accuracy in either of the simulated 2.2 MHz testcases. This is probably caused by the fixed resistances of the implemented bondwires which should decrease with the lower switching frequency due to the skin effect.

Simulation time was an important parameter for the model as well. If the model was too slow it would not be that practical and useful. Therefore, simulation times for different configurations were tested by running a single current efficiency simulation. Simulation time results are in Table 11.

Table 11. *Simulation times with different configurations.*

Phases	Model level	CPU time (s)
1	0	18.45
	1	49.15
2	0	136.61
	1	274.36
3	0	703.44
	1	1875.52
4	0	-
	1	-

The four-phase models were simulated for over 10 hours, but the POP analysis still had not converged. Those simulations were stopped, and those the configurations were determined to be unfeasible to be simulated with this model. All tests were run with simulation settings shown in Table 12.

Table 12. *Simulation time test settings.*

Input voltage (V)	3.3
Output voltage (V)	1
Load current (A)	1
Switching frequency (MHz)	4.4
Force multiphase	1
Inductor (nH)	220
Cycles before POP	500
Cycles plotted	3

Simulation could be sped up by decreasing the “Cycles before POP” value. Obviously, the simulation times will vary depending on the simulation hardware used as well and these tests were run on Intel i7 8700k.

9. CONCLUSIONS

This thesis had a lot of variety in it and a lot of different things were introduced and learnt during the process. Usage of the Cadence IC tools had to be learnt from scratch as no previous experience with those tools were had. Other completely new tools that had to be learnt to use were Ansys SIWave and Ansys Q3D Extractor which were used for the PCB parasitic extraction. The thesis was not all about other simulators and some measurements were done as well. During the inductor measurements it was observed how poor amplitude accuracy the oscilloscope has in measurements. Also, the effect of propagation delay in the oscilloscope probes had been completely neglected before. Inductor measurements also provided an opportunity to refresh LabVIEW and Matlab skills. However, the main point that was learnt during the thesis is what different loss components there are in switched mode converters and how they affect efficiency of the device.

The implemented efficiency model includes the losses caused by MOSFET, bondwire, PCB and external component parasitics and was tested with two different inductors with two different switching frequencies. Implemented MOSFETs are based on the level 2 equivalent circuit with a few simplifications. Modeled MOSFET parasitics include the capacitances between different terminals and channel resistance which were modeled based on Cadence simulations. The implemented MOSFET models should have been tested with the complete simulation model sooner to avoid a lot of unnecessary work with the parameterized MOSFET models. The PCB parasitics were modeled based on the simulations done with Ansys Q3D Extractor and the SPICE netlists for input net and output nets were extracted.

The power stage gate drivers were mostly redone when comparing to the model at the beginning. A charge pump was implemented to raise the gate voltage for the high side MOSFET and the drivers itself were done using switches arranged in a push-pull configuration. Switches had on-resistance but other than that they were ideal. The resistances were calculated to match the gate currents simulated in Cadence. Also, other losses happening in the driver were approximated by adding a secondary current with current controlled current source which emulated the other driver losses.

The inductors were modeled using L-R ladders to match the datasheet graphs. Also, the inductor losses were compared against the measurement data gathered in the laboratory and other inductor power loss calculators. The inductors were also the most problematic component in simulations as well as in measurements due to the complex

theory behind magnetics and various challenges in measurements. The models and the inductor measurement results were revised even late into the actual writing process. A lot of unnecessary work was done due to incorrect measurement setups and the modeling process went to the wrong way from the beginning. Inductor measurement system should have been automatized from the beginning and no manual measurements should have been done. An automatic vertical range selection should also have been implemented as the power loss waveform was highly dependent on the selected inductor voltage range.

The final efficiency model achieved approximately 1 % accuracy on average with less than 30 second simulation time depending on the configuration. The model was validated against one-phase and two-phase configurations with two different inductors and switching frequencies. The average error for each configuration is summarized in Table 13.

Table 13. *Average error in simulated efficiency with level 0 model.*

	220 nH, 4.4 MHz Single-phase	**470 nH, 2.2 MHz Single-phase**	**470 nH, 2.2 MHz Two-phase**
Error (%)	1.44	0.72	0.65

Single-phase simulation with 220 nH inductor and higher switching frequency gave the least accurate results and lower switching frequency gave more accurate results. Every configuration was tested with five different output voltages and two different input voltages. Intended use case for the simulation model is to do a load current sweep with multistep function and a script to parse and draw the efficiency data was made using the scripting language in SIMPLIS.

Future research could be made on the MOSFET modeling. One interesting feature that could be investigated is if the physical parameters of the transistors could be considered in the model. In other words, the transistor capacitances and channel resistances would be modeled based on the channel width and length, gate finger quantity, device quantity and so on. This would bring the SIMPLIS transistors closer to the transistor models in Cadence. Of course, the model would be specific to a certain manufacturing process and probably would be a quite complex subject to study.

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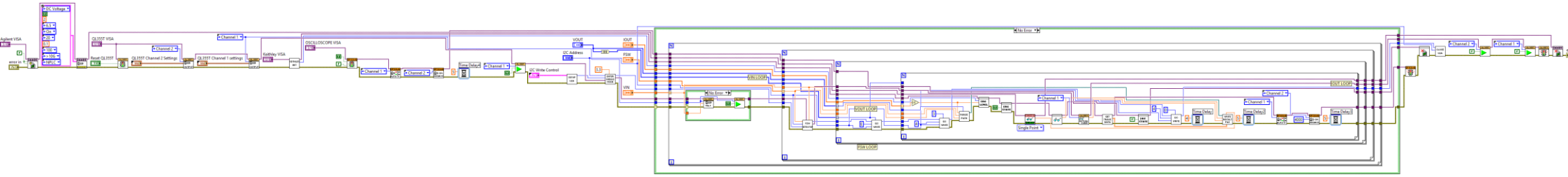
APPENDIX A: LABVIEW SEQUENCE TOP VIEW



APPENDIX B: OUTPUT SPICE NETLISTS

```
.subckt CCMP_CLOCAL_VOUT_10XDISCRETE_2_2MHZ_DCR 1 2
X1 1 2 CCMP_CLOCAL_VOUT_10XDISCRETE_2_2MHZ_DCR_series

.subckt CCMP_CLOCAL_VOUT_10XDISCRETE_2_2MHZ_DCR_series 1 2
V1 1 3 dc 0.0
R1 3 2 0.00128982036529
.ends CCMP_CLOCAL_VOUT_10XDISCRETE_2_2MHZ_DCR_series
.ends CCMP_CLOCAL_VOUT_10XDISCRETE_2_2MHZ_DCR


.subckt CCMP_SW_CLOCAL_10XDISCRETE_2_2MHZ_ACR 1 2
X1 1 2 CCMP_SW_CLOCAL_10XDISCRETE_2_2MHZ_ACR_series

.subckt CCMP_SW_CLOCAL_10XDISCRETE_2_2MHZ_ACR_series 1 2
V1 1 3 dc 0.0
R1 3 2 0.00362467549738
.ends CCMP_SW_CLOCAL_10XDISCRETE_2_2MHZ_ACR_series
.ends CCMP_SW_CLOCAL_10XDISCRETE_2_2MHZ_ACR


.subckt CCSP_CLOCAL_VOUT_10XDISCRETE_4_4MHZ_DCR 1 2
X1 1 2 CCSP_CLOCAL_VOUT_10XDISCRETE_4_4MHZ_DCR_series

.subckt CCSP_CLOCAL_VOUT_10XDISCRETE_4_4MHZ_DCR_series 1 2
V1 1 3 dc 0.0
R1 3 2 0.00262174227239
.ends CCSP_CLOCAL_VOUT_10XDISCRETE_4_4MHZ_DCR_series
.ends CCSP_CLOCAL_VOUT_10XDISCRETE_4_4MHZ_DCR


.subckt CCSP_SW_CLOCAL_10XDISCRETE_4_4MHZ_ACR 1 2
X1 1 2 CCSP_SW_CLOCAL_10XDISCRETE_4_4MHZ_ACR_series

.subckt CCSP_SW_CLOCAL_10XDISCRETE_4_4MHZ_ACR_series 1 2
V1 1 3 dc 0.0
R1 3 2 0.00965147086836
.ends CCSP_SW_CLOCAL_10XDISCRETE_4_4MHZ_ACR_series
.ends CCSP_SW_CLOCAL_10XDISCRETE_4_4MHZ_ACR
```

APPENDIX C: INPUT SPICE NETLIST

```
.subckt INPUT_NET_DCR_ACL 1 2
X1 1 2 INPUT_NET_DCR_ACL_series

.subckt INPUT_NET_DCR_ACL_series 1 2
V1 1 3 dc 0.0
R1 3 4 0.00109094836007
L1 4 2 8.42793902571e-10
.ends INPUT_NET_DCR_ACL_series
.ends INPUT_NET_DCR_ACL
```

APPENDIX D: EFFICIENCY CALCULATION

```
let step_count = NumDivisions(:RLOAD#P)
let LoadCurrent = makevec(step_count)
let effvector = makevec(step_count);

for i = 0 to step_count-1 step 1
     * or alternatively use arbitrary probes or power probes to get
the current
     let Iout = :RLOAD#P[i]
     let Vout = :#Vout[i]
     let Iin = :Vin#N[i]
     let Vin = :#Vin[i]
     let Pout = Iout*Vout
     let Pin = Iin*Vin
     let effvector[i] = mean(Pout)/mean(Pin)*100
     let LoadCurrent[i] = mean(Iout)
next i

if step_count = 1 then
     * If only one simulation is done,
     * print result in console
     let Iout = :RLOAD#P
     let Vout = :#Vout
     let Iin = :Vin#N
     let Vin = :#Vin
     let Pout = Iout*Vout
     let Pin = Iin*Vin
     let effvector[0] = mean(Pout)/mean(Pin)*100
     echo Efficiency: {effvector[0]}
else
     let effvector_orig = effvector
     let loadcurrent_orig = LoadCurrent
     * SORT INDEXES
     let indexes = SortIdx2(LoadCurrent,'forward')
     * Sorting is needed if the sweep is done using multicore multi-
step
     for i = 0 to step_count-1 step 1
          let effvector[i] = effvector_orig[indexes[i]]
          let LoadCurrent[i] = loadcurrent_orig[indexes[i]]
     next i
     * Use
     * /xl 10m 3.5
     * for 10mA to 3.5 A horizontal axis
     Plot /xauto /yl 0 100 /ylabel Efficiency /xlabel "Load Current"
/yunit "%%" /xunit "A" /name "Efficiency" effvector LoadCurrent
endif
```