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Stoyan Stoyanov, *Senior Member, IEEE*, Chris Bailey, *Senior Member, IEEE*, Paul Stewart, Mike Parker and John Roulston

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Experimental and Modelling Study on Delamination Risks for Refinished Electronic Packages under Hot Solder Dip Loads

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***Abstract* – For electronic packaging engineers in the high reliability sectors such as aerospace, defense, oil & gas, etc., the use of commercial off-the-shelf components offer significant advantages due to their high availability, fast delivery time, and low cost. However, these components pose significant reliability challenges due to the risks associated with tin whisker formation and uncertainty on the long-term reliability of lead-free solders. To address these risks, the hot solder dip process is used to refinish the package by replacing lead-free solder finishes with lead-based finishes to meet the stringent packaging and assembly requirements for these sectors which are exempt from RoHS legislation. But the hot solder dip process is an extra process that exposes the package to an additional thermal load which will result in thermo-mechanical stresses that need to be properly understood and controlled. To address this challenge, a multi-disciplinary methodology combining thermo-mechanical models with "dip-to-destroy" experiments and Scanning Acoustic Microscopy has been developed to identify the risk of package material delamination for a number of package designs. Results show that the developed models can predict delamination risks for a range of imposed thermal gradients. Electronic package designs with a direct heat path from dipped terminations to internals of the package show a higher risk of overstress-induced delamination, and this failure is generally driven by the high temperature excursion above the glass transition point of the molding compound. The novelty and significance of these findings is that the derived methodology can be used by electronic packaging designers to optimize the thermal parameters of the hot-solder-dip process so that subsequent refinished packages can meet the stringent high reliability requirements for these sectors.**

***Index Terms* — Finite Element Modelling, Reliability, Component Terminations, Hot Solder Dip Refinishing Process, Tin Whiskers, Commercial Off-The-Shelf Components, Scanning Acoustic Microscopy.**

ACRONYMS

D2D	Dip-to-Destroy
C-SAM	C-Mode Scanning Acoustic Microscopy
THRU-Scan™	Through transmission imaging
COTS	Commercial Off-The-Shelf
rHSD	Robotic hot solder dip
EMC	Epoxy molding compound
IC	Integrated Circuit
PQFP	Plastic Quad Flat Pack
LQFP	Low Profile Quad Flat Pack
TQFP	Thin Quad Flat Pack
TSSOP	Thin-Shrink Small Outline Package
TO	Transistor Outline
CT	Computed tomography
CAD	Computer-aided design[2]

I. INTRODUCTION

ELECTRONICS manufacturers of equipment and systems used in high reliability, long service life, and safety critical applications are increasingly relying on the use of lead-free packaged, commercial off-the-shelf (COTS) components. Lead-free assemblies are prone to high reliability risks related to short-circuit malfunctions caused by tin whisker growth [1]. To mitigate these risks, Aerospace, Defense and High Performance (ADHP) equipment manufacturers have adopted a post-manufacture processing practice known as hot solder dipping (HSD). This process removes tin or tin-rich coatings from component terminations and replaces those with tin-lead solder finishes (known as backward conversion) [2,3].

The HSD approach was originally developed as a manual "hand dipping" technique, but in recent years this has migrated to a fully automated, robotically controlled process available from a limited number of suppliers. An example of such a process, developed by Micross Components Ltd, is shown in Fig. 1 [4]. When lead-free legislations were introduced initially, the HSD was adopted mainly in the (forward) conversion of package terminations from tin-lead to lead-free solder finishes. Today the refinishing is predominantly used for backward finish conversion to allow for lead-free packaged COTS components to be readily used in high reliability and safety critical electronic systems which are exempt from RoHS legislation.

An experimental programme carried out under the Transformational ManTech Research Project S1057 [5] assessed the effect of the hot solder dip refinishing process on a range of 23 part types, with varying package and die dimensions as well as pin count and pitch sizes, representing several common package configurations such as Small Outline Packages (SOP), Plastic Quad Flat Packs (PQFP), Plastic Transistor Outline (TO) and Plastic/Ceramic Dual Inline Packages (CERDIP and PDIP). Focused specifically on

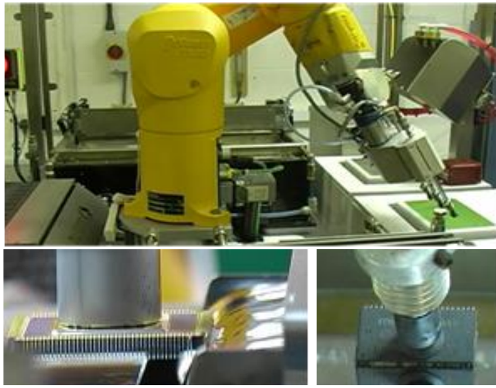

Fig. 1. Robotically controlled hot solder dipping at Micross Components [4].

assessing the susceptibility to thermo-mechanical damage of the tested electronic packages, this study confirmed that overall normal refinishing processes, as guided by ANSI/GEIA-STD-0006 standard [3], will not damage most leaded component constructions [5,6]. However, some of the part-types in this study, namely fine-pitch < 0.65 mm TSSOP, PQFP and TQFP, and TO-220, have shown damage issues (e.g. shifts in electrical performance attributed to detected internal delamination) post-refinishing and/or after subsequent environmental testing [6]. While the results from this study gave some assurances to industry, it also showed that with some packages their suitability for refinishing cannot be taken for granted. Components should be deemed as being appropriate for hot solder dip post-processing following a careful consideration of their package type and internal design, and evaluations from physical testing. Despite the value of this work, there is a continuing lack of knowledge and understanding about the safety margins associated with the "standard" hot solder dip process conditions and sensitivities of package design to thermally induced stresses and the risk of delamination within the internal package construction.

Apart from the study referenced above, there is to date limited published research on the hot solder dipping process. Subbarayan *et al*. [7] studied the conversion of pure tin finish to tin-lead (SnPb) and lead-free finishes (SnAgCu and SnAg) as well as the conversion of SnPb finish to lead-free SAC (SnAgCu) finish by solder dipping but only in the context of the resulting pull strength of the solder joints for assembled leaded components. Wang *et al.* [8] reported results from a similar investigation on the solder joint reliability of lead-free SAC solder refinished components under temperature cycling test. In related work, Mathew *et al.* [9] studied the effectiveness of solder dipping on preventing tin whisker growth using the SnPb solder and lead-free solders.

With regards modelling, Winslow *et al.* [10] developed thermal models to predict the thermal gradients in a single dip refinishing process and identified the important role of pre-heating of the package to minimize process related thermal gradients. This is an important issue as IC manufacturers stipulate that the packaged IC should not to be exposed to thermal gradients greater than 3C°/sec. Validated thermal models enabling accurate simulation of the transient behavior of an electronic component under the complete sequence of a robotic double dip refinishing process steps have been also reported [11]. However, thermo-mechanical models for predicting stress in packages subjected to solder dipping and relating such predictions to overstress failure risks have received very limited attention to date [12,13].

Validated thermo-mechanical models of electronic packages that predict their mechanical behavior during the hot solder dip process will provide electronic packaging engineers with a tool that will mitigate against risks of damage to the package when subjected to thermal gradients imposed by this process. This paper details a methodology, combining experimental results with finite element modelling, aimed at predicting the stresses that refinished components endure before showing signs of delamination failure under solder dip loads. The experimental study, termed "Dip-to-Destroy" (D2D), is based on a series of solder dip tests aimed at inducing graded delamination in the tested components. Components are examined using Interface Scan (C-SAM) and THRU-Scan techniques to confirm their initial (virgin) and post-D2D status.

Thermo-mechanical finite element modelling of packages subjected to D2D thermal loads is performed in parallel. Model predictions for interfacial stresses are used to formulate a stress-based delamination failure criterion and through correlation with C-SAM results to derive interfacial strength limits for the critical package interfaces - identified to be between the epoxy molding compound (EMC) and the copper lead-frame/ thermal pad. This work demonstrates that the developed methodology and its capability to predict stress under solder dip conditions, validated against experimental data, can be used as an effective and cost efficient approach to assess safety margins and the susceptibility to interface delamination of an electronic component under applied refinishing process loads.

II. Hot Solder Dip (Refinishing) Process

Refinishing is a fully automated process where a component is picked and held by a robotic arm, and then taken through a sequence of process steps to remove tin-rich finishes that are a reliability risk. In a typical process, the package is first picked with the robot arm and assessed for positioning. It is then taken to a flux bath and the leads or any exposed metal terminations that require refinishing are fluxed. Flux temperature is about 30°C. The package is then moved to a pre-heater and heated from ambient enclosure temperature (38-42°C) to 140°C under a closed-loop temperature control using an integrated pre-heater IR sensor. Based on these IR readings, the heat is controlled so that the ramp rate of pre-heating does not exceed 3°C/sec. The package is then moved to the solder reservoir (bath). In a sequence, the leads on each side of the package, or any other component-dependent termination, are dipped in the molten solder bath. This step is undertaken under an inert nitrogen blanket. The molten solder is typically maintained at 250°C and the time of dipping each leaded side is 3 seconds.

In a double-dip hot solder dip process, the package is taken for a second time to the flux bath where in a similar way the leads at each side are fluxed. During these steps, the package cools down, hence a second pre-heat is required to heat the

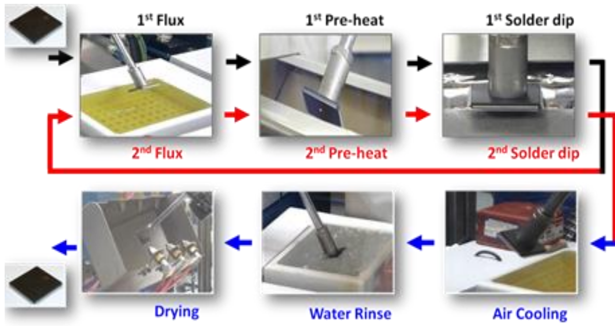

Fig. 2. Schematic of double-dip HSD process steps.

component from its current thermal state to 140°C. A second solder dip of the package leads then follows. The next steps in the process involve air cooling followed by a water wash. Drying the package then completes the process. Fig. 2 shows a diagram of the sequence of key steps in the hot solder double-dip process [4].

III. Experimental Study

Under the "Dip-to-Destroy" (D2D) experimental study, two representative package constructions were subjected to elevated (graded) thermal loads, by means of solder dipping, in order to induce thermo-mechanical stresses at different levels of severity. The objective was to establish the impact of these different thermal loads and which loads would induce delamination in the components. Insights into the failure modes and mechanisms associated with the applied dipping loads were also sought. From the point of view of package design, a primary aim was to evaluate any dependence on package vulnerability due to the design characteristics of the conductive heat path from the dipped termination to the IC die. Based on these characteristics, two package construction types are identified:

1. *Type 1 Packages*: These have a thermally enhanced construction which enables efficient heat dissipation from the encapsulated IC die to the outside of the package. Examples include gull-wing components with one or more leads directly connected to the die pad of the internal lead-frame, and also components with exposed thermal pads. Note that the exposed thermal pad will also need to be refinished in component constructions such as QFNs, TO, and Pentawatt packages (e.g. RR06 in Fig. 3). Such thermally enhanced packages are believed to be potentially more vulnerable to HSD processing.
2. *Type 2 Packages*: These have a construction that is not thermally enhanced. For example, gull-wing components, such as QFPs (e.g. SX08 in Fig. 3), that have lead-frame/die pad that is fully encapsulated. The connections between the die and the outer leads is solely via internal wire bonds. Hence, these packages have high thermal resistance between the leads and the lead-frame/die pad.

A. Tested Electronic Components

The two components selected for the D2D study are illustrated in Fig. 3, where the internal package structure (obtained with a computer tomography technique) is shown.

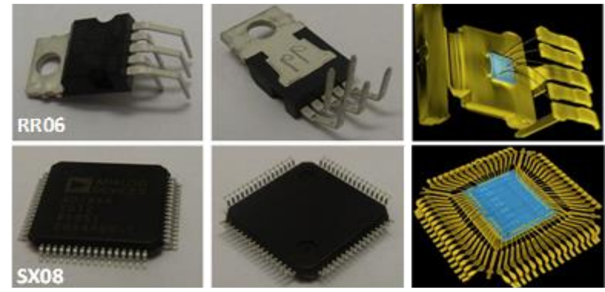

Fig. 3. RR06 (top row) and SX08 (bottom row) components. The first two images are actual package photos and the third image details the internal construction (3D CT scan).

The first component, referenced RR06, is a Pentawatt Audio Power Amplifier. This component has an exposed thermal (and die) pad, coarse geometry, and represents a silicon chip packaging extreme for the Type 1 packages. In terms of constructional design, this package is representative of a common class of electronic components such as power chips and covers a wide range of analog voltage regulator package constructions. An important attribute of this package is that it has a lead directly connected with the die pad. The die pad plays also the role of a thermal pad, with the bottom side being externally exposed (see Fig 3). Hence, it is an excellent example of a component type with a direct heat path between the leads/thermal pad and IC die.

The second component (Type 2 package), referenced as SX08, is a Low-Profile Quad Flat Pack (LQFP) component representative of a common class of ICs such as memory, processor, etc. This Analog-to-Digital Converter (ADC) carries an interesting mix of precision analog and fast digital technology. The IC is an example of a package constructional design with heat path via wire bonds only between the package leads and the internal lead-frame die pad/IC die.

Important specifications and constructional dimensions of these two packages are summarized in Table I.

TABLE I
Package Specifications

Ref	Package Type	Pin count	Pitch (mm)	Package Size (mm) [a]			Die Size (mm)		
				L	W	t	L	W	t
RR06	Pentawatt	5	1.7	10.2	9.2	4.8	1.9	1.5	0.25
SX08	LQFP	64	0.5	10.0	10.0	1.40	5.5	4.45	0.34

[a] L = length, W = width, t=thickness.

The D2D experiments were designed to induce graded thermal loads (low to high) and respectively graded delamination in the tested parts. The thermal load is achieved by means of hot solder dip. The graded loads are obtained by setting, with each experiment, the following three hot solder dip load parameters:

- Solder dip time: 3, 9 and 25 sec.
- Molten solder bath temperature: 260°C, 290°C, 325°C, 360°C and 400°C.
- Thermal loads with and without preheat of the component, prior to applying the actual solder dip, are investigated. The preheat condition involves heating the component from room temperature to 140°C at a rate of 3°C/sec.

Not all combinations of the above thermal load parameters are implemented and experimentally tested. Instead, a judicious approach has been used to identify a selection of tests that are considered most important and expected to maximize the information and data generated in the experimental study. In particular, the main interest was to discover which elevated solder dip conditions are causing delamination in the internal layered structure of the parts. The test loads are detailed in Table II along with the respective sample size of tested components.

TABLE II
EXPERIMENTS PLAN OF D2D STUDY

Thermal Load Profile	NO-preheat Dip time: 25 sec		PREHEAT Dip time: 9 sec		NO-preheat Dip time: 9 sec		PREHEAT Dip time: 3 sec		NO-preheat Dip time: 3 sec	
	Part Ref / Batch size		Part Ref / Batch size		Part Ref / Batch size		Part Ref / Batch size		Part Ref / Batch size	
Solder temp. /°C	RR06	SX08	RR06	SX08	RR06	SX08	RR06	SX08	RR06	SX08
400	4	4			4	4			4	4
360									4	4
325	4	5	5	5	4	5			4	5
290			6	8	6	8			6	8
260	6	5	6	8	6	8	6	8	6	8

All D2D tests are undertaken using robotic hot solder dip equipment. It should be noted that the thermal load profiles in Table II are graded and more extreme than a standard hot solder dip process specification. Only one profile in the table, the least severe preheat test with solder dip time and temperature of 3 seconds and 260°C respectively, can be considered as being close to a standard solder dip condition. In all D2D tests the solder dip is followed by cooling of the components down to room temperature.

The dipped terminations for each of the two component types are illustrated in Fig. 4. For RR06, standard refinishing would require solder dip of both the exposed thermal pad and the leads of the package, which means the resulting thermo-mechanical effects will be cumulative, from two separate hot solder dip loads (for the thermal-pad and the leads respectively). The hot solder dip load on the thermal pad is the most extreme in terms of heat transfer. Hence, the D2D tests for RR06 (Table II) were based on solder dipping the exposed thermal pad only. The thermal pad was dipped in solder to the depth of the metal tab. The leads were not dipped. This overall dip strategy for the RR06 package provided a more robust approach to inducing measurable and graded delamination in these components.

In the case of the SX08 package, the leads at one side of the package are dipped. The shown temperature contours, obtained from validated thermal models [11], are for illustration only. Note that for the RR06 package, the central pin will be notably heated as a result of being directly connected to the hot solder dipped thermal pad (see Figs. 3 and 4).

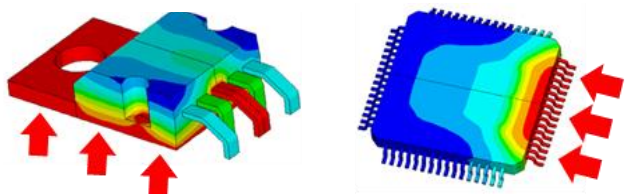

Fig. 4. Model-based illustration of the package termination where the solder dip is applied (indicated by arrows) in the experimental D2D study: RR06 (left) and SX08 (right). Contours for illustration only, showing high (red) and low (blue) temperature regions in package under D2D solder dip load.

Moisture present at the epoxy-based interfaces of plastic IC packages can lead to popcorn failures/delaminations at these interfaces. For the hot solder dipping process, moisture controls are defined based on the IPC/JECED J-STD-033 standard. The package drying conditions achieve moisture levels of less than 5%RH within the floor life (i.e. the soldering process window) in the case of circuit card assembly. To ensure moisture is not a factor in the undertaken D2D tests, the team went further than required by the J-STD-033 and baked the parts for > 6 days at 125°C. After this, the oven was reduced to do a stabilisation bake at 50°C for a couple of hours before the actual D2D processing. All parts were then subjected to the D2D processing within a 90-minutes period from removal from the oven.

B. *Experimental Results*

Prior to the D2D tests, all components were examined using C-Mode Scanning Acoustic Microscopy (C-SAM) to confirm their initial no-damaged status. C-SAM is also used to assess the post-D2D state of all components in order to confirm if any measurable delamination has been induced. The C-SAM examination in this study is performed by SonoLab, a division of SonoScan [14]. The components were inspected with C-SAM at operating frequencies of 15MHz and 50MHz, and 50 microns resolution. Both Interface Scan and THRU-Scan techniques are utilised to analyse each of the two package types.

In an Interface Scan image, induced delamination creates negative echoes and appear red or yellow, while bonded areas create positive echoes and appear grey. Areas in which no ultrasound is returned appear black. THRU-Scan is based on propagating ultrasound throughout the entire thickness of the sample. The images appear as shadow graphs that display the internal features of the components. Bright areas in the images indicate high ultrasonic transmission, which indicates bonding and material continuity. Defects, such as voids and delamination, block the transmission of ultrasound and appear black in the images. Fig. 5 shows an example of post D2D state of a SX08 component revealed through Interface Scan and THRU-Scan CSAM techniques.

The D2D experimental study was successful as it achieved, as intended, measurable and graded delamination under some of the thermal solder dip-to-destroy profiles. Not surprisingly, higher solder temperature and higher dip time increase the risk of delamination, both individually and in combination.

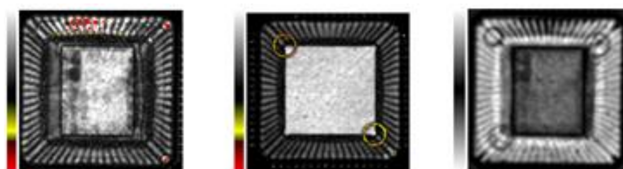

Fig. 5. Interface topside scan (left), Interface backside scan (middle) and THRU-Scan (right) images of a SX08 component showing measurable delamination at the leads interfaces at the package side caused by a single sided dip-to-destroy, elevated stress-promoting hot solder dip thermal load.

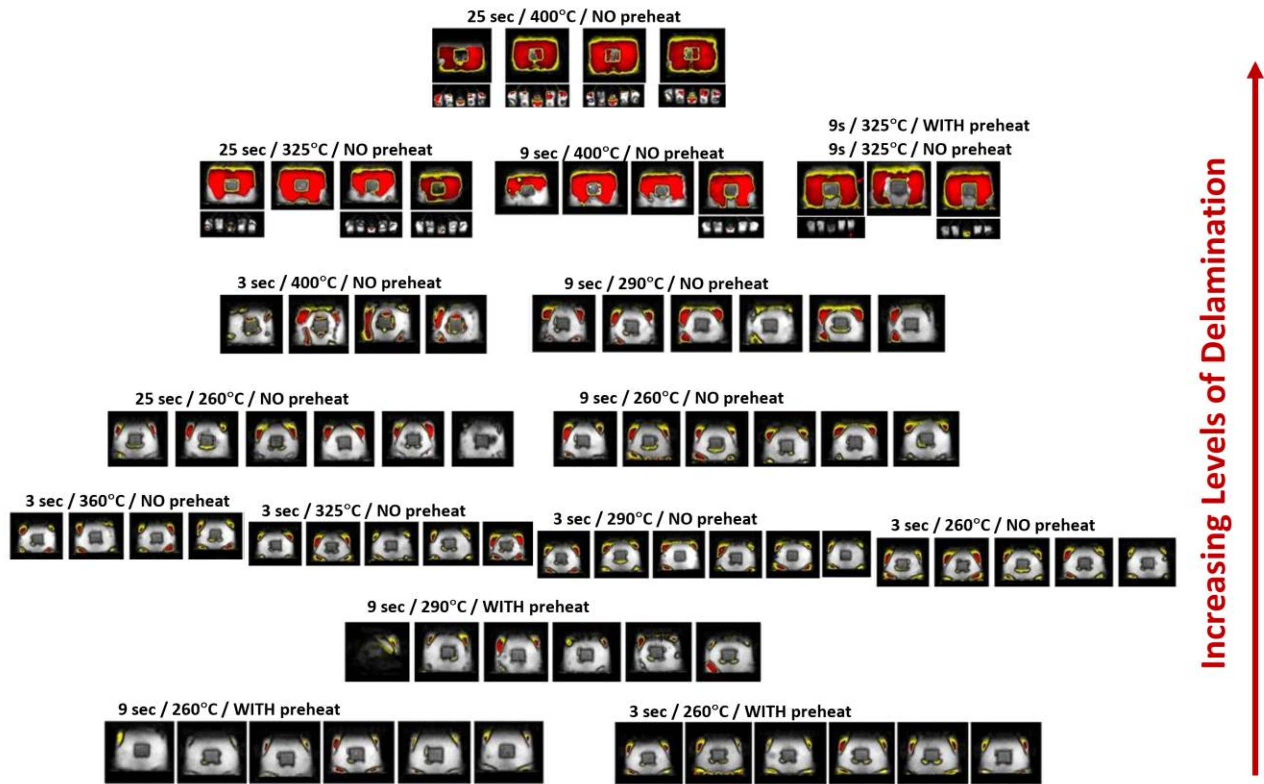

Fig. 6. Delamination failure tree ranking the states of RR06 components after D2D tests. Representative C-SAM images are used to show the impact of each thermal profile. Labels of images specify the hot solder dip load condition in the format: solder dip time / solder temperature / with or without preheat.

Type 1 packages pose a higher risk of overstress-induced delamination. Fig. 6 details the Interface Scan C-SAM images of RR06 components after D2D, showing the encapsulated region of the thermal pad/IC die domain of the package. If delamination has also occurred in the leads' interfaces, then these C-SAM images are also included in Fig. 6. This figure provides a diagram constructed in the form of a delamination failure tree. The C-SAM images at the top are for the parts with highest delamination, and the least delaminated components appear at the bottom of the diagram. The label above each image details the hot solder dip load condition given in the format: solder dip time / solder temperature / with or without preheat (for example: 25 sec / 400°C / NO preheat).

The defects found in the interface scans were confirmed independently by THRU-Scan image results. As evident from the C-SAM results, measurable delamination is found at the interface between the dipped thermal pad and the package molding compound. Only the most extreme thermal load profiles caused stresses that exceeded the respective interfacial strength limits at the leads/molding compound interface and at the die/molding compound interface.

Type 2 packages (e.g. SX08) pose a lower risk to delamination. Only four thermal load profiles (the profiles with 400°C solder temperature and the profile 25sec/325°C) developed signs of delamination at the lead/molding compound interface. This can be explained by the thermal path which is in the form of wire bonds only. It prevents substantial heat transfer into the package body occurring. But, under elevated temperature loads the dipped leads undergo thermal shock that is extreme enough to cause delamination at the lead/molding compound interface. Due to very limited thermal conduction from the dipped leads into the package internals (caused by the wire bonds and high thermal resistance molding compound gap, see SX08 in Fig. 3), no delamination is observed at die or die attach interfaces.

Fig. 7 shows the results from C-SAM for SX08. This figure references only the profiles that have caused observable delamination. As no delamination is found with the remaining test conditions, these are not detailed in the figure and should be considered as loads where no difference (i.e. no delamination), is detected when comparing the parts' pre- and post- D2D state.

Because of the moisture controls and baking of the parts prior to their D2D processing, it can be asserted with a high degree of confidence that there is no moisture effect in the delamination failures reported in Figs. 6 and 7. The delaminations induced in the two component types are therefore attributed to the differential multi-material coefficient of thermal expansion miss-match. For this reason, the models discussed in the next sections of the paper focus on modelling the delamination risk due to CTE miss-match induced thermal stresses as opposed to other potential factors such as the moisture induced delamination through popcorn mechanisms.

The main conclusion from the D2D experimental study is that the design construction of the package has an impact on the conductive heat path from dipped terminations to package internals. This is the main factor that determines the package susceptibility to delamination under solder dip loads, where:

- Type 1 packages provide greater heat transfer into the internals of the package and hence greater susceptibility to

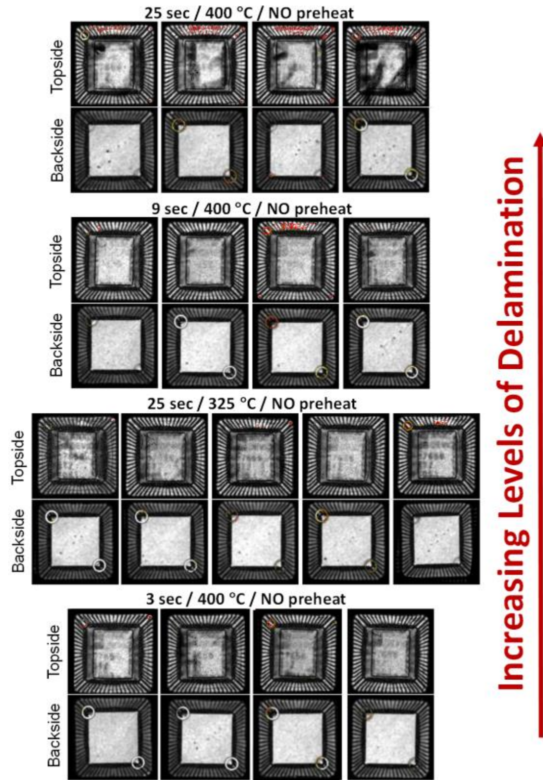

Fig. 7. Delamination failure tree showing the state of SX08 components with observable delamination after D2D tests. No delamination was found with all other D2D test conditions detailed in Table II (hence components under these tests are not shown in the figure). Selected representative C-SAM images are used to show the impact of D2D thermal conditions causing delamination.

overstress-induced delamination. This is the case for the RR06 package where measurable delamination is observed which, with some of the least severe D2D profiles, may be acceptable within the J-STD-020 standard [15].

- Type 2 packages with dipped terminations (i.e. the leads) not connected directly to the internal lead-frame/die pad, such as is the case of the tested SX08 component, have risk of delamination at the dipped lead interfaces but to induce such failure would require substantially elevated process conditions (long dip time and/or high process (solder) temperature).

IV. FINITE ELEMENT THERMO-MECHANICAL MODELLING

The modelling element of the study focused on assessing the capability of developed thermo-mechanical models to predict overstress-induced delamination in components subjected to D2D thermal load profiles. The objectives of the modelling work are three-fold:

1. Develop thermo-mechanical models: These models of the hot solder dip process build upon our previous work where validated thermal models for the hot solder dip process were developed [11].
2. Validate model results and confirm the hypothesis that package type 1 is more susceptible to delamination: The validated finite element models are used to identify interfacial strength limits in relation to the delamination failure mode identified using the C-SAM data.
3. Define a methodology that can be used to ensure that the solder dip process is safe and if required can be optimized so that stress related delamination failure risks are eliminated for different package types.

A. *Thermo-Mechanical Models*

Three-dimensional thermo-mechanical models for both package types were developed using the ANSYS simulation software [16]. Due to half symmetry in both packages, the models are developed to represent only half of the package geometry, with standard boundary conditions applied on the symmetry plane (i.e. for thermal: heat flux zero, and for mechanical: zero displacement in the perpendicular for the symmetry plane direction). For the thermal analyses, the package is meshed with the ANSYS 8-node thermal solid element type SOLID70. For the stress analysis the element type is SOLID185. The mesh sizes of the RR06 and SX08 models are 28,264 and 60,608 respectively. The half symmetry models with the mesh of the two packages are shown in Fig. 8.

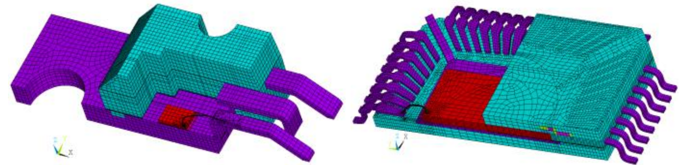

Fig. 8. CAD and mesh models of RR06 (left) and SX08 (right) – half symmetry representations of the two packages. EMC mesh domain is partly removed (not visualized) in the images to reveal the internal package features included in the models (e.g. die, die attach, representative wire bond, lead-frame).

All 32 experimental tests detailed in Table II are simulated. The thermal analysis is based on the validated hot solder dip process modeling approach in [11]. Each simulation captures the transportation of the dipped component, held by the robot arm, from the storage tray to the solder bath. As this step takes 3 sec, the actual dipping when no pre-heat is used starts at simulation time 3 sec. After the completion of the solder dip, the component is taken away from the solder bath and cooled down to room temperature. These predicted temperature profiles are used as the thermal loads in the subsequent stress analysis.

The stress-free temperature for the package is set to 110 °C which corresponds to the lower bound of the glass transition temperature (Tg) range for the EMC encapsulation. For the stress calculations, the applied thermal load is defined as a combined profile of: (1) isothermal load from the stress-free temperature 110°C to room temperature (to account for any post-packaging residual stress) and (2) the D2D test thermal load obtained from the thermal analysis.

The finite element analyses assumed the material data and material constitutive laws detailed in Table III. The EMC is modeled with visco-elastic behavior using the time-temperature superposition principle (TTS), stress relaxation master curve obtained from a range of relaxation curves at different temperatures and an associated Prony series model for the EMC stress relaxation [17]. As a result of implementing the EMC visco-elastic behavior model, the elastic modulus of the

TABLE III
COMPONENT MATERIAL DATA FOR FINITE ELEMENT ANALYSIS OF D2D TESTS

Package Material	Density ρ (kg/m^3)	Thermal Conductivity k (W/m.K)	Specific Heat Cp (J/kg.K)	Elastic Modulus E (GPa)	*CTE* (10^{-6} ppm/K)
Epoxy Molding Compound (EMC) (Tg range 110-140 °C)	2020	0.72	794 @ 20 °C 1190 @ 125 °C 1420 @ 250 °C 1420 @ 400 °C	Visco-Elastic Behavior, E(t,T), using Prony Series Model for the stress relaxation master curve [17]. Illustrative modulus values at *t*=0 sec: 16.6 @ 20 °C | 16.5 @ 110 °C 7.2 @ 150 °C | 2.9 @ 185 °C 1.3 @ 250 °C | 0.7 @ 400 °C	12.0 @ 20 °C 15.0 @ 110 °C 35.0 @ 140 °C 40.0 @ 250 °C 40.0 @ 400 °C
Copper	8900	380	385	120.0 @ 25 °C 110.0 @ 250 °C | 110.0 @ 400 °C Plastic Behavior Model: Bi-linear hardening: yield stress 172 MPa; tangent modulus 1065 MPa	17.0
Silicon	2330	146 @ 20 °C 99 @ 125 °C 76 @ 250 °C	712	131	2.8
Epoxy with Ag particles (Tg = 80 °C) / SX08 Die attach /	3560	2.1	714	0.80 @ 20 °C 0.05 @ 250 °C 0.05 @ 400 °C	31.0 *below* Tg 150.0 *above* Tg
Pb (Melt @ 327.5 °C) / RR06 Die attach /	11,350 @ 25°C 11,150 @ 200°C 10,600 @ 400°C	33	128.7 @ 25 °C 136.8 @ 227 °C	14.0 *below* Melting Point 0.014 *above* Melting Point	29.1
Gold (wire bonds)	19,320	310	129	77	14.2

molding compound is not only temperature-dependent but also time-dependent. The values for the EMC elastic modulus in Table III at *t*=0s are for illustration of the Prony series model and do not represent piece wise linear variation of this property. Copper has elastoplastic behavior captured with the use of the bi-linear hardening plastic model. These material models are standard in ANSYS. Remaining materials are assumed elastic with temperature dependent properties as detailed in Table III.

The visco-elastic model accounts for the softening and the stress relaxation with time of the EMC at a given temperature. This captures implicitly the weakening in the chemical cross-linking in the epoxy at the EMC regions in the vicinity of the hot solder dipped terminations. With the most severe D2D tests the temperature in these regions becomes >300°C. The adhesion strength of the molding compound is therefore expected to reduce because of the thermal degradation of the bonds in the epoxy structure. Due to unavailability of EMC thermal degradation characterization it was not possible to establish explicitly in the study the temperature-dependent adhesion degradation of the EMC at such high temperature regimes. Instead, the methodology outlined in the next sections adopts the approach of obtaining the delamination strength limits implicitly through empirical correlation of the predicted stress using FEA and the experimentally observed delamination.

All modelling results from the finite element simulations are transient. Time steps are user controlled, where same time-steps are used for both thermal and stress analysis. This was done to ensure results are not influenced by the transient time step setup. As a reference, time step of 0.05 sec was used for the simulation of the hot solder dip phase of the thermal load. The thermo-mechanical analyses generated transient predictions for temperature, displacement, strain and stress.

Published work on reflow processing [18,19] clearly identifies delamination as a major concern and the most likely failure mode of electronic packages under temperature loads. In the context of the hot solder dip thermal loads, delamination is also deemed to be the critical failure mode for certain package types. This has been confirmed with the ManTech Research Project findings [5,6]. Hence, the proposed stress-promoting dip-to-destroy experiments aimed at the same failure mechanism (overstress) and mode as observed with the C-SAM delamination results detailed in Figs. 6 and 7. Therefore, the discussion presented here provides details for the modelling capabilities to predict the interfacial stresses due to a one-off D2D thermal load application and the formulation and validation of a stress-based delamination failure criterion for the EMC to lead-frame/pad interfaces in the packages.

Different approaches are available for delamination damage modelling including statistical thermodynamics [20], fracture mechanics methods [21], energy-based methods [22], stress-based methods [23, 24], and plasticity damage models. Respective methods have different advantages and limitations. For example, with strain energy density methods, the energy density is compared against a limiting value for an interfacial location of interest without the requirement to presume an existing crack. The key challenge is the availability/generation of constitutive material laws and/or traction-separation constitutive laws for the interface layer for the FE model. These are not readily available and are epoxy material dependent. The fracture mechanics methods are suitable to examine the crack propagation and regarded as accurate but still require difficult to gather data for energy release rates and critical values as well as knowledge for the initial existence, location and size of the delamination. The inclusion of fracture mechanics methods in three-dimensional FE modelling is also challenging particularly

in the case of IC packages with complex designs. In general, delamination damage models aim to capture cumulative load effects and to predict the evolution of delamination cracks.

At a continuum length scale, the adhesion strength of the bi-material interface characterizes the susceptibility of the interface to delamination under an applied stress field. Given the focus in this study was on the delamination failure occurrence under a one-off thermal load application, consideration was given to a simple stress-strength conceptual delamination failure criterion over the more sophisticated energy-/entropy-based delamination progression damage modelling approaches which capture the decohesion physical phenomenon under cyclic loading over time. Unlike fracture mechanics and thermodynamically consistent damage models that require parameter values and data not readily available, a stress-based failure criterion is easier to use by designers since the stress distribution is directly available from the finite element calculations. Stress-based methods have been demonstrated successfully, particularly for the problem of delamination onset modelling [23,24,30], and reported to provide good correlation to respective experimentally observed delamination in packaged IC devices [25-27].

During application of dipping loads, bi-material interfaces are subjected to complex patterns of stress that are not well understood but carry the risk of delamination. Given that a high temperature dip load typically puts the package internal structure in compression as a result of the high CTE of the EMC at temperature above Tg, it is considered that the maximum shear component of the stress field is what drives the initiation and propagation of delamination cracks.

After analyzing different alternatives for the definition of a stress-based parameter for delamination risk assessment, the stress intensity (σ_I) levels in the interfacial layer of the epoxy molding compound with the internal metal structure (i.e. the copper lead-frame) is selected and used. The stress intensity σ_I is defined as the maximum difference, in absolute terms, between the principal stress components, i.e.

$$\sigma_I = max\{|\sigma_1 - \sigma_2|, |\sigma_2 - \sigma_3|, |\sigma_3 - \sigma_1|\} \qquad (1)$$

where σ_1, σ_2 and σ_3 are the principal stresses. The stress intensity σ_I is directly related to the maximum shear stress τ_{max} [16], i.e.

$$\sigma_I = 2\tau_{max} \qquad (2).$$

It should be noted that stresses predicted using FEA are mesh dependent in layered packaging, particularly in linear elastic analysis [28]. To address this, averaging procedures are typically used for stress-based [23,30] failure predictions to avoid stress singularities at interfacial edges/corners and mesh effects. Averaging is also used for energy-based [29] damage and failure predictions to avoid mesh effects.

In our study, the mesh elements at both sides of the EMC/metal interfaces (identified as having risk of delamination) are defined in a geometric layer that has thickness t_l. The location where delamination failure is assessed is defined with an interfacial area A_{loc} at that location. The volume given with EMC interfacial mesh elements enclosed within A_{loc} and within the interfacial layer with thickness t_l is denoted V_{loc}. Then, the local averaged stress-based parameter, denoted σ_{AVE}, at the interfacial location of interest is calculated as:

$$\sigma_{AVE} = \frac{1}{V_{loc}} \int_{V_{loc}} \sigma_I dV \qquad (3)$$

where σ_{AVE} is the volume weighted average of the stress intensity results over the interfacial mesh elements associated with V_{loc}.

In this study, the averaging stress calculations using (3) utilized t_l=0.05 mm and A_{loc}=0.04 mm^2 which were judged to be appropriate given the lead-frame/ thermal pad interfacial dimensions of the two analyzed components. The averaged stress intensity calculation for σ_{AVE} ensures that any stress singularity fields which may occur at the bi-material interface edges/corners are not affecting the delamination assessment predictions.

The general qualitative trend is that the models are capable of predicting the graded delamination caused by the graded solder dip thermal loads, and are in good agreement with the C-SAM diagrams reported with Figs. 6 and 7. For example, Fig. 9 shows the stress intensity contours at the interface between the molding compound and the copper leads at the SX08 solder dipped package side under three of the D2D test conditions with 25 sec solder dip and temperatures for the solder bath of 400°C, 325°C and 260°C respectively. The stress contours refer to the state of the interfaces of interest at the end of the 25 sec. dip step. In each figure, there is also a representative C-SAM image of the package under the same load condition. Given the C-SAM data, the models are found to provide very good spatial predictive capability for the regions of interfacial stress concentration.

In a similar way, the stress intensity observations are performed at the mold compound interfaces to the copper internal structure for the RR06. Fig. 10 illustrates the stress contours at the thermal pad/leads to EMC interfaces where delamination failure was most likely to occur. It has already been noted that the D2D load is applied to the exposed thermal

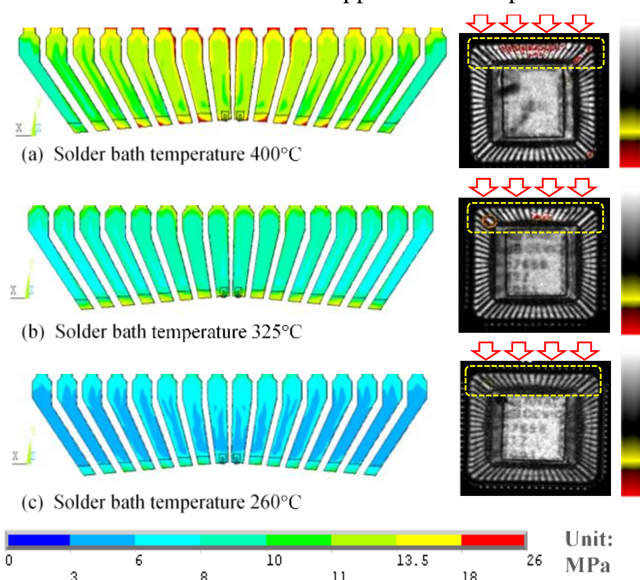

Fig. 9. Model predictions for stress intensity at EMC to copper leads interface for SX08 package under single sided solder dip load with 25 sec dip duration and solder temperature (a) 400°C, (b) 325°C and (c) 260°C. Images on the right show representative C-SAM results under respective load profiles.

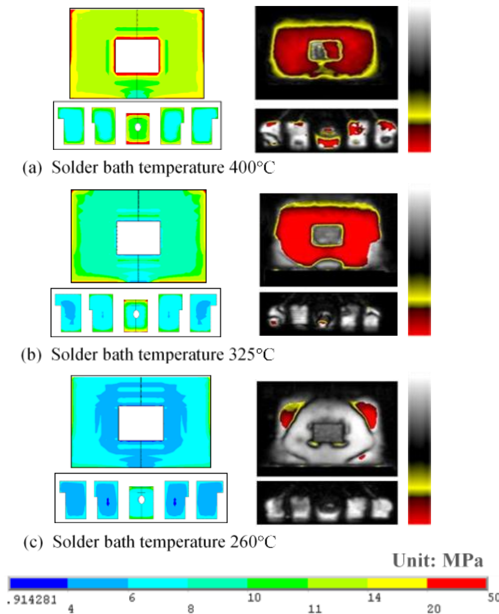

Fig. 10. Model predictions for the stress intensity at EMC to copper thermal pad/leads interfaces for RR06 package under solder dip of the component thermal pad, with 25 sec dip duration and solder temperature (a) 400°C, (b) 325°C and (c) 260°C. Images on the right show representative C-SAM results under respective load profiles.

pad of the package and not the leads. Also, the central lead of the package is directly connected to the thermal-pad tab thus having direct heat conductive path with the dipped thermal pad. The other leads are encapsulated with the molding compound and connected only with bond wires to the die.

Based on the way the thermal load for the D2D is applied, it is not surprising that the interfaces at the metal thermal pad experience higher stress intensity levels compared with the leads. Analyzing the stress responses at the package lead interfaces, it is also evident from the model results that the central lead is the one which is most stressed. Package stress responses are well captured both qualitatively and quantitatively. For example, the model-experiment comparison illustrated in Fig. 10 shows that predicted interfacial stresses and spatial stress distribution from the models agree very well with the observed graded delamination found in the respective C-SAM reference images.

B. Intrefacial Stress-Strength Relations above and below Glass Transition Temperature of EMC

Delamination failure assessment due to dipping loads using stress-based criterion predictions requires some additional observations. With solder temperature in the range 260-400°C for the D2D load profiles, the solder dipping step results in positive thermal load in the context of the EMC glass transition temperature range 110-140°C and the associated with it stress-free state of the packages. Similarly, the cooling phase of the profile, which brings the package to room temperature, results in the application of a negative thermal load.

An important observation is that at high D2D test temperatures the EMC is above its glass transition temperature. At room temperature the EMC obeys elastic behavior, but at these high D2D temperatures, the material is in a viscous state and softens with modulus decreasing and CTE increasing as temperature rises. As already pointed, the adhesion strength at internal package interfaces is substantially lower at high temperature and much easier to break. Hence, lower induced stresses (as a result of the low EMC modulus) at higher temperatures can be also risky and cause delamination.

Our modelling results delivered a strong evidence that the stress intensity levels at high temperature, considered in the context of the viscous state and EMC modulus in the range of 1 GPa and below, are the main driver for the bi-material delamination detected at the interface between the molding compound and the copper lead-frame and/or leads. For example, Fig. 11 shows the averaged stress intensity (σ_{AVE}) results at bi-material EMC-to-copper lead location at the central lead of the dipped SX08 package side. The figure shows the stress curves for two different load profiles: (1) 25 sec dip step and solder temperature 400°C and (2) 25 sec dip step and solder temperature 260°C. While the averaged stress intensity result in cooling is very similar for both profiles, there is a big difference in the stress during the dip step, i.e. when the interfacial location is at high (>200°C) temperature. With the evidence from C-SAM examination that no delamination is created with one of these two profiles and substantial delamination with the other, it can be concluded that it is indeed the difference between the two stress profiles during the solder dip step that is the factor for inducing failure with one of the test conditions. Although these high temperature loads (shocks) are not representative of real hot solder dip profiles, these results helped to identify the stress levels that can cause observable delamination. If this occurs, then such delamination in the package when placed in the field will grow due to further temperature excursion and moisture ingress.

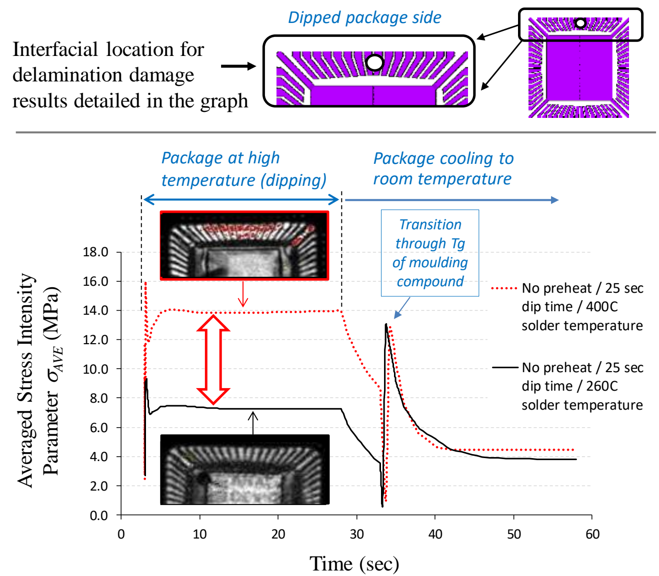

Fig. 11. SX08 model predictions of transient averaged stress intensity (σ_{AVE}) variation at the EMC-to-copper interface location at the central lead of the dipped package side (schematically shown at the top side of the figure).

Similar results for σ_{AVE} but at the EMC-to-copper interface in the case of the RR06 package are detailed in Fig. 12. The interfacial location is near the corner of the copper thermal pad.

Similarly, as with the SX08 analysis, the observation is that the stress intensity level during the dipping step is the main factor driving the delamination failure with the higher solder temperature condition. It should be noted that although in this instance there is also difference in the stress level at the latter stage of the two profiles, during components cooling and when the EMC is below its Tg, these stress values are of the magnitude of the package residual stress found at room temperature and prior to applying the dipping load profile (note all D2D parts had confirmed pre-dip delamination free state). Predicted absolute stress levels need to be considered having in mind the respective state of the EMC during the application of a D2D load (viscous vs. elastic, and different modulus of the EMC above and below the glass transition temperature range).

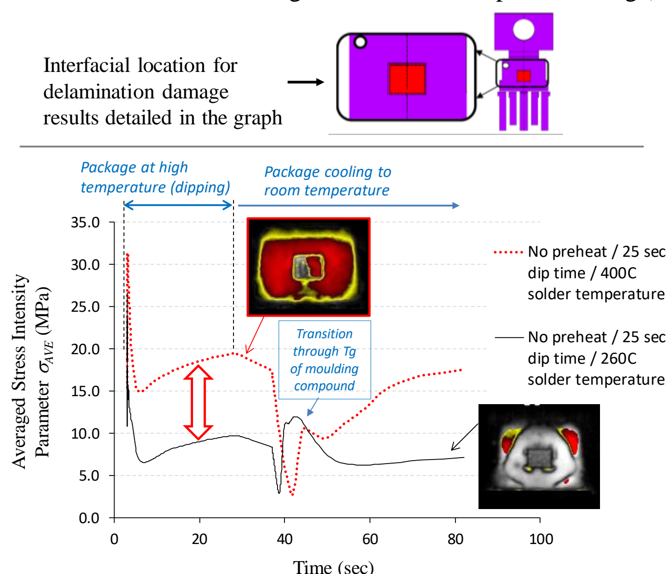

Fig. 12. RR06 model predictions of transient averaged stress intensity (σ_{AVE}) variation at EMC-to-copper interface location near the corner of the dipped thermal pad. Interfacial location for the graph results detailed at the top side.

C. *Correlation of Experimental and Modelling Results*

With the understanding that the high temperature excursion during D2D load application is causing the interfacial delamination initiation, an approach for correlation the model predictions for σ_{AVE} to delamination failure stress limit can be developed. A delamination failure parameter, σ_{MAX}, is defined as the maximum of the σ_{AVE} transient values predicted over the complete solder dip step following the very initial thermal shock instantaneous peak. This definition was found to provide the best model to C-SAM result correlation. Higher values of the delamination failure parameter σ_{MAX} are associated with greater risk of delamination at that location and vice versa.

A small subset, 6 out of the total 32 D2D test profiles, is used for model correlation. For a given dip time, D2D load cases that bracket most closely delaminated and non-delaminated states for the two tested packages, as revealed with the C-SAM, are identified and used. Using model predictions for σ_{MAX} at the C-SAM informed locations of delamination failure boundaries in the components under these specific dip load profiles, the following EMC-lead-frame adhesion strength limit, σ_{DL}, is defined:

$$\sigma_{DL}(t) = \begin{cases} 17.818t^{-0.2195} & ,3 \leq t \leq 9 \\ 13.503t^{-0.0933} & ,9 < t \leq 25 \end{cases} \quad (4)$$

where the strength limit is in unit of MPa and t is the duration of the solder dip time in seconds.

The reason for deriving σ_{DL} in (4) as function of the solder dip time is because no time-dependent interfacial strength degradation model and characterization data were available in this study. The adhesion strength limit relationship (4) is therefore empirically derived using the available C-SAM data and the model results.

D. *Validation of Model-Predicted Delamination Results*

Fig. 13 and 14 summarize the model results for the delamination failure parameter σ_{MAX} at the most critical delamination-wise EMC and lead-frame (or thermal pad) interfaces of RR06 and SX08 packages. In these diagrams, the model predicted σ_{MAX} values are plotted as offset values from the respective adhesion strength limit value σ_{DL}. As the horizontal axis in the graphs is moved at σ_{DL} failure stress level, a bar above indicates by how much the σ_{MAX} at the interfacial location of interest exceeds the delamination failure limit. This is indicative for occurrence of delamination failure. Graph bars pointing downwards from the level of σ_{DL} show the extent to which the predicted delamination failure parameter σ_{MAX} is below the critical failure limit.

The graphs summarize the results for all D2D profiles (i.e. thermal load conditions), and therefore also include the six profiles across all 32 tests for RR06 and SX08 used to correlate the models to the experimental data for the purpose of establishing the adhesion strength limit relation (4). These few profiles should not be seen as part of the validation but for completeness are included in the charts so that the full set of D2D model results is recorded. Each model result and prediction for delamination should be considered in conjunction with the actual experimental C-SAM Interface Scan (Figs. 6 and 7) and the THRU-Scan results.

Fig. 13 details the model predictions for the delamination failure parameter σ_{MAX} at interfacial location near the corner of the thermal pad of the RR06 component. Almost under all D2D profiles the models predict delamination happening at this location. The predicted σ_{MAX} values are lower for loads with smaller dip time and lower solder temperature but still above the failure limit (thus predicting delamination occurs) except for the two least extreme pre-heat profiles of the D2D at 260°C solder temperature (3 and 9 sec dip times). This is in excellent agreement with the C-SAM observations (refer to Fig. 6) for delamination at this interfacial location. C-SAM data suggest that with the above mentioned two pre-heat profiles some minor delamination is still possible at the thermal pad corners (may be acceptable within the J-STD-020 standard [15]).

In Fig. 14, the delamination failure parameter σ_{MAX} values for the SX08 package are calculated at the central lead interface with the EMC, as illustrated with the top side image of the figure. Modelling results show that only four D2D load profiles will cause delamination at that interfacial location. In the context of model validation, a very good agreement with the

CSAM data in relation to SX08 delamination in D2D tests is found (refer to C-SAM data discussed with Fig. 7). It should be noted that σ_{MAX} predictions close to the adhesion strength limit σ_{DL} are more uncertain.

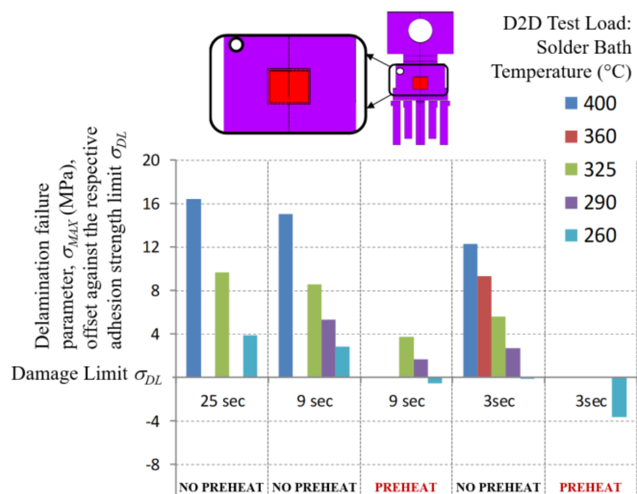

Fig. 13. Model validation for RR06. Delamination failure parameter σ_{MAX} predictions, derived for the range of D2D load conditions, observed at the high-risk package interfacial location at the corner of the thermal pad of the power chip. The σ_{MAX} values are offset against the delamination damage limit σ_{DL}.

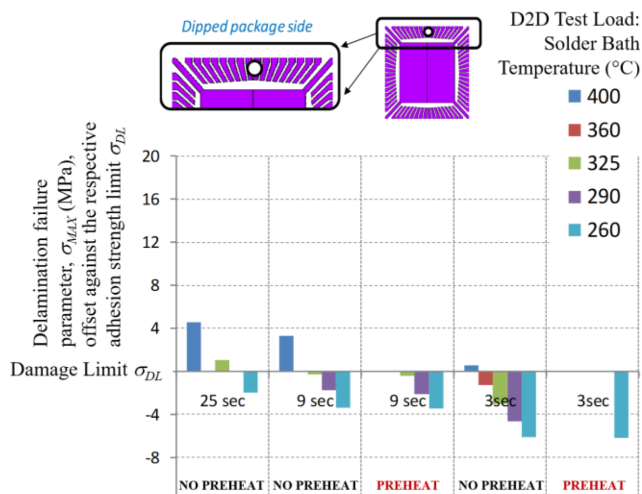

Fig. 14. Model validation for SX08. Delamination failure parameter σ_{MAX} predictions, derived for the range of D2D load conditions, observed at the high-risk package interfacial location found at central lead of the solder dipped side of this LQFP package. The σ_{MAX} values are offset against the delamination damage limit σ_{DL}. Dipping profile 3sec/260°C with preheat (closest to a standard refinishing condition) has safety factor of approximately 2X.

The reason why the pre-heat D2D condition reduces the delamination risk is explained with the effect it has on the spatial (and temporal) thermal gradients in the package body. The transient temperature predictions from the validated thermal models show that the no-preheat test loads cause notably different and more severe spatial thermal gradients compared to the equivalent load but preceded by a gradual 3°C/sec pre-heat of the package. Consequently, the severity of the differential CTE expansion of the package materials is different. The pre-heat condition aims to ensure the reduction of the thermal gradients and thus lowering the magnitudes of the induced by the CTE miss-match thermal stress.

E. Methodology

Adopting graded stress-inducing dip-to-destroy experimental tests, with failure detection C-SAM data, and thermo-mechanical models provides electronic packaging engineers with a methodology for assessing damage limits and safety margins for different component types under hot solder dip loads. In addition, it is also possible to establish damage sensitivities to solder dip conditions and to optimize the refinishing process. The proposed methodology can be characterized through the following steps:

1) *Package Characterization*: Internal geometry of the package type is gathered (e.g. 3D CT-Scan and datasheets).
2) *Material Characterization*: Material characterization is performed (e.g. Scanning Electron Microscopy with energy dispersive X-ray Spectrometry, SEM–EDX) and respective material properties are obtained.
3) *C-SAM Evaluation*: C-SAM evaluation, using Interface Scan and THRU-Scan images, of virgin-state parts (prior to D2D) to confirm their damage-free state.
4) *Perform D2D Tests*: D2D experiments undertaken on the investigated package type using damage-free parts.
5) *C-SAM Evaluation*: C-SAM results obtained with Interface Scan and THRU-Scan data for the post-D2D solder dipped parts. Graded damage observed, with both non-damaged and damaged parts identified.
6) *Develop Models*: Thermo-mechanical models developed for the D2D tests.
7) *Identify Failure Limits*: Using the model stress predictions and the failure data revealed with C-SAM, correlations for failure limits are obtained with respect to the defined model predicted stress-related delamination failure parameter.
8) *Identify Safety Margins/ Optimize Process*: Use the identified delamination failure criterion to assess safety margin for the package type, under the standard refinishing process. Use the model to optimize process conditions to reduce stress and thus mitigate against potential risks of damage where there is insufficient safety margin.

Using the above methodology, electronic packaging engineers can identify stresses imposed by hot solder dip loads, optimize respective process conditions, and ensure that refinishing can be risk-free and has sufficient safety margin.

The presented work shows that thermo-mechanical models, developed and validated in line with the presented methodology and experimental tests data, are reliable alternatives to an experimental only approach in assessing risk of damage. The study outlined here emphasizes the importance of deriving damage limits that can be used with respective model predictions. While initial derivation of such limits do require empirical correlation and experiments, once the damage levels are available then they can be used again and again with similar models and similar package types. This is true as long as the geometry and material constructions do not change dramatically with any new parts that need to be assessed. The modelling results can also provide in-depth understanding and quantitative evaluation of the safety margins.

V. Conclusions

Although the robotic hot solder dip process has been advanced and aligned to standards in recent years, and adopted safely by high reliability equipment electronics manufacturers, there is still limited understanding about the stress safety margins in relation to process thermal loads. How susceptibility to damage is affected by the package constructional design is also not well understood. This was illustrated in the Transformational ManTech Research Project S1057 [5,6].

The significance of the work reported in this paper is the new knowledge and methodology for quantitative evaluation of the stresses that hot solder dipped leaded components could endure before showing signs of thermo-mechanical damage under solder dip loads. This can enable the industry to assess the damage risks in a timely and cost-efficient manner.

The main conclusions from this work are:

- A carefully structured experimental programme of damage-promoting hot solder dip-to-destroy test conditions, combined with C-SAM examinations, can generate results and data which can help to assess and map robustly the observed graded damage to the severity of the respective hot solder dip load.
- Accurate finite element models for the stresses driving the expected failure mode of interfacial delamination under hot solder dip loads were developed. These built upon previous work of the team on thermal process models for hot solder dip [11], and thus represent a contribution to an enhanced modelling capability and new knowledge with regard to the refinishing process.
- Failure limits for delamination at the molding compound to the lead-frame interfaces using finite element model stress predictions and C-SAM data were derived and used in subsequent validation of the developed stress models. The modelling predictions were found to be in excellent agreement with the C-SAM-observed delamination damage results and trends.
- With availability of relevant data, the proposed methodology allows for the user to adopt different delamination failure models and failure criteria than those reported in the paper.
- Susceptibility to solder dip damage was found to be predominantly affected by the package design features and materials defining the thermal path from the dipped termination to the package internal structure.
- Package types without thermal enhancement are likely to have good safety margins to the standard refinishing process. Some extreme package designs that require refinishing of an externally exposed thermal pad, or leads fused to the pad of the lead-frame, may need assessments to confirm no risks of latent damage or measurable delamination to hot solder dip.

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Stoyan Stoyanov (M’08–SM’16) received the BSc degree in mathematics and MSc in applied mathematics from Sofia University, Bulgaria in 1994 and 1996 respectively. He has obtained his PhD degree in computational engineering at University of Greenwich, London, United Kingdom, in 2004. Since 2004, he is a member of the Computational Mechanics and Reliability Group (CMRG) at the School of Computing and Mathematical Sciences at University of Greenwich.

In 2009 he was promoted from the position of Senior Research Fellow to Reader in Computational Engineering. His research interests include the modelling and simulation of the performance and reliability of electronics products and microsystems, physics-of-failure modelling, computational intelligence for data-driven and prognostics modelling, additive manufacturing and design optimization.

Dr. Stoyanov is a member of the IEEE Electronics Packaging Society and a member of the Steering Committee of the IEEE International Spring Seminar on Electronics Technology.

Chris Bailey (M’03-SM’05) received his PhD in Computational Modelling from Thames Polytechnic, UK, in 1988, and an MBA in Technology Management from the Open University, UK, in 1996. He then joined Carnegie Mellon University as a Research Fellow within the Department of Materials Science from 1988-1991. He then joined the University of Greenwich and in 2001 obtained a Professorship in Computational Mechanics and Reliability.

Professor Bailey is Director of the Computational Mechanics and Reliability Group at the University of Greenwich, London, United Kingdom. His research interests include Prognostics and Health Management, Engineering Reliability, Embedded and Smart Systems, Optimization, Computational Mechanics, Multi-physics modelling, Maritime Engineering, Structural Analysis, Micro and Nano Systems and Additive Manufacturing. He has published over 250 papers in the field of modelling and reliability of micro-technology based processes and products and consults with a number of companies worldwide.

Professor Bailey is president on the board of governors of IEEE-EPS, member of the Heterogeneous Integration Roadmap team, Chair of the UK&RI IEEE EPS/Reliability chapter, and an associate editor of the IEEE CPMT Transactions. He is also a member of several IEEE conference committees including EuroSime, ESTC and EPTC. He is also an executive member of the EPSRC funded Centre for Power Electronics in UK.

Paul Stewart received a BSc degree (Honours) in electronic and electrical engineering from Robert Gordon University (RGU), Scotland in 1986 and an MBA from Edinburgh University Business School in 1999. He has worked for Leonardo MW Ltd, Edinburgh (and its previous incarnations) for 31 years in a number of engineering roles, primarily concerned with product reliability and product safety.

Since 2006, he has been Engineering Lead for lead-free design and in 2013 became the Interconnects group Engineering Lead. His research interests include lead-free manufacturing, reliability of electronics products and physics-of-failure.

Mike Parker biography not available at the time of manuscript submission.

John F. Roulston received his BSc (Hons) in electrical engineering from Queens University, Belfast, in 1970 and MSc in Digital Communications from Heriot Watt University (HWU) in 1982. He was awarded Honorary Doctorate in Engineering, HWU, 1998, Honorary Doctorate in Science from Edinburgh University, (EU), 1989, Industrial Professor of Electronics, EU.

He is a specialist in radar and microwave communications and Ex-Technical Director of Ferranti Scotland, Marconi Avionics and BAE Systems Avionics. Currently he is owner of Scimus Solutions Limited, a technology consultancy.

Professor Roulston’s awards and honors include FIET, FREng., FRSE, British gold medal of the Royal Aeronautical Society and the James Alfred Ewing Gold Medal of the Royal Academy of Engineering. Professor Roulston is a trustee of the James Clerk Maxwell Foundation in Edinburgh.