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Fault discrimination and protection coordination for a bipolar full-bridge MMC-HVDC scheme

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Abstract: Fault discrimination and protection design for bipolar high-voltage direct current transmission solutions based on modular multilevel converters (MMC-HVDC) links are of significant importance for a reliable and resilient power transmission. If full-bridge submodules are utilised, fault-dependent handling concepts considering the location of an event are enabled. This study presents a comprehensive approach to differentiate and deal with internal converter and dc side faults. While a multitude of measurements inside and at the clamps of each converter is usually only used for simple threshold-based hardware-related protection, additional differential and derivative criteria may further improve selectivity. However, this requires careful configuration to avoid improper reactions. To highlight the coordinated manner of the proposed concept, various faults are analysed and selected examples are explicitly investigated and visualised using the PSCAD EMTDC software.

1 Introduction

Bipolar high-voltage direct current transmission solutions based on modular multilevel converters (MMC-HVDC) provide an attractive set of operational benefits compared to traditional ac grid enforcement [1]. As each scheme consists of a fully control- and protection-wise independent upper and lower subsystem, in case a ground-return path or a dedicated metallic return (DMR) are present, inherent line redundancy allows at least a continuing supply of half the rated transmission power in case of a dc pole or single converter fault. If full-bridge (FB) or comparable submodule topologies are utilised, dc side contingencies can be handled actively by using controls. This avoids blocking (converter passivation) and enables continuing in-feed of reactive power (STATCOM) into the connected ac network. To supplement available literature mainly dealing with dc fault current interruption (FCI) and restart procedures [2, 3], this work focuses on protection scheme design and threshold determination to obtain high selectivity.

The paper is structured as follows. In Section 2, basics of bipolar MMC-HVDC are presented and a multi-stage protection concept is introduced. Furthermore, Section 3 describes the investigated scenario and provides insights into protection threshold determination. Characteristic transients are shown in Section 4. Finally, Section 5 concludes the work and highlights further research opportunities.

2 Bipolar MMC-HVDC

Bipolar terminals, named consecutively with superscript Tx where $x \in 1, 2$, consist of two series connected converters. Their internal quantities can be distinguished by superscript Cxp and Cxn for positive/upper and negative/lower converter, respectively. In Fig. 1, the detailed equivalent three-phase circuit ($y \in 1, 2, 3$) for a non-grounded terminal is presented. Typically, a wye-delta transformer (delta lags wye), which connects each converter to the ac network, is used. Additionally, a dc reactor is implemented to establish a separation between dc transmission system and the converter with its attached dc yard.

2.1 Control basics

In contrast to first generation voltage source converter technology, the implemented energy storage in a MMC is distributed into six converter arms. Each arm consists of several hundred submodules in FB configuration. Even though this increases overall complexity in terms of control design and energy balancing/reallocation, decoupled ac and dc clamp current controls minimise ac–dc interactions and enable furthermore advanced control features [4].

For the upper converter in Fig. 1, superscript as well as resistive components are removed or neglected to simplify the presentation, the following two loops can be obtained for an arbitrary phase y:

$$u_{\mathrm{ac},N0} + u_{\mathrm{ac},yN} + u_{p,y} + \mathrm{d}i_{p,y}/\mathrm{d}t \cdot L_{\mathrm{arm}} - u_{\mathrm{dc}} - u_{\mathrm{conv,DMR}} = 0, \quad (1)$$

and

$$u_{\mathrm{ac},N0} + u_{\mathrm{ac},yN} - u_{n,y} - \mathrm{d}i_{n,y}/\mathrm{d}t \cdot L_{\mathrm{arm}} - u_{\mathrm{conv,DMR}} = 0. \quad (2)$$

Now, a phase module current is introduced

$$i_{\mathrm{phm},y} = \left(i_{p,y} + i_{n,y}\right)/2. \quad (3)$$

These quantities are used to control converter inner ($i_{\mathrm{phm},\alpha\beta}$) currents for balancing purposes and the dc side ($i_{\mathrm{phm},0} \sim i_{\mathrm{dc}}$) current to adjust power exchange in the fixed $\alpha\beta 0$-frame. Performing some maths, the initially underlying basic differential equations for decoupled control can be derived. These are

$$u_{\Sigma,y} = \left(u_{p,y} + u_{n,y}\right)/2 = -\mathrm{d}i_{\mathrm{phm},y}/\mathrm{d}i \cdot L_{\mathrm{arm}} - u_{\mathrm{dc}}/2, \quad (4)$$

and

$$u_{\Delta,y} = \left(u_{n,y} - u_{p,y}\right) = -\mathrm{d}i_{\mathrm{ac},y}/\mathrm{d}t \cdot L_{\mathrm{arm}} - 2 \cdot u_{\mathrm{conv},yN} + c_{\mathrm{off}}, \quad (5)$$

where the constant offset c_{off} has no impact on ac current exchange due to the chosen transformer setting.

2.2 Protection zone definition

In recent projects, MMC-HVDC links have been dominantly carried out in half-bridge symmetrical monopolar configurations. While these realisations strictly require converter blocking and ac circuit breaker operation to interrupt fault currents, an immediate classification of fault locations has been beyond specification and need. This aspect changes for bipolar schemes equipped with FBs, as advanced controls enable a control-wise current interruption

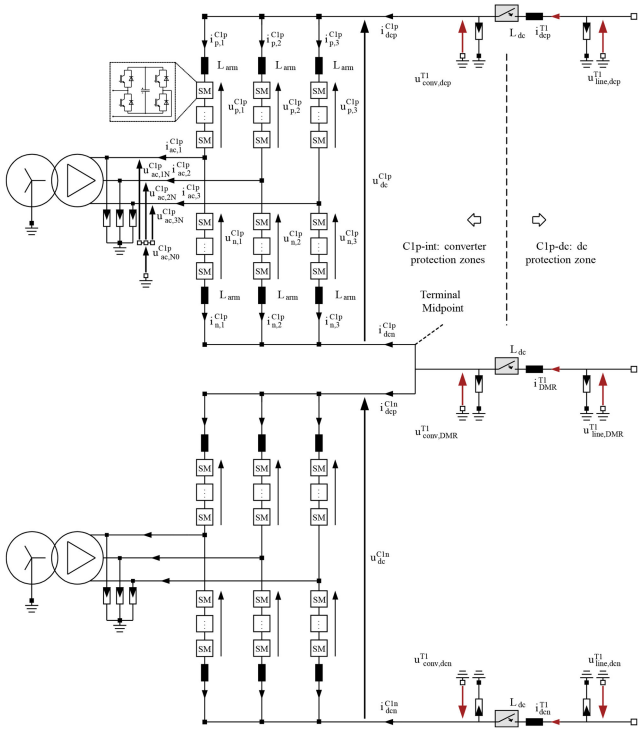

Fig. 1 *Bipolar terminal three-phase equivalent circuit*

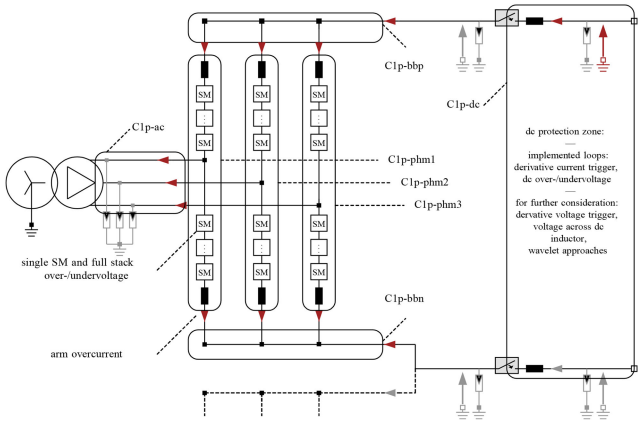

Fig. 2 *Individual converter protection zone overview*

during dc side contingencies. As mentioned in [3], STATCOM functionality (reactive current capability) can be maintained.

Therefore, a separation between several internal protection zones, where faults are cleared by blocking insulated-gate bipolar transistors (IGBTs) (countervoltage injection) and ac breaker operation, and a dc protection zone for each individual converter has to be established. According to Fig. 2, an example of the upper converter of a terminal is shown. To provide insights on the implementation of measurements, related quantities and their specified monitoring location are indicated. Further, to improve selectivity and enable a clear separation between the zones, a dc inductor is implemented.

2.3 DC protection and active fault current interruption

The proposed active current interruption in case of dc/external contingencies (mainly single pole to ground faults) imposes tough requirements for system protection. Especially in terms of speed – mainly to remain a reasonable current capability margin towards the overcurrent limit of power electronic devices and to limit impact on the other subsystem – derivative methods seem beneficial. Control-wise, the dc fault current can be interrupted by adjusting $u_{\Sigma,0}$ to influence $i_{\text{phm},0}$ ($i_{\text{phm},1-3}$ transformed into stationary $\alpha\beta 0$ frame) [4]. Within this work, a method utilising the current derivative at each high-voltage pole has been selected. Signal input originates from the current measurement device on the dc transmission side of the inductor, and is delayed and finally compared to the selected threshold. For the sake of completeness, as also indicated in Fig. 2, it should be mentioned that other concepts or combined variations of approaches are as well feasible [2]. Additionally, to handle high ohmic faults (non-severe) with limited transient impact, over-/under-voltage protection ($|u_{\text{line}\cdot\text{dcp}/n}| < 0.5$ pu or >1.5 pu for 10 ms) is introduced.

2.4 Differential protection for internal faults

Conventionally, converter internal faults are detected by safe operating area violations of implemented hardware. However, similar to the motivation above, the impact on the non-affected subsystem in a bipolar scheme can be minimised by increasing detection speed. Using a differential current concept, six independent zones are continuously observed in each converter. In case a threshold related to the overall accuracy of affected measurements is exceeded ($i_{pz,\max}$), module blocking is triggered. As an example, the following condition

$$C1\text{p} - \text{phm1}: \sum i = i_{p,1} - i_{\text{ac},1} - i_{n,1} < i_{pz,\max} \tag{6}$$

indicates normal operation conditions within zone C1p-phm1.

2.5 Power electronics and submodule protection

Today, a tremendous effort is focussing on MMC-HVDC related research, mainly regarding control design and balancing. Nevertheless, considerations related to feasible operation ranges of implemented hardware during steady state as well as transients are scarce. Influenced by an initial manufacturer's perspective in [5], a feasible range for thresholds can be determined considering case-specific ratings of selected devices. Most importantly, this comprises arm overcurrents ($i_{\text{arm},\max}$) and a feasible operating range of submodule capacitors ($u_{\text{SM},\min}$, $u_{\text{SM},\max}$). Due to the importance of these loops to avoid severe hardware damage, they always overrule control-wise FCI in case of a malfunction.

2.6 Overview

To summarise prior considerations, the introduced multistage protection concept is visualised in Fig. 3. It allows a differentiation between internal and external faults and enables fault location dependent handling strategies. To address the fact that control-wise FCI poses a substantial risk to power electronic assets and submodules, it should be emphasised that converter internal protection loops remain activated under all circumstances.

3 Scenario and threshold determination

Within the scope of this contribution, a bipolar MMC-HVDC link consisting of two terminals (T1 is controlling the dc current, T2 controls the dc voltage) is investigated in PSCAD EMTDC. The system is carried out with single point grounding ($R_{\text{gnd}} = 0.7\ \Omega$) at T2 and DMR. Overall, transmission length equals 700 km. For the investigations, frequency-dependent line models and submodule stack equivalents classified as Type 4 related to [6] are used. Main system parameters are provided in Table 1.

3.1 Derivative threshold for dc protection

Long overheadline corridors are likely to be subject to pole to ground faults caused by externally triggered incidents. As it is desired to continue power transmission on the non-faulted subsystem of the bipolar scheme, while the other scheme interrupts the dc fault current, a suitable threshold for the derivative current criterion needs to be identified. For this purpose, a sweep of various fault locations along the OHL (where $x = 0$, 300, 350, 400 and 700 km) utilising a wide range of fault resistances has been carried out. To exclude immediate converter impact, fault detection is disabled at both stations while the peak value of the first incoming travelling wave is recorded. As indicated in Fig. 4,

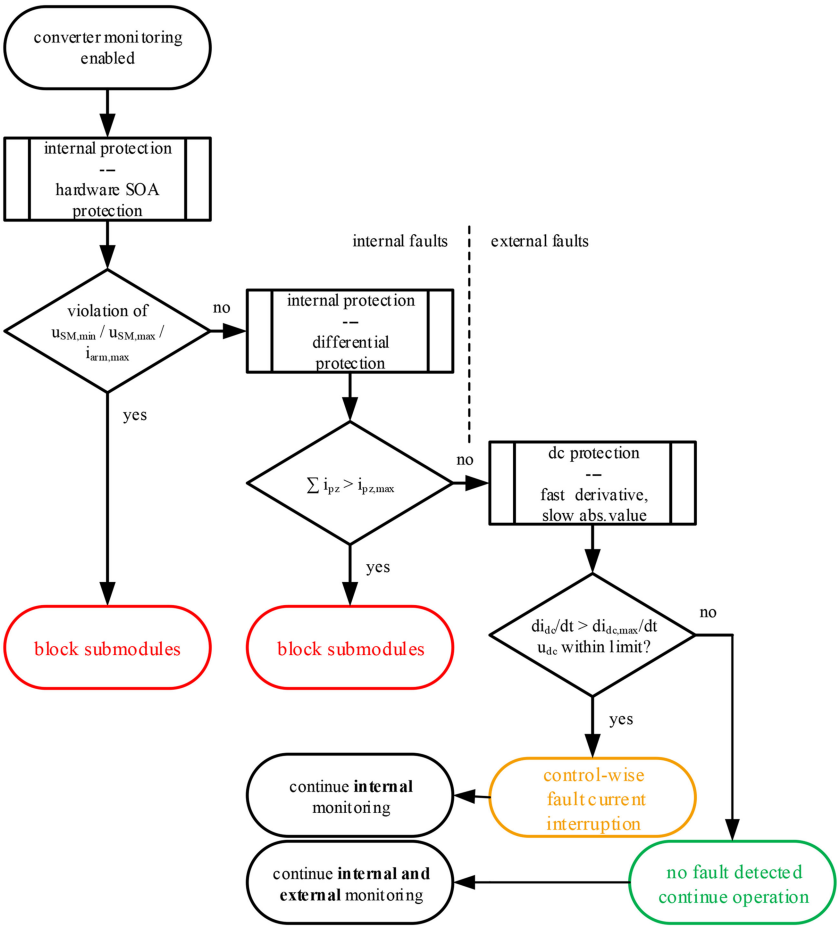

Fig. 3 *Schematic overview of multi-stage protection concept*

Table 1 Specification of investigated single point grounded bipolar scheme with DMR

Parameter	Value
nominal dc voltage (pole to ground)	±525 kV
nominal ac voltage (grid/converter)	400 kV/320 kV
ac network X/R ratio	10
P_{rated}/Q_{rated} (@ ac pcc) per converter	1.05 GW/450 MVA
line frequency	50 Hz
submodules per arm	270
submodule capacitor	8.5 mF
steady-state arm sum voltage	675 kV

exemplarily shown for terminal T2, a suitable threshold can be identified to achieve a selective behaviour (only C2p tiggers). The corresponding scheme is introduced in Fig. 5.

3.2 Thresholds for internal protection

A summary of selected thresholds is provided in Table 2. Additionally, the following paragraphs enable detailed insights on relevant considerations.

- *Protection zone trigger limit*: The selection of this threshold is generally uncritical, as severe low impedance faults within the converter cause rapid imbalance and can be quickly detected within single protection intervals. Nevertheless, to detect faults within zones close to ground potential, located near the ground electrode or the converter midpoint, the selected value should be minimised and just slightly exceed aggregated measurement uncertainty of involved current measurement devices.
- *IGBT current limit*: Current limits have been selected considering state-of-the-art IGBT devices with high current capability (3 kA dc, up to 6 kA peak for 1 ms) and a rated collector–emitter voltage of 4.5 kV [7]. This choice is mainly caused by (i) increasing requirements for more powerful embedded onshore transmission (bulk-power) as well as (ii) an additional dynamic current margin need to be caused by the desired active dc FCI capability. To account for uncertainties regarding the shape and duration of occurring transients, a conservative limit of 4 kA has been selected. Further improvements may include thermal boundary conditions (ambient temperature, pre-fault junction temperature, cooling circuit design) to improve the degree of device utilisation.
- *Submodule capacitor limits*: Besides regular arm sum voltage oscillations during steady-state operation of MMCs, transient events cause significant deviations and shall not exceed hardware-critical limits. Also for non-directly affected converters in case of a dc fault at the opposite pole, it must be ensured at all time that relevant quantities are maintained within a predefined band during fault ride through (FRT). Even though this is normally reflected by internal converter balancing, a risk remains and requires a backup.

In Fig. 6, an overview of voltage limits during steady state and dynamic MMC operation are provided. While overshoots are

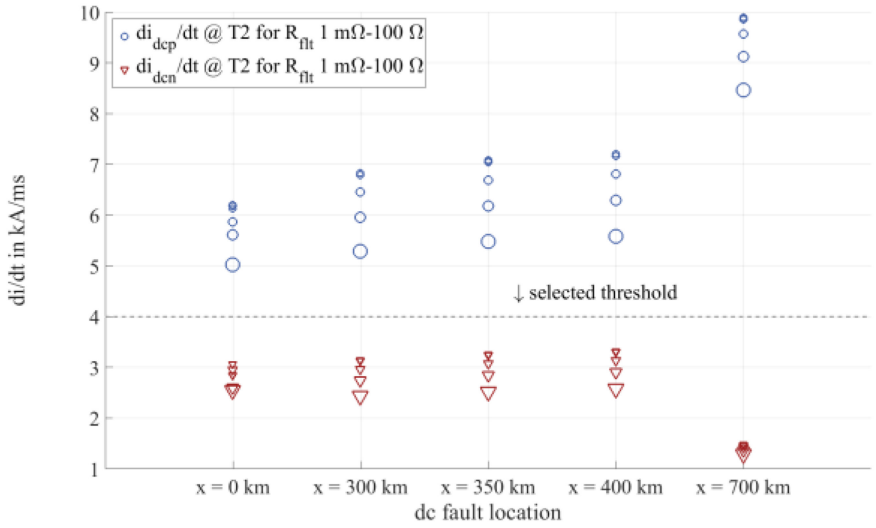

Fig. 4 *Measured current derivatives at T2 during sweep of positive pole to ground faults. Marker size indicates value of inserted fault resistance*

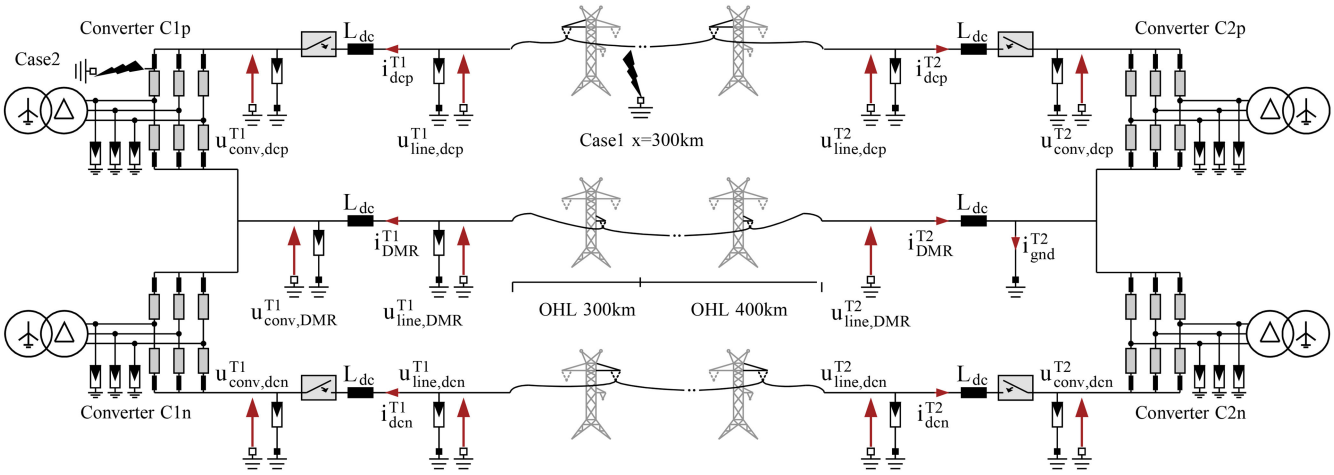

Fig. 5 *Schematic overview of bipolar scheme including dc voltage and current quantities*

Table 2 Detailed overview of selected protection design parameters and threshold values

System protection	Value
dc varistor MCOV	535 kV
midpoint varistor MCOV	90 kV
varistor protective level	1.8 pu at 1 kA
signal processing (control/measure)	40 µs + 60 µs
External/dc protection	
d*i*/d*t* threshold	4 kA/ms
dc voltage (violated for 10 ms)	750 kV/250 kV
Internal/converter protection	
SM capacitor limits (max./min.)	3.3 kV/1.7 kV
max. arm current	4 kA
protection zone trigger limit	0.15 kA

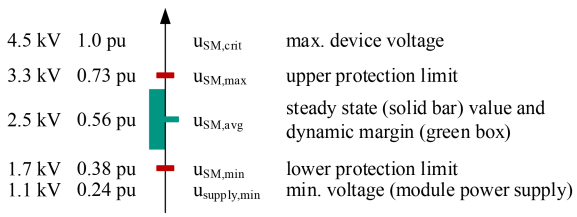

Fig. 6 *Selected submodule voltage limits, steady-state levels and dynamic margin for control purposes similar to [5]*

primarily critical in terms of hardware damage, hitting lower limits impacts controllability and both require blocking.

4 Results

To highlight transient fault performance of the proposed concept, two exemplary cases are provided. Prior to the faults, rated power

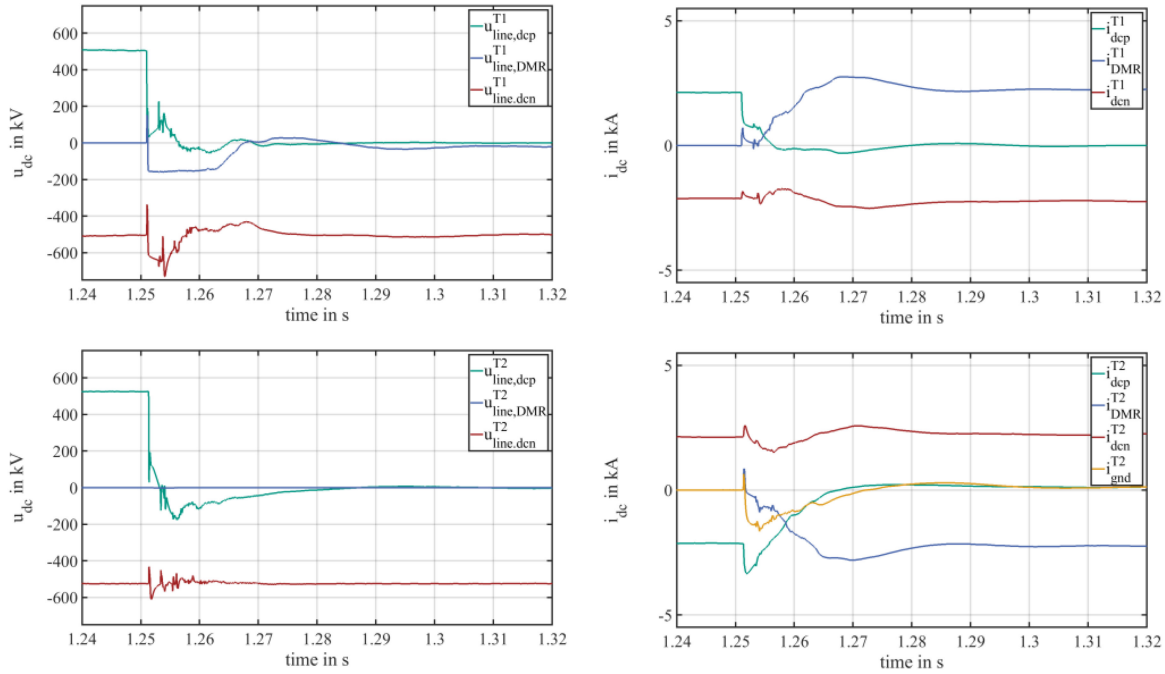

Fig. 7 *Case 1 – transient response of bipolar scheme to a positive pole to ground fault at x = 300 km (R_{flt} = 1 m Ω, t_{flt} = 1.25 s)*

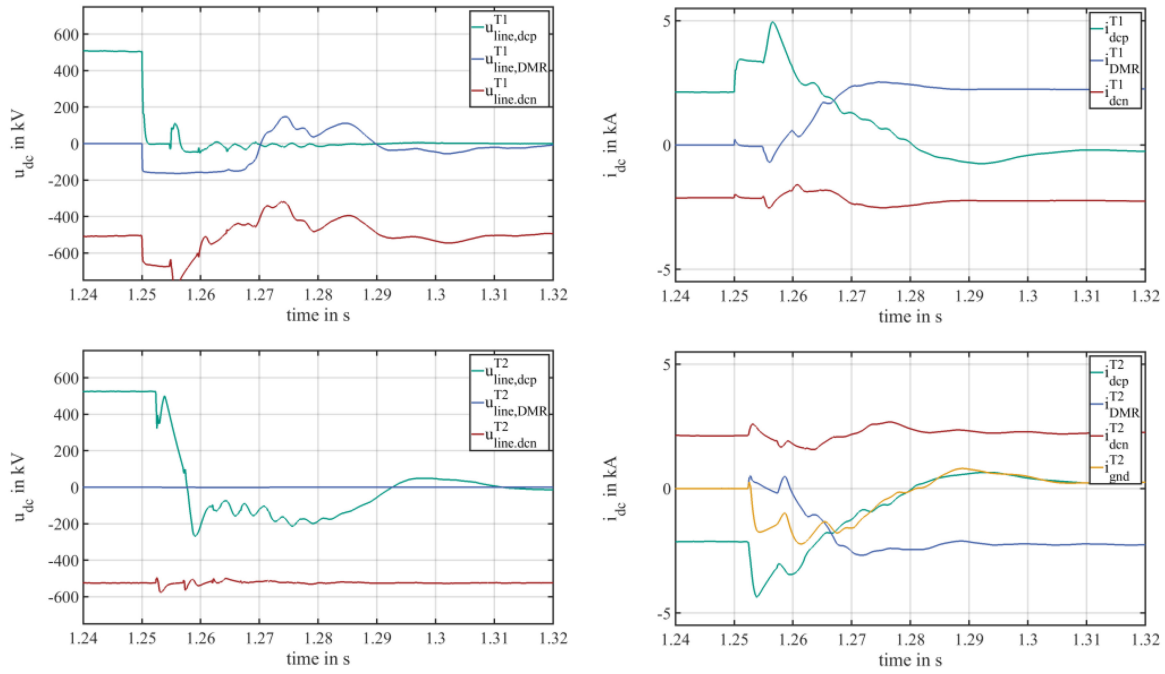

Fig. 8 *Case 2 – transient response of bipolar scheme to a phase to ground arm fault in phase one of converter C1p (R_{flt} = 1 mΩ, t_{flt} = 1.25 s)*

of 2.1 GW (ac infeed at T1) is transferred. The reactive power setpoint of each converter corresponds to $Q = +450$ MVA.

In Fig. 7, voltage and current transients subsequent to a pole to ground fault at location $x = 300$ km along the positive dc conductor are shown. The fault occurs at $t = 1.25$ s. Triggered by the incoming travelling wave, both upper converters detect a dc current derivative threshold violation, while the negative dc pole derivatives remain below the specified limit and power transmission is continued. Transient distortions on the healthy pole do not violate any other hardware related limit. To clear the external fault and avoid further fault current contribution, both upper MMCs actively reduce their dc output current by quickly adapting the dc clamp output voltage. Within ~30 to 40 ms, current flow on the positive pole is fully interrupted and is commutated into the DMR. At the non-grounded terminal, midpoint voltage is transiently shifted, clamped for first 10 ms by the corresponding surge arrestor and enters post-fault steady state.

The visible offset corresponds to the voltage drop along the line caused by continuing current flow in the lower subsystem.

In Fig. 8, case 2 shows response to an internal arm to ground fault in converter C1p. The fault is located between converter submodules and upper arm inductor of phase one. Triggered by the differential protection, which identifies a violation in zone C1p-phm1, the converter quickly blocks its module stacks. Nevertheless, dc fault current further increases until C2p triggers FCI, as the fault is connected through the arm inductance to the dc conductor of the scheme. Here, blocking cannot decouple the dc side from the fault. Generally, a slightly more oscillatory behaviour compared to the previous case can be observed. As the fault is now located within T1, impact on the dc clamp of converter C1n is increased compared to the previous case.

To enable a better understanding of effects happening within the terminals and converters, Figs. 9 and 10 show C1p arm currents and C1n arm sum voltages, respectively. The most striking difference occurs when comparing arm currents between the two

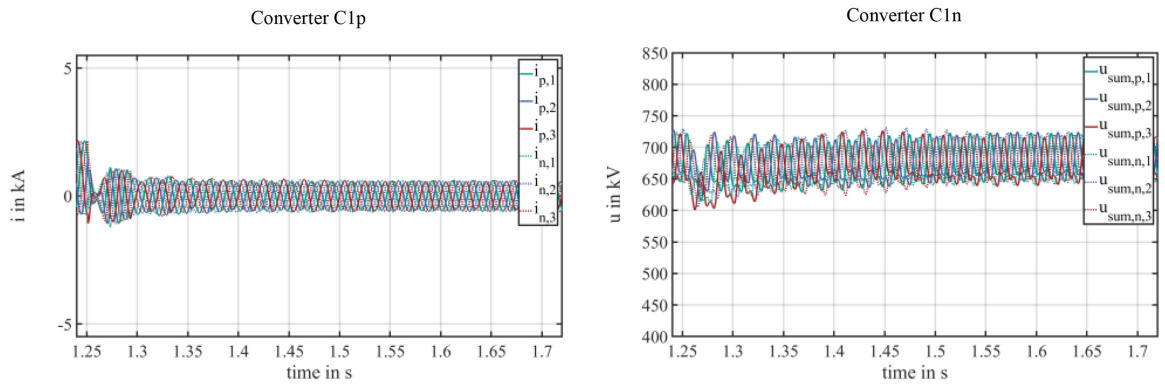

Fig. 9 *Case 1 – transient arm currents of converter C1p during FCI and impact on converter arm sum voltages of converter C1n during FRT*

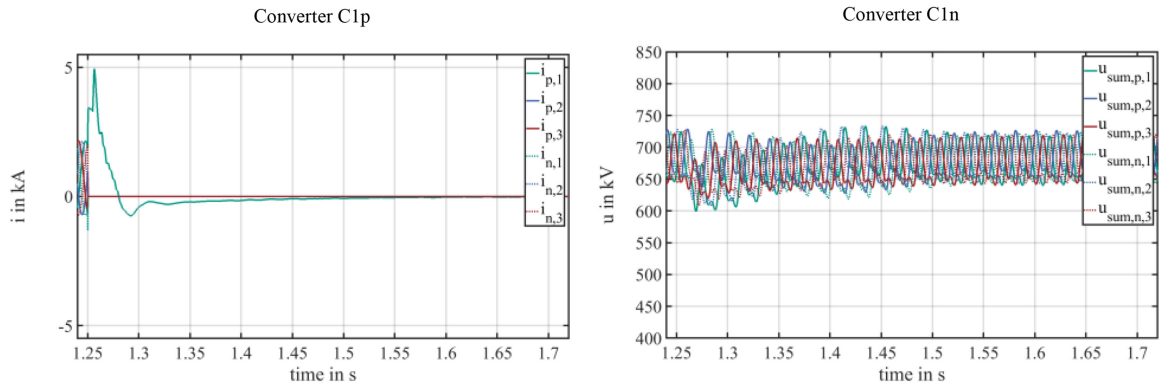

Fig. 10 *Case 2 – transient arm currents of converter C1p subsequent to module blocking and impact on converter arm sum voltages of converter C1n during FRT*

cases. While C1p rides through the dc line faults within case 1 and provides reactive power, the converter is blocked in case 2 and only current $i_{p,1}$ remains. This is related to the fault location between submodule stack and current measurement, but has no impact on power electronic assets. Additionally, monitoring the arm sum voltages u_{sum} in MMC C1n at T1, satisfactory control performance enables a smooth FRT of the lower subsystem. The converter returns into a steady state around 300 ms after the fault.

5 Conclusion

This contribution introduces a multi-stage fault detection and handling concept for a bipolar MMC-HVDC scheme with OHL transmission. The scheme differentiates and deals with internal and dc side faults in a coordinated manner. Analysis of multiple runs and transients for characteristic cases – obtained using the PSCAD EMTDC software – provide proof of the universal capability of the proposed concept and give detailed insights into threshold determination and performance. Beyond this work, the impact of mixed dc cable and OHL transmission on system design and protection are subject of current research activities.

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