On Achieving Capture Power Safety in At-Speed Scan-Based Logic BIST

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Abstract—The applicability of at-speed scan-based logic ***built-in self-test*** (***BIST***) is being severely challenged by excessive capture power that may cause erroneous test responses for good chips. Different from conventional low-power BIST, this paper is the first that has explicitly focused on achieving ***capture power safety*** with a practical scheme called ***capture-power-safe BIST*** (***CPS-BIST***). The basic idea is to identify all possibly-erroneous test responses and use the well-known technique of mask (***partial-mask*** or ***full-mask***) to block them from reaching the MISR. Experiments with large benchmark and industrial circuits show that CPS-BIST can achieve capture power safety with negligible impact on both test quality and area overhead.

I. Introduction

A. Importance of Test Power Safety

Scan design is the foundation for both ***stored pattern testing*** (using tester-applied pre-generated test vectors) and ***built-in self-test*** (***BIST***) (using on-chip-generated pseudo-random test vectors) [1]. Scan design makes it possible to conduct ***scan testing***, in which test vectors are shifted-in via scan chains in shift mode and test responses are loaded into individual flip-flops in capture mode for shifted-out via scan chains in subsequent shift mode. Furthermore, ***at-speed scan testing***, in which the test cycle is set to be equal to the functional clock cycle, has become indispensable for delay testing [2].

However, the power dissipation in scan testing can become excessive [3,4] and may have adverse impacts as illustrated in Fig. 1 based on the ***launch-on-capture*** (***LOC***) clocking scheme. ***Shift power***, caused by shift switching activity in the whole circuit due to the consecutive application of shift clock pulses, may result in chip damage, path delay increase, and reliability degradation. On the other hand, ***capture power*** is caused by the ***launch switching activity*** (***LSA***) triggered by the stimulus launch clock pulse at T_1, causing IR-drop in the ***power distribution network*** (***PDN***) that results in delay increase along sensitized paths. The instantaneous impact of excessive capture power is excessive-delay-increase-induced erroneous test responses from sensitized paths at T_2, causing a good chip to unduly fail in scan testing. Therefore, both ***shift power safety*** and ***capture power safety*** need to be guaranteed in scan testing [5].

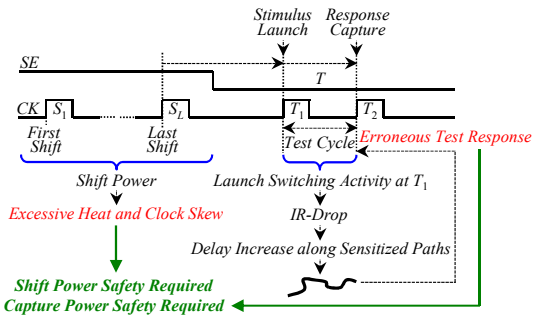


Fig. 1. Scan test power safety in LOC at-speed scan testing.

B. From Low-Power Test to Power-Safe Test

The test power issue has been conventionally tackled by ***low-power test*** [3,4], which reduces shift power or capture power or both by *circuit modification*, *test data manipulation*, *test clocking adjustment*, etc. However, low-power test may not guarantee that its reduction effect is always sufficient to avoid any excessive-test-power-induced problem [6]. In addition, local test power may remain excessive in some regions of a circuit even though low-power test has reduced global test power in the whole circuit to a very low level. Therefore, low-power test may not always guarantee test power safety.

- ***Towards Shift Power Safety***

There are a few solutions for achieving shift power safety. An example is ***scan segmentation*** [7], in which each original scan chain is split into N shorter segments and only one segment is shifted at a time. It reduces scan shift transitions to $1/N$ without increasing scan shift time. By properly selecting N based on circuit characteristics and package materials, the heat impact of shift power can be effectively managed. Note that this technique is applicable for both stored pattern testing (including compressed scan testing) and logic BIST. For logic BIST, techniques based on *supersession* (toggle and pattern) are also effective in achieving shift power safety [8, 9].

- ***Towards Capture Power Safety***

A typical capture-power-safe solution for stored pattern testing is ***rescue-&-mask*** [5], in which (1) the local switching activity around a ***long sensitized path*** (***LSP***) of a test vector is checked to see if it is a ***risky path*** (i.e., an LSP whose surrounding switching activity is so high that the test response from the LSP is ***possibly-erroneous*** (i.e., *the test response becomes an uncertain value*)); (2) for any risky path, X-filling is conducted in a pinpoint manner to reduce the local switching activity around the risky path; (3) if the effect of switching activity reduction is insufficient to turn a risky path into a non-risky path, the uncertain test response from the risky path will be masked to instruct the tester not to use it. This way, the impact of excessive capture power on final test results is avoided, thus achieving capture power safety.

However, *rescue-&-mask* cannot be applied to scan-based logic BIST. This is because (1) the *rescue* process is conducted by changing test vector contents by X-filling and (2) the *mask* process is conducted by changing test response values, both being impossible in the logic BIST environment. Therefore, this paper will focus on the issue of capture power safety in logic BIST.

C. Capture Power Safety Problem in Logic BIST

As shown in Fig. 2, test stimuli in logic BIST are generated by an on-chip ***pseudo-random pattern generator*** (***PRPG***) and test responses are analyzed by an on-chip ***multiple input signature register*** (***MISR***) [1]. Additionally, logic BIST includes a ***phase shifter*** for reducing pattern content correlations, a ***compactor*** for reducing the MISR bit-width, and a ***BIST controller*** for coordinating all BIST operations. These blocks are collectively called ***BIST-specific blocks***. The original circuit is converted into a ***BIST-ready circuit*** by *scan insertion*, *X-bounding*, and *test point insertion* [1].

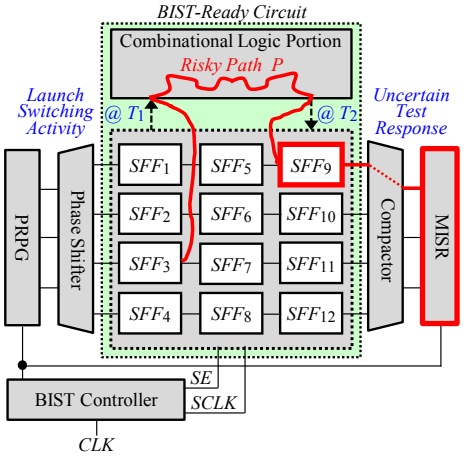


Fig. 2. Capture power safety problem in logic BIST.

Suppose that the LOC clocking of Fig. 1 is applied to the logic BIST of Fig. 2. In the design stage, capture power analysis may find that the launch switching activity at T_1 (also shown in Fig. 1) causes excessive switching activity around some long sensitized paths in the combinational logic portion of the BIST-ready circuit. These paths are ***risky paths*** (e.g., P in Fig. 2) since test responses from them are ***possibly-erroneous*** (i.e., *test response values become* ***uncertain***) [5]. At T_2 (also shown in Fig. 1), such ***uncertain test responses*** are loaded into some scan flip-flips (e.g., SSF_9 in Fig. 2). As a result, when test responses are shifted-out to the MISR in subsequent shift mode, uncertain test responses will corrupt the MISR content to unduly fail a good chip.

Many low-power BIST techniques have been proposed [9], most of them focusing on shift power reduction. Although some of them also help reduce capture power, the reduction is mostly global, and there is no guarantee that it is always sufficient to eliminate all risky paths. This means that previous low-power BIST techniques may not always guarantee capture power safety.

D. Contributions of This Paper

Hardware-based masking is a technique that is widely employed in logic BIST for X-bounding and test (mostly shift) power reduction [1, 3, 4, 9]. It is a straightforward idea to apply masking for achieving capture power safety. For example, the uncertain test response at the output of SSF_9 (shown in Fig. 2) can be masked in one way or another to prevent it from reaching the MISR. However, there is so report so far about using hardware-based masking to achieve capture power safety. The obvious reason is the perception that such masking will severely impact test quality and area overhead in logic BIST.

This paper is the first that has explicitly focused on achieving capture power safety in logic BIST by showing the feasibility of making use of the well-known technique of masking. Its major contributions are as follows:

(1) It reveals an important property that uncertain test responses in logic BIST are actually very few. This makes it feasible to achieve capture power safety by masking uncertain test responses.

(2) Two masking options, ***partial-mask*** and ***full-mask***, are proposed to realize a ***capture-power-safe BIST*** (***CPS-BIST***) scheme. Comprehensive experiments show that the impact of masking on test quality and area overhead are negligible.

E. Paper Organization

Sect. 2 provides the background, Sect. 3 presents the details of CPS-BIST, Sect. 4 reports experimental results, and Sect. 5 concludes the paper.

II. BACKGROUND

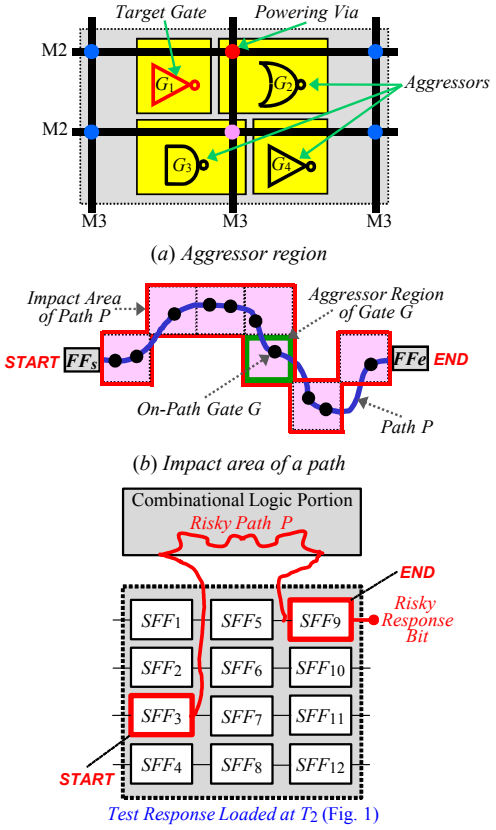
A. LSP-Based Capture Power Safety Checking

The root cause of the capture power problem is excessive launch switching activity at T_1 (shown in Fig. 1), which may cause excessive local switching activity around a sensitized path, resulting in excessive delay increase along the path and consequently a timing failure at T_2 (shown in Fig. 1). It is obvious that a ***long sensitized path*** (***LSP***) is vulnerable to such timing impact of capture power [4, 5]. Therefore, capture power safety checking can be conducted with a long-sensitized-path-based approach based on the following definitions [5]:

Definition 1: The aggressor region of a gate G, denoted by $AR(G)$, is composed of aggressor nodes (gates and flip-flops) whose transitions have a strong impact on the supply voltage of G.

Definition 2: The ***impact area*** of P, denoted by $IA(P)$, is composed of the aggressor regions of all on-path gates $(G_1, G_2, ..., G_n)$ of P. That is, $IA(P) = AR(G_1) \cup AR(G_2) \cup ... \cup AR(G_n)$.

Definition 3: A path P is a ***risky path*** under a test vector V if (1) P is long (w.r.t. Threshold-I), (2) P is sensitized by V, and (3) the launch switching activity at T_1 (shown in Fig. 1) in $IA(P)$ is excessive (w.r.t. Threshold-II).



(*a*) *Aggressor region*

(*b*) *Impact area of a path*

(*c*) *Risky path and risky response bit*

Fig. 3. LSP-based capture power safety checking.

The two thresholds in Definition 3 are as follows: A path is long if its length is greater than *PATHLIMIT* (as Threshold-I), which is usually set as a percentage of the longest path (measured by either its delay or its logical level) in a circuit. Furthermore, whether the launch switching activity in the impact area of a path is excessive can be determined by checking the ***weighted switching activity*** (***WSA***) [4] in the impact area of the path since the

local WSA has a high correlation with the delay increase along the path [4, 5]. That is, launch switching activity in the impact area of a path is considered excessive if the WSA in the impact area is higher than *WSALIMIT* (as Threshold-II), which is usually set as a percentage of the maximum WSA in the impact area. Capture safety checking based on these two thresholds is also applicable for advanced capture power management [10].

Definition 4: A test response bit is a ***risky response bit*** if it corresponds to the end point of a risky path.

As described above, it is clear that a risky response bit is ***possibly-erroneous***. That is, a risky response bit is an ***uncertain*** value in the design stage. In this sense, a risky response bit is a type of unknown value (X).

Definition 5: A test vector V is a ***risky test vector*** if there is at least one risky path under V.

Definition 6: Scan-based logic BIST is ***capture-power-safe*** if none of its pseudo-random test vectors is risky.

The above definitions are illustrated in Fig. 3. Fig. 3 (a) shows how to identify the aggressor region for a gate G_1 by using layout and ***power distribution network*** (***PDN***) data [4]. Fig. 3 (b) shows how to identify the impact area of a path P. Fig. 3 (c) shows a risky path P and its corresponding risky response bit at the end point of P.

The capture power safety of scan-based logic BIST can be determined as described above by considering all pseudo-random test vectors to be applied. Position information on risky response bits and risky test vectors is obtained at the same time and stored for later use in the CPS-BIST design flow to be described in Sect. 3.

B. Property of Uncertain Test Responses in Logic BIST

As described above, excessive capture power may cause uncertain test responses in logic BIST. Since logic BIST applies a large number of pseudo-random test vectors, the conventional perception is that logic BIST must have many uncertain test responses. However, comprehensive experiments have shown that this perception is false.

Table I lists the circuits used for the experiments. Large ITC'99 benchmark circuits and a large industrial circuit (*dpro*) were used. Long-sensitized-path-based capture power safety checking was conducted for 10,000, 30,000, and 50,000 pseudo-random test vectors. Percentages of risky response bits and risky test vectors for different threshold settings are shown in Table II and Table III, respectively. In all experiments, *PATHLIMIT* (i.e., the threshold for determining whether a path is long) was set to 70% and 80% of the longest structural path in a circuit. *WSALIMIT* (i.e., the threshold for determining excessive launch switching activity in the impact area of a long sensitized path) was set to 20% of the maximum WSA in the impact area, which is a value commonly used in many other low-power or power-safe test solutions.

TABLE I. CIRCUIT STATISTICS

Circuit	*# of Gates*	*# of FFs*	*Longest Path Length (logic levels)*
b17	29,102	1,317	44
b18	94,438	3,064	62
b19	189,225	6,130	66
b20	29,128	430	61
b21	29,656	430	61
b22	42,567	645	59
dpro	731,487	99,759	105

The small percentages of risky response bits and risky test vectors shown in Tables II and III clearly demonstrate that uncertain test responses, contrary to the conventional perception, are actually very few in logic BIST. This property is especially evident for larger circuits, *b19* and *dpro*. Possible explanations for this important property of uncertain test responses are as follows:

TABLE II. PERCENTAGE OF RISKY RESPONSE BITS
("0.0000" means "<0.00004")

#TV	*PATH LIMIT*	*b17*	*b18*	*b19*	*b20*	*b21*	*b22*	*dpro*
10,000	*70%*	0.0003	0.0000	0.0000	0.0020	0.0048	0.0093	0.0000
	80%	0.0000	0.0000	0.0000	0.0000	0.0002	0.0001	0.0000
30,000	*70%*	0.0004	0.0000	0.0000	0.0050	0.0047	0.0104	0.0000
	80%	0.0000	0.0000	0.0000	0.0000	0.0003	0.0001	0.0000
50,000	*70%*	0.0003	0.0000	0.0000	0.0048	0.0053	0.0100	0.0000
	80%	0.0000	0.0000	0.0000	0.0000	0.0003	0.0001	0.0000

TABLE III. PERCENTAGE OF RISKY TEST VECTORS
("0.0000" means "<0.00004")

#TV	*PATH LIMIT*	*b17*	*b18*	*b19*	*b20*	*b21*	*b22*	*dpro*
10,000	*70%*	0.4100	0.0100	0.0000	0.6100	1.2000	2.8700	0.0000
	80%	0.0000	0.0000	0.0000	0.0200	0.0700	0.0600	0.0000
30,000	*70%*	0.4367	0.0333	0.0267	1.2800	1.1467	3.0033	0.0100
	80%	0.0033	0.0033	0.0000	0.0133	0.0967	0.0800	0.0000
50,000	*70%*	0.4360	0.0020	0.0120	1.2140	1.2240	2.9240	0.0080
	80%	0.0080	0.0000	0.0020	0.0200	0.0900	0.0500	0.0000

(1) ***Strict Sensitization Condition***: It is difficult for long paths to be sensitized even with a large number of pseudo-random test vectors in logic BIST. This is not surprising since, even for transition delay test vectors generated by sophisticated ATPG, the average % of risky test vectors for six ITC'99 circuits (*b17~b22*) was 4.17%, and the % of risky test vectors for the largest ITC'99 circuit (*b19*) was only 0.2% [5].

(2) ***Uneven Distribution***: Although test vectors applied in logic BIST are pseudo-random in nature, long paths sensitized by them and launch switching activity caused by them in a circuit are usually not evenly distributed across the circuit.

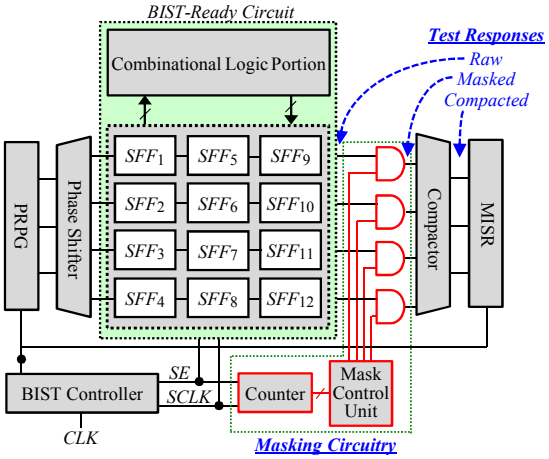
(3) ***Shared Path End Points***: Many risky paths share the same end point, which makes a single risky response bit to correspond to multiple risky paths.

III. CPS-BIST

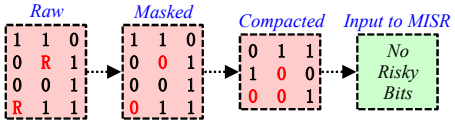
The ***capture-power-safe BIST*** (***CPS-BIST***) scheme directly achieve capture power safety in logic BIST by masking either all risky response bits (***partial-mask***) or the responses for all risky test vectors (***full-mask***) to prevent uncertain test responses from reaching the MISR. CPS-BIST is different from conventional low-power BIST techniques in that, instead of reducing capture power, CPS-BIST allows the existence of excessive capture power (*note that this has little to do with hot spots, which are more related to the accumulative impact of shift power*) but prevents its impact from invalidating the final signature by masking uncertain test responses. This is similar to *X*-bounding [1]; however, CPS-BIST is the first to apply masking for capture power safety in logic BIST.

A. Partial-Mask CPS-BIST

Fig. 4 (a) illustrates partial-mask CPS-BIST, consisting of a ***BIST-ready circuit***, ***BIST-specific blocks*** (PRPG, phase-shifter, compactor, MISR, BIST controller), and ***masking circuitry***. The BIST-specific blocks and masking circuitry are collectively called ***CPS-BIST-specific blocks***. Masking circuitry consists of (1) a ***mask network***, (2) a ***counter*** for getting the current scan slice position, and (3) a combinational ***mask control unit*** for generating required masking signals. Fig. 4 (b) shows the impact of partial-mask CPS-BIST on test responses. ***Raw*** test responses become ***masked*** test responses after risky response bits (denoted by R) are masked into 0 (in red). Masked test responses become ***compacted*** test responses to the MISR.

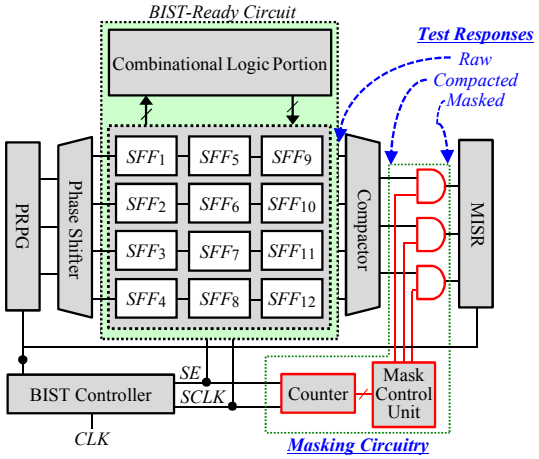


(*a*) *General scheme*

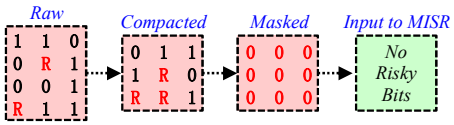


(*b*) *Effect on test responses*

Fig. 4. Partial-mask CPS-BIST.



(*a*) *General scheme*



(*b*) *Effect on test responses*

Fig. 5. Full-mask CPS-BIST.

As shown in Fig. 4, the BIST signature will not be corrupted by excessive-capture-power-induced uncertain test responses since no risky response bits can reach the MISR. As a result, capture power safety is achieved by partial-mask CPS-BIST. The partial-mask CPS-BIST scheme has the following characteristics:

(1) Fault coverage loss is minimized because only risky response bits are masked. Understandably, this benefit comes at the cost of a larger mask control unit.

(2) Risky response bits are masked before the compactor because a single unknown value (a risky response bit in this case) often becomes multiple unknown values after going through the compactor.

B. Full-Mask CPS-BIST

Fig. 5(a) illustrates full-mask CPS-BIST. The masking circuitry consists of (1) a ***mask network***, (2) a ***counter*** for getting the current test vector position, and (3) a combinational ***mask control unit*** for generating required masking signals. Fig. 5(b) illustrates the impact of full-mask CPS-BIST on test responses. ***Raw*** test responses become ***compacted*** test responses after going through the compactor. Both raw and compacted test responses contain risky response bits (denoted by R). The compacted test responses become ***masked*** test responses after all test response bits (both risky ones and non-risky ones) are masked into 0 (in red), and go into the MISR.

Full-mask CPS-BIST also achieves capture power safety since no risky response bits can reach the MISR. Although masking the complete test response for each risky test vector tend to cause fault coverage loss, the impact will be insignificant since the percentage of risky test vectors is very small in logic BIST. Full-mask CPS-BIST has the following characteristics:

(1) Area overhead of the mask control unit of full-mask CPS-BIST is less than that of partial-mask CPS-BIST. This is because the mask control of full-mask CPS-BIST is much simpler in that it only needs to mask the whole test response for a risky test vector.

(2) Fault coverage loss of full-mask CPS-BIST may be slightly higher than that of partial-mask CPS-BIST but still insignificant since the percentage of risky test vectors is very small in logic BIST.

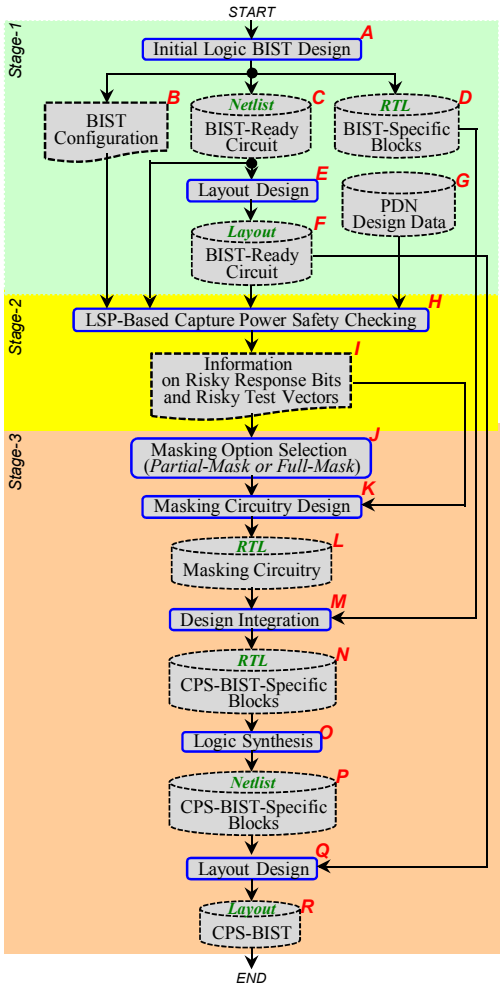


Fig. 6. CPS-BIST design flow.

(3) Risky response bits are masked after the compactor because there are significantly more input lines than output lines for the compactor.

C. CPS-BIST Design Flow

Fig. 6 shows the general CPS-BIST design flow. It consists of three stages as described below:

- **Stage-1 (*Initial Design*)**: First, initial logic BIST design (***A***) is conducted. The BIST configuration (***B***) is determined; the *circuit-under-test* (*CUT*) is converted into a BIST-ready circuit (***C***) by scan insertion, *X*-bounding, and test point insertion; and the RTL design of the BIST-specific blocks (***D***) is conducted. Design techniques [8, 9] can be applied to the BIST-ready circuit to achieve shift power safety. After that, layout design (***E***) is conducted for the BIST-ready circuit.
- **Stage-2 (*Capture Power Safety Checking*)**: LSP-based capture power safety checking (***H***) for the initial logic BIST is conducted by using BIST-ready circuit design data and *power network distribution* (*PDN*) network design data (***G***). The layout data (***F***) and PDN design data (***G***) are used to identify the impact area of each long sensitized path while the netlist (***C***) is used for identifying sensitized paths and conducting logic simulation to calculate WSA values in impact areas. The position information on risky response bits and risky test vectors (***I***) is also obtained at this stage.
- **Stage-3 (*CPS-BIST Design*)**: If the initial logic BIST is capture-power-risky, a masking option is selected (***J***), and the RTL design of the corresponding masking circuitry is conducted (***K***). Then, design integration (***M***) is conducted to combine the RTL masking circuitry (***L***) with RTL BIST-specific blocks (***D***) to create RTL CPS-BIST-specific blocks (***N***). After that, logic synthesis (***O***) is conducted to create the netlist of CPS-BIST-specific blocks (***P***). Finally, layout design (***Q***) is conducted to create the layout data of CPS-BIST.

```
module MCU_MASK-NETWORK (COUNTER, RAW, MASKED);
  input [17:0] COUNTER;    // Input from Counter
  input [3:0] RAW;         // Raw Test Response Input
  output [3:0] MASKED;     // Masked Test Response Output
  wire MCU_OUT[3:0];       // Mask Control Unit Output
  // Mask Control Unit
  assign MCU_OUT[0] = func_MCU_0(COUNTER);
  assign MCU_OUT[1] = func_MCU_1(COUNTER);
  assign MCU_OUT[2] = func_MCU_2(COUNTER);
  assign MCU_OUT[3] = func_MCU_3(COUNTER);
  function func_MCU_0;
    input [17:0] COUNTER;
    func_MCU_0 = 1'b0;
  endfunction
  function func_MCU_1;
    input [17:0] COUNTER;
    case (COUNTER)
      18'b010111001100100101: func_MCU_1 = 1'b0;
      18'b100100000010101001: func_MCU_1 = 1'b0;
      default: func_MCU_1 = 1'b1;
    endcase
  endfunction
  function func_MCU_2;
    input [17:0] COUNTER;
    func_MCU_2 = 1'b0;
  endfunction
  function func_MCU_3;
    input [17:0] COUNTER;
    case (COUNTER)
      18'b010100010110011101: func_MCU_3 = 1'b0;
      default: func_MCU_3 = 1'b1;
    endcase
  endfunction
  // Mask Network Composed of AND Gates
  assign MASKED[0] = (MCU_OUT[0] == 1'b0)? 1'b0 : RAW[0];
  assign MASKED[1] = (MCU_OUT[1] == 1'b0)? 1'b0 : RAW[1];
  assign MASKED[2] = (MCU_OUT[2] == 1'b0)? 1'b0 : RAW[2];
  assign MASKED[3] = (MCU_OUT[3] == 1'b0)? 1'b0 : RAW[3];
endmodule
```

Position Information of Risky Response Bits

Fig. 7. Sample Verilog design file for partial-mask circuitry.

D. CPS-BIST Design Example

Fig. 7 shows a sample Verilog design file for part of the masking circuitry (including the mask network and the mask control unit but without the counter) for the partial-mask CPS-BIST scheme illustrated in Fig. 4 (a). Here, the number of pseudo-random test vectors to be applied in logic BIST is set to 50,000. Since there are 4 scan chains and 3 scan slices, an 18-bit counter for scan slice counting, a 4-bit mask control unit (MCU) and a mask network composed of four AND gates are used. The major portion of this design file is surrounded by the red frames, which is automatically created by using the position information of risky response bits (***I*** in Fig. 6), represented by the counter content and obtained by LSP-based capture power safety checking (***H*** in Fig. 6).

IV. Experimental Results

Comprehensive evaluation was conducted by using six large ITC'99 circuits *(b17~b22)* as well as an industrial circuit (*dpro*), whose statistics are as shown in Table I, on a workstation with an Intel Xeon® 3.33GHz CPU and a 24GB main memory. Design Complier® from Synopsys and a commercial 90nm cell library was used for synthesizing the complete CPS-BIST circuit in order to assess the area overhead of the masking circuitry.

The BIST configuration was `<#-Scan-Chains=200, PRPG-Bit-Width=2, Phase-Shifter=20-to-200, Space-Compactor=200-to-20, MISR-Bit-Width=20>`. In all experiments, 10,000, 30,000, and 50,000 pseudo-random test vectors were applied. Their capture power safety was determined by LSP-based capture safety checking (***H*** in Fig. 6), in which the threshold *PATHLIMIT* for determining whether a path is long or not was set to 70% and 80% of the longest structural path in a circuit, while the threshold *WSALIMIT* for determining whether the launch switching activity in the impact area of a long sensitized path is excessive or not was set to 20% of the maximum WSA in the impact area of the path, which is calculated by assuming all gates in the impact area have transitions.

Experimental results are summarized in Table IV. Here, `# TV` is the number of pseudo-random test vectors, `# LSP` is the number of long sensitized paths, `# Risky Paths` is the number of risky paths, `# Risky Response Bits` is the number of risky response bits, and `# Risky Test Vectors` is the number of risky test vectors. The impact of the proposed CPS-BIST scheme (with both *partial-mask* and *full-mask* options) on test quality was evaluated by percentage change in fault coverage (`Δ FC`). In addition, the increase in circuit size (`% area overhead`) and total execution time (`CPU`) were also obtained.

The results of Table 4 shows that CPS-BIST can indeed achieve capture power safety with negligible impact on test quality and area overhead. In addition, the following important observations can be made.

(1) The fault coverage loss for both partial-mask and full-mask options in CPS-BIST is negligible but area overhead of partial-mask is higher than that of full-mask. *This indicates that full-mask CPS-BIST is a preferable solution for practical use*.

(2) Extremely good results (negligible fault coverage loss as well as negligible area overhead) have been obtained for the largest ITC'99 circuit (*b19*) and the large industrial circuit (*dpro*). *This indicates that the larger a circuit, the better performance of CSP-BIST*.

(3) Different from conventional low-power BIST, CPS-BIST does not reduce capture power. Instead, it allows the existence of excessive capture power but uses the on-chip hardware-based masking mechanism to prevent the impact of excessive capture power from invalidating the BIST signature. *This has proved the feasibility of achieving capture power safety in logic BIST by the well-known technique of masking*.

TABLE IV. EXPERIMENTAL RESULTS

Circuit	# TV	PATH LIMIT (%)	WSA LIMIT (%)	# LSP	# Risky Paths	# Risky Response Bits	# Risky Test Vectors	Δ FC (%)		Area Overhead (%)		CPU (*Sec.*)
								Partial-Mask	Full-Mask	Partial-Mask	Full-Mask	
b17	10000	70	20	125	101	377	41	-0.0074	-0.0445	0.4676	0.4543	1113
		80	20	9	0	0	0	0	0	0.0000	0.0000	2967
	30000	70	20	471	336	1244	131	-0.0099	-0.3364	0.9951	0.8088	4196
		80	20	22	8	9	1	0	0	0.0859	0.0462	5375
	50000	70	20	732	581	2045	218	-0.0037	-0.1534	1.4995	1.2401	4197
		80	20	66	51	37	4	0	0	0.1461	0.1004	5376
b18	10000	70	20	26	26	9	1	-0.0089	-0.1564	0.0271	0.0173	2590
		80	20	0	0	0	0	0	0	0.0000	0.0000	2543
	30000	70	20	40	32	19	1	-0.0096	-0.1537	0.0272	0.0200	10006
		80	20	8	8	9	1	-0.0092	-0.1537	0.0272	0.0171	10163
	50000	70	20	55	52	9	1	0	-0.0476	0.0272	0.0161	10527
		80	20	0	0	0	0	0	0	0.0000	0.0000	12101
b19	10000	70	20	0	0	0	0	0	0	0.0000	0.0000	6966
		80	20	0	0	0	0	0	0	0.0000	0.0000	6960
	30000	70	20	75	73	83	8	-0.0128	-0.2593	0.0310	0.0308	19544
		80	20	0	0	0	0	0	0	0.0000	0.0000	20591
	50000	70	20	297	297	73	6	-0.0023	-0.0405	0.0270	0.0261	29594
		80	20	4	4	10	1	0	-0.0034	0.0132	0.0084	25886
b20	10000	70	20	1260	1260	690	61	-0.0838	-0.9459	1.2026	0.5804	755
		80	20	5	5	20	2	-0.0003	-0.0316	0.1071	0.0654	780
	30000	70	20	5359	5359	4559	384	-0.0156	-0.0996	6.0246	1.7905	2489
		80	20	16	16	38	4	0	0	0.1447	0.1065	2693
	50000	70	20	10459	10456	7157	607	-0.0101	-0.0606	7.7729	2.8072	3814
		80	20	50	50	97	10	0	-0.0011	0.2482	0.2249	3728
b21	10000	70	20	3786	3786	1574	120	-0.0322	-0.2844	2.4491	0.7643	814
		80	20	113	113	88	7	0	-0.0167	0.1943	0.1900	812
	30000	70	20	9317	9317	4601	344	-0.0278	-0.1211	5.5283	1.7097	2742
		80	20	237	237	335	29	-0.0033	-0.0089	0.6137	0.4713	2928
	50000	70	20	22866	22866	8387	612	-0.0067	-0.0689	7.0312	2.7853	3000
		80	20	1044	1044	582	45	0	-0.0032	1.0073	0.6210	3127
b22	10000	70	20	5636	5633	3675	287	-0.0643	-0.5043	3.9880	0.9006	1236
		80	20	15	15	58	6	0	-0.0076	0.1085	0.0954	1206
	30000	70	20	16605	16590	11949	901	-0.0318	-0.1921	7.5467	2.0130	4185
		80	20	81	81	244	24	0	-0.0053	0.3030	0.2856	4108
	50000	70	20	26479	26446	19332	1462	-0.0197	-0.1225	10.2411	2.9158	5563
		80	20	148	148	265	25	0	-0.0068	0.3323	0.2980	4891
dpro	10000	70	20	0	0	0	0	0	0	0.0000	0.0000	56234
		80	20	0	0	0	0	0	0	0.0000	0.0000	54543
	30000	70	20	160	73	29	3	0	0	0.0030	0.0029	181880
		80	20	0	0	0	0	0	0	0.0000	0.0000	171385
	50000	70	20	94	22	29	3	0	0	0.0030	0.0027	249057
		80	20	0	0	0	0	0	0	0.0000	0.0000	232618

("0.0000" means "<0.00004")

V. CONCLUSIONS

This paper is the first that has explicitly addressed the issue of capture power safety (instead of capture power reduction) in scan-based logic BIST by using the well-known technique of masking. The proposed solution, ***capture-power-safe BIST*** (**CPS-BIST**), directly achieves capture power safety in a guaranteed manner by using ***partial-mask*** or ***full-mask*** to prevent excessive-capture-power-induced uncertain test responses (identified by long-sensitized-path-based capture power safety checking in a pinpoint manner) from reaching the MISR. This paper has also revealed an important property that uncertain test responses in logic BIST are actually very few. This indicates that the masking-based CPS-BIST can achieve capture power safety in logic BIST with negligible impact on test quality and area overhead. This has been confirmed by comprehensive evaluations with large benchmark and industrial circuits.

Future work includes (1) speeding-up the capture power safety checking procedure and (2) evaluating a programmable masking circuitry design (e.g., using memory instead of logic circuit) in CPS-BIST.

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