# FPGA-Based Implementation of Finite Set-MPC for a VSI System Using XSG-Based Modeling

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# FPGA-Based Implementation of Finite Set-MPC for a VSI System Using XSG-Based Modeling

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**Abstract:** Finite set-model predictive control (FS-MPC) is used for power converters and drives having unique advantages as compared to the conventional control strategies. However, the computational burden of the FS-MPC is a primary concern for real-time implementation. Field programmable gate array (FPGA) is an alternative and exciting solution for real-time implementation because of the parallel processing capability, as well as, discrete nature of the hardware platform. Nevertheless, FPGA is capable of handling the computational requirements for the FS-MPC implementation, however, the system development involves multiple steps that lead to the time-consuming debugging process. Moreover, specific hardware coding skill makes it more complex corresponding to an increase in system complexity that leads to a tedious task for system development. This paper presents an FPGA-based experimental implementation of FS-MPC using the system modeling approach. Furthermore, a comparative analysis of FS-MPC in stationary $\alpha\beta$ and rotating $dq$ frame is considered for simulation as well as experimental result. The FS-MPC for a three-phase voltage source inverter (VSI) system is developed in a realistic digital simulator integrated with MATLAB-Simulink. The simulated controller model is further used for experimental system implementation and validation using Xilinx FPGA: Zedboard Zynq Evaluation and Development Kit. The digital simulator termed as Xilinx system generator (XSG) provided by Xilinx is used for modeling-based FPGA design.

**Keywords:** field-programmable gate array; finite set-model predictive control; model-based design; voltage source inverter; Xilinx system generator

## 1. Introduction

Model predictive control (MPC) possess appealing characteristics such as flexibility of simultaneous handling of multiple constraints and easy inclusion of nonlinearities [1–4]. This leads to considerable attention to exploit the characteristics of MPC for a wide variety of applications. However, it suffers from the problem of high computation requirement that results in real-time implementation problems. Despite the fact of high computational requirement, the real-time implementation of predictive control for power converters is of considerable interest to improve the dynamic performance as well as to optimize the entire system performance by including additional constraints. MPC has been applied for two-level voltage source inverter (VSI) [5,6], three-level neutral-point clamped converter (NPC) [2,7], active front end rectifier [8,9], cascaded H-Bridge inverter [10–12], asymmetric flying capacitor converter [13], three-phase direct Matrix converters [14,15], predictive control for UPS applications [16,17], predictive torque control (PTC), and field oriented control (FOC) of an induction machine [2,18], to name a few.

The fundamental approach behind the MPC is to have an appropriate plant or system model for the prediction of the future behavior of control parameters. Finite set-model predictive control (FS-MPC), also known as finite control set-MPC, is a classification of MPC which utilizes a discrete-time model of power converter having a limited number of switching states for solving the optimization problem and the control action can be directly applied to the converter without the need of external modulator [2,9]. This method reduces the computational loads up to some extent as compared to generalized MPC method by considering the discrete nature of the power converter model. The optimization function (cost function) for FS-MPC is designed considering the primary control objectives such as current, voltage, or power and any additional constraints. In general, the cost function is formulated based on the stationary $\alpha\beta$ co-ordinates [19,20]. Considering current control with FS-MPC, the sinusoidal future current references need to be predicted accurately using an extrapolation method, however, the extrapolated reference causes unwanted oscillations that influence the transient response [7,9,19]. Considering the above issue, the cost function can be designed using a rotating $dq$ frame that does not require extrapolation method because of continuous current references [19]. However, the comparative analysis based on design constraints and performance indices is required to be addressed for two frames. Furthermore, the computational burden corresponding to each co-ordinate system is crucial for practical system implementation.

Because of the computational requirements, practical implementations of predictive controls for power converters mainly depend on the micro-processing solutions such as digital signal processor (DSP) [3,4,18]. The computation required for the algorithm should strictly complete within a given sampling interval. However, delay in the computation of optimum switching state is observed that deteriorates the quality of waveforms [5,21]. To cope with this issue, delay compensation techniques are necessary to compute optimum switching state within the specified sampling interval [22,23]. Nevertheless, delay compensation techniques encounter additional issues of increased computational burden and an increased average switching frequency [22].

Field programmable gate array (FPGA) is a solution of choice because of parallel processing capability and distributed on-chip logic resources [24–31]. The FPGA-based system implementation makes the system compact, cost-effective for controller prototyping, and flexible for functional interfacing of devices according to our own choices. FPGAs consist of configurable logic blocks that can be utilized to realize various designs. One of the key features of FPGAs is its flexibility in hardware programmability and addressing a broader application area [30]. However, the system implementation using FPGA requires specific programming skill that is hardware description language (HDL) coding. Designing HDL code for a particular application is a tedious and time-consuming process toward controller development and considered more cumbersome with an increase in the level of controller complexity [25,26,32].

The controller development approach is crucial considering the FPGA-based real-time system implementation with an aspect of the straightforward utilization of the product in industrial applications. The digital simulator as a realistic virtual FPGA platform is advantageous considering the controller development process that facilitates an automatic code generation through the developed system to ease the FPGA-based system implementation. Moreover, model-based design (MBD) platform of the digital simulator provides system visualization and easy debugging that is appealing for rapid controller prototyping.

Xilinx system generator (XSG) as a digital simulator adopting MBD platform was used for the step-by-step design and modeling of the FS-MPC algorithm in $\alpha\beta$-frame in [31] for the load current control of three-phase VSI system. The performance of the FS-MPC was analyzed through the simulations in the integrated platform of XSG and MATLAB-Simulink considering steady state response and intermediate responses with the change in the sampling time. In [33], a hardware-in-the-loop (HIL) simulation methodology was adopted for the verification of the XSG-based FS-MPC in $\alpha\beta$-frame for a three-phase VSI system with motor load condition. The performance was tested for the step-by-step verification through simulations considering the controller in MATLAB-Simulink, XSG, and HIL

co-simulation. A comparative analysis was presented through the controller performance with the effect of sampling time and reference tracking under dynamic conditions.

This paper presents the FPGA-based real-time implementation of FS-MPC for experimental validation of controller modeled in the digital simulator (XSG). The FS-MPC is developed for a three-phase VSI system with RL load using an optimization function consisting of current control objectives considering both stationary $\alpha\beta$ and rotating $dq$ reference frames for comparative analysis. The functionality of MBD platform is demonstrated through some intermediate responses for the controller development in both frames. In addition, the change in reference current is considered for transient behavior and dynamic response analysis. The computational requirements for both frames based on an FPGA resource sharing are used for comparative analysis. The FPGA board used for the experimental system is the Zedboard Zynq Evaluation and Development Kit.

Other sections of this paper are organized as follows: Section 2 describes the algorithm of FS-MPC in both $\alpha\beta$ and $dq$ frames considering the discrete-time mathematical model of the three-phase VSI system. In Section 3, the model-based design and development of controller in the digital simulator is explained. Section 4 covers the simulation results with detailed discussion. The experimental setup and the validation of the system performance are presented in Section 5. Finally, appropriate conclusions are drawn in Section 6.

## 2. Finite Set-MPC

The power circuit of three-phase VSI with *RL* load is shown in Figure 1 where $R$ is the load resistance and $L$ is the load inductance. The FS-MPC based on current control objective uses a discrete-time model of the load current dynamic equation for the formulation of the control algorithm and deals only with a limited number of possible switching states of the power converter. The switching states of the converter are determined by the switching signals $S_a$, $S_b$, and $S_c$ as shown in Table 1. Considering all the possible switching combinations of the switching signals, eight switching states $S$ ($S_0$–$S_7$) and hence, eight voltage vectors $v_i$ ($v_0$–$v_7$) are obtained as shown in Table 2.

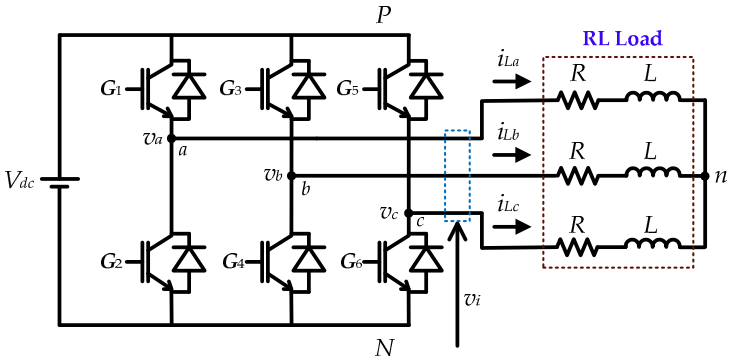



**Figure 1.** Power circuit of three-phase VSI with *RL* load.

**Table 1.** Gating signals of the inverter power switches.

| Leg '*a*', $S_a$ | Leg '*b*', $S_b$ | Leg '*c*', $S_c$ |
|---|---|---|
| $G_1$ ON, 1 | $G_3$ ON, 1 | $G_5$ ON, 1 |
| $G_2$ OFF, 0 | $G_4$ OFF, 0 | $G_6$ OFF, 0 |
| $G_1$ OFF, 0 | $G_3$ OFF, 0 | $G_5$ OFF, 0 |
| $G_2$ ON, 1 | $G_4$ ON, 1 | $G_6$ ON, 1 |

**Table 2.** Voltage vectors and switching states with index number.

| Switching States | | | Voltage Vectors | Index Number |
|---|---|---|---|---|
| $S = [S_a$ | $S_b$ | $S_c]$ | $v_i = [v_{i\alpha}\ v_{i\beta}]$ | |
| $S_0 = [0$ | 0 | 0] | $v_0 = [0, 0]$ | 0 |
| $S_1 = [1$ | 0 | 0] | $v_1 = [2V_{dc}/3, 0]$ | 4 |
| $S_2 = [1$ | 1 | 0] | $v_2 = [V_{dc}/3, \sqrt{3}V_{dc}/3]$ | 6 |
| $S_3 = [0$ | 1 | 0] | $v_3 = [-V_{dc}/3, \sqrt{3}\ V_{dc}/3]$ | 2 |
| $S_4 = [0$ | 1 | 1] | $v_4 = [-2V_{dc}/3, 0]$ | 3 |
| $S_5 = [0$ | 0 | 1] | $v_5 = [-V_{dc}/3, -\sqrt{3}V_{dc}/3]$ | 1 |
| $S_6 = [1$ | 0 | 1] | $v_6 = [V_{dc}/3, -\sqrt{3}V_{dc}/3]$ | 5 |
| $S_7 = [1$ | 1 | 1] | $v_7 = [0, 0]$ | 7 |

The load current dynamics behavior can be described by the vector differential equation as below:

$$\boldsymbol{v}_i = R\boldsymbol{i}_L + L\frac{d\boldsymbol{i}_L}{dt} \tag{1}$$

where inverter output voltage $\boldsymbol{v}_\mathrm{i}$ is defined as a vector form in terms of the phase-to-neutral voltages of three phases $a$, $b$, $c$ and expressed as follows:

$$\boldsymbol{v}_i = \frac{2}{3}\left(v_{aN} + e^{j(2\pi/3)}v_{bN} + e^{j(4\pi/3)}v_{cN}\right) \tag{2}$$

Similarly, three-phase load currents $\boldsymbol{i}_L$ can be expressed in terms of line currents $i_{La}$, $i_{Lb}$, $i_{Lc}$ of three phases as given below:

$$\boldsymbol{i}_L = \frac{2}{3}\left(i_{La} + e^{j(2\pi/3)}i_{Lb} + e^{j(4\pi/3)}i_{Lc}\right) \tag{3}$$

### *2.1. Discrete-Time Predictive Model*

The discrete-time model of the load current dynamics (1) for a sampling time $T_S$ represents the predictive model. It will be used to predict the future value of load currents considering all voltage vectors. The discrete-time model can be obtained by an approximation of load current derivative $d\boldsymbol{i}_L/dt$ using the forward Euler discretization method given as:

$$\frac{d\boldsymbol{i}_L}{dt} \approx \frac{\boldsymbol{i}_L(k+1) - \boldsymbol{i}_L(k)}{T_S} \tag{4}$$

After substituting (4) into (1), an expression of predicted future load current at sampling interval $k$+1, is obtained for each of the seven different voltage vectors $\boldsymbol{v}_\mathrm{i}(k)$ in $\alpha\beta$ frame as:

$$\begin{aligned} i^p_{L\alpha}(k+1) &= k_1 i_{L\alpha}(k) + k_2 v_{i\alpha}(k) \\ i^p_{L\beta}(k+1) &= k_1 i_{L\beta}(k) + k_2 v_{i\beta}(k) \end{aligned} \tag{5}$$

where $k_1 = \left(1 - \frac{RT_S}{L}\right)$, $k_2 = \frac{T_S}{L}$. $\boldsymbol{i}^p{}_{L\alpha,\beta}(k+1)$, and $\boldsymbol{i}_{L\alpha,\beta}(k)$ denotes the predicted future load currents at time $k+1$ and the measured load currents at instant $k$, respectively, in $\alpha\beta$-frame. The coordinate transforms from $abc$ to $\alpha\beta$ are computed using mathematical relation defined by Clarke transformation as:

$$\begin{bmatrix} x_\alpha \\ x_\beta \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 \\ 0 & \frac{1}{\sqrt{3}} & -\frac{1}{\sqrt{3}} \end{bmatrix} \begin{bmatrix} x_a \\ x_b \\ x_c \end{bmatrix} \tag{6}$$

where $x$ can be any quantity voltage or current.

The predicted load currents in rotating $dq$-frame considering feed-forward terms for the decoupling of the $d$ and $q$ components of the current using forward Euler discretization is given below:

$$\begin{aligned} i^{p}_{Ld}(k+1) &= k_1 i_{Ld}(k) + k_2\left\{v_{id}(k) + k_3 i_{Lq}(k)\right\} \\ i^{p}_{Lq}(k+1) &= k_1 i_{Lq}(k) + k_2\left\{v_{iq}(k) - k_3 i_{Ld}(k)\right\} \end{aligned} \tag{7}$$

where $k_1 = \left(1 - \frac{RT_S}{L}\right)$, $k_2 = \frac{T_S}{L}$, $k_3 = \omega^* L$, $\omega^*$ is the angular frequency of the current reference. The voltages $v_{id}$, $v_{iq}$ and currents $i_{Ld}$, $i_{Lq}$ can be computed using Park transformation relation to get $dq$ from $\alpha\beta$ components given as:

$$\begin{bmatrix} x_d \\ x_q \end{bmatrix} = \begin{bmatrix} \cos\theta^* & \sin\theta^* \\ -\sin\theta^* & \cos\theta^* \end{bmatrix} \begin{bmatrix} x_\alpha \\ x_\beta \end{bmatrix} \tag{8}$$

where $\theta^*$ is the reference phase angle for the coordinate conversion.

### 2.2. Selection Criteria

To select the optimum switching state according to optimum voltage vector in each sampling and to minimize the error between the predicted and reference variables, a selection criteria is required to be defined considering desired control objectives. A cost function is formulated by incorporating error between each predicted and reference control variables as well as any constraints.

A simple cost function considering current control objective is usually defined in terms of the orthogonal $\alpha\beta$ coordinates as follows:

$$g_{\alpha\beta} = \left|i^*_{L\alpha}(k+1) - i^{p}_{L\alpha}(k+1)\right| + \left|i^*_{L\beta}(k+1) - i^{p}_{L\beta}(k+1)\right| \tag{9}$$

where $i^*_{L\alpha}$ and $i^*_{L\beta}$ are the real and imaginary components of the reference current. The future reference current value required by (9) has to be predicted using Lagrange extrapolation formula [5]. However, for sufficient small $T_S$, a simple approximation $i^*_L(k+1) \approx i^*_L(k)$ can be used and no extrapolation is required. The same approximation is considered in this paper.

The cost function to control $d$ and $q$ components of the load current is formulated as:

$$g_{dq} = \left|i^*_{Ld}(k+1) - i^{p}_{Ld}(k+1)\right| + \left|i^*_{Lq}(k+1) - i^{p}_{Lq}(k+1)\right| \tag{10}$$

where $i^*_{Ld}$ and $i^*_{Lq}$ are the reference currents for $d$ and $q$ components, respectively.

In order to demonstrate the implementation methodology of the FS-MPC in two different coordinates, the schematic diagram of the load current control using FS-MPC with stationary $\alpha\beta$ and rotating $dq$ reference frames are depicted in Figure 2a,b, respectively.

## 3. Model-Based Design of FS-MPC

Model-based design of the FS-MPC is divided into three steps: computation of cost function, selection of optimum switching state, and generation of switching signals. The steps for modeling of the controller are described in the following subsections.

### 3.1. Computation of Cost Functions

The cost function is computed using the predictive model that is modeled using discrete-time mathematical equations described in Section 2. The computation of cost function corresponding to a voltage vector (for ex. $v_3$) is shown by the block diagram in Figure 3a,b for FS-MPC in $\alpha\beta$ and $dq$ frames, respectively. The modeling for the computation of predicted load currents and the cost function is represented for the FS-MPC in $\alpha\beta$-frame (Figure 3a) using (5) and (9) respectively. Similarly, the

model-based design for the load current prediction and the cost function computation is performed using (7) and (10) respectively for the FS-MPC in *dq*-frame (Figure 3b).

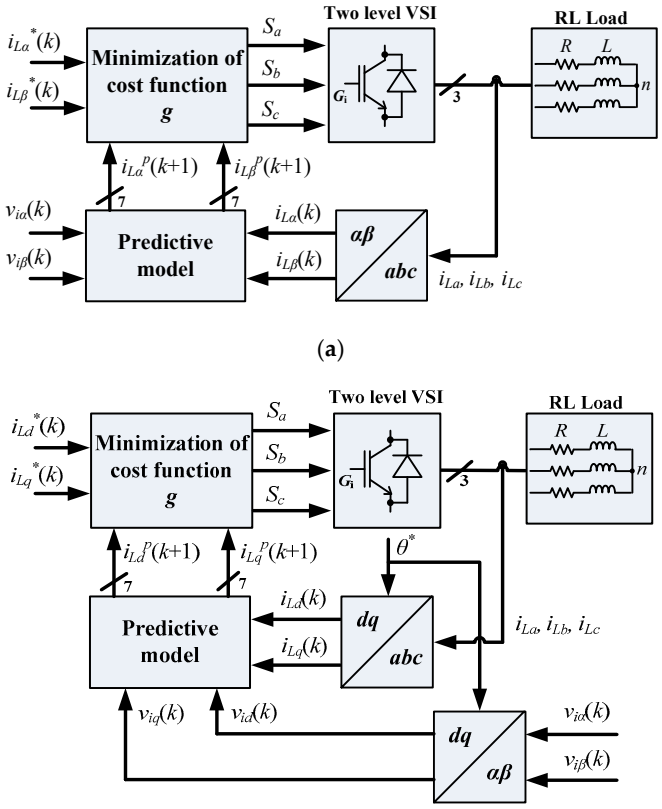



**Figure 2.** Schematic diagram of load current control using finite set-model predictive control (FS-MPC) in (**a**) $\alpha\beta$-frame and, (**b**) *dq*-frame.

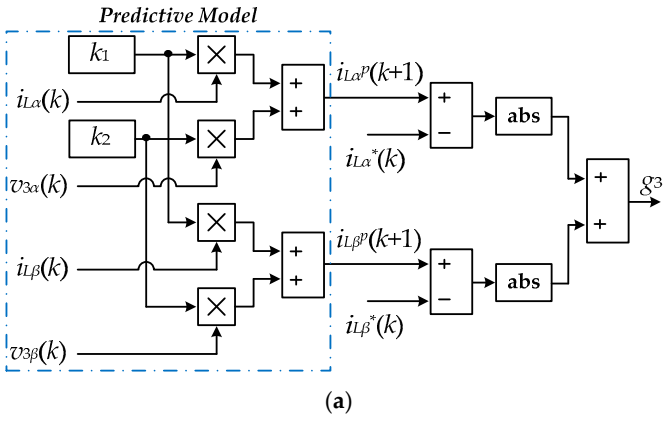



**Figure 3.** *Cont.*

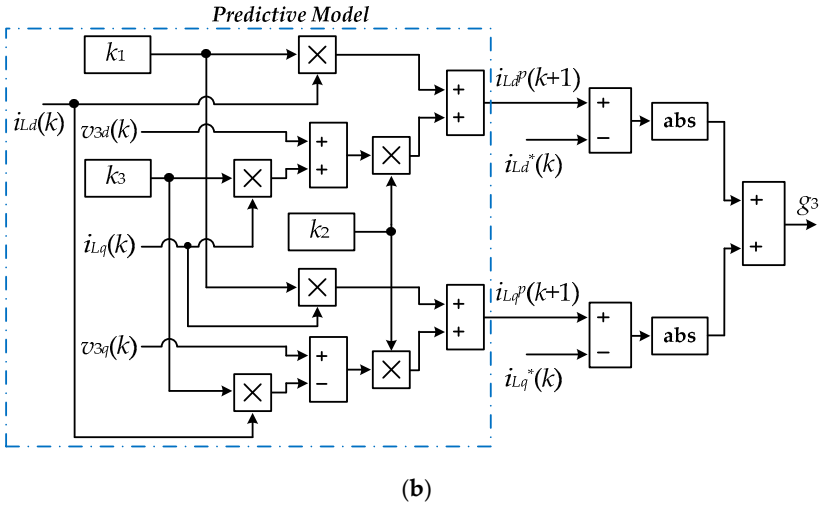



**Figure 3.** Block diagram representing modeling of a cost function for the FS-MPC in (**a**) $\alpha\beta$-frame and, (**b**) $dq$-frame using a voltage vector $v_3$.

Although only a single voltage vector ($v_3$) is considered for the demonstration of the modeling steps during the computation of cost function, the cost functions need to be computed for each inverter voltage vectors ($v_0$–$v_7$) defined for corresponding switching states ($S_a$, $S_b$, $S_c$) as given in Table 2 to select minimum cost function in each sampling interval.

### 3.2. Selection of Optimum Switching State

The block diagram for the selection of an optimum switching state $S_{opt}$ corresponding to the minimum cost function $g_{min}$ for each sampling interval is shown in Figure 4. A simple pipelining method is used to find the minimum among the computed cost functions. A logic to select a minimum between the two consecutive cost functions is developed using a comparator (C) and a 2:1 multiplexer (M). The output of the comparators (binary digit "0" or "1") are used as select lines ($sel_0$–$sel_6$) for the multiplexers in the combined C&M (C&M0 ~ C&M6) to select the minimum cost function ($g_{m0}$–$g_{m6}$) out of the two as shown in Figure 4a. Similar to the selection of $g_{min}$, an optimum switching state $S_{opt}$ is selected using the corresponding select lines ($sel_0$–$sel_6$) fed to the multiplexers (M0 ~ M6) by taking consecutive two switching states as shown in Figure 4b.

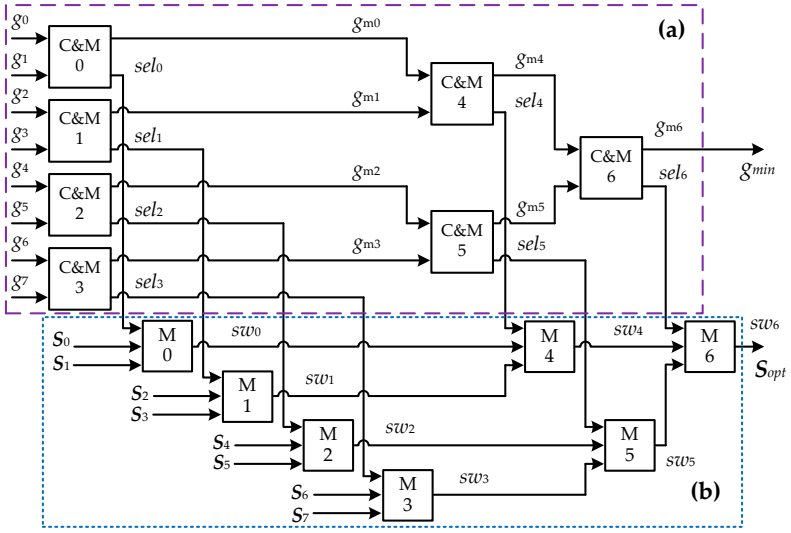



**Figure 4.** Block diagram to represent logic for the (**a**) selection of minimum of cost function, and (**b**) selection of optimum switching state.

### *3.3. Generation of Switching Signal and Index Number*

The switching signals corresponding to selected $S_{opt}$ is also generated through modeling. The 3-bit binary combination of $S_{opt}$ is sliced to generate switching signals for respective upper switches ($G_1$, $G_3$, $G_5$), and complementary switching conditions are applied to lower switches ($G_2$, $G_4$, $G_6$).

An index number is considered for an in-depth analysis purpose corresponding to eight possible voltage vectors ($v_0$–$v_7$) as mentioned in Table 2. The index numbers are defined considering the decimal equivalent of the binary values of $S_a$, $S_b$, $S_c$. For example, the index number is defined as "4" corresponding to $v_1$ having {$S_a$, $S_b$, $S_c$} as {1, 0, 0}. The $S_{opt}$ corresponding to the $g_{min}$ is used to select an index number that replicates the definite switching state selection in each sampling time.

The digital logic for the selection of $g_{min}$, selection of the $S_{opt}$, and the implementation of $S_{opt}$ to inverter through the model-based XSG (digital simulator) diagram was demonstrated in [31] based on the block diagram shown in Figure 4.

## 4. Simulation Results

To demonstrate the development approach of the controller in $\alpha\beta$ as well as $dq$ frames, a simulation methodology is represented in Figure 5. The power circuit of three-phase VSI is developed in MATLAB-Simulink using simscape power systems toolbox, whereas the controller is developed in the digital environment of XSG using XSG toolbox. A fixed-point number representation approach was adopted for the development of FS-MPC in both frames. The parameters considered for the simulation are as follows; supply DC voltage ($V_{dc}$): 145 V, load resistor ($R$): 10 Ω, load inductor ($L$): 10 mH, sampling time ($T_S$): 50 µs.

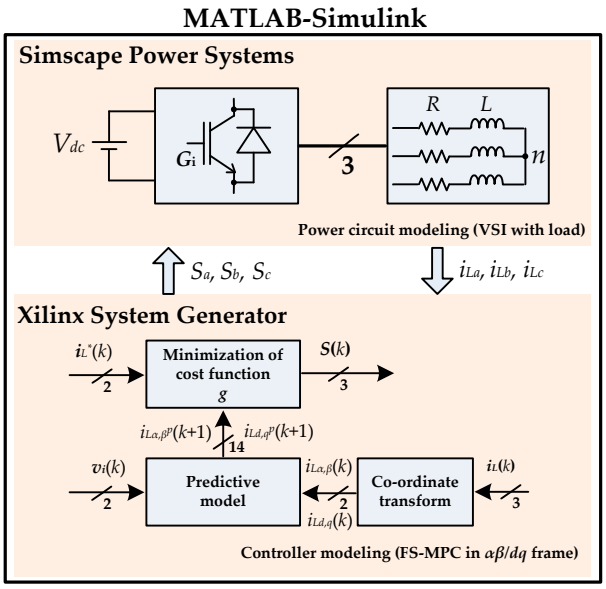



**Figure 5.** Block diagram representation for modeling and simulation.

### *4.1. System Performance*

The three-phase load currents ($i_{La}$, $i_{Lb}$, $i_{Lc}$) in Figure 6a,b are presented to validate the system performance with the FS-MPC implemented in $\alpha\beta$ and $dq$ frames, respectively. In order to investigate the dynamic performance of the FS-MPC for the three-phase VSI system, two step changes in reference current are considered for current tracking during the transients. The tracking performance of the load current is demonstrated for change in reference current from 2.5 A to 4 A at instant 0.062 s and from 4 A to 2.5 A at instant 0.14 s for the FS-MPC in $\alpha\beta$-frame (Figure 7a) and $dq$-frame (Figure 7b), respectively.

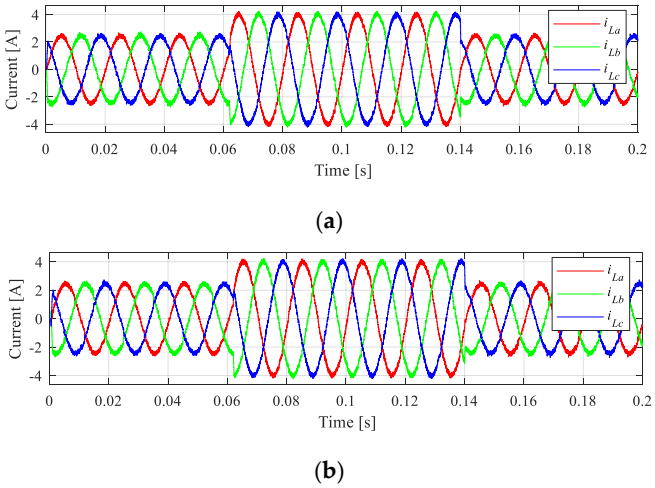



**Figure 6.** Simulation result: three-phase load current for the FS-MPC in (**a**) $\alpha\beta$-frame and (**b**) $dq$-frame.

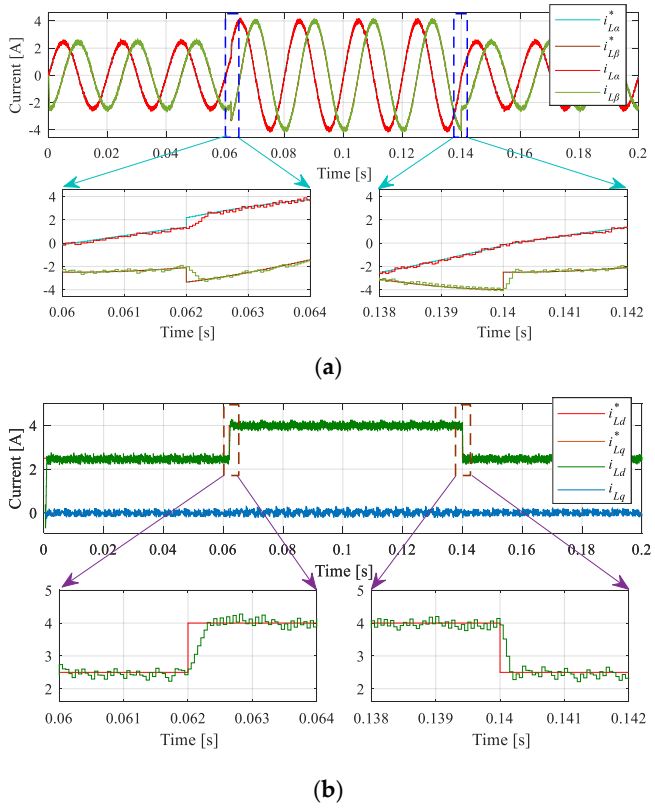
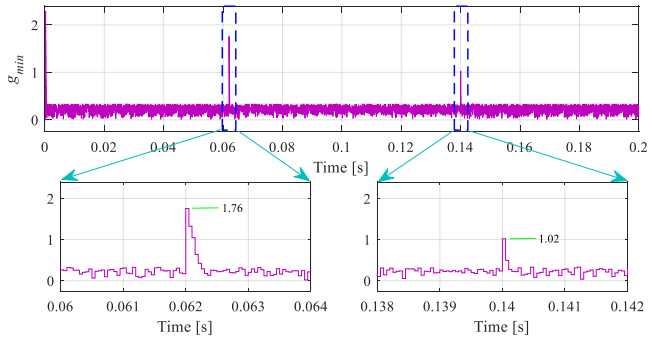



**Figure 7.** Simulation result: tracking performance of load current for the FS-MPC in (**a**) $\alpha\beta$-frame and (**b**) $dq$-frame.

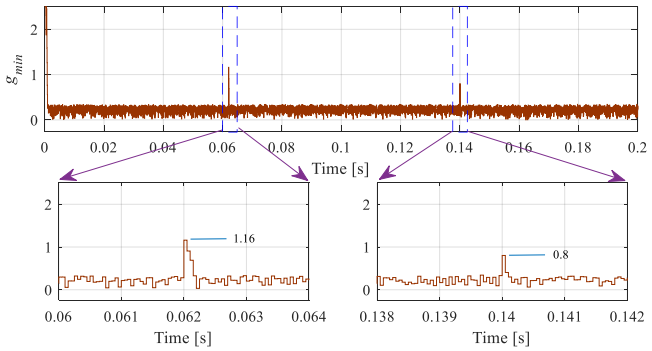
In the case of $dq$-frame, the step changes are applied in the $d$-axis component of the reference current, keeping $q$-axis reference current zero. The harmonic content in the load current is also analyzed considering both the frames. A higher percentage THD is observed for current reference of 2.5 A (5.28% in $\alpha\beta$-frame and 5.61% in $dq$-frame) as compared to reference current of 4 A having percentage THD 3.54% in $\alpha\beta$-frame and 3.74% in $dq$-frame. The THD for lower current reference is not the same in $\alpha\beta$ and $dq$ frames, however, the THD is almost the same for higher reference current condition. The slight difference in THD may be due to the different mathematical computation for $\alpha\beta$ and $dq$ frames.

### *4.2. Intermediate Response*

The intermediate responses are vital not only for the design and development of the controller, but also for in-depth analysis. In this paper, the performance of FS-MPC is analyzed considering the intermediate responses: minimum cost function $g_{min}$ and index number at each sampling interval. The selected $g_{min}$ represents the minimum current error and index number represents the switching state $\boldsymbol{S}_{opt}$ at each sampling interval. The value of $g_{min}$ are shown in Figure 8a,b for the FS-MPC in $\alpha\beta$ and $dq$ frames, respectively. Further, the index number of the selected $\boldsymbol{S}_{opt}$ corresponding to the $g_{min}$ at each sampling interval are shown in Figure 9a,b for the FS-MPC in $\alpha\beta$ and $dq$ frames, respectively.

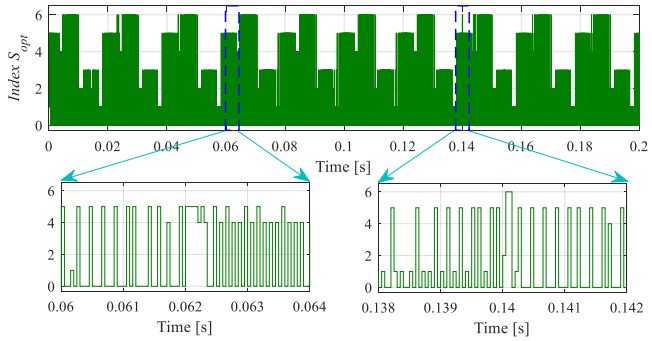



(**a**)



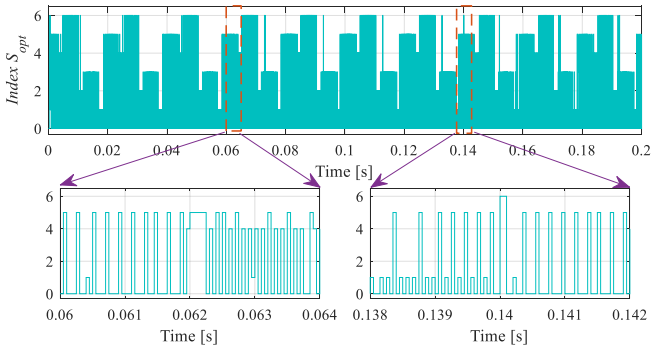

(**b**)

**Figure 8.** Simulation results: the values of minimum cost function $g_{min}$ for the FS-MPC in (**a**) $\alpha\beta$-frame and (**b**) $dq$-frame.




(**a**)

**Figure 9.** *Cont.*




(**b**)

**Figure 9.** Simulation result: the index number of selected optimum switching state $S_{opt}$ in each sampling interval for the FS-MPC in (**a**) $\alpha\beta$-frame and (**b**) $dq$-frame.

The index number is almost following the same profile for each cycle of current. However, the selected $S_{opt}$ in each sampling intervals is not identical in $\alpha\beta$ and $dq$ frames that signify the different selection of optimum voltage vectors, consequently having the non-identical minimum current error.

The intermediate responses are intentionally demonstrated as enlarged view during the instant of transients caused by the step change in reference current. The minimum current error in Figure 8 is possessing a sharp spike at the instant of change in reference current. The value of the current spike in $dq$-frame is lower as compared to the $\alpha\beta$-frame. The intermediate responses for selection of minimum cost function and the index number corresponding to optimum switching state is analyzed for modeling and implementation of FS-MPC.

## 5. Experimental Results

The experimental setup for real-time implementation of the FS-MPC is represented using block diagram as shown in Figure 10. The laboratory prototype of the experimental setup is depicted in Figure 11 and the experimental system components used for the development of laboratory prototype are listed in Table 3. The FPGA code was generated automatically through the modeled controller and programmed using dedicated software (Xilinx Vivado Design Suite) for real-time operation of VSI system with FS-MPC.

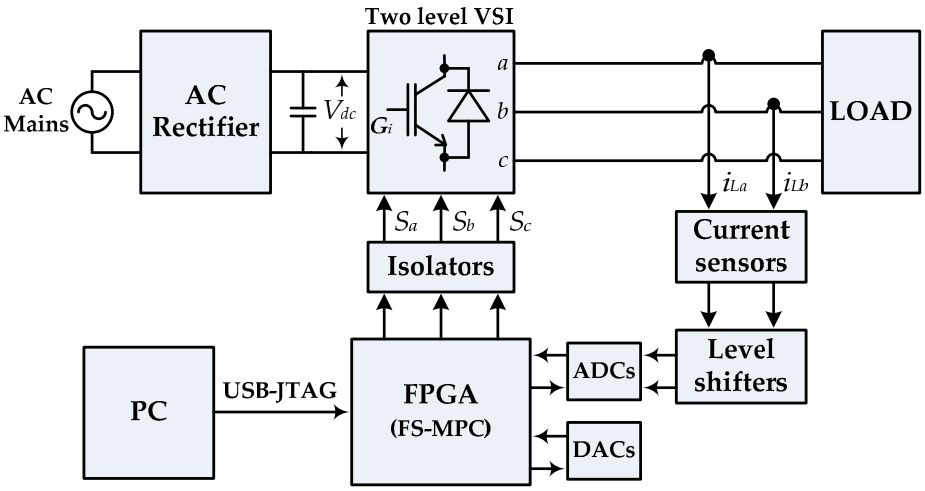



**Figure 10.** Block diagram of experimental setup.

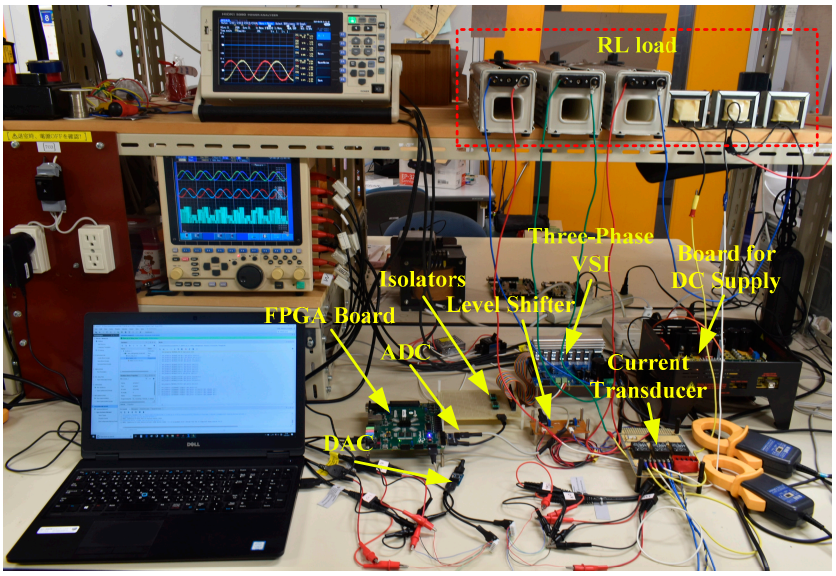



**Figure 11.** Laboratory prototype of the experimental setup.

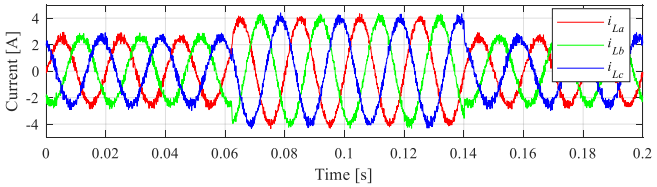
**Table 3.** Description of components specifications for the experimental system.

| S. No. | Components | Specifications |
|---|---|---|
| 1 | Three-phase VSI | STEVAL-IHM023V3, 1 kW |
| 2 | DC supply | THDSHVMTRPFCKIT |
| 3 | Current transducer | LA 25-NP |
| 4 | Op-amp IC for level shifter | LM385N |
| 5 | Isolator IC | ADuM3440 |
| 6 | ADC | Digilent Pmod AD1 |
| 7 | DAC | Digilent Pmod DA4 |
| 8 | FPGA board | Zedboard Zynq Evaluation and Development Kit |

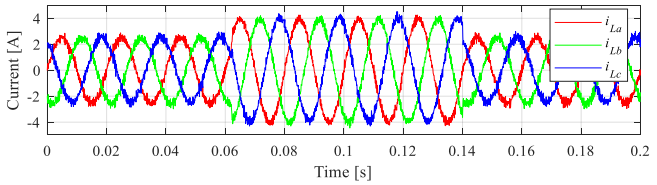
The performance of the FS-MPC in $\alpha\beta$ and $dq$ frames was experimentally evaluated and the experimental data are obtained through HIOKI 8855 Memory Hicorder. Further, the data are plotted with the help of MATLAB plotting tool for demonstration and analysis of experimental results.

### *5.1. System Performance*

The FS-MPC in both frames is experimentally validated for system performance analysis considering the same system parameters as in the case of simulation. The three-phase load currents ($i_{La}$, $i_{Lb}$, $i_{Lc}$) are shown in Figure 12a,b for the FS-MPC in $\alpha\beta$ and $dq$ frames, respectively. Further, the dynamic response is demonstrated in Figure 13a,b for the FS-MPC in $\alpha\beta$ and $dq$ frame, respectively, with the same step change in reference current as adopted in the simulation (2.5 and 4 A at instants 0.062 s and 0.14 s respectively). In order to investigate the dynamic response of the FS-MPC, the time span is intentionally expanded to demonstrate the current tracking during the transient caused by step changes in reference current.

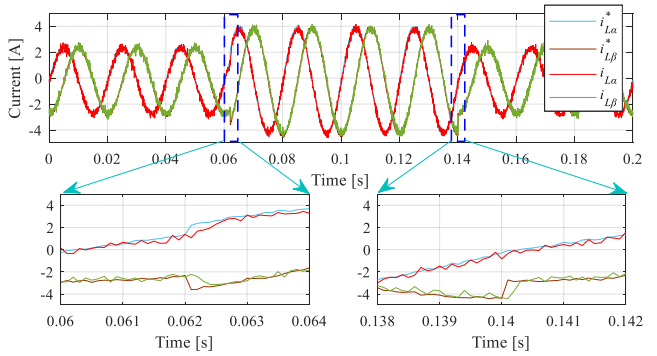



(**a**)

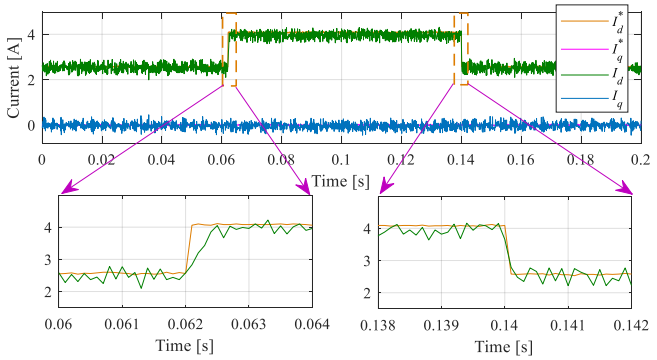



(**b**)

**Figure 12.** Experimental result: three-phase load current for the FS-MPC in (**a**) $\alpha\beta$-frame and (**b**) $dq$-frame.




(**a**)



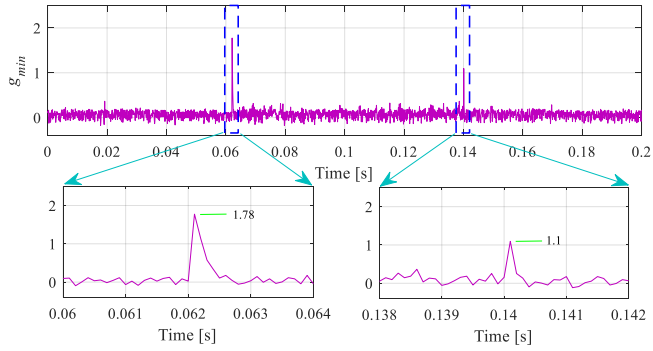

(**b**)

**Figure 13.** Experimental result: tracking performance of load current for the FS-MPC in (**a**) $\alpha\beta$-frame and (**b**) $dq$-frame.

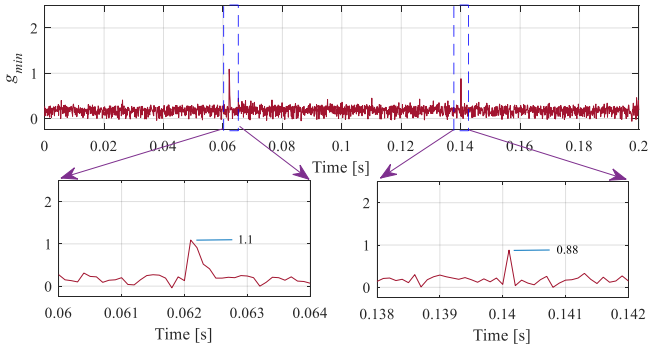
The harmonic content in the load current during the experiment was measured through HIOKI power analyzer and current clamp sensor. The percentage THD in load current is 7.91% in $\alpha\beta$-frame, 8.15% in $dq$-frame for current reference of 2.5 A and 4.9% in $\alpha\beta$-frame, 4.8% in $dq$-frame for current reference of 4 A. Considering the simulation results, the current THD is significantly high during the experiment for lower current reference as compared to higher current reference. However, the difference between the percentage THD through the implementation with the FS-MPC in $\alpha\beta$ and $dq$ frame is smaller during the experiment as compared to the simulation.

### 5.2. Intermediate Response

The value of $g_{min}$ and the index number at each sampling interval are demonstrated in Figures 14 and 15 for the FS-MPC in $\alpha\beta$ and $dq$ frames, respectively. The index number profile for $\boldsymbol{S}_{opt}$ is similar to that analyzed during the simulations for each sampling interval. The non-identical nature of selected $\boldsymbol{S}_{opt}$ with respect to sampling interval validates the different selection of optimum voltage vectors, consequently the different minimum current error between the FS-MPC in $\alpha\beta$ and $dq$ frames.




(**a**)

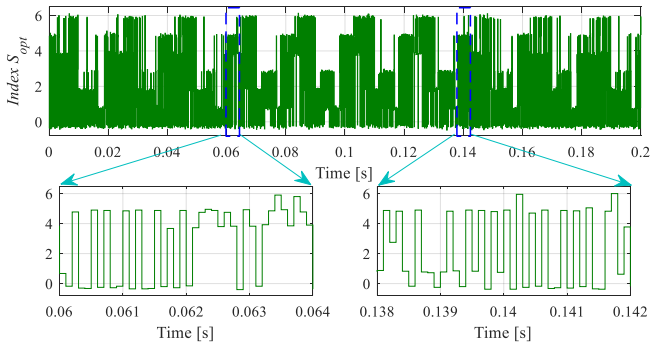



(**b**)

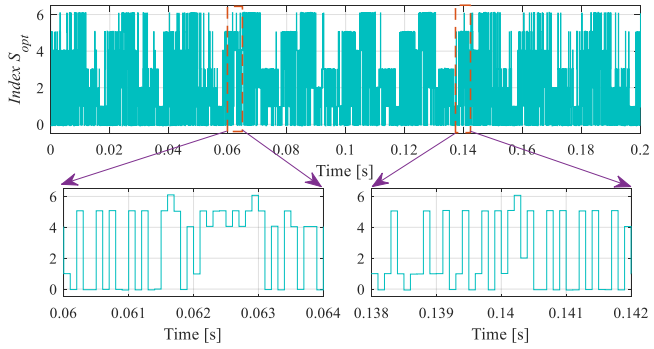
**Figure 14.** Experimental results: the values of minimum cost function $g_{min}$ for the FS-MPC in (**a**) $\alpha\beta$-frame and (**b**) $dq$-frame.

Similar to the simulation results, $g_{min}$ shows a sharp spike at the instant of step change and the value of the current spikes in the case of $\alpha\beta$ frame is higher than $dq$ frame. In addition, the value of current spikes during simulation and experiment is almost the same for both the frames.

In order to summarize the results obtained during simulation (Sim.) as well as experiments (Exp.) with both frames, a comparative analysis is presented in Table 4. The average switching frequency ($f_{SW}$) is also depicted in the same table with the percentage THD in load current corresponding to the load changes. There is a noticeable difference between the average $f_{SW}$ during the simulation and the experiment. A higher value of the average $f_{SW}$ during the simulation may be due to the ideal power switches and absence of realistic inductive load properties. The average $f_{SW}$ in $\alpha\beta$ and $dq$ frame for experiment is almost similar. However, the slight difference in THD as well as average switching frequency is maybe due to the different mathematical computation in $\alpha\beta$ and $dq$ frames. In addition, usually there are difference in performance between both frames and a decoupling term is included in $dq$-frame to compensate the computational difference of the $\alpha\beta$ and $dq$ frame.




(**a**)




(**b**)

**Figure 15.** Experimental results: the index number of selected optimum switching state $S_{opt}$ in each sampling interval for the FS-MPC in (**a**) $\alpha\beta$-frame and (**b**) $dq$-frame.

### *5.3. FPGA Resource Utilization*

Digital logic resources of an FPGA are used during the implementation of the controller in real-time. The configurable logic blocks (CLBs) are the main constituents of the FPGA resources. A CLB element contains a pair of slices where a slice is composed of look-up tables (LUTs) and flip-flops (FFs) [34,35]. An FPGA chip consists of large arrays of LUTs. LUTs are used for making digital logics for desired system designs, whereas flip-flops are binary shift registers used to synchronize logic and save logical states between clock cycles within an FPGA circuit. The number of LUTs and flip-flops in a single slice varies based on the family of the FPGA chip. In 7 series FPGAs, a slice contains four LUTs and eight flip-flops [35]. In addition, DSP slices are a major component of the FPGA resources that are mainly used to implement signal processing functions. A DSP slice is composed of signed multiplier, adder/accumulator, arithmetic logic unit (ALU), and many more [36].

In order to analyze the complexity level between the FS-MPC developed in $\alpha\beta$ and $dq$ frames, the resource utilization of FPGA are summarized in Table 5. The number of slice LUTs and DSP cells show higher resource utilization for the case of FS-MPC in $dq$-frame. DSP cells utilization is nearly three times higher for $dq$-frame than $\alpha\beta$-frame. A higher FPGA resource utilization in the case of the FS-MPC in $dq$-frame is due to the additional coordinate transformation ($\alpha\beta$ to $dq$) for voltage vectors including measured current, reference phase angle $\theta^*$ generation using CORDIC SINCOS, and an extra effort for computation of feed-forward term used for decoupling.

**Table 4.** Comparative analysis chart for the FS-MPC in two frames.

| Performance Indices | FS-MPC in $\alpha\beta$-Frame | | FS-MPC in $dq$-Frame | | Comments |
|---|---|---|---|---|---|
| | Sim. | Exp. | Sim. | Exp. | |
| Current error (spike) at instant 0.062 s | 1.76 | 1.78 | 1.16 | 1.1 | 1. lower for $dq$-frame<br>2. quite similar in experiment as compared to simulation for both frames |
| Current error (spike) at instant 0.14 s | 1.02 | 1.1 | 0.8 | 0.88 | 1. quite similar for both frames<br>2. slightly lower for $dq$-frame |
| THD and average $f_{SW}$ for $i_L$ = 2.5 A | 5.28%<br>3053 Hz | 7.91%<br>2310 Hz | 5.61%<br>3306 Hz | 8.15%<br>2350 Hz | 1. higher for $dq$-frame<br>2. significantly high in experiment for both frames |
| THD and average $f_{SW}$ for $i_L$ = 4 A | 3.54%<br>3733 Hz | 4.9%<br>2550 Hz | 3.74%<br>3920 Hz | 4.8%<br>2580 Hz | 1. quite similar for both frames<br>2. slightly high in experiment |
| Transient response: Settling time for step change at 0.062 s | 200 µs | 400 µs | 250 µs | 500 µs | 1. significantly high in experiment for both frames<br>2. slightly higher for $dq$-frame |
| Transient response: Settling time for step change at 0.14 s | 150 µs | 280 µs | 130 µs | 200 µs | 1. high in experiment for both frames<br>2. slightly lower for $dq$-frame |

**Table 5.** Field-programmable gate array (FPGA) resource utilization for the FS-MPC implementation.

| Logic Utilization Indices | Available | Used | | Utilization Percentage | |
|---|---|---|---|---|---|
| | | $\alpha\beta$-Frame | $dq$-Frame | $\alpha\beta$-Frame | $dq$-Frame |
| Number of slice LUTs | 53,200 | 4364 | 8534 | 8.2% | 16.04% |
| Number of FFs | 106,400 | 1078 | 1327 | 1.01% | 1.25% |
| Number of DSP cells | 220 | 25 | 66 | 11.36% | 30% |

## 6. Conclusions

This paper presents an FPGA-based real-time implementation of the FS-MPC in $\alpha\beta$ as well as $dq$ coordinates for the load current control of a three-phase VSI system. The FS-MPC algorithm is developed in a digital simulator of Xilinx which is an integrated platform with MATLAB-Simulink. A modeling approach was adopted for controller development to have an insight into the FS-MPC performance. To demonstrate the functionality of the modeling approach, the intermediate responses such as minimum cost function and index number are presented considering step-by-step analysis. The system performance is validated through simulation results and experimental results considering the dynamic behavior during transients for the FS-MPC in both frames as summarized in Table 4.

The current error spike during transient is almost the same for the simulation and experiment results that authenticates the realistic controller modeling in a digital simulator. However, the percentage THD of load current is higher in experiments as compared to the simulations that are because of the simplified model of the VSI and the load used for the simulation study. In addition, in $\alpha\beta$-frame slightly better percentage THD is achieved as compared to $dq$-frame in the simulation as well as the experiment. The system implementation through the FS-MPC in $dq$-frame can be used for in-depth system analysis, however, for the real-time implementation $\alpha\beta$-frame should be preferred as it has 2–3 times lower complexity considering the overall FPGA resource utilization.

**Author Contributions:** The manuscript preparation including system design, simulation, and experiments was performed by V.K.S. The idea of controller modeling was suggested by R.N.T. The work was completed under the supervision of T.H., R.N.T. and T.H. also contributed to the manuscript correction. All authors have read and agreed to the published version of the manuscript.

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