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Ratioless full-complementary 12-transistor static random access memory for ultra low supply voltage operation

Ratioless full-complementary 12-transistor static random access memory for ultra low supply voltage operation

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In this study, a ratioless full-complementary 12-transistor static random access memory (SRAM) was developed and measured to evaluate its operation under an ultra low supply voltage range. The ratioless SRAM design concept enables a memory cell design that is free from the consideration of the static noise margin (SNM). Furthermore, it enables a SRAM function without the restriction of transistor parameter (W/L) settings and the dependence on the variability of device characteristics. The test chips that include both conventional six-transistor SRAM cells and the ratioless full-complementary 12-transistor SRAM cells were developed by a 180 nm CMOS process to compare their stable operations under an ultra low supply voltage condition. The measured results show that the ratioless full-complementary 12-transistor SRAM has superior immunity to device variability, and its inherent operating ability at the supply voltage of 0.22 V was experimentally confirmed.

1. Introduction

For static random access memory (SRAM) using state-of-the-art processes of deep-submicron generation, it is becoming difficult to secure operating margins owing to the decrease in the power supply voltage and the increase in the device characteristic variation. Figure 1(a) shows a conventional six-transistor CMOS SRAM cell that has been widely used until now. In this circuit, the write operation is performed by transferring the data of bit lines through transfer transistors, while the read operation is performed by outputting the stored data to the bit lines through the same transfer transistors without destroying the data in the memory cell. To achieve both secure write and read operations with the same transfer transistors, the size of the transfer transistors should satisfy the allowable impedance ratios that are so-called β-ratio and γ-ratio. As a method of quantitative evaluation for this design margin in SRAM cells, the static noise margin (SNM) index shown in Fig. 1(b) is generally used.[1-4] There are two types of SNM, namely, read-SNM (RSNM) and write-SNM (WSNM). A stable operation of a memory cell should satisfy both RSNM>0 and WSNM>0. Considering both the device characteristic variation and the device characteristic aging effect, the SNMs should be as high as possible to achieve a stable SRAM operation under various voltage and temperature conditions. In recent years, with device dimensions becoming very small, it is becoming difficult to secure these two SNMs simultaneously.

Various techniques have been proposed to overcome this problem; however, all the circuits proposed as SRAM cells require either the ratio design or dynamic control in the three states of write, read, and write-half-select.[5-23] We proposed a ratioless SRAM design with the ratioless 10-transistor SRAM cell.[24] This enables the memory cell design that is free from the consideration of SNM. We call the cell as a 'ratioless SRAM cell' since its operation is secured regardless of the sizes of all the transistors.

In this study, we developed the ratioless 12-transistor SRAM (RL-12T-SRAM) test chip and measured it to evaluate its operation at ultra low supply voltages. This study consists of the following sections. In Sect. 2, previously proposed circuit techniques to improve the SRAM operating margins are briefly reviewed. In Sect. 3, the ratioless SRAM operation is explained. In Sect. 4, a test chip design using a 180 nm CMOS process and its experimental results of the minimum operating supply voltage and fail-bit distribution at ultra low voltages are explained. In Sect. 5, the effect of device variability on SRAM operations is discussed by comparing the measured data with the simulated results.

2. Prior improvements for SRAM operation margins

In order to improve the operating margins for SRAM, various techniques have been proposed.[5-23] First, there are various techniques that try to improve RSNM and WSNM independently by optimizing the word line potential (V_{wl}) and/or the voltage of the power supply of the memory cell (V_{cell}) during read and write operations; however, these techniques still require the ratio design [Fig. 2(a)].[5] Second, there are other approaches to add more transistors to the memory cell. A circuit named 8T-SRAM has been proposed [Fig. 2(b)].[14] In this method, RSNM may be freely set since it has a dedicated read buffer. It is also possible to design the read cell current without any restriction in ratio design. However, with 8T-SRAM, in order to avoid the problem of half-selection during the write operation, either combining it with the write-after-read technique or further adding transistors to enable the cross-point selection by the row (WLx) and column (WLy) word lines is required, as shown in Figs. 2(c) and 2(d).[16-19] As a different approach, a technique has been proposed to make WSNM free by breaking the flip/flop loop during the write operation [Fig. 2(e)].[20] With a similar concept, another 7T configuration shown in Fig. 2(f) has been proposed to make RSNM temporarily free by dynamically breaking the loop during the read cycle.[21] In another category, there are 1-bit register file circuits that are shown in Figs. 2(g) and 2(h). These register file circuits are composed of ten transistors and they make both RSNM and WSNM free by collapsing V_{cell} or breaking the flip/flop loop and by having a dedicated read buffer such as the 8T cell.[22-23] These cells achieve a subthreshold operation; however, they cannot be directly applied to the SRAM cell array because the write-half-select problem is not solved because all the cells that share the same word line are accessed in the register file application. The conventional techniques discussed above are summarized in Table I. Some techniques have abilities of near-threshold or subthreshold operation.[17-23] However, all the circuits proposed as SRAM cells require either the ratio design or dynamic control in the three states of write, read, and write-half-select. Additionally, the register file design does not consider the write-half-select state that is mandatory for SRAM applications. It is expected that sufficiently satisfying both RSNM and WSNM will be severely difficult for the existing circuit techniques in applications that require the robustness for operation over wide PVT variations.

3. Ratioless 12-transistor SRAM operation

To overcome this problem, we proposed a ratioless SRAM design with the ratioless 10-transistor SRAM cell.[24] Figures 3(a) and 3(b) show the basic logic block diagrams for the conventional six-transistor SRAM (6T-SRAM) and ratioless SRAM (RL-SRAM) cells. In addition to the 6T-SRAM cell, the RL-SRAM cell has INV3 and SW3. The complementary bit line pair is divided into the dedicated write bit line (WB) and dedicated read bit line (RB). Two word lines are prepared for the dedicated write word line (WWL) and dedicated read word line (RWL). The INV3 is the dedicated read buffer for driving the read bit line, while the SW3 is added to break the flip-flop loop in the write operation. We have reported the basic ratioless operation with the ratioless 10-transistor SRAM cell shown in Fig. 4(a), in which the input switch and output tristate inverter were configured with single channels.[24-25] However, for the low-supply-voltage operation, it was suggested that the full-complementary configuration of the 12-transistor ratioless cell, as shown in Fig. 4(b), would be suitable because it has rail-to-rail read and write capabilities, and achieves a fully static operation.

The circuit operations of the ratioless SRAM cell during the hold, read, and write states are summarized in Fig. 5. In the hold state [Fig. 5(a)], the data is held by the closed cell local loop (CLL), which consists of two inverters (INV1 and INV2) and a closed SW3. In the read operation [Fig. 5(b)], the data is read out to a read bit line (RB) through the read buffer that consists of the INV3 and a closed SW2 between the CLL and the read bit line (RB). Also, the stored data is never destroyed because the CLL is isolated from the RB by the read buffer (INV3). In the write operation [Fig. 5(c)], the CLL is broken by the open SW3 while the write word line is asserted. Thus, ratioless margin-free hold, read, and write operations can be performed because these operations are independent of the transistor size and impedance of the bit line.

There are write-selected and write-half-selected cells, as shown in Fig. 6(a). In write-selected cells, cell data would successfully be updated by the upcoming write data. On the other hand, in the write-half-selected cells, the stored data are lost because the CLL no longer exists. In order to overcome the data corruption problem in write-half-selected cells, we proposed the static column retention loop (SCRL) to hold the data on behalf of the broken CLL.[12] Figure 6(b) shows the SCRL structure, which simply has the loop-back switch (LBS) to forward the read-out signal from the RB to the WB. When the write word line is asserted, the memory retention loops in the write-half-selected columns are switched from the CLL to the SCRL. Since a SCRL is composed of four (even) stages of inverters

(INV2, INV3, DSA, and WD), the data of the half-selected cells are statically retained.

4. Test chip design and measurement results

In order to demonstrate the ratioless operation of the proposed technique by measurement, we designed 1Kbit SRAM TEGs in which both the 6T-SRAM and RL-12T-SRAM cells are incorporated by using a 180 nm CMOS process. The layouts of the developed chips are shown in Figs. 7(a) and 7(b), respectively. The total layout area for the RL-12T-SRAM is almost one and a half times that for the 6T-SRAM.

Figure 8 shows the measured minimum operating supply voltage versus operating frequency obtained from the test with the marching patterns. For the 6T-SRAM, the minimum supply voltage is almost constant at 0.5 V for the cycle time of 10 μs or more. On the other hand, the minimum supply voltage for the RL-12T-SRAM shows a scalability with the cycle time, and it reaches 0.22 V with a longer cycle time.

Figures 9(a) and 9(b) show the measured fail bit counts for the low supply voltage at the low-frequency operation for the 6T-SRAM and RL-12T-SRAM, respectively. As can be seen in these figures, the distribution of the supply voltage for the 6T-SRAM between the first failure bit and the last failure bit is wider than that for the RL-12T-SRAM, especially in the low-frequency operation. Figures 10 and 11 show the measured fail-bit maps (FBMs) obtained from the measurements of the 6T-SRAM and RL-12T-SRAM with the low cycle time of 1 ms, respectively. The failure bits in the 6T-SRAM start to occur randomly at the supply voltage of 0.49 V, while most of the memory cells are changed to fail in a supply voltage range from 0.3 to 0.22 V. These results indicate that a 6T-SRAM cell operation becomes more sensitive for the device variability in the low supply voltage region such as 0.5 V or less. On the other hand, in the RL-12T-SRAM, the failure bits occur nearly simultaneously even at low supply voltages. All of the memory cells of the RL-12T-SRAM are changed to fail in a narrow supply voltage range from 0.17 to 0.21 V. This is because the basic operation of the RL-12T-SRAM is fully digital and complementary. As a result, the RL-12T-SRAM has strong immunity to the variabilities of device characteristics.

5. Comparison with the simulated result

Figures 12(a) and 12(b) show the circuit schematics for the 6T-SRAM and RL-12T-SRAM that are used for the circuit simulations of Monte Carlo analysis. Each MOS transistor in the memory cell has a voltage source at the gate terminal to shift its threshold voltage (Vth). Figures 13(a) and 13(b) show the simulated results from the Monte Carlo analysis for the 6T-SRAM and RL-12T-SRAM, respectively. As a result, if the Vth shift voltage is 20 mV for one standard deviation, the simulated results agree well with the measured results shown in Fig. 8. This estimated Vth shift voltage of 20 mV is also in agreement with that of 22 mV with the minimum channel length and width of the standard 180 nm process shown in Refs. 26 and 27. This result indicates that the minimum operating voltages for the 6T-SRAM were strongly affected by the variability of transistors, whereas the RL-12T-SRAM has a superior immunity to the device variability.

We also compared the measured results of the minimum supply voltage of the SRAMs with that of the 51-stage CMOS ring oscillator, as shown in Fig. 14. As can be seen in this figure, the RL-12T-SRAM can be operated even at subthreshold voltages and has similar scalability between the minimum supply voltage and operating frequency of the CMOS ring oscillator. This indicates that the basic operation of the RL-12T-SRAM, as well as that of CMOS logic circuits, is fully digital and complementary.

6. Conclusions

A ratioless full-complementary 12-transistor SRAM was developed and measured to evaluate its operation under an ultra low supply voltage range. The test chips that include both conventional six-transistor and ratioless 12-transistor SRAM cells were developed by a 180 nm CMOS process. As a result, we confirmed that the ratioless full-complementary 12-transistor SRAM has superior immunity to the variabilities of the device characteristics and an inherent ability of operation in the ultra low supply voltage of 0.22 V.

References

1) E. Seevinck, F. J. List, and J. Lohstroh, IEEE J. Solid-State Circuits **SC-22**, 748 (1987).

2) T. Hiramoto, M. Suzuki, X. Song, K. Shimizu,T. Saraya, A. Nishida, T. Tsunomura, S. Kamohara, K. Takeuchi, and T. Mogami, IEEE Trans. Electron Devices **58**, 2249 (2011).

3) E. Grossar, M. Stucchi, K. Maex, and W. Dehaene, IEEE J. Solid-State Circuits **41**, 2577 (2006).

4) K. Nakamura, K. Noda, and H. Koike, IEEE Int. Conf. Microelectronic Test Structures (ICMTS), 2009, p. 9.

5) H. Yamauchi, J. of Semiconductor Technology and Science **9**, 37 (2009).

6) M. Yamaoka, N. Maeda, Y. Shinozaki, Y. Shimazaki, K. Nii, S. Shimada, K. Yanagisawa, and T. Kawahara, International Solid-State Circuits Conf. Dig. Tech. Pap., 2005, p. 480.

7) D. Bol, R. Ambroise, D. Flandre, and J. D. Lagat, Faible Tension Faible Consommation, 2008, p. 117.

8) K. Matsumoto, T. Hirose, Y. Osaki, N. Kuroki, and M. Numa, IEICE Trans. electronics **E94-C**, 1042 (2011).

9) M. Yabuuchi, K. Nii, Y. Tsukamoto, S. Ohbayashi, S.Imaoka, H. Makino, Y. Yamagami, S. Ishikura, T. Terano, T. Oashi, K. Hashimoto, A. Sebe, G. Okazaki, K. Satomi, H. Akamatsu, and H. Shinohara, IEEE J. Solid-State Circuits Dig. Tech. Pap., 2007, p. 326.

10) S. Ohbayashi, M. Yabuuchi, K. Nii, Y. Tsukamoto, S. Imaoka, Y. Oda, M. Igarashi, M. Takeuchi, H. Kawashima, H. Makino, Y. Yamaguchi, K. Tsukamoto, M. Inuishi, K. Ishibashi, and H. Shinohara, Symp. VLSI Circ. Dig. Tech. Pap., 2006, p. 17.

11)H. Yamauchi, T. Iwata, H. Akamatsu, and T. Fujita, VLSI Circ. Dig. Tech. Pap., 1996, p. 126.

12) D. P. Wang, H. J. Liao, H. Yamauchi, W. Hwang, Y. L. Lin, Y. H. Chen, and H. C. Chang, IEEE System-on-Chip Conf. Dig. Tech. Pap., 2007, p. 211.

13) Y. Chung and S. W. Shim, Electronics and Telecommunications Research Institute Journal **29**, 457 (2007).

14) L. Chang, D. M. Fried, J. Hergenrother, J. W. Sleight, R. H. Dennard, R. K. Montoye, L. Sekaric, S. J. McNab, A. W. Topol, C. D. Adams, K. W. Guarini, and W. Haensch,Symp. VLSI Tech., 2005, p.128.

15) V. Naveen and A. P. Chandrakasan, IEEE J. Solid-State Circuits Dig. Tech. Pap., 2007, p. 328.

16) Y. Morita, H. Fujiwara, H. Noguchi, Y. Iguchi, K. Nii, H. Kawaguchi, and M. Yoshimoto, Symp. VLSI Circ., 2007, p. 256.

17) J. S. Wang, P. Y. Chang, and C. C. Lin, IEICE Trans. electronics **95**, 172 (2012).

18) I. J. Chang J-J. Kim, P. Park, and K. Sang Roy, International Solid-State Circuits Conf. Dig. Tech. Pap., 2008, p. 388.

19) M. H. Tu, J. Y. Lin, M. C. Tsai, C. Y. Lu, Y. J. Lin, M. H. Wang, H. S. Huang, K. D. Lee, W. C. Shih, and S. J. Jou, IEEE J. Solid-State Circuits **47**, 1469 (2012).

20) J. Singh, J. Mathew, D. K. Pradhan, and S. P. Mohanty, IEEE System-on-Chip Conf., 2008, p. 243.

21) K. Takeda, Y. Hagihara, Y. Aimoto, M. Nomura, Y. Nakazawa, T. Ishii, and H. Kobatake, IEEE J. Solid-State Circuits **41**, 113 (2006).

22) B. H. Calhoun and A. P. Chandrakasan, IEEE J. Solid-State Circuits **42**, 680 (2007).

23) A. Agarwal, S. K. Mathew, S. K. Hsu, M. A. Anders, H. Kaul, F. Sheikh, R. Ramanarayanan, S. Srinivasan, R. Krishnamurthy, and S. Borkar, International Solid-State Circuits Conf. Dig. Tech. Pap., 2010, p. 328.

24) T. Saito, H. Okamura, H. Yamamoto, and K. Nakamura, IEEE Int. Memory Workshop, 2012, p. 167.

25) H. Okamura, T. Saito, H. Goto, M. Yamamoto, and K. Nakamura, IEEE Int. Conf. Microelectronic Test Structures (ICMTS), 2013, p. 212.

26) J. Pineda-Gyvez and H. P. Tuinhout, IEEE J. Solid-State Circuits **39**, 157 (2004).

27) M. J .M. Pelgrom, H. P. Thinhout, and M. Vertregt, IEEE International Electron Devices Meeting, 1998, p. 915.

RL-12T-SRAM.

Fig. 13. Simulated results of Monte Carlo analysis: (a) 6T-SRAM and (b) RL-12T-SRAM.

Fig. 14. Comparison of the minimum operating voltages for 6T-SRAM, RL-12T-SRAM, and 51-stage CMOS ring oscillator.

Table I.   Comparison of SRAM memory cells.

Reference	Conv, [5]	[14]	[16][17]	[18]	[19]	[20]	[21]	[22]	[23]	Our Prev.[24]	*This work*
Number of TRs	6	8	8	10	9	7	7	10	10	10	*12*
Number of word and bit lines	1 + 2	1 + 3	1 + 3	2^{*1} + 2	3^{*1} + 1	2 + 1	3 + 2	2^{*3} + 3	3 + 2	3 + 2	*4 + 2*
Read margin	RSNM>0	Free	Free	Free	Free	RSNM>0	Free^{*2}	Free	Free	*Free*	*Free*
Write margin	WSNM>0	WSNM>0	WSNM>0	WSNM>0	WSNM>0	Free	Free	Maybe*3	Free	*Free*	*Free*
Write(halfselect) margin	RSNM'>0	RSNM'>0	Free	Free	Free	Free	Free	N/A	N/A	*Free*	*Free*
Flip/flop loop cutting for write	No	No	No	No	No	Yes	Yes	Maybe*3	Yes	Yes	Yes
Rail-to-rail write ability	No	No	No	No	No	No	No	Maybe*3	Yes	No	Yes
Rail-to-rail & static read ability	No	No	No	No	No	No	No	No	No	No	Yes
Write-half-select protection	Vword / Vcell		W.after.R	XY-Select	XY-Select		W.after.R	N/A	N/A	SCRL^{*4}	*SCRL^{*4}*

*1: Cross point (XY) select word lines,   *2: Free in dynamic read operation ,   *3 Vcell collaping for write,   *4 Static column retention loop

11
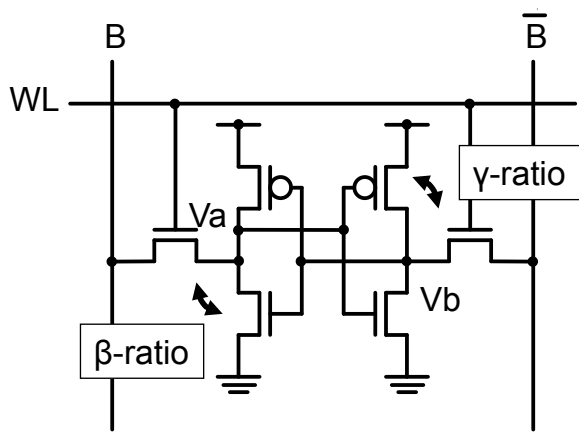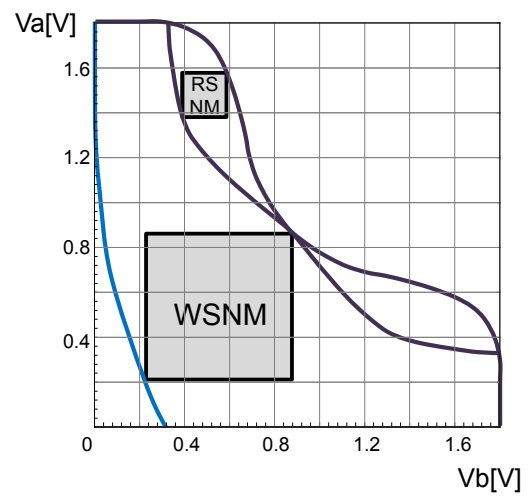
Fig. 1. Conventional six-transistor SRAM cell
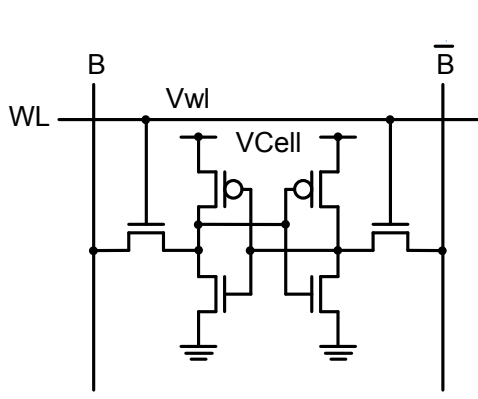
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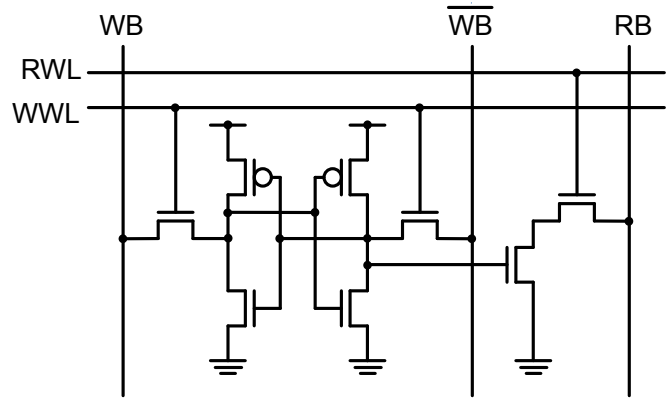
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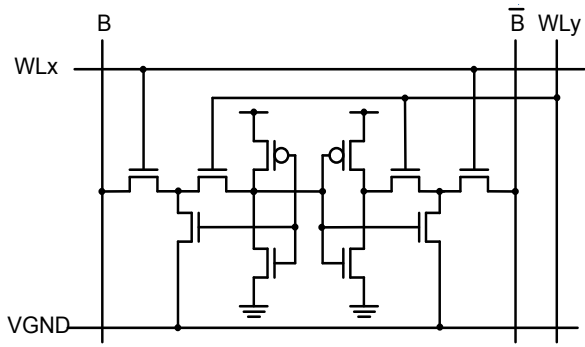
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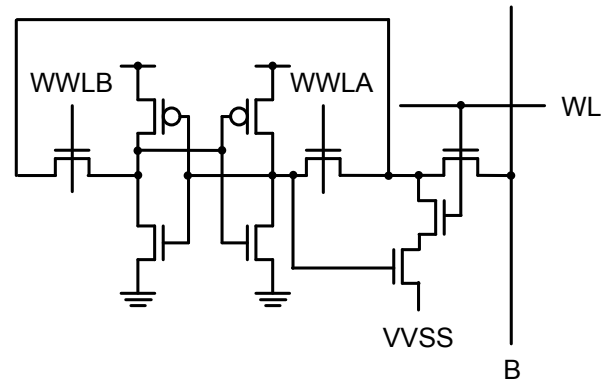
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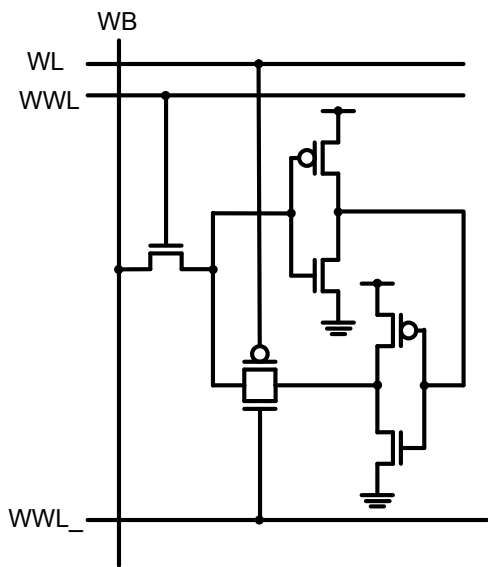
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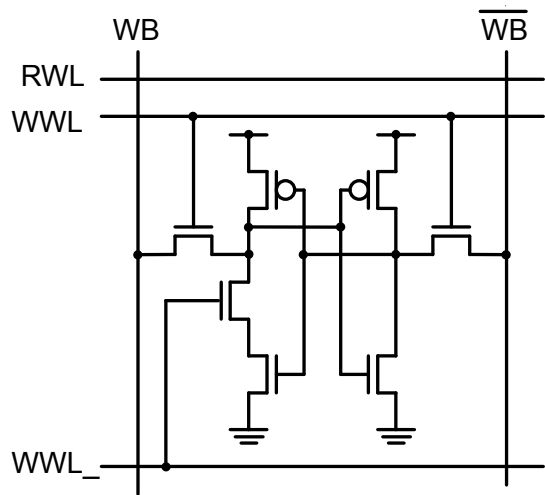
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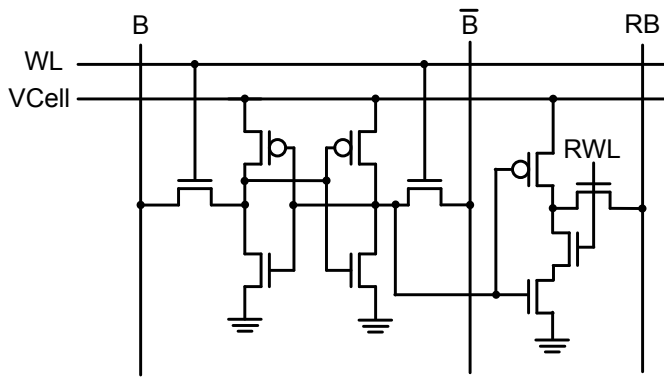
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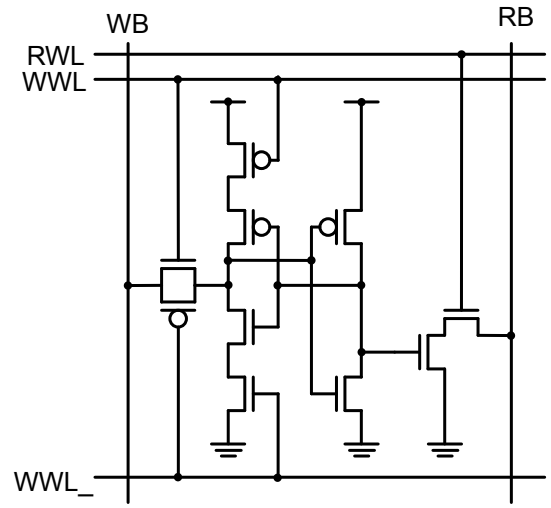
(h)

Fig. 2. Memory cells for SRAM

(a)

(b)
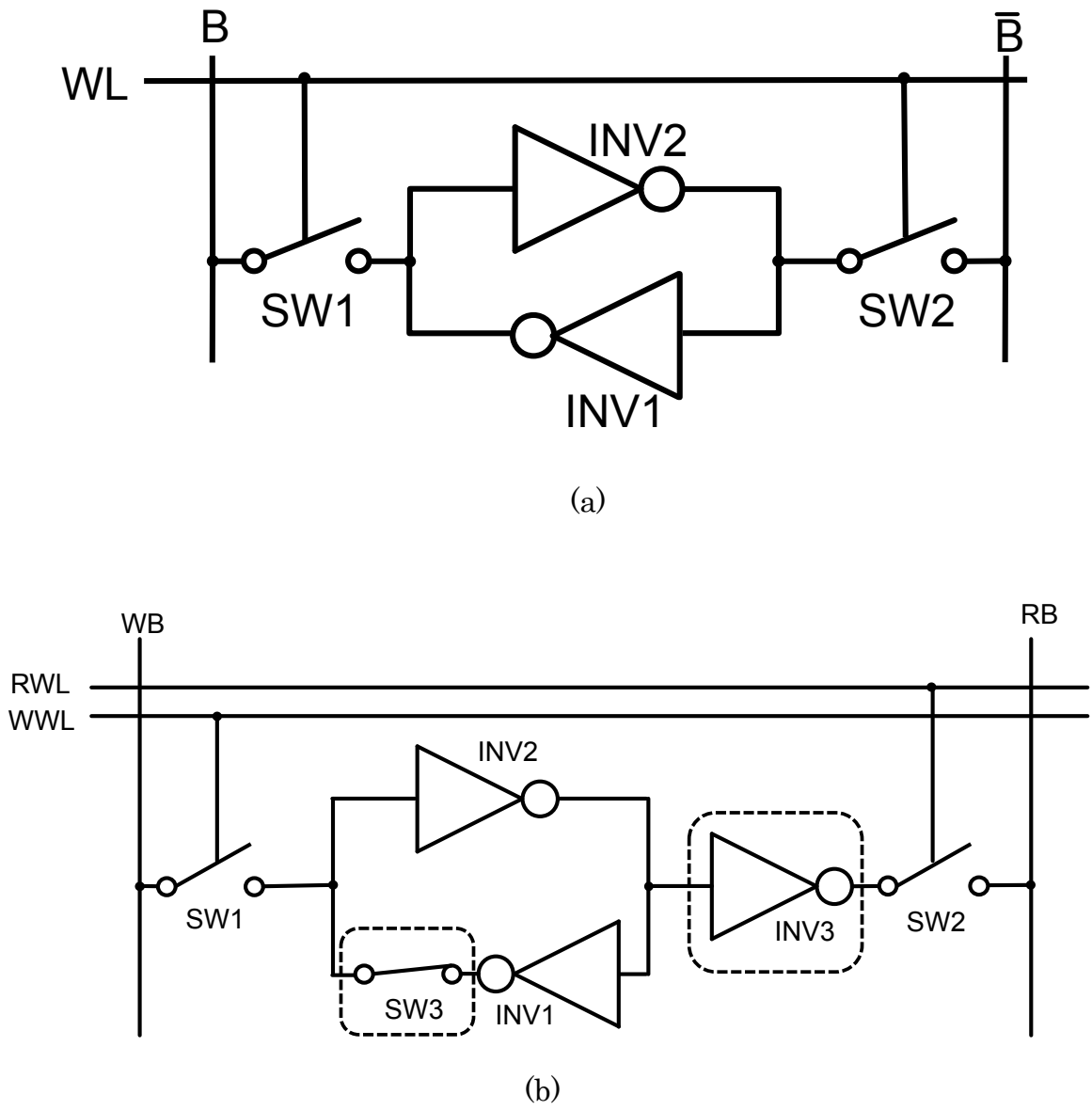
Fig. 3. Logic-level schematics of SRAM cells
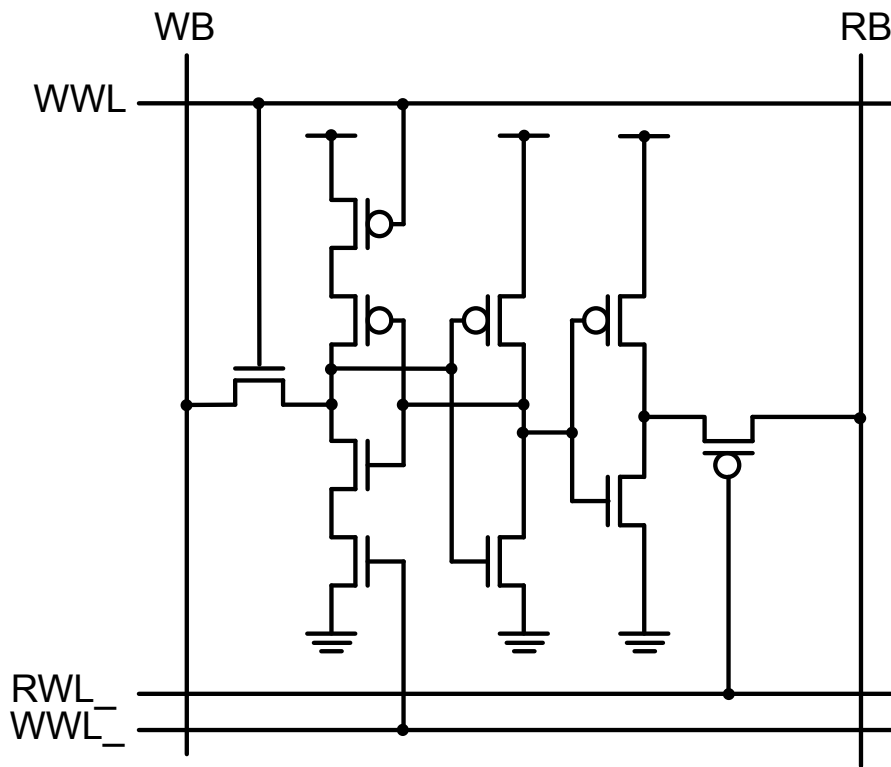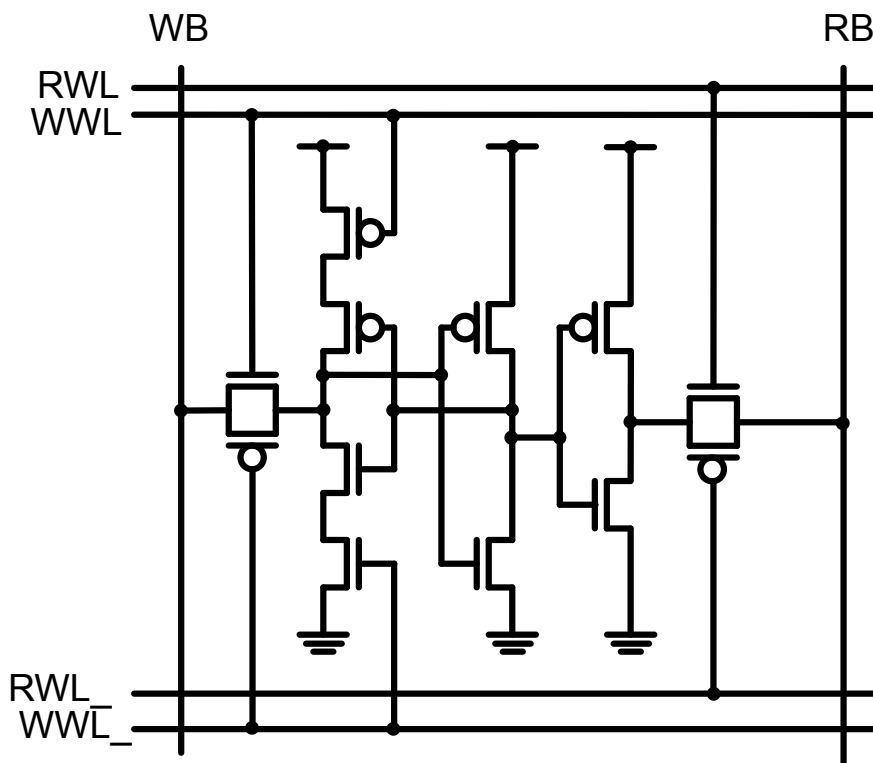
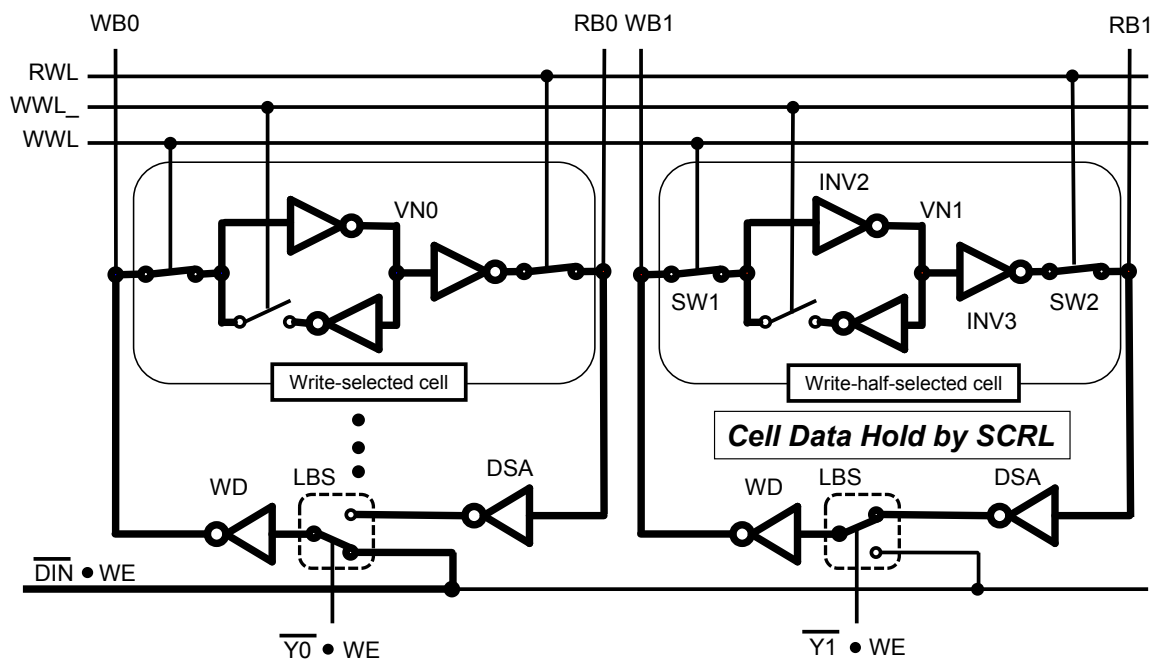Fig. 4. Ratioless SRAM cells

16
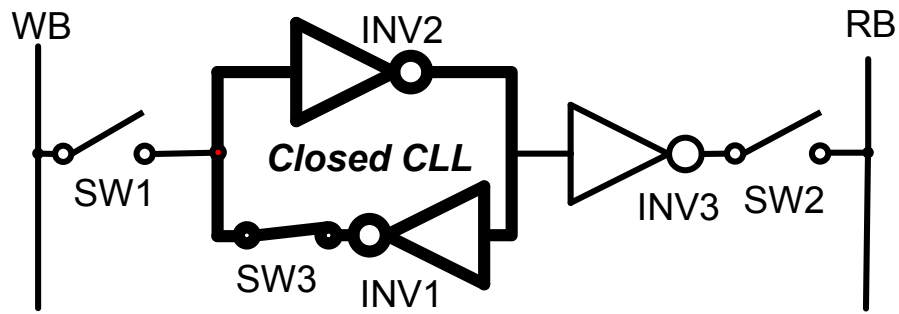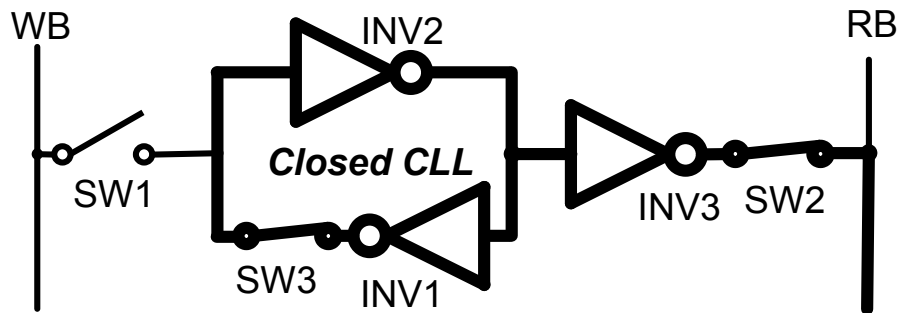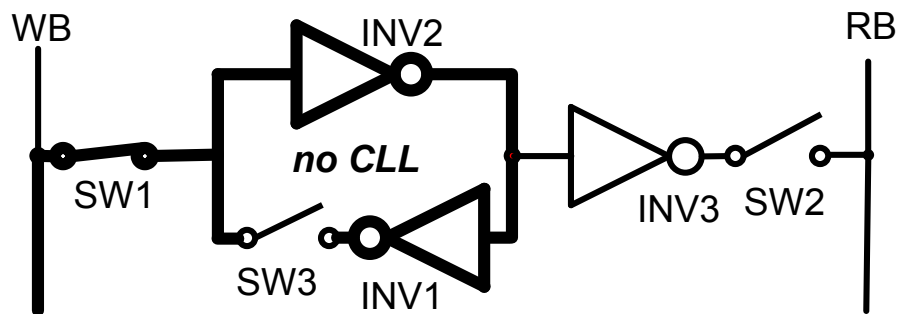
Fig. 5. Operations of ratioless SRAM cell
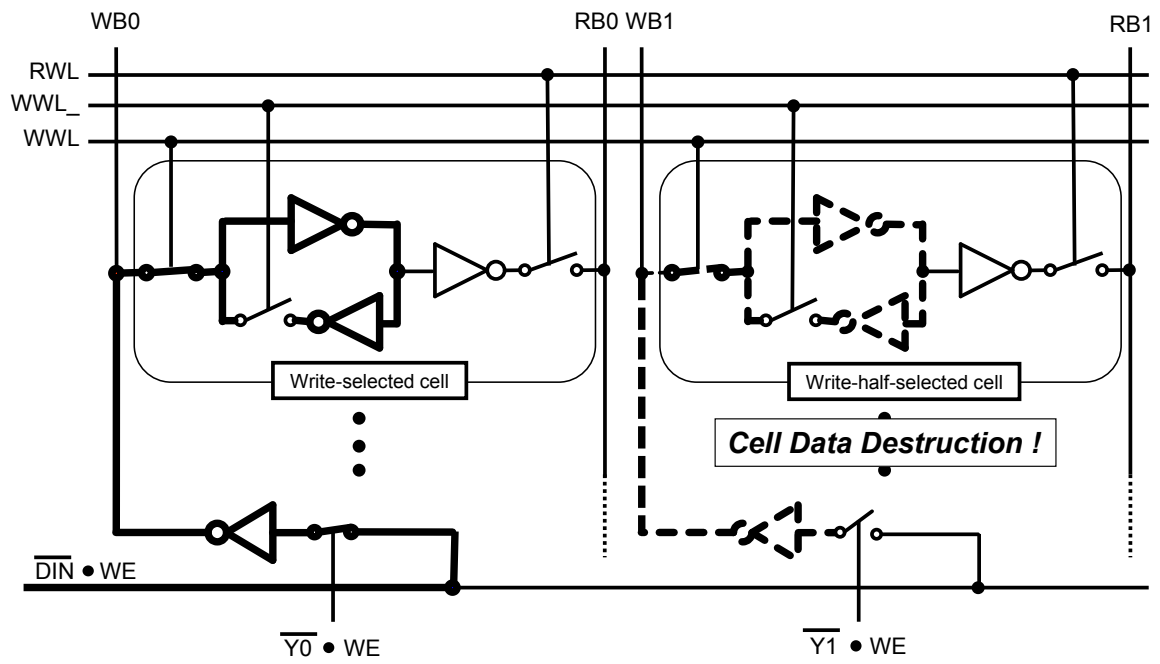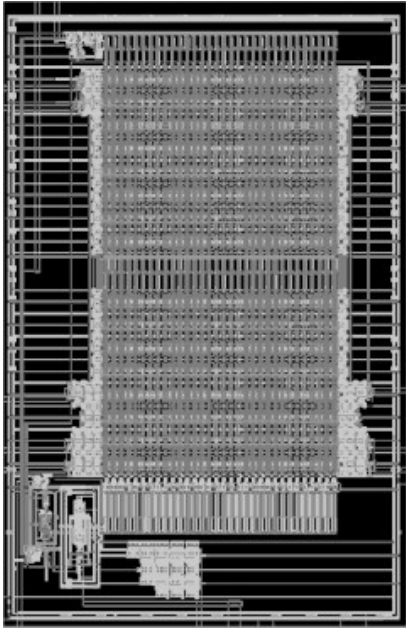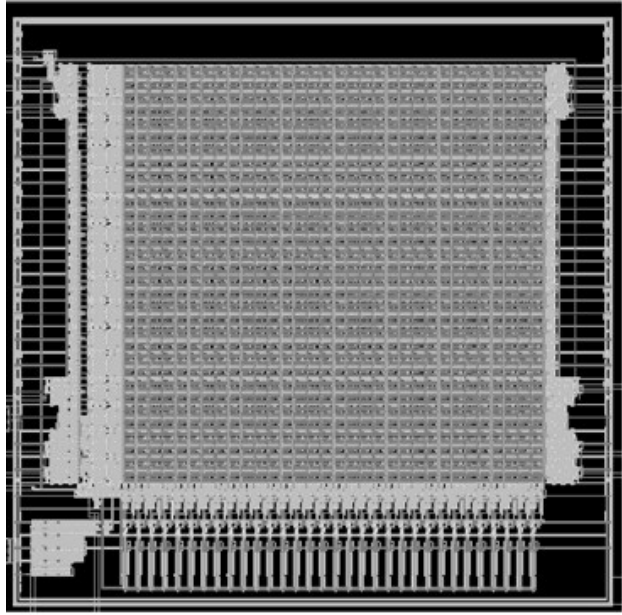
(a)

(b)

Fig. 6. Static column retention loop (SCRL) structure

350 x 230 µm²   350 x 350 µm²

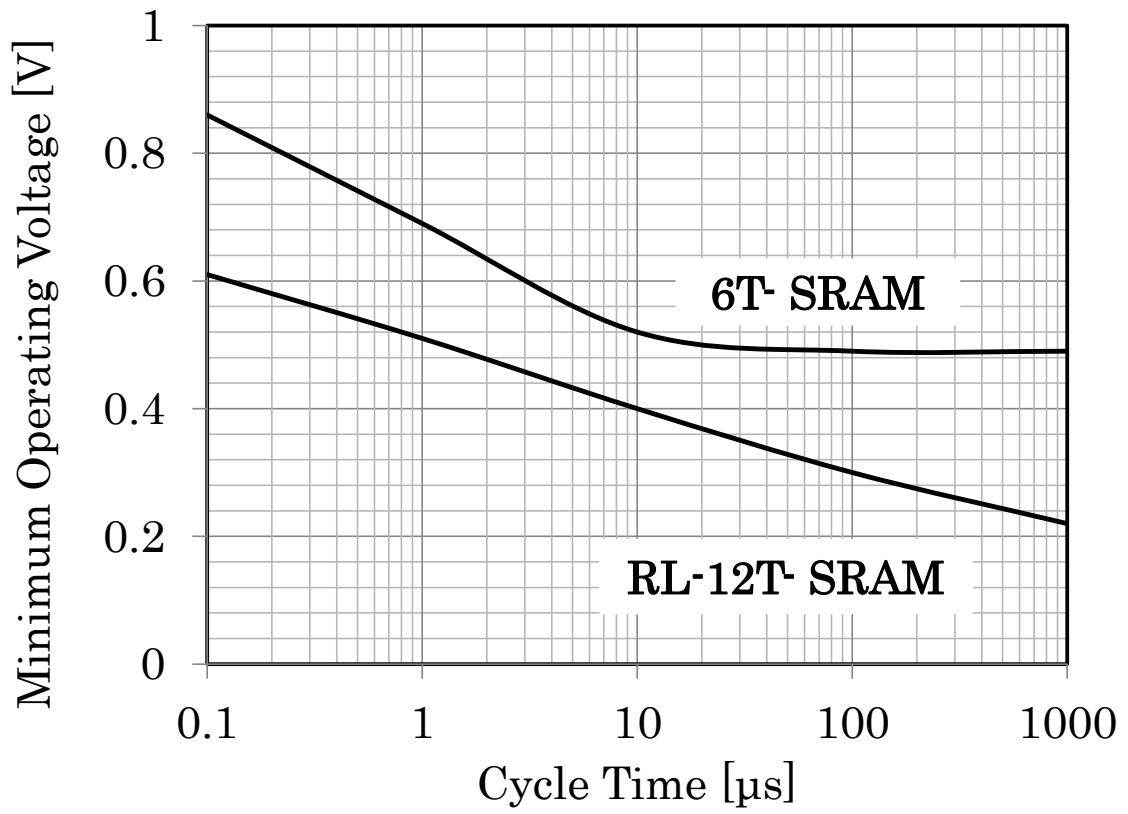(a)   (b)

Fig. 7. Chip layout

Fig. 8. Measured minimum operating voltage versus cycle time
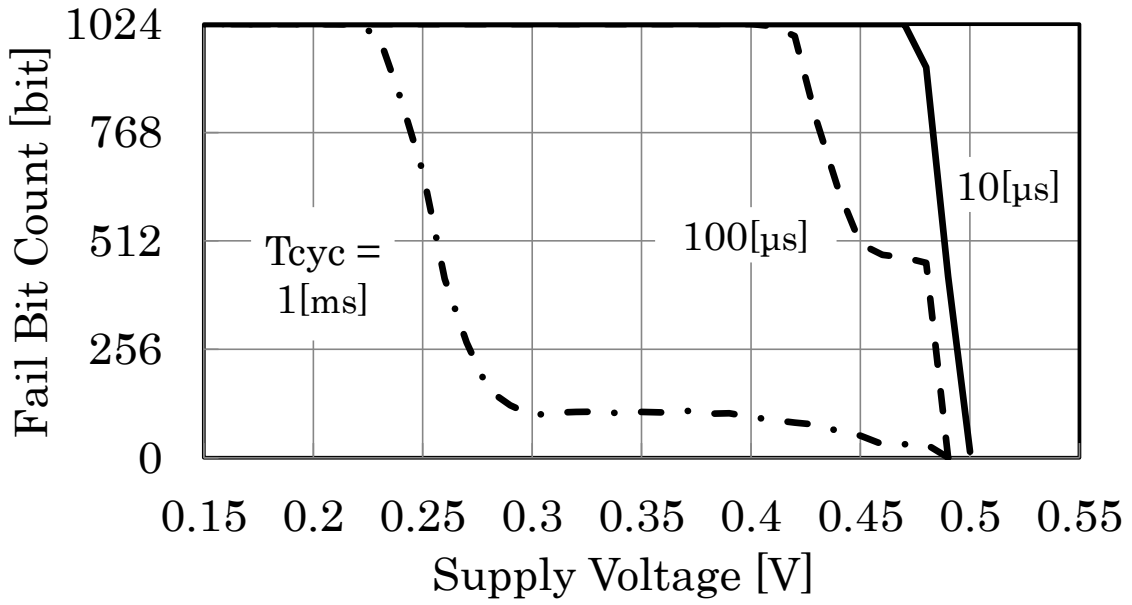
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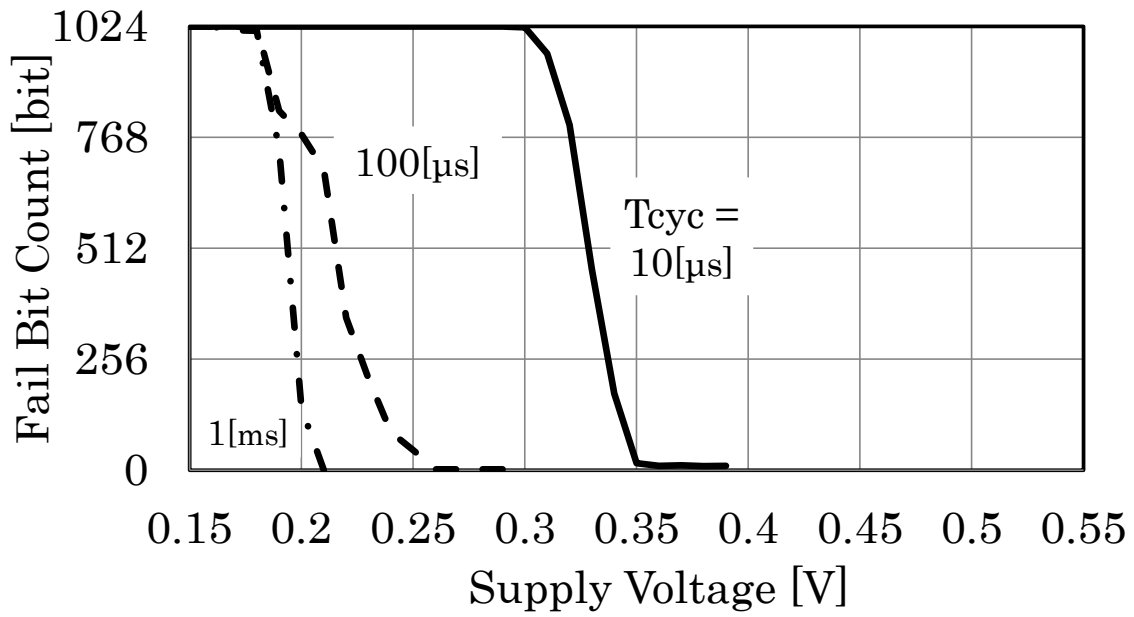
(b)

Fig. 9. Measured fail bit count versus supply voltage
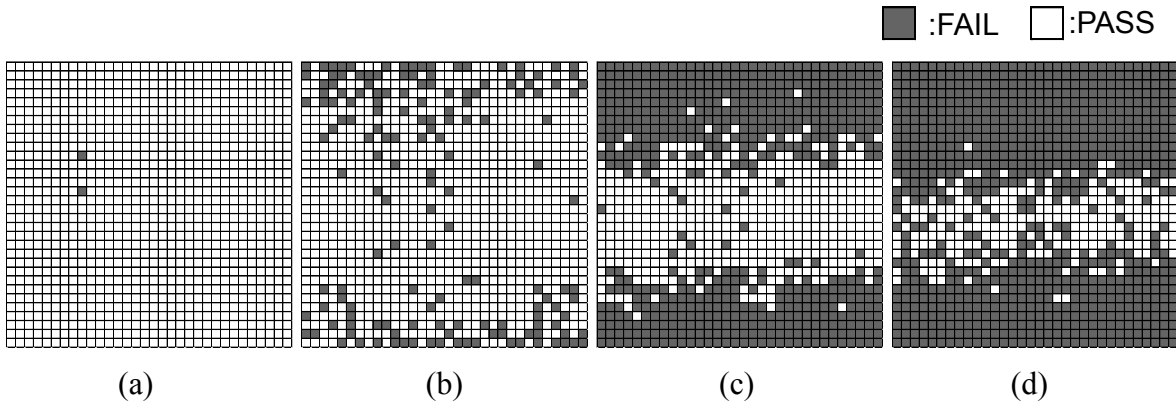
Fig.10. Measured fail bit map for 6T-SRAM
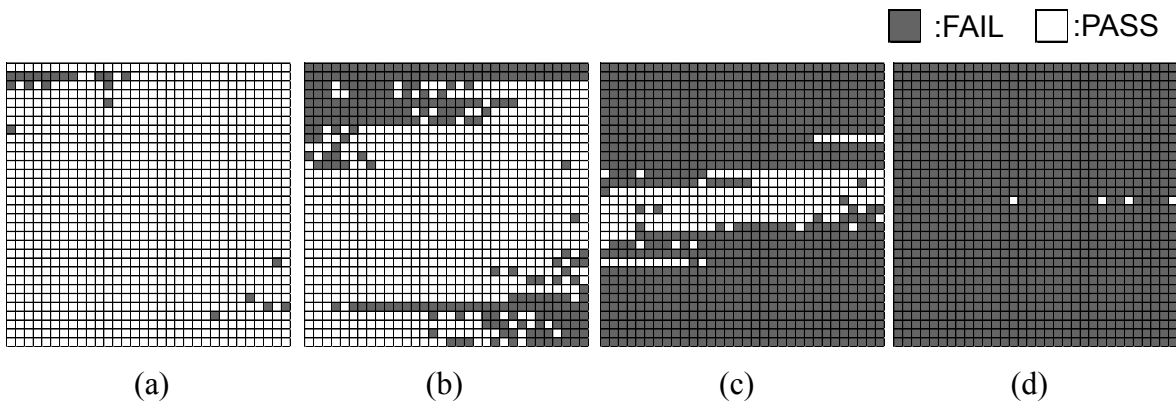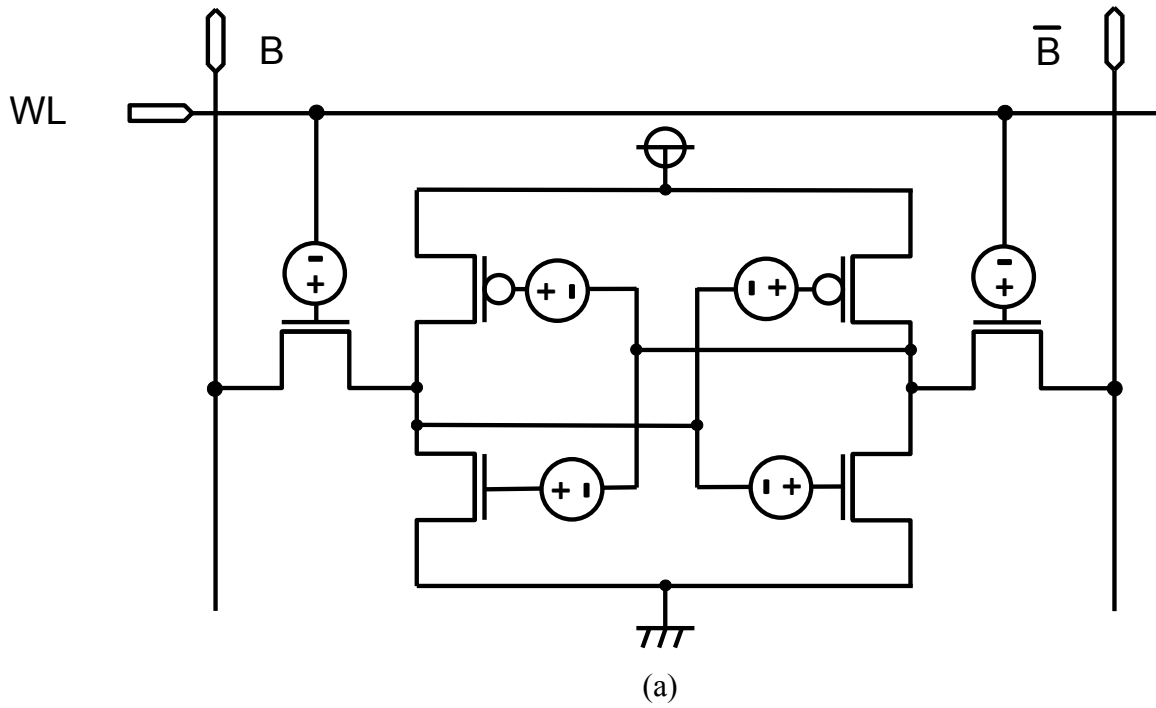
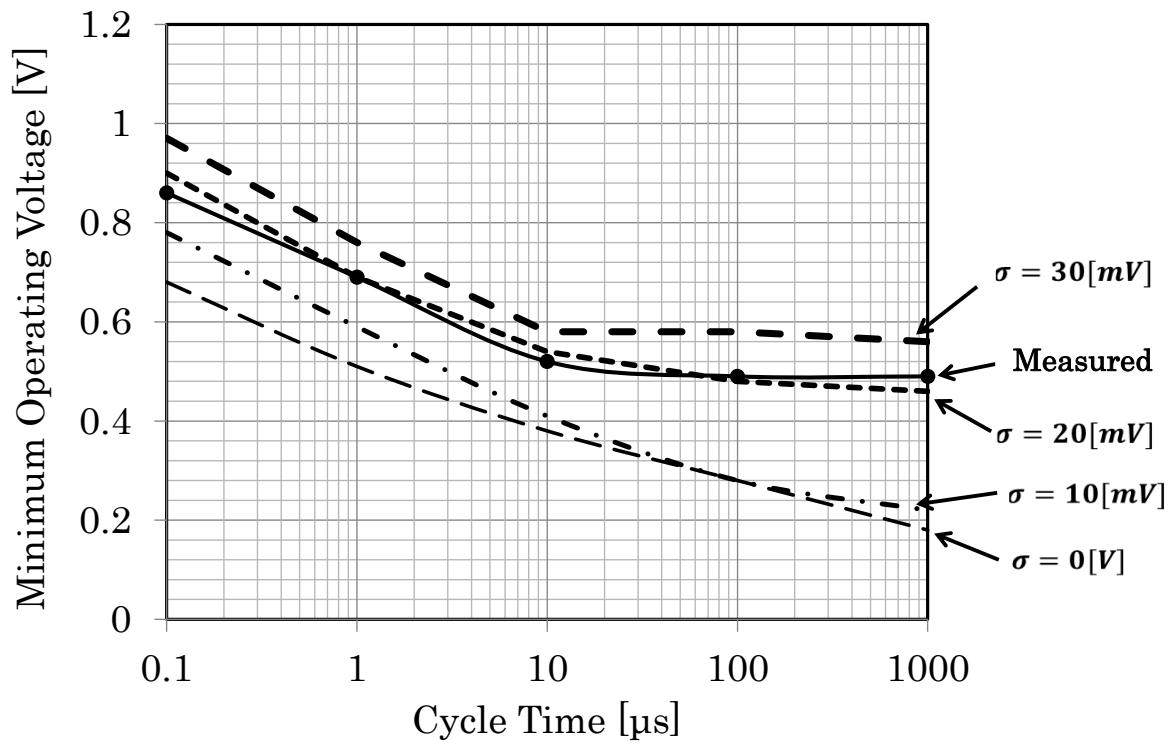Fig. 11. Measured fail bit map for 12T-SRAM
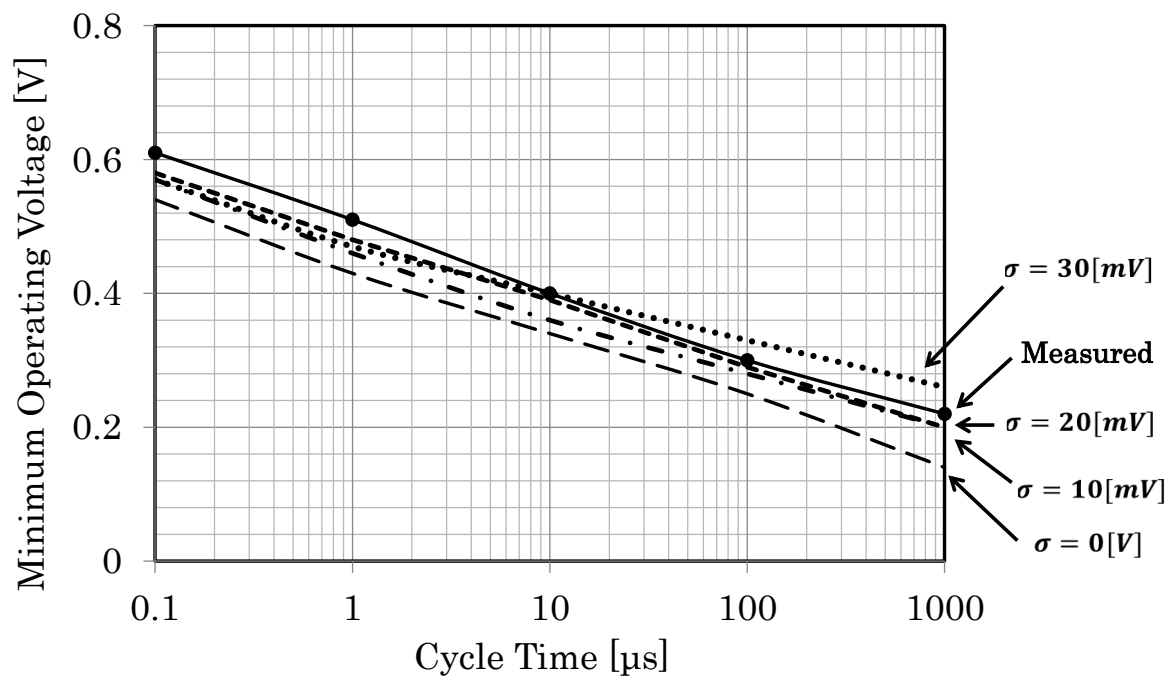
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(b)
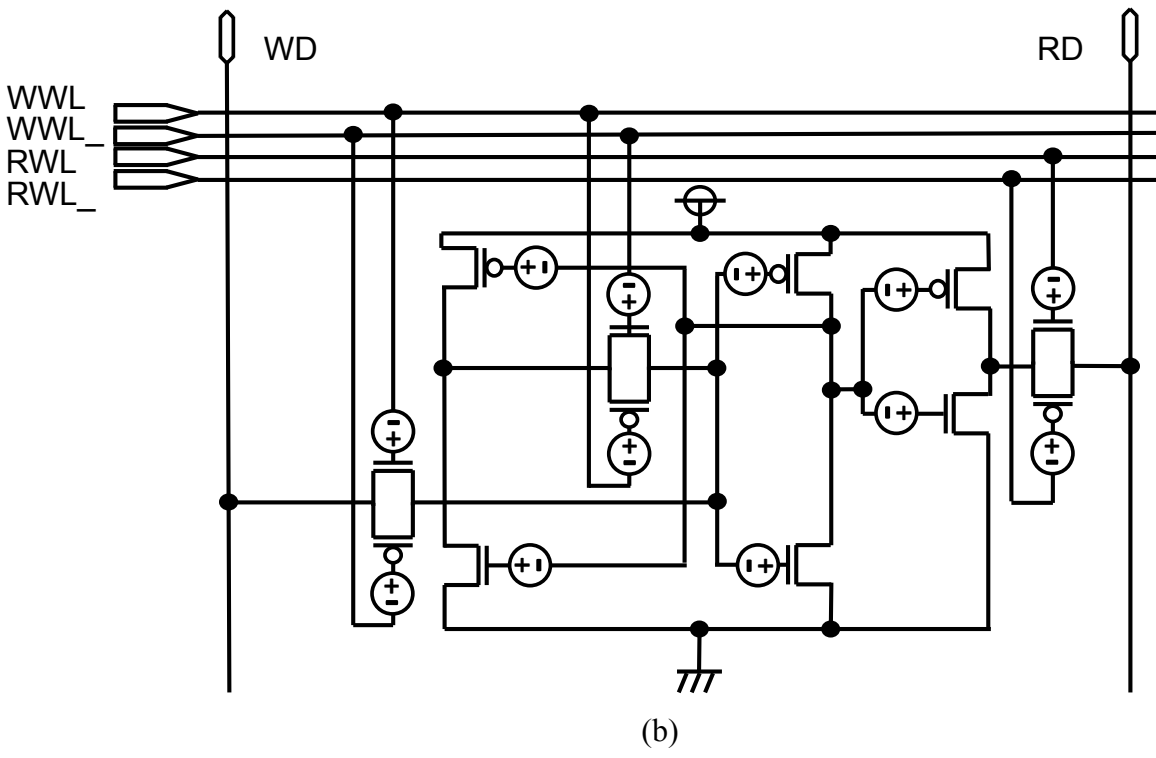
Fig. 12. Vth shift configuration for Monte Carlo analysis

(a)

(b)
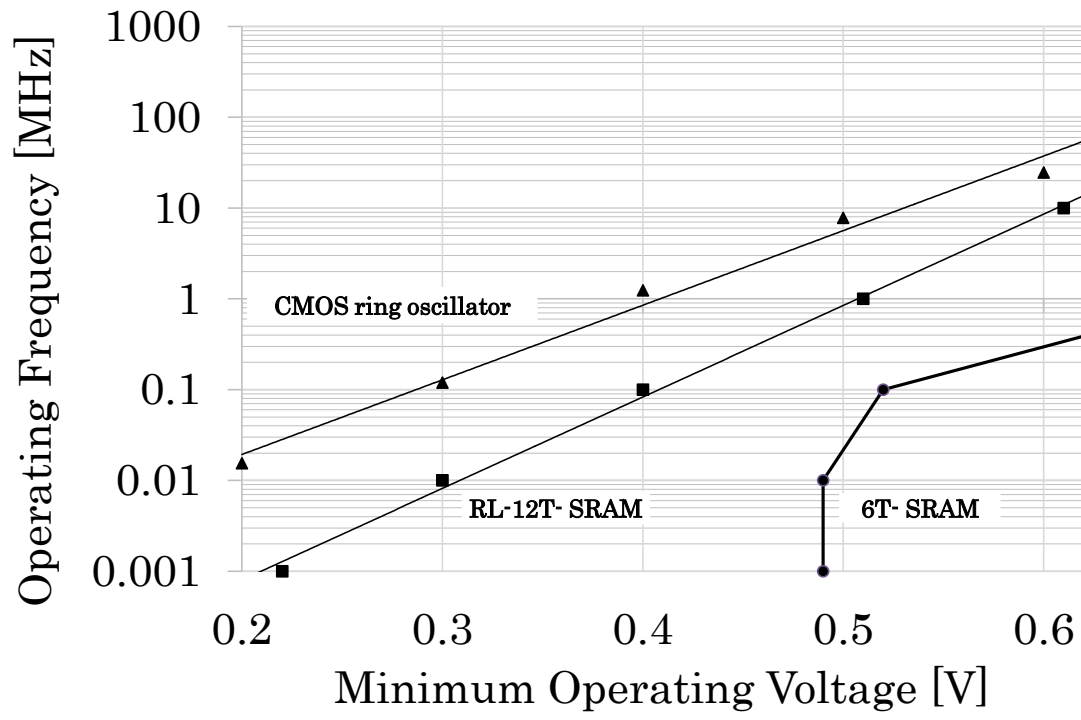
Fig. 13. Simulated results of Monte Carlo analysis

Fig. 14. Comparison of the minimum operating voltages for 6T-SRAM, RL-12T-SRAM and 51-stage CMOS ring oscillator