A Stabilization Technique for Intermediate Power Level in Stacked-Vdd ICs using Parallel I/O Signal Coding

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1. Introduction

The optimal supply voltages for high-performance LSIs should be locally generated by the step-down regulator from the power voltage on the print circuit board. In recent LSIs with the down-scaled CMOS device, the supply voltage should be lowered to satisfy the device reliability. Therefore the quantity of the step-down voltage generated by the regulator tends to increase. As a result, it causes the wasteful power consumption and its heat production has an adverse effect to the neighboring LSIs.

To overcome this problem, we are researching the stacked-Vdd circuit configuration by connecting the two (or more) circuit blocks in a stacked structure between the power source and ground [1][2]. However with this structure, if there is a difference of the current consumption between the upper and lower circuit blocks, the fluctuation of the Intermediate Power Level (IPL) will increase and a supporting regulator is needed to suppress the fluctuation. In this paper, we propose to eliminate the supporting regulator by stabilizing the fluctuation of the IPL by using the coding method.

2. Stacked-Vdd Structure without Regulator

The conventional circuit configuration using a step-down regulator and the power stacked circuit configuration with the supporting regulator are shown in Fig.1 (a) and (b), respectively. Even though the current flow in supporting regulator in Fig1 (b) is much smaller than the step-down regulator in Fig.1 (a), the waste of power still exists. In order to completely remove the supporting regulator, the power consumption of each upper and lower circuit block needs to be made equal.

In CMOS circuits, the consumption current will depend mainly on the operating current of the internal circuit and the switching current of the I/O buffer circuit. So the internal circuit we chose is SRAMs which always consume constant internal current. Fig.5 (a) shows the measured result of the IPL when a variety of data are read from the upper and lower SRAMs. In the worst case, the intermediate level is far different from the half of the Vdd. This is because, depending on the data pattern there is a large difference in the number of switching of the output buffers in the lower and upper circuit blocks and it occurs the large difference in the consumption current. For example when the output of the upper circuit block frequently switches and the output of the lower circuit stay constant then the IPL would continue to decrease.

3. Current Balance by I/O Coding

In this research, we examined the coding method, to achieve the uniformity of the consumption current and to completely remove the supporting regulatior by controlling the number of switching in I/O buffer as shown in Fig 1.(c). We first focused on two coding methods: (a) Bus-invert coding and (b) 8B/10B coding [3][4]. The Bus-invert coding can halve the number of switching in parallel bus by adding 1 redundant bit. It contributes 50% reduction of the simultaneous switching noise of CMOS I/O. On the other hand, 8B/10B coding is a DC-balanced coding in which almost a 50% existence probability of “1”s is guaranteed by converting an 8-bit code to a corresponding 10-bit code. 8B/10B coding is commonly used in optical and high-speed serial interfaces.

4. 8B/10B Coding with Toggle Converter

Here we need to control the number of switching instead of number of “1”s in 8B/10B coding because noise is generated when the circuit changes its states. Therefore we also employ “1” to toggle conversion circuit with the 8B/10B coding circuit as shown as Fig.2. The 8-bit output from the SRAM is converted to the 10-bit DC-balanced code by the 8B/10B encoder. Then the “1”s in the 10-bit code are converted to switching by the toggle-flip/flop (T-F/F). At the receiver, toggles are converted “1”s, then 10B/8B decoding is performed. In the generated 10-bit code, the number of switching is always guaranteed to 5-bit. Therefore the numbers of switching in the upper and lower I/O buffers are balanced, so the fluctuation of the IPL is will suppressed as shown in Fig.3.

5. Chip Design and Measurements

To verify the effectiveness of proposed methods by the measurement, we have developed a test chip with 0.18um CMOS process. The photo of the chip is shown in Fig.4. In this photo, (a) is the SRAM macro, (b) is the Bus-Invert Coding, (c) is the 8B/10B coding circuit and (d) is the toggle conversion circuit, respectively. SRAM can store any data. In addition, SRAM can optionally be followed by the two coding circuits and toggle conversion circuit. Two test chips are used to construct stacked-Vdd structure. The measurement results of the fluctuation of the IPL are shown in Figures 5(a)-(d). When applying Bus–Invert Coding (Fig.5 (b)) or just 8B/10B Coding (Fig.5 (c)), the fluctuations were not suppressed. However as shown in Fig.5 (d), with the proposed 8B/10B Coding followed by toggle conversion circuit, the stability of the IPL was confirmed to be much better than other ways for any bit pattern excluding the noise caused by measurement environment. The transistor counts and power consumption

ratios for 8-bit I/O buffers for circuit blocks shown in Fig.4 are summarized in Table I.

6. Conclusion

We have proposed a method to achieve Stacked-Vdd structure without the supporting regulators. It minimizes the difference of the number of switching in upper and lower CMOS I/Os by using 8B/10B coding followed by toggle converter. The noise reduction effect was experimentally demonstrated with two test chips.

Acknowledgments

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References

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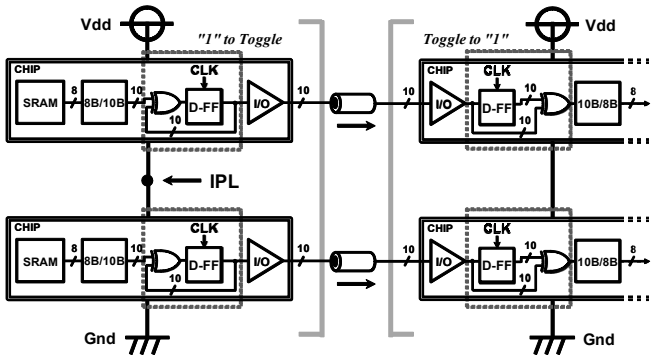


Fig.2 8B/10B Coding with Toggle Converter

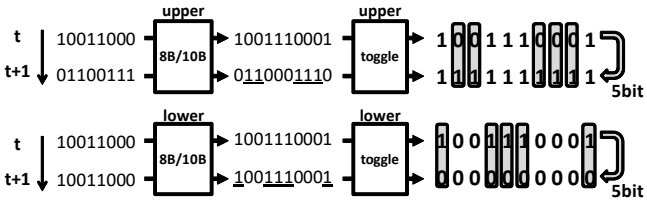
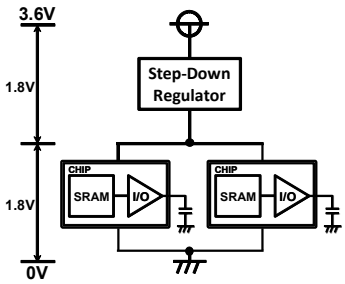
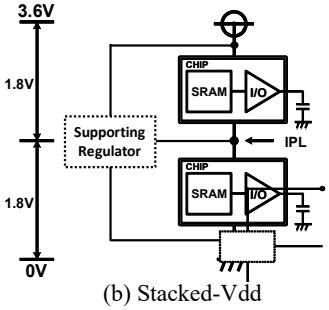


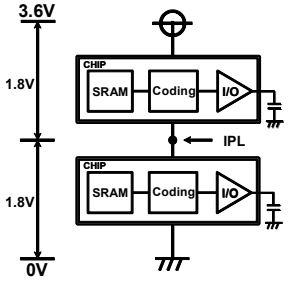
Fig.3 Coding Examples of Proposed Scheme



(a) Conventional



(b) Stacked-Vdd



(c) Stacked-Vdd with I/O Coding

Fig.1 Circuit Configuration

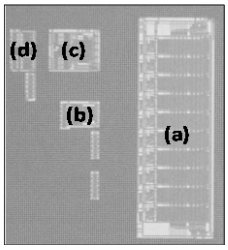
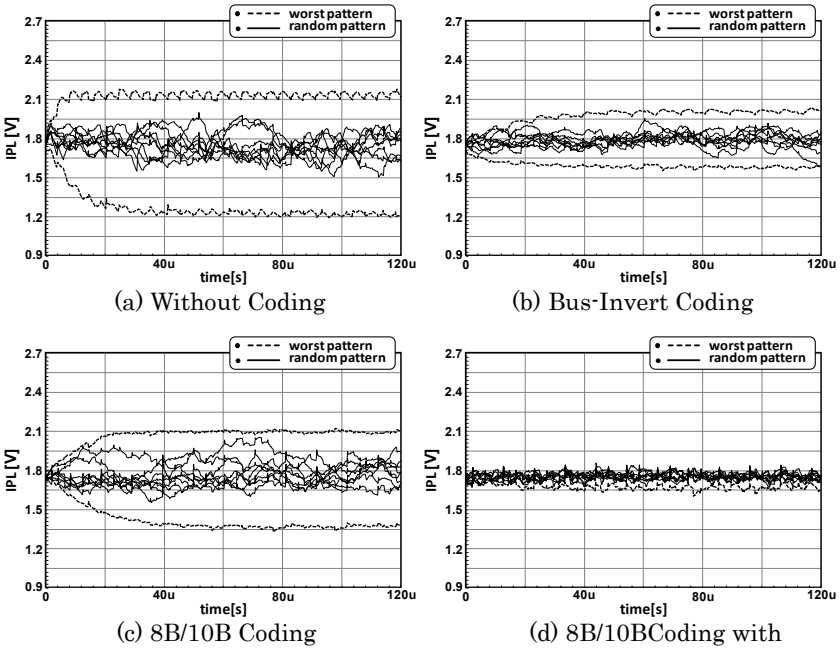


Fig.4 Photo of Test Chip

Table I Area and Power Overheads

Circuit	Transistor Counts	Power Consumption Ratio [%] *
(b)	638	1.17
(c)	1164	1.97
(c)+(d)	1484	2.52

* for 8-bit I/O buffers with 30pF load.



(a) Without Coding (b) Bus-Invert Coding

(c) 8B/10B Coding (d) 8B/10BCoding with Toggle Conversion

Fig.5 Measured Results