# A Memory-Based Programmable Logic Device Using a Look-Up Table Cascade with Synchronous SRAMs

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## 1. Introduction

An LUT (Look-Up Table) cascade has been proposed to achieve a novel programmable logic device[1][2]. It is composed of a serial connection of large-scale memories. It requires memory size that is only 1/100 to 1/1000 of the straightforward RAM realization. Since LUT cascades are realizable by using the memory technology, the design, test and production costs of LUT cascades should be quite low. We have developed the first implementation of the LUT cascade[3]. It was a straightforward implementation of LUT cascade connection with asynchronous SRAM cores. Unfortunately, its performance was not acceptable especially for power dissipation.

In order to improve the performance, we developed a second version. To achieve competitive performance (Area, Speed, Power and Cost) to FPGAs, we developed several circuit techniques: 1) flexible cascade connection to increase the memory efficiency and free I/O pin assignment, 2) 8/9 multi-phase pseudo-asynchronous operations with synchronous SRAM cores to achieve high-speed and low-power operations and 3) LUT-bypass redundancy to improve the chip yield.

## 2. Design of LUT Cascade LSI

Figure 1 shows the block diagram of our implementation. It consists of eight LUT blocks. Figure 2 shows the detail of a single LUT block. In Fig.2, each LUT block consists of a 64kbit synchronous SRAM core with 13b address inputs and 8b data I/O, and a few additional circuits: two 8b switches (SW1, SW2), 8b data register, the mode register and an 8b rail switch. The 8b rails switch selects either the signals from the previous LUT block or external inputs (EXT_IN). An LUT cascade can be implemented by a simple series connection of the LUT blocks. In order to increase memory efficiency and free I/O pin assignment, we developed a flexible cascade connection structure. In Fig.2, the switch (SW1) selects one of two inputs (IN1,IN2) to the cascade. This is connected to two adjacent LUT blocks, horizontally and vertically. As a result, the eight LUTs form a single loop, dual 4-LUT loops, or quadruple 2-LUT loops (See Fig.3). With each loop structure, any LUT can be the first stage of the cascade, and this increases I/O pin assignment flexibility. In addition, we made a bypass switch (SW2 in Fig.2) for redundancy from the cascade input to the output data registers. This just makes the input data skip to the next LUT block without accessing the memory array. Therefore, a faulty block can be bypassed to improve the chip yield. The bypassed SRAM core can be turned off by a pMOS power switch.

## 3. Pseudo-asynchronous Interleaved Operation

Since the memory in an LUT cascade operates as a data-path, consecutive asynchronous memory access operation is required. Employing asynchronous SRAM for an LUT block is straightforward[3]. However, it causes DC current flow in the memory cell and sense amplifier. In the LUT cascade operation, all memory blocks should operate simultaneously, so the total power dissipation in an LUT cascade LSI with asynchronous SRAMs will be too large. In order to solve the power and consecutive access problems, we developed a pseudo-asynchronous interleaved operation with synchronous SRAMs using a multi-phase clock. Figure 4 shows the developed 8/9 multi-phase clock generator. First, the PLL generates a clock that is 9 times (9x) the frequency of the original clock. Then 9-phase non-overlap clock signals (p0-p8) are generated from the complement of the 9x clock and IO_CLK. Here, 8 signals (p0-p7) are selected for control clock signals for LUT blocks. Synchronous SRAM in each LUT block is operated in the “high” period of the LUT clock. The output data of the LUT block are latched into registers at the falling edge of each LUT clock (See Fig.2). This 8 / 9 phase operation makes the data setup and hold timing margins (tm1,tm2) 1/18 of the I/O clock cycle time among the I/O registers and the first LUT block and the last LUT block as shown in Fig.4. Figure 5(a) shows the simulated internal delay time distribution in the critical path. The latency of an internal LUT is 3.3ns. Figure 5(b) shows the pseudo asynchronous operation in three operation modes. In the dual 4-LUT cascade mode, 4 operations in 5 phases are performed. The operating frequency of 33MHz in the single 8-LUT cascade mode with 122mW is experimentally confirmed. Note that a design with asynchronous SRAMs dissipates about 10 times more power than this design[3].

## 4. Measurement Result

Figure 6 shows a photomicrograph of the LUT cascade LSI developed by 0.35um standard CMOS logic process. The memory cell size is 5.2um x 7.5um (6Tr SRAM). This chip includes 512K-bit cells and a PLL control clock generator. The chip size is 9.8mm x 9.8mm and its core size is 5.1mm x 7.1mm. The ratio of the memory cell area to the core area (memory cell efficiency) is 52%. It almost looks like a conventional large-scale memory. In an LUT block, 99.5% of the area is devoted to the SRAM circuit, while only 0.5% is devoted to switches and registers.

## 5. Conclusion

The second generation of an LUT cascade LSI with a flexible cascade architecture, pseudo-asynchronous operation and LUT-bypass redundancy scheme has been developed. With the advanced high-density memory technologies, such as Gbit DRAM technologies, we can improve the area efficiency by a factor of 100 or higher. Since our architecture is very simple and logic design is straightforward, programmable logic using LUT cascade architecture implemented by advanced memory technology is quite

promising in the future sub-100nm LSI.

**Acknowledgement**

The chip has been fabricated through VLSI Design and Education Center (VDEC), the University of Tokyo in collaboration with Rohm Corporation and Toppan Printing Corporation.

**References**

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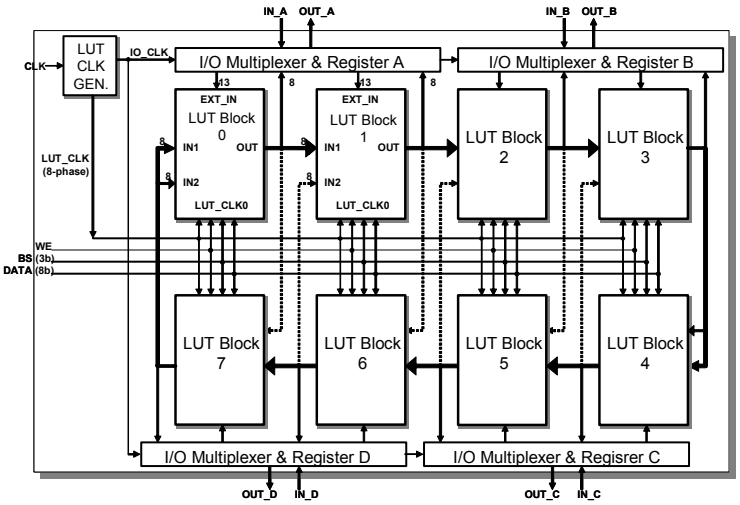



Fig.1 Block Diagram of LUT Cascade LSI

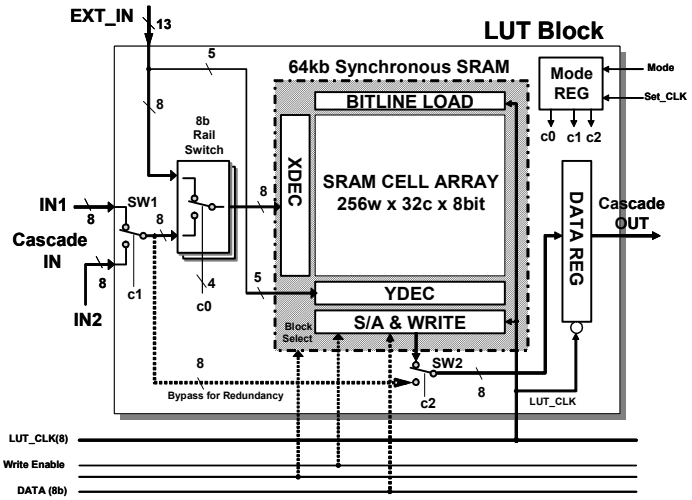



Fig.2 LUT Block

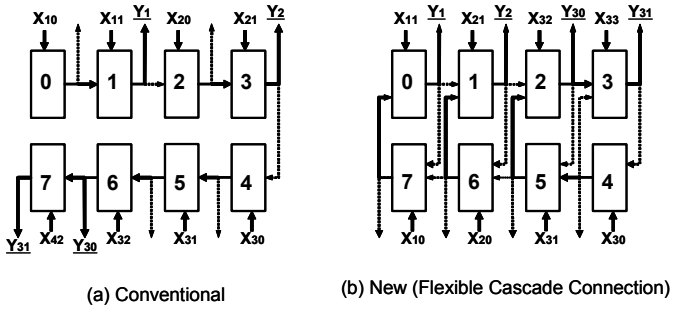



Fig.3 Mapping Examples of 4+2+2 LUT-Cascades

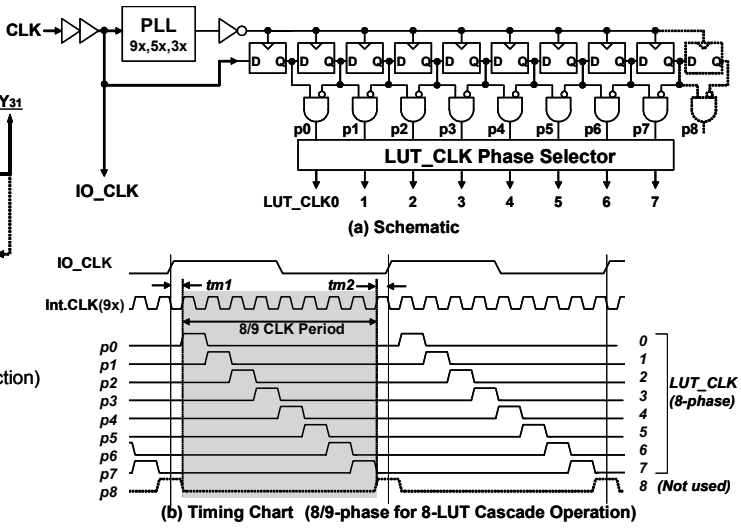



Fig.4 Multi-phase LUT-CLK Generator

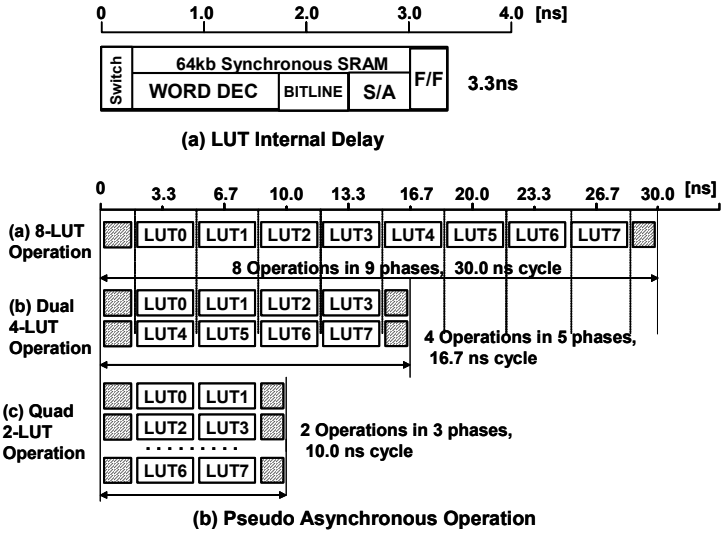
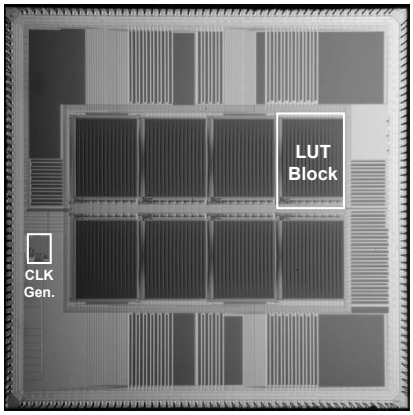



Fig.5 Internal LUT Operation




(Core Size : 5.1mm x 7.1mm, Chip Size : 9.8mm x 9.8mm, 208pins)

Fig.6 Chip Photomicrograph