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journal or publication title	2008 International Conference on Solid State Devices and Materials (SSDM2008)
year	2008-09-25
URL	http://hdl.handle.net/10228/00007555

An Optimal Design Method for Even-Stage Ring Oscillators with a CMOS Latch

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***Abstract*- This paper describes an analysis of oscillation conditions in CMOS ring oscillators composed of even-stage inverters. A design method optimizing the oscillator's operational margin based on this analysis is also described. We have found that stable oscillation margin analysis for this type of circuit is basically equivalent to the Static Noise Margin (SNM) analysis for SRAM write/read operations. Using this concept, we have established a design method that determines the optimal circuit design parameters to ensure stable oscillation.**

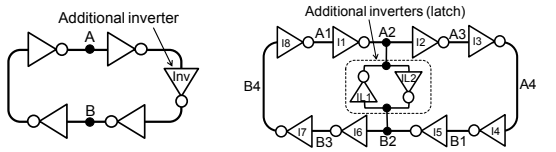
1. Introduction

Ring oscillator circuits composed of a CMOS inverter chain are widely used because of their simple structure and high-speed, low-voltage operation. Fig. 1 shows the basic circuit diagrams for two types of ring oscillators. Fig. 1(a) is a typical ring oscillator with odd-stage inverters connected in series. Continuous oscillation is obviously guaranteed by this circuit topology. Fig. 1(b) is another ring oscillator that has a delay line composed of inverters with even stages and a CMOS latch. The CMOS latch is placed to guarantee that the nodes A2 and B2 are at the opposite levels so that the oscillation behavior is appropriately achieved. This type of ring oscillator with even-stage inverters is often used in frequency synthesizers, clock data recovery, and so on. Because it has low noise characteristics and can generate even-phase clocks (e.g. 2-phase, 4-phase) [1]. This circuit, however, has an inherent problem where the node voltages may fall into DC stable levels and hence its oscillation will stop, unless the circuit dimension parameters (transistor W/Ls) are appropriately designed. A balance is required for output impedance in the latch: If the output impedance is too high, the latch function itself will be lost. On the other hand, the voltage levels at the nodes A2 and B2 will stay at the fixed values, if the output impedance is too low. Thus some appropriate design is required.

2. Analysis of Stable Oscillation Condition

In this section, the oscillation stability of the circuit shown in Fig. 1(b) is analyzed. We first focus on its similarity to the SRAM cell and its peripheral circuitry. Fig. 2 was created by redrawing Fig. 1(b). In this figure, the latch composed of the inverters IL1 and IL2 is regarded as an SRAM cell, I1 and I5 as write drivers, and I2 and I6 as sense amplifiers.

Using this SRAM analogy, a stable oscillation condition in the circuit can be recognized in the following conditions corresponding to the A1 and B1 nodes.



(a) Odd-stage inverters (b) Even-stage inverters with a latch

Fig. 1. Ring oscillator circuits using inverters.

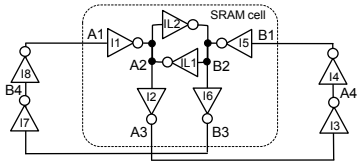


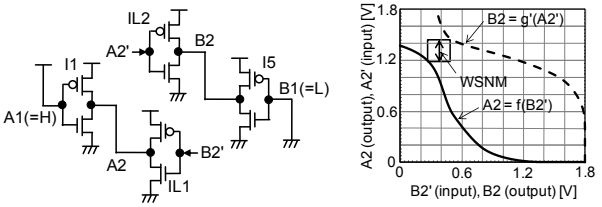
Fig. 2 The oscillator circuit re-drawn like an SRAM cell.

Case i) (A1, B1) = (H, L) or (L, H) : When the circuit keeps oscillating normally, the levels of the nodes (A1, B1) should always be either (H, L) or (L, H). In this case, the (A1, B1) signals must be transmitted to the SRAM-output nodes (A3, B3). In other words, data must be written into the SRAM cell composed of IL1, IL2.

Case ii) (A1, B1) = (H, H) or (L, L) : This state occurs when oscillation stops, or may occur instantaneously even during normal oscillation. To maintain stable oscillation, the data in the SRAM cell must be accessed without being destroyed, and both output nodes from the SRAM cell (A3, B3) must have different levels (i.e. A3≠B3). In other words, the SRAM cell data must be stable during (A1, B1) = (H, H) or (L, L) state.

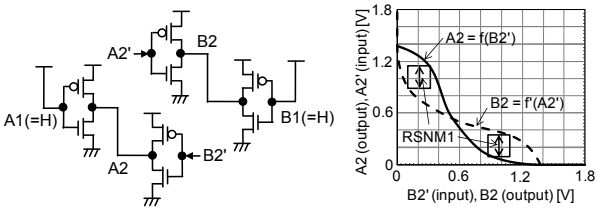
These two conditions for stable oscillation are equivalent to those for SRAM's write/read operations in terms of Static Noise Margin (SNM). Case i) corresponds to the condition where the Write Static Noise Margin (WSNM) > 0, and Case ii) corresponds to a Read Static Noise Margin (RSNM) > 0.

Fig. 3(a) shows the equivalent circuit to calculate the WSNM value for case i), and Fig. 3(b) shows the SPICE-simulated result for WSNM. In the SPICE simulation, a 0.18-um process technology with a supply voltage Vdd of 1.8V is assumed. Fig. 3(a) is extracted from the essential part of Fig. 2: I1, I5, IL1 and IL2 in which nodes A2 and B2 are divided and nodes A1 and B1 are set at H and L, respectively. The WSNM value can be calculated using the results of SPICE DC-analysis, which are B2 output voltage dependency on A2' input, and A2 output voltage dependency on B2' input in Fig. 3(b). Finally, the WSNM value is obtained as the distance between these two curves. Fig. 4 and Fig. 5 show the equivalent circuit to calculate the RSNM1 ((A1, B1) = (H, H)), RSNM2 ((A1, B1) = (L, L)) value in case ii), and the simulated result of RSNM1 and RSNM2,



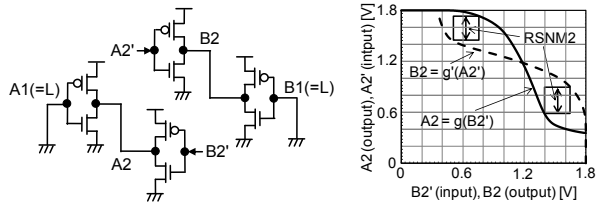
(a) Circuit (b) Result

Fig. 3. DC analysis for the (A1,B1)=(H,L) case.



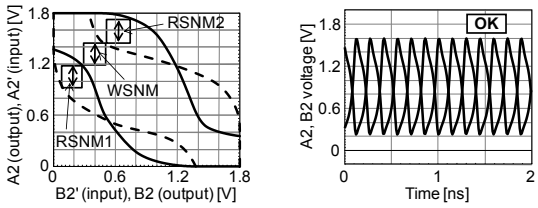
(a) Circuit (b) Result

Fig. 4. DC analysis for the (A1,B1)=(H,H) case.



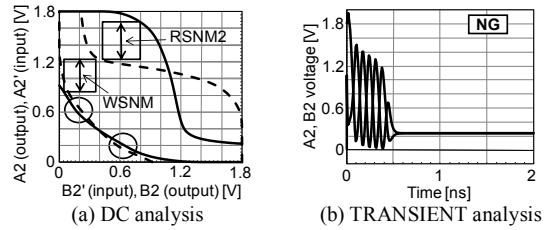
(a) Circuit (b) Result

Fig. 5. DC analysis for the (A1,B1)=(L,L) case.



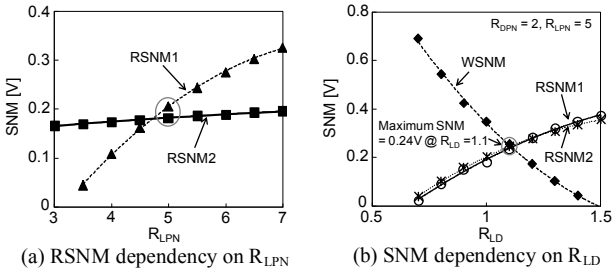
(a) DC analysis (b) TRANSIENT analysis

Fig. 6. Correlation between SNM (DC) and oscillation (TRANSIENT)



(a) DC analysis (b) TRANSIENT analysis

Fig. 7. Correlation between SNM (DC) and oscillation (TRANSIENT)



(a) RSNM dependency on R_{LPN} (b) SNM dependency on R_{LD}

Fig. 8. Optimization of the oscillator circuit.

respectively[2]. WSNM, RSNM1, and RSNM2 must all be designed to have positive values to enable the circuit to oscillate stably.

Fig. 6(a) summarizes the triple SNM (WSNM, RSNM1, RSNM2) characteristics in the same figure, and Fig. 6(b) shows the corresponding TRANSIENT analysis results displaying oscillating waveforms. Fig. 6 represents the case where the oscillation conditions are fully satisfied. On the other hand, Fig. 7 represents the case where one condition is not satisfied (RSNM1<0). The correlation between the WSNM, RSNM1, and RSNM2 values and the stability of oscillation is confirmed.

3. Optimal Design Method

In this section, the optimal design method for the oscillators is discussed using the triple SNM concept described in Section 2. There are three circuit design parameters: (a) PMOS / NMOS transistor size ratio in the delay inverter (R_{DPN}), (b) PMOS / NMOS transistor size ratio in the latch inverter (R_{LPN}), (c) NMOS in the latch / NMOS in the delay transistor size ratio (R_{LD}).

The optimization strategy is as follows: First, the R_{DPN}, which is a core parameter of the delay line, is set to 2 to minimize the propagation delay time and layout design convenience. Then, R_{LPN} and R_{LD} are determined to maximize three kinds of SNMs. It can be reasonably assumed that the maximum operational margin is obtained when the total voltage margins are assigned equally to each SNM. Next, the dependency of RSNM1 and RSNM2 on R_{LPN} are examined. As shown in Fig. 8(a), we can adjust the RSNM1 / RSNM2 ratio appropriately. The optimal value of R_{LPN} is set to 5, where RSNM1 / RSNM2 is nearly equal to 1. Then, the WSNM, RSNM1, and RSNM2 dependency on R_{LD}, are evaluated as shown in Fig. 8(b). It can be seen that the oscillation margin is ensured in the range of R_{LD} = 0.6 ~ 1.5, and obtains the maximum SNM value (= 0.24V) at R_{LD} = 1.1. The ideal upper limit value of SNM is 0.3V, which is the 1/3 of a half Vdd (1.8/2 = 0.9V). At this optimal design, each SNM value achieved 80% of the ideal value. Consequently, we obtain R_{LD}=1.1 ± 45% (0.6 ~ 1.5) when R_{DPM} = 2, R_{LPN} = 5 as the optimal ratio for the oscillator.

4. Conclusion

The oscillation conditions and the quantitative operation margins for CMOS ring oscillators composed of even-stage inverters are analyzed noticing the similarity between the oscillator and SRAM cell circuitry. Optimal design method to maximize the triple Static Noise Margins is provided to ensure stable oscillation.

Acknowledgements

The physical design parameters for VLSI design were provided through VLSI Design and Education Center (VDEC), the University of Tokyo, in collaboration with Rohm Corporation and Toppan Printing Corporation. This research was partially supported by funds from the Japanese Ministry: MEXT via the Kyushu knowledge-based cluster project. The authors thank NEC Micro Systems, LTD. for their useful suggestions.

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