A Vth-Shiftable SRAM Cell TEGs for Direct Measurement for the immunity of the Threshold Voltage Variability

V_{th}-shiftable SRAM Cell TEGs for Direct Measurement for the Immunity of the Threshold Voltage Variability

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1. Introduction

For SRAM using state-of-the-art processes of deep sub-micron generation, it is becoming difficult to secure operating margins due to the lowering of power supply voltage and the increase in the device characteristic variation [1][2]. To overcome this problem, we proposed the ratio-less SRAM (RL-SRAM) design [3][4]. In order to demonstrate the immunity of the ratio-less SRAM operation for the device characteristic variability by the measurement, we also developed MOSAIC SRAM cell TEGs with intentionally-added device variability within the gate width [5]. However, the immunity for the device variability in the threshold voltage (V_{th}) of MOSFETs has not been evaluated by the measurement. Therefore, we newly developed the V_{th}-shiftable SRAM cell TEGs (VTSTs).

2. Design of V_{th} shiftable SRAM Cell TEG

Figure 1 shows a simple model for V_{th}-shifts in the MOSFETs in a 6 transistor SRAM (6T-SRAM) Cell. Each MOSFET may have the inherent V_{th}-shift caused by the device characteristic variabilities. Figure 2 shows the developed VTST for 6T-SRAM. In this structure, the all gate terminals of MOSFETs are extracted to the chip boundary and tapped to analog I/O (AIO) buffers. Six external voltage sources (EVSs) are employed to apply the V_{th}-shift to each MOSFET. The arbitral V_{th}-shift value and its polarity can be manipulated by the EVS. Figure 3 shows the photo and layout of our developed VTST for 6T-SRAM using the 0.18µm CMOS process.

3. Measured Results and Discussions

In the evaluation of measured results of the VTST, we defined fail condition map (FCM) which summarizes all the combinations of the polarity setting for a V_{th}-shift. Since the V_{th}-shift for each MOSFET can be set to ($+\Delta V_{th}$ or $-\Delta V_{th}$), the total number of combinations for the measurement is 64 ($= 2^6$) for the 6T-SRAM cell. Figure 4 shows the FCM for the voltage shift values of ±0.15V for 6T-SRAM. The one cell in FCM indicates one combination of the polarities ($+\Delta V_{th}$ or $-\Delta V_{th}$) of six transistors of which an SRAM cell is composed. For example, in the left and the upper corner cell in FCM in Fig.4, the V_{th}-shifts for all six MOSFETs are set to -0.15V. In the FCM, white colored cells and gray colored cells mean the combination of V_{th}-shifts is operable (Pass) as SRAM cell or not operable (Fail), respectively. In the Fig. 4, we can recognize the 6 combinations of the polarities of V_{th}-shift of ±0.15V are not operable. Figures 5 and 6 show the measured FCMs for the V_{th}-shift values of 0.25V and 0.3V, respectively.

Figure 7 summarizes the total counts of the fail conditions of FCMs versus the V_{th}-shifts ($|\Delta V_{th}|$) and the supply voltages (V_{dd}). This figure means the maximum limit of $|\Delta V_{th}|$ for 6T-SRAM operation is 0.1V or less. Here we defined the Critical V_{th} ($C\Delta V_{th}$) as the maximum limit of V_{th}- shift for stable SRAM operation. Figure 8 shows the detail of relationship between the $C\Delta V_{th}$ and the supply voltage. From the results of FCMs in Figs. 4-6, the V_{th}-shifts of N3 and N4 tend to decide the $C\Delta V_{th}$. This is because the higher V_{th}-shifts of N3 and N4 prevents the write operation.

4. Conclusion

We developed VTST for 6T-SRAM and evaluated the influences of SRAM operation by threshold voltage fluctuation using measured FCMs and $C\Delta V_{th}$s. The VTST for the ratio-less 12 transistor SRAM (RL-12T-SRAM) was also developed as shown in Fig.12, however the number of combinations of 4096($=2^{12}$) for an FCM is too huge to finish the measurement by manual operation. Therefore now we are trying to construct the automated measurement environment for the RL-12T-SRAM VTST. Figure 10 includes the simulated $C\Delta V_{th}$ for RL-12T-SRAM, however we will obtain the similar measurement results for RL-12T-SRAM soon.

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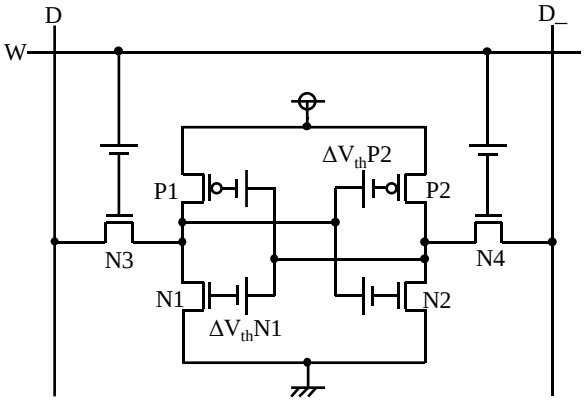

Figure 1: Model of V_{th}-Shifts in 6T-SRAM Cell

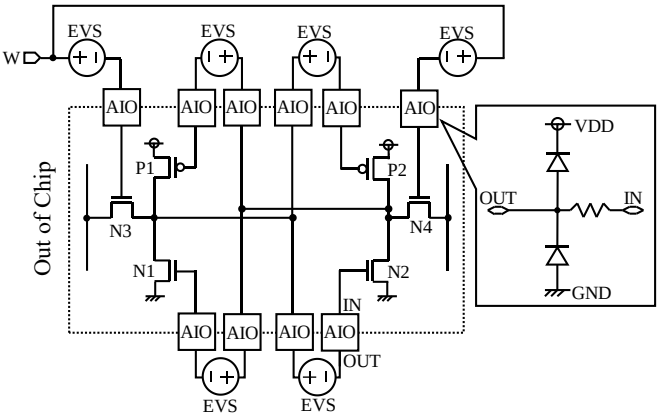

Figure 2: Structure of V_{th}-shiftable SRAM Cell TEG (VTST)

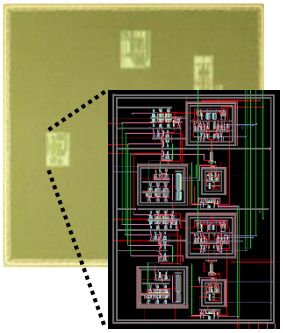

Figure 3: Photo and Layout of VTST for 6T-SRAM

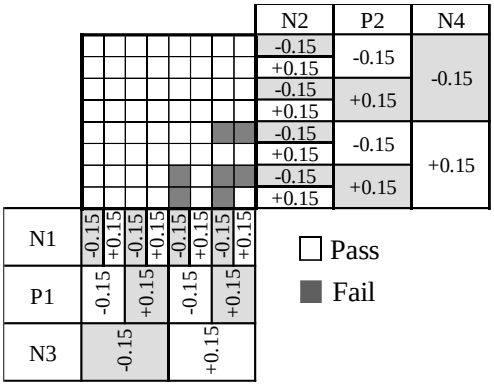

Figure 4: Fail Condition Map (FCM) for ΔV_{th}=±0.15V and V_{dd}=1.8V

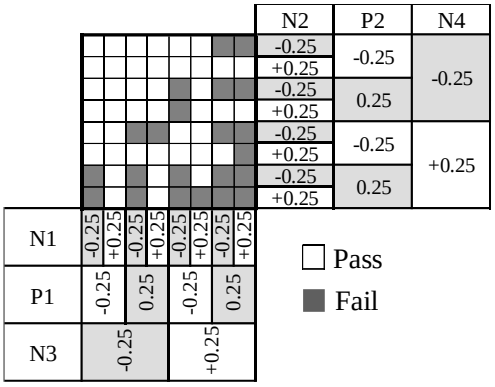

Figure 5: FCM for ΔV_{th}=±0.25V and V_{dd}=1.8V

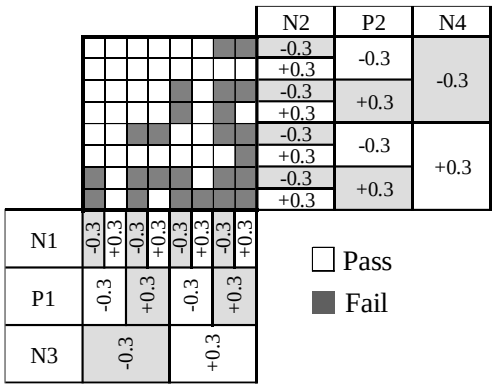

Figure 6: FCM for ΔV_{th}=±0.3V and V_{dd}=1.8V

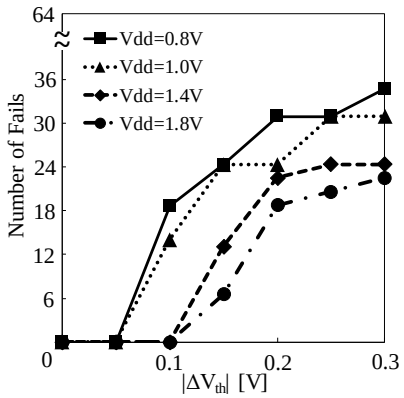

Figure 7: Number of Fail Conditions versus ΔV_{th} and V_{dd}

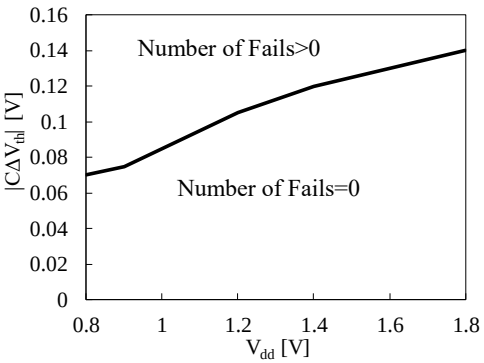

Figure 8: Measured Critical-ΔV_{th} versus V_{dd}

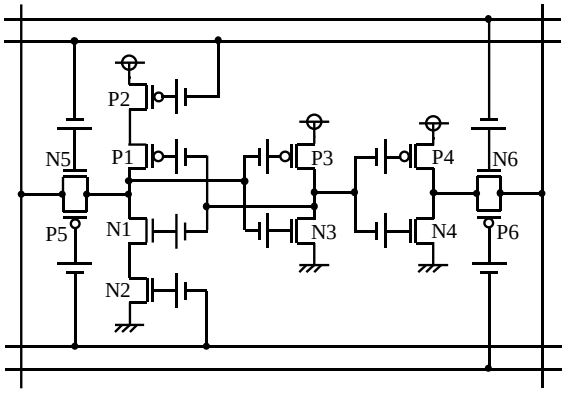

Figure 9: Model of V_{th}-Shifts RL-12T-SRAM Cell

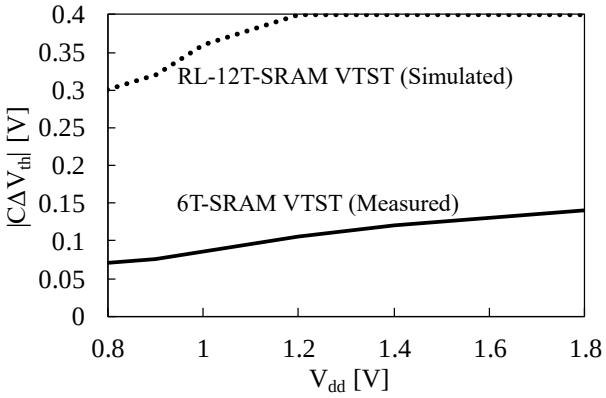

Figure 10: Comparison of CV_{th} for 6T-SRAM and RL-12T-SRAM