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Summary

The measurement system in which the Monte Carlo analysis of SRAM operation can be performed in actual measurement was developed. The measured results of the Monte Carlo analysis for SRAM function test and the static noise margin evaluation were agreed well with the simulated results. The proposed method can compactly cope with the recently proposed SRAM with a larger number of transistors.

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1. Introduction

For SRAM using state-of-the-art processes of deep sub- micron generation, it is becoming difficult to secure operating margins such as static noise margin (SNM) due to the lowering of power supply voltage and the increase in the device characteristic variation [1]. To overcome this problem, we had proposed the 12-transistor ratio less SRAM (RL-SRAM) design [2][3]. In order to demonstrate the immunity of the RL-SRAM operation for the device characteristic variability by the measurement, we had developed MOSAIC SRAM cell TEGs with intentionally added device variability within the gate width [4]. We had also developed the Vth shiftable SRAM cell TEGs (VTSTs) to demonstrate the immunity for the device variability in the threshold voltage (Vth) of MOSFETs [5]. Figures 1 shows simple models for Vth-shifts in the MOSFETs in 6T-SRAM cell. Each MOSFET may have the inherent Vth-shift caused by the device characteristic variability. Figure 2 shows the VTST for 6T-SRAM in which the all gate terminals of MOSFETs are extracted to the chip boundary and tapped with the analog I/O (AIO) buffers. In our previous research, six external voltage sources (EVSs) were manipulated to apply the fixed Vth-shift to each MOSFET to evaluate the fail condition maps (FCMs) and critical-Vths [5]. In this paper, we construct the advanced measurement system to evaluate the statistical operation margin for SRAM in measurement, as well as the Monte Carlo analysis in SPICE simulation.

2. Dynamic V_{th}-shift Circuit

The Monte Carlo analysis performed in the SPICE is to repeat simulations by randomly modifying design values to be on the Gaussian distribution. In our previous research as shown in Fig. 3(a), the Vth-shift was set manually by using multiple EVSs, however, in order to perform the Monte Carlo analysis in measurement, it is necessary to automate the setting of the individual Vth-shift values. Therefore, as shown in Fig. 3 (b), we employ only one programmable EVS (P-EVS) that generates Vth-shift values that are successively charged in target capacitors connected to the gates of the respective MOSFETs. In this method, EVSs as many as the number of transistors are not required, and further, it is possible to avoid influences such as characteristic variations among the EVSs. Fig. 4 shows the time dependence of the discharge characteristics of some capacitance components. Since mechanical relays are used in our measurement system to switch connections, the retention time of sub-second order is required. For that purpose, an aluminum electrolytic capacitor of 1000-μF or more should be employed. Figure 5 shows a dynamic Vth-shift circuit (DVSC) for setting individual Vth-shift voltages for each MOSFET. It consists of an electrolytic capacitor (Cvs) and two double-pole double-throw (DPDT) mechanical relays (MR1 and MR2). The input voltage of the DVSC is supplied by the common P-EVS with the values of the Gaussian distribution. Then it applies to the Cvs in DVSC via MR1 to store the respective Vth-shift by the charge select (CS) signal (Fig.5 (a)). Since the aluminum electrolytic capacitor is the polarized electronic component, the second DPDT relay (MR2) controlled by the polarity select (PS) signal is further required to support the negative Vth-shifts (Fig.5 (b)).

3. SRAM Function Test

Figure 6 shows a configuration diagram for performing Monte Carlo analysis for the SRAM function test using the VTST. Six DVSCs are connected to the gate of six transistors in the VTST. By sequentially selecting DVSCs, the Vth shift value of the Gaussian distribution is set for each MOSFET. Then the function test is performed by LSI tester. By repeating this procedure, Monte Carlo analysis is performed by actual measurement. Figure 7 shows the results of the Monte Carlo analysis in which the function test was repeated 2000 times. The measurement and the simulation results agree well with in both Vdd = 1.8 V and Vdd = 0.6 V.

4. Static Noise Margin Analysis

In the design of the SRAM memory cell, SNM evaluation (so-called Butterfly Curve) is commonly used to confirm its operation margin. Our measurement system is also applicable to the SNM evaluation. Using three DVSCs as shown in Fig. 8, the DC input / output characteristics of an inverter consisting the SRAM cell can be repeatedly measured. Figures 9 (a) and (b) show the butterfly curves obtained by the simulation and measurement, respectively. Figure 10 summarizes the relationships between the Vth-shift for one standard deviation (1σ) and the SNM. In both results, the simulation result and the measurement result very well agree with each other. It was confirmed that the Monte Carlo analysis similar to the simulation could be performed by actual measurement.

5. Conclusions

We have successfully achieved the Monte Carlo analysis for SRAM in actual measurement using VTST, P-EVS and DVSCs. Since our proposed method shares the P-EVS, it can compactly cope with SRAM having a larger number of transistors which are proposed in recent years.

Acknowledgements

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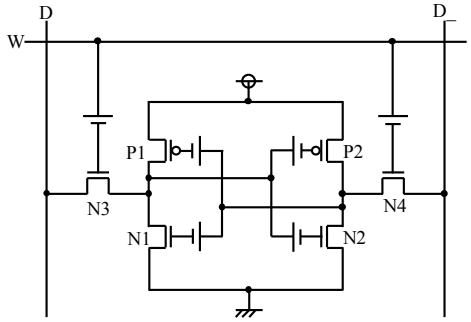


Fig. 1 Model of Vth-shifts in 6T-SRAM

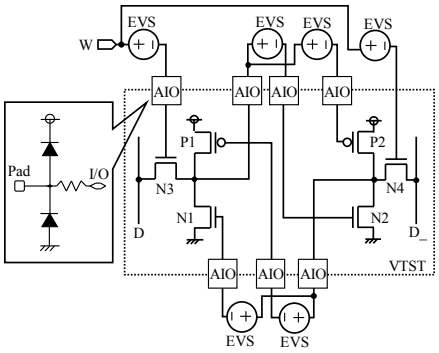
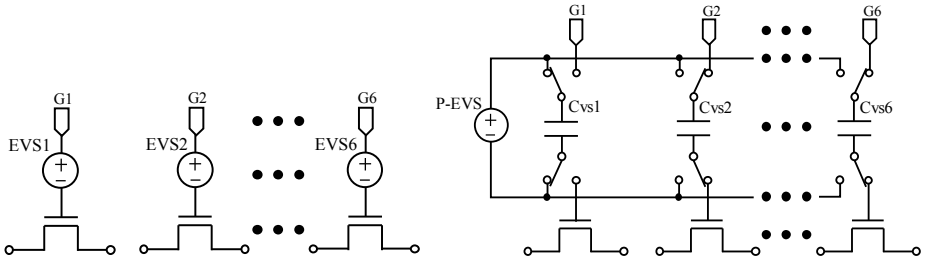


Fig. 2 VTST for 6T-SRAM



(a) with Multiple EVSs (b) with Programmable EVS (P-EVS) and capacitors

Fig. 3 Vth-shift settings for MOSFETs

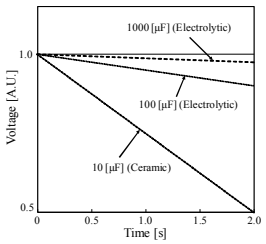
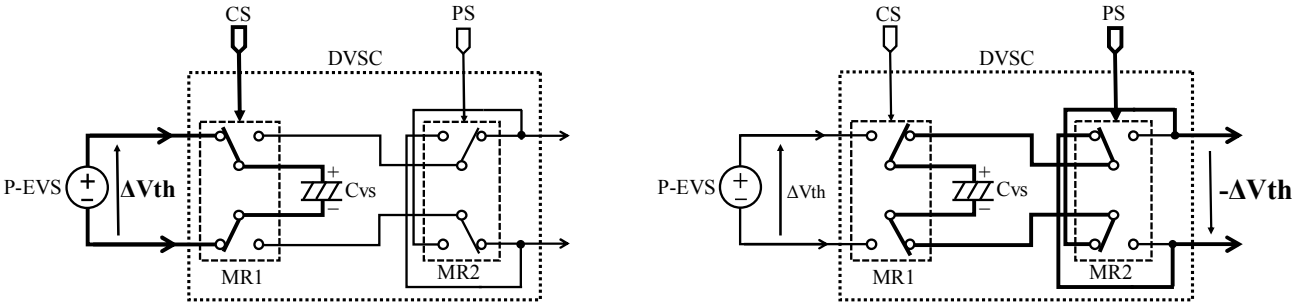


Fig. 4 Discharge characteristics for capacitor components



(a) Precharge for Cvs (b) Polarity selection

Fig. 5 Dynamic V_{th}-shift circuit (DVSC)

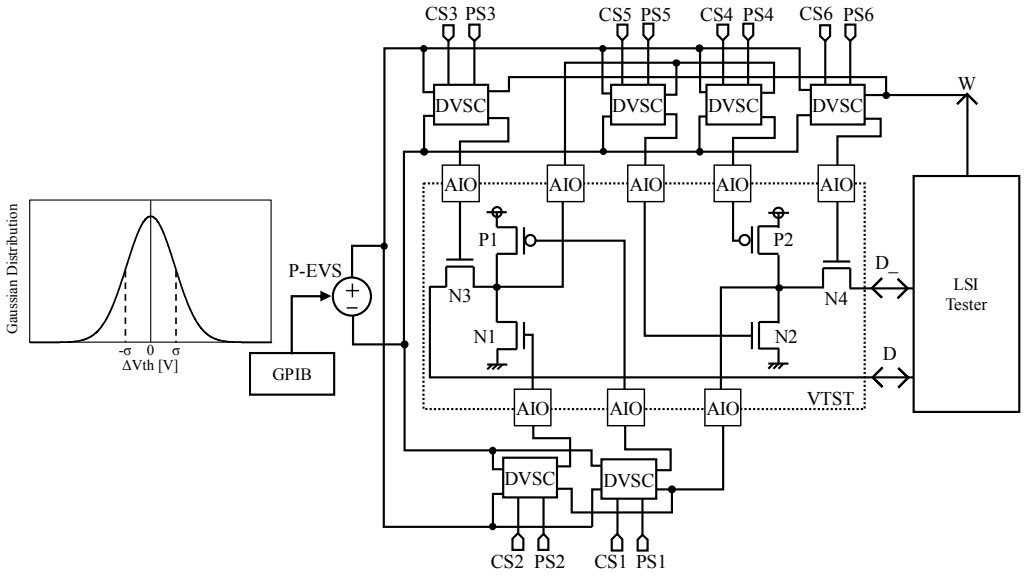


Fig. 6 Configuration for SRAM function test

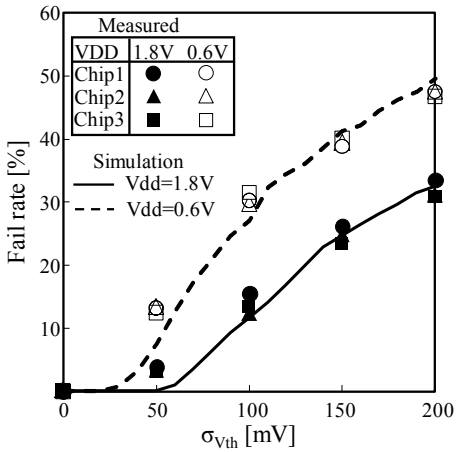


Fig. 7 Result of Monte Carlo analysis of SRAM function test (Frequency = 100 Hz, N = 2000)

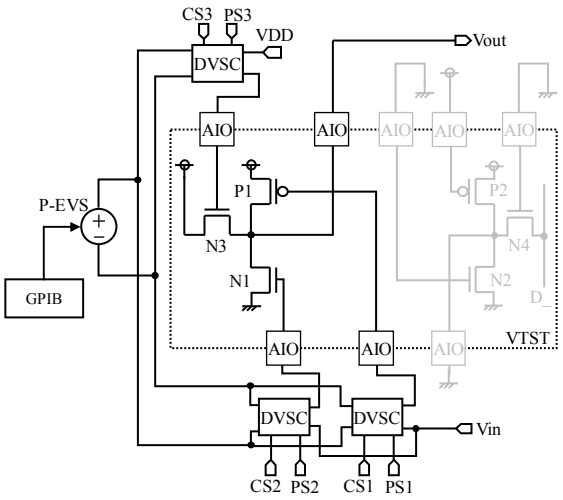
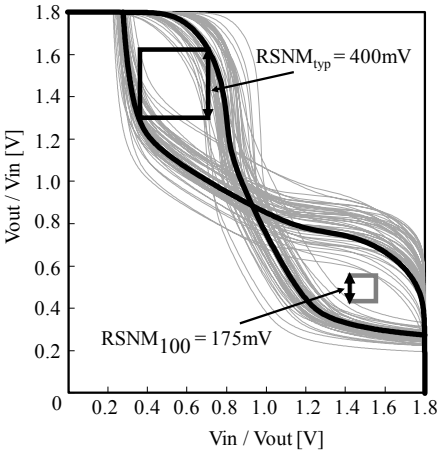
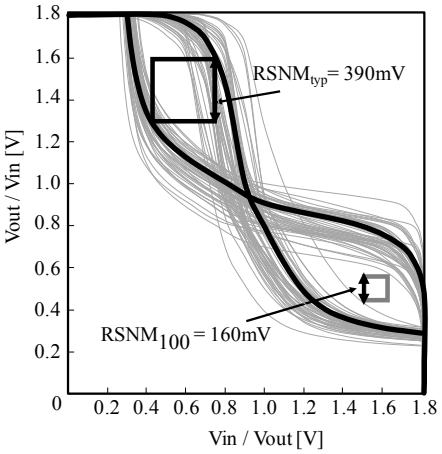


Fig. 8 Configuration for SNM Measurement



(a) Simulated



(b) Measured

Fig. 9 Butterfly Curves for SRAM cell (Vdd = 1.8 V, σ_{Vth} = 0.1 V, N = 100)

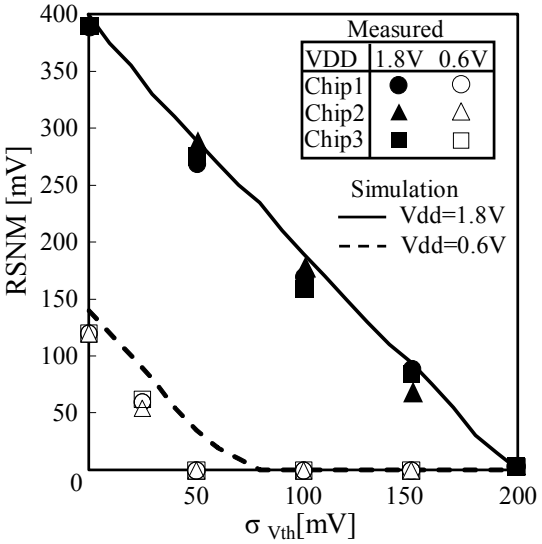


Fig. 10 Result of Monte Carlo analysis of SNM