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Summary

In order to demonstrate the immunity of the 12-transistor ratio-less SRAM operation for the variability of the threshold voltage (V_{th}) of MOSFETs by the measurement, we developed the V_{th}-shiftable SRAM cell TEGs (VTSTs). The measured results are discussed by the fail condition maps (FCMs) and the maximum limit of V_{th}-shift for stable SRAM operation.

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1. Introduction

For SRAM using state-of-the-art processes of deep sub-micron generation, it is becoming difficult to secure operating margins due to the lowering of power supply voltage and the increase in the device characteristic variation [1][2]. To overcome this problem, we proposed the 12-transistor ratio-less SRAM (RL-SRAM) design [3][4]. In order to demonstrate the immunity of the ratio-less SRAM operation for the device characteristic variability by the measurement, we developed MOSAIC SRAM cell TEGs with intentionally-added device variability within the gate width [5]. However, the immunity for the device variability in the threshold voltage (V_{th}) of MOSFETs has not been evaluated by the measurement. Therefore, we newly developed the V_{th}-shiftable SRAM cell TEGs (VTSTs).

2. Design of V_{th}-shiftable SRAM Cell TEGs

Figures 1 and 2 show simple models for V_{th}-shifts in the MOSFETs in a 6-transistor SRAM (6T-SRAM) cell and the 12-transistor ratio-less SRAM (RL-SRAM) cell, respectively. Each MOSFET may have the inherent V_{th}-shift caused by the device characteristic variability. Figure 3 shows the developed VTST for 6T-SRAM. In this structure, the all gate terminals of MOSFETs are extracted to the chip boundary and tapped to analog I/O (AIO) buffers. Six external voltage sources (EVSs) are employed to apply the V_{th}-shift to each MOSFET. The arbitral V_{th}-shift value (ΔV_{th}) and its polarity can be manipulated by the EVS. Figure 4 shows the VTST for the RL-SRAM with the polarity switching circuits (PSCs) that are employed to achieve the computerized polarity switching of the EVSs. Figure 5 shows the photo of developed VTSTs for 6T-SRAM and RL-SRAM using the 0.18μm CMOS process.

3. Measured Results and Discussions

In the evaluation of measured results of the VTST, we defined the fail condition map (FCM) which summarizes all the combinations of the polarity setting for a V_{th}-shift. Since the V_{th}-shift for each MOSFET can be set to ($+\Delta V_{th}$ or $-\Delta V_{th}$), the total number of combinations for the measurement are 64 ($= 2^6$) for the 6T-SRAM cell and 4096 ($=2^{12}$) for the 12-transistor RL-SRAM cell, respectively. Figure 6 shows the FCM for the V_{th}-shift values of ±0.15V for the 6T-SRAM. The one cell in FCM indicates one combination of the polarities ($+\Delta V_{th}$ or $-\Delta V_{th}$) of six transistors of which an SRAM cell is composed. For example, in the left and the upper corner cell in FCM in Fig.6, the V_{th}-shifts for all six MOSFETs are set to -0.15V. In the FCM, white colored cells and dark gray colored cells mean the combination of the V_{th}-shifts is operable (Pass) as SRAM cell or not operable (Fail) as SRAM cell, respectively. In the Fig. 6, we can recognize the 7 combinations of the polarities of V_{th}-shift of ±0.15V are not operable. Figures 7 and 8 show the measured FCMs for the V_{th}-shift values of ±0.25V and ±0.3V, respectively. From the results of FCMs in Figs. 6-8, the V_{th}-shifts of N3 and N4 tend to decide the operation. This is because the higher V_{th}-shifts of N3 and N4 prevent the write operation in the 6T-SRAM.

Figure 9 shows the FCM for the RL-SRAM for V_{dd}=1.8V, ΔV_{th}=±0.3V. In spite of the same setting of the Fig.8 for 6T-SRAM, it has no fail. Figures 10 and 11 show the FCMs for V_{dd}=0.8V. Since the number of combinations of 4096 for an FCM for the RL-SRAM is too huge to finish the measurement by manual operations, the automated measurement environment using PSCs as shown in Fig.4 was developed. Figures 12 and 13 summarize the total counts of the fail conditions of FCMs versus the V_{th}-shifts ($|\Delta V_{th}|$) for the 6T-SRAM and the RL-SRAM, respectively. Figure 12 means the maximum limit of V_{th}-shift for the 6T-SRAM is less than 0.15V even in the typical supply voltage (V_{dd}=1.8V). Here we defined the Critical ΔV_{th} ($C\Delta V_{th}$) as the maximum limit of $|\Delta V_{th}|$ for stable SRAM operation. Figure 14 summarizes the detail of the relationship between the $C\Delta V_{th}$ and the supply voltage for the 6T-SRAM and RL-SRAM, respectively. The fail in the RL-SRAM can be observed just in the less than half of the typical supply voltage.

4. Conclusion

We developed VTSTs for 6T-SRAM and RL-SRAM and evaluated them to investigate the influences of SRAM operation by Vth fluctuation using measured FCMs and $C\Delta V_{th}$s. As a result, we successfully confirmed the superior immunity of V_{th} fluctuation of the RL-SRAM than the 6T-SRAM.

Acknowledgements

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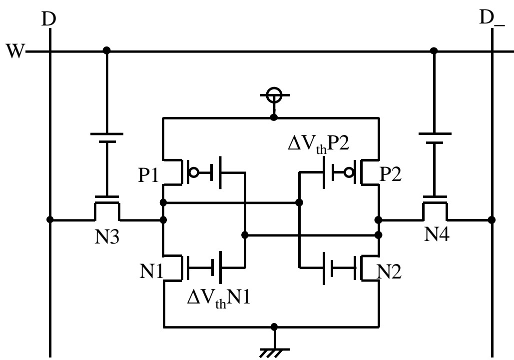

Figure 1: Model of V_{th}-shifts in 6T-SRAM Cell

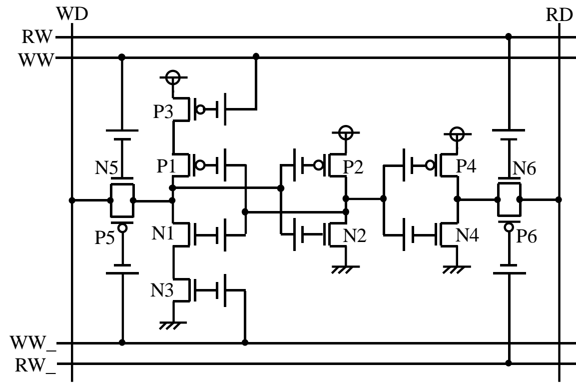

Figure 2: Model of V_{th}-shifts RL-SRAM Cell

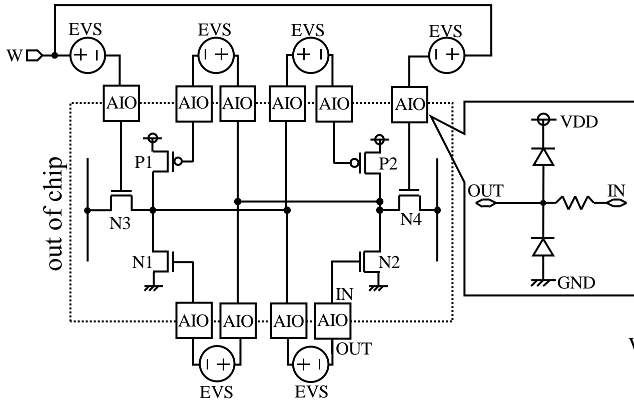

Figure 3: Structure of VTST for 6T-SRAM

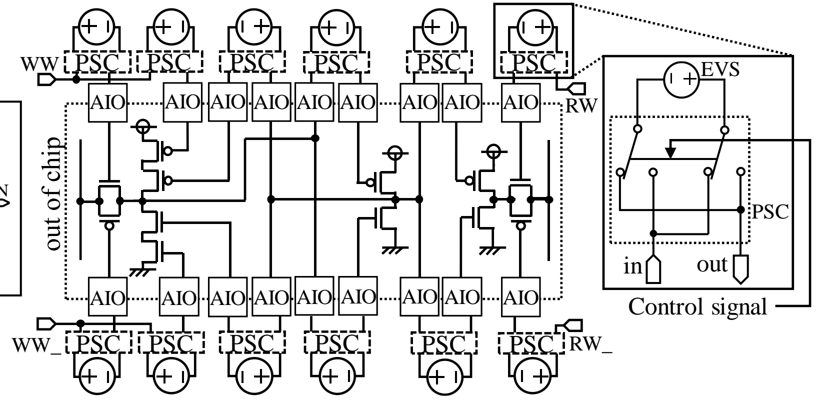

Figure 4: Structure of VTST for the RL-SRAM

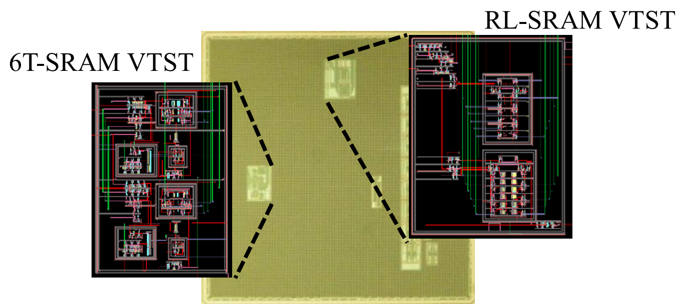

Figure 5: Chip Photo of the Developed VTSTs

N4	P2	N2								
		N1	-0.15	+0.15	-0.15	+0.15	-0.15	+0.15	-0.15	+0.15
		P1	-0.15		+0.15		-0.15		+0.15	
		N3	-0.15				+0.15			
-0.15	-0.15	-0.15	Pass	Pass	Pass	Pass	Pass	Pass	Pass	Pass
		+0.15	Pass	Pass	Pass	Pass	Pass	Pass	Pass	Pass
	+0.15	-0.15	Pass	Pass	Pass	Pass	Pass	Pass	Pass	Pass
		+0.15	Pass	Pass	Pass	Pass	Pass	Pass	Pass	Pass
+0.15	-0.15	-0.15	Pass	Pass	Pass	Pass	Pass	Pass	Fail	Fail
		+0.15	Pass	Pass	Pass	Pass	Pass	Pass	Pass	Pass
	+0.15	-0.15	Pass	Pass	Pass	Pass	Fail	Pass	Fail	Fail
		+0.15	Pass	Pass	Pass	Pass	Fail	Pass	Fail	Pass

□ Pass
■ Fail

Figure 6: FCM for 6T-SRAM (ΔV_{th}=±0.15V, V_{dd}=1.8V, Frequency=100Hz)

N4	P2	N2								
		N1	-0.25	+0.25	-0.25	+0.25	-0.25	+0.25	-0.25	+0.25
		P1	-0.25		0.25		-0.25		0.25	
		N3	-0.25				+0.25			
-0.25	-0.25	-0.25	Pass	Pass	Pass	Pass	Pass	Pass	Fail	Fail
		+0.25	Pass	Pass	Pass	Pass	Pass	Pass	Pass	Pass
	0.25	-0.25	Pass	Pass	Pass	Pass	Fail	Pass	Fail	Fail
		+0.25	Pass	Pass	Pass	Pass	Fail	Pass	Pass	Pass
+0.25	-0.25	-0.25	Pass	Pass	Fail	Fail	Pass	Pass	Fail	Fail
		+0.25	Pass	Pass	Pass	Pass	Pass	Pass	Pass	Fail
	0.25	-0.25	Fail	Pass	Fail	Pass	Fail	Pass	Fail	Fail
		+0.25	Fail	Pass	Fail	Pass	Fail	Fail	Fail	Fail

□ Pass
■ Fail

Figure 7: FCM for 6T-SRAM (ΔV_{th}=±0.25V, V_{dd}=1.8V, Frequency=100Hz)

N4	P2	N2								
		N1	-0.3	+0.3	-0.3	+0.3	-0.3	+0.3	-0.3	+0.3
		P1	-0.3		+0.3		-0.3		+0.3	
		N3	-0.3				+0.3			
-0.3	-0.3	-0.3	Pass	Pass	Pass	Pass	Pass	Pass	Fail	Fail
		+0.3	Pass	Pass	Pass	Pass	Pass	Pass	Pass	Pass
	+0.3	-0.3	Pass	Pass	Pass	Pass	Fail	Pass	Fail	Fail
		+0.3	Pass	Pass	Pass	Pass	Fail	Pass	Fail	Pass
+0.3	-0.3	-0.3	Pass	Pass	Fail	Fail	Pass	Pass	Fail	Fail
		+0.3	Pass	Pass	Pass	Pass	Pass	Pass	Pass	Fail
	+0.3	-0.3	Fail	Pass	Fail	Fail	Fail	Pass	Fail	Fail
		+0.3	Fail	Pass	Fail	Pass	Fail	Fail	Fail	Fail

□ Pass
■ Fail

Figure 8: FCM for 6T-SRAM (ΔV_{th}=±0.3V, V_{dd}=1.8V, Frequency=100Hz)

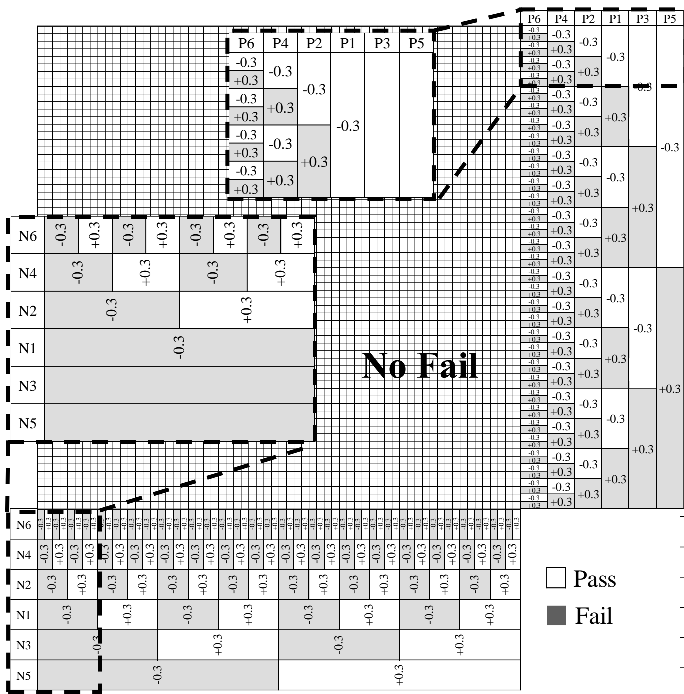

Figure 9: FCM for RL-SRAM (ΔV_{th}=±0.3V, V_{dd}=1.8V, Frequency=100Hz)

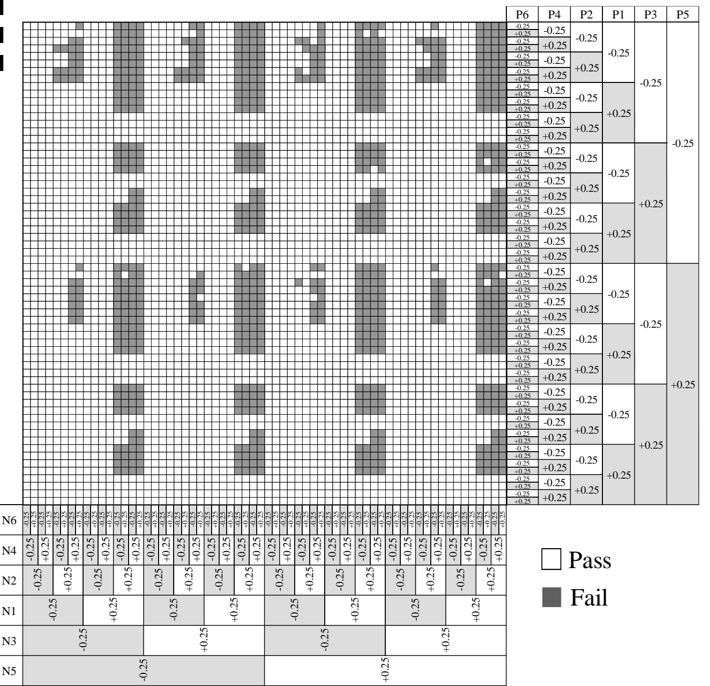

Figure 10: FCM for RL-SRAM (ΔV_{th}=±0.25V, V_{dd}=0.8V, Frequency=100Hz)

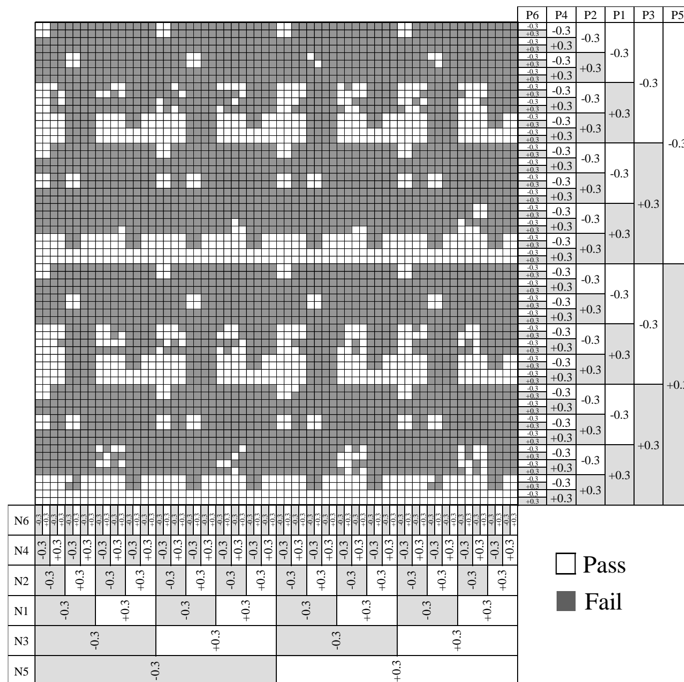

Figure 11: FCM for RL-SRAM (ΔV_{th}=±0.3V, V_{dd}=0.8V, Frequency=100Hz)

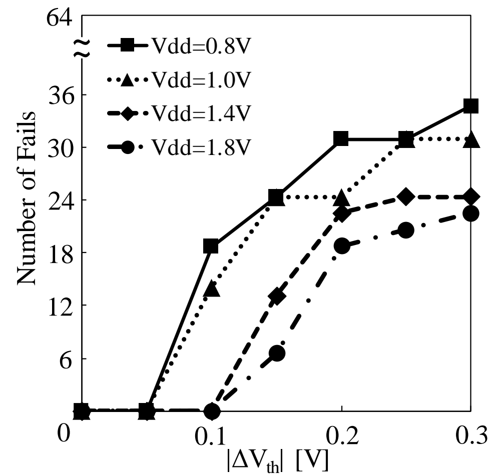

Figure 12: Number of Fail Conditions versus ΔV_{th} and V_{dd} (6T-SRAM)

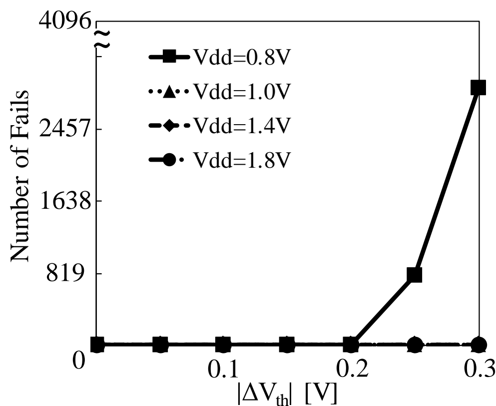

Figure 13: Number of Fail Conditions versus ΔV_{th} and V_{dd} (RL-SRAM)

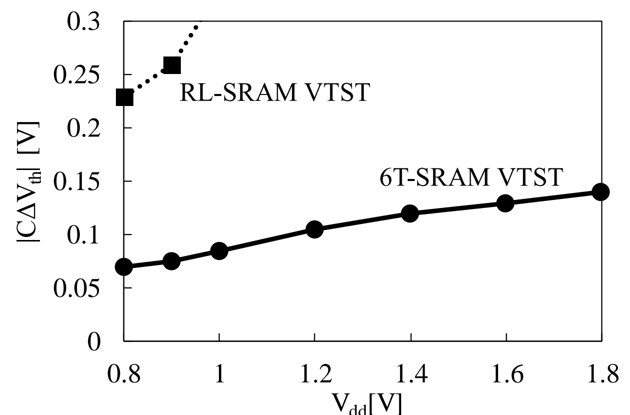

Figure 14: Comparison of $C\Delta V_{th}$