A Ratio-Less 10-Transistor Cell and Static Column Retention Loop Structure for Fully Digital SRAM

A Ratio-less 10-Transistor Cell and Static Column Retention Loop Structure for Fully Digital SRAM Design

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***Abstract*- In this paper, a new memory cell along with a new peripheral circuit for SRAM in ultra fine advanced process technologies is presented. A unique feature of the proposed circuit technique is its circuit design concept to achieve the fully digital ratio-less operation. This enables memory cell design that is free from consideration of the Static Noise Margin (SNM). Furthermore, it enables SRAM function without the restriction of transistor parameter (W/L) settings in circuit design and the dependency on local process variation. To achieve these unique features, we propose (1) a ratio-less memory cell in which the flip/flop loop can be broken in write operation and a push-pull tri-state buffer for secure read operation and (2) the configuration of a static Column Retention Loop (CRL) to prevent loss of memory cell data in the write half-select state. Combining these two key circuit techniques, a new SRAM circuit that is free from design restriction of SNM was developed. A 0.18-μm 1024-bit MOSAIC SRAM TEG consisting of memory cells having all combinations of gate sizes of 10 transistors differing by two orders of magnitude was developed and tested to verify the proposed circuits.**

I. INTRODUCTION

For SRAM using state-of-the-art processes of the deep sub-micron generation, it is becoming difficult to secure operational margins due to the lowering of the power supply voltage and the increase in local process variation. Figure 1(a) shows a conventional 6-transistor CMOS SRAM cell which has been widely used in the past and up to the present as the basic SRAM memory cell circuit. In this circuit, the write (flip/flop inversion) operation is performed from the outside through the impedance of the transfer transistors (SN1, SN2), while the read operation must be performed by outputting the stored information to the bit-lines through the same transfer transistors but without destroying the information in the flip/flop. In the design of the transfer gate transistors, therefore, there exist values of the margins of the upper and lower limit values that are permissible from considerations of impedances, and the ratio design of the so-called β-ratio and γ-ratio is thus required. As a method of quantitatively evaluating this design margin in SRAM cells, there is the Static Noise Margin (SNM) index [1]. There are two types of SNM, the read-SNM (RSNM) and write-SNM (WSNM), and the feasibility of operation of a memory cell is such that RSNM > 0 and WSNM > 0. In recent years, with device dimensions having become very small, it is becoming difficult to secure these two SNMs simultaneously, because they are subject to direct effects of the lowering of the power supply voltage and the increase in process variation among devices. A variety of techniques have been proposed to avoid this problem [2-8]. First, as an approach to improve characteristics

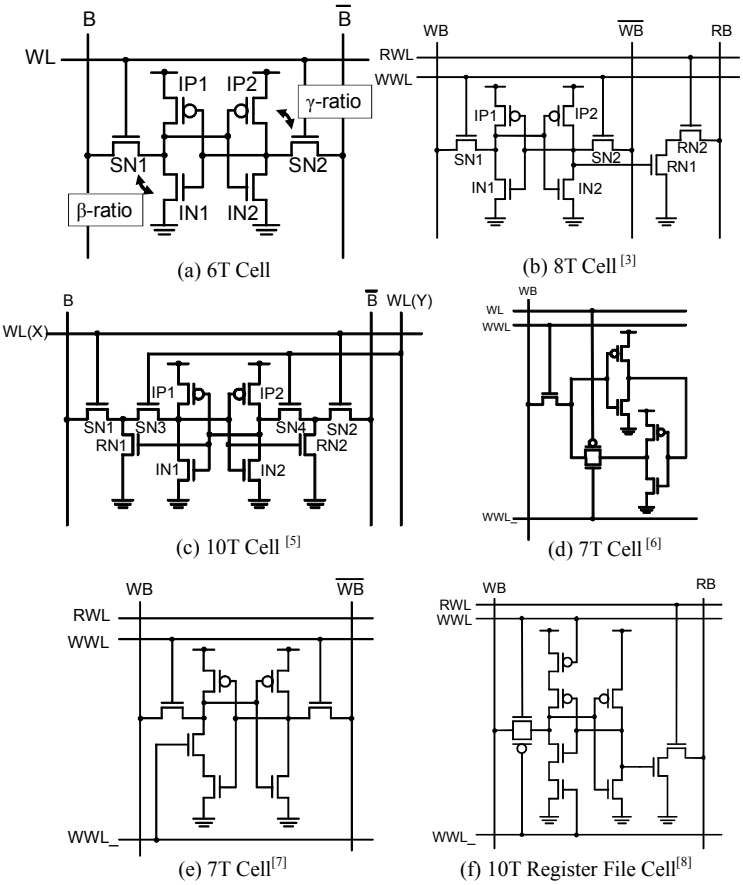


Fig.1 Memory Cells for SRAM

without increasing the number of transistors, there are many techniques to improve the values of RSNM and WSNM independently by optimizing the word line potential and/or the voltage of power supply of the memory cell during each of read and write operations; however, there remains the necessity of ratio design [2]. On the other hand, there are approaches to improve characteristics by adding transistors to the memory cell. A circuit named 8T-SRAM has been proposed (Fig. 1(b)) [3]. In this method, the RSNM may be freely set since it has a dedicated read buffer and it is also possible to design the read cell current without relation to ratio design. However, with 8T-SRAM there is a problem of half-selection during the write operation, and in order to avoid it, it is necessary to either combine it with the write-after-read technique in which the read operation is performed once before writing and the latched information is forwarded to the write bit line, or to further add transistors to support a

Table.1 Comparison of SRAM Memory Cells

Reference	Conv, [2]	[3]	[4]	[5]	[6]	[7]	[8]	***This work***
# of TRs	6Tr	8Tr	8Tr	10Tr	7Tr	7Tr	10Tr	***10Tr***
# of Word and Bit lines	1 + 2	2 + 3	2 + 3	2^{*1} + 2	3 + 1	3 + 2	3 + 2	***3 + 2***
Read Margin	RSNM > 0	***Free***	***Free***	***Free***	RSNM > 0	Free^{*2}	***Free***	***Free***
Write Margin	WSNM > 0	WSNM > 0	WSNM > 0	WSNM > 0	***Free***	***Free***	***Free***	***Free***
Write(halfSelect) Margin	RSNM' > 0	RSNM' > 0	***Free***	***Free***	***Free***	***Free***	N/A	***Free***
Flip/flop Loop Cutting	No	No	No	No	Yes	Yes	Yes	Yes
Peripheral Assist	Vword / Vcell		W.after.R			W.after.R		***CRL**^{*3}*

*1: Cross-point (XY) selected word lines, *2: Free in dynamic read operation , *3 No bit-line pre-charge required.

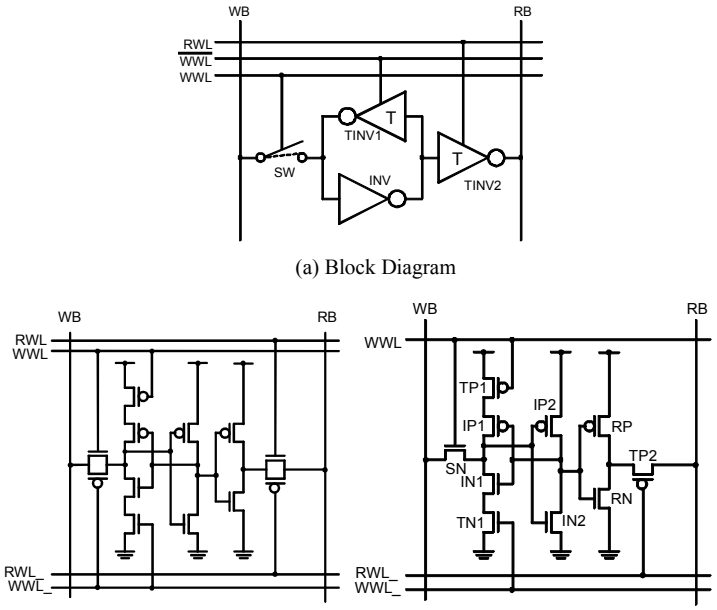
cross-point selection by the row(X) and column(Y) word lines as shown in Fig. 1(c) [4][5].

As a further different approach, a technique has been proposed to make the WSNM free by breaking the flip/flop loop that is usually constituted of two CMOS inverters [6] (Fig. 1(d)). With a similar concept, the 7T configuration shown in Fig. 1(e) which can temporarily make RSNM free as well by dynamically breaking the loop during read also has been proposed [7]. In other category, there is a 1-bit register file circuit as shown in Fig. 1(f) which is composed of ten transistors and may be considered to be a circuit that makes both the RSNM and WSNM free by breaking the flip/flop loop and having a dedicated read buffer like the 8T cell [8]. However, write-half-select operations are not presumed in the register file application, and therefore it cannot be directly applicable to an SRAM cell. It is also to be noted that pre-charge cycle is required before read operation.

The conventional techniques described above are summarized in Table 1. All the circuits proposed as SRAM cells require ratio design or dynamic control in the three states of write, read and write-half-select. Additionally, in the register file design, there is a lack of consideration for the write-half-select that is necessary for SRAM applications. It is expected that satisfying both RSNM and WSNM will be severely difficult for the existing circuit techniques due to the large local process variation in ultra-deep sub-micron technologies in the near future.

II. THE RATIO-LESS SRAM CELL

This paper proposes an SRAM cell and its peripheral circuit that make all three states of the read/write/write-half-select margin free. This SRAM cell is referred to as a ratio-less SRAM cell since its operation is secured regardless of the sizes of all the transistors. The basic block diagram of a memory cell with the proposed ratio-less configuration is shown in Fig. 2(a). The ratio-less cell comprises an input switch (SW), a latch inverter (INV), a tri-state inverter (TINV1) and an output tri-state inverter (TINV2). In a full complementary configuration, it would be a 12-transistor configuration with 4 word-lines and 2 bit-lines (12T, 4W, 2B) as shown in Fig. 2(b). Without assuming the ultra-low power supply voltage, the complementary transfer gate is not necessary. In this paper, the ratio-less 10T, 3W, 2B configuration having n-ch and p-ch transfer gates to have the same number of n-ch and p-ch transistors can symmetrically be laid out in a memory cell (Fig.2(c)) is discussed.



(a) Block Diagram

(b) 12T Full Complementary (c) 10T Single-channel Transfer Gate

Fig.2 Ratio-less SRAM Cell Topologies

III. STATIC COLUMN RETENTION LOOP STRUCTURE

The circuit operations of the ratio-less SRAM cell during hold, read and write are shown in Fig.3. In the hold state (Fig.3(a)), information is held by the Cell Local Loop (CLL) which consists of an inverter and the enabled tri-state-inverter in the memory cell. In read operation (Fig.3(b)), information is read out to a read bit-line through the dedicated read buffer circuit, which is tri-state-inverter interposed between the CLL and the read bit-line. Thus, hold and read out operation can be performed in a ratio-less and margin-free because these operations are independent of the transistor size and impedance of the bit-line. Also the stored information is never destroyed because the CLL is protected by the read buffer.

In the write operation (Fig.3(c)), there are write selected cell(s) and write half-selected cells. CLLs in both cases are broken while the write word-line is asserted. In write selected cell(s), this operation achieves the write operation to be ratio-less and margin-free. On the other hand, in write half-selected cells, the stored information must be lost because the CLL is broken. Therefore, we propose to form an alternative flip/flop loop: a Column Retention Loop (CRL) to

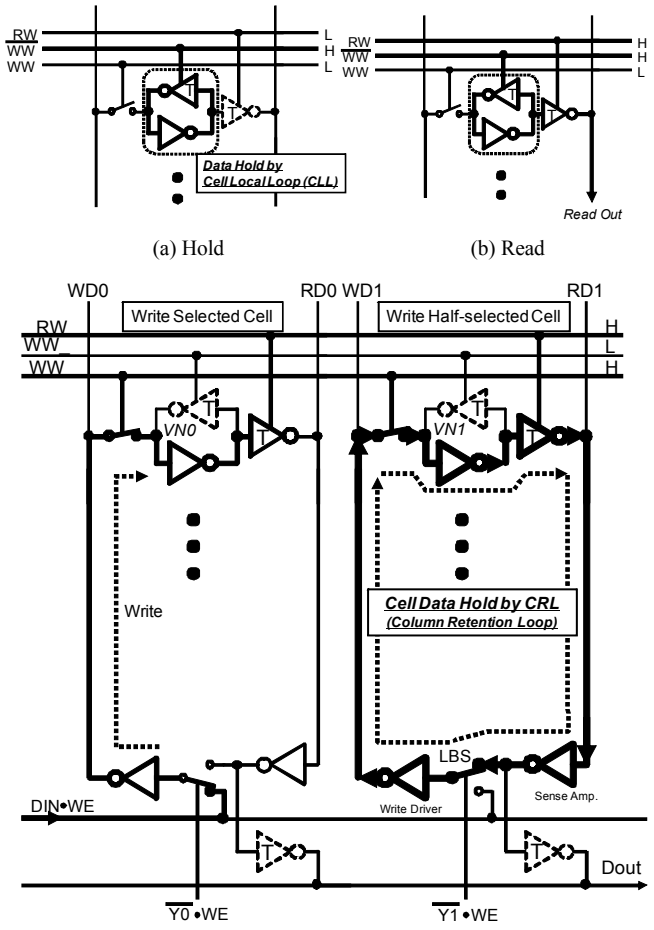


Fig.3 Ratio-less SRAM Operations

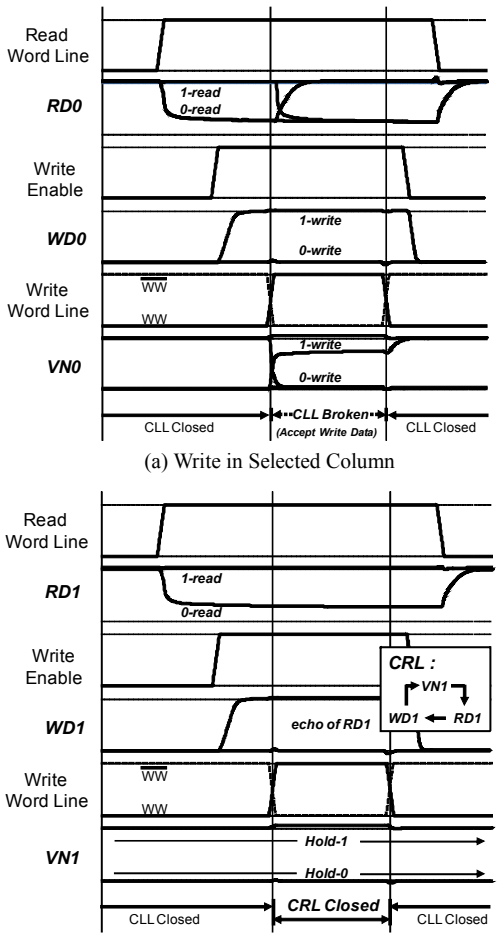
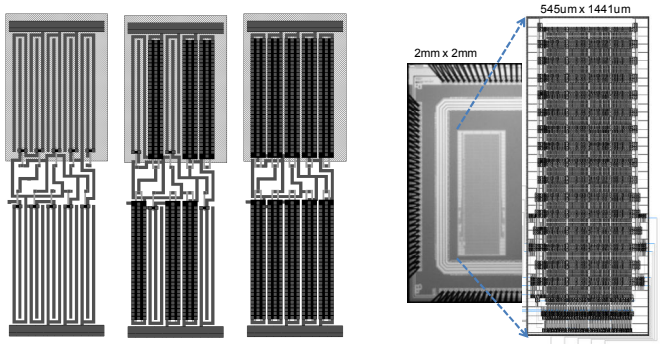


Fig.4 Simulated Waveforms

hold the information in the write half-selected columns on behalf of the broken CLL. A CRL is composed of read and write bit-lines, two inverters as the part of the memory cell, a read sense amp (an inverter), and a write driver (an inverter) as shown in Fig.3(c). Because we adopt the 10-transistor output push-pull ratio-less cell shown in Fig.2(c) for the memory cells, it enables to use a digital sense amplifier (just CMOS inverter) and helps to form the CRLs fully static. Note that the output stage of 10T Register File Cell shown in Fig.1(f) requires the bit line pre-charge and cannot be used with CRL. Figure 4 shows the simulated waveforms for write and write-half-select operations. First, the information held in memory cells is read out to the read bit-lines (RDs) by enabling the read word line. When the write enable signal is asserted to start the write operation, write data is transferred to the selected write bit-line (WD0). Then, the write word-line is asserted, the data in memory cell is securely updated in selected column because the CLL is cut. On the other hand, in write half-selected columns, the data on RDs are bypassed to WDs by enabling the loop back switch (LBS). Next, when the write word-line is asserted, the memory retention mechanism is switched from CLL to CRL. The information of the half-selected cells are successfully retained by transposing it to the static CRL. In this way, there is no need for a dedicated latch circuit such as that used in the write-after-read technique [4].

IV. DEVELOPMENT OF A TEST CHIP

In order to demonstrate by measurement the ratio-less operation of the proposed technique, we developed a 1024-bit MOSAIC SRAM TEG using 0.18μm CMOS in which the W value of each set of 10 transistors in a memory cell was varied by a range of two orders of magnitude. Our 1024-bit MOSAIC SRAM TEG includes the complete set of size combinations (the number of different designs are two to the tenth power, or 1024) as 1-bit memory cells. The cell layout examples are shown in Fig. 5(a)-(c). The sizes of the ten transistors composing a memory cell were designed to be either 0.3μm or 30μm. Cell_0 in Fig. 5(a) is the case in which all transistors have the minimum size of 0.3μm, Cell_1023 in Fig. 5(c) is the case in which all transistors have the maximum size of 30μm, and Cell_374 in Fig. 5(b) is an example of a mix of 0.3 and 30μm transistors. The area occupied when all transistors have the maximum (30μm) is secured as the size of the memory cell for all 1024 cells. To construct the 1024-bit MOSAIC SRAM TEG shown in Fig. 5(d), 1024 combinations for memory cells were automatically



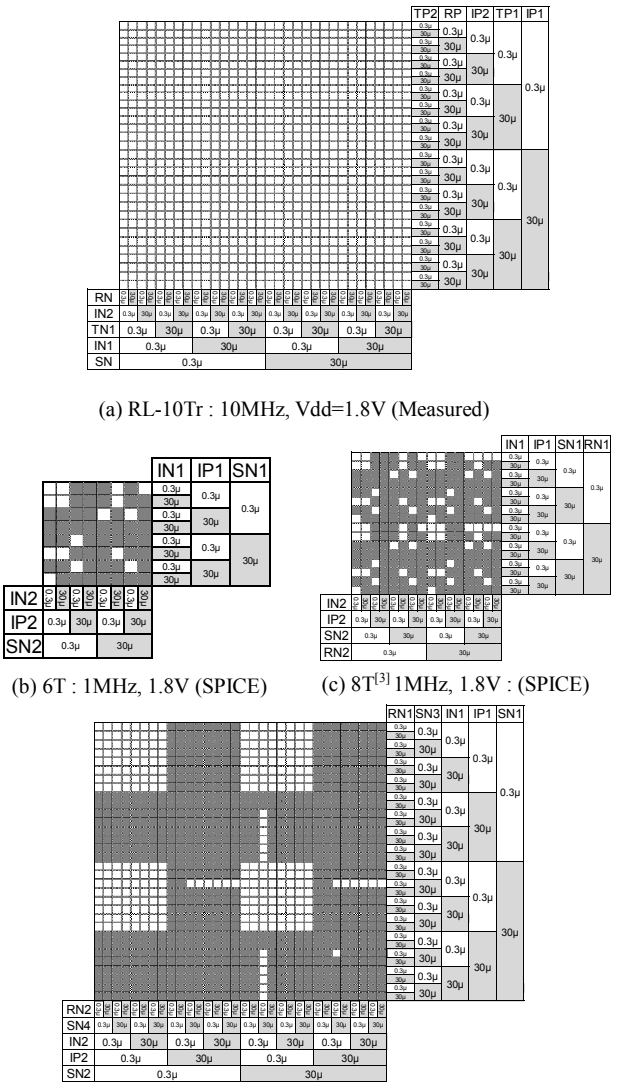
(a) Cell_0 (b) Cell_374 (c) Cell_1023 (d) 1024b Chip

Fig.5 Chip Photograph and Layout of MOSAIC SRAM TEG

generated.

V. MEASUREMENT RESULT

Figure 6(a) is a measured fail bit map (FBM) obtained by applying marching pattern tests to our MOSAIC SRAM including ratio-less 10T (RL-10Tr) cells. In the MOSAIC SRAM design, the position of the memory cell corresponds to the combination of transistor sizes as indicated to the right and bottom of the FBMs. Figures 6(b), (c) and (d) respectively show the results obtained in simulations of 6T SRAM, 8T SRAM and 10T SRAM designed like RL-10Tr MOSAIC SRAM. The hatched parts in the figures are failed cells. In our ratio-less SRAM, the operation of whole cells is experimentally confirmed at an operating frequency at 10MHz. In contrast, the results for 6T / 8T / 10T SRAMs show that there are many failed cells in spite of the low-operating frequency of 1MHz. Since these circuits require ratio design, many combinations are inoperative.



(a) RL-10Tr : 10MHz, Vdd=1.8V (Measured)

(b) 6T : 1MHz, 1.8V (SPICE)

(c) 8T[3] 1MHz, 1.8V : (SPICE)

(d) 10T[5] 1MHz, 1.8V : (SPICE)

Fig.6 Measurement Result of MOSAIC TEG and Comparison with 6Tr, 8Tr and 10Tr SRAMs

VI. CONCLUSION

This paper proposed a new SRAM circuit that comprises a ratio-less SRAM cell, which makes the securing of the SNM unnecessary in all read, write, and write-half-select states, and a static Column Retention Loop (CRL) configuration, which prevents the loss of information during write-half-select operation. To demonstrate the ratio-less operation, a 1024-bit MOSAIC SRAM TEG was developed, and it was confirmed that operation of the SRAM is independent of the size of transistors in the memory cell. This newly developed technique is expected to be a breakthrough for the integration density limitation of SRAMs using state-of-the-art processes due to the large local process variation. And it also has high affinity with the next-generation transistor, FinFET, since the W values for the memory cell can all be the same and a minimum.

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