An electrically adjustable 3-terminal regulator with post-fabrication level-trimming function

An Electrically Adjustable 3-Terminal Regulator with Post-Fabrication Level-Trimming Function

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Abstract - This paper describes a new technique for 3-terminal regulators to adjust the output voltage level without additional terminals or extra off-chip components. By applying a serial control pattern using the intermediate voltage level between the supply voltage and the regulator output, the adjustment data in the internal nonvolatile memory are safely updated without noise disturbance. In an on-board test with a chip fabricated using a 0.35-μm standard CMOS process, we confirm successful output voltage adjustment with sub-10mV precision.

I. Introduction

Recent LSIs require varying supply voltage levels to demonstrate their best performance in diverse electronic equipment. Moreover, lowering the supply voltage level requires higher precision in the supply voltage setting for 3-terminal regulator ICs, which are usually used to generate DC supply voltages for LSIs. To address these requirements, various techniques for 3-terminal regulators such as level correction with off-chip components, level trimming for wafer, or updating internal nonvolatile memory with additional terminals, etc, have been proposed[1][2][3][4]. These methods, however, increase costs, due to the extra off-chip components or additional terminals.

II. Adjustable Regulator System Design

A block diagram of the proposed 3-terminal regulator is shown in Fig. 1. This circuit has only 3 external terminals, supply voltage (VDD), ground (GND), and regulated voltage output (OUT). The parts enclosed within the dotted line form a feedback loop composed of an operational amplifier, an output transistor, and a voltage divider, as is the case in the conventional 3-terminal regulator. The reference voltage level can be adjusted depending on the data stored in the nonvolatile memory. As shown in Fig. 2(a), by forcing the OUT terminal voltage to exceed the regulator output level, the drain terminal of the output transistor enters the Hi-Z state, enabling it to pass the control signal into the circuit. The control signal, as shown in Fig. 2(b), consists of a sequence of 3 serial data patterns, namely, (1) high-frequency burst signal (10-MHz, >30-cycles), (2) low-frequency key pattern signal (250-Kbps, 6-bits), and (3) voltage-level adjustment code (250-Kbps, 8-bits), to prevent a malfunction in the circuit due to noise. The control signal is input via the Control Signal Detector, and then the Burst Detector checks whether or not the signal includes a burst signal. When a burst signal is detected, the Serial Interface Circuit begins the operation of verifying the signal with the pre-defined key pattern. If this verification succeeds, the contents of the nonvolatile memory are updated with the subsequent adjustment code, and finally the output voltage level is changed.

III. Circuit Design

Fig. 3 shows the Control Signal Detector and Burst detector. The Control Signal Detector includes a comparator, the comparison threshold level of which is set to a value between the regulated output level and supply voltage level. It also has a low-pass filter function that cuts off more than 33-MHz signal owing to the capacitor connected to the output node of the comparator. In the Burst Detector shown in Fig. 3, transition of the input signal is converted to the current Iu with fixed pulse width, by the function of a delayed inverter and an EXOR gate. The Iu pulse charges up the capacitor connected to the node BURST. On the other hand, the constant discharge current Id always discharges it. According to the setting of Id, the voltage of the node BURST can be increased for an input signal with frequency greater than the specified frequency (in this design, 7-MHz). The simulated waveforms of this circuit are shown in Fig. 4. The circuit was designed to recognize a continuous 30-cycle clock signal with a frequency of about 10-MHz as the burst signal.

Fig. 5(a) shows the Key Pattern Checker including Serial Interface circuit. The logical value of a serial pattern is determined by the pulse width. As shown in Fig. 5(b), using the Rise Delay Buffer, the data is regarded as "0" or "1" if the input signal pulse width is, respectively, shorter or longer than the time threshold Tth. Fig. 5(c) illustrates the circuit diagram for the Rise Delay Buffer. Since it has been designed with (Wp/Lp) << (Wn/Ln), the clock signal (CK) is not generated for an input signal with period less than Tth.

IV. Chip Fabrication and Measurement

A test chip was fabricated using a 0.35-μm standard CMOS process. A photograph of the chip and layout of the main circuit are shown in Fig. 6. Fig. 7 shows the measured waveform of the chip. After receiving the voltage adjustment data (11010101:LSB First), it can be confirmed that the output voltage level is successfully changed to 2.117V. Fig. 8 shows the measured output voltage for the adjustment code. An output voltage control step with 6.5-mV precision was confirmed. Table 1 summarizes the current dissipation and layout area for each block of our circuit. Considering that the output current and chip area of a general 3-terminal regulator are several hundred mA and several square mm, respectively, the current and area overheads are negligibly small.

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V. Conclusion

A technique enabling the output voltage of a 3-terminal regulator to be changed electrically without additional terminal pins has been proposed and verified. This feature can be utilized after packaging or implementation on a board, and thus satisfies the requirements of recent LSIs for diversity of supply voltage levels with higher precision.

Acknowledgments

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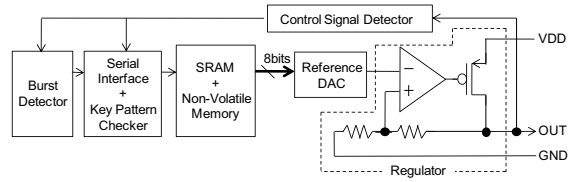

Fig. 1 Block diagram

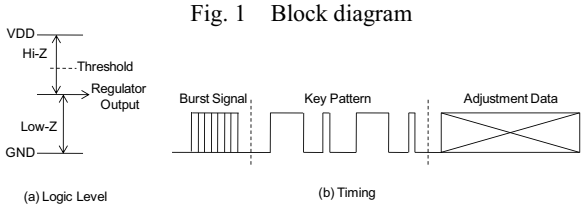

Fig. 2 Serial control signal format

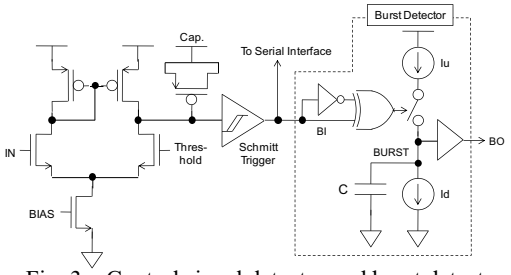

Fig. 3 Control signal detector and burst detector

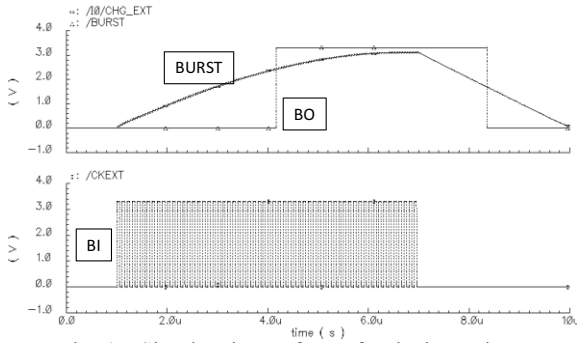

Fig. 4 Simulated waveforms for the burst detector

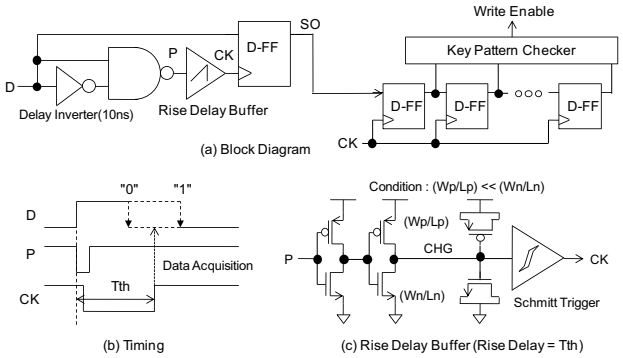

Fig. 5 Key pattern checker with serial interface circuit

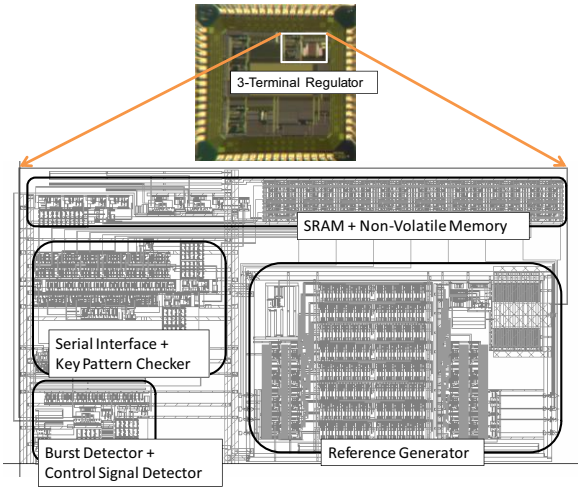

Fig. 6 Chip photograph and main circuit layout

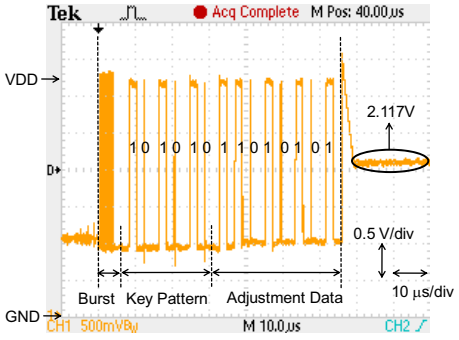

Fig. 7 Measured waveform

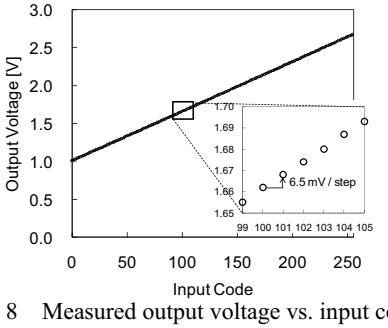

Fig. 8 Measured output voltage vs. input code

Table 1 Current and area for each circuit block

Block Name	Current [mA]	Area [mm^2]
Burst Detector + Control Signal Detector	0.246	0.017
Serial Interface + Key Pattern Checker	<0.001	0.037
SRAM + Non-Volatile Memory	0.161	0.033
Total	0.407	0.087